

N0434N

N-channel MOSFET 40 V, 100 A, 3.7 m Ω

R07DS0556EJ0200 Rev.2.00 2020.6.10

Features

• Low on-state resistance : $R_{DS (on)} = 3.7 \text{ m}\Omega$ MAX. ($V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$)

Low C_{iss}: C_{iss} = 5550 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)

• High current : I_{D(DC)} = ±100 A

RoHS Compliant

Quality Grade : Standard

• Applications : For high current switching

Ordering Information

Part No.	Package	Packing		
N0434N-S23-AY	TO-262, Pb-free Note1	50 pcs / Magazine (Tube)		

Note: 1. Pb-free means that this product does not contain lead in the external electrode.

Absolute Maximum Ratings ($T_A = 25^{\circ}C$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS} 40		V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±100	Α
Drain Current (pulse) Note2	I _{D(pulse)}	±400	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	119	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current Note3	las	55	Α
Single Avalanche Energy Note3	E _{AS}	300	mJ

Note: Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

Notes: 2. PW \leq 10 μ s, Duty Cycle \leq 1%

3. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{DD} = 25 V, V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

Thermal Resistance

Item	Symbol	Max. Value Note4	Unit
Channel to Case Thermal Resistance	R _{th(ch-C)}	1.05	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)}	83.3	°C/W

Notes: 4. This data is the designed target maximum value on Renesas's measurement condition. (Not tested)

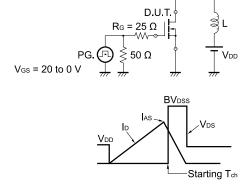
Electrical Characteristics (T_A = 25°C)

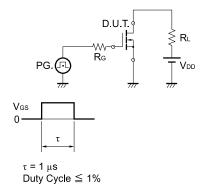
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μA	V _{DS} = 40 V, V _{GS} = 0 V
Gate Leakage Current	Igss			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Cut-off Voltage	V _{GS(off)}	2.0		4.0	V	$V_{DS} = 10 \text{ V}, I_{D} = 1 \text{ mA}$
Forward Transfer Admittance Note5	yfs	26			S	$V_{DS} = 10 \text{ V}, I_{D} = 50 \text{ A}$
Drain to Source On-state Resistance Note5	R _{DS(on)}		2.7	3.7	mΩ	V _{GS} = 10 V, I _D = 50 A
Input Capacitance	Ciss		5550		pF	V _{DS} = 25 V,
Output Capacitance	Coss		580		pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	Crss		320		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		29.0		ns	$V_{DD} = 20 \text{ V}, I_D = 50 \text{ A},$
Rise Time	t _r		15.0		ns	V _{GS} = 10 V,
Turn-off Delay Time	$t_{\text{d(off)}}$		64.0		ns	$R_G = 0 \Omega$
Fall Time	t _f		13.0		ns	
Total Gate Charge	Q_{G}		100		nC	$V_{DD} = 32 V$,
Gate to Source Charge	Q _{GS}		26		nC	$V_{GS} = 10 V,$
Gate to Drain Charge	Q_{GD}		32		nC	I _D = 100 A
Body Diode Forward Voltage Note5	$V_{F(S-D)}$			1.5	٧	I _F = 100 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		40		ns	$I_F = 50 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Qrr		44		nC	di/dt = 100 A/μs

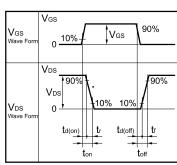
Notes: 5. Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME







TEST CIRCUIT 3 GATE CHARGE

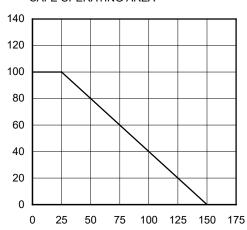
$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \text{ mA} \\ \hline \end{array} \begin{array}{c} RL \\ \hline \end{array}$$

dT - Percentage of Rated Power - %

Ip - Drain Current - A

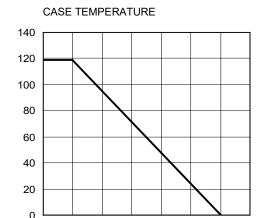
Typical Characteristics Notes

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



 $\ensuremath{\mathsf{T}_{\mathsf{C}}}$ - Case Temperature - ${}^{\circ}\mathsf{C}$ FORWARD BIAS SAFE OPERATING AREA

P_T - Total Power Dissipation - W



TOTAL POWER DISSIPATION vs.

T_C - Case Temperature - °C

75

100

125

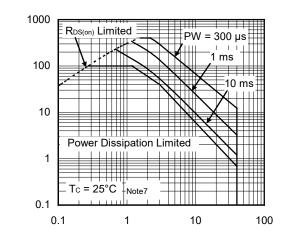
150

175

25

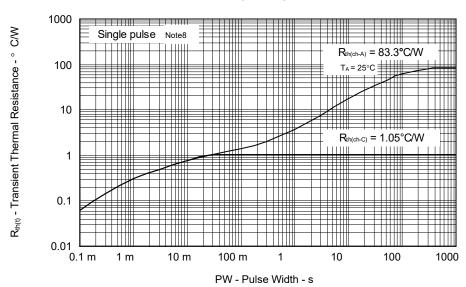
0

50



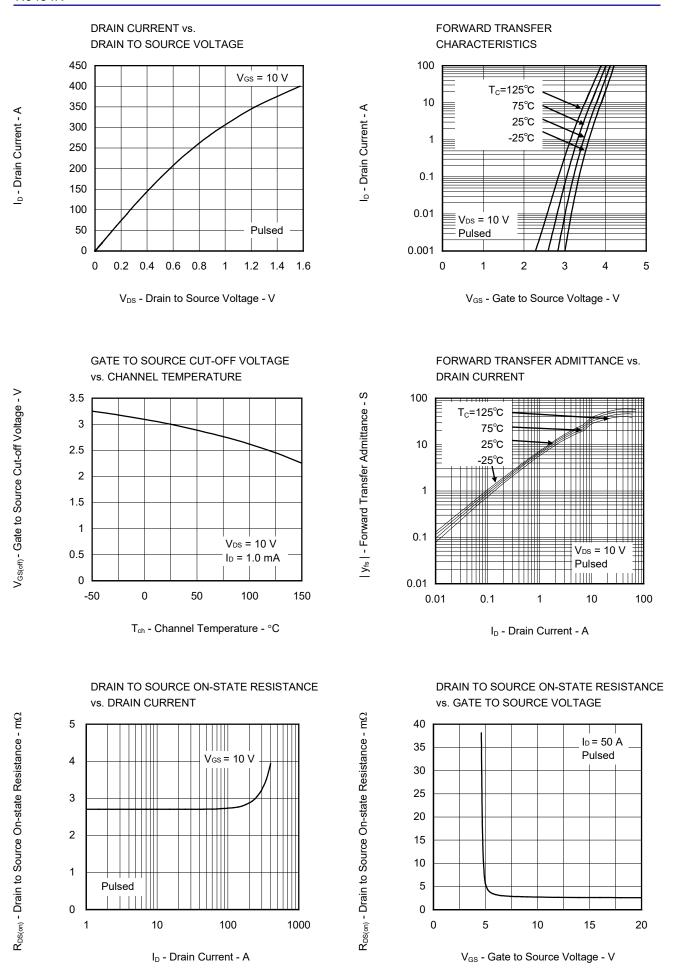
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

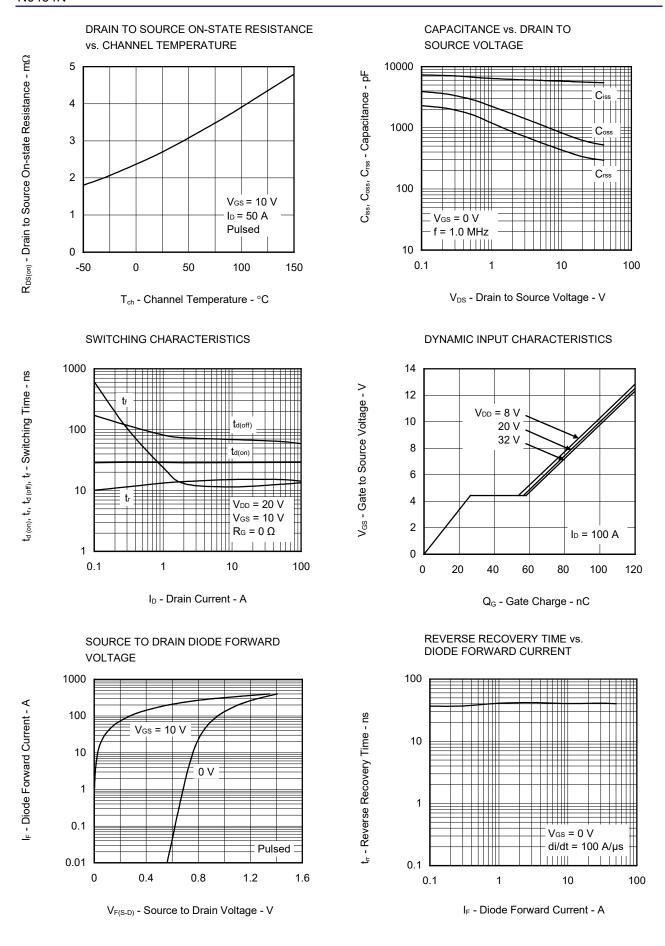
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



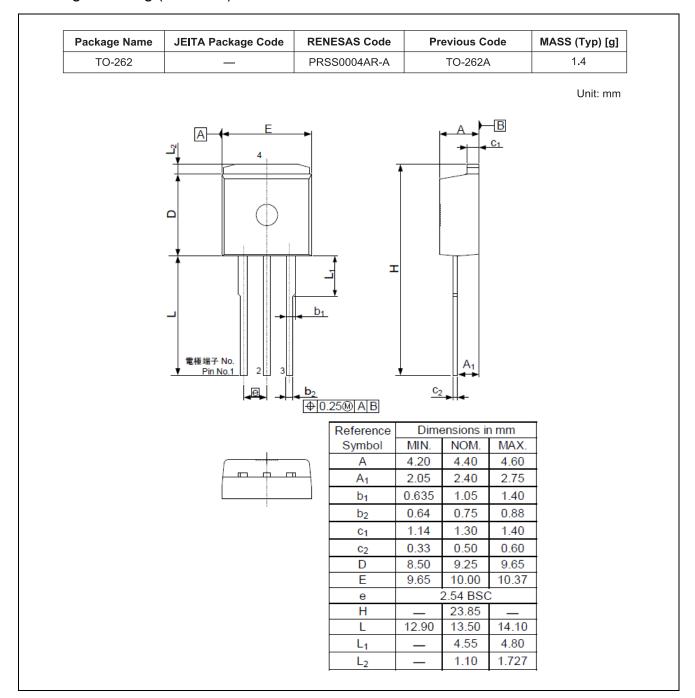
Notes: 6. Designed target value on Renesas measurement condition. (T_C = 25°C, unless otherwise specified)

- 7. This data is the designed value on Renesas's measurement condition. Renesas recommends that operating conditions are designed according to a document "Power MOSFET/IGBT Attention of Handling Semiconductor Devices (R07ZZ0010)".
- 8. This data is the designed target maximum value on Renesas's measurement condition.

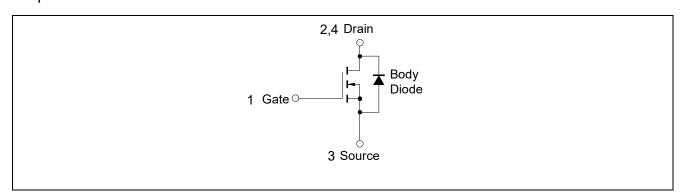




Package Drawing (Unit: mm)



Equivalent Circuit



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