NP75N04YLG

40 V – 75 A – N-channel Power MOS FET
Application: Automotive

R07DS1247EJ0100
Rev.1.00
Mar 02, 2015

Description

The NP75N04YLG is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
  $R_{DS(on)}$ = 4.8 mΩ MAX. (V_{GS} = 10 V, I_D = 38 A)
  $R_{DS(on)}$ = 8.3 mΩ MAX. (V_{GS} = 4.5 V, I_D = 38 A)
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP75N04YLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP75N04YLG-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±75	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±225	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	138	W
Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *3	I_{AR}	35	A
Repetitive Avalanche Energy *3	E_{AR}	123	mJ

Notes: *1 T_C = 25°C, $P_W \leq$ 10 μs, Duty Cycle ≤ 1%
*2 Mounted on glass epoxy substrate of 40 mm × 40 mm × 1.6 mmt with 4% Copper area (35 μm)
*3 Tch(peak) ≤ 150°C, R_G = 25 Ω

Thermal Resistance

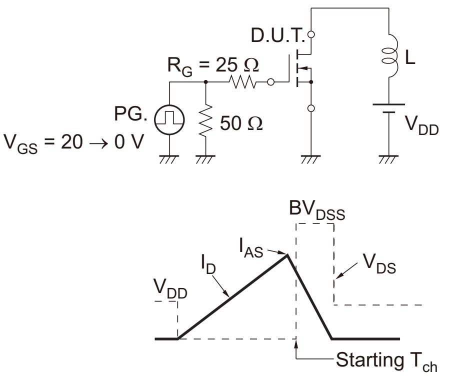
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.09	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	150	°C/W

Electrical Characteristics (T_A = 25°C)

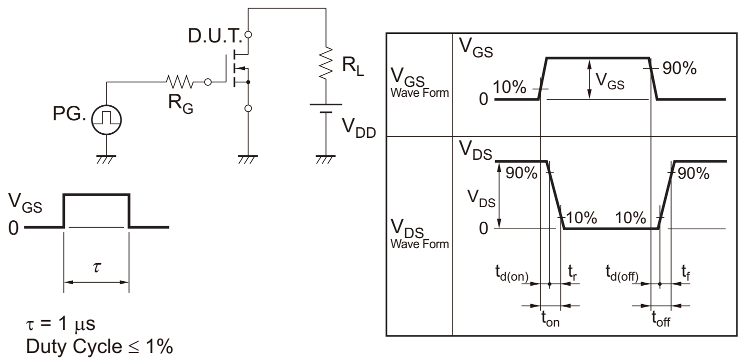
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±10	µA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.0	2.5	V	V_{DS} = V_{GS}, I_D = 250 µA
Forward Transfer Admittance *1	| y_{fs} |	40	46	—	S	V_{DS} = 5 V, I_D = 38 A
Drain to Source On-state Resistance *1	$R_{DS(on)}$	—	3.8	4.8	mΩ	V_{GS} = 10 V, I_D = 38 A
		—	4.5	8.3	mΩ	V_{GS} = 4.5 V, I_D = 38 A
Input Capacitance	C_{iss}	—	4300	6450	pF	V_{DS} = 25 V
Output Capacitance	C_{oss}	—	400	600	pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss}	—	250	450	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$	—	22	44	ns	V_{DD} = 20 V, I_D = 38 A
Rise Time	t_r	—	17	41	ns	V_{GS} = 10 V
Turn-off Delay Time	$t_{d(off)}$	—	40	140	ns	R_G = 0 Ω
Fall Time	t_f	—	11	27	ns	
Total Gate Charge	Q_G	—	77	116	nC	V_{DD} = 32 V
Gate to Source Charge	Q_{GS}	—	20	—	nC	V_{GS} = 10 V
Gate to Drain Charge	Q_{GD}	—	25	—	nC	I_D = 75 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	I_F = 75 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	34	—	ns	I_F = 75 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	34	—	nC	di/dt = 100 A/µs

Note: *1 Pulsed test

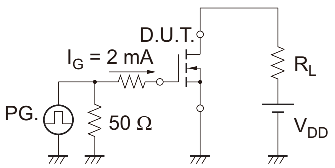
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



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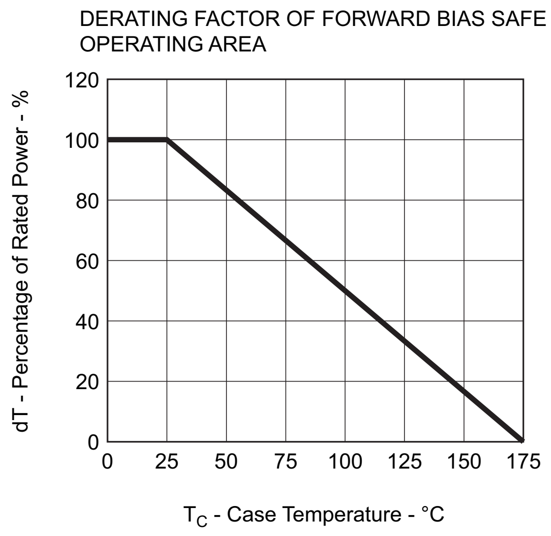
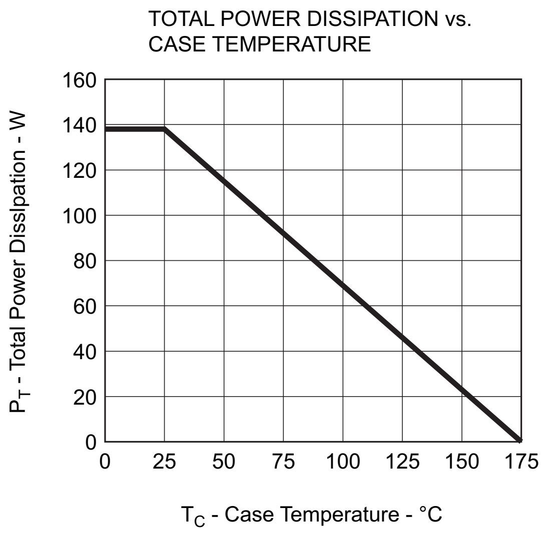
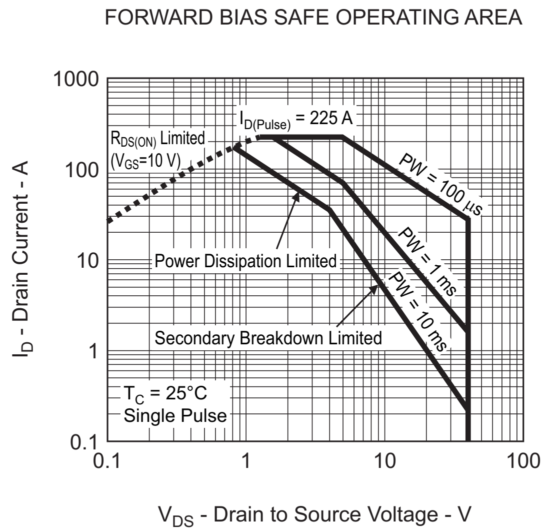
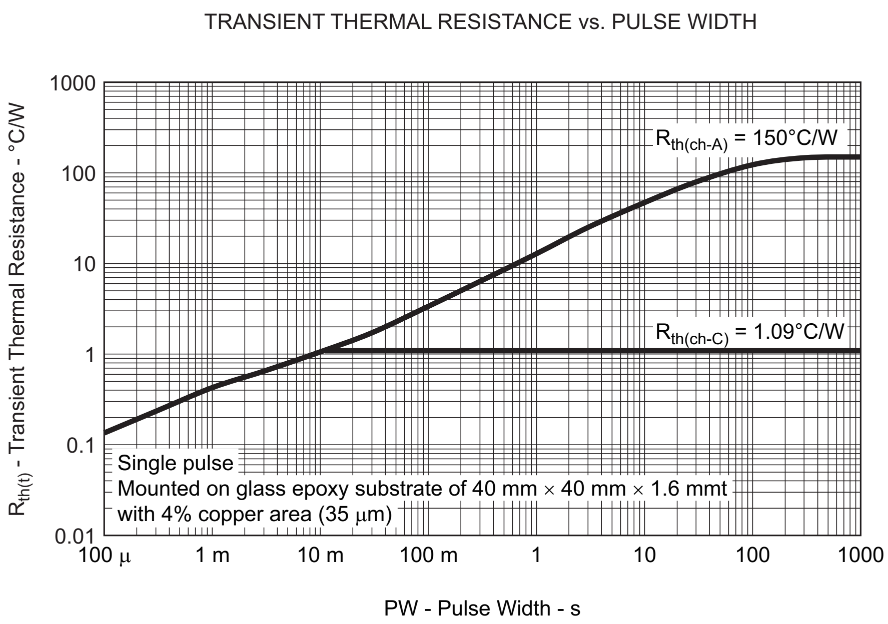
Typical Characteristics (T_A = 25°C)

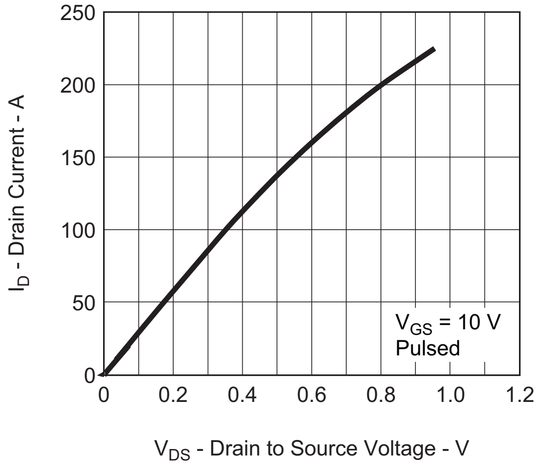




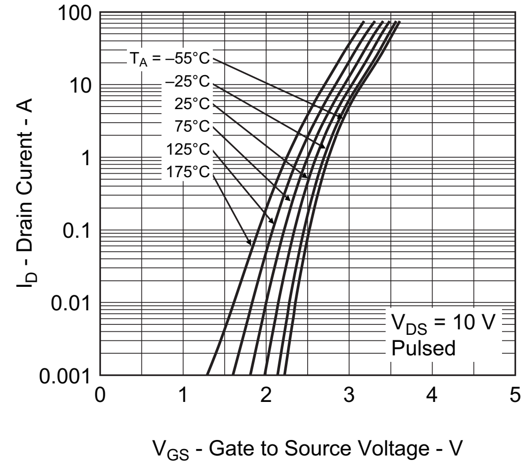




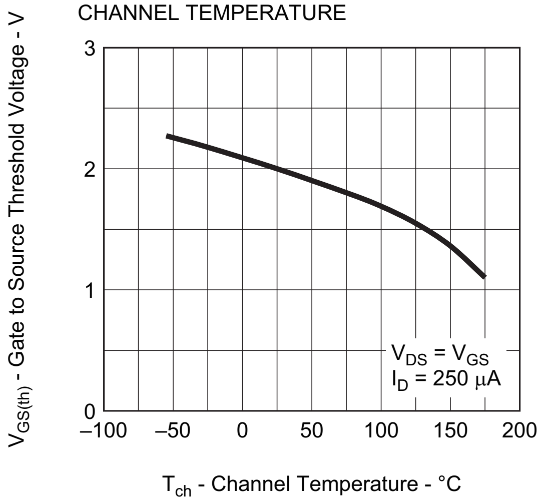
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



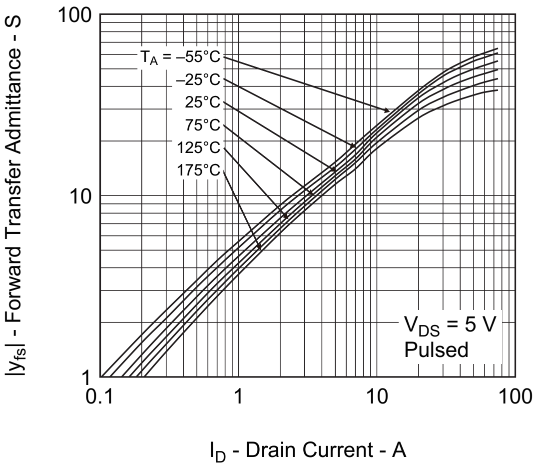
FORWARD TRANSFER CHARACTERISTICS



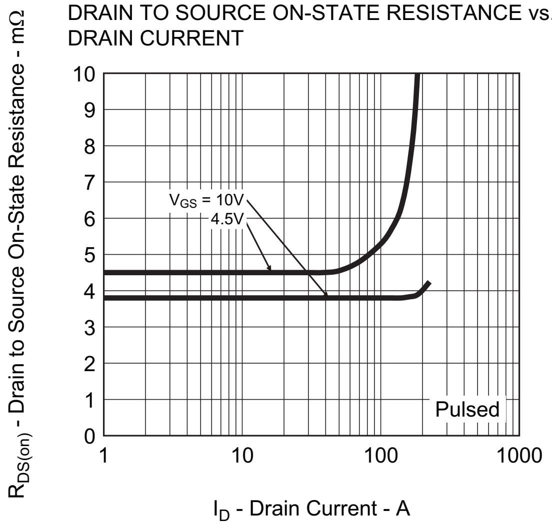
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



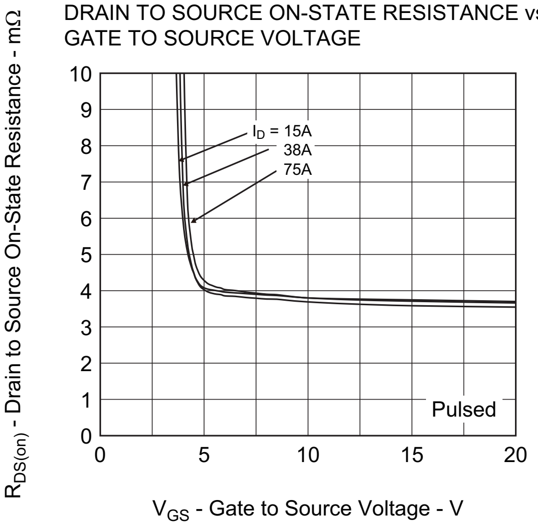
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



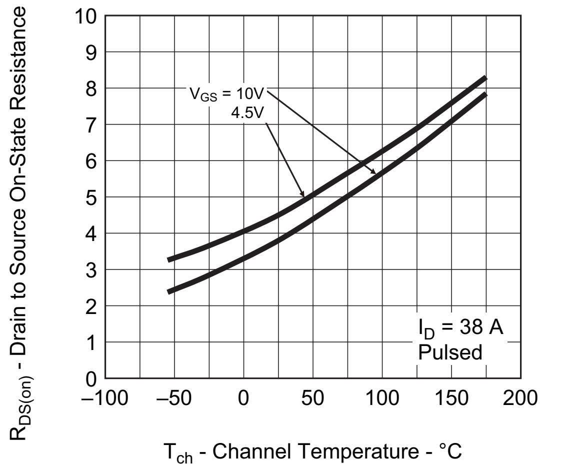
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



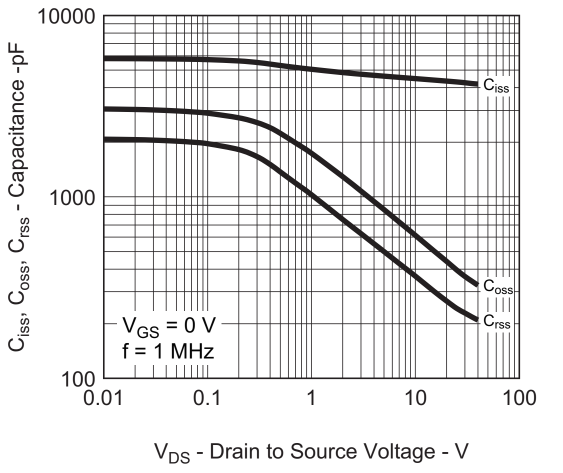
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



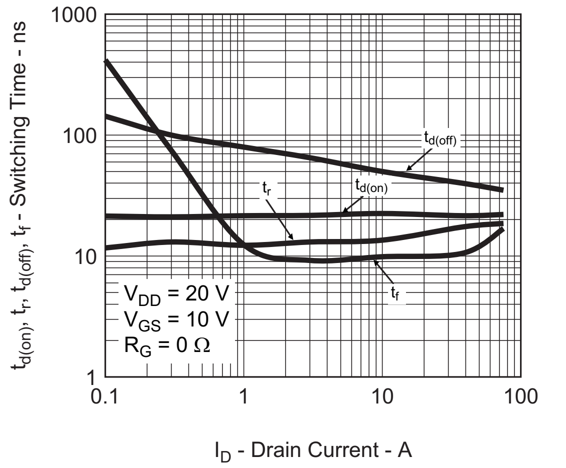
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



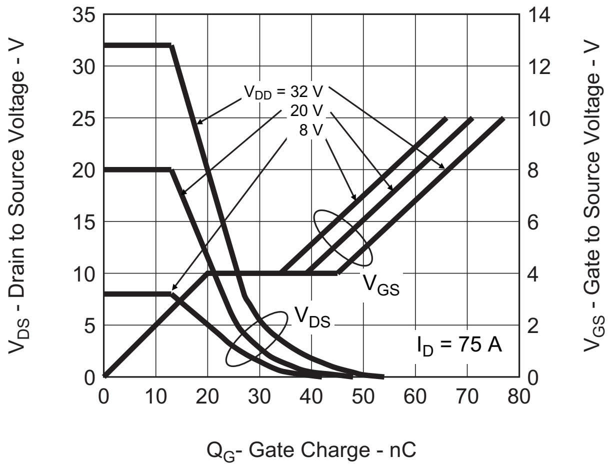
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



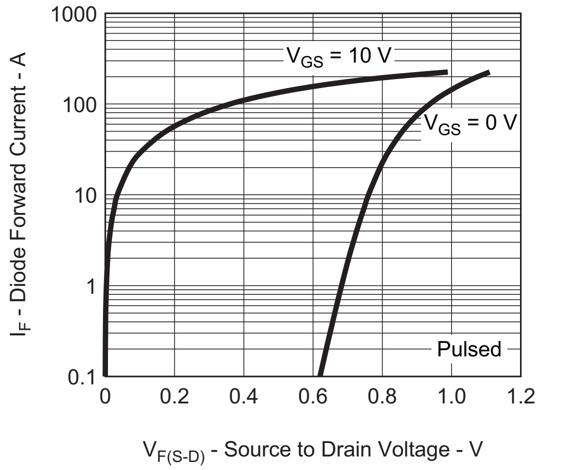
SWITCHING CHARACTERISTICS



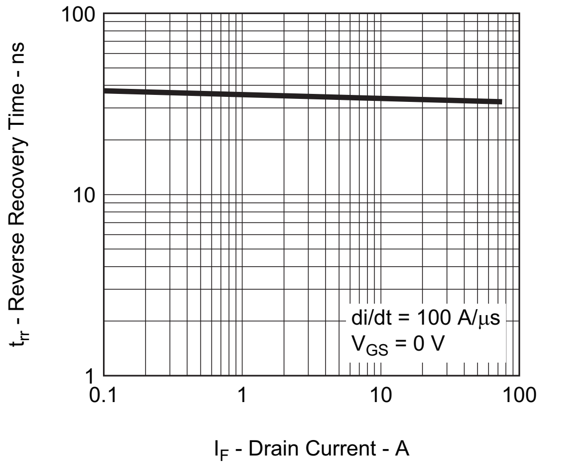
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



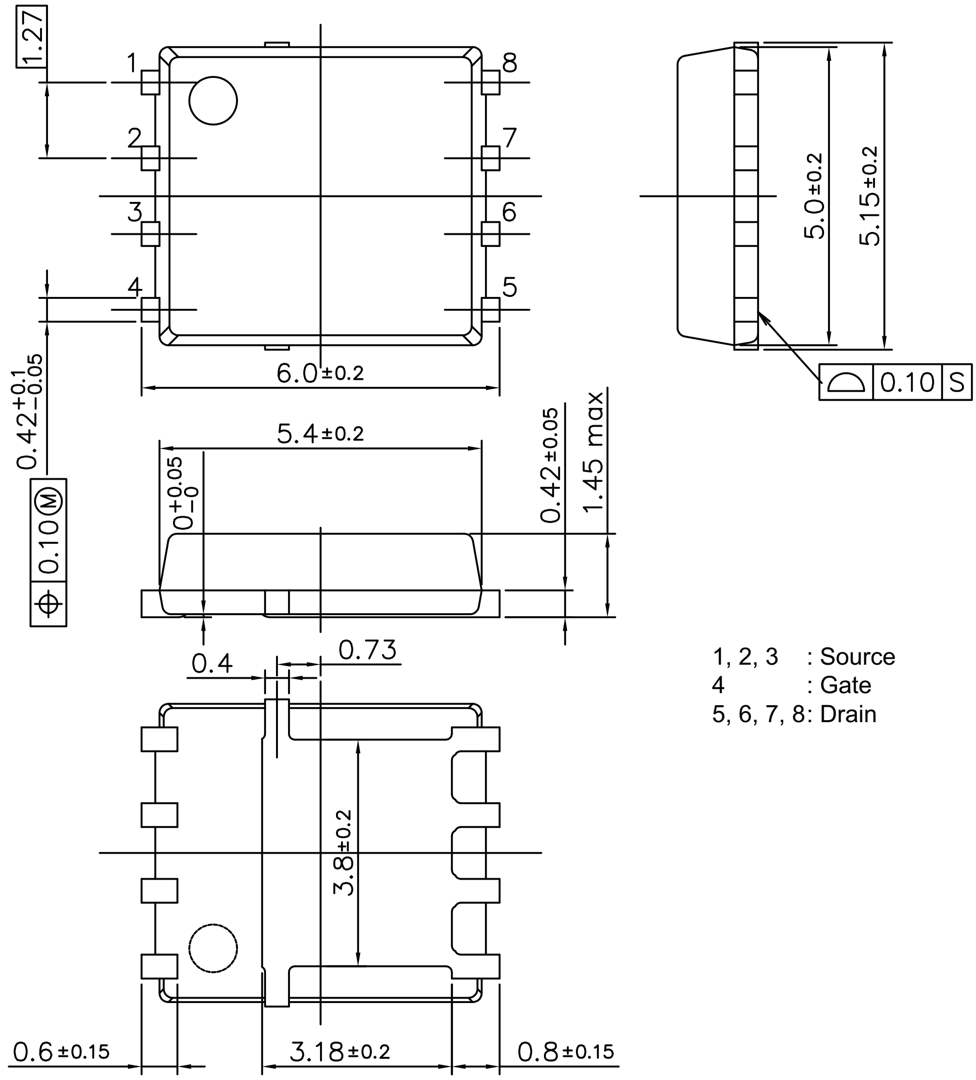
REVERSE RECOVERY TIME vs. DRAIN CURRENT



Package Drawing (Unit: mm)

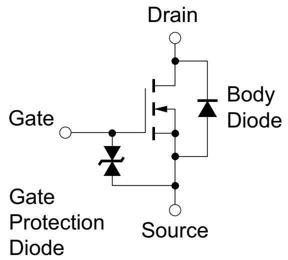
8-pin HSON (Mass: 0.128 g TYP.)

Renesas Code: PLSN0008KA-A



1, 2, 3 : Source
4 : Gate
5, 6, 7, 8: Drain

Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP75N04YLG Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar 02, 2015	—	First Edition Issued

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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