

# NP75N04YLG

40 V – 75 A – N-channel Power MOS FET  
 Application: Automotive

R07DS1247EJ0100  
 Rev.1.00  
 Mar 02, 2015

## Description

The NP75N04YLG is N-channel MOS Field Effect Transistors designed for high current switching applications.

## Features

- Super low on-state resistance  
 $R_{DS(on)} = 4.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 38 \text{ A)}$   
 $R_{DS(on)} = 8.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 38 \text{ A)}$
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

## Ordering Information

Part No.	Lead Plating	Packing		Package
NP75N04YLG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP75N04YLG-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 75$	A
Drain Current (pulse) *1	$I_{D(pulse)}$	$\pm 225$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	138	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *2	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Repetitive Avalanche Current *3	$I_{AR}$	35	A
Repetitive Avalanche Energy *3	$E_{AR}$	123	mJ

Notes: \*1  $T_C = 25^\circ\text{C}$ ,  $P_W \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2 Mounted on glass epoxy substrate of 40 mm  $\times$  40 mm  $\times$  1.6 mm with 4% Copper area (35  $\mu\text{m}$ )

\*3  $T_{ch(peak)} \leq 150^\circ\text{C}$ ,  $R_G = 25 \Omega$

## Thermal Resistance

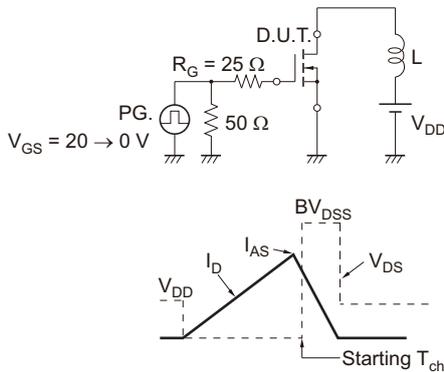
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.09	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	150	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>A</sub> = 25°C)

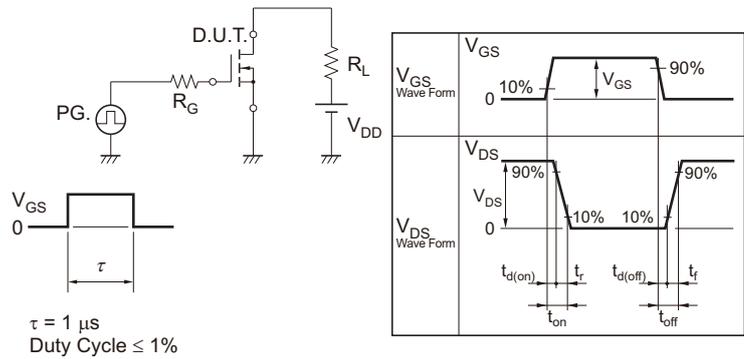
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	1.5	2.0	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	40	46	—	S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 38 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>	—	3.8	4.8	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 38 A
		—	4.5	8.3	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 38 A
Input Capacitance	C <sub>iss</sub>	—	4300	6450	pF	V <sub>DS</sub> = 25 V V <sub>GS</sub> = 0 V f = 1 MHz
Output Capacitance	C <sub>oss</sub>	—	400	600	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	250	450	pF	
Turn-on Delay Time	t <sub>d(on)</sub>	—	22	44	ns	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 38 A V <sub>GS</sub> = 10 V R <sub>G</sub> = 0 Ω
Rise Time	t <sub>r</sub>	—	17	41	ns	
Turn-off Delay Time	t <sub>d(off)</sub>	—	40	140	ns	
Fall Time	t <sub>f</sub>	—	11	27	ns	
Total Gate Charge	Q <sub>G</sub>	—	77	116	nC	V <sub>DD</sub> = 32 V V <sub>GS</sub> = 10 V I <sub>D</sub> = 75 A
Gate to Source Charge	Q <sub>GS</sub>	—	20	—	nC	
Gate to Drain Charge	Q <sub>GD</sub>	—	25	—	nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>	—	0.9	1.5	V	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	—	34	—	ns	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	—	34	—	nC	di/dt = 100 A/μs

Note: \*1 Pulsed test

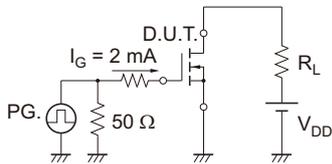
TEST CIRCUIT 1 AVALANCHE CAPABILITY



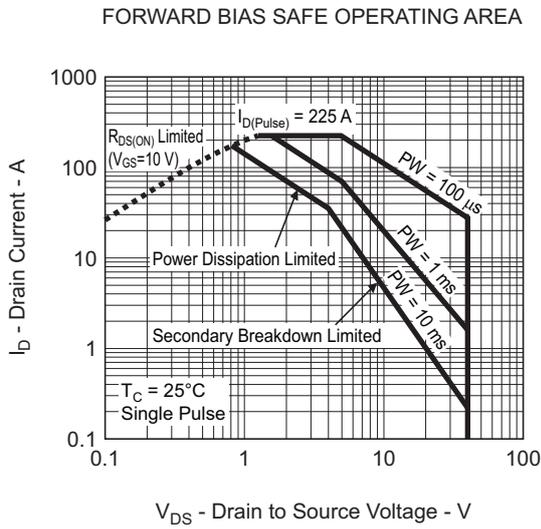
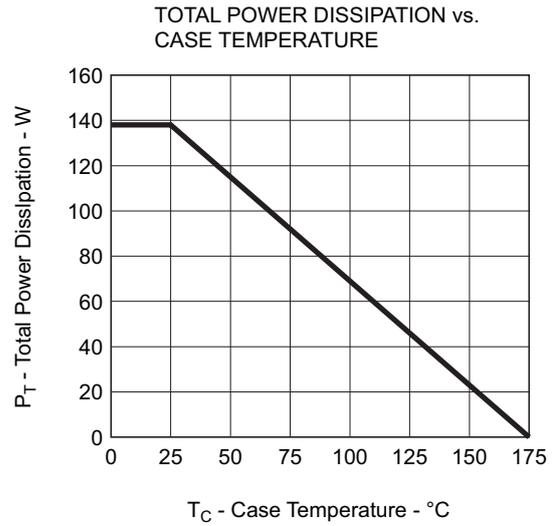
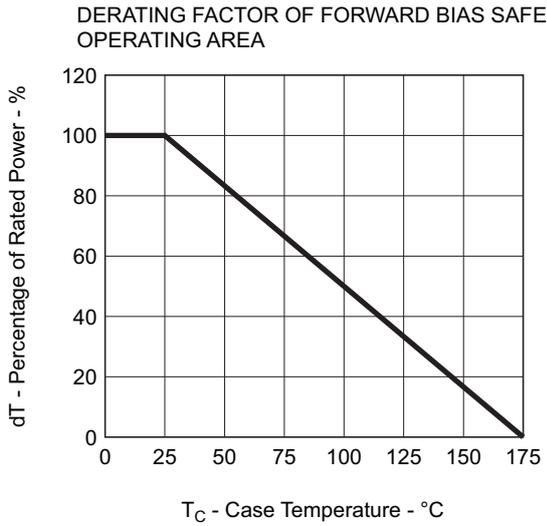
TEST CIRCUIT 2 SWITCHING TIME



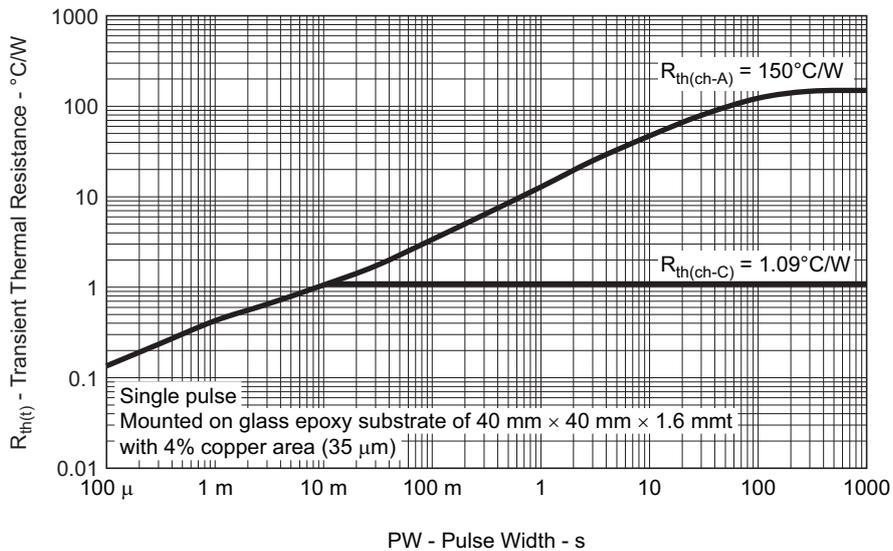
TEST CIRCUIT 3 GATE CHARGE



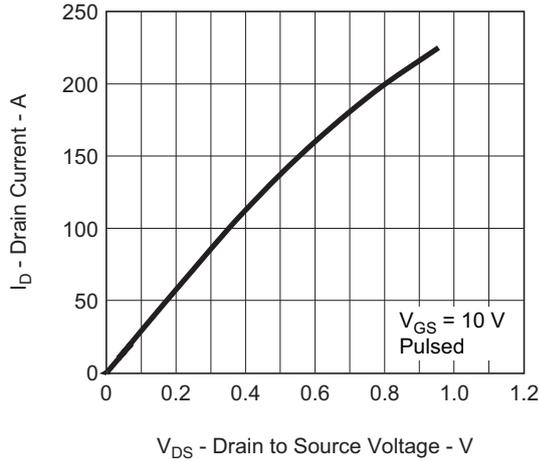
Typical Characteristics (T<sub>A</sub> = 25°C)



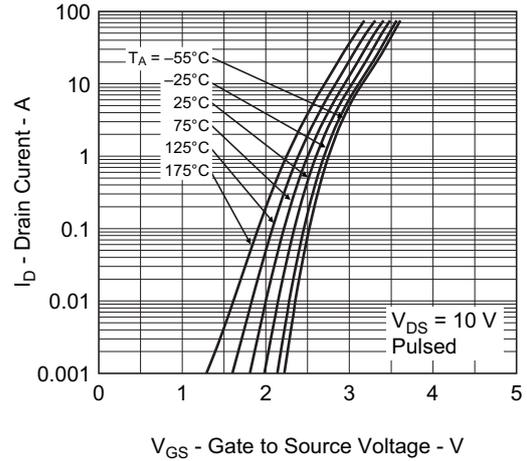
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



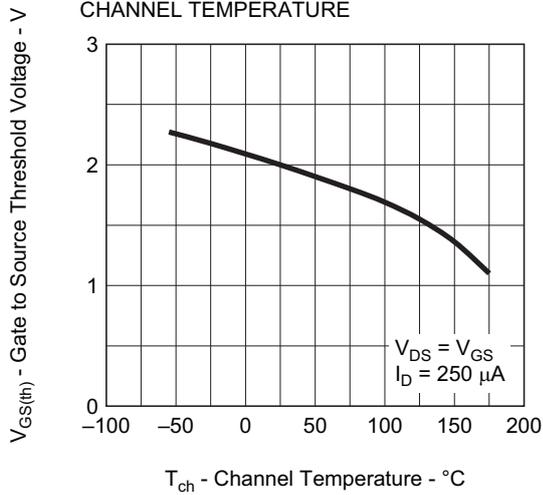
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



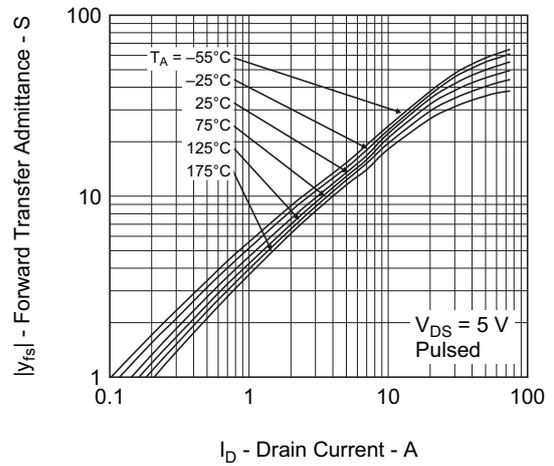
FORWARD TRANSFER CHARACTERISTICS



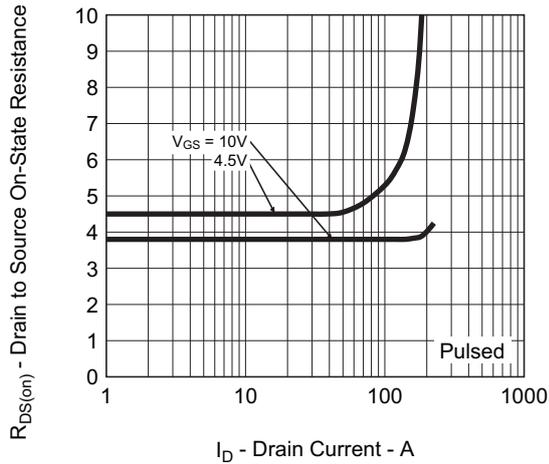
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



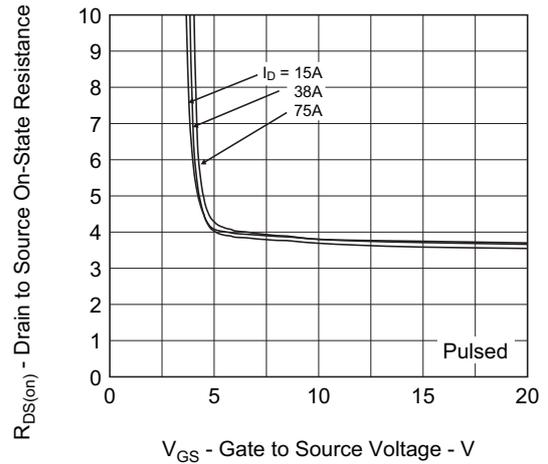
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



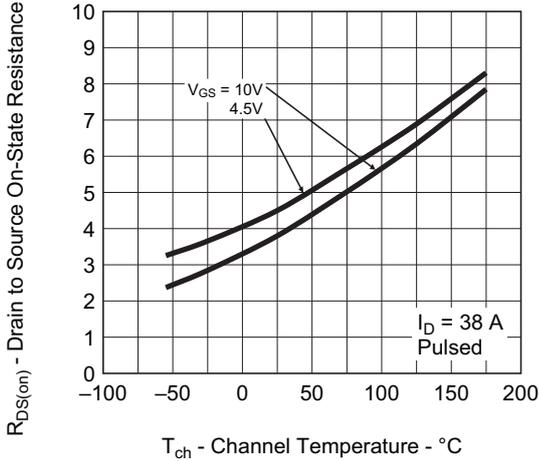
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



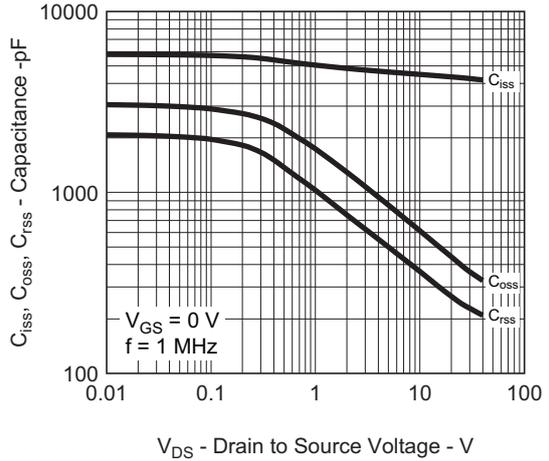
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



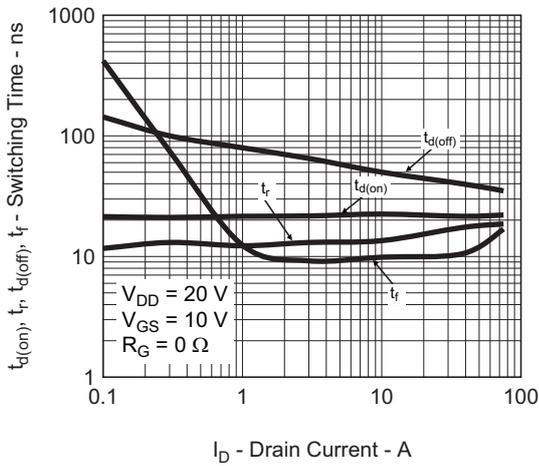
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



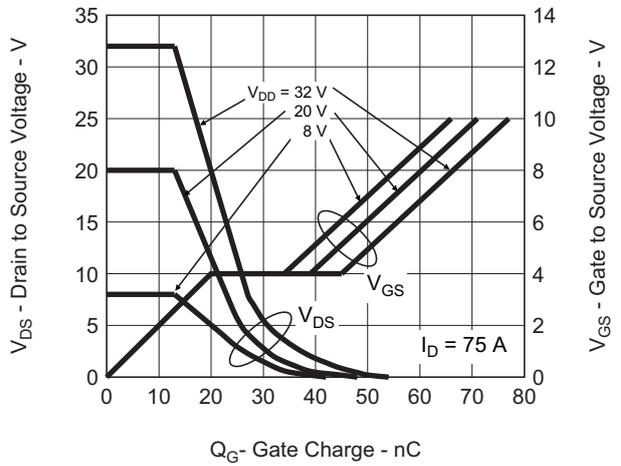
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



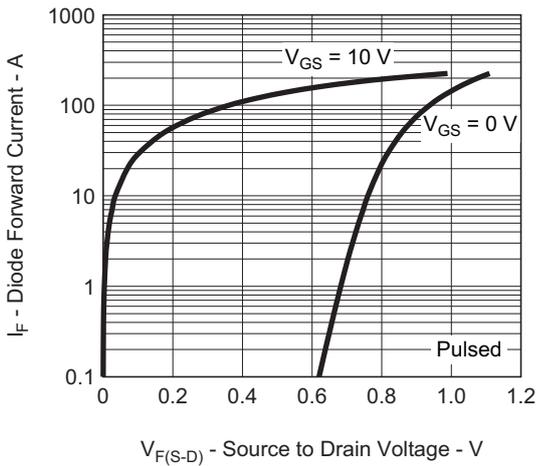
SWITCHING CHARACTERISTICS



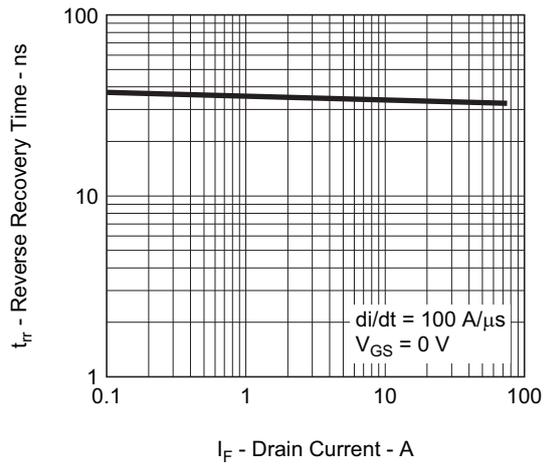
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



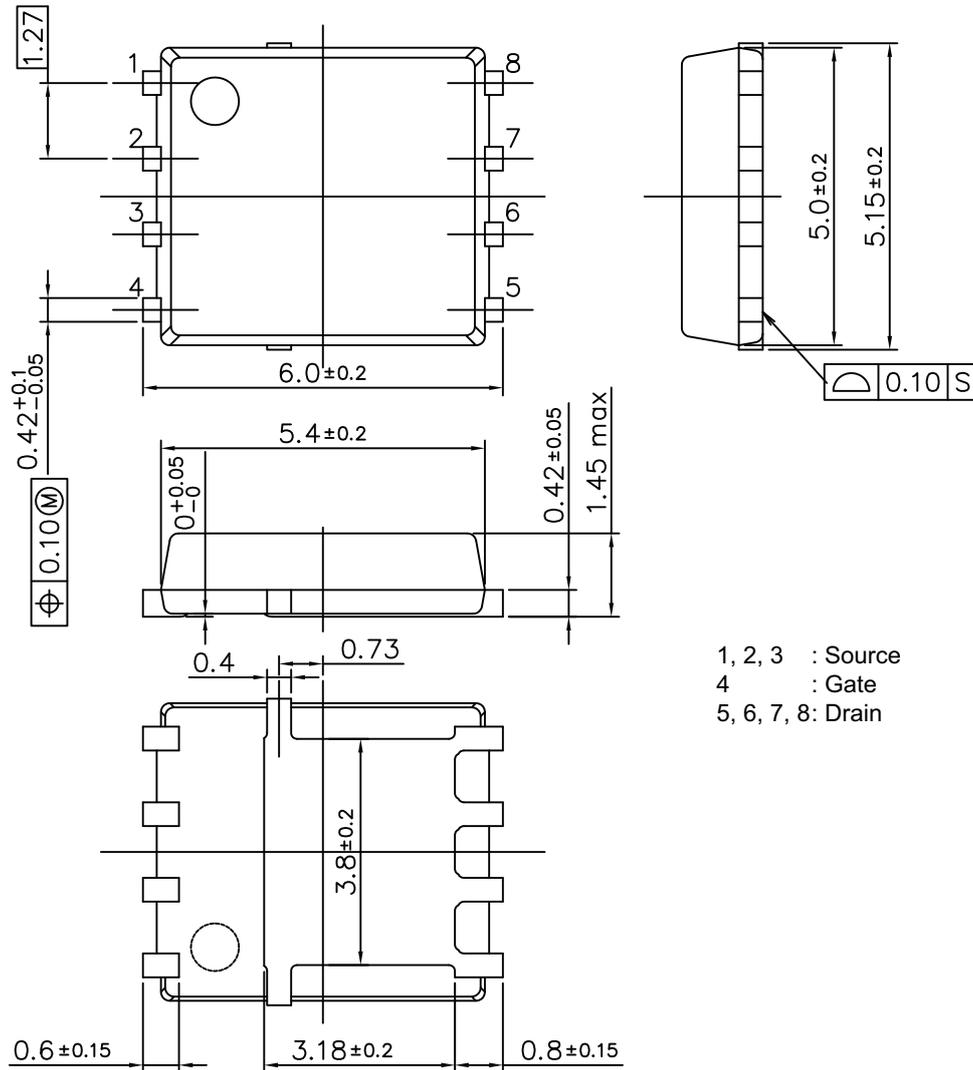
REVERSE RECOVERY TIME vs. DRAIN CURRENT



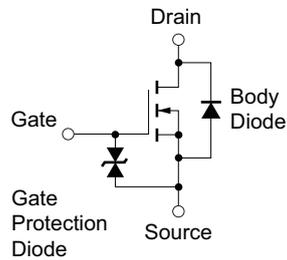
Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)

Renesas Code: PLSN0008KA-A



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

<b>Revision History</b>	<b>NP75N04YLG Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 02, 2015	—	First Edition Issued

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