Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR

NP80N03EDE, NP80N03KDE

NP80N03CDE, NP80N03DDE, NP80N03MDE, NP80N03NDE

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	₩ PACKAGE		
NP80N03EDE-E1-AY Note1, 2			TO 202 (MD 257 I) 4 in 4.4 in		
NP80N03EDE-E2-AY Note1, 2	Dura Ca (Tia)	Tana 200 n/raal	TO-263 (MP-25ZJ) typ. 1.4 g		
NP80N03KDE-E1-AY Note1	Pure Sn (Tin)	Tape 800 p/reel	TO 202 (MD 257K) him 4.5 m		
NP80N03KDE-E2-AY Note1			TO-263 (MP-25ZK) typ. 1.5 g		
NP80N03CDE-S12-AZ Note1, 2	Sn-Ag-Cu		TO-220 (MP-25) typ. 1.9 g		
NP80N03DDE-S12-AY Note1, 2		Tuba CO a thicka	TO-262 (MP-25 Fin Cut) typ. 1.8 g		
NP80N03MDE-S18-AY Note1	Pure Sn (Tin)	Tube 50 p/tube	TO-220 (MP-25K) typ. 1.9 g		
NP80N03NDE-S18-AY Note1		-0	TO-262 (MP-25SK) typ. 1.8 g		

Notes 1. Pb-free (This product does not contain Pb in the external electrode.)

2. Not for new design

FEATURES

- Channel Temperature 175 degree rated
- Super Low on-state Resistance

 $R_{DS(on)1} = 7.0 \text{ m}\Omega$ MAX. (Vgs = 10 V, ID = 40 A)

 $R_{DS(on)2} = 9.0 \text{ m}\Omega$ MAX. (Vgs = 5 V, ID = 40 A)

 $R_{DS(on)3} = 11 \text{ m}\Omega$ MAX. (Vgs = 4.5 V, ID = 40 A)

Low input capacitance

Ciss = 2600 pF TYP.

(TO-220)



(TO-262)



(TO-263)



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ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	Voss	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C) Note1	ID(DC)	±80	Α
Drain Current (pulse) Note2	ID(pulse)	±320	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	120	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Single Avalanche Current Note3	las	50/40/9	Α
Single Avalanche Energy Note3	Eas	2.5/160/400	mJ

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

- **2.** PW \leq 10 μ s, Duty cycle \leq 1%
- 3. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V (See **Figure 4.**)

THERMAL RESISTANCE

°C/W EOL announced Channel to Case Thermal Resistance 1.25 Rth(ch-C) Channel to Ambient Thermal Resistance

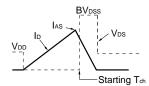


ELECTRICAL CHARACTERISTICS (TA = 25°C)

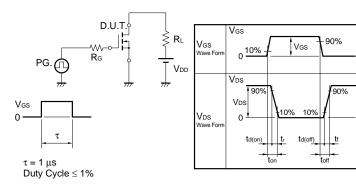
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 40 A	20	41		S
Drain to Source On-state Resistance	RDS(on)1	V _{GS} = 10 V, I _D = 40 A		5.3	7.0	mΩ
	RDS(on)2	V _{GS} = 5 V, I _D = 40 A		6.8	9.0	mΩ
	RDS(on)3	V _{GS} = 4.5 V, I _D = 40 A		7.5	11	mΩ
Input Capacitance	Ciss	V _{DS} = 25 V,		2600	3900	pF
Output Capacitance	Coss	V _{GS} = 0 V,		590	890	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz	*	270	490	pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 40 A,	Ç	20	44	ns
Rise Time	tr	V _{GS} = 10 V,	5	12	31	ns
Turn-off Delay Time	t _{d(off)}	R _G = 1 Ω		60	120	ns
Fall Time	tf			14	35	ns
Total Gate Charge	Q _{G1}	I _D = 80 A, V _{DD} = 24 V, V _{GS} = 10 V		48	72	nC
	Q _{G2}	V _{DD} = 24 V,		28	42	nC
Gate to Source Charge	QGS	V _{GS} = 5 V,		10		nC
Gate to Drain Charge	Q _{GD}	I _D = 80 A		14		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 80 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	trr	I _F = 80 A, V _{GS} = 0 V,		34		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		22		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

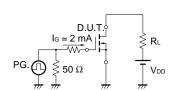
$V_{GS} = 20 \rightarrow 0 \text{ V}$ $R_{G} = 25 \Omega$ $R_{G} = 25 \Omega$



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (TA = 25°C)

Figure 1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

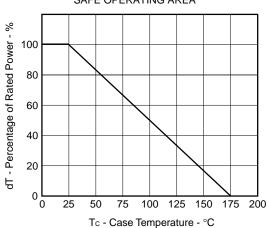


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

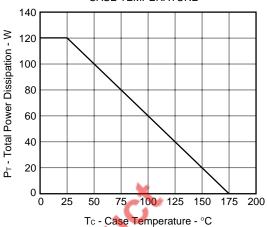


Figure 3. FORWARD BIAS SAFE OPERATING AREA

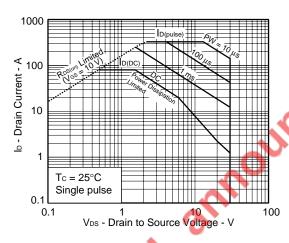


Figure 4. SINGLE AVALANCHE ENERGY DERATING FACTOR

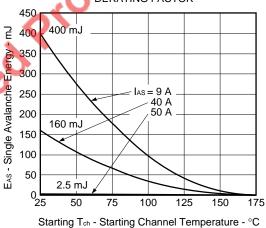


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

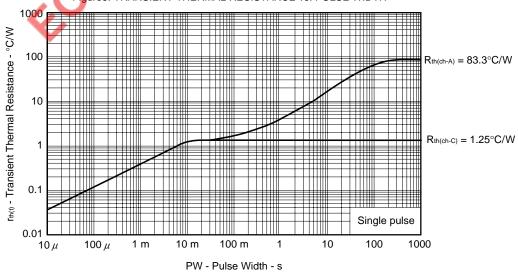


Figure 6. FORWARD TRANSFER CHARACTERISTICS

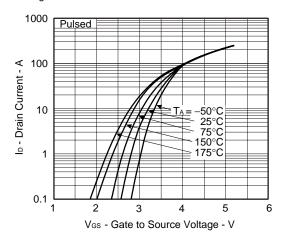


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

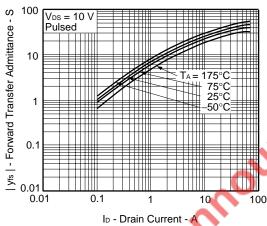


Figure 10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

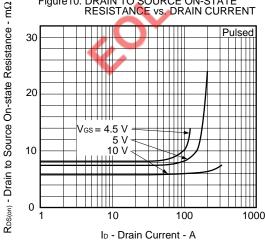


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

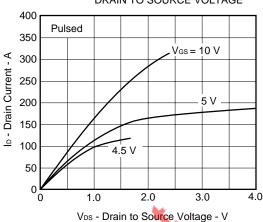


Figure 9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

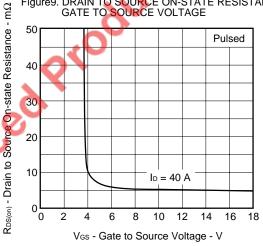


Figure 11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

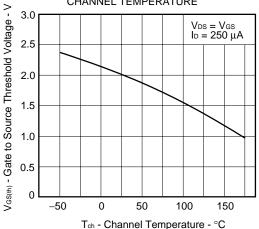




Figure 12. DRAIN TO SOURCE ON-STATE RESISTANCE V CHANNEL TEMPERATURE

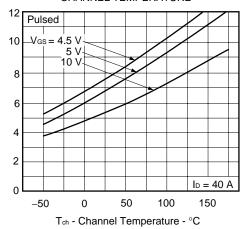


Figure 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

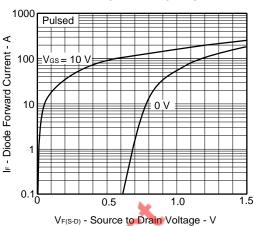


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

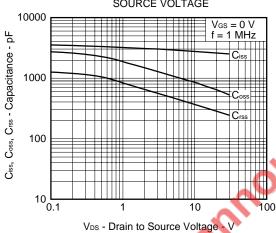


Figure 15. SWITCHING CHARACTERISTICS

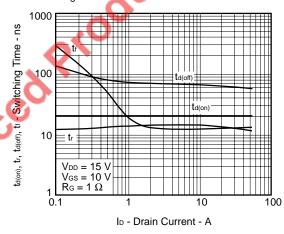


Figure 16. REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

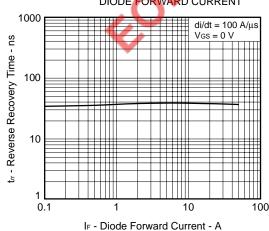
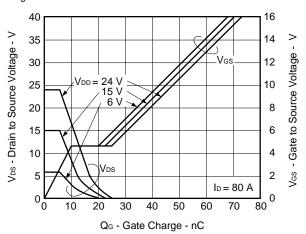
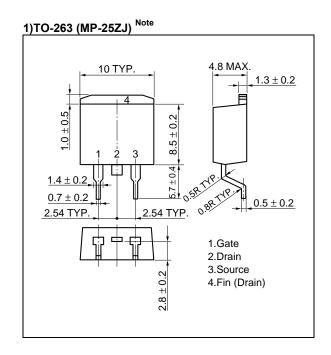
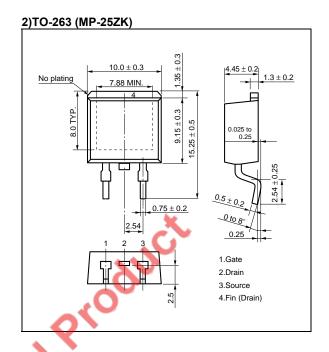


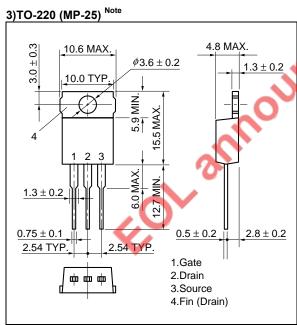
Figure 17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

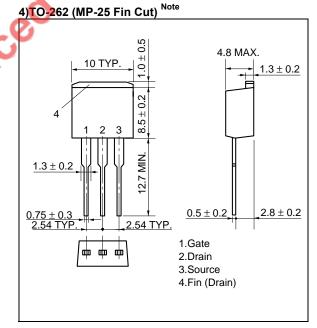


<R> PACKAGE DRAWINGS (Unit: mm)

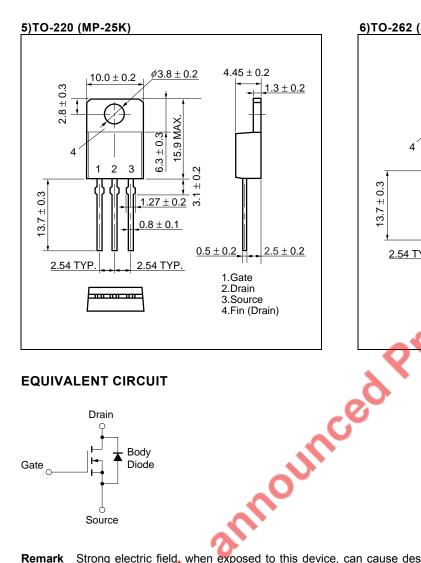


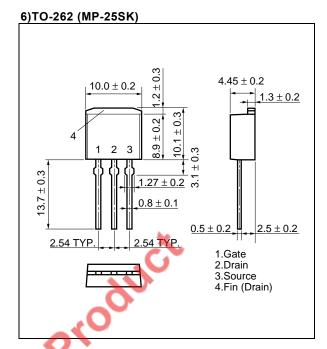




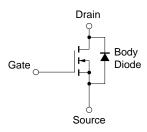


Note Not for new design





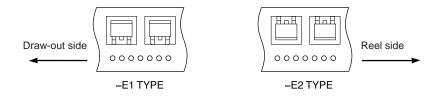
EQUIVALENT CIRCUIT



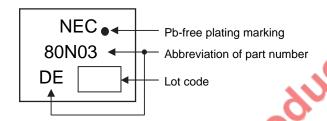
Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

<R> TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



<R> MARKING INFORMATION



<R> RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

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For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol	
Infrared reflow MP-25ZJ, MP-25ZK	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less	IR60-00-3	
	Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less		
Wave soldering MP-25, MP-25K, MP-25SK, MP-25 Fin Cut	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS	
Partial heating MP-25ZJ, MP-25ZK, MP-25K, MP-25SK	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350	
Partial heating MP-25, MP-25 Fin Cut	Maximum temperature (Pin temperature): 300°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P300	

Caution Do not use different soldering methods together (except for partial heating).

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