5 Watt Wireless Power Receiver IC

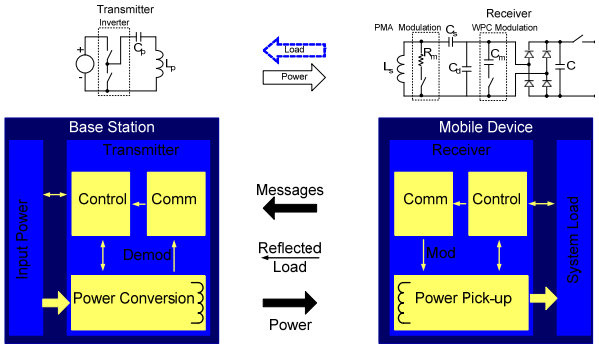
IDTP9023 Product Datasheet

Features

- **Single Chip Solution for Wireless Power Consortium (WPC) "Qi" Compliant Power Receiver**
- **Conforms to WPC 1.1 Specification**
- **Conforms to PMA Type 1 Specification**
- **Integrated Full-Bridge Synchronous Rectifier**
- **Integrated Synchronous Buck Converter**
- **Closed Loop Power Transfer Control between Base Station and Mobile Device**
- **Security and Encryption up to 64 bit**
- **Foreign Object Detection (FOD)**
- **Proprietary Base-to-Mobile Communication Channel for Authentication**
- **Over Temperature/Voltage/Current Protection**
- **Thermal Control Loop**
- **Open-Drain LED Indicator Outputs**
- **I²C Interface**

Applications

- **WPC and PMA Compliant Wireless Chargers for Mobile Applications**
- **Non-WPC Compliant Wireless Chargers for Mobile Applications**

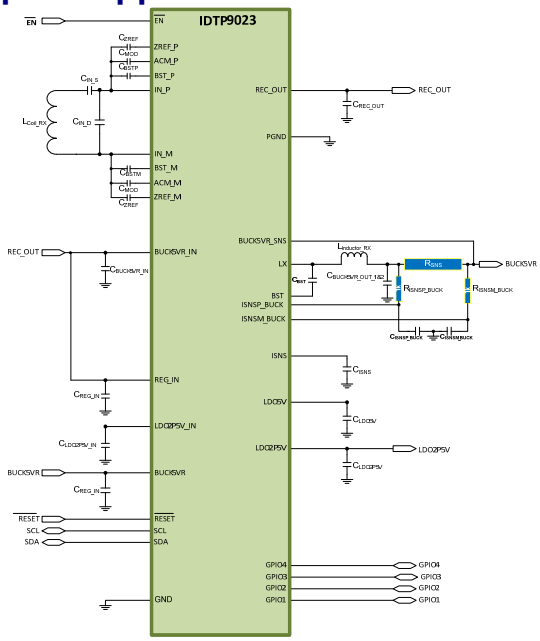


Description

The IDTP9023 is a highly integrated single-chip WPC and PMA compliant wireless power receiver IC. The device operates with an AC power signal from a compatible wireless transmitter and converts it into a regulated 5V output voltage, which can be used to power devices or supply the charger input in mobile applications. The IDTP9023 integrates a high efficiency Synchronous Full Bridge Rectifier (SFBR), high-efficiency synchronous buck converter, and control circuits used to modulate the load to transmit WPC and PMA compliant message packets to the base station to optimize power delivery.

The device includes over temperature/voltage/current protection and an FOD method to protect the base station and mobile device from over-heating in the presence of a metallic foreign object. Fault conditions associated with power transfer are managed by the embedded MCU which also controls status LEDs to indicate operating and fault modes.

Typical Application Circuit



Package: WLCSP-79, 4.095x3.898mm, 0.4mm pitch (See page 25)
Ordering information (See page 26)

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ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9023 at absolute maximum ratings is not implied. Application of the absolute maximum rating conditions affects device reliability.

Table 1. Absolute Maximum Ratings Summary. All voltages are referred to ground, unless otherwise noted.

PINS	RATING	UNITS
IN_M, IN_P, ACM_M, ACM_P, ZREF_P, ZREF_M	-1 to 24	V
$\overline{EN}$, REG_IN, REC_OUT, BUCK5VR_IN, LX	-0.3 to 24	V
GPIO4:1, $\overline{RESET}$, LDO5V, LDO2P5V_IN, ISNS, ISNSP_BUCK, ISNSM_BUCK, BUCK5VR, BUCK5VR_SNS, VDDIO, SDA, SCL	-0.3 to 6.0	V
SDA, SCL	-0.3 to VDDIO	V
BST	-0.3 to LX+5	V
BST_P, BST_M	-0.3 to IN_P+5, IN_M+5	V
GND, AGND, DGND, REFGND, PGND, PGND_BUCK, PGND_REC	-0.3 to 0.3	V
LDO2P5V	-0.3 to 2.75	V
Maximum Current from REC_OUT	2.25	A
Maximum RMS Current from IN_P, IN_M	1	A
Maximum Current from LX	2.25	A

The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	RATING WITH 14 THERMAL VIAS	UNITS
Θ_{JA}	Maximum Thermal Resistance (WLCSP-9x9)	45	°C/W
T_J	Junction Operating Temperature Range	0 to 125	°C
T_{JS}	Junction Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	°C

This thermal rating was calculated based on a JEDEC 51 standard 4-layer board with dimensions 4in x 4.5in in still air conditions. Actual thermal resistance will be affected by PCB size, solder joint quality, PCB layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3. ESD Information

TEST MODEL	PINS	RATINGS	UNITS
HBM	All Pins	1500	V
CDM	All Pins	500	V

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SPECIFICATION TABLE

Table 4. Device Characteristics

V_{REC_OUT} = $V_{BUCK5VR\_IN}$ = V_{REG_IN} = 12V; $\overline{EN}$ = LOW; $\overline{RESET}$ = HIGH , Synchronous Rectifier, LDO2P5V, LDO5V, and DC/DC Converter blocks must be operated together, unless otherwise noted. T_A = 0 to +85°C. Typical values are at 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Synchronous Full Bridge Rectifier (SFBR)						
$I_{RECT-STANDBY}$	Standby Current	No load on REC_OUT, BUCK5VR, LDO5V, and LDO2P5V		13		mA
$I_{RECT-DIS}$	Disabled Current	V_{REC_OUT}=$V_{BUCK5VR\_IN}$=V_{REG_IN}=18V, $V_{\overline{EN}}$=5V to 20V		7	10	mA
$R_{DSON-SFBR}$	SFBR switch resistance			120		mΩ
Modulation						
$R_{DS-ON-CMOD-AC}$	Mosfet on resistance driving C_{MOD}		1	1.8	3	Ω
$I_{LEAK-AC-MOD}$	AC_MOD switch leakage	AC_MOD switches off	-1		1	µA
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			62.5		kSPs
Channel	# of Channels			8		
ADC_{CLK}	ADC Clock Frequency			1		MHz
$V_{IN\ FS}$	Full Scale Range		2.41	2.44	2.47	V
AC Clamp						
$V_{RECT-CL}$	AC Clamp protection for rectified voltage (Rising)		18.5		20	V
$V_{RECT-CL-HYS}$	Hysteresis			2.2		V
$I_{LEAK-AC-CLAMP}$	AC_CLAMP switch leakage	AC_CLAMP switches off	-1		1	µA
UVLO						
$V_{RECT-UVLO}$	Rising		2.8		3.3	V
$V_{RECT-UVLO-HYS}$	Hysteresis			120		mV
DC/DC Converter						
V_{OUT}	Output voltage	6V≤$V_{BUCK5VR\_IN}$≤18V, 10mA≤I_{OUT}≤1.0 A	4.75	5	5.25	V
I_{OUT}	Maximum output current capability	4.75V≤V_{out}≤5.25V, R_{ISNSP_BUCK}=R_{ISNSM_BUCK} = 1kΩ	1.1		1.3	A
$R_{DSON-HS}$	High side switch on resistance			85		mΩ
$R_{DSON-LS}$	Low side switch on resistance			145		mΩ
$BUCK5VR\_SNS_{IIMP}$	Input impedance			750		kΩ
Low-Drop-Out Regulators						
LDO2P5V						
V_{OUT}	Output voltage	4.75V≤$V_{LDO2P5V\_IN}$ ≤ 5.25V	2.375	2.5	2.625	V
I_{OUT}	Output current	Note:1			100	mA
I_{SCP}	Short-circuit protection current				7	mA

Note 1: LDO2P5V Output current is subtracted from the output current capability of the buck.

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Table 4. Device Characteristics, Continued

V_{REC_OUT} = $V_{BUCK5VR\_IN}$ = V_{REG_IN} = 12V; $\overline{EN}$ = LOW; $\overline{RESET}$= HIGH, Synchronous Rectifier, LDO2P5V, LDO5V, and DC/DC Converter blocks must be operated together, unless otherwise noted. T_A = 0 to +85°C. Typical values are at 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
LDO5V						
V_{OUT}	Output voltage	5.5V≤ Vin ≤ 18V, I_{OUT}=5mA	4.75	5	5.25	V
I_{SCP}	Short-circuit protection current				20	mA
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		150		°C
T_{SD-HYS}	Hysteresis			30		°C
Microcontroller						
F_{CLOCK}	Clock frequency			12		MHz
V_{MCU}	MCU supply voltage			2.5		V
$\overline{ENABLE}$						
V_{IH}			1.25			V
V_{IL}					0.4	V
I	$\overline{EN}$ input current	$V_{\overline{EN}}$ = 0V, V_{REG_IN} = 18V	-1		+1	µA
		$V_{\overline{EN}}$ = 5V, V_{REG_IN} = 18V	6		10	µA
		$V_{\overline{EN}}$ = 20V, V_{REG_IN} = 18V	45		60	µA
General-Purpose Inputs/Outputs (GPIO)						
V_{IH}	Input Threshold High	Note:2	0.7*$V_{LDO2P5V\_IN}$			V
V_{IL}	Input Threshold Low				0.3*$V_{LDO2P5V\_IN}$	V
I_{LKG}	Input Leakage		-1		+1	µA
V_{OH}	Output Logic High	I_{OH} = -8mA	4			V
V_{OL}	Output Logic Low	I_{OL} = 8mA			0.4	V
$\overline{RESET}$						
V_{IH}	Input Threshold High		0.7*$V_{LDO2P5V\_IN}$			V
V_{IL}	Input Threshold Low				0.3*$V_{LDO2P5V\_IN}$	V
$R_{PU\ RESET}$	Internal pull-up resistance			10		kΩ
SCL, SDA (I^2C Interface)						
f_{SCL}	Clock Frequency	IDTP9023 as Slave	0		400	kHz
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs

Note 2: - The GPIO connected to the ADC have a max operating input voltage of 2.44V to prevent saturation of the ADC.

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Table 4. Device Characteristics, Continued

V_{REC_OUT} = $V_{BUCK5VR\_IN}$ = V_{REG_IN} = 12V; $\overline{EN}$ = LOW; $\overline{RESET}$ = HIGH, Synchronous Rectifier, LDO2P5V, LDO5V, and DC/DC Converter blocks must be operated together, unless otherwise noted. T_A = 0 to +85°C. Typical values are at 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
$t_{HD:STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		10			ns
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line			150		pF
C_{BIN}	Input Capacitance			5		pF
V_{IL}	Input Threshold Low				0.7	V
V_{IH}	Input Threshold High		1.4			V
I_{LKG}	Input Leakage Current		-1		+1	µA
V_{OL}	Output Logic Low	I_{OL}= 4mA			0.4	V

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TYPICAL PERFORMANCE CHARACTERISTICS

Typical Performance Characteristics: System Efficiency versus RX Output Power
$\overline{EN}$ = 0, $\overline{RESET}$ = 1, TA = 25°C

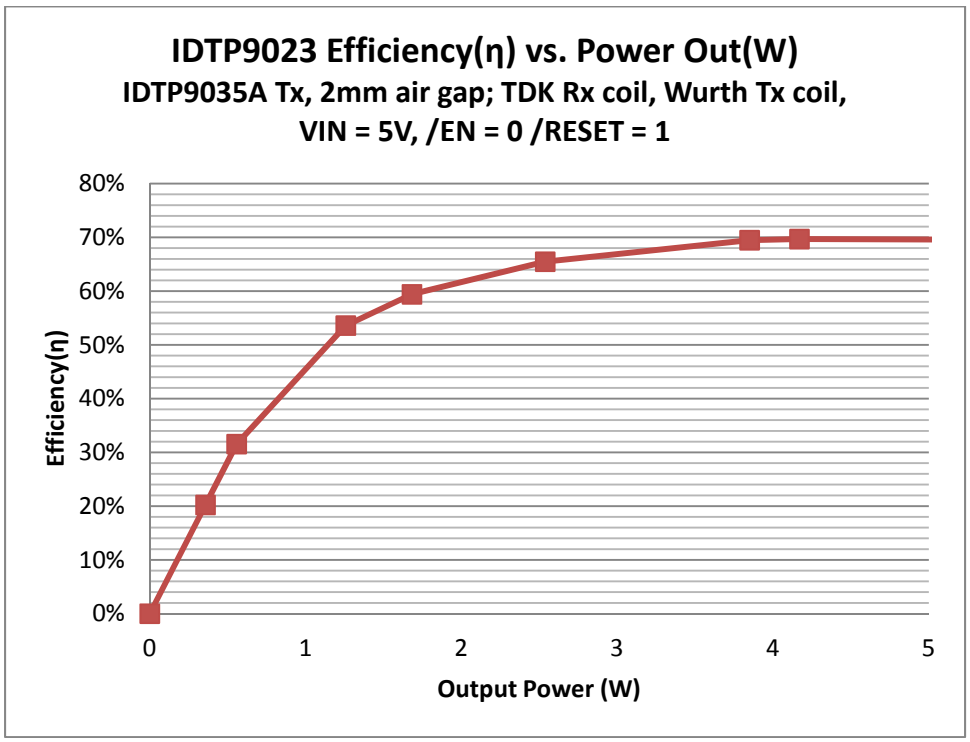

Figure 1 – IDTP9023 input DC to Output DC total system efficiency with IDTP9035A WPC QI Transmitter.

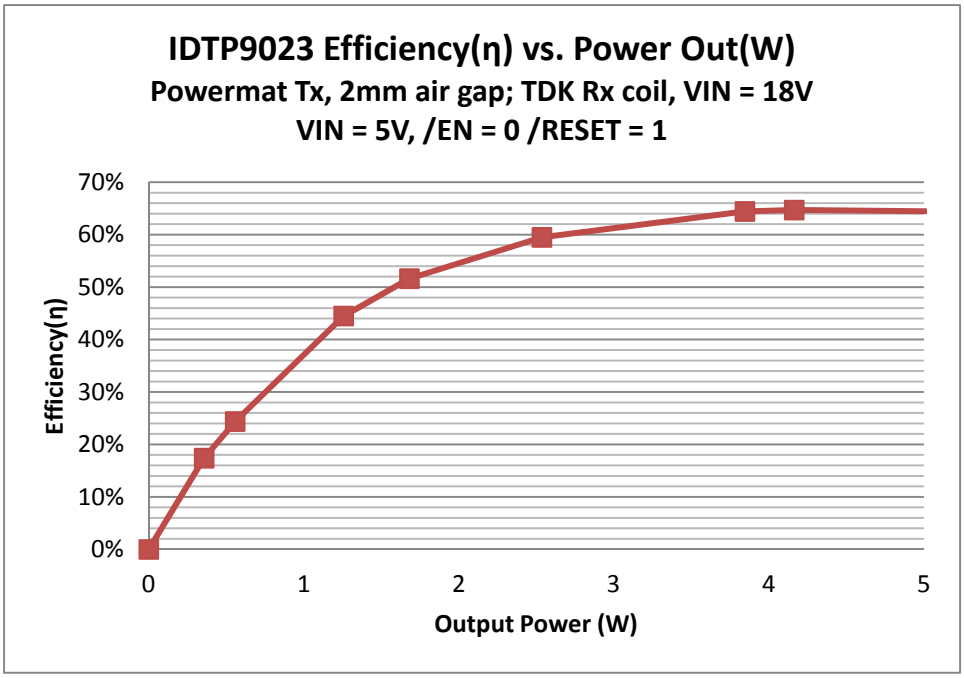

Figure 2 – IDTP9023 input DC to Output DC total system efficiency with Powermat PMA Transmitter.

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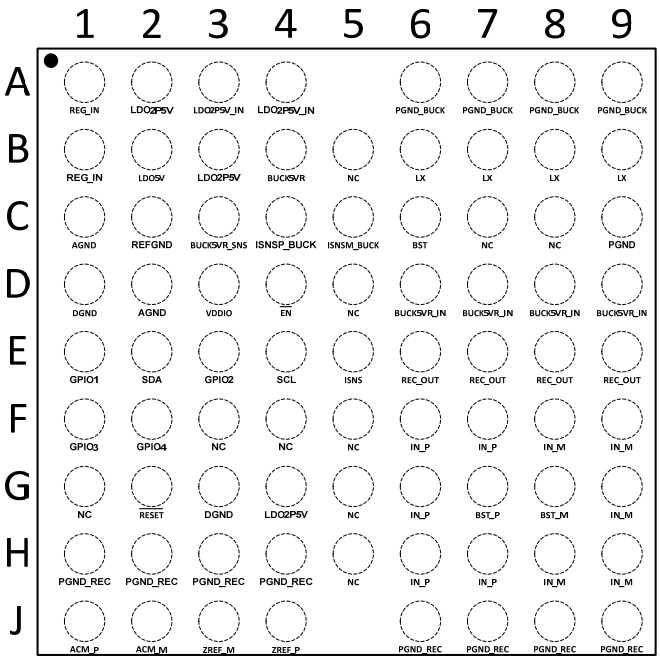
PIN CONFIGURATION & DESCRIPTION

Top View



Bottom View

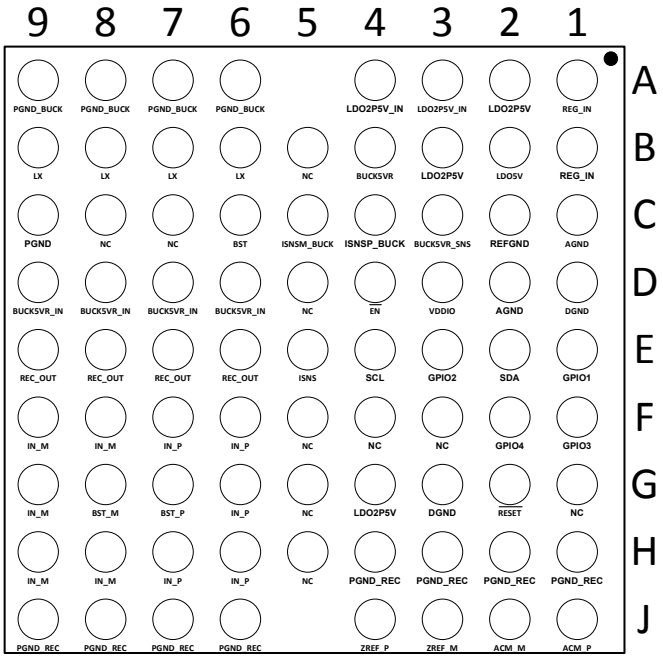


Figure 3: WLCSP-79, 4.095x3.898mm -9x9, 0.4 mm Pitch

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PIN DESCRIPTION

Table 5. WLCSP Ball Functions by Pin Number (See Figure 3)

PIN	NAME	TYPE	DESCRIPTION
A1	REG_IN	I	Analog power supply input
A2	LDO2P5V	O	Analog/Digital supply output. Do not load with more than 7mA during startup, or more than 100mA when in regulation.
A3	LDO2P5V_IN	I	Analog power supply input
A4	LDO2P5V_IN	I	Analog power supply input
A5		-	No ball, internally connected
A6	PGND	-	Switching regulator power ground
A7	PGND	-	Switching regulator power ground
A8	PGND	-	Switching regulator power ground
A9	PGND	-	Switching regulator power ground
B1	REG_IN	I	Analog power supply input
B2	LDO5V	O	5V analog supply output
B3	LDO2P5V	O	Analog/Digital supply output. Do not load with more than 7mA during startup, or more than 100mA when in regulation.
B4	BUCK5VR	I	Power and digital supply input
B5	NC	-	Not internally connected. This pin may be connected to others to facilitate routing or to improve thermal performance.
B6	LX	I/O	Switching regulator switch node
B7	LX	I/O	Switching regulator switch node
B8	LX	I/O	Switching regulator switch node
B9	LX	I/O	Switching regulator switch node
C1	AGND	-	Analog ground

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Table 5. WLCSP Ball Functions by Pin Number (Continued, see Figure 3)

PIN	NAME	TYPE	DESCRIPTION
C2	REFGND	-	Signal ground. Must be connected to AGND.
C3	BUCK5VR_SNS	I	Switching regulator feedback
C4	ISNSP_BUCK	I	Positive current sense input
C5	ISNSM_BUCK	I	Negative current sense input
C6	BST	I	Switching regulator bootstrap capacitor
C7	NC	-	Internally connected to C8. This pin may be connected to others to facilitate routing or to improve thermal performance.
C8	NC	-	Internally connected to C7. This pin may be connected to others to facilitate routing or to improve thermal performance.
C9	PGND	-	Power ground
D1	DGND	-	Digital ground
D2	AGND	-	Analog ground
D3	VDDIO	I	Digital I/O power supply input for SDA and SCL. Connect VDDIO to the same supply used for the I^2C pull up resistors
D4	$\overline{EN}$	I	Chip enable, active low. LDO5V remains in regulation when chip enable is logic high.
D5	NC	-	Not internally connected. This pin may be connected to others to facilitate routing or to improve thermal performance.
D6	BUCK5VR_IN	I	Switching regulator power supply input
D7	BUCK5VR_IN	I	Switching regulator power supply input
D8	BUCK5VR_IN	I	Switching regulator power supply input
D9	BUCK5VR_IN	I	Switching regulator power supply input
E1	GPIO1	I/O	General-purpose I/O pin. This pin can operate as an analog input with 12-bit resolution or as a digital I/O.

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Table 5. WLCSP Ball Functions by Pin Number (Continued, see Figure 3)

PIN	NAME	TYPE	DESCRIPTION
E2	SDA	I/O	I²C data
E3	GPIO2	I/O	General-purpose I/O pin. This pin is a digital I/O.
E4	SCL	I	I²C clock
E5	ISNS	O	Current sense output signal
E6	REC_OUT	O	Rectified output
E7	REC_OUT	O	Rectified output
E8	REC_OUT	O	Rectified output
E9	REC_OUT	O	Rectified output
F1	GPIO3	I/O	General-purpose I/O pin. This pin can operate as an analog input with 8-bit resolution or as a digital I/O.
F2	GPIO4	I/O	General-purpose I/O pin. This pin can operate as an analog input with 8-bit resolution or as a digital I/O.
F3	NC	I	No connect, internally connected. This pin must be left floating.
F4	NC	I	No connect, internally connected. This pin must be left floating.
F5	NC	-	Internally connected to G5 and H5. This pin may be connected to others to facilitate routing or to improve thermal performance.
F6	IN_P	I	Positive bridge input
F7	IN_P	I	Positive bridge input
F8	IN_M	I	Negative bridge input
F9	IN_M	I	Negative bridge input
G1	NC	I	No connect, internally connected. This pin must be left floating.
G2	$\overline{\text{RESET}}$	I	Chip reset, active low. This pin has an internal 10kΩ pull-up to 5V.

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Table 5. WLCSP Ball Functions by Pin Number (Continued, see Figure 3)

PIN	NAME	TYPE	DESCRIPTION
G3	DGND	-	Digital ground
G4	LDO2P5V	I	LDO2P5V output sense
G5	NC	-	Internally connected to F5 and H5. This pin may be connected to others to facilitate routing or to improve thermal performance.
G6	IN_P	I	Positive bridge input
G7	BST_P	I	Rectifier positive bootstrap capacitor
G8	BST_M	I	Rectifier negative bootstrap capacitor
G9	IN_M	I	Negative bridge input
H1	PGND	-	AC Modulation and Clamp power ground
H2	PGND	-	AC Modulation and Clamp power ground
H3	PGND	-	AC Modulation and Clamp power ground
H4	PGND	-	AC Modulation and Clamp power ground
H5	NC	-	Internally connected to F5 and G5. This pin may be connected to others to facilitate routing or to improve thermal performance.
H6	IN_P	I	Positive bridge input
H7	IN_P	I	Positive bridge input
H8	IN_M	I	Negative bridge input
H9	IN_M	I	Negative bridge input
J1	ACM_P	I	AC modulation input, positive end
J2	ACM_M	I	AC modulation input, negative end
J3	ZREF_M	I	AC clamp, positive end
J4	ZREF_P	I	AC clamp, negative end

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Table 5. WLCSP Ball Functions by Pin Number (Continued, see Figure 3)

PIN	NAME	TYPE	DESCRIPTION
J5		-	No ball, internally connected
J6	PGND	-	Rectifier power ground
J7	PGND	-	Rectifier power ground
J8	PGND	-	Rectifier power ground
J9	PGND	-	Rectifier power ground

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SIMPLIFIED BLOCK DIAGRAM

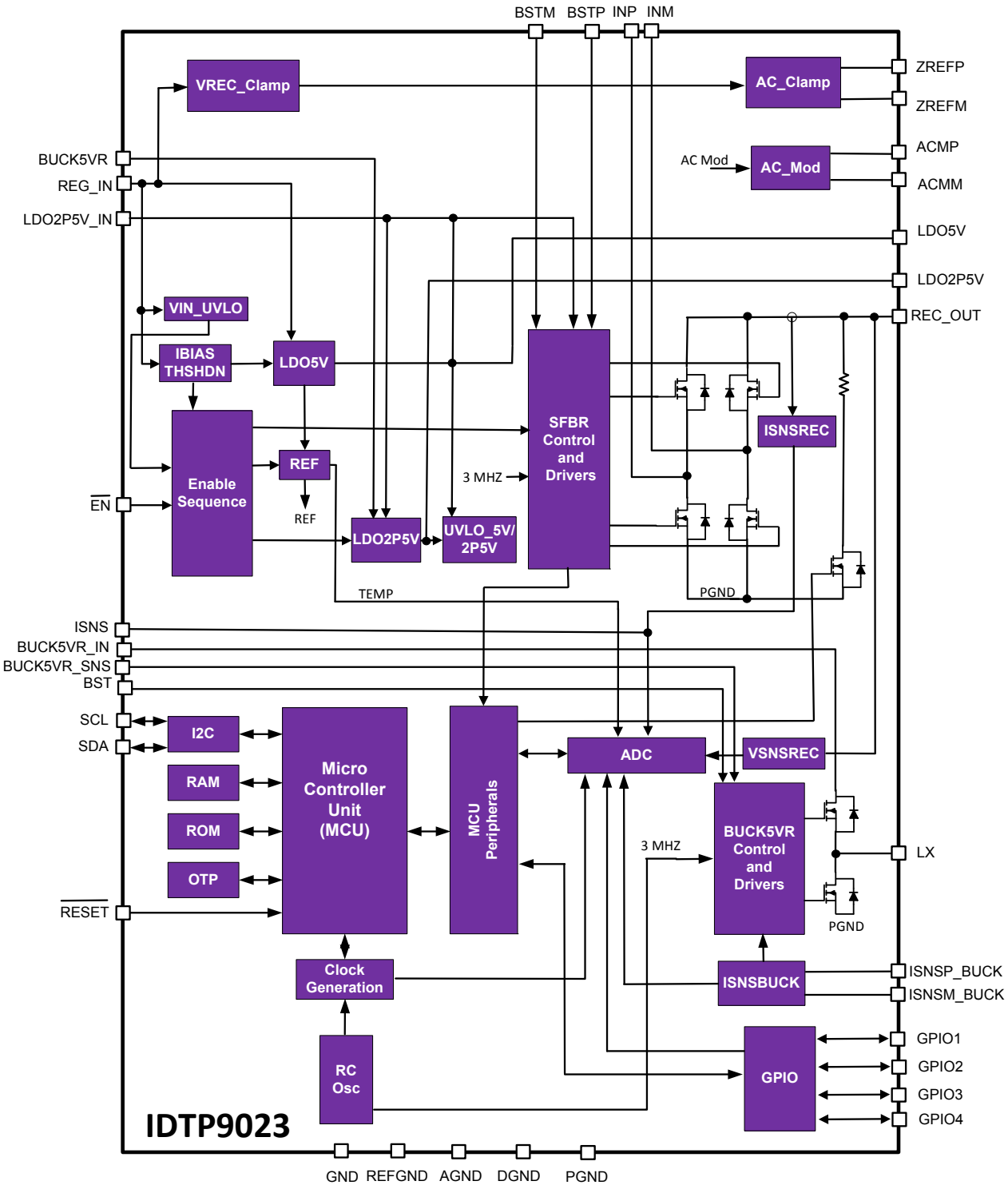

Figure 4: IC Internal Block Diagram

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Description of the Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. A WPC[1] transmitter may be a *free-positioning* or *magnetically-guided* type. PMA[2] supports only the *magnetically-guided* configuration. A *free-positioning* type of transmitter has an array of coils that gives limited spatial freedom to the end-user, whereas a *magnetically-guided* type of transmitter helps the end-user align the receiver to the transmitter with a magnetic attraction.

The amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The communication is purely digital, and communication 1's and 0's ride on top of the power link that exists between the two coils.

A large part of the efficiency of the wireless charging system arises from the fact that when it's not actually charging a mobile device, the transmitter is in a very-low-power sleep mode. Until the transmitter detects the presence of a receiver, it remains in a low-power state.

Theory of Operation

The IDTP9023 is a highly-integrated wireless power receiver IC solution for mobile devices. It can transfer up to 5W of power in WPC Qi and PMA modes, from a wireless transmitter to a load (e.g., a battery charger) using near-field magnetic induction.

Note 1 - Refer to the WPC specification at http://www.wirelesspowerconsortium.com/ for the most current information

Note 2 – PMA members can download the most current PMA Receiver Interoperability Specification at http://www.powermatters.org.

OVERVIEW

The simplified block diagram of the IDTP9023 is shown in Figure 2. An external inductor and two capacitors transfer energy from the transmitter's coil through the IDTP9023's IN_M and IN_P pins to be full-wave-rectified and stored on a capacitor connected to REC_OUT. Until the voltage across the capacitor exceeds the threshold of the VIN_UVLO block, the rectification is performed by the body diodes of the Synchronous Full Bridge Rectifier FETs. After the internal biasing circuit is enabled, the SFBR Control and Drivers block operates the MOSFET switches in the rectifier for increased efficiency. An internal ADC monitors the voltage at REC_OUT and the load current, and the IDTP9023 sends instructions to the wireless power transmitter to increase or decrease the amount of power transferred or to terminate power transmission. The voltages at the outputs of the voltage regulators and the internal temperature are also monitored to ensure proper operation.

STARTUP

When the voltage at REC_OUT exceeds the Under-Voltage Lock-Out threshold with $\overline{EN}$ at a logic low, the Enable Sequence block is activated, enabling the internal biasing circuitry. When the 5V LDO and the reference voltage are ready, the 2.5V LDO is enabled and power is supplied to the Micro-Controller Unit, the Analog-to-Digital-Converter, the Synchronous Full-Bridge Rectifier, and related circuitry.

EXTERNAL CHIP $\overline{RESET}$ and $\overline{EN}$

The IDTP9023 can be externally reset by pulling the $\overline{RESET}$ pin to a logic LOW below the V_{IL} level. The $\overline{RESET}$ pin is a dedicated active-LOW digital input, and its effect is similar to the power-up reset function. Because of the internal low-voltage monitoring scheme, the use of the external $\overline{RESET}$ pin is not mandatory, the $\overline{RESET}$ pin has an internal 10kΩ pull-up to 5V. A manual external reset scheme can be added by connecting 5V to the $\overline{RESET}$ pin through a simple switch. When $\overline{RESET}$ is LOW, the microcontroller's registers are set to the default configuration. When the $\overline{RESET}$ pin is released to a HIGH, the microcontroller starts executing the code from the internal ROM or the optional external EEPROM.
If the particular application requires the IDTP9023 to be disabled, this can be accomplished with the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled high, either through the internal 10kΩ pullup to 5V or externally, the device is suspended and

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placed in low current (sleep) mode. If pulled low, the device is active.

The current into $\overline{EN}$ is approximately

$$I_{\overline{EN}} = \frac{V_{\overline{EN}} - 2V}{300k\Omega}$$

for input voltages between V_{IN} and +2V, and close to zero if V($\overline{EN}$) is less than 2V.

RECTIFIER and VREC_CLAMP

When the 5V and 2.5V UVLOs have been released, the full-bridge rectifier switches to synchronous mode to more efficiently transfer energy from the transmitter to the load at REC_OUT. VSNSREC monitors the REC_OUT voltage. If the voltage at REC_OUT exceeds V_{RECT_CL}, the VREC_CLAMP turns on two internal FETs to connect IN_P and IN_M to ground through external capacitors, shunting current from the secondary coil away from the IDTP9023. The clamp is released when the voltage at REC_OUT falls below the V_{RECT_CL} hysteresis level. REC_OUT must not be directly loaded.

DC/DC CONVERTER

The 5V buck switching regulator is turned on shortly after the 2.5V LDO is activated, operating at 3MHz with internal power FETs and regulating the voltage at BUCK5VR to 5V. When the buck switcher reaches regulation, it provides power to the IDTP9023's internal circuitry and the external load.

LDOs

In addition to the 5V buck switching regulator, the IDTP9023 has two low-drop-out linear regulators to power internal circuitry. Avoid injecting noise into the LDO output pins, as these pins power sensitive circuitry in the device.

POWER CONTROL

The voltage at REC_OUT and the current through the rectifier are sampled periodically by the VSNSREC and ISNSREC blocks, and digitized by the ADC. The digital equivalents of the voltage and current are supplied to the MCU, which decides whether the loading conditions on REC_OUT indicate that a change in the operating point is required. If the load is heavy enough to bring the voltage at REC_OUT below its target, the transmitter is instructed to move its frequency lower, closer to resonance. If the voltage at REC_OUT is higher than its target, the transmitter is instructed to increase its frequency.

MODULATION/COMMUNICATION

In both WPC and PMA applications, receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's inductor. To the transmitter, this appears as an impedance change which results in measurable variations of the transmitter's output waveform. The communication protocols are covered in the documentation from the WPC and PMA.

I²C Communication

The IDTP9023 includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the IDTP9023 will initially become I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. In some configurations, the I²C master is disabled. The I²C Master mode on the IDTP9023 does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the IDTP9023 has finished any firmware uploading and has released control of the bus as I²C Master.

After any firmware uploading from external memory is complete, and when the IDTP9023 begins normal operation, the IDTP9023 is normally configured by the firmware to be exclusively in I²C Slave mode.

EEPROM

The IDTP9023 could use an external EEPROM which contains either standard or custom TX firmware. The external EEPROM memory chip is pre-programmed with a standard start-up program that is automatically loaded when the voltage on REC_OUT is high enough to enable the IDTP9023's MCU. The IDTP9023 uses I²C slave address 0x50 to access the EEPROM. The IDTP9023 slave address is 0x39. The EEPROM can be reprogrammed to update the start-up program using the IDT Windows GUI (see the IDTP9023 Demo Board User Manual for complete details). The IC will look initially for an external EEPROM and use the firmware built into the IC ROM if no external memory device is found. A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard default/built-in firmware is not suitable for the application, custom ROM options are possible. Please contact IDT sales for more information. IDT will provide the appropriate image in the format best suited to the application.

OSCILLATOR

An internal RC oscillator generates the frequencies at which the MCU and buck switching regulator operate.

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SIMPLIFIED APPLICATION DIAGRAMS

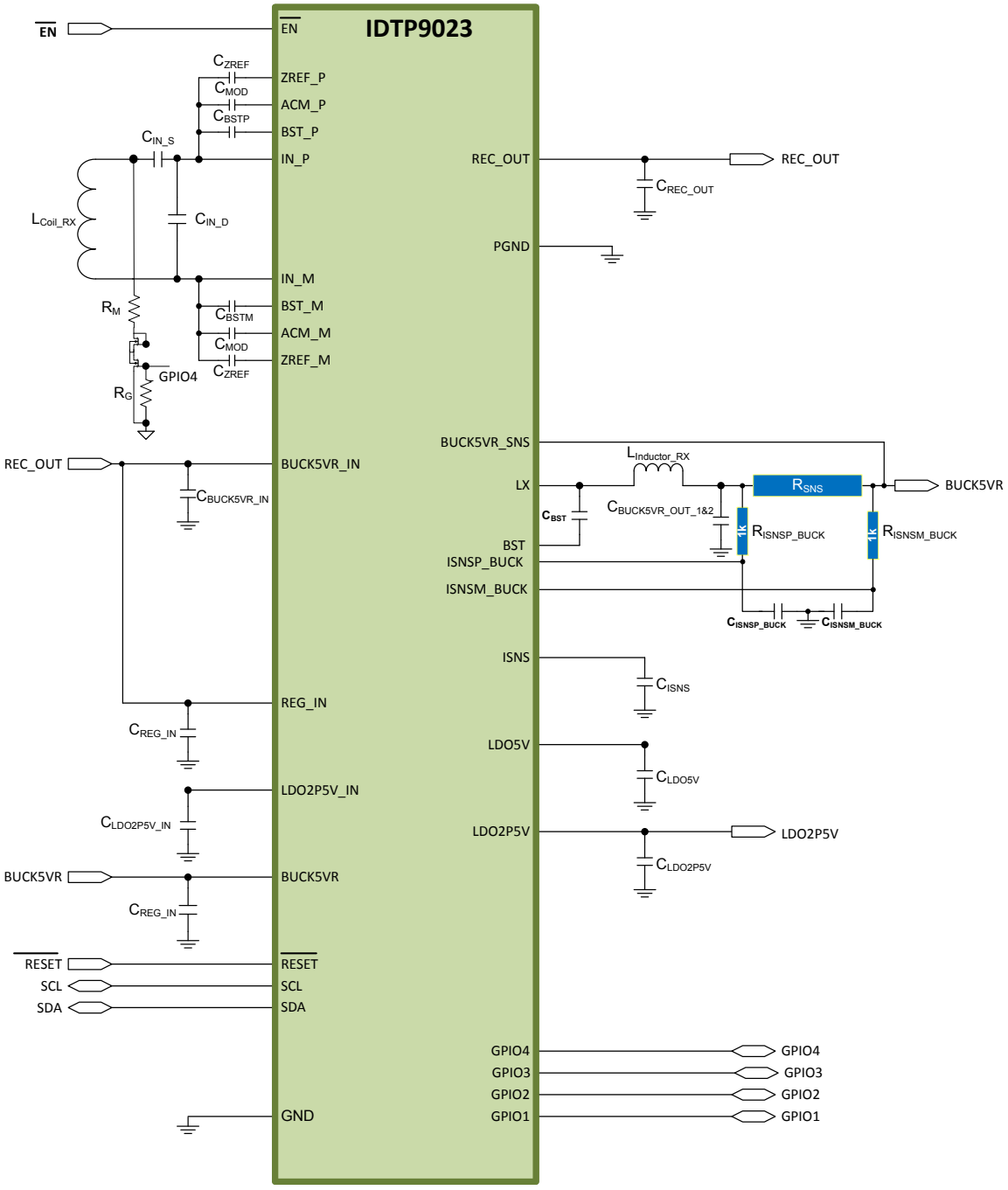

Figure 5: IDTP9023 Simplified Typical Application Circuit

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SIMPLIFIED SYSTEM DIAGRAM

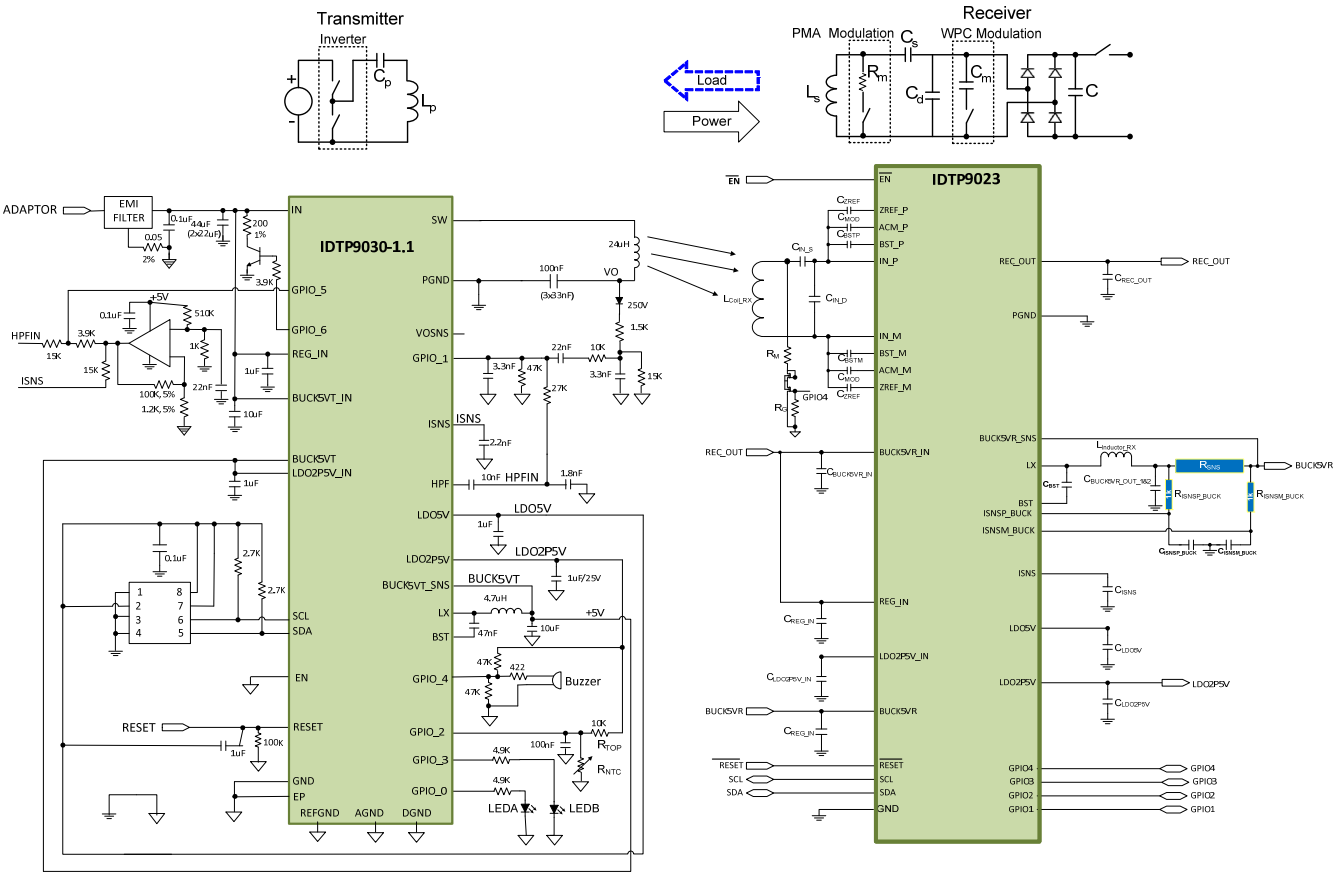

Figure 6: Simplified Typical System Application Circuit

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DETAILED SYSTEM DIAGRAM

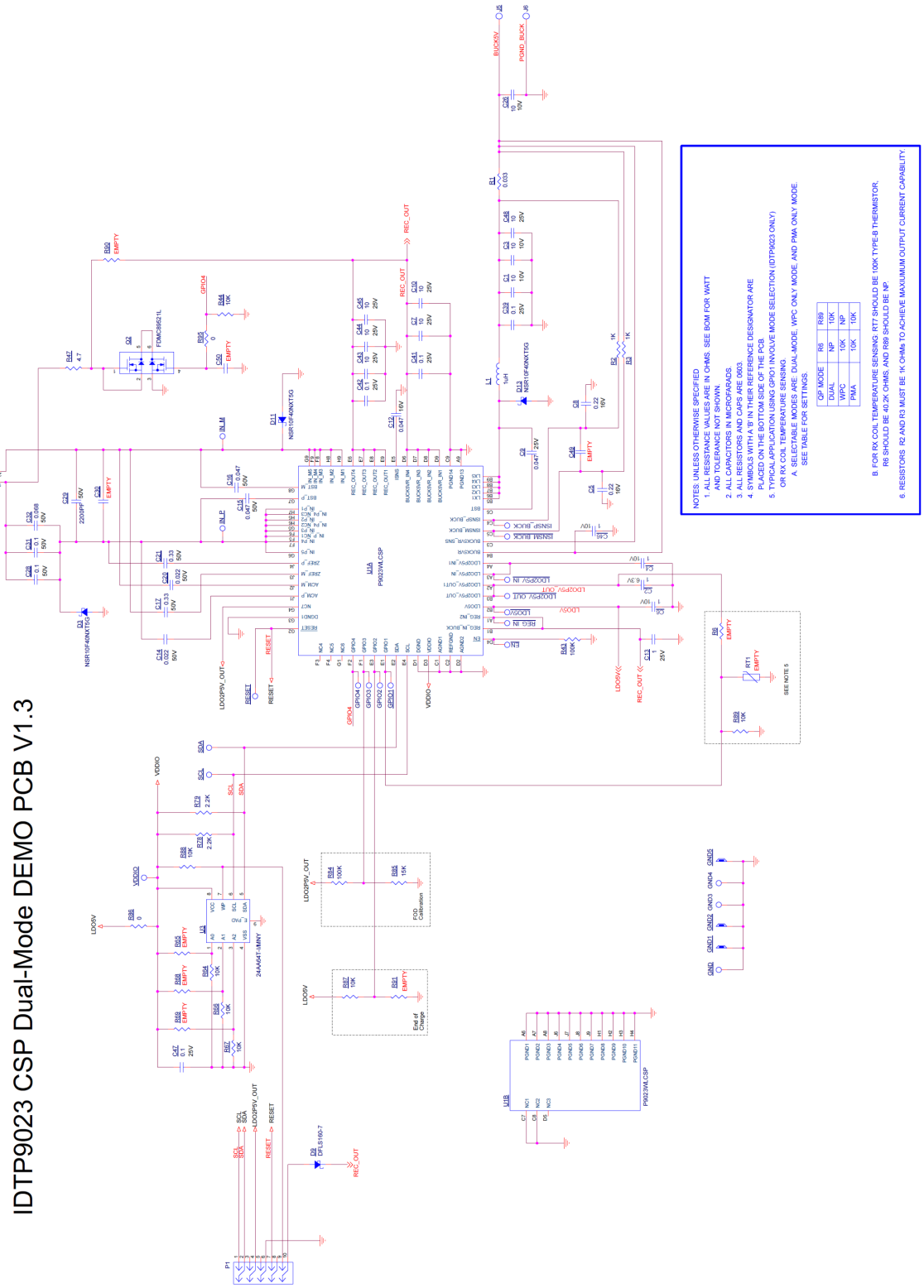

Figure 7: IDTP9023 Preliminary Dual-mode WPC/PMA Application Schematic

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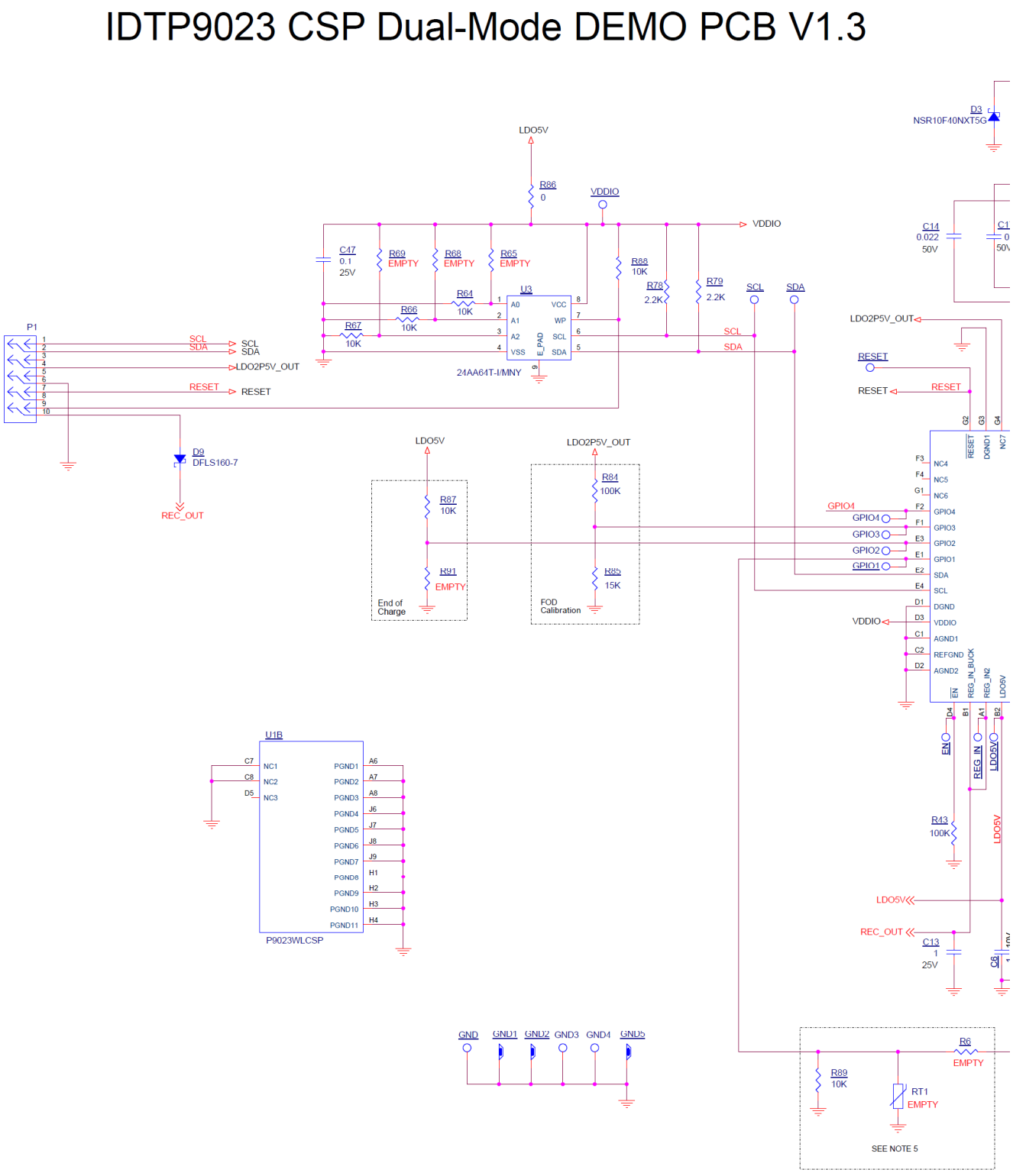

Figure 7a: Left side of IDTP9023 Preliminary Dual-mode WPC/PMA Application Schematic

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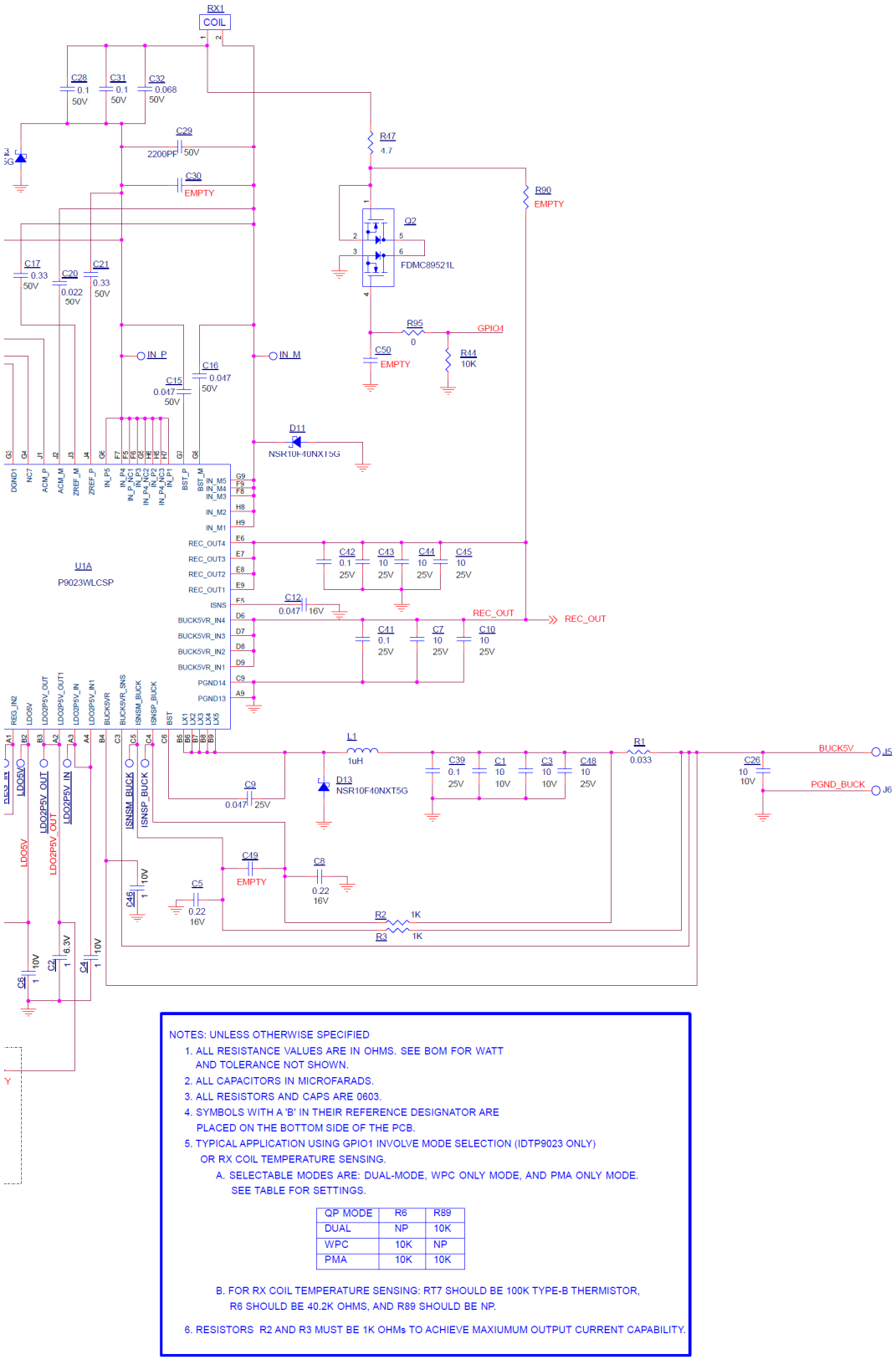

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS. SEE BOM FOR WATT AND TOLERANCE NOT SHOWN.
2. ALL CAPACITORS IN MICROFARADS.
3. ALL RESISTORS AND CAPS ARE 0603.
4. SYMBOLS WITH A 'B' IN THEIR REFERENCE DESIGNATOR ARE PLACED ON THE BOTTOM SIDE OF THE PCB.
5. TYPICAL APPLICATION USING GPIO1 INVOLVE MODE SELECTION (IDTP9023 ONLY) OR RX COIL TEMPERATURE SENSING.
   A. SELECTABLE MODES ARE: DUAL-MODE, WPC ONLY MODE, AND PMA ONLY MODE. SEE TABLE FOR SETTINGS.

QP MODE	R6	R89
DUAL	NP	10K
WPC	10K	NP
PMA	10K	10K

   B. FOR RX COIL TEMPERATURE SENSING: RT7 SHOULD BE 100K TYPE-B THERMISTOR, R6 SHOULD BE 40.2K OHMS, AND R89 SHOULD BE NP.
6. RESISTORS R2 AND R3 MUST BE 1K OHMs TO ACHIEVE MAXIUMUM OUTPUT CURRENT CAPABILITY.

Figure 7b: Right side of IDTP9023 Preliminary Dual-mode WPC/PMA Application Schematic

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COMPONENTS SELECTION

Table 6. Component List

Item	Quantity	Reference	Part Number	Value	PCB Footprint
1	3	C1,C3,C26	CL05A106MP5NUNC	10	402
2	1	C2	C0603X5R0J105M030BC	1	201
3	3	C4,C6,C46	CL03A105MP3NSNC	1	201
4	2	C5,C8	C0603X5R1E224K030BC	0.22	201
5	5	C7,C10,C43,C44,C45	GRM188R61E106MA73	10	603
6	2	C9,C12	C0603X5R1E473K030BB	0.047	201
7	1	C13	TMK105BJ105MV-F	1	402
8	2	C14,C20	CGJ2B3X7R1H223K050BB	0.022	402
9	2	C15,C16	CGA2B3X7R1H473K050BD	0.047	402
10	2	C17,C21	C1608X5R1H334K	0.33	603
11	2	C28,C31	C1608X7R1H104K080AA	0.1	603
12	2	C29,C30	C1005X7R1H222K050BA	2200PF	402
13	1	C32	C1608X7R1H683K	0.068	603
14	4	C39,C41,C42,C47	C0603X5R1E104K030BB	0.1	201
15	4	D3,D11, D13	NSR10F40NXT5G	NSR10F40NXT5G	0502_diode
16	1	D9	DFLS160-7	DFLS160-7	DFLS160
17	10	GPIO1,GPIO2,GPIO3,GPIO4,	5002	WHT	80-40pth
		SDA,SCL,RESET,ISNSP_BUCK,			
		ISNSM_BUCK,EN			
18	6	GND1,GND2,GND3,GND4,GND5,	5001	WHT	80-40pth
		GND			
19	7	LDO5V,LDO2P5V_OUT,	5000	WHT	80-40pth
		LDO2P5V_IN,VDDIO,REG_IN,			
		IN_P,IN_M			
20	2	J5,J6	S1751-46R	1P	SMT3-65X2-05
21	1	L1	DFE252010C-1R0M	1uH	IND-HUTCH3X
22	1	P1	5103308-1	10P	HEADER10P2Rlatch
23	1	Q2	FDMC89521L	FDMC89521L	FET_PWR_33
24	1	RT7	91700011	100K	JUMPER2PIN01IN
25	1	RX1	760308201 WR-483250-15M2-G (with added FK2 Ferrite)	10uH	COIL_9022
26	1	R1	UCR10EVHJSR033	0.033	0805_SENSE
27	2	R2,R3	ERJ-1GEF1001C	1K	201
28	1	R6	ERJ-2RKF4022X	40.2K	402
29	2	R43,R84	ERJ-1GEJ104C	100K	201
30	1	R44	ERJ-1GEJ103C	10K	201
31	1	R47	ERJ-3GEYJ2R4V	2.4	603
32	7	R64,R65,R66,R67,R68,R69,	ERJ-2GEJ103X	10K	402
		R88			
33	2	R78,R79	ERJ-2GEJ222X	2.2K	402
34	1	R85	ERJ-1GEF1502C	15K	201
35	1	R86	MCT06030Z0000ZP500	0	603
36	1	R87	ERJ-2GEJ103X	10K	201
37	1	U1	P9023	IDTP9023	BGA_IDTP9022_CSP
38	1	U3	24AA64T-I/MNY	24AA64T-I/MNY	TDFN08
39	1	6		SCH_NOTES	

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FUNCTIONAL DESCRIPTION

The IDTP9023 is a highly-integrated single-chip receiver-side WPC Qi/PMA compliant solution. It can deliver up to 5W to the external load through a high-efficiency synchronous buck converter. Incoming AC power from the resonant tank is conditioned and rectified through a full-wave synchronous rectifier and regulated down to 5V for delivery to the system as shown below:

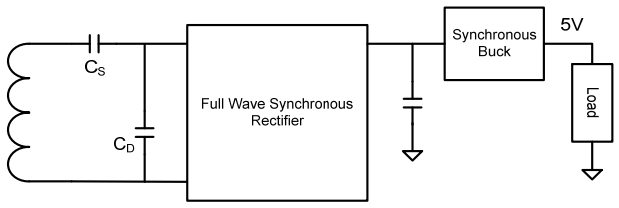

Figure 8: Wireless power delivery to the load

Modulation

The IDTP9023 is compatible with all WPC-recommended coils: RX-A,B,C,D, and with PMA Type 1 coils. Each receiver coil type has a unique inductance value. As such, a unique resonant capacitor is used for a given type of receiver coil. Additionally, each receiver type has a unique modulation capacitor, for WPC it is C_{MOD}, as shown below:

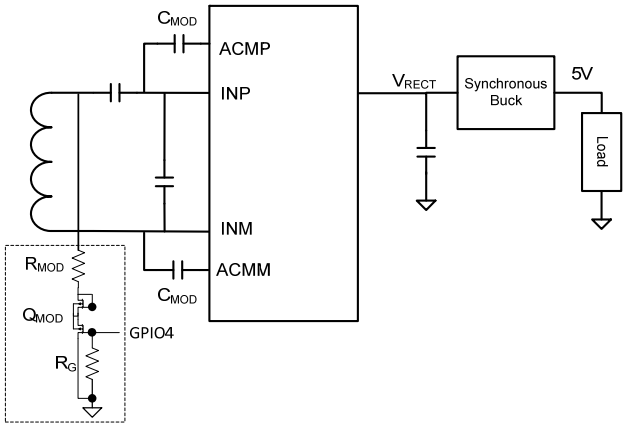

Figure 9: Modulation components

PMA compliant systems require the modulation components and connections shown in the dashed box, R_{MOD}, Q_{MOD} and R_G. Consult the factory for assistance with configuring a system with a specific coil type.

Communication

The IDTP9023 communicates with the base via communication packets, which follow different protocols between the WPC and PMA. For further information on receiver-to-transmitter communication, refer to the WPC and PMA websites.

System Feedback Control

The IDTP9023 is fully compatible with WPC specification Rev. 1.1 and PMA specification 1.0, and has all necessary circuitry to communicate with the base station via WPC/PMA-compliant communication packets.

The wireless power delivery system comprising the transmitter and receiver (e.g., IDTP9030 and IDTP9023) goes through phases of discovery, identification, sustained power transfer, and end-of-power-delivery, all contingent upon successful communication from the receiver to the transmitter. If communication is lost (for example, the wireless is removed from the charging pad), the transmitter terminates power transfer.

OVER-VOLTAGE/TEMPERATURE PROTECTION

If the voltage at REC_OUT exceeds V_{RECT_CL}, the VREC_CLAMP turns on two internal FETs to connect IN_P and IN_M to ground through external capacitors, shunting current from the secondary coil away from the IDTP9023. The clamp is released when the voltage at REC_OUT falls below the V_{RECT_CL} hysteresis level. REC_OUT must not be directly loaded.

The internal temperature is monitored, and the IDTP9023 is temporarily deactivated if the temperature exceeds approximately 150°C and reactivated when the temperature falls below 120°C.

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APPLICATIONS INFORMATION

External Components

The IDTP9023 requires a minimum number of external components for proper operation, as indicated in Figure 7 and Table 6.

ADC Considerations

GPIO1, GPIO3, and GPIO4 are connected internally to a successive-approximation ADC via a multiplexed input. GPIO1 maintains the full 12 bit resolution while GPIO3 and GPIO4 are limited to 8 bits.

The GPIO pins that are connected to the ADC have limited input range, so attention should be paid to the maximum input voltages (2.44V). Decoupling capacitors can be added to minimize noise.

GPIO2 is a digital I/O.

Buck Converter

- The input capacitors (C_{IN}) should be connected as close to the BUCK5VR_IN and PGND pins as practical.
- The output capacitor (C_{OUT}) should be connected as close to the PGND pin as possible to minimize switching ripple caused by ground potential differences.
- The high-side gate bootstrap pin requires a small capacitor to pull the DC-DC regulator's HS gate voltage higher than the input voltage level. Connect a 47nF bootstrap capacitor rated above 35V between the BST pin and the LX pin.
- The output-sense connection to the feedback pins should be separated from any power trace. Connect the output-sense trace as close as possible to the load point to avoid additional load regulation errors.
- The power traces, including GND traces, the LX or BUCK5VR traces should be kept short, direct and wide to reduce parasitic resistance that could affect performance. The inductor connection to the LX and BUCK5VR pins should be as short as possible to reduce the magnetic loop. Use several via pads when routing between layers.

LDOs

Input Capacitor

The input capacitors should be located as close as possible to the power pins, LDO2P5V_IN and REG_IN, and ground (GND). Ceramic capacitors are recommended for their lower ESR and small profile. See Table 6 for voltage ratings.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO (LDO2P5V and LDO5V). The output capacitor connection to the ground pin (PGND) should be made as short as practical for maximum device performance. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please contact IDT Inc. for Gerber files that contain the recommended board layout and Application Note #811 which contains additional layout guidelines.
- As with all switching power supplies, especially those providing high current at high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as generate EMI problems. Therefore, use wide and short traces for high current paths.
- An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the IDTP9023. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs because the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout

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techniques should be used to remove the heat due to device power dissipation.

- The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
    1. PC board traces with large cross-sectional areas remove more heat. For optimum results, use large-area PCB patterns with wide copper traces, placed on the uppermost side of the PCB.
    2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
    3. Thermal vias are needed to provide a thermal path to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

Power Dissipation and Thermal Requirements

The IDTP9023 is offered in a WLCSP package, the maximum power dissipation of which is determined by the number of thermal vias between the package and the printed circuit board. The maximum power dissipation of the package is defined by the die's specified maximum operating junction temperature, T_J, of 125°C. The junction temperature rises when the heat generated by the device's power dissipation goes through the package thermal resistance. The WLCSP package has a typical Θ_{JA} of 45°C/W with 14 thermal vias and 66°C/W with no thermal vias. Clearly, maximizing the thermal vias is highly recommended. The techniques as noted in the PCB layout section must be followed when designing the printed circuit board layout, as well as the placement of the IDTP9023 IC package in proximity to other heat-generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing Θ_{JA} (in the order of decreasing influence) are PCB characteristics, thermal vias, and internal package construction. Board designers should keep in mind that the package thermal metric Θ_{JA} is impacted by the characteristics of the PCB itself upon which the IC is mounted. For example, in a still-air environment, as is often the case, a significant amount of the heat generated (~85%) is absorbed by the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and, thus, the board's heat-sinking efficiency.

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation should be calculated:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

In which

$P_{D(MAX)}$ = Maximum Power Dissipation

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP9023 device is 125°C. For the WLCSP package, the maximum recommended power dissipation is:

$$P_{D(Max)} = (125°C - 85°C) / 45°C/W \approx 0.9 \text{ Watt}$$

Thermal Overload Protection

The IDTP9023 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 150°C. To allow the maximum load current on each regulator and the synchronous rectifier, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP9023 is dissipated into the PCB. All the available WLCSP balls (pins) must be soldered to the PCB. NC pins that are indicated as "Not Internally Connected" should be soldered to the PCB ground plane to improve thermal performance with multiple vias exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

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Package Outline Drawing

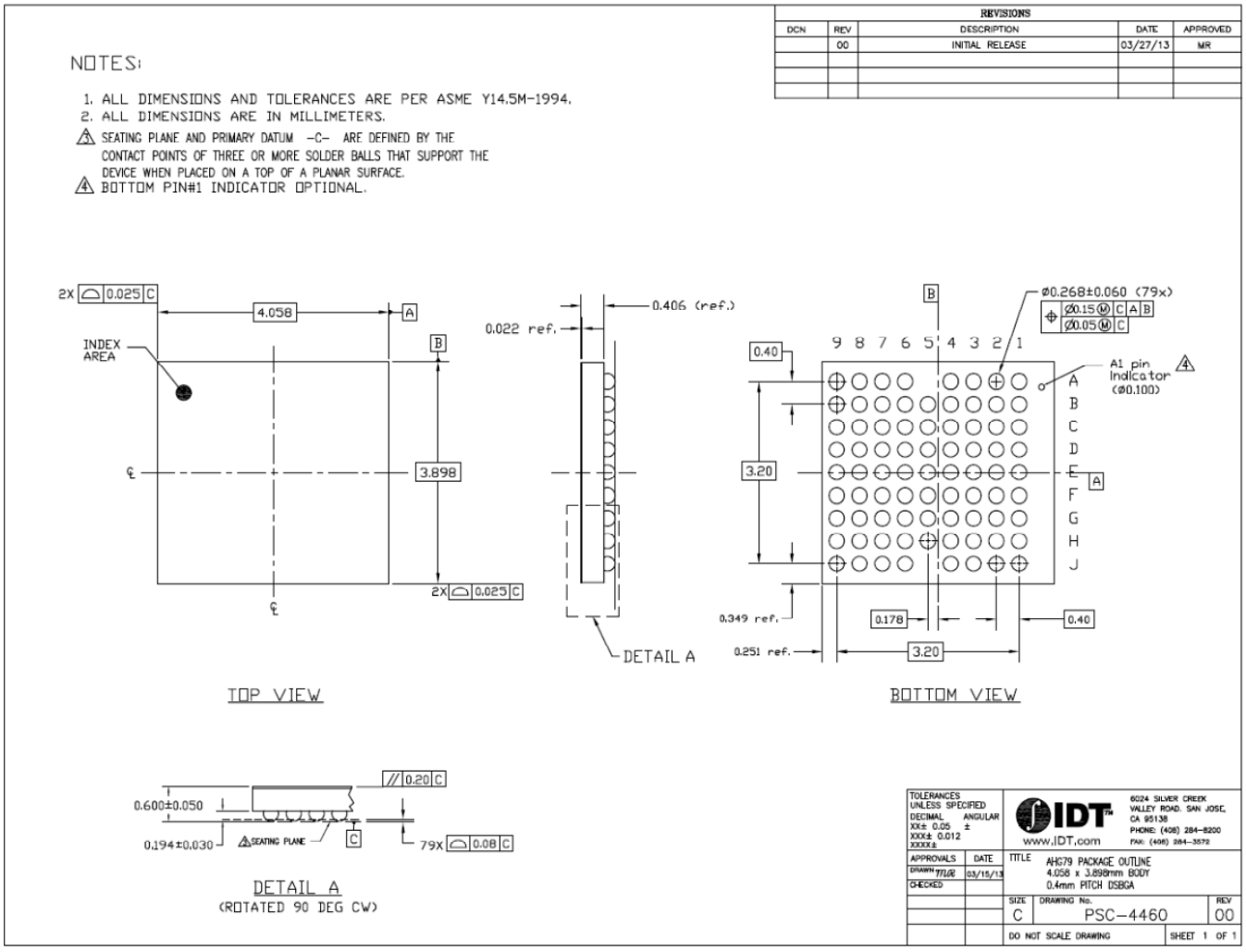

Figure 10: WLCSP-79, 0.4mm pitch POD

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ORDERING GUIDE

Table Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER
P9023-x*AHGI8	P9023-x*AHGI	WLCSP	0°C to +85°C	Tape and reel

*Note – this field is a custom value that is specific to each customer. Please contact your local sales team for your particular value for this field.

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