

Features

- V_{IN} range: 4.25 – 21 Volts
- WPC-1.1.2 compliant
- Up to 7W of power transfer
- 82% peak efficiency
- Integrated power stage drivers
- Low standby power
- Best in class EMI
- Simultaneous Voltage & Current demodulation
- Integrated 32bit ARM® Cortex®-M0 Processor
- Supports I²C interface
- Over-current & over-temperature protection
- Optional Proprietary Back-Channel Communication
- -40 to +85°C temperature range
- Available in QFN5X5-40 package

Applications

- Charging Mats or Pads
- Office Furniture
- Personal Computer Docks
- Portable Instruments

Package: QFN-40 5mmx5mm (See page 16)
 Ordering information (See page 18)

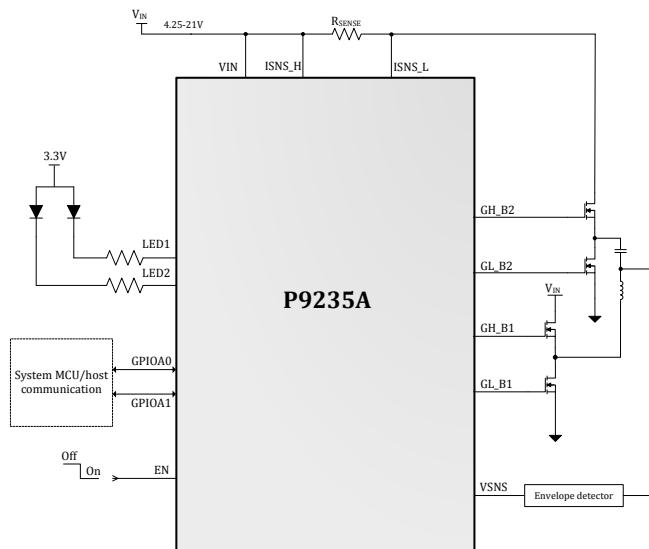
Description

The P9235A is a new 5W, magnetic induction wireless power transmitter product supporting WPC's A5/A11 coil configurations. The system-on-chip integrates power controller, micro-controller, voltage regulation, foreign object detection (FOD), full bridge power stage drivers and on-chip simultaneous voltage and current demodulation. The product is designed to withstand a wide input voltage range of 4.25 to 21V while consuming 1mA of current in the standby mode.

The transmitter includes industry-leading 32bit ARM® Cortex®-M0 processor offering high level of programmability while consuming extremely low standby power meeting the ENERGY STAR® requirement. In addition, the new µController empowers the users to customize features such as LED patterns, buzzer and FOD threshold settings. The device supports the I²C serial interface protocol. The product offers input undervoltage, input overvoltage, output short circuit and over-temperature protection to safeguard the device and system under fault conditions.

The P9235A is available in a Pb-free, space-saving QFN 5mm X 5mm, 40 pin package. The product is rated over an operating temperature range of -40 to +85°C.

Typical Application



ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the P9235A at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods may affect long-term reliability.

Table 1. Absolute Maximum Ratings Summary. (All voltages are referred to ground.)

Pins	Rating	Units
ENB, VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, ISNS_H, ISNS_L, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2	-0.3 to 28	V
REF_CAP, LDO33_CAP, LDO_VIN, LED1, LED2, VDDIO, GPIOA0, GPIOA1, GPIOA2, GPIOA3, GPIOA4, GPIOA5, GPIOA6, GPIOB0, GPIOB1, GPIOB2, GPIOB3, GL_BRG1, GL_BRG2, VSNS_IN, ISNS_IN, ISNS_OUT, DRV_IN	-0.3 to 6	V
GND	+0.3	V
LDO18_CAP	-0.3 to 2	V

Table 2^{1,2,3}. Package Thermal Information

SYMBOL	DESCRIPTION	TQFN RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient	28.5	°C/W
θ_{JC}	Thermal Resistance Junction to Case	21.87	°C/W
θ_{JB}	Thermal Resistance Junction to Board	1.27	°C/W
T_J	Operating Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Notes:

1. The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
2. This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.
3. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3. ESD Information

TEST MODEL	PINS	RATINGS	UNITS
HBM	All pins	+/- 2000	V
CDM	All pins.	+/- 500	V

SPECIFICATION TABLE

Table 4. Device Characteristic

$V_{IN} = 5V$, $V_{DDIO} = 3.3V$, $\bar{EN} = 0V$, $L_P = 6.5\mu H$, $C_P = 400nF$ $T_A = -40$ to $+85^\circ C$. Typical values are at $25^\circ C$, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Input Supplies & UVLO						
V_{IN}^1	Input Operating Range		4.25 ⁵	5.0	21	V
V_{IN_UVLO}	Under-Voltage Lockout	V_{IN} Rising	3.1	3.4	3.6	V
		V_{IN} Falling		3		V
I_{IN}^4	Operating Mode Input Current	Normal power transfer state		10		mA
$I_{STD_BY}^4$	Standby Mode Current	Periodic ping		1		mA
I_{SLP}	Sleep Mode Input Current			85	150	μA
I_{SHD}	Shutdown Current	$ENB = V_{IN}$		25	80	μA
Buck Converter^{3,4} - $C_{out}=20\mu F$; $L=4.7\mu H$						
V_{OUT}	Buck Output Voltage	$V_{IN} > 5.5V$	4.85	5.1	5.35	V
I_{OUT}	Output Current			50		mA
N-Channel MOSFET Drivers						
$T_{LS_ON_OFF}$	Low Side Gate Drive Rise & Fall times	$C_L = 3nF$; 10 – 90%, 90 – 10%		50	150	nS
$T_{HS_ON_OFF}$	High Side Gate Drive rise & Fall times	$C_L = 3nF$; 10 – 90%, 90 – 10%		150	300	nS
Input Current Sense						
V_{SEN_OFST}	Amplifier offset voltage	Measured at $ISNS_OUT$ pin; $ISNS_H = ISNS_L$		0.6		V
$ISENACC_TYP^2$	Measured Current sense accuracy – typical current	$V_{R_ISEN} = 25mV$, $I = 1.25A$		± 3.5		%
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of channels			10		
$V_{IN,FS}$	Full scale Input voltage			2.4		V
LDO18^{3,4} - $C_{out}=1\mu F$; $V_{IN_LDO} = 5.5V$						
V_{OUT18}	Output voltage		1.71	1.8	1.89	V
$\Delta V_{OUT}/V_{OUT}$	Output voltage accuracy			± 5		%
I_{OUT18_MAX}	Maximum load current			10		mA
LDO33^{4,3} - $C_{out}=1\mu F$; $V_{IN_LDO} = 5.5V$						
V_{OUT33}	Output voltage	Programmable; Default setting=3.3V	3.15	3.3	3.45	V
$\Delta V_{OUT}/V_{OUT}$	Output voltage accuracy			± 5		%
I_{OUT33_MAX}	Maximum Output Current			20		mA
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		140		$^\circ C$
		Threshold Falling		120		$^\circ C$

SPECIFICATION TABLE

Table 4. Device Characteristic (Continued)

VIN = 5V, VDDIO=3.3V, EN = 0V, LP = 6.5µH, CP=400nF TA = -40 to +85°C. Typical values are at 25°C, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Clock Oscillators						
F _{LSOSC}	Low speed clock			50		KHz
F _{CLOCK}	OSC clock frequency			6		MHz
F _{CENTER} ⁴	PLL VCO frequency			240		MHz
General Purpose Inputs/Outputs (GPIO)						
V _{IH}	Input high voltage		0.7*VDDIO			V
V _{IL}	Input low voltage			0.3*VDDIO		V
I _{LKG}	Leakage Current		-1.0		1.0	µA
V _{OH}	Output logic high	I=8mA	2.4			V
V _{OL}	Output logic low	I=8mA			0.5	V
SCL, SDA (I²C Interface)						
f _{SCL_MSTR}	Clock Frequency	As I ² C master		400		kHz
f _{SCL_SLV}	Clock Frequency	As I ² C slave		400		kHz
C _B	Capacitive load	For each bus line			100	pF
C _{BIN}	SCL, SDA Input Capacitance			5.0		pF
I _{LKG}	Leakage Current		-1.0		1.0	µA

NOTES:

1. Input Voltage Operating Range is dependent upon the type of Transmitter Power Stage (full-bridge, half-bridge) and Transmitting Coil Inductance. WPC Specifications should be consulted for appropriate input voltage ranges by end product type.
2. A 20mΩ, 1% or better sense resistor & 4.7 Ω, 1% input filter resistor is required to meet the FOD specification.
3. Do not externally load. For internal biasing only.
4. Guaranteed by design and not subject to 100% production testing
5. This is the minimum IC operating specification. Full power transfer will not occur at this level.

TYPICAL PERFORMANCE CHARACTERISTICS

Typical Performance Characteristics: System Efficiency versus RX Output Power

TA = 25°C

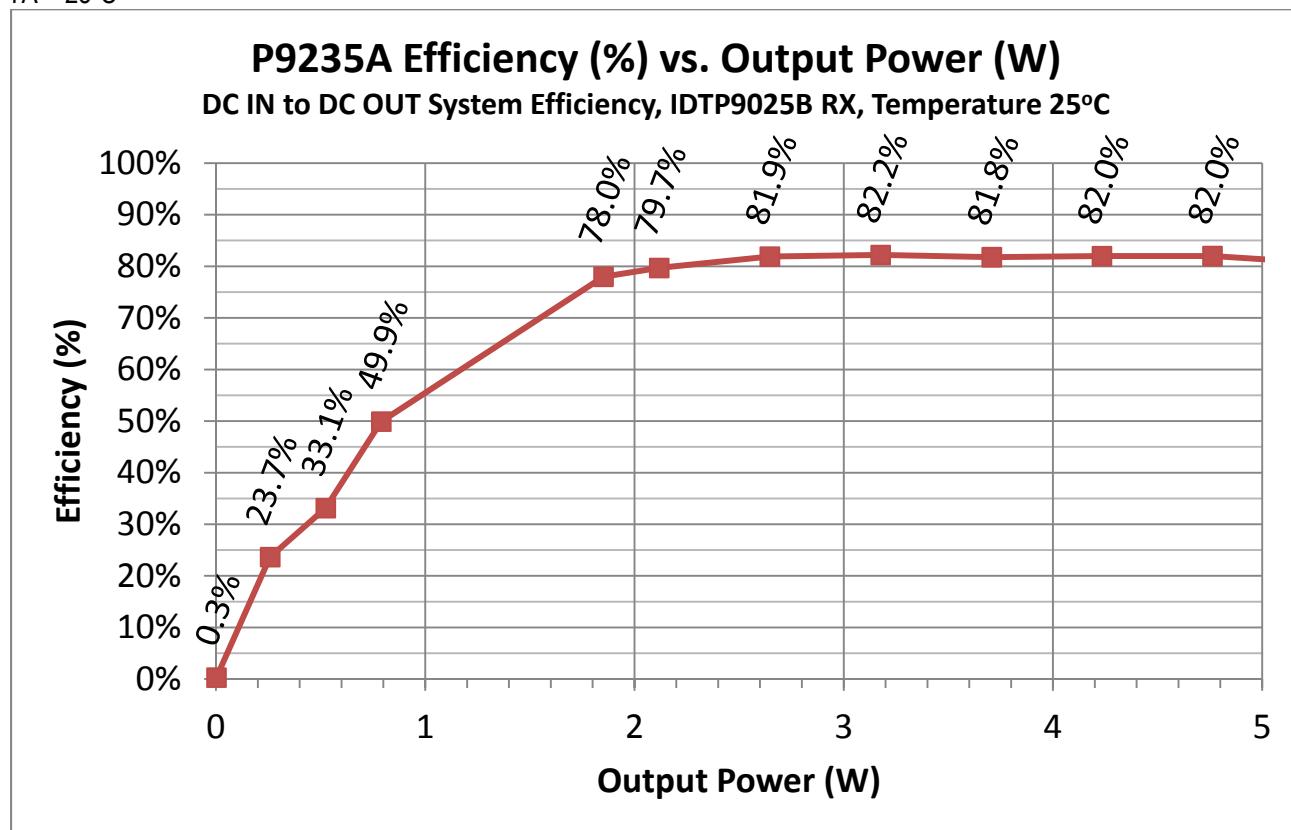


Figure 1. P9235A System Efficiency versus Output Power

PIN CONFIGURATION & DESCRIPTION

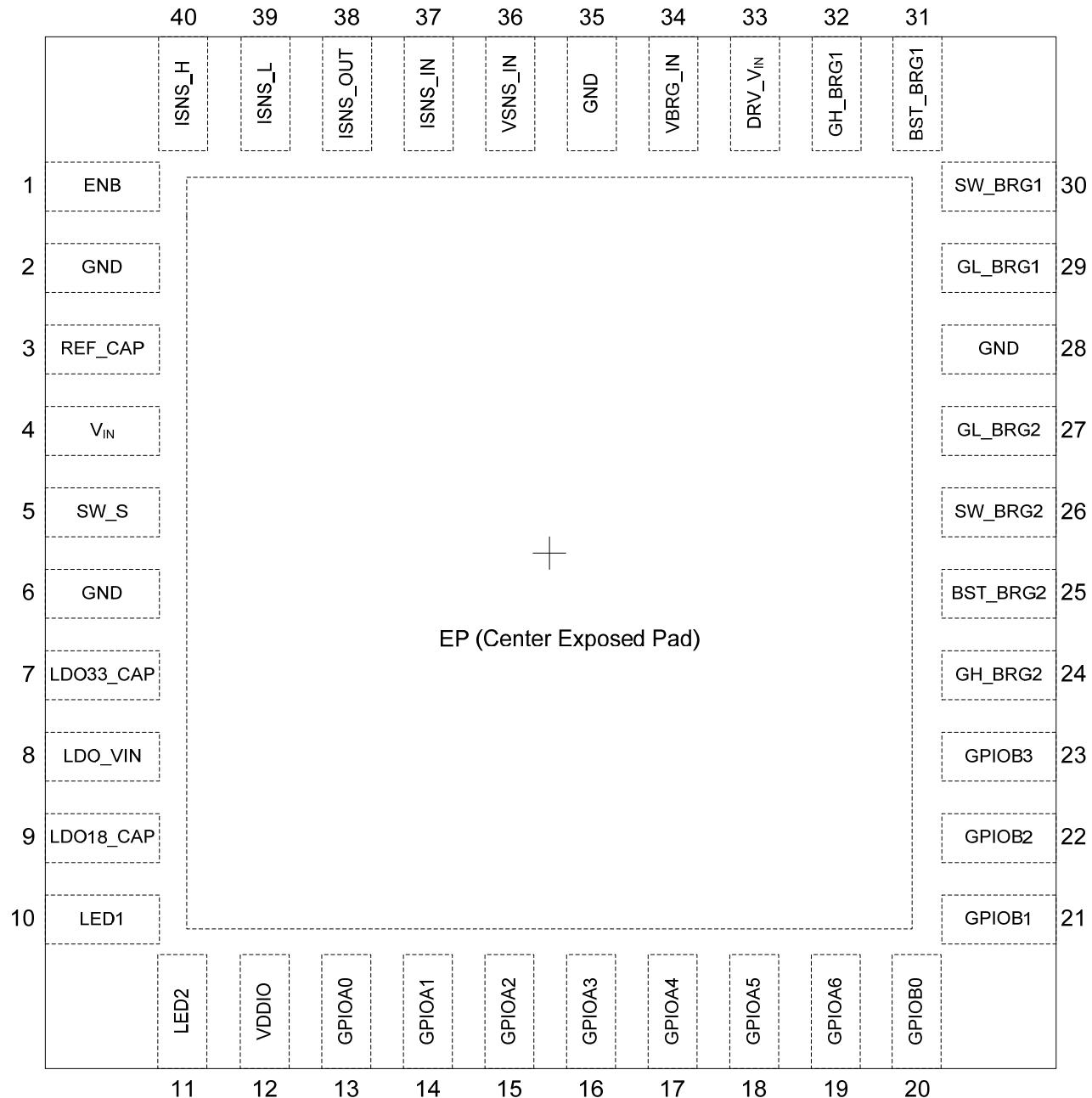


Figure 2. QFN-40 5mmx5mm (Top View)

Table 5. Pin Descriptions

PIN(s)	Name	Type	Function
1	ENB	I	Active low enable pin. When connected to logic high, the device shutdown and consumes less than 50 μ A of current. When connected to logic low, the device is in normal operation.
2, 6, 28, 35	GND	-	Ground connection.
3	REF_CAP	O	Regulated output voltage for the internal power management. Provides power for the entire power management block after the device has been shutdown (ENB= logic high). Connect a 1 μ F capacitor from this pin to ground. This pin should not be externally loaded.
4	V _{IN}	I	Input power supply. Connect a 10 μ F capacitor from this pin to ground.
5	SW_S	O	Step-down regulator switch node. Connect one of the terminals of the 4.7 μ H inductor to this pin.
7	LDO33_CAP	O	Regulated 3.3V output voltage used for internal device biasing. Connect a 1 μ F capacitor from this pin to ground. This pin should not be loaded. Other available output voltage options are: 3.6, 3.9 & 4.2V. Consult factory for different voltage setting.
8	LDO_VIN	I	Low Dropout input power supply. Connected this pin to the input supply voltage.
9	LDO18_CAP	I/O	Regulated 1.8V output voltage used for internal device biasing. Connect a 1 μ F capacitor from this pin to ground. This pin should not be externally loaded.
10, 11	LED1, LED2	I	Open drain output. Connect the LED's to these two pins.
12	VDDIO	I	Input power supply for both GPIO A and B. Can be connected to a power supply ranging from 1.8 – 5.0V.
13,14,15,16, 17,18,19	GPIOA [0:6]	I/O	Bank A general purpose input/output. The GPIO's power are supplied from VDDIO pin.
20, 21, 22, 23	GPIOB [0:3]	I/O	Bank B general purpose input/output. The GPIO's power are supplied from VDDIO pin.
24	GH_BRG2	O	Gate driver output for the high-side half bridge 2.
25	BST_BRG2	I	Bootstrap pin for half Bridge 2. Tie an external capacitor from this pin to the SW_BRG2 to generate drive voltage higher the input voltage.
26	SW_BRG2	O	Switch node for half bridge 2.
27	GL_BRG2	O	Gate driver output for the low-side half bridge 2.
29	GL_BRG1	O	Gate driver output for the low-side half bridge 1.
30	SW_BRG1	O	Switch node for half bridge 1.
31	BST_BRG1	O	Bootstrap pin for half Bridge 1. Tie an external capacitor from this pin to the SW_BRG1 to generate drive voltage higher the input voltage.
32	GH_BRG1	O	Gate driver output for the high-side half bridge 1.
33	DRV_VIN	I	Input power supply for the internal gate drivers. Connect a 10 μ F capacitor from this pin to ground.
34	VBRG_IN	I	Bridge Voltage input sense.
36	VSNS_IN	I	Voltage sense input.
37	ISNS_IN	I	Current sense input.
38	ISNS_OUT	O	Input Current Sense output
39	ISNS_L	I	Input Current Sense Negative Input
40	ISNS_H	I	Input Current Sense Positive Input
	EPD	-	Expose pad. Thermal pad for heatsinking purposes. Connect EPD to GND plane.

FUNCTIONAL BLOCK DIAGRAM

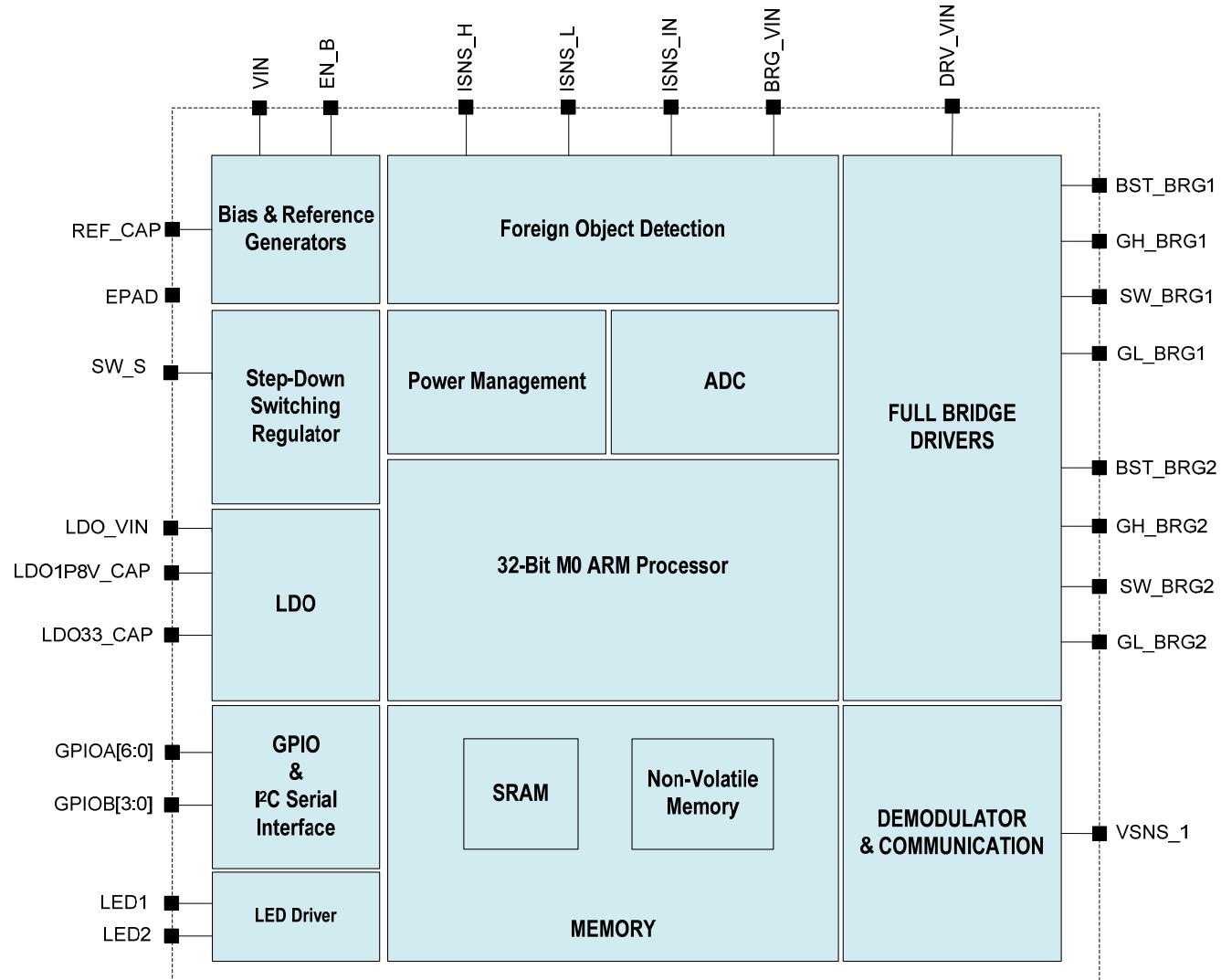


Figure 3. P9235A Block Diagram

Description of the Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. A WPC¹ transmitter may be a *free-positioning* or *magnetically-guided* type. A *free-positioning* type of transmitter has an array of coils that gives limited spatial freedom to the end-user, whereas a *magnetically-guided* type of transmitter helps the end-user align the receiver to the transmitter with a magnetic attraction.

The amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The communication is purely digital, and communication 1's and 0's ride on top of the power link that exists between the two coils.

A large part of the efficiency of the wireless charging system arises from the fact that when it's not actually charging a mobile device, the transmitter is in a very-low-power sleep mode. Until the transmitter detects the presence of a receiver, it remains in a low-power state.

Theory of Operation

The P9235A is a highly-integrated wireless power transmitter IC solution for mobile devices. It can transfer up to 5W of power in WPC mode, from a wireless transmitter to a load (e.g., a battery charger) using near-field magnetic induction.

OVERVIEW

The simplified block diagram of the P9235A is shown in Figure 3 and contains the following functions:

- Optimized and fully supports WPC transmitter specification.
- Supports WPC low power transmitter types with external MOSFET.
- Powerful 32 bit ARM® Cortex®-M0 processor, with SRAM for data memory and OTP for trimming and field updated-able program.
- Supports high speed serial flash (SPI interface) for system development, chip bring up and debug.
- Dithered PWM controller for high resolution voltage modulation.
- Multiple new and enhanced demodulation schemes using less external components for a robust communication
- Built-in I²C interface to communicate with external devices.
- Built-in PLL and clock synthesizer for PWM generation and back channel communication.
- Support variable logic I/O voltages with dedicated VDD_IO pin.
- Built-in general purpose 12 bit, 100 KSPS ADC for temperature, voltage, current measurement and processing.
- Two banks of GPIO's with dedicated power supply.

Note 1 - Refer to the WPC specification at <http://www.wirelesspowerconsortium.com/> for the most current information

DETAILED SYSTEM DIAGRAM

IDTP9235 A11 Single Coil 5V REFERENCE SCHEMATIC V1.1

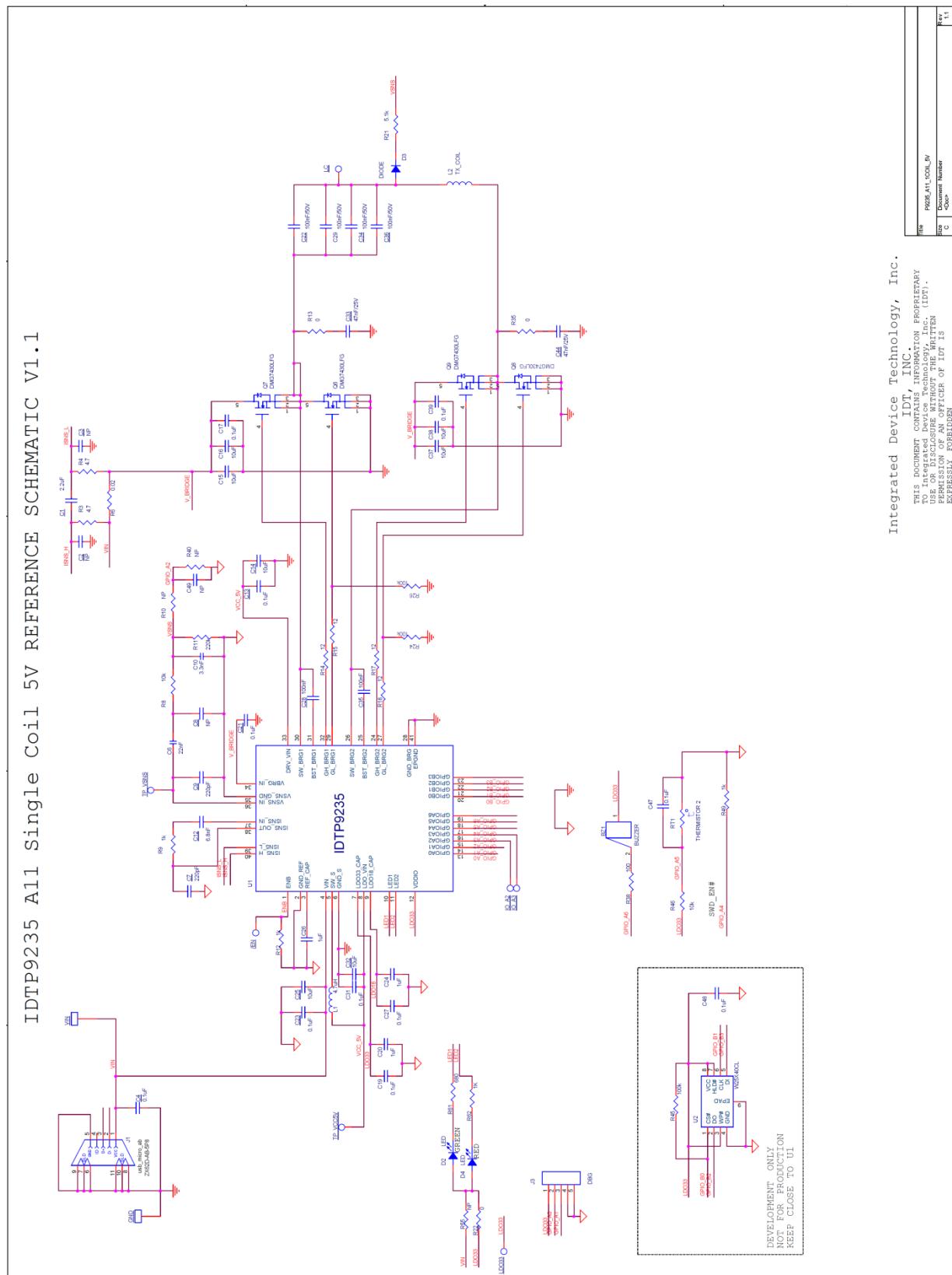


Figure 4. P9235A Preliminary WPC Reference Design Schematic

COMPONENTS SELECTION

Table 6. Component List

Item	Quantity	Reference	Part	PCBFootprint	PartNumber	Description
1	1	BZ1	BUZZER	buzz_ps1240	PS1240P02CT3 (Optional)	BUZZER PIEZO 4KHZ 12.2MM PC MNT
2	1	C1	2.2uF	402	C0402C225M8PACTU	CAP CER 2.2UF 10V 20% X5R 0402
3	2	C2,C3	NP	603		
4	6	C4,C17,C21,C23,C39,C47	0.1uF	402	TMK105BJ104KV-F	CAP CER 0.1UF 25V 10% X5R 0402
5	1	C6	22nF	603	C1608X7R1H223K	CAP CER 0.022UF 50V 10% X7R 0603
6	2	C7,C9	220pF	402	CL05B221KB5NNNC	CAP CER 220PF 50V 10% X7R 0402
7	2	C8, C49	NP	402		
8	1	C10	3.3nF	603	CL10B332KB8SFNC	CAP CER 3300PF 50V 10% X7R 0603
9	1	C12	6.8nF	402	GRM155R71E682KA01D	CAP CER 6800PF 25V 10% X7R 0402
10	4	C13,C19,C27,C31	0.1uF	402	LMK105BJ104KV-F	CAP CER 0.1UF 10V 10% X5R 0402
11	6	C14,C15,C16,C25,C37,C38	10uF	603	CL10A106MA8NRNC	CAP CER 10UF 25V 20% X5R 0603
12	3	C20,C24,C26	1uF	402	CL05A105MP5NNNC	CAP CER 1UF 10V 20% X5R 0402
13	4	C22,C29,C34,C36	100nF/50V	1206	C3216COG1H104J160AA	CAP CER 0.1UF 50V 5% COG 1206
14	2	C28,C35	100nF	402	C1005X6S1V104K050BB	CAP CER 0.1UF 35V 10% X6S 0402
15	1	C32	10uF	603	CL10X106MP8NRNC	CAP CER 10UF 10V 20% X6S 0603
16	2	C33,C44	47nF/25V	402	TMK105B7473KV-F	CAP CER 0.047UF 25V 10% X7R 0402
17	1	D2	LED	0603_diode	150 060 GS7 500 0	LED SMARTLED GREEN 570NM 0603
18	1	D3	DIODE	sod123	BAV21W-7-F	DIODE SWITCHING 200V 0.2A SOD123
19	1	D4	LED	0603_diode	150 060 RS7 500 0	LED SMARTLED GREEN 570NM 0603
20	1	L1	4.7uH	603	CIG10W4R7MNC	INDUCTOR MULTILAYER 4.7UH 1008
21	1	L2	TX_COIL	IND_A11_TX_COIL_SMD	760 308 111	TX WPC A11 Coil
22	4	Q6,Q7,Q8,Q9	DMG7430LFG	powerdi3333_8ld_fet	DMG7430LFG	MOSFET N CH 30V POWERDIA 3333-8
23	1	RT1	THERMISTOR 2	805		
24	2	R3,R4	4.7	402		RES 4.7 OHM 1/10W 5% 0402 SMD
25	1	R6	0.02	805	WSL0805R0200FEA	RES .02 OHM 1/8W 1% 0805 SMD
26	1	R8	10k	402	CRCW040210K0JNED	RES 10K OHM 1/16W 5% 0402 SMD
27	1	R9	1k	402	RC0402FR-071KL	RES 1K OHM 1/16W 5% 0402 SMD
28	3	R10,R40,R55	NP	402	TBD	
29	1	R11	220k	402	RC0402FR-07220KL	RES 220K OHM 1/16W 1% 0402 SMD
30	3	R12,R49,R62	1K	402	RC0402JR-071KL	RES 1K OHM 1/16W 5% 0402 SMD
31	3	R13,R22,R35	0	402	RC0402JR-070RL	RES 0.0 OHM 1/16W JUMP 0402 SMD
32	4	R14,R15,R17,R18	12	402	ERJ-2GEJ120X	RES 12 OHM 1/10W 5% 0402 SMD
33	1	R21	5.1k	402	MCR01MRTJ512	RES 5.1K OHM 1/16W 5% 0402 SMD
34	2	R24,R26	100k	402	ERJ-2GEJ104X	RES 100K OHM 1/10W 5% 0402 SMD
35	1	R38	100	603	ERJ-3GEYJ101V	RES 100 OHM 1/10W 5% 0603 SMD
36	1	R46	10k	402	MCR01MRTJ103	RES 10K OHM 1/16W 5% 0402 SMD
37	1	R61	680	402	RC0402JR-07680RL	RES 680 OHM 1/16W 5% 0402 SMD
38	1	U1	P9235A	qfn_40ld_5x5mm_3p75therm		A5/A11 Wireless Power Transmitter
Development/Optional BOM						
39	1	C48	0.1uF		402 LMK105BJ104KV-F	CAP CER 0.1UF 10V 10% X5R 0402
40	1	R45	100k		402 ERJ-2GEJ104X	RES 100K OHM 1/10W 5% 0402 SMD
41	1	U2	W25X40CL	uson_2x3_8LD	W25X40CLUXIG	IC FLASH 4MBIT 104MHZ 8WSON

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

The P9235A requires a minimum number of external components for proper operation, as indicated in Figure 4 and Table 6.

OTP, EXTERNAL FLASH, and SRAM

The P9235A uses OTP (256kbits) which is field programmable using GPIO_A0 (SCL) and GPIO_A1 (SDA) and follows I²C communications protocols. Once the device is powered the firmware settings that have been burned into the OTP are executed based on the hex file that has been programmed into memory. For development and applications that may require updates to operation a FLASH memory should be utilized. The Flash will allow multiple time programming. In order for the Flash to be loaded, GPIO_A4 pin must be pulled to GND at initial device power-up, otherwise the device will execute the contents of the OTP memory. The Flash firmware program is directly executed by the device when GPIO_A4 is pulled to GND at startup. The Flash IC should be connected to the P9235A as shown in Figure 4. SRAM is used by the device to temporarily store and retrieve data during device operation.

BUCK REGULATOR

The input capacitors (C_{VIN}) must be connected directly between the power pin (VIN) and power GND pin (GND_S) and placed as close as possible to the respective IC pins. The output capacitor (C_{VCC_5V}) must be placed close to the device and power ground pin (GND pin 6). The output voltage is sensed by the LDO_VIN pin; therefore, the connection from the BUCK output (VCC_5V) to the LDO_VIN pin should be made as wide and short as possible to minimize output voltage errors. The BUCK regulator operates in hysteretic pulse mode to set the output voltage and will regulate the VCC_5V node near 5.1V when VIN is greater than 5.5VDC. For operation with VIN less than 5.5V the BUCK output will decrease below 5.1V and when the VIN is less than 5.1V the regulator will switch to linear mode and operate similar to an LDO regulator. Since the BUCK regulator provides power for internal functions, such as the gate drivers along with the LDO18 & LDO33 circuits it is important to select an appropriately rated inductor for use to generate the regulated voltage with acceptable output ripple. For applications with the VIN > 10V it is not recommended to use an inductor less than 4.7 μ H and for applications with

VIN < 10V it is recommended to use an inductor that is between 3.3 and 4.7 μ H.

INDUCTOR SELECTION

To simplify the selection of inductors, the following approximations and equations should be used.

$$I_{PEAK_startup} = I_{PEAK} + \Delta I \text{ (A)}, \quad \text{Equation 1}$$

where, I_{PEAK} = peak current that flows through the BUCK inductor during device startup. The maximum peak current is limited internally and can be as high as 300mA.

The following equations can be used to determine the inductor minimum current ratings.

$$I_{Max} = I_{OUT} + \Delta I \text{ (A)}, \quad \text{Equation 2}$$

where, I_{MAX} = the peak current during operation

I_{OUT} = the average load current (sum of any external load on the BUCK output up to 50mA and the internal loading (~25mA maximum, 10mA typical)

ΔI = the positive inductor ripple current

$$\Delta I = \frac{(VIN - VCC_5V) \times t_{BLANK}}{L} \text{ (A)}, \quad \text{Equation 3}$$

where, L = Inductance (μ H)

t_{BLANK} = time the High-Side BUCK switch is on. The hysteresis mode is time controlled based on the VCC_5V voltage. Once the High-side BUCK switch is triggered (VCC_5V = 5.1V) the 80ns (t_{BLANK} , 100ns maximum) blanking timer starts. To eliminate consecutive blanking pulses a 100ns (120ns maximum) hysteretic timer is in place. The blanking timer and hysteresis timer are based on the same clock; therefore, they can never overlap.

The inductor rated current should be chosen to exceed the greater value of I_{MAX} or $I_{PEAK_startup}$ and the saturation current should be higher than I_{MAX} . The DCR should be kept to a minimum to improve the efficiency of the regulator.

OUTPUT CAPACITOR

The output capacitor should be assigned based on the typical reference schematic to avoid control loop stability errors and should not be less than 10 μ F. For applications

that require lower ripple voltage levels or have transient loads, additional capacitance may be added in order to meet voltage ripple requirements. Low ESR ceramic capacitors are recommended.

OVERVIEW OF GPIO USAGE

There are 2 banks of GPIOs on the P9235A transmitter IC. The GPIOs are controlled by OTP or by FLASH. Some of the GPIOs are semi-dedicated for specific operations as described below:

- GPIO_A0: This pin is used as SCL for I²C communication, can be connected to the ADC, or can be used as a digital I/O.
- GPIO_A1: This pin is used as SDA for I²C communication, can be connected to the ADC, or can be used as a digital I/O.
- GPIO_A4: This pin is used to instruct the P9235A to execute FLASH memory or OTP, can be connected to the ADC, or can be used as a digital I/O.
- GPIO_B0: This pin is used for CS function with Flash or as a digital I/O.
- GPIO_B1: This pin is used for SCK function with Flash or as a digital I/O.
- GPIO_B2: This pin is used for MISO function with Flash or as a digital I/O.
- GPIO_B3: This pin is used for MOSI function with Flash or as a digital I/O.
- GPIO_A0 – GPIO_A5: These pins may be configured to connect to the ADCs or as digital I/Os.
- All GPIO pins can be configured to be used as digital I/Os.

For additional usage or questions on capabilities, consult the factory.

LDOs

INPUT CAPACITOR

The input capacitors should be located as close as possible to the power pin, LDO_VIN and ground (GND). Ceramic capacitors are recommended for their lower ESR and small profile. The recommended external components are shown in Table 6.

OUTPUT CAPACITOR

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO (LDO18 and LDO33). The output capacitor connection to the ground pin (GND pin 6) should be made as short as practical for optimal device performance. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

WPC TX Coil

When used in the WPC TX-A5 or A11 full-bridge configuration, each half-bridge output connects to a series-resonance circuit made by a WPC Type-A5/A11 coil and series resonance capacitors. The inductor serves as the primary coil of a loosely-coupled transformer, the secondary of which is the inductor connected to the power receiver (IDTP9025A or another).

The TX power transmitter coils are mounted on a ferrite base acting as a shield to concentrate the field on the top side of the coil and to reduce EMI. The coil assembly can be mounted next to the P9235A. Either a ground plane or grounded metal shielding (preferably copper) can be added beneath the ferrite shield for added reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the ground plane by a single trace leading back independently to the board input power connector.

For other WPC TX-coil configurations consult the WPC specification for proper coil design and resonance capacitors selection and ratings. Consult with the factory for proper implementation and firmware questions.

ADC CONSIDERATIONS

GPIO_A0 through GPIO_A5 can be connected internally to successive-approximation ADCs via a multiplexed input. All GPIOs maintain the full 12 bit resolution.

The GPIO pins that are connected to the ADC have limited input range, so attention should be paid to the maximum full-scale input voltage (2.4V). Decoupling capacitors with a value of 0.1 μ F can be added to minimize noise.

APPLICATIONS INFORMATION (CONTINUED)

DECOUPLING/BULK CAPACITORS

As with any high-performance mixed-signal IC, the P9235A must be isolated from the system power supply noise to perform optimally. A decoupling capacitor of $0.1\mu\text{F}$ must be connected between each power supply pin and the PCB ground plane and placed as close as possible to these pins. For optimal device performance, the decoupling capacitor must be mounted on the component side of the PCB. Additionally, at least one $10\mu\text{F}$ capacitor should be placed at the VIN pin and two $10\mu\text{F}$ capacitors should be placed across each half-bridge used to convert DC to AC for power transfer to minimize ripple voltage and voltage droop due to the large current requirements. These $10\mu\text{F}$ capacitors must be connected as close as possible to the respective pins. The effective value of the capacitors will derate due to applied voltage. For example, a $10\mu\text{F}$ X5R 25V capacitor's value is actually $6\mu\text{F}$ when operating at 10V, depending on the manufacturer. The effective capacitance of each $10\mu\text{F}$ capacitor should be maintained above $6\mu\text{F}$ during operation for optimal performance.

PCB LAYOUT CONSIDERATIONS

- For optimal device performance and lowest output phase noise, the following guidelines should be observed. Please contact IDT Inc. for Gerber files that contain the recommended board layout and application note AN866, "P9235A Layout Guidelines".
- As with all switching power supplies, especially those providing high current, layout is an important design step. If layout is not carefully done, the regulator or inverter could show instability as well as cause EMI problems. Therefore, use wide and short traces for high current paths.
- An optimal layout is one with all components on the same side of the board, minimizing high power signals transitions to other layers. Other signal traces should be routed away from the P9235A Bridge Inverters. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs because the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat

away from the package. Appropriate PC layout techniques should be used to remove the heat due to device power dissipation.

- The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:

1. PC board traces with large cross-sectional areas remove more heat. For optimal results, use large-area PCB patterns with wide copper traces, placed on the component side of the PCB.
2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
3. Thermal vias are needed to provide a thermal path from the bridge FETs to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

POWER DISSIPATION AND THERMAL REQUIREMENTS

The P9235A is offered in a TQFN-40 package for which has a maximum power dissipation capability of about 1.4W, the maximum power dissipation of which is determined by the number of thermal vias between the package and the printed circuit board. The maximum power dissipation of either package is defined by the die's specified maximum operating junction temperature, $T_{J(MAX)}$ of 125°C . The junction temperature rises when the heat generated by the device's power dissipation flows through the package thermal resistance. The TQFN package offers a typical thermal resistance, junction to ambient (Θ_{JA}), of 28.5°C/W when the PCB layout guideline and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB layout section must be followed when designing the printed circuit board layout. Attention to the placement of the P9235A IC and bridge FET packages in proximity to other heat-generating devices in a given application design should also be considered. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing Θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size (TQFN) and thermal vias and final system hardware construction. Board designers should keep in mind that the package thermal metric Θ_{JA} is

impacted by the characteristics of the PCB itself upon which the IC is mounted. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

In summary, the three basic approaches for enhancing thermal performance are listed:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation should be calculated:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

In which

$P_{D(MAX)}$ = Maximum Power Dissipation

θ_{JA} = Package Thermal Resistance ($^{\circ}\text{C/W}$)

$T_{J(MAX)}$ = Maximum Device Junction Temperature ($^{\circ}\text{C}$)

T_A = Ambient Temperature ($^{\circ}\text{C}$)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9235A device is 125 $^{\circ}\text{C}$. The thermal resistance of the 40-pin TQFN package (NDG48) is optimally $\theta_{JA}=28.5\text{ }^{\circ}\text{C/W}$. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85 $^{\circ}\text{C}$. Therefore, the maximum recommended power dissipation is:

$$P_{D(MAX)} = (125\text{ }^{\circ}\text{C} - 85\text{ }^{\circ}\text{C}) / 28.5\text{ }^{\circ}\text{C/W} \cong 1.4 \text{ Watt.}$$

All the previously mentioned thermal resistances are the values found when the ICs are mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

Thermal Protection

The P9235A integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds the thermal shutdown specification. To allow the maximum load current on and to prevent thermal overload it is important to ensure that the heat generated by the P9235A solution is dissipated into the PCB. All the available pins must be soldered to the PCB. GND pins (especially the E-PAD) and bridge FETs should be soldered to the PCB ground plane to improve thermal performance with multiple vias connected to all layers of the PCB. For the TQFN package the exposed paddle (EP) must be soldered to the PCB, with multiple vias evenly distributed under the package and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

SPECIAL NOTES

NDG TQFN-40 PACKAGE ASSEMBLY

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly-opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125 $^{\circ}\text{C}$ within 24 hours prior to the assembly reflow process.

PACKAGE OUTLINE DRAWING

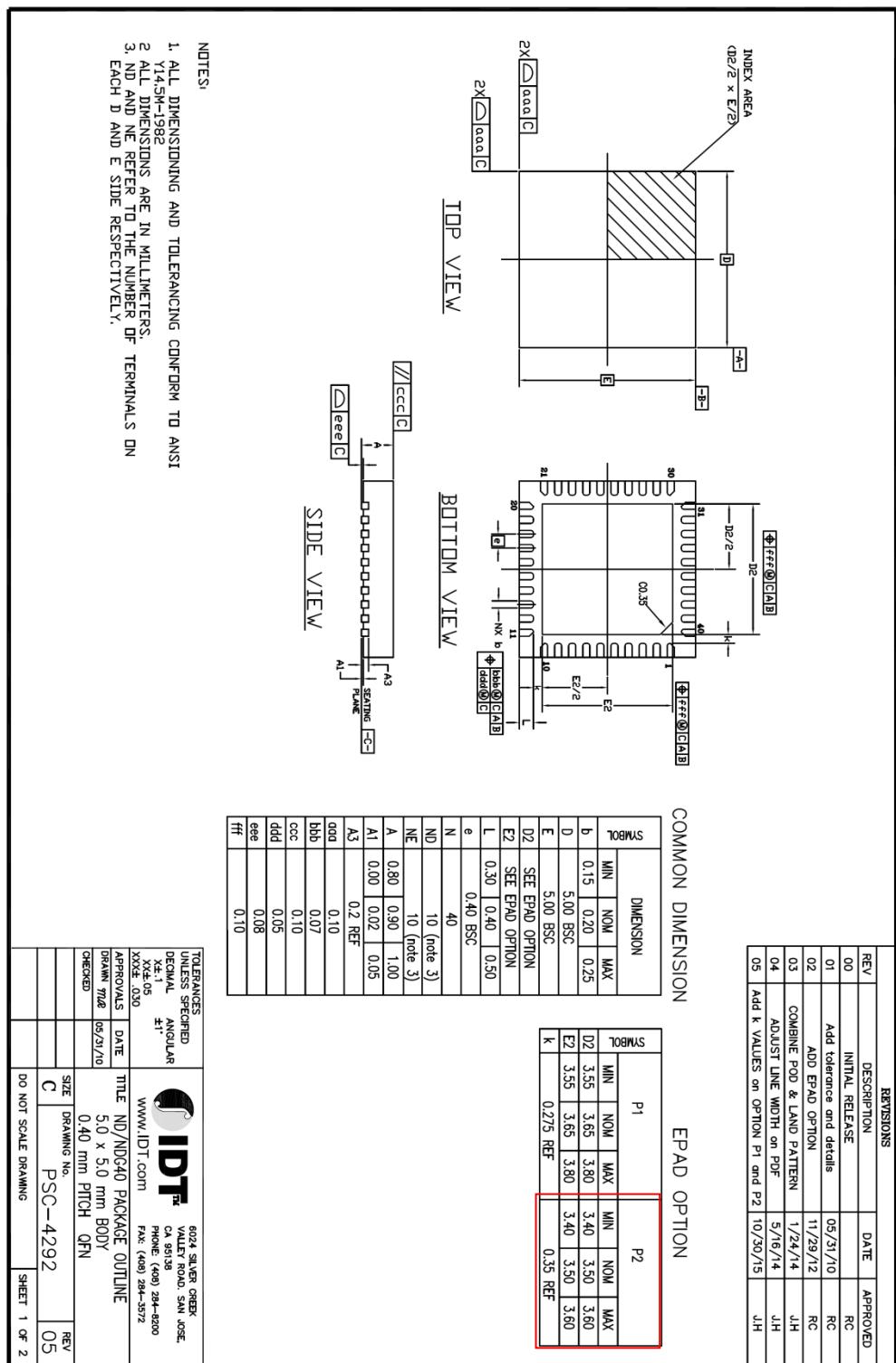


Figure 5. QFN-40 NDG40 5mmx5mm Package Outline Drawing (POD) . P9235A uses Option P2.

LANDING PATTERN DRAWING

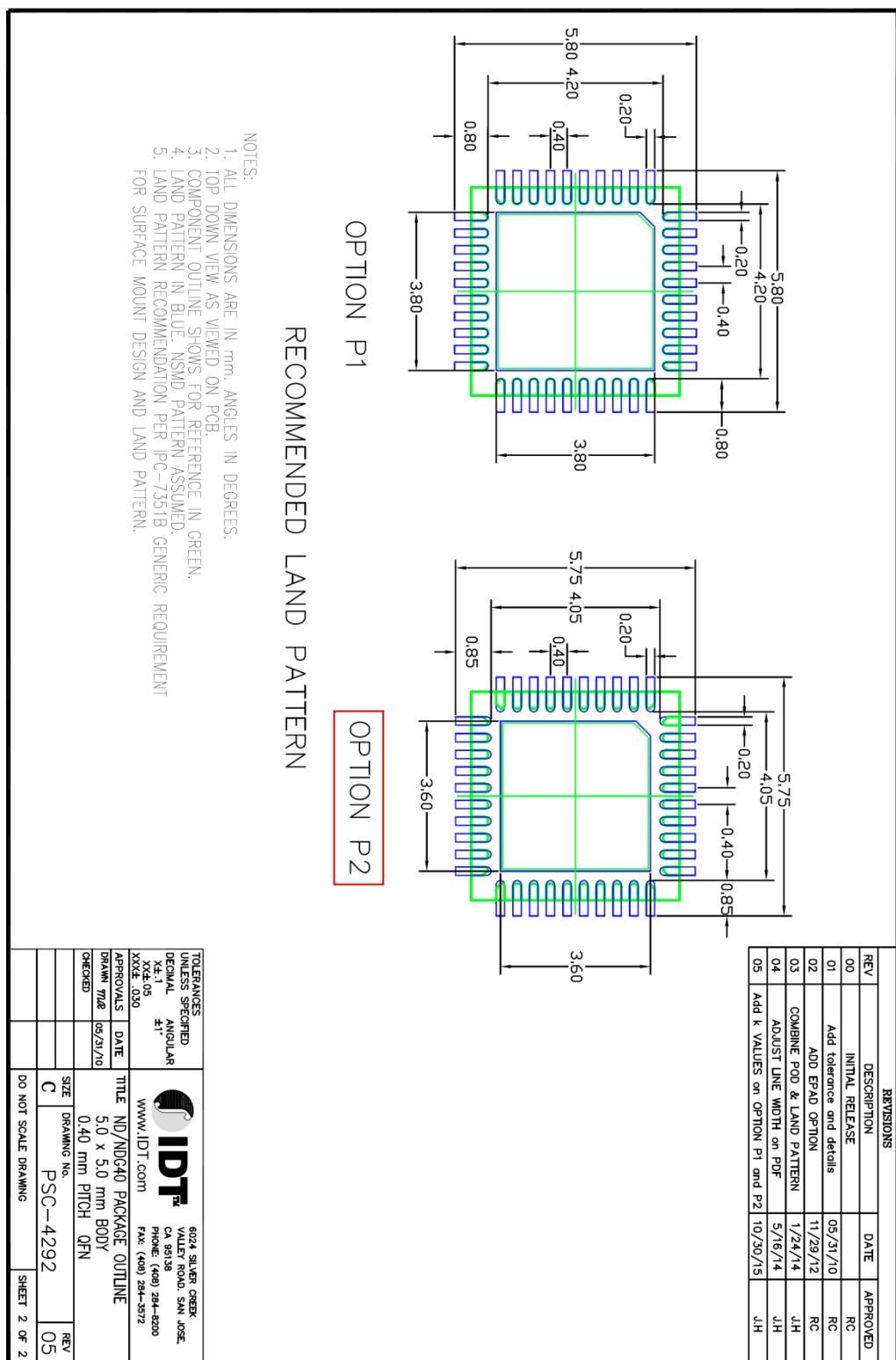


Figure 7: QFN-40 NDG40 Landing Pad Drawing

ORDERING GUIDE

Table 7. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER
P9235A-0*NDGI	P9235A-0*NDGI	NDG40 - QFN-40 5x5x0.40	-40°C to +85°C	Tray
P9235A-0*NDGI8	P9235A-0*NDGI	NDG40 - QFN-40 5x5x0.40	-40°C to +85°C	Tape and reel

*Note – this field is a custom value that is specific to each customer. Please contact your local sales team for your particular value for this field.

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