

**FEATURES:**

- Enhanced N channel FET with no inherent diode to Vcc
- Bidirectional signal flow
- 24:12 Mux/Demux switches connect inputs to outputs
- Individual controls for each bank
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control inputs
- TTL-compatible control inputs
- Available in 48-pin QVSOP package

**APPLICATIONS:**

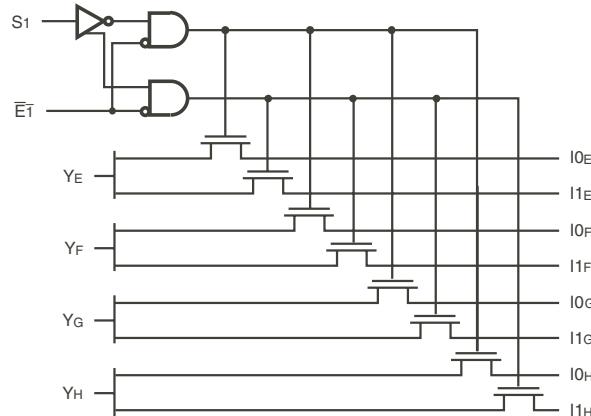
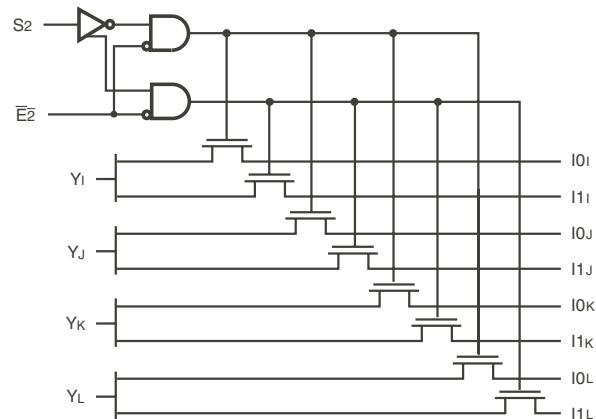
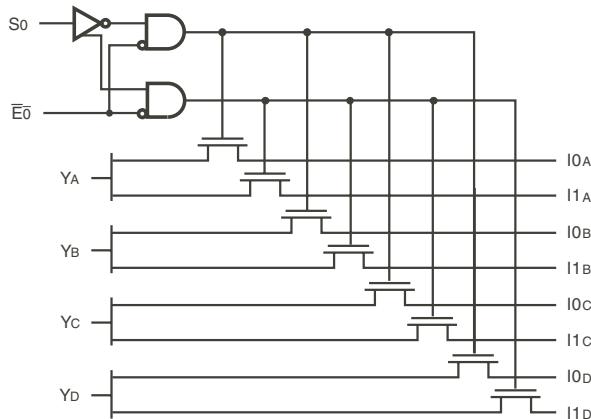
- Logic replacement
- Video, audio, graphics switching, muxing
- Hot-swapping, hot-docking
- Voltage translation (5V to 3.3V)
- Bus funneling

**DESCRIPTION:**

The QS33X257 is a high-speed CMOS TTL-compatible 24:12 multiplexer/demultiplexer. The QS33X257 is functionally compatible to three of the QuickSwitch version of the 74F257, 74FCT257, and the 74ALS/AS/LS257 Quad 2:1 multiplexers. The low ON resistance of the QS33X257 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. This part will be used in wide bus multiplexing where board space is at a premium.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

The QS33X257 is characterized for operation at -40°C to +85°C.

**FUNCTIONAL BLOCK DIAGRAM**

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

**INDUSTRIAL TEMPERATURE RANGE**

**AUGUST 2012**

## PIN CONFIGURATION

S0	1	48	VCC
I0A	2	47	$\bar{E}0$
I1A	3	46	I0D
YA	4	45	I1D
I0B	5	44	YD
I1B	6	43	I0C
YB	7	42	I1C
GND	8	41	YC
S1	9	40	VCC
I0E	10	39	$\bar{E}1$
I1E	11	38	I0H
YE	12	37	I1H
I0F	13	36	YH
I1F	14	35	I0G
YF	15	34	I1G
GND	16	33	YG
S2	17	32	VCC
I0I	18	31	$\bar{E}2$
I1I	19	30	I0L
YI	20	29	I1L
I0J	21	28	YL
I1J	22	27	I0K
YJ	23	26	I1K
GND	24	25	YK

QVSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Supply Voltage to Ground	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Switch Voltage Vs	-0.5 to +7	V
VTERM <sup>(3)</sup>	DC Input Voltage Vin	-0.5 to +7	V
VAC	AC Input Voltage (pulse width $\leq$ 20ns)	-3	V
IOUT	DC Output Current Max. Sink Current/Pin	120	mA
PMAX	Maximum Power Dissipation	0.5	W
TSTG	Storage Temperature	-65 to +150	°C

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Vcc terminals.

3. All terminals except Vcc.

## CAPACITANCE

(TA = +25°C, f = 1.0MHz, Vin = 0V, Vout = 0V)

Pins		Typ.	Max. <sup>(1)</sup>	Unit
Control Pins		4	5	pF
Quickswitch Channels (Switch OFF)	Demux	5	7	pF
	Mux	9	10	

NOTE:

1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I/O	Data Inputs
Sx	I	Select Input
$\bar{E}x$	I/O	Enable Input
Yx	I/O	Data Outputs

## FUNCTION TABLE<sup>(1)</sup>

$\bar{E}x$	Sx	Outputs				Function
		YA	YB	Yc	YD	
H	X	Z	Z	Z	Z	Disable
L	L	I0A	I0B	I0C	I0X	Select 0
L	H	I1A	I1B	I1C	I1X	Select 1

NOTE:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

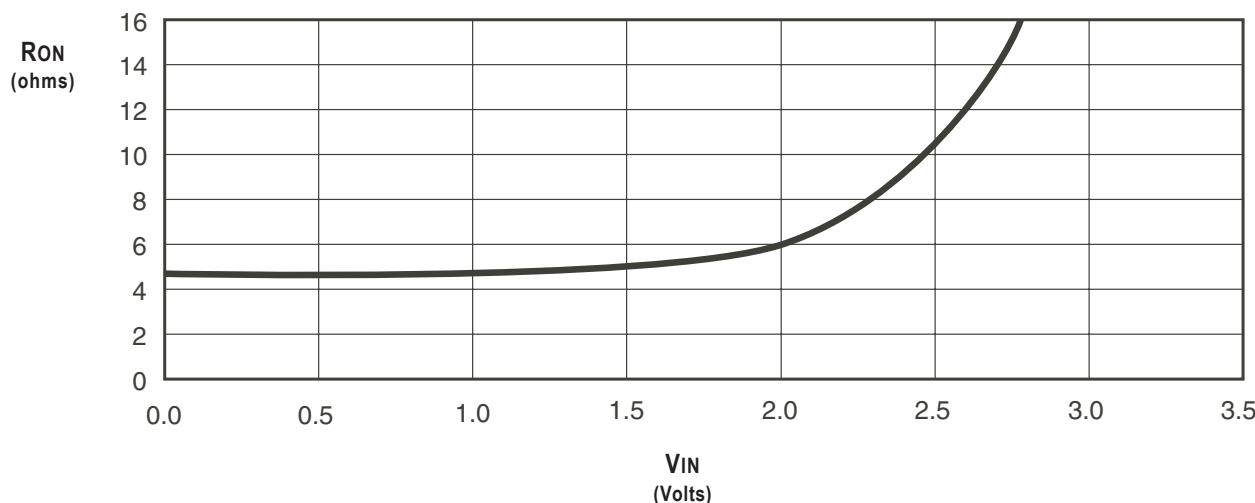
Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH for Control Pins	2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$I_{IN}$	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	Off-State Output Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
$R_{ON}$	Switch ON Resistance	$V_{CC} = \text{Min.}$ , $V_{IN} = 0\text{V}$ , $I_{ON} = 30\text{mA}$	—	5	7	$\Omega$
		$V_{CC} = \text{Min.}$ , $V_{IN} = 2.4\text{V}$ , $I_{ON} = 15\text{mA}$	—	10	15	
$V_P$	Pass Voltage <sup>(2)</sup>	$V_{IN} = V_{CC} = 5\text{V}$ , $I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

NOTES:

1. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
2. Pass Voltage is guaranteed but not production tested.

## TYPICAL ON RESISTANCE vs $V_{IN}$ AT $V_{CC} = 5\text{V}$



## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max.	Unit
I <sub>CCQ</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub> , f = 0	9	µA
ΔI <sub>CC</sub>	Power Supply Current per Control Input HIGH <sup>(2)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f = 0	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current per MHz <sup>(3)</sup>	V <sub>CC</sub> = Max., I and Y pins open Control Inputs Toggling at 50% Duty Cycle	0.25	mA/MHz

### NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per TLL driven input (V<sub>IN</sub> = 3.4V, control inputs only). I and Y pins do not contribute to ΔI<sub>CC</sub>.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed but not production tested.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 5%;

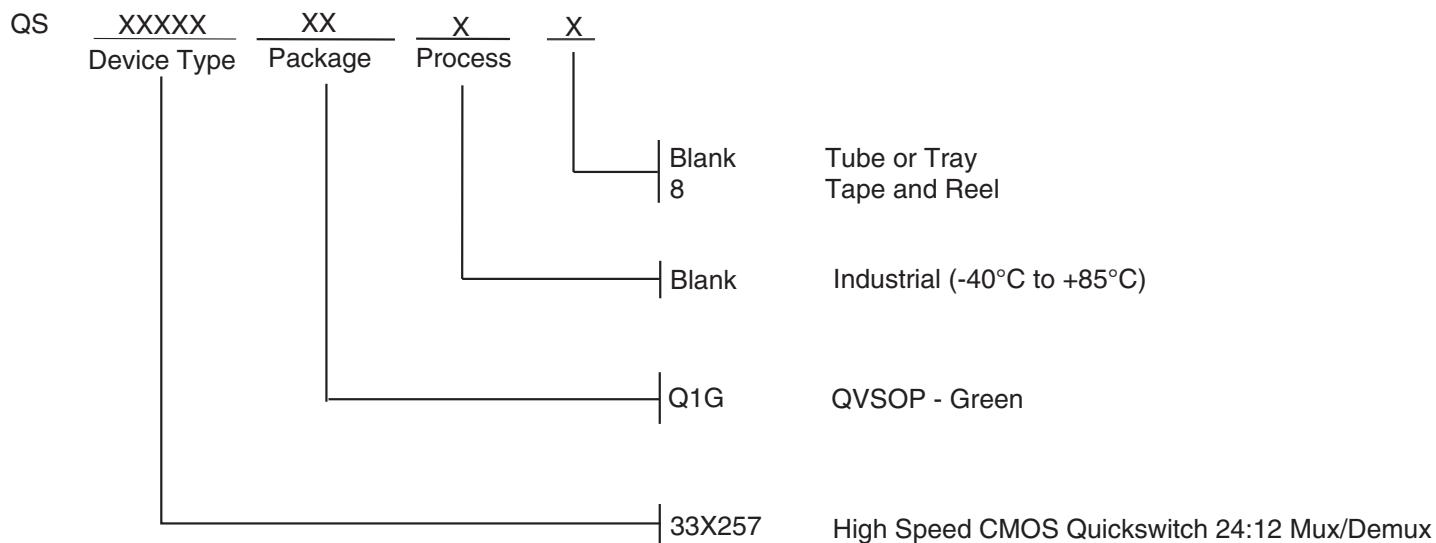
C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Parameter	Min. <sup>(1)</sup>	Typ.	Max.	Unit
t <sub>PLH</sub>	Data Propagation Delay <sup>(2,3)</sup> Ix to Y	—	0.25	—	ns
t <sub>PHL</sub>	Switch Turn-on Delay Sx to Y	0.5	—	5.2	ns
t <sub>PZL</sub>	Switch Turn-off Delay Ex to Y	0.5	—	4.8	ns
t <sub>PZH</sub>	Switch Turn-off Delay <sup>(2)</sup> Ex to Y, Sx to Y	0.5	—	5	ns

### NOTES:

1. Minimums are guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for C<sub>L</sub> = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## **ORDERING INFORMATION**



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).