

FEATURES:

- N channel FET switches with no parasitic diode to Vcc
 - Isolation under power-off conditions
 - No DC path to Vcc or GND
 - 5V tolerant in OFF and ON state
- 5V tolerant I/Os
- Flat Ron characteristics over operating range
- Rail-to-rail switching 0 - 5V
- Bidirectional dataflow with near-zero delay: no added ground bounce
- Excellent Ron matching between channels
- Vcc operation: 2.3V to 3.6V
- High bandwidth
- LVTTI-compatible control Inputs
- Undershoot Clamp Diodes on all switch and control Inputs
- Low I/O capacitance, 4pF typical
- 25Ω resistors for low noise and line matching
- Available in 80-pin QVSOP package

APPLICATIONS:

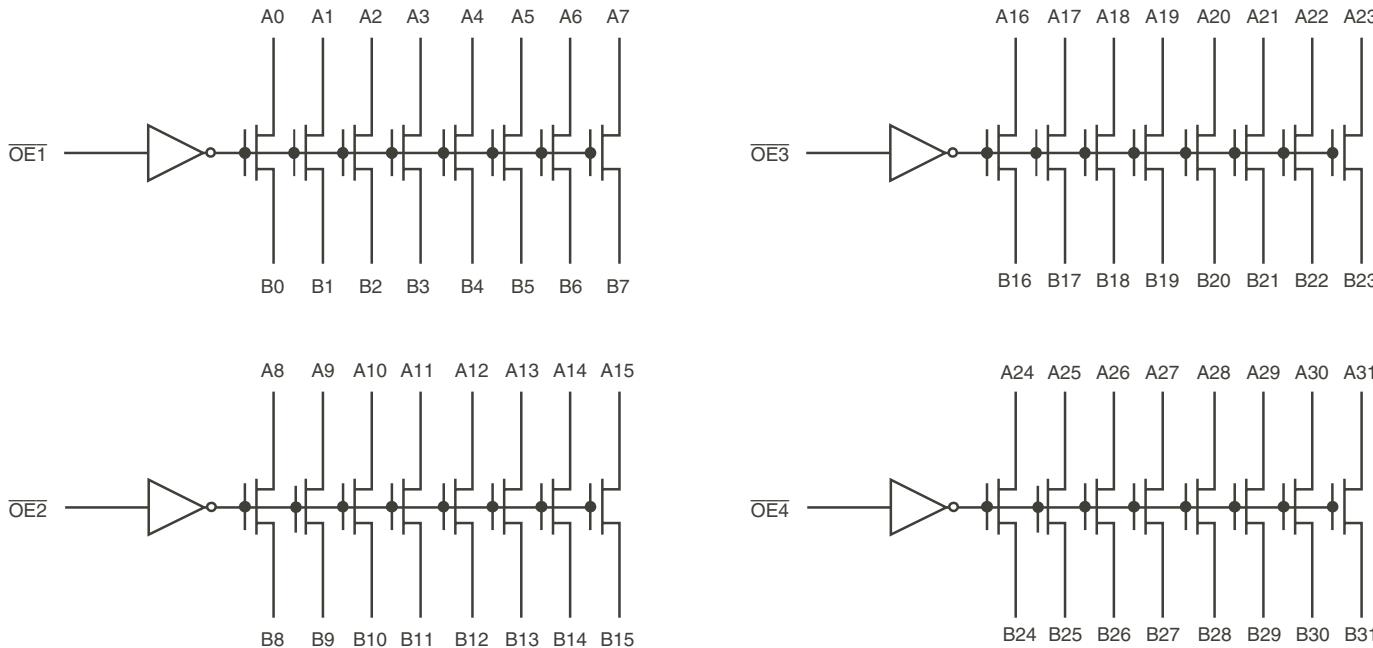
- Hot-swapping
- Low distortion analog switch
- Replaces mechanical relay
- ATM 25/155 switching

DESCRIPTION:

The QS34XVH2245 is a high bandwidth, 32-bit bus switch. The QS34XVH2245 with 25Ω resistance and 1.35ns propagation delay is ideal for line matching and low noise environments. The switches can be turned ON under the control of individual LVTTI-compatible Output Enable (OE_x) signals for bidirectional data flow with no added delay or ground bounce. In the ON state, the switches can pass signals up to 5V. In the OFF state, the switches offer very high impedance at the terminals.

The combination of small propagation delay, high OFF impedance, and over-voltage tolerance makes the QS34XVH2245 ideal for high performance communications applications.

The QS34XVH2245 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

JANUARY 2013

PIN CONFIGURATION

NC	1	80	Vcc
A0	2	79	\overline{OE}_1
A1	3	78	B0
A2	4	77	B1
A3	5	76	B2
A4	6	75	B3
A5	7	74	B4
A6	8	73	B5
A7	9	72	B6
GND	10	71	B7
NC	11	70	Vcc
A8	12	69	\overline{OE}_2
A9	13	68	B8
A10	14	67	B9
A11	15	66	B10
A12	16	65	B11
A13	17	64	B12
A14	18	63	B13
A15	19	62	B14
GND	20	61	B15
NC	21	60	Vcc
A16	22	59	\overline{OE}_3
A17	23	58	B16
A18	24	57	B17
A19	25	56	B18
A20	26	55	B19
A21	27	54	B20
A22	28	53	B21
A23	29	52	B22
GND	30	51	B23
NC	31	50	Vcc
A24	32	49	\overline{OE}_4
A25	33	48	B24
A26	34	47	B25
A27	35	46	B26
A28	36	45	B27
A29	37	44	B28
A30	38	43	B29
A31	39	42	B30
GND	40	41	B31

QVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Supply Voltage to Ground	-0.5 to +4.6	V
VTERM ⁽³⁾	DC Switch Voltage Vs	-0.5 to +5.5	V
VTERM ⁽³⁾	DC Input Voltage V _{IN}	-0.5 to +5.5	V
VAC	AC Input Voltage (pulse width \leq 20ns)	-3	V
I _{OUT}	DC Output Current (max. sink current/pin)	120	mA
T _{TG}	Storage Temperature	-65 to +150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc .

CAPACITANCE (TA = +25°C, F = 1MHz, V_{IN} = 0V, V_{OUT} =

Symbol	Parameter ⁽¹⁾	Typ.	Max.	Unit
C _{IN}	Control Inputs	3	5	pF
C _{I/O}	Quickswitch Channels (Switch OFF)	4	6	pF
C _{I/O}	Quickswitch Channels (Switch ON)	8	12	pF

NOTE:

1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
\overline{OE}_x	I	Output Enable
A _x	I/O	Bus A
B _x	I/O	Bus B

FUNCTION TABLE⁽¹⁾

\overline{OE}_x	Function
H	Disconnected
L	Connect (A _x = B _x)

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

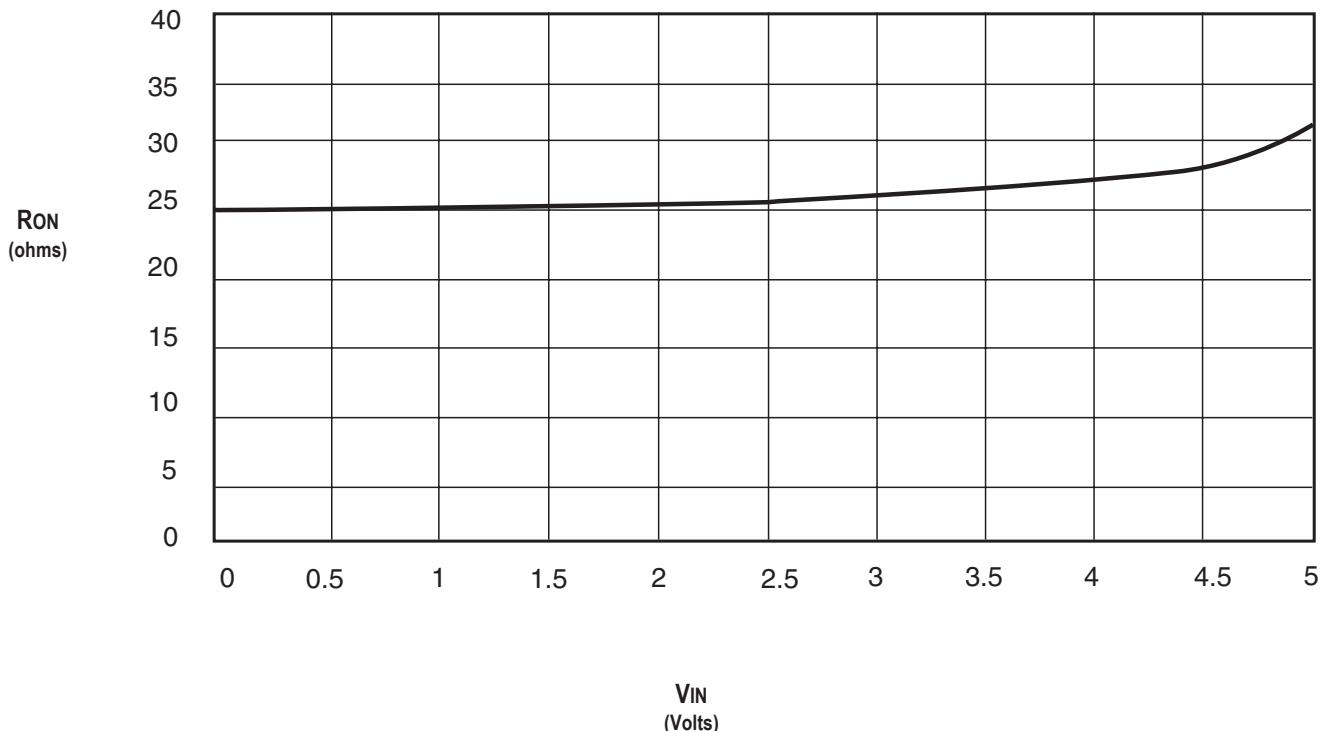
Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions			Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
			$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
			$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IN}	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$			—	—	± 1	μA
I_{OZ}	Off-State Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq 5\text{V}$, Switches OFF			—	—	± 1	μA
I_{OFF}	Data Input/Output Power Off Leakage	V_{IN} or V_{OUT} 0V to 5V , $V_{CC} = 0\text{V}$			—	—	± 1	μA
R_{ON}	Switch ON Resistance	$V_{CC} = 2.3\text{V}$ Typical at $V_{CC} = 2.5\text{V}$	$V_{IN} = 0\text{V}$	$I_{ON} = 30\text{mA}$	18	27	39	Ω
			$V_{IN} = 1.7\text{V}$	$I_{ON} = 15\text{mA}$	18	28	41	
		$V_{CC} = 3\text{V}$	$V_{IN} = 0\text{V}$	$I_{ON} = 30\text{mA}$	18	25	38	
			$V_{IN} = 2.4\text{V}$	$I_{ON} = 15\text{mA}$	18	26	40	

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$ and $T_A = 25^\circ\text{C}$.

TYPICAL ON RESISTANCE vs V_{IN} AT $V_{CC} = 3.3\text{V}$



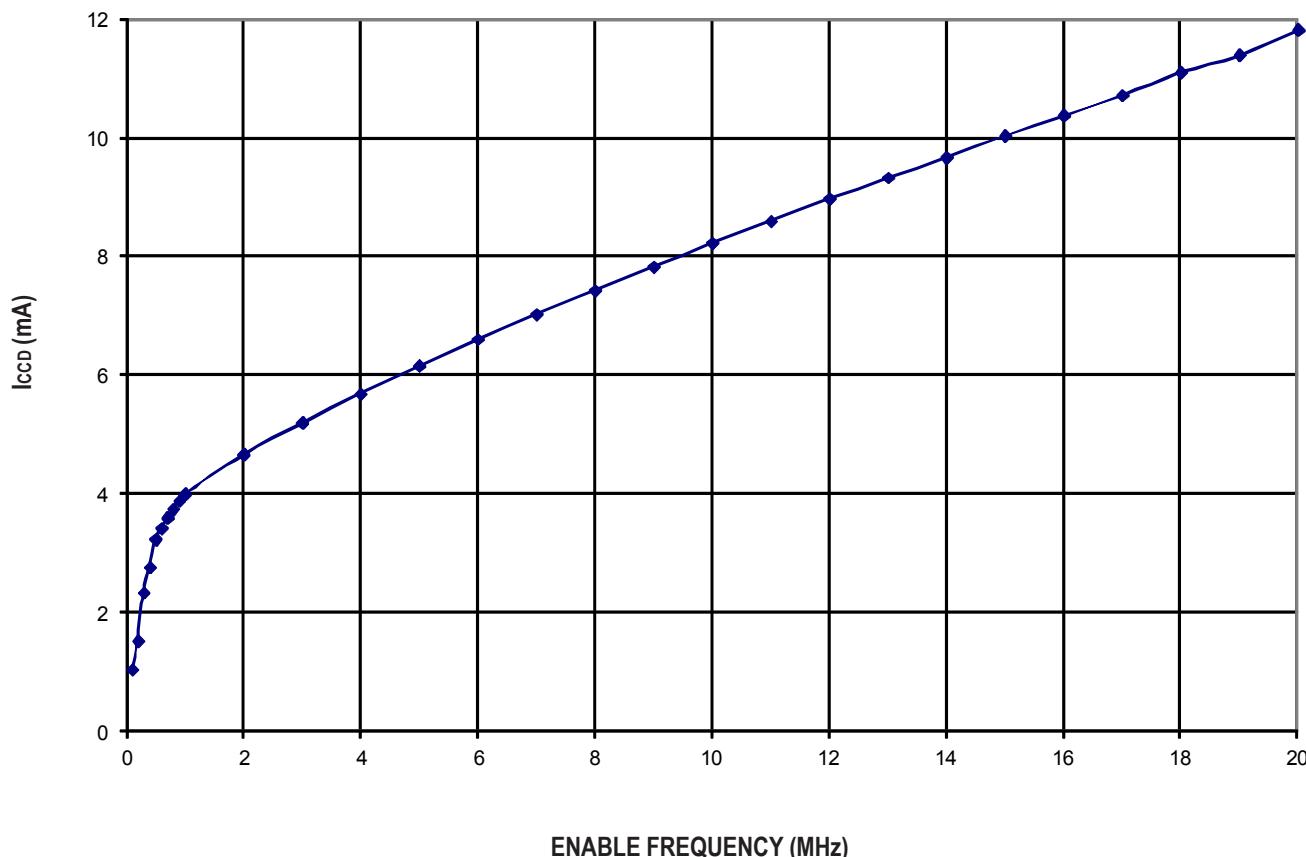
POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Unit
I _{CCQ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0	—	8	16	mA
ΔI _{CC}	Power Supply Current ^(2,3) per Input HIGH	V _{CC} = Max., V _{IN} = 3V, f = 0 per Control Input	—	—	30	μA
I _{CCD}	Dynamic Power Supply Current per Output Enable Control Input ⁽⁴⁾	V _{CC} = 3.3V, A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	See Typical I _{CCD} vs Enable Frequency graph below			

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per input driven at the specified level. A and B pins do not contribute to ΔI_{CC}.
3. This parameter is guaranteed but not tested.
4. This parameter represents the current required to switch internal capacitance at the specified frequency. The A and B inputs do not contribute to the Dynamic Power Supply Current. This parameter is guaranteed but not production tested.

TYPICAL I_{CCD} VS ENABLE FREQUENCY CURVE AT V_{CC} = 3.3V



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

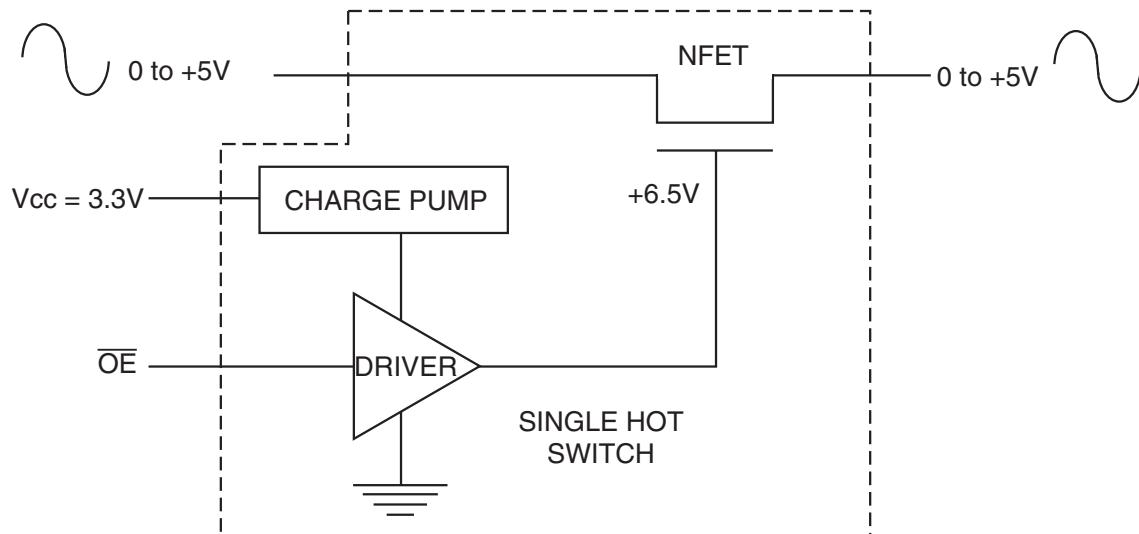
TA = -40°C to +85°C

Symbol	Parameter	Vcc = 2.5 ± 0.2V ⁽¹⁾		Vcc = 3.3 ± 0.3V ⁽¹⁾		Unit
		Min. ⁽⁴⁾	Max.	Min. ⁽⁴⁾	Max.	
tPLH tPHL	Data Propagation Delay ^(2,3) Ax to/from Bx	—	0.9	—	1.35	ns
tpZL tpZH	Switch Turn-On Delay OE _X to Ax/Bx	1.5	9	1.5	8	ns
tPLZ tPHZ	Switch Turn-Off Delay OE _X to Ax/Bx	1.5	7.5	1.5	7.5	ns
f _{OEx}	Operating Frequency - Enable ^(2,5)	—	10	—	20	MHz

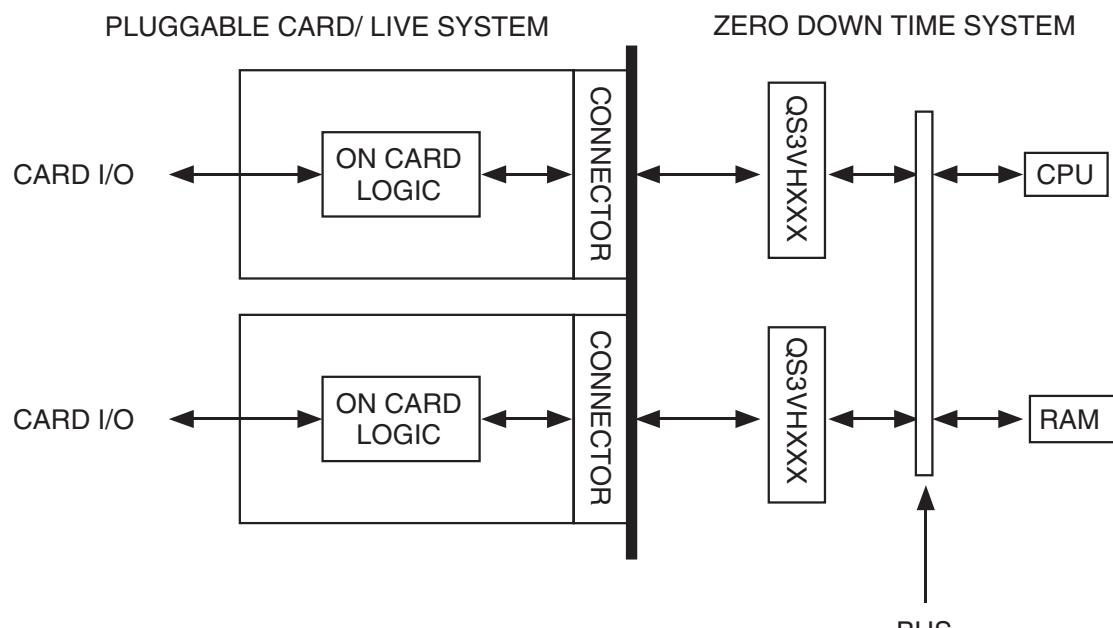
NOTES:

1. See Test Conditions under TEST CIRCUITS AND WAVEFORMS.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 1.35ns at C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Minimums are guaranteed but not production tested.
5. Maximum toggle frequency for OE_X control input (pass voltage > V_{cc}, V_{IN} = 5V, R_{LOAD} ≥ 1MΩ, no C_{LOAD}).

SOME APPLICATIONS FOR HOTSWITCH PRODUCTS



Rail-to-Rail Switching

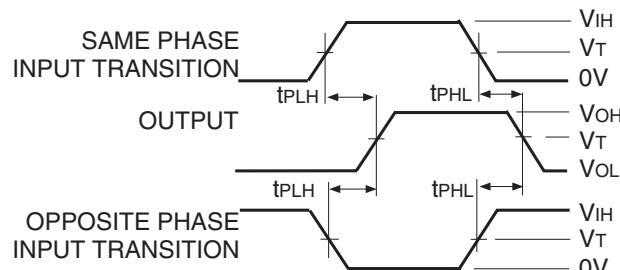


Hot-Swapping

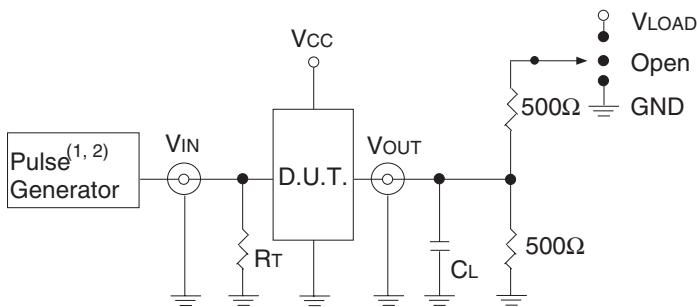
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	$2 \times V_{CC}$	V
V_{IH}	3	V_{CC}	V
V_T	1.5	$V_{CC}/2$	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



Propagation Delay



Test Circuits for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

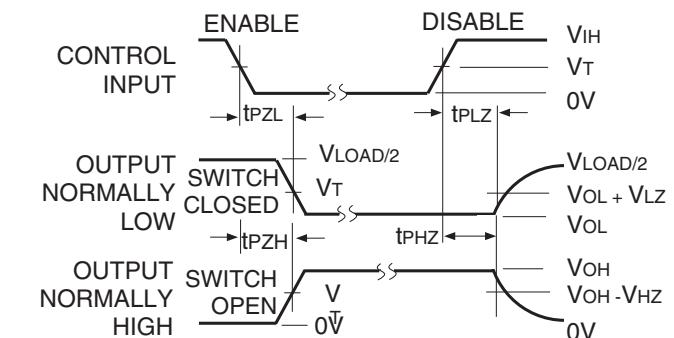
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_f \leq 2.5ns$; $t_r \leq 2.5ns$.
2. Pulse Generator for All Pulses: Rate $\leq 10MHz$; $t_f \leq 2ns$; $t_r \leq 2ns$.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open



NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

ORDERING INFORMATION

QS	<u>XXXXX</u>	<u>XX</u>	<u>X</u>		
	Device Type	Package			
				Blank	Tube or Tray
				8	Tape and Reel
				Q3G	80-Pin QVSOP - Green
				34XVH2245	2.5V / 3.3V 32-Bit High Bandwidth Bus Switch

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.