

R1RW0408DI Series

Wide Temperature Range Version 4M High Speed SRAM (512-kword × 8-bit) R10DS0287EJ0100 Rev.1.00 Nov.18.19

Description

The R1RW0408DI is a 4-Mbit high speed static RAM organized 512-kword \times 8-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The R1RW0408DI is packaged in 400-mil 36-pin SOJ for high density surface mounting.

Features

Single 3.3V supply: 3.3V ± 0.3V

Access time: 12ns (max)Completely static memory

No clock or timing strobe required

· Equal access and cycle times

• Directly TTL compatible

— All inputs and outputs

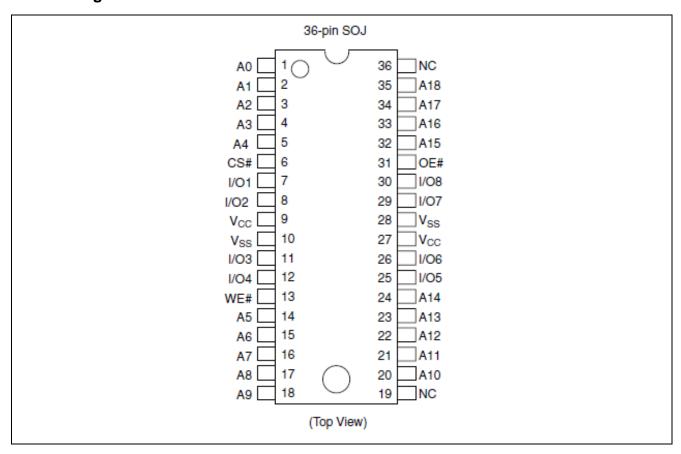
Operating current: 100mA (max)
TTL standby current: 40mA (max)
CMOS standby current: 5mA (max)

• Temperature range: -40 to +85°C

Ordering Information

Type No.	Access time	Package
R1RW0408DGE-2PI	12ns	400-mil 36-pin plastic SOJ

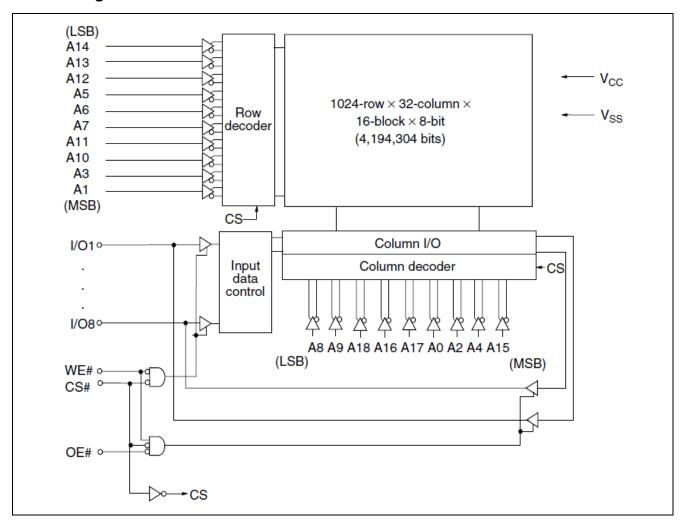
Pin Arrangement



Pin Description

Pin name	Function			
A0 to A18	Address input			
I/O1 to I/O8	Data input/output			
CS#	Chip select			
OE#	Output enable			
WE#	Write enable			
Vcc	Power supply			
Vss	Ground			
NC	No connection			

Block Diagram



Operation Table

CS#	OE#	WE#	Mode	Vcc current	I/O	Ref. cycle
Н	×	×	Standby	I _{SB} , I _{SB1}	High-Z	_
L	Н	Н	Output disable	Icc	High-Z	_
L	L	Н	Read	Icc	D _{OUT}	Read cycle (1) to (3)
L	Н	L	Write	Icc	D _{IN}	Write cycle (1)
L	L	L	Write	Icc	D _{IN}	Write cycle (2)

Note: H: VIH, L: VIL, X: VIH or VIL

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to Vss	Vcc	−0.5 to +4.6	V
Voltage on any pin relative to V _{SS}	V _T	-0.5^{*1} to V _{CC} + 0.5^{*2}	V
Power dissipation	P _T	1.0	W
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	-40 to +85	°C

Notes: 1. V_T (min) = -2.0V for pulse width (under shoot) \leq 6ns.

2. V_T (max) = V_{CC} + 2.0V for pulse width (over shoot) \leq 6ns.

Recommended DC Operating Conditions

 $(Ta = -40 \text{ to } +85^{\circ}C)$

Parameter	Symbol	Min	Тур	Max	Unit
Supply voltage	Vcc*3	3.0	3.3	3.6	V
	Vss*4	0	0	0	V
Input voltage	ViH	2.0	_	Vcc + 0.5*2	V
	VIL	-0.5* ¹		0.8	V

Notes: 1. V_{IL} (min) = -2.0V for pulse width (under shoot) \leq 6ns.

- 2. V_{IH} (max) = V_{CC} + 2.0V for pulse width (over shoot) \leq 6ns.
- 3. The supply voltage with all V_{CC} pins must be on the same level.
- 4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

(Ta = -40 to +85°C, Vcc = 3.3V \pm 0.3V, Vss = 0V)

Parameter	Symbol	Min	Max	Unit	Test conditions
Input leakage current	I _{LI}	_	2	μΑ	$V_{IN} = V_{SS}$ to V_{CC}
Output leakage current	I _{LO}	_	2	μΑ	$V_{IN} = V_{SS}$ to V_{CC}
Operating power supply current	Icc	_	100	mA	Min cycle $CS\# = V_{IL}, I_{OUT} = 0mA$ Other inputs = V_{IH}/V_{IL}
Standby power supply current	I _{SB}	_	40	mA	Min cycle, CS# = V _{IH} , Other inputs = V _{IH} /V _{IL}
	I _{SB1}	_	5	mA	$ f = 0MHz \\ V_{CC} \ge CS\# \ge V_{CC} - 0.2V, \\ (1) \ 0V \le V_{IN} \le 0.2V \ or \\ (2) \ V_{CC} \ge V_{IN} \ge V_{CC} - 0.2V $
Output voltage	Vol	_	0.4	V	I _{OL} = 8mA
	Vон	2.4	_	V	I _{OH} = -4mA

Capacitance

 $(Ta = +25^{\circ}C, f = 1.0MHz)$

Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance*1	C _{IN}	_	6	pF	$V_{IN} = 0V$
Input/output capacitance*1	C _{I/O}	_	8	pF	$V_{I/O} = 0V$

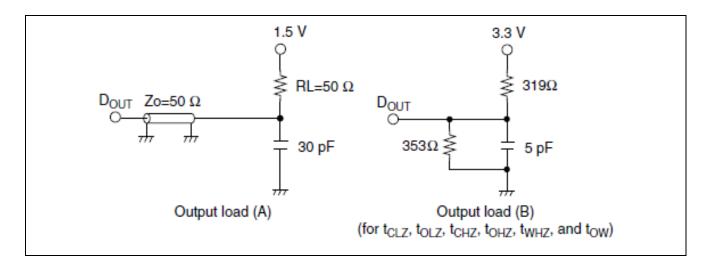
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Ta = -40 to +85°C, $V_{CC} = 3.3V \pm 0.3V$, unless otherwise noted.)

Input pulse levels: 3.0V/0.0VInput rise and fall time: 3ns

Input and output timing reference levels: 1.5VOutput load: See figures (Including scope and jig)



Read Cycle

		R1RW	0408DI		
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	12	_	ns	
Address access time	t _{AA}	_	12	ns	
Chip select access time	t _{ACS}	_	12	ns	
Output enable to output valid	t _{OE}	_	6	ns	
Output hold from address change	t _{OH}	3	_	ns	
Chip select to output in low-Z	tclz	3	_	ns	1
Output enable to output in low-Z	tolz	0	_	ns	1
Chip deselect to output in high-Z	tcHZ		6	ns	1
Output disable to output in high-Z	tонz	_	6	ns	1

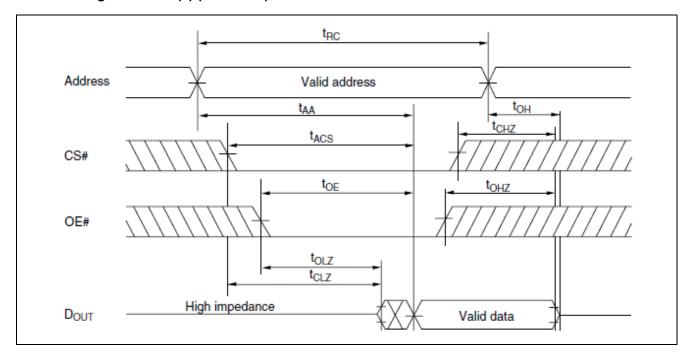
Write Cycle

	R1RW0408DI				
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	12	_	ns	
Address valid to end of write	t _{AW}	8	_	ns	
Chip select to end of write	tcw	8	_	ns	9
Write pulse width	twp	8	_	ns	8
Address setup time	tas	0	_	ns	6
Write recovery time	twR	0	_	ns	7
Data to write time overlap	t _{DW}	6	_	ns	
Data hold from write time	tрн	0	_	ns	
Write disable to output in low-Z	tow	3	_	ns	1
Output disable to output in high-Z	tонz	_	6	ns	1
Write enable to output in high-Z	t _{WHZ}	_	6	ns	1

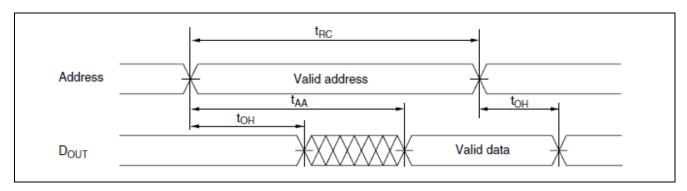
- Notes: 1. Transition is measured $\pm 200 \text{mV}$ from steady voltage with output load (B). This parameter is sampled and not 100% tested.
 - 2. Address should be valid prior to or coincident with CS# transition low.
 - 3. WE# and/or CS# must be high during address transition time.
 - 4. If CS# and OE# are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 - 5. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, output remains a high impedance state.
 - 6. tas is measured from the latest address transition to the later of CS# or WE# going low.
 - 7. twR is measured from the earlier of CS# or WE# going high to the first address transition.
 - 8. A write occurs during the overlap of a low CS# and a low WE#. A write begins at the latest transition among CS# going low and WE# going low. A write ends at the earliest transition among CS# going high and WE# going high. twp is measured from the beginning of write to the end of write.
 - 9. t_{CW} is measured from the later of CS# going low to the end of write.

Timing Waveforms

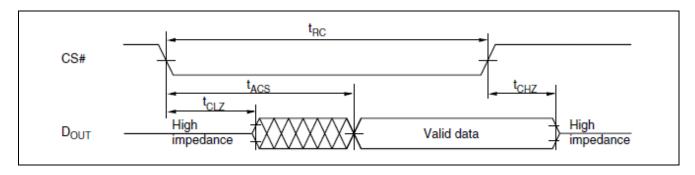
Read Timing Waveform (1) (WE# = VIH)



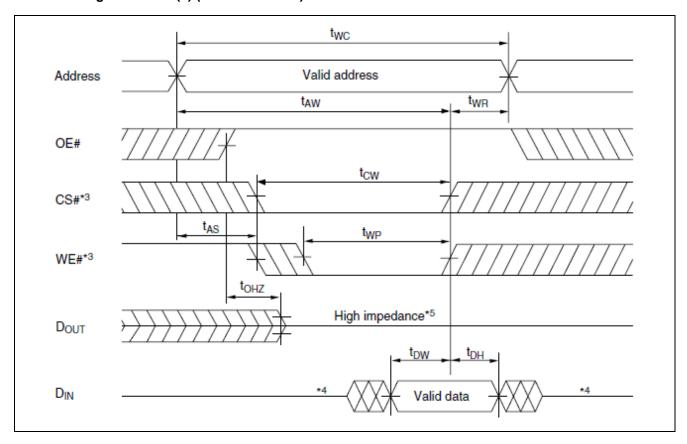
Read Timing Waveform (2) (WE# = V_{IH} , LB# = V_{IL} , UB# = V_{IL})



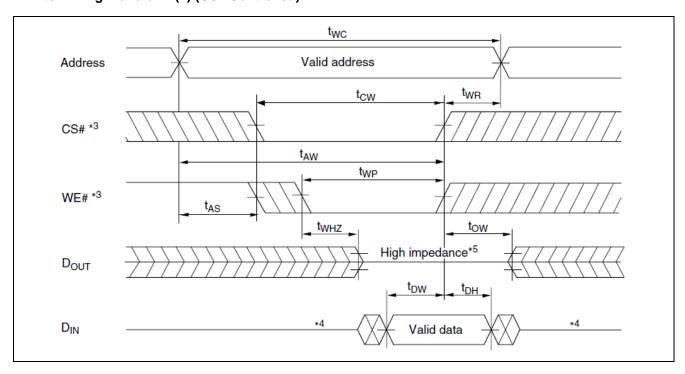
Read Timing Waveform (3) (WE# = V_{IH} , CS# = V_{IL} , OE# = V_{IL})*2



Write Timing Waveform (1) (WE# Controlled)



Write Timing Waveform (2) (CS# Controlled)



Revision History

			Description				
Rev.	Date	Page Summary					
1.00	Nov.18.19	-	First Edition issued				

All documents should contain the following section break and paragraph as the last item. The footers of this document refer to the paragraph in order to reference the last page of the document.

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