

# R2A20134ASP

R03DS0067EJ0301

Rev.3.01

Jan 08, 2016

## LED Lighting Power Controller

### Description

R2A20134ASP is a LED lighting controller IC.

Control method is a fixed frequency mode.

Error Amp Mode realizes High Power Factor and High Efficiency.

And the Peak Current Mode makes it possible to reduce external parts and realize low system cost.

The Error amp Mode control output current and the Peak Current Mode control output power.

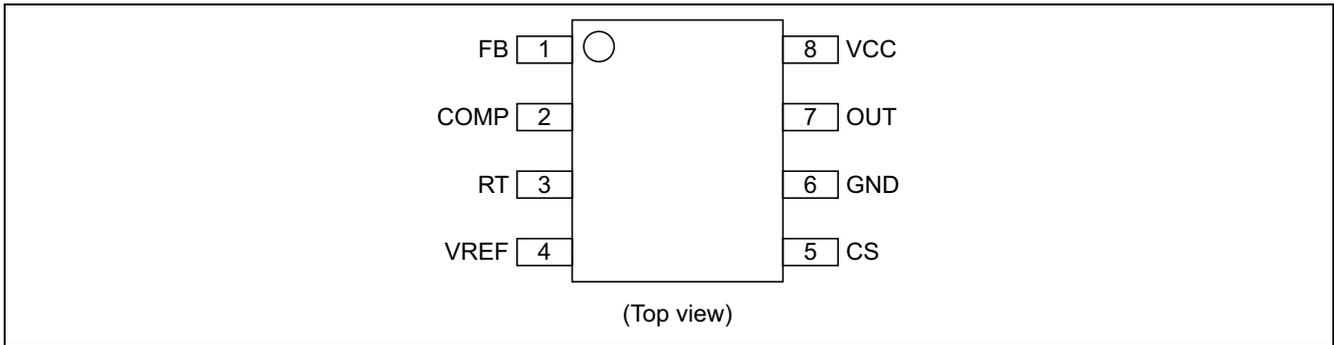
### Features

- Absolute maximum ratings
  - Supply voltage  $V_{cc}$ : 24 V
  - Junction temperature  $T_j$ :  $-40$  to  $+150^{\circ}\text{C}$
- Electrical characteristics
  - UVLO operation start voltage  $V_H$ :  $12\text{ V} \pm 0.8\text{ V}$
  - UVLO operation shutdown voltage  $V_L$ :  $9.2\text{ V} \pm 0.7\text{ V}$
  - UVLO hysteresis voltage  $H_{ysuvl}$ :  $2.8\text{ V} \pm 0.7\text{ V}$
- Functions
  - Fixed frequency mode (When  $R_{rt}$  is connected by  $V_{ref}$ )
  - Overcurrent protection (2step)
  - Overvoltage protection
  - Thermal shutdown (T.S.D.)
  - Package lineup: Pb-free SOP-8 (JEDEC)

### Ordering Information

Part No.	Package Name	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
R2A20134ASP#W5	—	PRSP0008DJ-A	SP	W (2,500 pcs/reel)

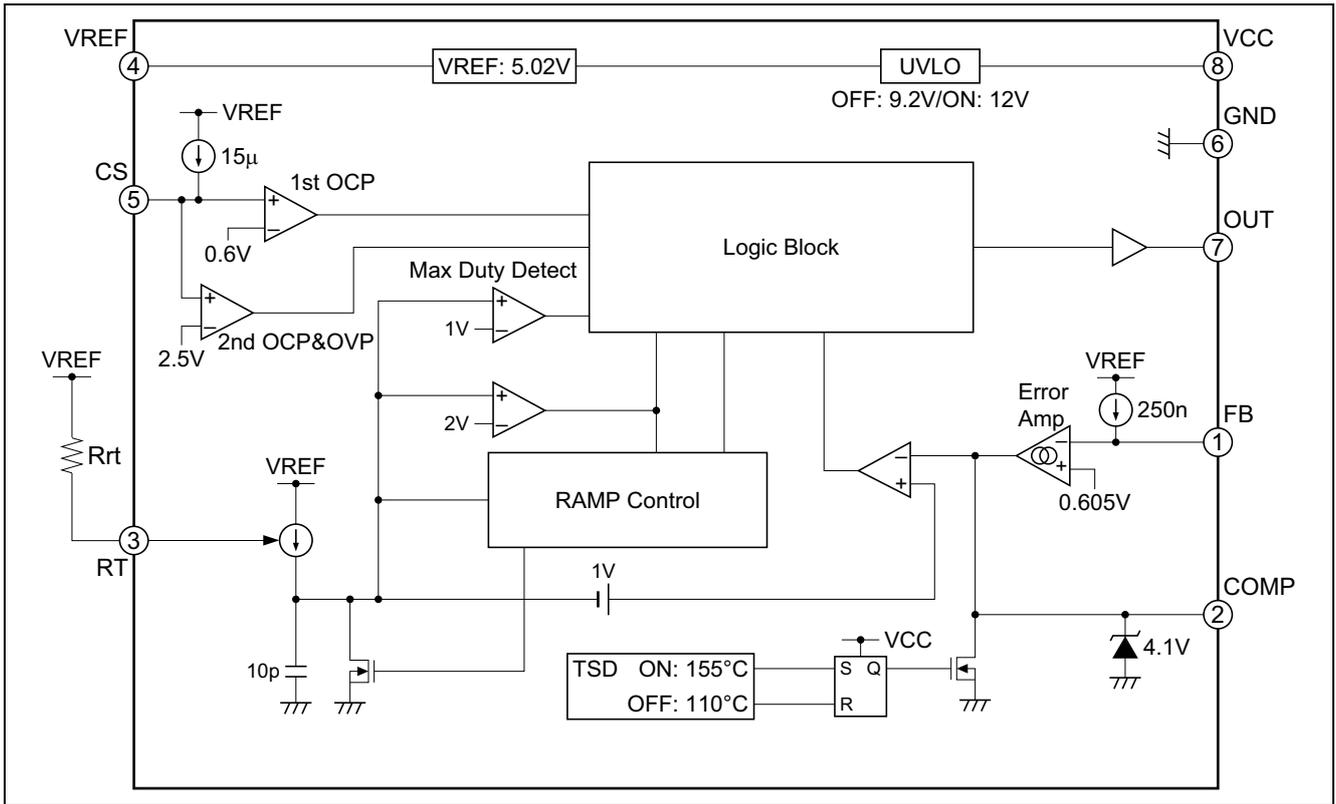
## Pin Arrangement



## Pin Function

Pin No.	Pin Name	Input/Output	Function
1	FB	Input	Error amplifier input terminal
2	COMP	Output	Error amplifier output terminal
3	RT	Input/Output	A resistor connection terminal for RAMP current setting
4	VREF	Output	Reference voltage output terminal
5	CS	Input	Overcurrent detection and overvoltage detection input terminal
6	GND	—	Ground
7	OUT	Output	Power MOSFET drive terminal
8	VCC	Input	Supply voltage terminal

### Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Power supply voltage	VCC	-0.3 to +24	V	
OUT terminal peak current	Ipk-snk-out	0.9	A	3
	Ipk-src-out	-0.50		
OUT terminal DC current	I <sub>dc</sub> -snk-out	100	mA	
	I <sub>dc</sub> -src-out	-50		
RT terminal current	I <sub>rt</sub>	200	μA	
VREF terminal current	I <sub>ref</sub>	-5	mA	
VREF terminal voltage	V <sub>t-ref</sub>	-0.3 to V <sub>ref</sub> + 0.3	V	
FB terminal voltage	V <sub>t-fb</sub>	-0.3 to +5	V	
CS terminal voltage	V <sub>cs</sub>	-0.3 to +5	V	
Power dissipation	P <sub>t</sub>	0.68	W	4
Operating ambient temperature	T <sub>a-opr</sub>	-40 to +125	°C	
Junction temperature	T <sub>j</sub>	-40 to +150	°C	5
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

- Notes:
- Rated voltages are with reference to the GND terminal.
  - For rated currents, inflow to the IC is indicated by (+), and outflow by (-).
  - Shows the transient current when driving a capacitive load.
  - In case of R2A20134ASP:  $\theta_{ja} = 120^{\circ}\text{C/W}$   
This value is a thing mounting on  $40 \times 40 \times 1.6$  [mm], a glass epoxy board of wiring density 10%.
  - Stresses exceeding the absolute maximum ratings may damage the device.  
These are stress ratings only. Functional operation above the recommended operating ambient temperature range is not implied.  
Extended exposure to stresses above the absolute maximum ratings may affect device reliability.

## Electrical Characteristics

(Ta = 25°C, VCC = 15 V, CS = 0 V, FB = COMP, RRT = 200 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	UVLO turn-on threshold	Vuvlh	11.2	12	12.8	V	
	UVLO turn-off threshold	Vuvll	8.5	9.2	9.9	V	
	UVLO hysteresis	Hysuvl	2.1	2.8	3.5	V	
	Standby current	Istby	—	130	250	μA	VCC = Vuvlh – 0.2 V
	Operating current	Icc	—	2.2	3.3	mA	FB: GND
VREF	Reference voltage	Vref	4.945	5.020	5.095	V	Isource = 0 mA
	Temperature stability	dVref	—	±80	—	ppm/°C	Tj = –40 to 150°C *1
	Line regulation	Vref-line	—	5	20	mV	Isource = 0 mA Vcc = 10 V to 24 V
	Load regulation	Vref-load	—	5	20	mV	Isource = 0 mA to –5 mA
Error amplifier	Feedback voltage	Vfb	0.587	0.605	0.623	V	
	Input bias current	Ifb	–0.75	–0.25	–0.1	μA	Measured pin: FB
	Open loop gain	Av	—	63	—	dB	
	Upper clamp voltage	Vclamp_comp	3.85	4.10	4.30	V	FB = 0.3 V COMP: Open
	Low voltage	Vl-comp	—	0.1	0.3	V	FB = 0.9 V COMP: Open
	Source current	Isrc-comp	–13	–9.5	–6	μA	FB = 0.3 V COMP: 2.5 V
	Sink current	Isnk-comp	6	9.5	13	μA	FB = 0.9 V COMP: 2.5 V
	Transconductance	gm	25	45	70	μs	FB = 0.55 V ↔ 0.65 V COMP: 2.5 V
RT	RAMP offset voltage	Voffset_ramp	—	1.0	—	V	
	RAMP amplitude	dVramp	2.9	3.1	3.3	V	*2
	RT voltage2	V-rt2	2.9	3.0	3.1	V	RT-Vref: 200 kΩ

Notes: 1. Design spec.

2. dVramp = Vclamp\_comp – Voffset\_ramp

## Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 15 V, CS = 0 V, FB = COMP, RRT = 200 kΩ)

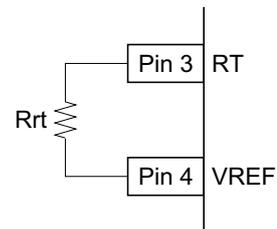
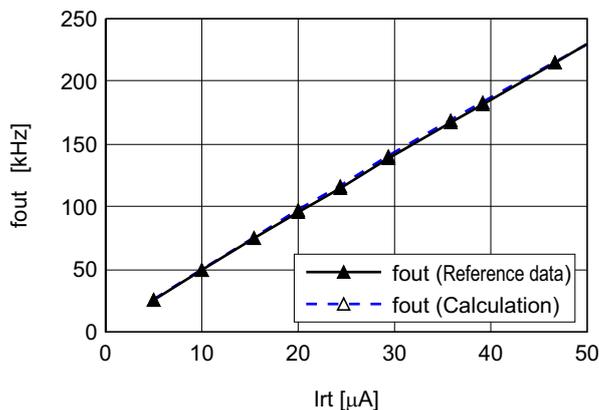
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
OUT	Rise time	tr-out	—	30	100	ns	CL = 1000 pF, FB = 0.3 V, COMP = 2.5 V
	Fall time	tf-out	—	30	100	ns	CL = 1000 pF, FB = 0.3 V, COMP = 2.5 V
	OUT low voltage	Vol1-out	—	0.08	0.20	V	Isink = 20 mA
		Vol2-out	—	0.05	0.70	V	Isink = 10 mA, VCC = 5 V
	OUT high voltage	Voh-out	14.5	14.8	—	V	Isource = -20 mA *1
	OUT frequency	fout	43	48	53	kHz	RT-Vref: 200 kΩ *3
Maximum duty cycle	Dmax	47	52	57	%	RT-Vref: 200 kΩ	
Over current protection	OCP threshold voltage	Vocp	0.57	0.6	0.63	V	
	OCP blanking time	tblank	170	300	450	ns	
	Input bias current	Ics	-30	-15	-7.5	μA	Vcs = 0 mV
2nd over current and over voltage protection	2nd OCP threshold voltage	V2ndocp	2.25	2.5	2.75	V	
Thermal shut down	Shut down temperature	TSD_ON	140	155	170	°C	*1
	TSD release temperature	TSD_OFF	90	110	130	°C	*1

Notes: 1. Design spec.

3. The fout is adjusted by changing resistance of Rrt connected between RT-VREF terminals.  
Reference data and a calculating formula are shown as follows.

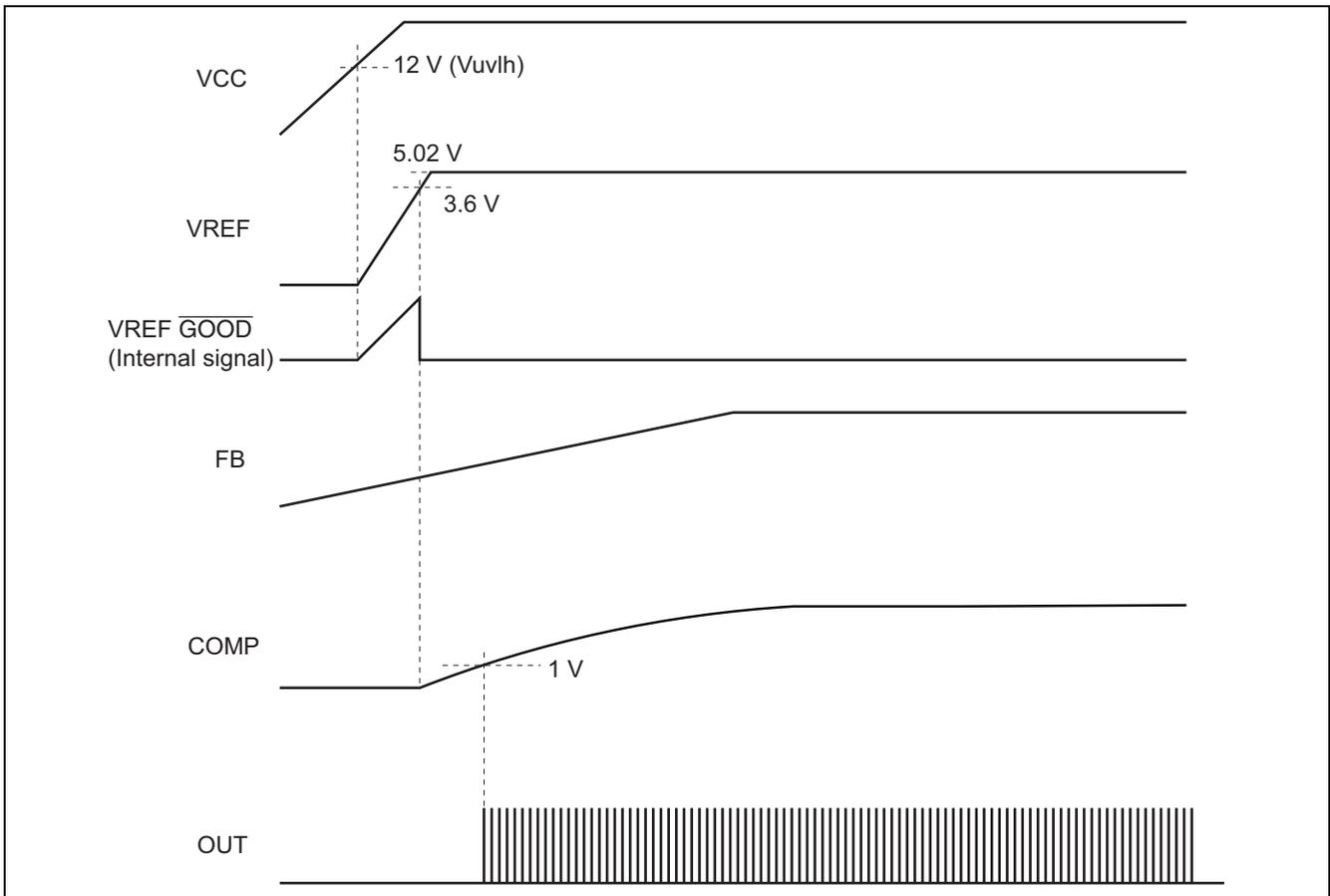
$$f_{out} [\text{kHz}] = \frac{1}{(100 \times 10^{-9} \times R_{rt}) + (360 \times 10^{-6})}$$

\* The graph is for reference only and does not guarantee actual characteristic.

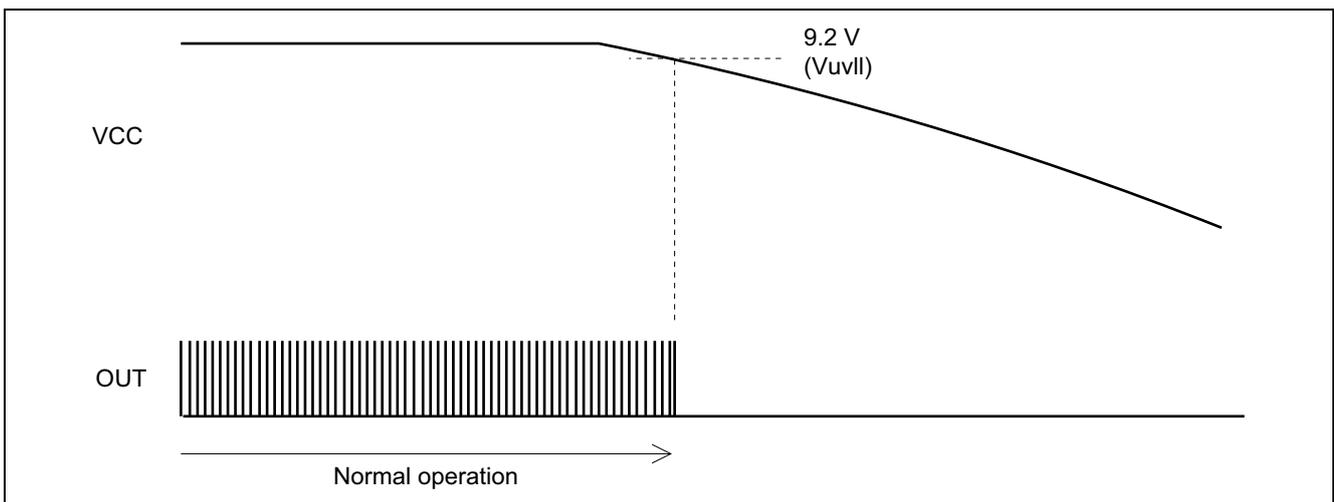


## Waveforms

### 1. Start-up Timing

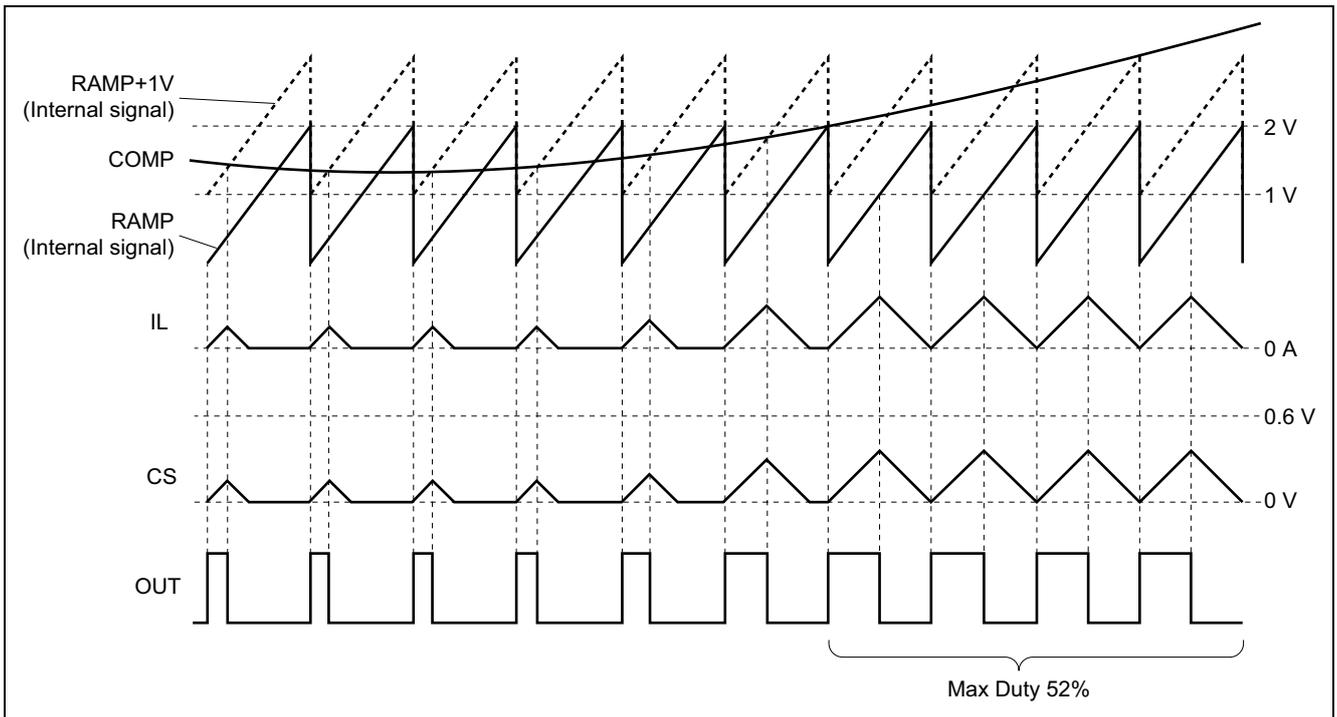


### 2. Stop Timing

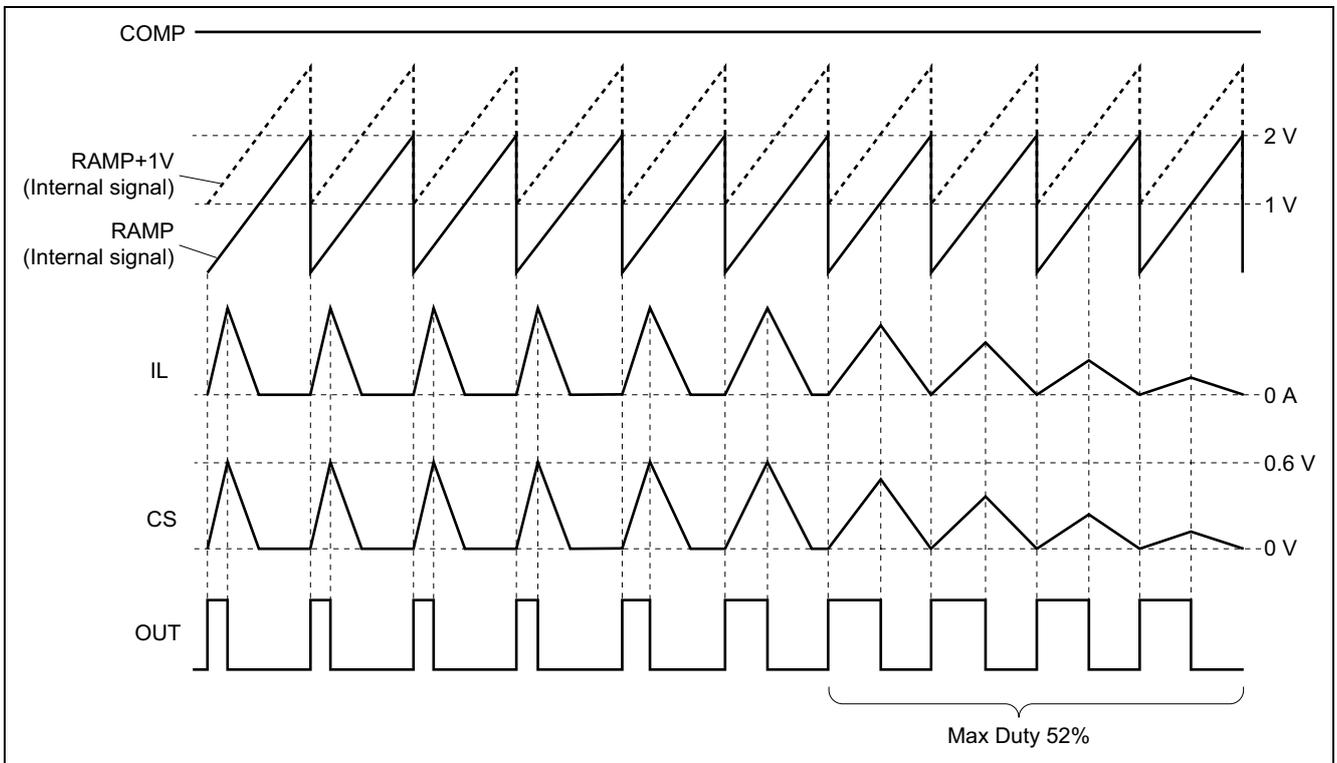


### 3. Gate Drive Output

#### 3.1 Error Amp Mode

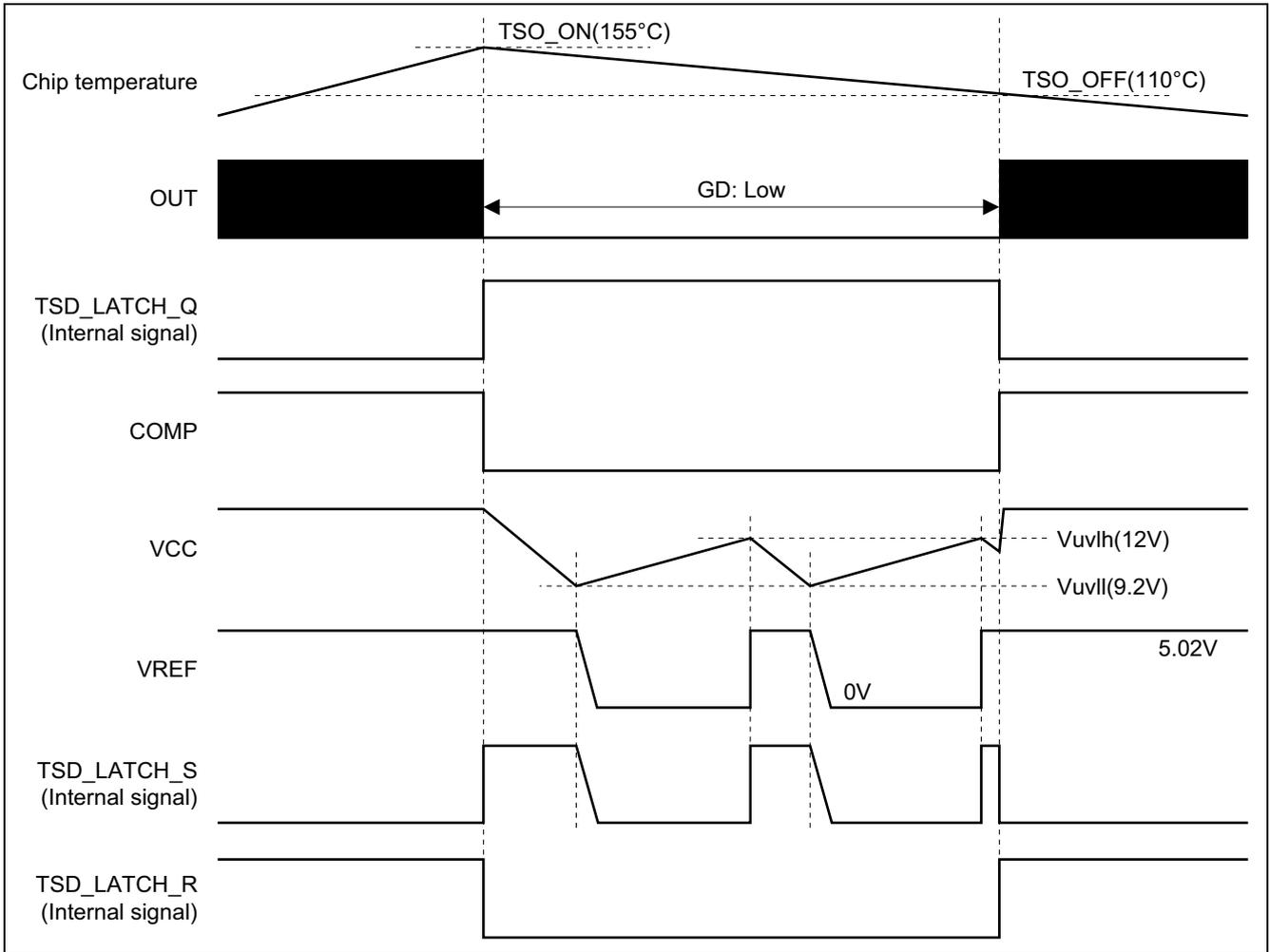


#### 3.2 Peak Current Mode



### 4. Thermal shutdown

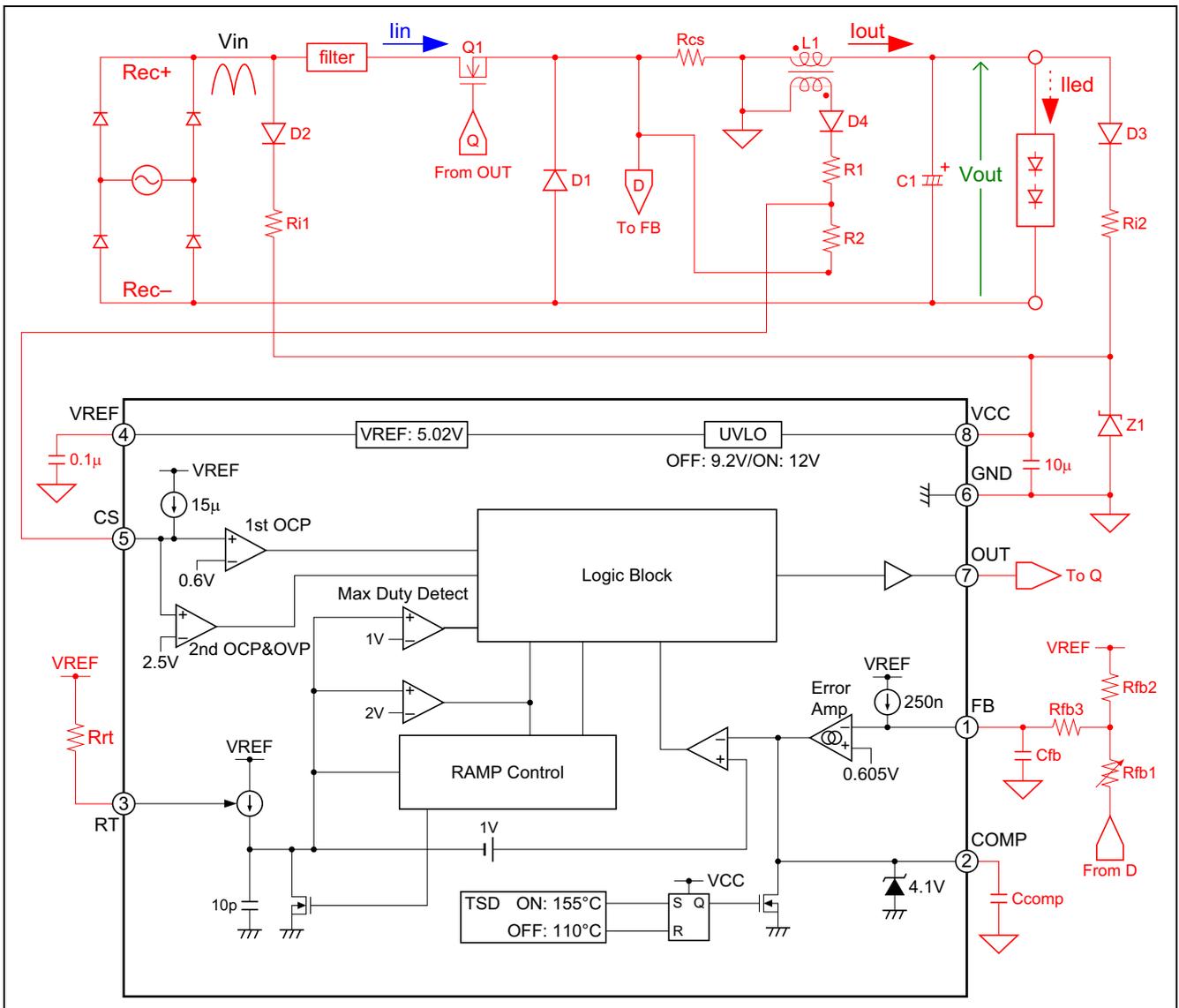
Note: TSD reset by chip temperature (TSD latch is removed by setting  $V_{cc} < 2.5\text{ V}$ .)



## System Diagram

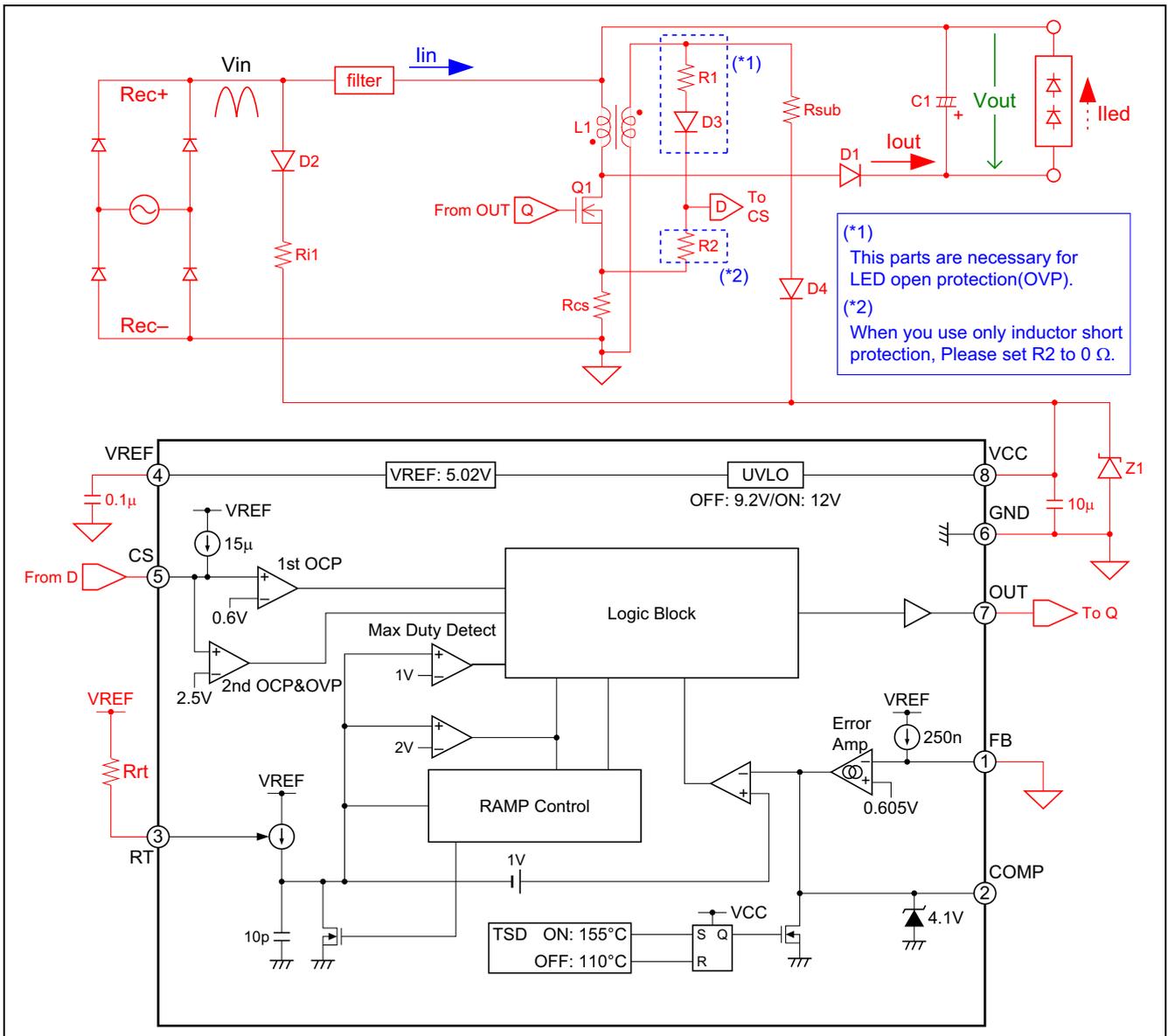
### 1. Error Amp control Mode / Buck-converter

#### 1.1 System Diagram

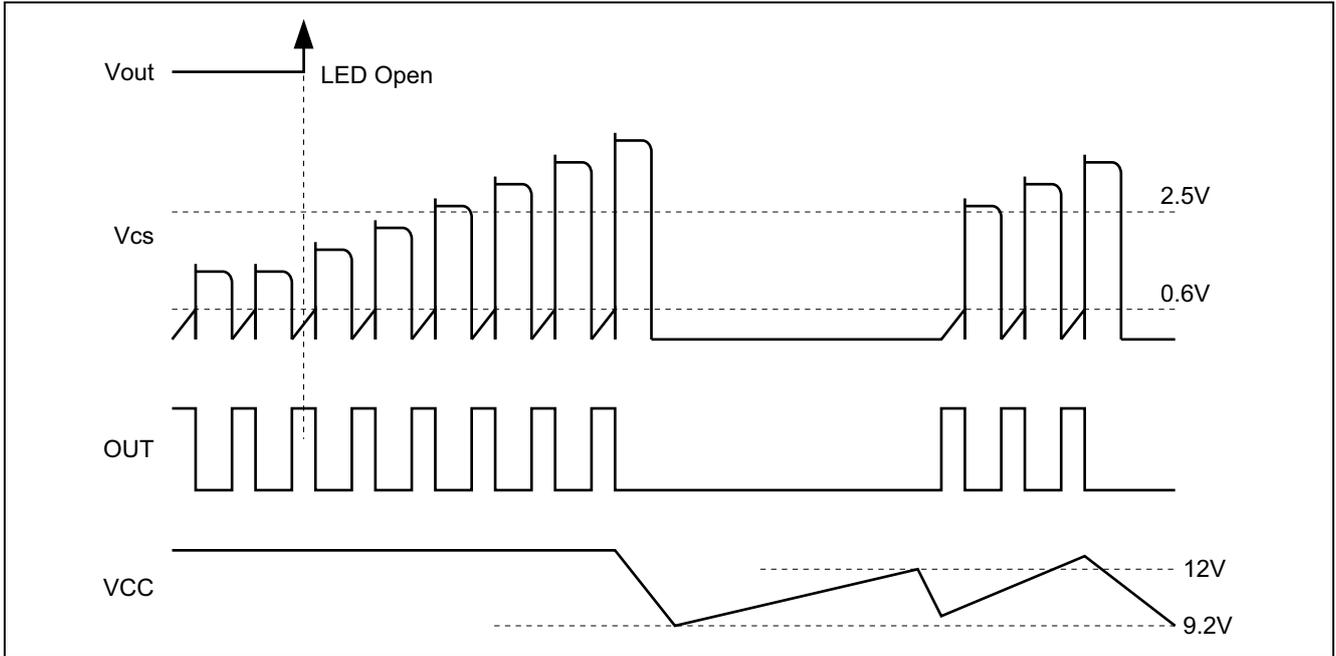


## 2. Peak Current and Zero Current Detection Mode Buck-Converter

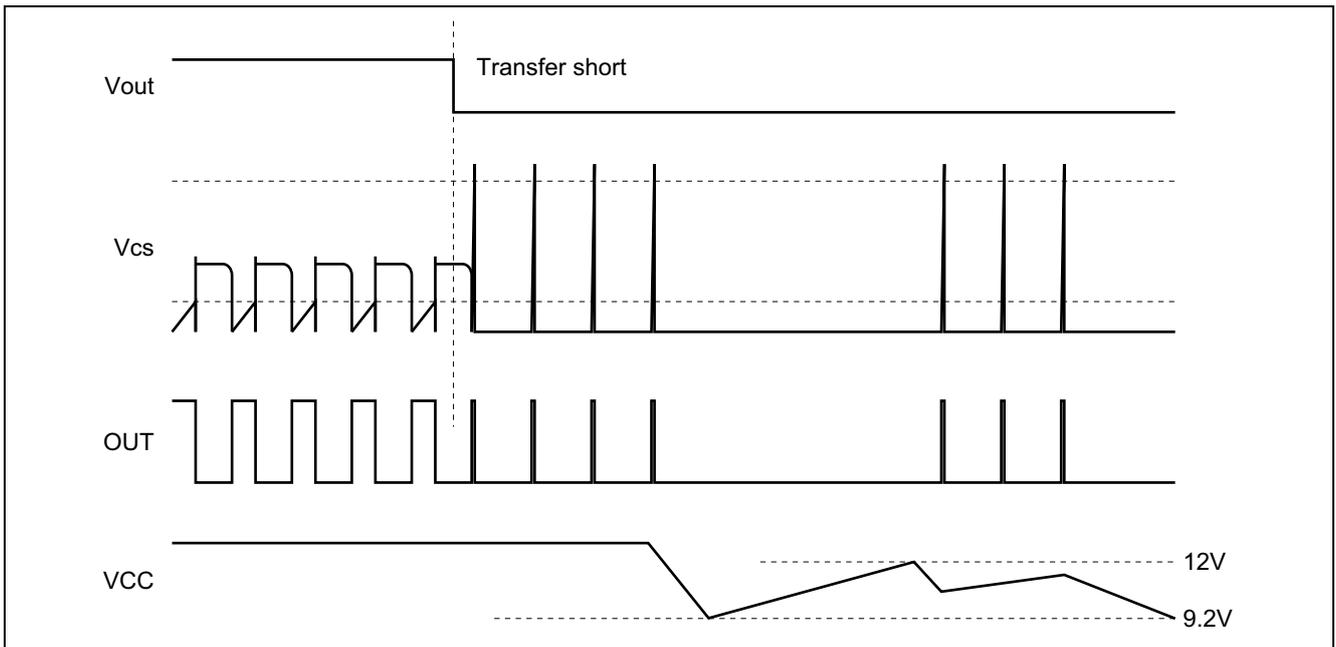
### 2.1 System Diagram



### 2.2 Waveforms of LED Open Protection (2nd OCP)

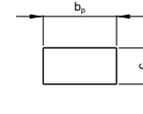
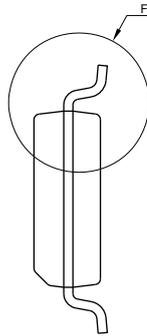
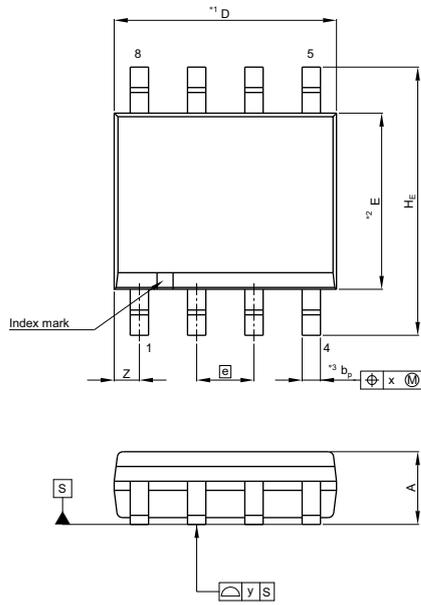


### 2.3 Waveforms of Transfer Short Protection

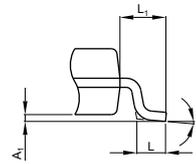


### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-3.94x4.93-1.27	PRSP0008DJ-A	—	0.073g



Terminal cross section  
(Ni/Pd/Au plating)



Detail F

NOTE)  
1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION\*\*3\*DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.80	4.93	4.98
E	3.81	3.94	3.99
A <sub>2</sub>	—	1.47	—
A <sub>1</sub>	0.10	0.15	0.25
A	—	—	1.73
b <sub>p</sub>	0.35	0.41	0.49
b <sub>1</sub>	—	—	—
c	0.19	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
HE	5.84	5.99	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
Z	—	0.56	—
L	0.41	0.64	0.89
L <sub>1</sub>	—	1.03	—

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