1. Overview

1.1 Features

The M16C Family offers a robust platform of 32-/16-bit CISC microcomputers (MCUs) featuring high ROM code efficiency, extensive EMI/EMS noise immunity, ultra-low power consumption, high-speed processing in actual applications, and numerous and varied integrated peripherals. Extensive device scalability from low- to high-end, featuring a single architecture as well as compatible pin assignments and peripheral functions, provides support for a vast range of application fields.

The R32C/100 Series is a high-end microcontroller series in the M16C Family. With a 4-Gbyte memory space, it achieves maximum code efficiency and high-speed processing with 32-bit CISC architecture, multiplier, multiply-accumulate unit, and floating point unit. The selection from the broadest choice of on-chip peripheral devices — UART, CRC, DMAC, A/D and D/A converters, timers, I^2C, and watchdog timer enables to minimize external components.

The R32C/100 Series, in particular, provides the R32C/142 Group and R32C/145 Group, products specific to gateway for in-vehicle network. These products, provided as 100-pin plastic molded LQFP package, have two channels of LIN module, three channels (R32C/142 Group) or six channels (R32C/145 Group) of CAN module, a CAN gateway module, and standard peripherals.

1.1.1 Applications

Automotive, etc.

1.1.2 Performance Overview

Table 1.1 and Table 1.2 show the performance overview of the R32C/142 Group and R32C/145 Group.

Table 1.1 Performance Overview (1/2)

Unit	Function	Explanation
CPU	Central processing unit	R32C/100 Series CPU Core • Basic instructions: 108 • Minimum instruction execution time: 15.625 ns (f(CPU) = 64 MHz) • Multiplier: 32-bit × 32-bit → 64-bit • Multiply-accumulate unit: 32-bit × 32-bit + 64-bit → 64-bit • IEEE-754 compatible FPU: Single precision • 32-bit barrel shifter • Operating mode: Single-chip mode
Memory		Flash memory: 256/512 Kbytes RAM: 32 Kbytes Data flash: 4 Kbytes × 2 blocks Refer to Tables 1.3 and 1.4 for details
Clock	Clock generator	• 4 circuits (main clock, sub clock, PLL, on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-2 to divide-by-24 selectable • Low power modes: Wait mode, stop mode
Interrupts		Interrupt vectors: 261 External interrupt inputs: $\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4 Interrupt priority levels: 7
Watchdog Timer		15 bits × 1 (selectable input frequency from prescaler output) Automatic timer start function is available
DMA	DMAC	4 channels • Cycle-steal transfer mode • Request sources: 45 • 2 transfer modes: Single transfer, repeat transfer
	DMAC II	• Can be activated by any peripheral interrupt source • 3 transfer functions: Immediate data transfer, calculation transfer, chained transfer
I/O Ports	Programmable I/O ports	• 2 input-only ports • 84 CMOS I/O ports • A pull-up resistor is selectable for every 4 input ports
Timer	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3
	Timer B	16-bit timer × 6 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Three-phase motor control timer	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) 8-bit programmable dead time timer

Table 1.2 Performance Overview (2/2)

Unit	Function	Explanation
Serial Interface	UART0 to UART4	Asynchronous/synchronous serial interface × 5 channels • I^2C-bus (UART0 to UART2) • Special mode 2 (UART0 to UART2)
A/D Converter		10-bit resolution × 26 channels Sample and hold functionality integrated Self test/Open-circuit detection assist
D/A Converter		8-bit resolution × 2
CRC Calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
X-Y Converter		16 bits × 16 bits
Intelligent I/O		Time measurement (input capture): 16 bits × 16 Digital debounce circuit contained Waveform generation (output compare): 16 bits × 16 Phase shift waveform output mode contained
Serial Bus Interface		2 channels • Synchronous serial communication mode • 4-wire serial bus mode Programmable character length: 8 to 16 bits
LIN Module		2 channels
CAN Module		3 channels for the R32C/142 Group 6 channels for the R32C/145 Group CAN functionality compliant with ISO 11898-1 16 mailboxes
Gateway Module		Up to 3 CAN channel routing control available for the R32C/142 Group Up to 6 CAN channel routing control available for the R32C/145 Group Routing table: up to 384 entries
Flash Memory		Programming and erasure supply voltage: VCC = 4.2 to 5.5 V, VCC0 = 3.0 V to VCC Minimum endurance: 100 program/erase cycles Security protection: ROM code protect, ID code protect Debugging: On-chip debug, on-board flash programming
Operating Frequency/Supply Voltage		64 MHz/VCC = 4.2 to 5.5 V, VCC0 = 3.0 V to VCC
Operating Temperature		-40°C to 85°C (J version) -40°C to 105°C (L version) (1) -40°C to 125°C (K version) (1)
Current Consumption		46 mA (VCC = 5.0 V, VCC0 = 3.3 V, f(CPU) = 64 MHz) 8 µA (VCC = 5.0 V, VCC0 = 3.3 V, f(XCIN) = 32.768 kHz, wait mode)
Package		100-pin plastic molded LQFP (PLQP0100KB-A)

Note:
1. Contact a Renesas Electronics sales office to use the L or K version products.

1.2 Product Information

Table 1.3 and Table 1.4 list the product information of the R32C/142 Group and R32C/145 Group, and Figure 1.1 shows the details of the part number.

Table 1.3 R32C/142 Group Product List **As of September, 2011**

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F6442FJFB	PLQP0100KB-A	256 Kbytes + 8 Kbytes	32 Kbytes	J Version
R5F6442FLFB				L Version (3)
R5F6442FKFB				K Version (3)
R5F6442HJFB		512 Kbytes + 8 Kbytes		J Version
R5F6442HLFB				L Version (3)
R5F6442HKFB				K Version (3)

Notes:
1. The old package code is as follows:PLQP0100KB-A: 100P6Q-A
2. Data flash memory provides an additional 8 Kbytes of ROM.
3. Contact a Renesas Electronics sales office to use the L or K version products.

Table 1.4 R32C/145 Group Product List **As of September, 2011**

Part Number	Package Code (1)	ROM Capacity (2)	RAM Capacity	Remarks
R5F6445FJFB	PLQP0100KB-A	256 Kbytes + 8 Kbytes	32 Kbytes	J Version
R5F6445FLFB				L Version (3)
R5F6445FKFB				K Version (3)
R5F6445HJFB		512 Kbytes + 8 Kbytes		J Version
R5F6445HLFB				L Version (3)
R5F6445HKFB				K Version (3)

Notes:
1. The old package code is as follows:PLQP0100KB-A: 100P6Q-A
2. Data flash memory provides an additional 8 Kbytes of ROM.
3. Contact a Renesas Electronics sales office to use the L or K version products.

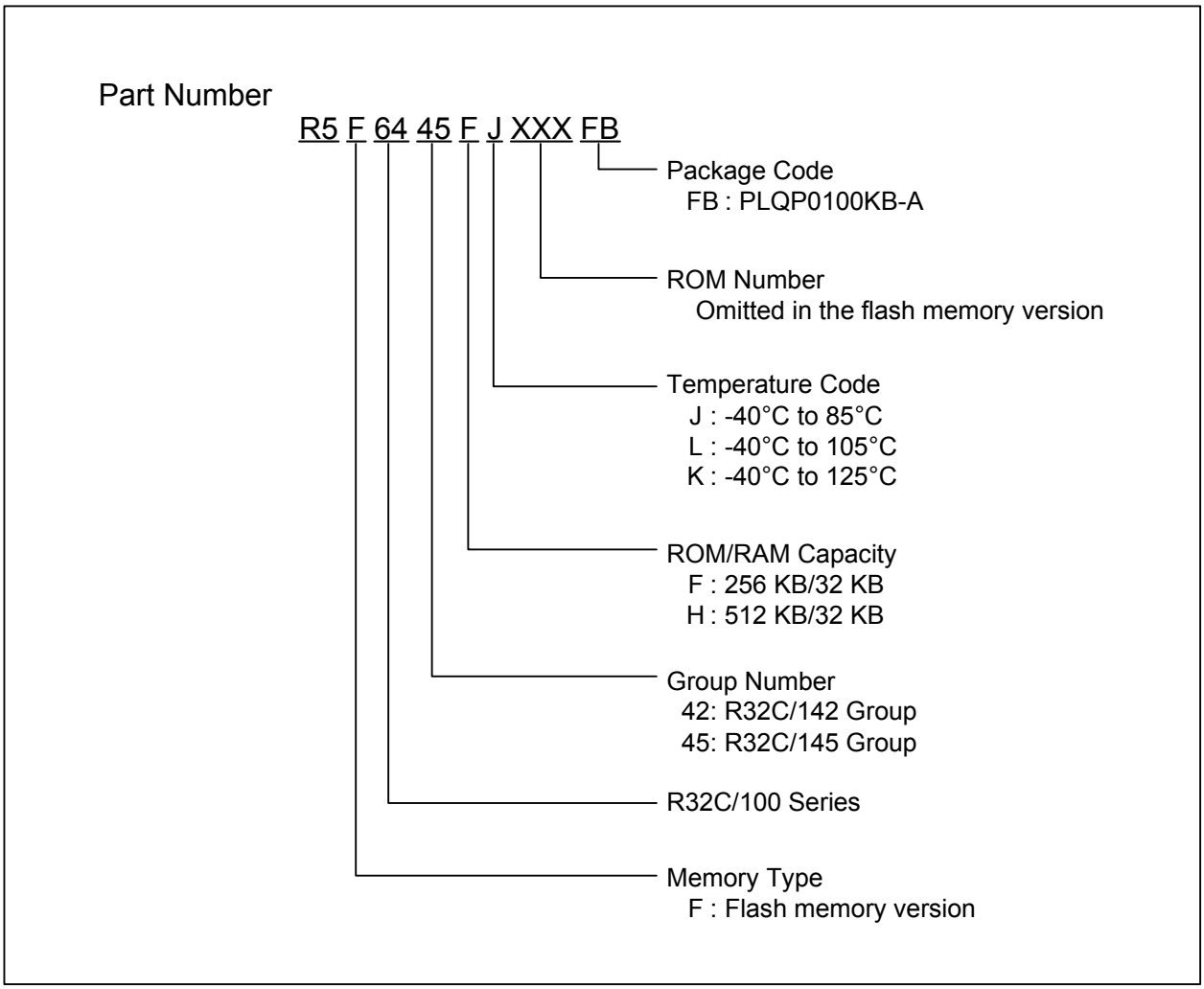


Figure 1.1 Part Numbering

1.3 Block Diagram

Figure 1.2 and Figure 1.3 show block diagrams of the R32C/142 Group and R32C/145 Group.

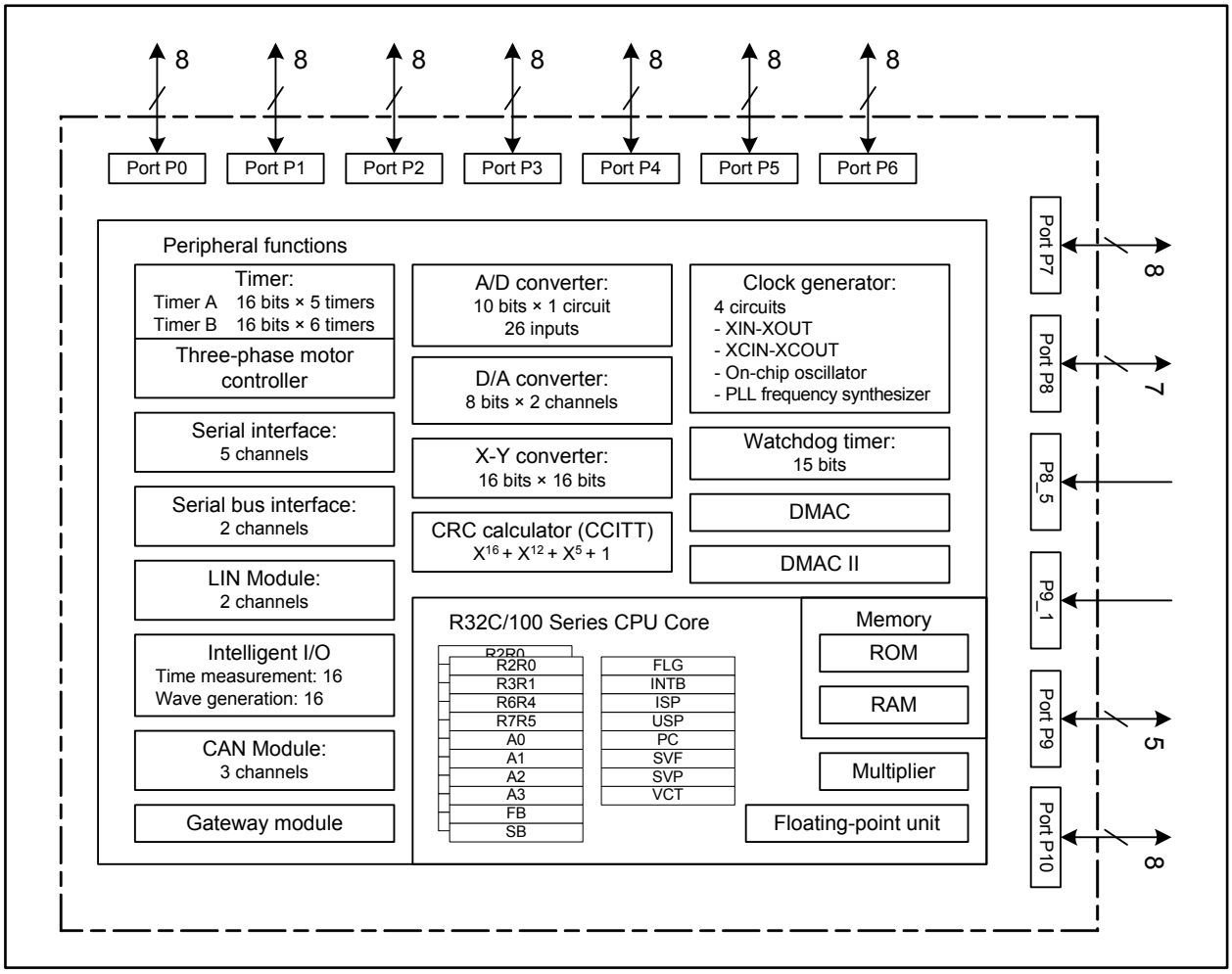


Figure 1.2 R32C/142 Group Block Diagram

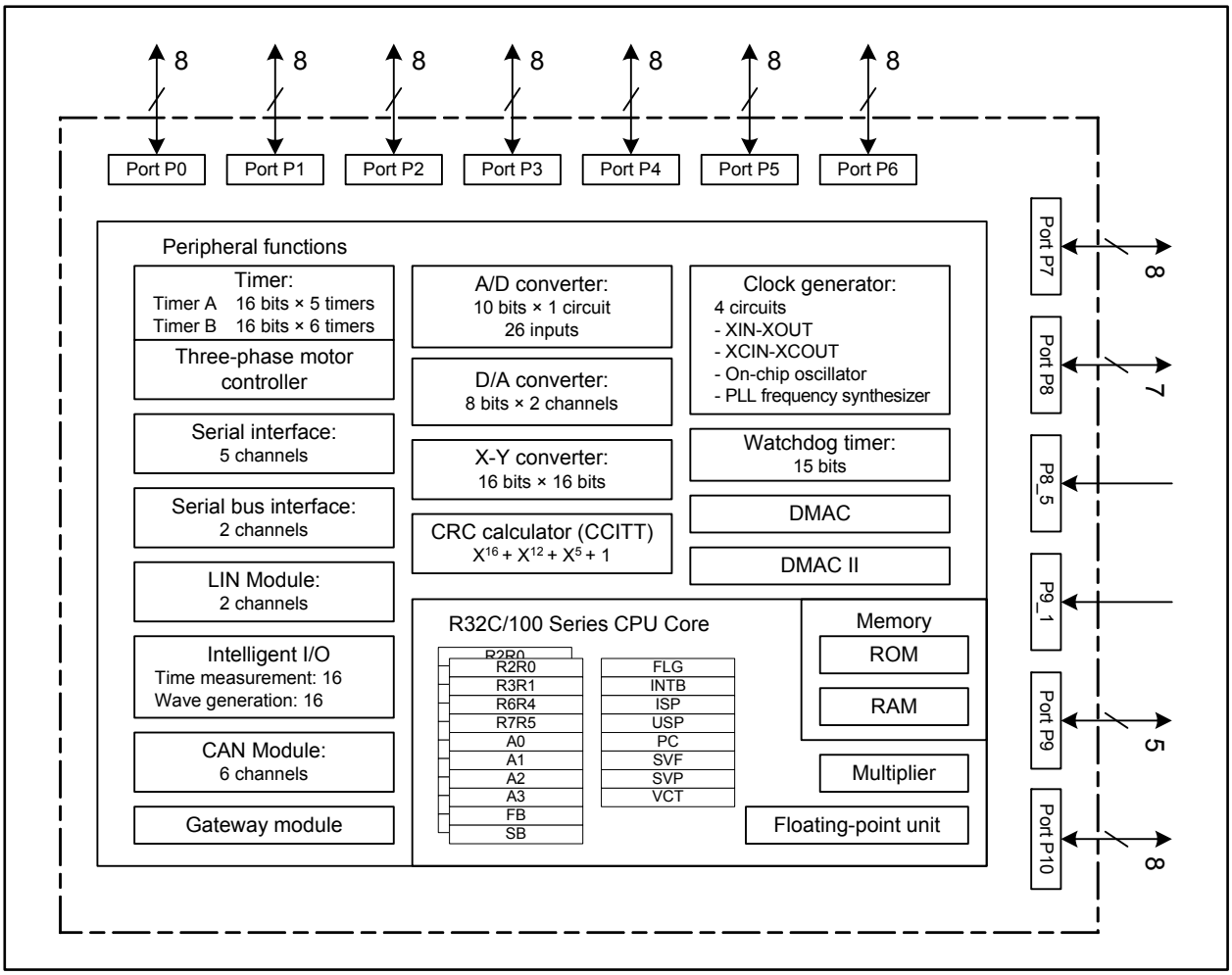
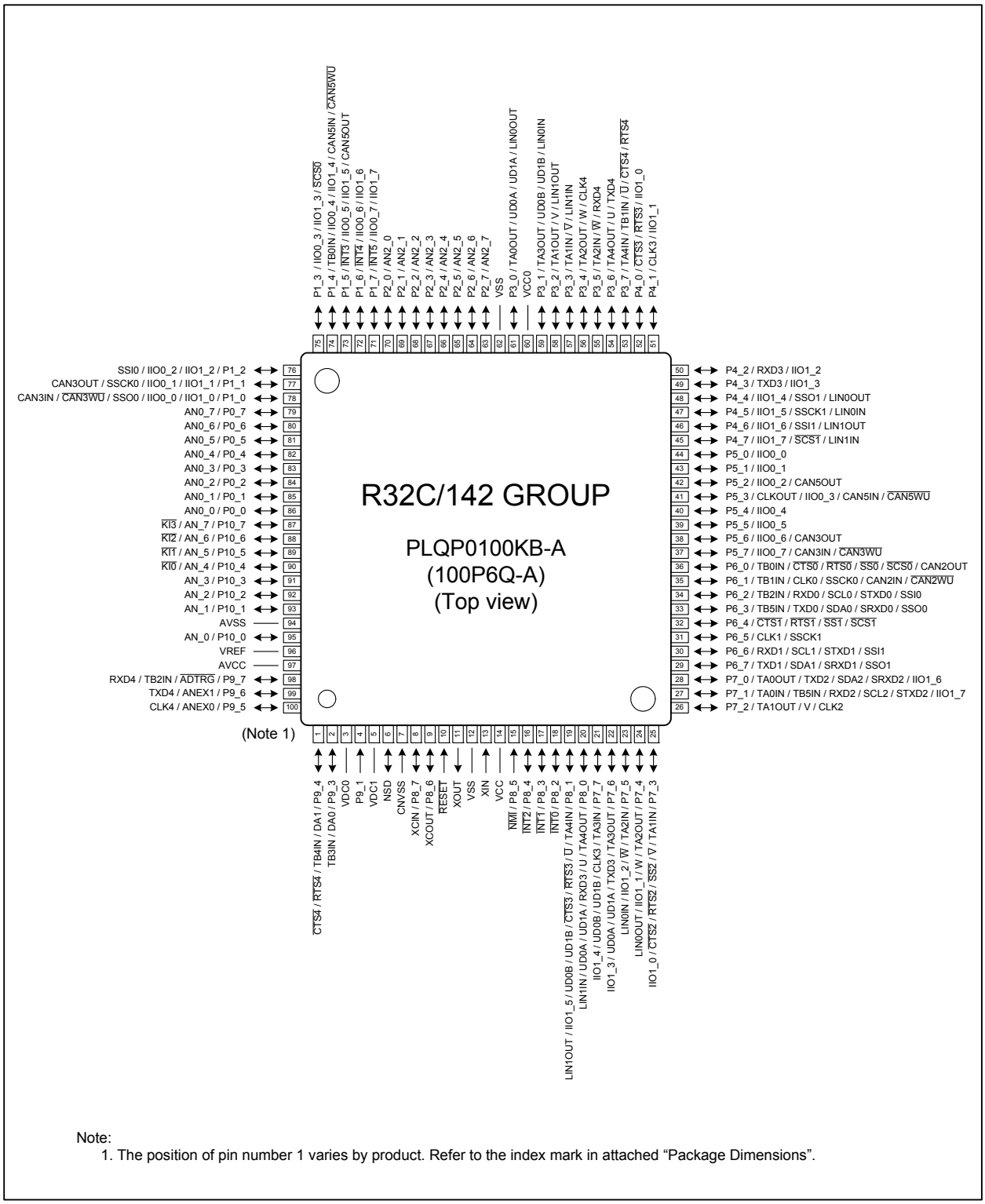


Figure 1.3 R32C/145 Group Block Diagram

1.4 Pin Assignment

Figure 1.4 and Figure 1.5 show the pin assignments (top view) and Table 1.5 to Table 1.10 show the pin characteristics of the R32C/142 Group and R32C/145 Group.



Note:
1. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.4 R32C/142 Group Pin Assignment (top view)

Table 1.5 Pin Characteristics for the R32C/142 Group (1/3)

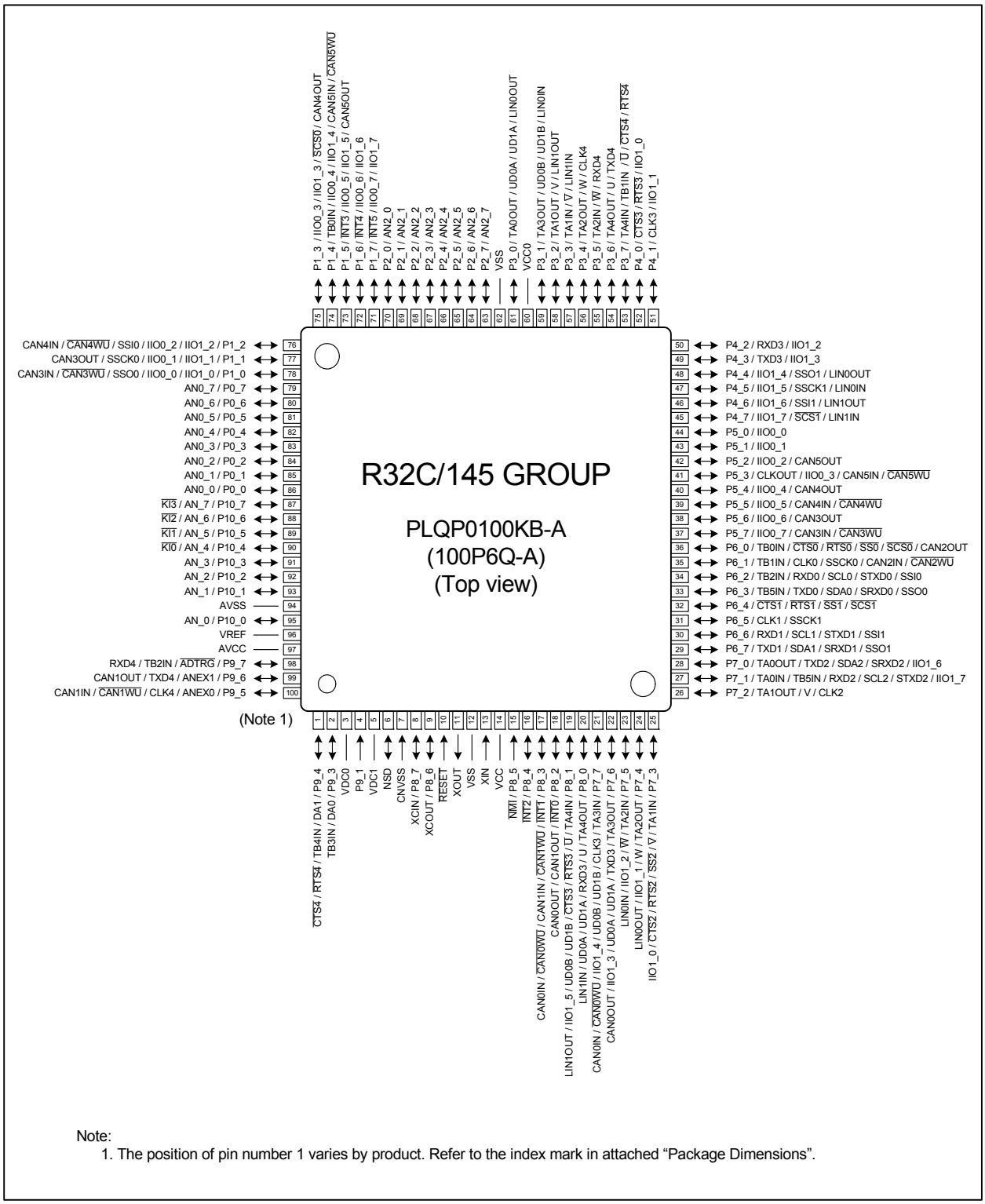
Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
1		P9_4		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$			DA1
2		P9_3		TB3IN				DA0
3	VDC0							
4		P9_1						
5	VDC1							
6	NSD							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	$\overline{\text{RESET}}$							
11	XOUT							
12	VSS							
13	XIN							
14	VCC							
15		P8_5	$\overline{\text{NMI}}$					
16		P8_4	$\overline{\text{INT2}}$					
17		P8_3	$\overline{\text{INT1}}$					
18		P8_2	$\overline{\text{INT0}}$					
19		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$	IIO1_5/UD0B/UD1B	LIN1OUT	
20		P8_0		TA4OUT/U	RXD3	UD0A/UD1A	LIN1IN	
21		P7_7		TA3IN	CLK3	IIO1_4/UD0B/UD1B		
22		P7_6		TA3OUT	TXD3	IIO1_3/UD0A/UD1A		
23		P7_5		TA2IN/$\overline{\text{W}}$		IIO1_2	LIN0IN	
24		P7_4		TA2OUT/W		IIO1_1	LIN0OUT	
25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	IIO1_0		
26		P7_2		TA1OUT/V	CLK2			
27		P7_1		TA0IN/ TB5IN	RXD2/SCL2/ STXD2	IIO1_7		
28		P7_0		TA0OUT	TXD2/SDA2/ SRXD2	IIO1_6		
29		P6_7			TXD1/SDA1/ SRXD1/SSO1			
30		P6_6			RXD1/SCL1/ STXD1/SSI1			
31		P6_5			CLK1/SSCK1			
32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$/ $\overline{\text{SCS1}}$			
33		P6_3		TB5IN	TXD0/SDA0/ SRXD0/SSO0			

Table 1.6 Pin Characteristics for the R32C/142 Group (2/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
34		P6_2		TB2IN	RXD0/SCL0/ STXD0/SSI0			
35		P6_1		TB1IN	CLK0/SSCK0		CAN2IN/$\overline{\text{CAN2WU}}$	
36		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$/ $\overline{\text{SCS0}}$		CAN2OUT	
37		P5_7				IIO0_7	CAN3IN/$\overline{\text{CAN3WU}}$	
38		P5_6				IIO0_6	CAN3OUT	
39		P5_5				IIO0_5		
40		P5_4				IIO0_4		
41	CLK-OUT	P5_3				IIO0_3	CAN5IN/$\overline{\text{CAN5WU}}$	
42		P5_2				IIO0_2	CAN5OUT	
43		P5_1				IIO0_1		
44		P5_0				IIO0_0		
45		P4_7			$\overline{\text{SCS1}}$	IIO1_7	LIN1IN	
46		P4_6			SSI1	IIO1_6	LIN1OUT	
47		P4_5			SSCK1	IIO1_5	LIN0IN	
48		P4_4			SSO1	IIO1_4	LIN0OUT	
49		P4_3			TXD3	IIO1_3		
50		P4_2			RXD3	IIO1_2		
51		P4_1			CLK3	IIO1_1		
52		P4_0			$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$	IIO1_0		
53		P3_7		TA4IN/ TB1IN/$\overline{\text{U}}$	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$			
54		P3_6		TA4OUT/U	TXD4			
55		P3_5		TA2IN/$\overline{\text{W}}$	RXD4			
56		P3_4		TA2OUT/W	CLK4			
57		P3_3		TA1IN/$\overline{\text{V}}$			LIN1IN	
58		P3_2		TA1OUT/V			LIN1OUT	
59		P3_1		TA3OUT		UD0B/UD1B	LIN0IN	
60	VCC0							
61		P3_0		TA0OUT		UD0A/UD1A	LIN0OUT	
62	VSS							
63		P2_7						AN2_7
64		P2_6						AN2_6
65		P2_5						AN2_5
66		P2_4						AN2_4
67		P2_3						AN2_3
68		P2_2						AN2_2
69		P2_1						AN2_1
70		P2_0						AN2_0
71		P1_7	$\overline{\text{INT5}}$			IIO0_7/IIO1_7		
72		P1_6	$\overline{\text{INT4}}$			IIO0_6/IIO1_6		

Table 1.7 Pin Characteristics for the R32C/142 Group (3/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
73		P1_5	$\overline{INT3}$			IIO0_5/IIO1_5	CAN5OUT	
74		P1_4		TB0IN		IIO0_4/IIO1_4	CAN5IN/$\overline{CAN5WU}$	
75		P1_3			$\overline{SCS0}$	IIO0_3/IIO1_3		
76		P1_2			SSI0	IIO0_2/IIO1_2		
77		P1_1			SSCK0	IIO0_1/IIO1_1	CAN3OUT	
78		P1_0			SSO0	IIO0_0/IIO1_0	CAN3IN/$\overline{CAN3WU}$	
79		P0_7						AN0_7
80		P0_6						AN0_6
81		P0_5						AN0_5
82		P0_4						AN0_4
83		P0_3						AN0_3
84		P0_2						AN0_2
85		P0_1						AN0_1
86		P0_0						AN0_0
87		P10_7	$\overline{KI3}$					AN_7
88		P10_6	$\overline{KI2}$					AN_6
89		P10_5	$\overline{KI1}$					AN_5
90		P10_4	$\overline{KI0}$					AN_4
91		P10_3						AN_3
92		P10_2						AN_2
93		P10_1						AN_1
94	AVSS							
95		P10_0						AN_0
96	VREF							
97	AVCC							
98		P9_7		TB2IN	RXD4			$\overline{ADTRG}$
99		P9_6			TXD4			ANEX1
100		P9_5			CLK4			ANEX0



Note:
1. The position of pin number 1 varies by product. Refer to the index mark in attached “Package Dimensions”.

Figure 1.5 R32C/145 Group Pin Assignment (top view)

Table 1.8 Pin Characteristics for the R32C/145 Group (1/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
1		P9_4		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$			DA1
2		P9_3		TB3IN				DA0
3	VDC0							
4		P9_1						
5	VDC1							
6	NSD							
7	CNVSS							
8	XCIN	P8_7						
9	XCOUT	P8_6						
10	$\overline{\text{RESET}}$							
11	XOUT							
12	VSS							
13	XIN							
14	VCC							
15		P8_5	$\overline{\text{NMI}}$					
16		P8_4	$\overline{\text{INT2}}$					
17		P8_3	$\overline{\text{INT1}}$				CAN0IN/$\overline{\text{CAN0WU}}$/ CAN1IN/$\overline{\text{CAN1WU}}$	
18		P8_2	$\overline{\text{INT0}}$				CAN0OUT/ CAN1OUT	
19		P8_1		TA4IN/$\overline{\text{U}}$	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$	IIO1_5/UD0B/UD1B	LIN1OUT	
20		P8_0		TA4OUT/U	RXD3	UD0A/UD1A	LIN1IN	
21		P7_7		TA3IN	CLK3	IIO1_4/UD0B/UD1B	CAN0IN/$\overline{\text{CAN0WU}}$	
22		P7_6		TA3OUT	TXD3	IIO1_3/UD0A/UD1A	CAN0OUT	
23		P7_5		TA2IN/$\overline{\text{W}}$		IIO1_2	LIN0IN	
24		P7_4		TA2OUT/W		IIO1_1	LIN0OUT	
25		P7_3		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	IIO1_0		
26		P7_2		TA1OUT/V	CLK2			
27		P7_1		TA0IN/ TB5IN	RXD2/SCL2/ STXD2	IIO1_7		
28		P7_0		TA0OUT	TXD2/SDA2/ SRXD2	IIO1_6		
29		P6_7			TXD1/SDA1/ SRXD1/SSO1			
30		P6_6			RXD1/SCL1/ STXD1/SSI1			
31		P6_5			CLK1/SSCK1			
32		P6_4			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$/ $\overline{\text{SCS1}}$			
33		P6_3		TB5IN	TXD0/SDA0/ SRXD0/SSO0			

Table 1.9 Pin Characteristics for the R32C/145 Group (2/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
34		P6_2		TB2IN	RXD0/SCL0/ STXD0/SSI0			
35		P6_1		TB1IN	CLK0/SSCK0		CAN2IN/$\overline{\text{CAN2WU}}$	
36		P6_0		TB0IN	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$/ $\overline{\text{SCS0}}$		CAN2OUT	
37		P5_7				IIO0_7	CAN3IN/$\overline{\text{CAN3WU}}$	
38		P5_6				IIO0_6	CAN3OUT	
39		P5_5				IIO0_5	CAN4IN/$\overline{\text{CAN4WU}}$	
40		P5_4				IIO0_4	CAN4OUT	
41	CLK-OUT	P5_3				IIO0_3	CAN5IN/$\overline{\text{CAN5WU}}$	
42		P5_2				IIO0_2	CAN5OUT	
43		P5_1				IIO0_1		
44		P5_0				IIO0_0		
45		P4_7			$\overline{\text{SCS1}}$	IIO1_7	LIN1IN	
46		P4_6			SSI1	IIO1_6	LIN1OUT	
47		P4_5			SSCK1	IIO1_5	LIN0IN	
48		P4_4			SSO1	IIO1_4	LIN0OUT	
49		P4_3			TXD3	IIO1_3		
50		P4_2			RXD3	IIO1_2		
51		P4_1			CLK3	IIO1_1		
52		P4_0			$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$	IIO1_0		
53		P3_7		TA4IN/ TB1IN/$\overline{\text{U}}$	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$			
54		P3_6		TA4OUT/U	TXD4			
55		P3_5		TA2IN/$\overline{\text{W}}$	RXD4			
56		P3_4		TA2OUT/W	CLK4			
57		P3_3		TA1IN/$\overline{\text{V}}$			LIN1IN	
58		P3_2		TA1OUT/V			LIN1OUT	
59		P3_1		TA3OUT		UD0B/UD1B	LIN0IN	
60	VCC0							
61		P3_0		TA0OUT		UD0A/UD1A	LIN0OUT	
62	VSS							
63		P2_7						AN2_7
64		P2_6						AN2_6
65		P2_5						AN2_5
66		P2_4						AN2_4
67		P2_3						AN2_3
68		P2_2						AN2_2
69		P2_1						AN2_1
70		P2_0						AN2_0
71		P1_7	$\overline{\text{INT5}}$			IIO0_7/IIO1_7		
72		P1_6	$\overline{\text{INT4}}$			IIO0_6/IIO1_6		

Table 1.10 Pin Characteristics for the R32C/145 Group (3/3)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Intelligent I/O Pin	LIN / CAN Module Pin	Analog Pin
73		P1_5	$\overline{INT3}$			IIO0_5/IIO1_5	CAN5OUT	
74		P1_4		TB0IN		IIO0_4/IIO1_4	CAN5IN/$\overline{CAN5WU}$	
75		P1_3			$\overline{SCS0}$	IIO0_3/IIO1_3	CAN4OUT	
76		P1_2			SSI0	IIO0_2/IIO1_2	CAN4IN/$\overline{CAN4WU}$	
77		P1_1			SSCK0	IIO0_1/IIO1_1	CAN3OUT	
78		P1_0			SSO0	IIO0_0/IIO1_0	CAN3IN/$\overline{CAN3WU}$	
79		P0_7						AN0_7
80		P0_6						AN0_6
81		P0_5						AN0_5
82		P0_4						AN0_4
83		P0_3						AN0_3
84		P0_2						AN0_2
85		P0_1						AN0_1
86		P0_0						AN0_0
87		P10_7	$\overline{KI3}$					AN_7
88		P10_6	$\overline{KI2}$					AN_6
89		P10_5	$\overline{KI1}$					AN_5
90		P10_4	$\overline{KI0}$					AN_4
91		P10_3						AN_3
92		P10_2						AN_2
93		P10_1						AN_1
94	AVSS							
95		P10_0						AN_0
96	VREF							
97	AVCC							
98		P9_7		TB2IN	RXD4			$\overline{ADTRG}$
99		P9_6			TXD4		CAN1OUT	ANEX1
100		P9_5			CLK4		CAN1IN/$\overline{CAN1WU}$	ANEX0

1.5 Pin Definitions and Functions

Table 1.11 to Table 1.13 show the pin definitions and functions.

Table 1.11 Pin Definitions and Functions (1/3)

Function	Symbol	I/O	Description
Power supply	VCC, VCC0, VSS	I	Applicable as follows: VCC = 4.2 to 5.5 V, VCC0 = 3.0 to 5.5 V, VSS = 0 V. It must be VCC0 ≤ VCC
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. AVCC and AVSS should be connected to VCC and VSS, respectively
Connecting pins for decoupling capacitor	VDC0, VDC1	—	A decoupling capacitor for internal voltage should be connected between VDC0 and VDC1
Reset input	$\overline{\text{RESET}}$	I	The MCU is reset when this pin is driven low
CNVSS	CNVSS	I	This pin should be connected to VSS via a resistor
Debug port	NSD	I/O	This pin is to communicate with a debugger. It should be connected to VCC via a resistor of 1 to 4.7 kΩ
Main clock input	XIN	I	Input/output for the main clock oscillator. A crystal, or a ceramic resonator should be connected between pins XIN and XOUT. An external clock should be input at the XIN while leaving the XOUT open
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. A crystal oscillator should be connected between pins XCIN and XCOUT. An external clock should be input at the XCIN while leaving the XCOUT open
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	Output of the clock with the same frequency as low speed clocks, f8, or f32
External interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input for external interrupts
NMI input	P8_5/$\overline{\text{NMI}}$	I	Input for NMI
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7	I/O	I/O ports in CMOS. Each port can be programmed to input or output under the control of the direction register. Pull-up resistors are selected for following 4-pin units, but are enabled only for the input pins: Pi_0 to Pi_3 and Pi_4 to Pi_7 (i = 0 to 10)
Input port	P9_1	I	Input port in CMOS. Pull-up resistors are selectable for P9_1 and P9_3
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
Timer B	TB0IN to TB5IN	I	Timers B0 to B5 input

Table 1.12 Pin Definitions and Functions (2/3)

Function	Symbol	I/O	Description
Three-phase motor control timer output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	Three-phase motor control timer output
Serial interface	$\overline{CTS0}$ to $\overline{CTS4}$	I	Handshake input
	$\overline{RTS0}$ to $\overline{RTS4}$	O	Handshake output
	CLK0 to CLK4	I/O	Transmit/receive clock input/output
	RXD0 to RXD4	I	Serial data input
	TXD0 to TXD4	O	Serial data output
I^2C-bus (simplified)	SDA0 to SDA2	I/O	Serial data input/output
	SCL0 to SCL2	I/O	Transmit/receive clock input/output
Serial interface special functions	STXD0 to STXD2	O	Serial data output in slave mode
	SRXD0 to SRXD2	I	Serial data input in slave mode
	$\overline{SS0}$ to $\overline{SS2}$	I	Input to control serial interface special functions
A/D converter	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7	I	Analog input for the A/D converter
	$\overline{ADTRG}$	I	External trigger input for the A/D converter
	ANEX0	I/O	Expanded analog input for the A/D converter and output in external op-amp connection mode
	ANEX1	I	Expanded analog input for the A/D converter
D/A converter	DA0, DA1	O	Output for the D/A converter
Reference voltage input	VREF	I	Reference voltage input for the A/D converter and D/A converter
Intelligent I/O	IIO0_0 to IIO0_7	I/O	Input/output for the Intelligent I/O group 0. Either input capture or output compare is selectable
	IIO1_0 to IIO1_7	I/O	Input/output for the Intelligent I/O group 1. Either input capture or output compare is selectable
	UD0A, UD0B, UD1A, UD1B	I	Input for the two-phase encoder
Serial bus interface	SSO0, SSO1	I/O	Serial data output. Functions as serial data input/output in 4-wire serial bus mode
	SSI0, SSI1	I/O	Serial data input. Functions as serial data input/output in 4-wire serial bus mode
	SSCK0, SSCK1	I/O	Transmit/receive clock input/output
	$\overline{SCS0}$, $\overline{SCS1}$	I/O	Input/output to control the synchronous serial interface
LIN module	LIN0OUT, LIN1OUT	O	Transmit data output for the LIN communications
	LIN0IN, LIN1IN	I	Receive data input for the LIN communications

Table 1.13 Pin Definitions and Functions (3/3)

Function	Symbol	I/O	Description
CAN module for the R32C/142 Group	CAN2IN, CAN3IN, CAN5IN	I	Receive data input for the CAN communications
	CAN2OUT, CAN3OUT, CAN5OUT	O	Transmit data output for the CAN communications
	$\overline{\text{CAN2WU}}$, $\overline{\text{CAN3WU}}$, $\overline{\text{CAN5WU}}$	I	Input for the CAN wake-up interrupt
CAN module for the R32C/145 Group	CAN0IN to CAN5IN	I	Receive data input for the CAN communications
	CAN0OUT to CAN5OUT	O	Transmit data output for the CAN communications
	$\overline{\text{CAN0WU}}$ to $\overline{\text{CAN5WU}}$	I	Input for the CAN wake-up interrupt

2. Central Processing Unit (CPU)

The CPU contains the registers shown below. There are two register banks each consisting of registers R2R0, R3R1, R6R4, R7R5, A0 to A3, SB, and FB.

Figure 2.1 CPU Registers

2.1 General Purpose Registers

2.1.1 Data Registers (R2R0, R3R1, R6R4, and R7R5)

These 32-bit registers are primarily used for transfers and arithmetic/logic operations.
Each of the registers can be divided into upper and lower 16-bit registers, e.g. R2R0 can be divided into R2 and R0, R3R1 can be divided into R3 and R1, etc.
Moreover, data registers R2R0 and R3R1 can be divided into four 8-bit data registers: upper (R2H and R3H), mid-upper (R2L and R3L), mid-lower (R0H and R1H), and lower (R0L and R1L).

2.1.2 Address Registers (A0, A1, A2, and A3)

These 32-bit registers have functions similar to data registers. They are also used for address register indirect addressing and address register relative addressing.

2.1.3 Static Base Register (SB)

This 32-bit register is used for SB relative addressing.

2.1.4 Frame Base Register (FB)

This 32-bit register is used for FB relative addressing.

2.1.5 Program Counter (PC)

This 32-bit counter indicates the address of the instruction to be executed next.

2.1.6 Interrupt Vector Table Base Register (INTB)

This 32-bit register indicates the start address of a relocatable vector table.

2.1.7 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Two types of 32-bit stack pointers (SPs) are provided: user stack pointer (USP) and interrupt stack pointer (ISP).
Use the stack pointer select flag (U flag) to select either the user stack pointer (USP) or the interrupt stack pointer (ISP). The U flag is bit 7 in the flag register (FLG). Refer to 2.1.8 “Flag Register (FLG)” for details.
To minimize the overhead of interrupt sequence due to less memory access, set the user stack pointer (USP) or the interrupt stack pointer (ISP) to a multiple of 4.

2.1.8 Flag Register (FLG)

This 32-bit register indicates the CPU status.

2.1.8.1 Carry Flag (C flag)

This flag retains a carry, borrow, or shifted-out bit generated by the arithmetic logic unit (ALU).

2.1.8.2 Debug Flag (D flag)

This flag is only for debugging. Only set this bit to 0.

2.1.8.3 Zero Flag (Z flag)

This flag becomes 1 when the result of an operation is 0; otherwise it is 0.

2.1.8.4 Sign Flag (S flag)

This flag becomes 1 when the result of an operation is a negative value; otherwise it is 0.

2.1.8.5 Register Bank Select Flag (B flag)

This flag selects a register bank. It indicates 0 when register bank 0 is selected, and 1 when register bank 1 is selected.

2.1.8.6 Overflow Flag (O flag)

This flag becomes 1 when the result of an operation overflows; otherwise it is 0.

2.1.8.7 Interrupt Enable Flag (I flag)

This flag enables maskable interrupts. To disable maskable interrupts, set this flag to 0. To enable them, set this flag to 1. When an interrupt is accepted, the flag becomes 0.

2.1.8.8 Stack Pointer Select Flag (U flag)

To select the interrupt stack pointer (ISP), set this flag to 0. To select the user stack pointer (USP), set this flag to 1.
It becomes 0 when a hardware interrupt is accepted or when an INT instruction designated by a software interrupt number from 0 to 127 is executed.

2.1.8.9 Floating-point Underflow Flag (FU flag)

This flag becomes 1 when an underflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.10 Floating-point Overflow Flag (FO flag)

This flag becomes 1 when an overflow occurs in a floating-point operation; otherwise it is 0. It also becomes 1 when the operand contains invalid numbers (subnormal numbers).

2.1.8.11 Processor Interrupt Priority Level (IPL)

The processor interrupt priority level (IPL), consisting of 3 bits, selects a processor interrupt priority level from level 0 to 7. An interrupt is enabled when the interrupt request level is higher than the selected IPL.
When the processor interrupt priority level (IPL) is set to 111b (level 7), all interrupts are disabled.

2.1.8.12 Fixed-point Radix Point Designation Bit (DP bit)

This bit designates the radix point. It also specifies which portion of the fixed-point multiplication result to extract. It is used for the MULX instruction.

2.1.8.13 Floating-point Rounding Mode (RND)

The 2-bit floating-point rounding mode selects a rounding mode for floating-point calculation results.

2.1.8.14 Reserved

Only set this bit to 0. The read value is undefined.

2.2 Fast Interrupt Registers

The following three registers are provided to minimize the overhead of the interrupt sequence.

2.2.1 Save Flag Register (SVF)

This 32-bit register is used to save the flag register when a fast interrupt is generated.

2.2.2 Save PC Register (SVP)

This 32-bit register is used to save the program counter when a fast interrupt is generated.

2.2.3 Vector Register (VCT)

This 32-bit register is used to indicate a jump address when a fast interrupt is generated.

2.3 DMAC-associated Registers

There are seven types of DMAC-associated registers.

2.3.1 DMA Mode Registers (DMD0, DMD1, DMD2, and DMD3)

These 32-bit registers are used to set DMA transfer mode, bit rate, etc.

2.3.2 DMA Terminal Count Registers (DCT0, DCT1, DCT2, and DCT3)

These 24-bit registers are used to set the number of DMA transfers.

2.3.3 DMA Terminal Count Reload Registers (DCR0, DCR1, DCR2, and DCR3)

These 24-bit registers are used to set the reloaded values for DMA terminal count registers.

2.3.4 DMA Source Address Registers (DSA0, DSA1, DSA2, and DSA3)

These 32-bit registers are used to set DMA source addresses.

2.3.5 DMA Source Address Reload Registers (DSR0, DSR1, DSR2, and DSR3)

These 32-bit registers are used to set the reloaded values for DMA source address registers.

2.3.6 DMA Destination Address Registers (DDA0, DDA1, DDA2, and DDA3)

These 32-bit registers are used to set DMA destination addresses.

2.3.7 DMA Destination Address Reload Registers (DDR0, DDR1, DDR2, and DDR3)

These 32-bit registers are used to set reloaded values for DMA destination address registers.

3. Memory

Figure 3.1 shows the memory map of the R32C/142 Group and R32C/145 Group.
The R32C/142 Group and R32C/145 Group provide a 4-Gbyte address space from 00000000h to FFFFFFFFh.

The internal ROM is mapped from address FFFFFFFFh in the inferior direction. For example, the 512-Kbyte internal ROM is mapped from FFF80000h to FFFFFFFFh.
The fixed interrupt vector table contains the start address of interrupt handlers and is mapped from FFFFFFDCh to FFFFFFFFh.
The internal RAM is mapped from address 00000400h in the superior direction. For example, the 32-Kbyte internal RAM is mapped from 00000400h to 000083FFh. Besides being used for data storage, the internal RAM functions as a stack(s) for subroutine calls and/or interrupt handlers.

Special function registers (SFRs), which are control registers for peripheral functions, are mapped from 00000000h to 000003FFh, and from 00040000h to 0004FFFFh. Unoccupied SFR locations are reserved, and no access is allowed.

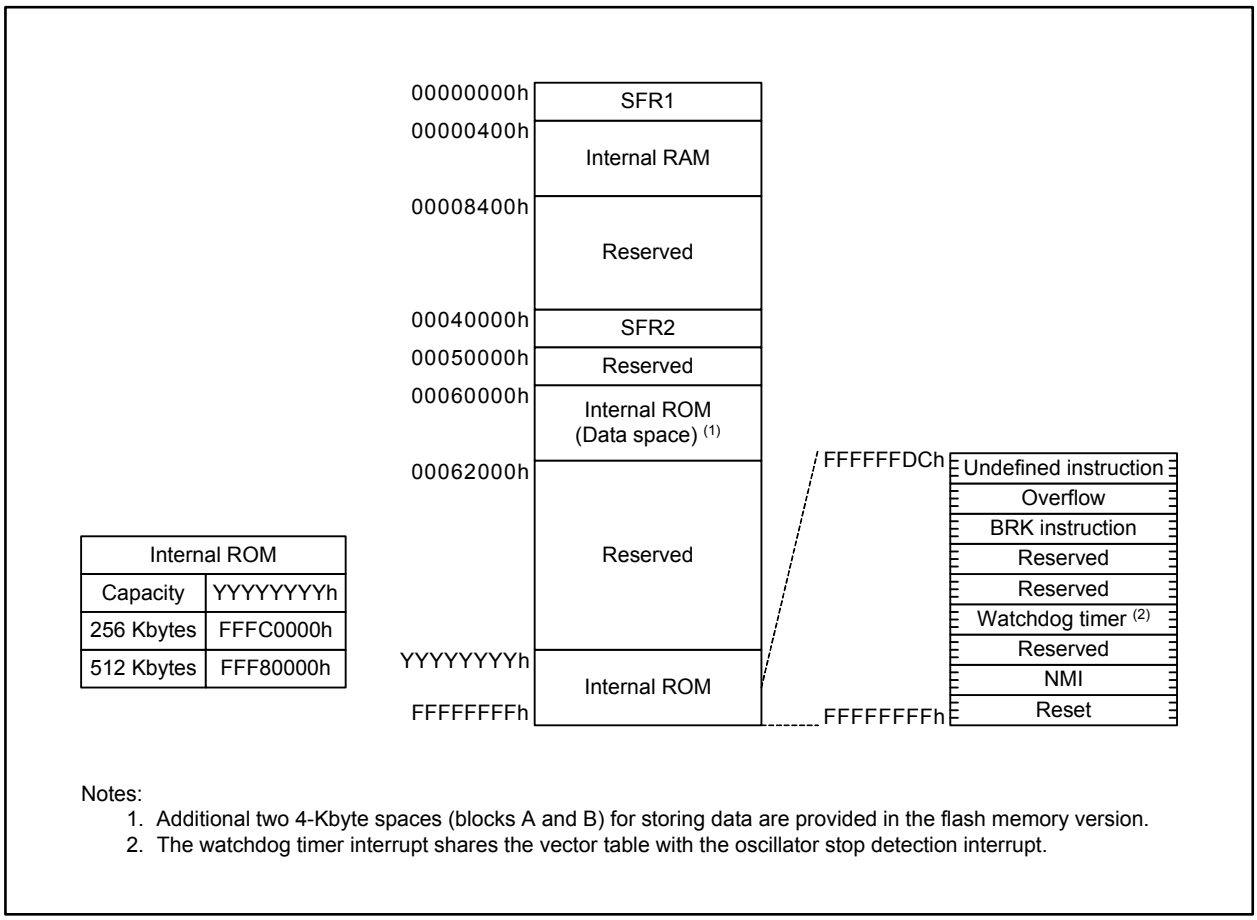


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

SFRs are memory-mapped peripheral registers that control the operation of peripherals. There are no SFRs associated with channels CAN0, CAN1, and CAN4 in the R32C/142 Group.
Table 4.1 SFR List (1) to Table 4.75 SFR List (75) list the SFR details.

Table 4.1 SFR List (1)

Address	Register	Symbol	Reset Value
000000h			
000001h			
000002h			
000003h			
000004h	Clock Control Register	CCR	0001 1000b
000005h			
000006h	Flash Memory Control Register	FMCR	0000 0001b
000007h	Protect Release Register	PRR	00h
000008h			
000009h			
00000Ah			
00000Bh			
00000Ch			
00000Dh			
00000Eh			
00000Fh			
000010h			
000011h			
000012h			
000013h			
000014h			
000015h			
000016h			
000017h			
000018h			
000019h			
00001Ah			
00001Bh			
00001Ch	Flash Memory Rewrite Bus Control Register	FEBC	0000h
00001Dh			
00001Eh	Peripheral Bus Control Register	PBC	0504h
00001Fh			
000020h to 00005Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.2 SFR List (2)

Address	Register	Symbol	Reset Value
000060h			
000061h	Timer B5 Interrupt Control Register	TB5IC	XXXX X000b
000062h			
000063h	UART2 Receive/ACK Interrupt Control Register	S2RIC	XXXX X000b
000064h			
000065h			
000066h			
000067h			
000068h	DMA0 Transfer Complete Interrupt Control Register	DM0IC	XXXX X000b
000069h	UART0 Start Condition/Stop Condition Detection Interrupt Control Register	BCN0IC	XXXX X000b
00006Ah	DMA2 Transfer Complete Interrupt Control Register	DM2IC	XXXX X000b
00006Bh	A/D Converter 0 Convert Completion Interrupt Control Register	AD0IC	XXXX X000b
00006Ch	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
00006Dh	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000b
00006Eh	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
00006Fh	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000b
000070h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
000071h	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000b
000072h	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000b
000073h	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X000b
000074h	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000b
000075h	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X000b
000076h	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
000077h	Intelligent I/O Interrupt Control Register 10	IIO10IC	XXXX X000b
000078h	Timer B3 Interrupt Control Register	TB3IC	XXXX X000b
000079h	CAN4 Wake-up Interrupt Control Register (1)	C4WIC	XXXX X000b
00007Ah	INT5 Interrupt Control Register	INT5IC	XX00 X000b
00007Bh	CAN0 Wake-up Interrupt Control Register (1)	C0WIC	XXXX X000b
00007Ch	INT3 Interrupt Control Register	INT3IC	XX00 X000b
00007Dh	CAN2 Wake-up Interrupt Control Register	C2WIC	XXXX X000b
00007Eh	INT1 Interrupt Control Register	INT1IC	XX00 X000b
00007Fh	LIN Low Detection Interrupt Control Register	LLDIC	XXXX X000b
000080h			
000081h	UART2 Transmit/NACK Interrupt Control Register	S2TIC	XXXX X000b
000082h			
000083h			
000084h			
000085h			
000086h			
000087h	UART2 Start Condition/Stop Condition Detection Interrupt Control Register	BCN2IC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. Channels CAN0 and CAN4 are not available in the R32C/142 Group.

Table 4.3 SFR List (3)

Address	Register	Symbol	Reset Value
000088h	DMA1 Transfer Complete Interrupt Control Register	DM1IC	XXXX X000b
000089h	UART1 Start Condition/Stop Condition Detection Interrupt Control Register	BCN1IC	XXXX X000b
00008Ah	DMA3 Transfer Complete Interrupt Control Register	DM3IC	XXXX X000b
00008Bh	Key Input Interrupt Control Register	KUPIC	XXXX X000b
00008Ch	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
00008Dh	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000b
00008Eh	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
00008Fh	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000b
000090h	UART0 Transmit/NACK Interrupt Control Register	S0TIC	XXXX X000b
000091h	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000b
000092h	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000b
000093h	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000b
000094h	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
000095h	Intelligent I/O Interrupt Control Register 9	IIO9IC	XXXX X000b
000096h	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
000097h	Intelligent I/O Interrupt Control Register 11	IIO11IC	XXXX X000b
000098h	Timer B4 Interrupt Control Register	TB4IC	XXXX X000b
000099h	CAN5 Wake-up Interrupt Control Register	C5WIC	XXXX X000b
00009Ah	INT4 Interrupt Control Register	INT4IC	XX00 X000b
00009Bh	CAN1 Wake-up Interrupt Control Register (1)	C1WIC	XXXX X000b
00009Ch	INT2 Interrupt Control Register	INT2IC	XX00 X000b
00009Dh	CAN3 Wake-up Interrupt Control Register	C3WIC	XXXX X000b
00009Eh	INT0 Interrupt Control Register	INT0IC	XX00 X000b
00009Fh			
0000A0h	Intelligent I/O Interrupt Request Register 0	IIO0IR	0000 0XX1b
0000A1h	Intelligent I/O Interrupt Request Register 1	IIO1IR	0000 0XX1b
0000A2h	Intelligent I/O Interrupt Request Register 2	IIO2IR	0000 0X01b
0000A3h	Intelligent I/O Interrupt Request Register 3	IIO3IR	0000 0XX1b
0000A4h	Intelligent I/O Interrupt Request Register 4	IIO4IR	000X 0XX1b
0000A5h	Intelligent I/O Interrupt Request Register 5	IIO5IR	0000 00X1b
0000A6h	Intelligent I/O Interrupt Request Register 6	IIO6IR	0000 00X1b
0000A7h	Intelligent I/O Interrupt Request Register 7	IIO7IR	000X 00X1b
0000A8h	Intelligent I/O Interrupt Request Register 8	IIO8IR	0000 00X1b
0000A9h	Intelligent I/O Interrupt Request Register 9	IIO9IR	0000 00X1b
0000AAh	Intelligent I/O Interrupt Request Register 10	IIO10IR	0000 00X1b
0000ABh	Intelligent I/O Interrupt Request Register 11	IIO11IR	0000 00X1b
0000ACh			
0000ADh			
0000AEh			
0000AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. Channel CAN1 is not available in the R32C/142 Group.

Table 4.4 SFR List (4)

Address	Register	Symbol	Reset Value
0000B0h	Intelligent I/O Interrupt Enable Register 0	IIO0IE	00h
0000B1h	Intelligent I/O Interrupt Enable Register 1	IIO1IE	00h
0000B2h	Intelligent I/O Interrupt Enable Register 2	IIO2IE	00h
0000B3h	Intelligent I/O Interrupt Enable Register 3	IIO3IE	00h
0000B4h	Intelligent I/O Interrupt Enable Register 4	IIO4IE	00h
0000B5h	Intelligent I/O Interrupt Enable Register 5	IIO5IE	00h
0000B6h	Intelligent I/O Interrupt Enable Register 6	IIO6IE	00h
0000B7h	Intelligent I/O Interrupt Enable Register 7	IIO7IE	00h
0000B8h	Intelligent I/O Interrupt Enable Register 8	IIO8IE	00h
0000B9h	Intelligent I/O Interrupt Enable Register 9	IIO9IE	00h
0000BAh	Intelligent I/O Interrupt Enable Register 10	IIO10IE	00h
0000BBh	Intelligent I/O Interrupt Enable Register 11	IIO11IE	00h
0000BCh			
0000BDh			
0000BEh			
0000BFh			
0000C0h	Serial Bus Interface 0 Interrupt Control Register	SS0IC	XXXX X000b
0000C1h	CAN0 Transmit Interrupt Control Register (1)	C0TIC	XXXX X000b
0000C2h			
0000C3h	CAN0 Error Interrupt Control Register (1)	C0EIC	XXXX X000b
0000C4h			
0000C5h	CAN1 Receive Interrupt Control Register (1)	C1RIC	XXXX X000b
0000C6h			
0000C7h	CAN2 Transmit Interrupt Control Register	C2TIC	
0000C8h	CAN4 Transmit FIFO Interrupt Control Register (1)	C4FTIC	XXXX X000b
0000C9h	CAN2 Error Interrupt Control Register	C2EIC	XXXX X000b
0000CAh	CAN5 Transmit FIFO Interrupt Control Register	C5FTIC	XXXX X000b
0000CBh	CAN3 Receive Interrupt Control Register	C3RIC	XXXX X000b
0000CCh			
0000CDh	CAN4 Transmit Interrupt Control Register (1)	C4TIC	XXXX X000b
0000CEh			
0000CFh	CAN4 Error Interrupt Control Register (1)	C4EIC	XXXX X000b
0000D0h	CAN0 Transmit FIFO Interrupt Control Register (1)	C0FTIC	XXXX X000b
0000D1h	CAN5 Receive Interrupt Control Register	C5RIC	XXXX X000b
0000D2h	CAN1 Transmit FIFO Interrupt Control Register (1)	C1FTIC	XXXX X000b
0000D3h			
0000D4h	CAN2 Transmit FIFO Interrupt Control Register	C2FTIC	XXXX X000b
0000D5h	LIN0 Interrupt Control Register	L0IC	XXXX X000b
0000D6h	CAN3 Transmit FIFO Interrupt Control Register	C3FTIC	XXXX X000b
0000D7h			
0000D8h			
0000D9h			
0000DAh			
0000DBh			
0000DCh			
0000DDh	UART3 Transmit Interrupt Control Register	S3TIC	XXXX X000b
0000DEh			
0000DFh	UART4 Transmit Interrupt Control Register	S4TIC	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. Channels CAN0, CAN1, and CAN4 are not available in the R32C/142 Group.

Table 4.5 SFR List (5)

Address	Register	Symbol	Reset Value
0000E0h	Serial Bus Interface 1 Interrupt Control Register	SS1IC	XXXX X000b
0000E1h	CAN0 Receive Interrupt Control Register (1)	C0RIC	XXXX X000b
0000E2h			
0000E3h	CAN1 Transmit Interrupt Control Register (1)	C1TIC	XXXX X000b
0000E4h			
0000E5h	CAN1 Error Interrupt Control Register (1)	C1EIC	XXXX X000b
0000E6h			
0000E7h	CAN2 Receive Interrupt Control Register	C2RIC	XXXX X000b
0000E8h	CAN4 Receive FIFO/Gateway Channel 4 Interrupt Control Register (1)	C4FRIC/GW4IC	XXXX X000b
0000E9h	CAN3 Transmit Interrupt Control Register	C3TIC	XXXX X000b
0000EAh	CAN5 Receive FIFO/Gateway Channel 5 Interrupt Control Register	C5FRIC/GW5IC	XXXX X000b
0000EBh	CAN3 Error Interrupt Control Register	C3EIC	XXXX X000b
0000ECh			
0000EDh	CAN4 Receive Interrupt Control Register (1)	C4RIC	XXXX X000b
0000EEh			
0000EFh	CAN5 Transmit Interrupt Control Register	C5TIC	XXXX X000b
0000F0h	CAN0 Receive FIFO/Gateway Channel 0 Interrupt Control Register (1)	C0FRIC/GW0IC	XXXX X000b
0000F1h	CAN5 Error Interrupt Control Register	C5EIC	XXXX X000b
0000F2h	CAN1 Receive FIFO/Gateway Channel 1 Interrupt Control Register (1)	C1FRIC/GW1IC	XXXX X000b
0000F3h			
0000F4h	CAN2 Receive FIFO/Gateway Channel 2 Interrupt Control Register	C2FRIC/GW2IC	XXXX X000b
0000F5h	LIN1 Interrupt Control Register	L1IC	XXXX X000b
0000F6h	CAN3 Receive FIFO/Gateway Channel 3 Interrupt Control Register	C3FRIC/GW3IC	XXXX X000b
0000F7h			
0000F8h	Gateway Error Interrupt Control Register	GWEIC	XXXX X000b
0000F9h			
0000FAh			
0000FBh			
0000FCh			
0000FDh	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0000FEh			
0000FFh	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
000100h	Group 1 Time Measurement/Waveform Generation Register 0	G1TM0/G1PO0	XXXXh
000101h			
000102h	Group 1 Time Measurement/Waveform Generation Register 1	G1TM1/G1PO1	XXXXh
000103h			
000104h	Group 1 Time Measurement/Waveform Generation Register 2	G1TM2/G1PO2	XXXXh
000105h			
000106h	Group 1 Time Measurement/Waveform Generation Register 3	G1TM3/G1PO3	XXXXh
000107h			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. Channels CAN0, CAN1, and CAN4 are not available in the R32C/142 Group.

Table 4.6 SFR List (6)

Address	Register	Symbol	Reset Value
000108h	Group 1 Time Measurement/Waveform Generation Register 4	G1TM4/G1PO4	XXXXh
000109h			
00010Ah	Group 1 Time Measurement/Waveform Generation Register 5	G1TM5/G1PO5	XXXXh
00010Bh			
00010Ch	Group 1 Time Measurement/Waveform Generation Register 6	G1TM6/G1PO6	XXXXh
00010Dh			
00010Eh	Group 1 Time Measurement/Waveform Generation Register 7	G1TM7/G1PO7	XXXXh
00010Fh			
000110h	Group 1 Waveform Generation Control Register 0	G1POCR0	0000 X000b
000111h	Group 1 Waveform Generation Control Register 1	G1POCR1	0X00 X000b
000112h	Group 1 Waveform Generation Control Register 2	G1POCR2	0X00 X000b
000113h	Group 1 Waveform Generation Control Register 3	G1POCR3	0X00 X000b
000114h	Group 1 Waveform Generation Control Register 4	G1POCR4	0X00 X000b
000115h	Group 1 Waveform Generation Control Register 5	G1POCR5	0X00 X000b
000116h	Group 1 Waveform Generation Control Register 6	G1POCR6	0X00 X000b
000117h	Group 1 Waveform Generation Control Register 7	G1POCR7	0X00 X000b
000118h	Group 1 Time Measurement Control Register 0	G1TMCR0	00h
000119h	Group 1 Time Measurement Control Register 1	G1TMCR1	00h
00011Ah	Group 1 Time Measurement Control Register 2	G1TMCR2	00h
00011Bh	Group 1 Time Measurement Control Register 3	G1TMCR3	00h
00011Ch	Group 1 Time Measurement Control Register 4	G1TMCR4	00h
00011Dh	Group 1 Time Measurement Control Register 5	G1TMCR5	00h
00011Eh	Group 1 Time Measurement Control Register 6	G1TMCR6	00h
00011Fh	Group 1 Time Measurement Control Register 7	G1TMCR7	00h
000120h	Group 1 Base Timer Register	G1BT	XXXXh
000121h			
000122h	Group 1 Base Timer Control Register 0	G1BCR0	0000 0000b
000123h	Group 1 Base Timer Control Register 1	G1BCR1	0000 0000b
000124h	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00h
000125h	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00h
000126h	Group 1 Function Enable Register	G1FE	00h
000127h	Group 1 Function Select Register	G1FS	00h
000128h			
000129h			
00012Ah			
00012Bh			
00012Ch			
00012Dh			
00012Eh			
00012Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.7 SFR List (7)

Address	Register	Symbol	Reset Value
000130h to 00016Fh			
000170h			
000171h			
000172h			
000173h			
000174h			
000175h			
000176h			
000177h			
000178h			
000179h			
00017Ah			
00017Bh			
00017Ch			
00017Dh			
00017Eh			
00017Fh			
000180h	Group 0 Time Measurement/Waveform Generation Register 0	G0TM0/G0PO0	XXXXh
000181h			
000182h	Group 0 Time Measurement/Waveform Generation Register 1	G0TM1/G0PO1	XXXXh
000183h			
000184h	Group 0 Time Measurement/Waveform Generation Register 2	G0TM2/G0PO2	XXXXh
000185h			
000186h	Group 0 Time Measurement/Waveform Generation Register 3	G0TM3/G0PO3	XXXXh
000187h			
000188h	Group 0 Time Measurement/Waveform Generation Register 4	G0TM4/G0PO4	XXXXh
000189h			
00018Ah	Group 0 Time Measurement/Waveform Generation Register 5	G0TM5/G0PO5	XXXXh
00018Bh			
00018Ch	Group 0 Time Measurement/Waveform Generation Register 6	G0TM6/G0PO6	XXXXh
00018Dh			
00018Eh	Group 0 Time Measurement/Waveform Generation Register 7	G0TM7/G0PO7	XXXXh
00018Fh			
000190h	Group 0 Waveform Generation Control Register 0	G0POCR0	0000 X000b
000191h	Group 0 Waveform Generation Control Register 1	G0POCR1	0X00 X000b
000192h	Group 0 Waveform Generation Control Register 2	G0POCR2	0X00 X000b
000193h	Group 0 Waveform Generation Control Register 3	G0POCR3	0X00 X000b
000194h	Group 0 Waveform Generation Control Register 4	G0POCR4	0X00 X000b
000195h	Group 0 Waveform Generation Control Register 5	G0POCR5	0X00 X000b
000196h	Group 0 Waveform Generation Control Register 6	G0POCR6	0X00 X000b
000197h	Group 0 Waveform Generation Control Register 7	G0POCR7	0X00 X000b
000198h	Group 0 Time Measurement Control Register 0	G0TMCR0	00h
000199h	Group 0 Time Measurement Control Register 1	G0TMCR1	00h
00019Ah	Group 0 Time Measurement Control Register 2	G0TMCR2	00h
00019Bh	Group 0 Time Measurement Control Register 3	G0TMCR3	00h
00019Ch	Group 0 Time Measurement Control Register 4	G0TMCR4	00h
00019Dh	Group 0 Time Measurement Control Register 5	G0TMCR5	00h
00019Eh	Group 0 Time Measurement Control Register 6	G0TMCR6	00h
00019Fh	Group 0 Time Measurement Control Register 7	G0TMCR7	00h

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.8 SFR List (8)

Address	Register	Symbol	Reset Value
0001A0h	Group 0 Base Timer Register	G0BT	XXXXh
0001A1h			
0001A2h	Group 0 Base Timer Control Register 0	G0BCR0	0000 0000b
0001A3h	Group 0 Base Timer Control Register 1	G0BCR1	0000 0000b
0001A4h	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00h
0001A5h	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00h
0001A6h	Group 0 Function Enable Register	G0FE	00h
0001A7h	Group 0 Function Select Register	G0FS	00h
0001A8h			
0001A9h			
0001AAh			
0001ABh			
0001ACh			
0001ADh			
0001AEh			
0001AFh			
0001B0h			
0001B1h			
0001B2h			
0001B3h			
0001B4h			
0001B5h			
0001B6h			
0001B7h			
0001B8h			
0001B9h			
0001BAh			
0001BBh			
0001BCh			
0001BDh			
0001BEh			
0001BFh			
0001C0h			
0001C1h			
0001C2h			
0001C3h			
0001C4h			
0001C5h			
0001C6h			
0001C7h			
0001C8h			
0001C9h			
0001CAh			
0001CBh			
0001CCh			
0001CDh			
0001CEh			
0001CFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.9 SFR List (9)

Address	Register	Symbol	Reset Value
0001D0h			
0001D1h			
0001D2h			
0001D3h			
0001D4h			
0001D5h			
0001D6h			
0001D7h			
0001D8h			
0001D9h			
0001DAh			
0001DBh			
0001DCh			
0001DDh			
0001DEh			
0001DFh			
0001E0h	UART3 Transmit/Receive Mode Register	U3MR	00h
0001E1h	UART3 Bit Rate Register	U3BRG	XXh
0001E2h	UART3 Transmit Buffer Register	U3TB	XXXXh
0001E3h			
0001E4h	UART3 Transmit/Receive Control Register 0	U3C0	00X0 1000b
0001E5h	UART3 Transmit/Receive Control Register 1	U3C1	XXXX 0010b
0001E6h	UART3 Receive Buffer Register	U3RB	XXXXh
0001E7h			
0001E8h	UART4 Transmit/Receive Mode Register	U4MR	00h
0001E9h	UART4 Bit Rate Register	U4BRG	XXh
0001EAh	UART4 Transmit Buffer Register	U4TB	XXXXh
0001EBh			
0001ECh	UART4 Transmit/Receive Control Register 0	U4C0	00X0 1000b
0001EDh	UART4 Transmit/Receive Control Register 1	U4C1	XXXX 0010b
0001EEh	UART4 Receive Buffer Register	U4RB	XXXXh
0001EFh			
0001F0h	UART3, UART4 Transmit/Receive Control Register 2	U34CON	X000 0000b
0001F1h			
0001F2h			
0001F3h			
0001F4h			
0001F5h			
0001F6h			
0001F7h			
0001F8h			
0001F9h			
0001FAh			
0001FBh			
0001FCh			
0001FDh			
0001FEh			
0001FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.10 SFR List (10)

Address	Register	Symbol	Reset Value
000200h	Group0 Phase Shift Waveform Output Mode Clock Division Setting Register	G0SDR	00h
000201h	Group0 Phase Shift Waveform Output Mode Control Register	G0PSCR	00h
000202h	Group1 Phase Shift Waveform Output Mode Clock Division Setting Register	G1SDR	00h
000203h	Group1 Phase Shift Waveform Output Mode Control Register	G1PSCR	00h
000204h			
000205h			
000206h			
000207h			
000208h	Timer B Event Clock Select Register	TBECKS	0000 0000b
000209h			
00020Ah			
00020Bh			
00020Ch			
00020Dh			
00020Eh			
00020Fh			
000210h	IIO0_7 Digital Debounce Register	IC07DDR	FFh
000211h	IIO1_7 Digital Debounce Register	IC17DDR	FFh
000212h			
000213h			
000214h			
000215h			
000216h			
000217h			
000218h			
000219h			
00021Ah			
00021Bh			
00021Ch			
00021Dh			
00021Eh			
00021Fh			
000220h	Timer A1 Mirror Register	TA1M	XXXXh
000221h			
000222h	Timer A1-1 Mirror Register	TA11M	XXXXh
000223h			
000224h	Timer A2 Mirror Register	TA2M	XXXXh
000225h			
000226h	Timer A2-1 Mirror Register	TA21M	XXXXh
000227h			
000228h	Timer A4 Mirror Register	TA4M	XXXXh
000229h			
00022Ah	Timer A4-1 Mirror Register	TA41M	XXXXh
00022Bh			
00022Ch			
00022Dh			
00022Eh			
00022Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.11 SFR List (11)

Address	Register	Symbol	Reset Value
000230h to 0002BFh			
0002C0h	X0 Register/Y0 Register	X0R/Y0R	XXXXh
0002C1h			
0002C2h	X1 Register/Y1 Register	X1R/Y1R	XXXXh
0002C3h			
0002C4h	X2 Register/Y2 Register	X2R/Y2R	XXXXh
0002C5h			
0002C6h	X3 Register/Y3 Register	X3R/Y3R	XXXXh
0002C7h			
0002C8h	X4 Register/Y4 Register	X4R/Y4R	XXXXh
0002C9h			
0002CAh	X5 Register/Y5 Register	X5R/Y5R	XXXXh
0002CBh			
0002CCh	X6 Register/Y6 Register	X6R/Y6R	XXXXh
0002CDh			
0002CEh	X7 Register/Y7 Register	X7R/Y7R	XXXXh
0002CFh			
0002D0h	X8 Register/Y8 Register	X8R/Y8R	XXXXh
0002D1h			
0002D2h	X9 Register/Y9 Register	X9R/Y9R	XXXXh
0002D3h			
0002D4h	X10 Register/Y10 Register	X10R/Y10R	XXXXh
0002D5h			
0002D6h	X11 Register/Y11 Register	X11R/Y11R	XXXXh
0002D7h			
0002D8h	X12 Register/Y12 Register	X12R/Y12R	XXXXh
0002D9h			
0002DAh	X13 Register/Y13 Register	X13R/Y13R	XXXXh
0002DBh			
0002DCh	X14 Register/Y14 Register	X14R/Y14R	XXXXh
0002DDh			
0002DEh	X15 Register/Y15 Register	X15R/Y15R	XXXXh
0002DFh			
0002E0h	X-Y Control Register	XYC	XXXX XX00b
0002E1h			
0002E2h			
0002E3h			
0002E4h	UART1 Special Mode Register 4	U1SMR4	00h
0002E5h	UART1 Special Mode Register 3	U1SMR3	00h
0002E6h	UART1 Special Mode Register 2	U1SMR2	00h
0002E7h	UART1 Special Mode Register	U1SMR	00h
0002E8h	UART1 Transmit/Receive Mode Register	U1MR	00h
0002E9h	UART1 Bit Rate Register	U1BRG	XXh
0002EAh	UART1 Transmit Buffer Register	U1TB	XXXXh
0002EBh			
0002ECh	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
0002EDh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
0002EEh	UART1 Receive Buffer Register	U1RB	XXXXh
0002EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.12 SFR List (12)

Address	Register	Symbol	Reset Value
0002F0h			
0002F1h			
0002F2h			
0002F3h			
0002F4h			
0002F5h			
0002F6h			
0002F7h			
0002F8h			
0002F9h			
0002FAh			
0002FBh			
0002FCh			
0002FDh			
0002FEh			
0002FFh			
000300h	Count Start Register for Timers B3, B4, and B5	TBSR	000X XXXXb
000301h			
000302h	Timer A1-1 Register	TA11	XXXXh
000303h			
000304h	Timer A2-1 Register	TA21	XXXXh
000305h			
000306h	Timer A4-1 Register	TA41	XXXXh
000307h			
000308h	Three-phase PWM Control Register 0	INVC0	00h
000309h	Three-phase PWM Control Register 1	INVC1	00h
00030Ah	Three-phase Output Buffer Register 0	IDB0	XX11 1111b
00030Bh	Three-phase Output Buffer Register 1	IDB1	XX11 1111b
00030Ch	Dead Time Timer	DTT	XXh
00030Dh	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XXh
00030Eh			
00030Fh			
000310h	Timer B3 Register	TB3	XXXXh
000311h			
000312h	Timer B4 Register	TB4	XXXXh
000313h			
000314h	Timer B5 Register	TB5	XXXXh
000315h			
000316h			
000317h			
000318h			
000319h			
00031Ah			
00031Bh	Timer B3 Mode Register	TB3MR	00XX 0000b
00031Ch	Timer B4 Mode Register	TB4MR	00XX 0000b
00031Dh	Timer B5 Mode Register	TB5MR	00XX 0000b
00031Eh			
00031Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.13 SFR List (13)

Address	Register	Symbol	Reset Value
000320h			
000321h			
000322h			
000323h			
000324h			
000325h			
000326h			
000327h			
000328h			
000329h			
00032Ah			
00032Bh			
00032Ch			
00032Dh			
00032Eh			
00032Fh			
000330h			
000331h			
000332h			
000333h			
000334h	UART2 Special Mode Register 4	U2SMR4	00h
000335h	UART2 Special Mode Register 3	U2SMR3	00h
000336h	UART2 Special Mode Register 2	U2SMR2	00h
000337h	UART2 Special Mode Register	U2SMR	00h
000338h	UART2 Transmit/Receive Mode Register	U2MR	00h
000339h	UART2 Bit Rate Register	U2BRG	XXh
00033Ah	UART2 Transmit Buffer Register	U2TB	XXXXh
00033Bh			
00033Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
00033Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
00033Eh	UART2 Receive Buffer Register	U2RB	XXXXh
00033Fh			
000340h	Count Start Register	TABSR	0000 0000b
000341h	Clock Prescaler Reset Register	CPSRF	0XXX XXXXb
000342h	One-shot Start Register	ONSF	0000 0000b
000343h	Trigger Select Register	TRGSR	0000 0000b
000344h	Increment/Decrement Select Register	UDF	0000 0000b
000345h			
000346h	Timer A0 Register	TA0	XXXXh
000347h			
000348h	Timer A1 Register	TA1	XXXXh
000349h			
00034Ah	Timer A2 Register	TA2	XXXXh
00034Bh			
00034Ch	Timer A3 Register	TA3	XXXXh
00034Dh			
00034Eh	Timer A4 Register	TA4	XXXXh
00034Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.14 SFR List (14)

Address	Register	Symbol	Reset Value
000350h	Timer B0 Register	TB0	XXXXh
000351h			
000352h	Timer B1 Register	TB1	XXXXh
000353h			
000354h	Timer B2 Register	TB2	XXXXh
000355h			
000356h	Timer A0 Mode Register	TA0MR	0000 0000b
000357h	Timer A1 Mode Register	TA1MR	0000 0000b
000358h	Timer A2 Mode Register	TA2MR	0000 0000b
000359h	Timer A3 Mode Register	TA3MR	0000 0000b
00035Ah	Timer A4 Mode Register	TA4MR	0000 0000b
00035Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
00035Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
00035Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
00035Eh	Timer B2 Special Mode Register	TB2SC	XXXX XXX0b
00035Fh	Count Source Prescaler Register	TCSPR	0000 0000b
000360h			
000361h			
000362h			
000363h			
000364h	UART0 Special Mode Register 4	U0SMR4	00h
000365h	UART0 Special Mode Register 3	U0SMR3	00h
000366h	UART0 Special Mode Register 2	U0SMR2	00h
000367h	UART0 Special Mode Register	U0SMR	00h
000368h	UART0 Transmit/Receive Mode Register	U0MR	00h
000369h	UART0 Bit Rate Register	U0BRG	XXh
00036Ah	UART0 Transmit Buffer Register	U0TB	XXXXh
00036Bh			
00036Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
00036Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
00036Eh	UART0 Receive Buffer Register	U0RB	XXXXh
00036Fh			
000370h			
000371h			
000372h			
000373h			
000374h			
000375h			
000376h			
000377h			
000378h			
000379h			
00037Ah			
00037Bh			
00037Ch	CRC Data Register	CRCD	XXXXh
00037Dh			
00037Eh	CRC Input Register	CRCIN	XXh
00037Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.15 SFR List (15)

Address	Register	Symbol	Reset Value
000380h	A/D0 Register 0	AD00	00XXh
000381h			
000382h	A/D0 Register 1	AD01	00XXh
000383h			
000384h	A/D0 Register 2	AD02	00XXh
000385h			
000386h	A/D0 Register 3	AD03	00XXh
000387h			
000388h	A/D0 Register 4	AD04	00XXh
000389h			
00038Ah	A/D0 Register 5	AD05	00XXh
00038Bh			
00038Ch	A/D0 Register 6	AD06	00XXh
00038Dh			
00038Eh	A/D0 Register 7	AD07	00XXh
00038Fh			
000390h			
000391h			
000392h	A/D0 Control Register 4	AD0CON4	XXXX 00XXb
000393h	A/D0 Control Register 5	AD0CON5	00h
000394h	A/D0 Control Register 2	AD0CON2	X00X X000b
000395h	A/D0 Control Register 3	AD0CON3	XXXX X000b
000396h	A/D0 Control Register 0	AD0CON0	00h
000397h	A/D0 Control Register 1	AD0CON1	00h
000398h	D/A Register 0	DA0	XXh
000399h			
00039Ah	D/A Register 1	DA1	XXh
00039Bh			
00039Ch	D/A Control Register	DACON	XXXX XX00b
00039Dh			
00039Eh			
00039Fh			
0003A0h			
0003A1h			
0003A2h			
0003A3h			
0003A4h			
0003A5h			
0003A6h			
0003A7h			
0003A8h			
0003A9h			
0003AAh			
0003ABh			
0003ACh			
0003ADh			
0003AEh			
0003AFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.16 SFR List (16)

Address	Register	Symbol	Reset Value
0003B0h			
0003B1h			
0003B2h			
0003B3h			
0003B4h			
0003B5h			
0003B6h			
0003B7h			
0003B8h			
0003B9h			
0003BAh			
0003BBh			
0003BCh			
0003BDh			
0003BEh			
0003BFh			
0003C0h	Port P0 Register	P0	XXh
0003C1h	Port P1 Register	P1	XXh
0003C2h	Port P0 Direction Register	PD0	0000 0000b
0003C3h	Port P1 Direction Register	PD1	0000 0000b
0003C4h	Port P2 Register	P2	XXh
0003C5h	Port P3 Register	P3	XXh
0003C6h	Port P2 Direction Register	PD2	0000 0000b
0003C7h	Port P3 Direction Register	PD3	0000 0000b
0003C8h	Port P4 Register	P4	XXh
0003C9h	Port P5 Register	P5	XXh
0003CAh	Port P4 Direction Register	PD4	0000 0000b
0003CBh	Port P5 Direction Register	PD5	0000 0000b
0003CCh	Port P6 Register	P6	XXh
0003CDh	Port P7 Register	P7	XXh
0003CEh	Port P6 Direction Register	PD6	0000 0000b
0003CFh	Port P7 Direction Register	PD7	0000 0000b
0003D0h	Port P8 Register	P8	XXh
0003D1h	Port P9 Register	P9	XXh
0003D2h	Port P8 Direction Register	PD8	00X0 0000b
0003D3h	Port P9 Direction Register	PD9	0000 0000b
0003D4h	Port P10 Register	P10	XXh
0003D5h			
0003D6h	Port P10 Direction Register	PD10	0000 0000b
0003D7h			
0003D8h			
0003D9h			
0003DAh			
0003DBh			
0003DCh			
0003DDh			
0003DEh			
0003DFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.17 SFR List (17)

Address	Register	Symbol	Reset Value
0003E0h			
0003E1h			
0003E2h			
0003E3h			
0003E4h			
0003E5h			
0003E6h			
0003E7h			
0003E8h			
0003E9h			
0003EAh			
0003EBh			
0003ECh			
0003EDh			
0003EEh			
0003EFh			
0003F0h	Pull-up Control Register 0	PUR0	0000 0000b
0003F1h	Pull-up Control Register 1	PUR1	XXXX 0000b
0003F2h	Pull-up Control Register 2	PUR2	0000 0000b
0003F3h	Pull-up Control Register 3	PUR3	XXXX XX00b
0003F4h			
0003F5h			
0003F6h			
0003F7h			
0003F8h			
0003F9h			
0003FAh			
0003FBh			
0003FCh			
0003FDh			
0003FEh			
0003FFh	Port Control Register	PCR	XXXX XXX0b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.18 SFR List (18)

Address	Register	Symbol	Reset Value
040000h	Flash Memory Control Register 0	FMR0	0X01 XX00b
040001h	Flash Memory Status Register 0	FMSR0	1000 0000b
040002h			
040003h			
040004h			
040005h			
040006h			
040007h			
040008h	Flash Register Protection Unlock Register 0	FPR0	00h
040009h	Flash Memory Control Register 1	FMR1	0000 0010b
04000Ah	Block Protect Bit Monitor Register 0	FBPM0	??X? ????b (1)
04000Bh	Block Protect Bit Monitor Register 1	FBPM1	XXX? ????b (1)
04000Ch			
04000Dh			
04000Eh			
04000Fh			
040010h			
040011h			
040012h			
040013h			
040014h			
040015h			
040016h			
040017h			
040018h			
040019h			
04001Ah			
04001Bh			
04001Ch			
04001Dh			
04001Eh			
04001Fh			
040020h	PLL Control Register 0	PLC0	0000 0001b
040021h	PLL Control Register 1	PLC1	0001 1111b
040022h			
040023h			
040024h			
040025h			
040026h			
040027h			
040028h			
040029h			
04002Ah			
04002Bh			
04002Ch			
04002Dh			
04002Eh			
04002Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. The reset value reflects the value of the protect bit for each block in the flash memory.

Table 4.19 SFR List (19)

Address	Register	Symbol	Reset Value
040030h to 04003Fh			
040040h			
040041h			
040042h			
040043h			
040044h	Processor Mode Register 0	PM0	1000 0000b
040045h			
040046h	System Clock Control Register 0	CM0	0000 1000b
040047h	System Clock Control Register 1	CM1	0010 0000b
040048h	Processor Mode Register 3	PM3	00h
040049h			
04004Ah	Protect Register	PRCR	XXXX X000b
04004Bh			
04004Ch	Protect Register 3	PRCR3	0000 0000b
04004Dh	Oscillator Stop Detection Register	CM2	00h
04004Eh			
04004Fh			
040050h			
040051h			
040052h			
040053h	Processor Mode Register 2	PM2	00h
040054h			
040055h			
040056h			
040057h			
040058h			
040059h			
04005Ah	Low Speed Mode Clock Control Register	CM3	XXXX XX00b
04005Bh			
04005Ch			
04005Dh			
04005Eh			
04005Fh			
040060h	Voltage Regulator Control Register	VRCR	0000 0000b
040061h			
040062h			
040063h			
040064h			
040065h			
040066h			
040067h			
040068h to 040093h			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.20 SFR List (20)

Address	Register	Symbol	Reset Value
040094h			
040095h			
040096h			
040097h	Three-phase Output Buffer Control Register	IOBC	0XXX XX0Xb
040098h	Input Function Select Register 0	IFS0	X0X0 X0X0b
040099h	Input Function Select Register 1	IFS1	00XX X0X0b
04009Ah	Input Function Select Register 2	IFS2	0000 0000b
04009Bh	Input Function Select Register 3	IFS3	0000 XXXXb
04009Ch			
04009Dh	Input Function Select Register 5	IFS5	XXXX X0X0b
04009Eh	Input Function Select Register 6	IFS6	XXXX 0000b
04009Fh			
0400A0h	Port P0_0 Function Select Register	P0_0S	0XXX X000b
0400A1h	Port P1_0 Function Select Register	P1_0S	XXXX X000b
0400A2h	Port P0_1 Function Select Register	P0_1S	0XXX X000b
0400A3h	Port P1_1 Function Select Register	P1_1S	XXXX X000b
0400A4h	Port P0_2 Function Select Register	P0_2S	0XXX X000b
0400A5h	Port P1_2 Function Select Register	P1_2S	XXXX X000b
0400A6h	Port P0_3 Function Select Register	P0_3S	0XXX X000b
0400A7h	Port P1_3 Function Select Register	P1_3S	XXXX X000b
0400A8h	Port P0_4 Function Select Register	P0_4S	0XXX X000b
0400A9h	Port P1_4 Function Select Register	P1_4S	XXXX X000b
0400AAh	Port P0_5 Function Select Register	P0_5S	0XXX X000b
0400ABh	Port P1_5 Function Select Register	P1_5S	XXXX X000b
0400ACh	Port P0_6 Function Select Register	P0_6S	0XXX X000b
0400ADh	Port P1_6 Function Select Register	P1_6S	XXXX X000b
0400AEh	Port P0_7 Function Select Register	P0_7S	0XXX X000b
0400AFh	Port P1_7 Function Select Register	P1_7S	XXXX X000b
0400B0h	Port P2_0 Function Select Register	P2_0S	0XXX X000b
0400B1h	Port P3_0 Function Select Register	P3_0S	XXXX X000b
0400B2h	Port P2_1 Function Select Register	P2_1S	0XXX X000b
0400B3h	Port P3_1 Function Select Register	P3_1S	XXXX X000b
0400B4h	Port P2_2 Function Select Register	P2_2S	0XXX X000b
0400B5h	Port P3_2 Function Select Register	P3_2S	XXXX X000b
0400B6h	Port P2_3 Function Select Register	P2_3S	0XXX X000b
0400B7h	Port P3_3 Function Select Register	P3_3S	XXXX X000b
0400B8h	Port P2_4 Function Select Register	P2_4S	0XXX X000b
0400B9h	Port P3_4 Function Select Register	P3_4S	XXXX X000b
0400BAh	Port P2_5 Function Select Register	P2_5S	0XXX X000b
0400BBh	Port P3_5 Function Select Register	P3_5S	XXXX X000b
0400BCh	Port P2_6 Function Select Register	P2_6S	0XXX X000b
0400BDh	Port P3_6 Function Select Register	P3_6S	XXXX X000b
0400BEh	Port P2_7 Function Select Register	P2_7S	0XXX X000b
0400BFh	Port P3_7 Function Select Register	P3_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.21 SFR List (21)

Address	Register	Symbol	Reset Value
0400C0h	Port P4_0 Function Select Register	P4_0S	XXXX X000b
0400C1h	Port P5_0 Function Select Register	P5_0S	XXXX X000b
0400C2h	Port P4_1 Function Select Register	P4_1S	XXXX X000b
0400C3h	Port P5_1 Function Select Register	P5_1S	XXXX X000b
0400C4h	Port P4_2 Function Select Register	P4_2S	XXXX X000b
0400C5h	Port P5_2 Function Select Register	P5_2S	XXXX X000b
0400C6h	Port P4_3 Function Select Register	P4_3S	XXXX X000b
0400C7h	Port P5_3 Function Select Register	P5_3S	XXXX X000b
0400C8h	Port P4_4 Function Select Register	P4_4S	XXXX X000b
0400C9h	Port P5_4 Function Select Register	P5_4S	XXXX X000b
0400CAh	Port P4_5 Function Select Register	P4_5S	XXXX X000b
0400CBh	Port P5_5 Function Select Register	P5_5S	XXXX X000b
0400CCh	Port P4_6 Function Select Register	P4_6S	XXXX X000b
0400CDh	Port P5_6 Function Select Register	P5_6S	XXXX X000b
0400CEh	Port P4_7 Function Select Register	P4_7S	XXXX X000b
0400CFh	Port P5_7 Function Select Register	P5_7S	XXXX X000b
0400D0h	Port P6_0 Function Select Register	P6_0S	XXXX X000b
0400D1h	Port P7_0 Function Select Register	P7_0S	XXXX X000b
0400D2h	Port P6_1 Function Select Register	P6_1S	XXXX X000b
0400D3h	Port P7_1 Function Select Register	P7_1S	XXXX X000b
0400D4h	Port P6_2 Function Select Register	P6_2S	XXXX X000b
0400D5h	Port P7_2 Function Select Register	P7_2S	XXXX X000b
0400D6h	Port P6_3 Function Select Register	P6_3S	XXXX X000b
0400D7h	Port P7_3 Function Select Register	P7_3S	XXXX X000b
0400D8h	Port P6_4 Function Select Register	P6_4S	XXXX X000b
0400D9h	Port P7_4 Function Select Register	P7_4S	XXXX X000b
0400DAh	Port P6_5 Function Select Register	P6_5S	XXXX X000b
0400DBh	Port P7_5 Function Select Register	P7_5S	XXXX X000b
0400DCh	Port P6_6 Function Select Register	P6_6S	XXXX X000b
0400DDh	Port P7_6 Function Select Register	P7_6S	XXXX X000b
0400DEh	Port P6_7 Function Select Register	P6_7S	XXXX X000b
0400DFh	Port P7_7 Function Select Register	P7_7S	XXXX X000b
0400E0h	Port P8_0 Function Select Register	P8_0S	XXXX X000b
0400E1h			
0400E2h	Port P8_1 Function Select Register	P8_1S	XXXX X000b
0400E3h			
0400E4h	Port P8_2 Function Select Register	P8_2S	XXXX X000b
0400E5h			
0400E6h	Port P8_3 Function Select Register	P8_3S	XXXX X000b
0400E7h	Port P9_3 Function Select Register	P9_3S	0XXX X000b
0400E8h	Port P8_4 Function Select Register	P8_4S	XXXX X000b
0400E9h	Port P9_4 Function Select Register	P9_4S	0XXX X000b
0400EAh			
0400EBh	Port P9_5 Function Select Register	P9_5S	0XXX X000b
0400ECh	Port P8_6 Function Select Register	P8_6S	XXXX X000b
0400EDh	Port P9_6 Function Select Register	P9_6S	0XXX X000b
0400EEh	Port P8_7 Function Select Register	P8_7S	XXXX X000b
0400EFh	Port P9_7 Function Select Register	P9_7S	XXXX X000b

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.22 SFR List (22)

Address	Register	Symbol	Reset Value
0400F0h	Port P10_0 Function Select Register	P10_0S	0XXX X000b
0400F1h			
0400F2h	Port P10_1 Function Select Register	P10_1S	0XXX X000b
0400F3h			
0400F4h	Port P10_2 Function Select Register	P10_2S	0XXX X000b
0400F5h			
0400F6h	Port P10_3 Function Select Register	P10_3S	0XXX X000b
0400F7h			
0400F8h	Port P10_4 Function Select Register	P10_4S	0XXX X000b
0400F9h			
0400FAh	Port P10_5 Function Select Register	P10_5S	0XXX X000b
0400FBh			
0400FCh	Port P10_6 Function Select Register	P10_6S	0XXX X000b
0400FDh			
0400FEh	Port P10_7 Function Select Register	P10_7S	0XXX X000b
0400FFh			
040100h			
040101h			
040102h			
040103h			
040104h			
040105h			
040106h			
040107h			
040108h			
040109h			
04010Ah			
04010Bh			
04010Ch			
04010Dh			
04010Eh			
04010Fh			
040110h			
040111h			
040112h			
040113h			
040114h			
040115h			
040116h			
040117h			
040118h			
040119h			
04011Ah			
04011Bh			
04011Ch			
04011Dh			
04011Eh			
04011Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.23 SFR List (23)

Address	Register	Symbol	Reset Value
040120h to 04403Fh			
044040h			
044041h			
044042h			
044043h			
044044h			
044045h			
044046h			
044047h			
044048h			
044049h			
04404Ah			
04404Bh			
04404Ch	Protect Register 4	PRCR4	0000 0000b
04404Dh	Watchdog Timer Clock Control Register	WDK	0000 0000b
04404Eh	Watchdog Timer Start Register	WDTS	XXXX XXXXb
04404Fh	Watchdog Timer Control Register	WDC	000X XXXXb
044050h			
044051h			
044052h			
044053h			
044054h			
044055h			
044056h			
044057h			
044058h			
044059h			
04405Ah			
04405Bh			
04405Ch			
04405Dh			
04405Eh			
04405Fh	Protect Register 2	PRCR2	0XXX XXXXb

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.24 SFR List (24)

Address	Register	Symbol	Reset Value
044060h			
044061h			
044062h			
044063h			
044064h			
044065h			
044066h			
044067h			
044068h			
044069h			
04406Ah			
04406Bh			
04406Ch			
04406Dh			
04406Eh			
04406Fh	External Interrupt Request Source Select Register 0	IFSR0	0000 0000b
044070h	DMA0 Request Source Select Register 2	DM0SL2	XX00 0000b
044071h	DMA1 Request Source Select Register 2	DM1SL2	XX00 0000b
044072h	DMA2 Request Source Select Register 2	DM2SL2	XX00 0000b
044073h	DMA3 Request Source Select Register 2	DM3SL2	XX00 0000b
044074h			
044075h			
044076h			
044077h			
044078h	DMA0 Request Source Select Register	DM0SL	XXX0 0000b
044079h	DMA1 Request Source Select Register	DM1SL	XXX0 0000b
04407Ah	DMA2 Request Source Select Register	DM2SL	XXX0 0000b
04407Bh	DMA3 Request Source Select Register	DM3SL	XXX0 0000b
04407Ch			
04407Dh	Wake-up IPL Setting Register 2	RIPL2	XX0X 0000b
04407Eh			
04407Fh	Wake-up IPL Setting Register 1	RIPL1	XX0X 0000b
044080h	External Interrupt Input Filter Select Register 0	INTF0	0000 0000b
044081h			
044082h	External Interrupt Input Filter Select Register 1	INTF1	0000 0000b
044083h			
044084h			
044085h			
044086h			
044087h			
044088h			
044089h			
04408Ah			
04408Bh			
04408Ch			
04408Dh			
04408Eh			
04408Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.25 SFR List (25)

Address	Register	Symbol	Reset Value
044090h to 044DFFh			
044E00h	LIN Channel Window Select/Input Signal Low Detection Status Register	LCW	0000 0000b
044E01h	LIN Baud Rate Generator Control Register	LBRG	0000 0000b
044E02h	LIN Baud Rate Prescaler 0	LBRP0	00h
044E03h	LIN Baud Rate Prescaler 1	LBRP1	00h
044E04h	LIN Mode Register 0	LMD0	0000 0000b
044E05h	LIN Mode Register 1	LMD1	00h
044E06h	LIN Wake-up Setting Register	LWUP	00h
044E07h			
044E08h	LIN Break Field Setting Register	LBRK	0000 0000b
044E09h	LIN Space Setting Register	LSPC	0000 0000b
044E0Ah	LIN Response Field Setting Register	LRFC	0000 0000b
044E0Bh	LIN ID Buffer Register	LIDB	00h
044E0Ch	LIN Status Control Register	LSC	0000 0000b
044E0Dh	LIN Transmission Control Register	LTC	0000 0000b
044E0Eh	LIN Status Register	LST	0000 0000b
044E0Fh	LIN Error Status Register	LEST	0000 0000b
044E10h	LIN Data 1 Buffer Register	LDB1	00h
044E11h	LIN Data 2 Buffer Register	LDB2	00h
044E12h	LIN Data 3 Buffer Register	LDB3	00h
044E13h	LIN Data 4 Buffer Register	LDB4	00h
044E14h	LIN Data 5 Buffer Register	LDB5	00h
044E15h	LIN Data 6 Buffer Register	LDB6	00h
044E16h	LIN Data 7 Buffer Register	LDB7	00h
044E17h	LIN Data 8 Buffer Register	LDB8	00h
044E18h			
044E19h			
044E1Ah			
044E1Bh			
044E1Ch			
044E1Dh			
044E1Eh			
044E1Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.26 SFR List (26)

Address	Register	Symbol	Reset Value
044E20h to 044EFFh			
044F00h			
044F01h			
044F02h			
044F03h			
044F04h			
044F05h			
044F06h	SS0 Receive Data Register	SS0RDR	FFh
044F07h	SS0 Receive Data Register (H)	SS0RDR (H)	FFh
044F08h	SS0 Control Register H	SS0CRH	00h
044F09h	SS0 Control Register L	SS0CRL	0111 1101b
044F0Ah	SS0 Mode Register	SS0MR	0001 0000b
044F0Bh	SS0 Enable Register	SS0ER	00h
044F0Ch	SS0 Status Register	SS0SR	00h
044F0Dh	SS0 Mode Register 2	SS0MR2	00h
044F0Eh	SS0 Transmit Data Register	SS0TDR	FFh
044F0Fh	SS0 Transmit Data Register (H)	SS0TDR (H)	FFh
044F10h			
044F11h			
044F12h			
044F13h			
044F14h			
044F15h			
044F16h	SS1 Receive Data Register	SS1RDR	FFh
044F17h	SS1 Receive Data Register (H)	SS1RDR (H)	FFh
044F18h	SS1 Control Register H	SS1CRH	00h
044F19h	SS1 Control Register L	SS1CRL	0111 1101b
044F1Ah	SS1 Mode Register	SS1MR	0001 0000b
044F1Bh	SS1 Enable Register	SS1ER	00h
044F1Ch	SS1 Status Register	SS1SR	00h
044F1Dh	SS1 Mode Register 2	SS1MR2	00h
044F1Eh	SS1 Transmit Data Register	SS1TDR	FFh
044F1Fh	SS1 Transmit Data Register (H)	SS1TDR (H)	FFh
044F20h			
044F21h			
044F22h			
044F23h			
044F24h			
044F25h			
044F26h			
044F27h			
044F28h to 0471FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.27 SFR List (27)

Address	Register	Symbol	Reset Value
047200h	Gateway Mode Register	GMR	0000 0000b
047201h			
047202h			
047203h			
047204h	Gateway Routing Table Checksum Control Register	GRMCC	0000 0000b
047205h	Gateway Transmit FIFO Check Control Register	GTFCC	0000 0000b
047206h			
047207h			
047208h	Gateway Transmit FIFO Clear Register	GTFCR	0000 0000b
047209h			
04720Ah			
04720Bh			
04720Ch	Gateway Channel Control Register	GCCR	0000 0000b
04720Dh			
04720Eh			
04720Fh			
047210h			
047211h			
047212h			
047213h			
047214h	Gateway Parity Check Control Register	GPCCR	0000 0000b
047215h			
047216h			
047217h			
047218h	Gateway Time Stamp Timer Control Register	GTSCR	0000 0000b
047219h			
04721Ah			
04721Bh			
04721Ch	Gateway Routing Table Base Pointer Register	GRMBP	00h
04721Dh			
04721Eh			
04721Fh			
047220h	Gateway Transmit FIFO Read Control Register	GTFRC	0000 0000b
047221h	Gateway Transmit FIFO Read Status Register	GTFRS	0000 0000b
047222h			
047223h			
047224h			
047225h			
047226h			
047227h			
047228h			
047229h			
04722Ah			
04722Bh			
04722Ch	Gateway Routing Table Entries Configuration Register	GMREC	0000h
04722Dh			
04722Eh	Gateway Echo-back Control Register	GEBCR	0000 0000b
04722Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.28 SFR List (28)

Address	Register	Symbol	Reset Value
047230h	Gateway Channel 0 FIFO0 Critical Level Configuration Register (1)	GF00CL	00h
047231h	Gateway Channel 1 FIFO0 Critical Level Configuration Register (1)	GF10CL	00h
047232h	Gateway Channel 2 FIFO0 Critical Level Configuration Register	GF20CL	00h
047233h	Gateway Channel 3 FIFO0 Critical Level Configuration Register	GF30CL	00h
047234h	Gateway Channel 4 FIFO0 Critical Level Configuration Register (1)	GF40CL	00h
047235h	Gateway Channel 5 FIFO0 Critical Level Configuration Register	GF50CL	00h
047236h			
047237h			
047238h	Gateway Channel 0 FIFO1 Critical Level Configuration Register (1)	GF01CL	00h
047239h	Gateway Channel 1 FIFO1 Critical Level Configuration Register (1)	GF11CL	00h
04723Ah	Gateway Channel 2 FIFO1 Critical Level Configuration Register	GFF21CL	00h
04723Bh	Gateway Channel 3 FIFO1 Critical Level Configuration Register	GFF31CL	00h
04723Ch	Gateway Channel 4 FIFO1 Critical Level Configuration Register (1)	GFF41CL	00h
04723Dh	Gateway Channel 5 FIFO1 Critical Level Configuration Register	GFF51CL	00h
04723Eh			
04723Fh			
047240h	Gateway Channel Status Register	GCSR	0000 0000b
047241h	Gateway Checksum Calculation/FIFO Check Status Register	GSCFC	0000 0000b
047242h			
047243h			
047244h	Gateway Routing Table Checksum Register	GRMSR	0000 0000h
047245h			
047246h			
047247h			
047248h	Gateway Channel 0 FIFO0 Fill Level (1)	GF00FL	00h
047249h			
04724Ah	Gateway Channel 0 FIFO1 Fill Level (1)	GF01FL	00h
04724Bh			
04724Ch	Gateway Channel 1 FIFO0 Fill Level (1)	GF10FL	00h
04724Dh			
04724Eh	Gateway Channel 1 FIFO1 Fill Level (1)	GF11FL	00h
04724Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. Channels CAN0, CAN1, and CAN 4 are not available in the R32C/142 Group.

Table 4.29 SFR List (29)

Address	Register	Symbol	Reset Value
047250h	Gateway Channel 2 FIFO0 Fill Level	GF20FL	00h
047251h			
047252h	Gateway Channel 2 FIFO1 Fill Level	GF21FL	00h
047253h			
047254h	Gateway Channel 3 FIFO0 Fill Level	GF30FL	00h
047255h			
047256h	Gateway Channel 3 FIFO1 Fill Level	GF31FL	00h
047257h			
047258h	Gateway Channel 4 FIFO0 Fill Level (1)	GF40FL	00h
047259h			
04725Ah	Gateway Channel 4 FIFO1 Fill Level (1)	GF41FL	00h
04725Bh			
04725Ch	Gateway Channel 5 FIFO0 Fill Level	GF50FL	00h
04725Dh			
04725Eh	Gateway Channel 5 FIFO1 Fill Level	GF51FL	00h
04725Fh			
047260h	Gateway Routing Error Status Register	GRESR	0000 0000b
047261h			
047262h	Gateway Error Entry Indication Register	GEEIR	0000h
047263h			
047264h			
047265h			
047266h			
047267h			
047268h	Gateway Time Stamp Timer Register	GTSTR	0000h
047269h			
04726Ah			
04726Bh			
04726Ch			
04726Dh			
04726Eh			
04726Fh			
047270h	Gateway Channel 0 Transmit FIFO Interrupt Enable Register (1)	GC0IE	0000 0000b
047271h	Gateway Channel 1 Transmit FIFO Interrupt Enable Register (1)	GC1IE	0000 0000b
047272h	Gateway Channel 2 Transmit FIFO Interrupt Enable Register	GC2IE	0000 0000b
047273h	Gateway Channel 3 Transmit FIFO Interrupt Enable Register	GC3IE	0000 0000b
047274h	Gateway Channel 4 Transmit FIFO Interrupt Enable Register (1)	GC4IE	0000 0000b
047275h	Gateway Channel 5 Transmit FIFO Interrupt Enable Register	GC5IE	0000 0000b
047276h			
047277h			
047278h	Gateway Channel 0 Transmit FIFO Status Register (1)	GC0SR	0000 0000b
047279h	Gateway Channel 1 Transmit FIFO Status Register (1)	GC1SR	0000 0000b
04727Ah	Gateway Channel 2 Transmit FIFO Status Register	GC2SR	0000 0000b
04727Bh	Gateway Channel 3 Transmit FIFO Status Register	GC3SR	0000 0000b
04727Ch	Gateway Channel 4 Transmit FIFO Status Register (1)	GC4SR	0000 0000b
04727Dh	Gateway Channel 5 Transmit FIFO Status Register	GC5SR	0000 0000b
04727Eh			
04727Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Note:
1. Channels CAN0, CAN1, and CAN 4 are not available in the R32C/142 Group.

Table 4.30 SFR List (30)

Address	Register	Symbol	Reset Value
047280h	Gateway Error Interrupt Enable Register	GIER	0000 0000b
047281h			
047282h			
047283h			
047284h	Gateway Error Status Register	GSR	0000 0000b
047285h			
047286h			
047287h			
047288h			
047289h			
04728Ah			
04728Bh			
04728Ch			
04728Dh			
04728Eh			
04728Fh			
047290h	Gateway Transmit FIFO Read Register 0	GFRR0	0000 0000h
047291h			
047292h			
047293h			
047294h	Gateway Transmit FIFO Read Register 1	GFRR1	0000 0000h
047295h			
047296h			
047297h			
047298h	Gateway Transmit FIFO Read Register 2	GFRR2	0000 0000h
047299h			
04729Ah			
04729Bh			
04729Ch	Gateway Transmit FIFO Read Register 3	GFRR3	0000 0000h
04729Dh			
04729Eh			
04729Fh			
0472A0h			
0472A1h			
0472A2h			
0472A3h			
0472A4h			
0472A5h			
0472A6h			
0472A7h			
0472A8h			
0472A9h			
0472AAh			
0472ABh			
0472ACh			
0472ADh			
0472AEh			
0472AFh			
0472B0h to 0472FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.31 SFR List (31)

Address	Register	Symbol	Reset Value
047300h	Gateway Routing Table Register 0L	GRM0L	XXXX XXXXh
047301h			
047302h			
047303h			
047304h	Gateway Routing Table Register 0H	GRM0H	XXXX XXXXh
047305h			
047306h			
047307h			
047308h	Gateway Routing Table Register 1L	GRM1L	XXXX XXXXh
047309h			
04730Ah			
04730Bh			
04730Ch	Gateway Routing Table Register 1H	GRM1H	XXXX XXXXh
04730Dh			
04730Eh			
04730Fh			
047310h	Gateway Routing Table Register 2L	GRM2L	XXXX XXXXh
047311h			
047312h			
047313h			
047314h	Gateway Routing Table Register 2H	GRM2H	XXXX XXXXh
047315h			
047316h			
047317h			
047318h	Gateway Routing Table Register 3L	GRM3L	XXXX XXXXh
047319h			
04731Ah			
04731Bh			
04731Ch	Gateway Routing Table Register 3H	GRM3H	XXXX XXXXh
04731Dh			
04731Eh			
04731Fh			
047320h	Gateway Routing Table Register 4L	GRM4L	XXXX XXXXh
047321h			
047322h			
047323h			
047324h	Gateway Routing Table Register 4H	GRM4H	XXXX XXXXh
047325h			
047326h			
047327h			
047328h	Gateway Routing Table Register 5L	GRM5L	XXXX XXXXh
047329h			
04732Ah			
04732Bh			
04732Ch	Gateway Routing Table Register 5H	GRM5H	XXXX XXXXh
04732Dh			
04732Eh			
04732Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.32 SFR List (32)

Address	Register	Symbol	Reset Value
047330h	Gateway Routing Table Register 6L	GRM6L	XXXX XXXXh
047331h			
047332h			
047333h			
047334h	Gateway Routing Table Register 6H	GRM6H	XXXX XXXXh
047335h			
047336h			
047337h			
047338h	Gateway Routing Table Register 7L	GRM7L	XXXX XXXXh
047339h			
04733Ah			
04733Bh			
04733Ch	Gateway Routing Table Register 7H	GRM7H	XXXX XXXXh
04733Dh			
04733Eh			
04733Fh			
047340h	Gateway Routing Table Register 8L	GRM8L	XXXX XXXXh
047341h			
047342h			
047343h			
047344h	Gateway Routing Table Register 8H	GRM8H	XXXX XXXXh
047345h			
047346h			
047347h			
047348h	Gateway Routing Table Register 9L	GRM9L	XXXX XXXXh
047349h			
04734Ah			
04734Bh			
04734Ch	Gateway Routing Table Register 9H	GRM9H	XXXX XXXXh
04734Dh			
04734Eh			
04734Fh			
047350h	Gateway Routing Table Register 10L	GRM10L	XXXX XXXXh
047351h			
047352h			
047353h			
047354h	Gateway Routing Table Register 10H	GRM10H	XXXX XXXXh
047355h			
047356h			
047357h			
047358h	Gateway Routing Table Register 11L	GRM11L	XXXX XXXXh
047359h			
04735Ah			
04735Bh			
04735Ch	Gateway Routing Table Register 11H	GRM11H	XXXX XXXXh
04735Dh			
04735Eh			
04735Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.33 SFR List (33)

Address	Register	Symbol	Reset Value
047360h	Gateway Routing Table Register 12L	GRM12L	XXXX XXXXh
047361h			
047362h			
047363h			
047364h	Gateway Routing Table Register 12H	GRM12H	XXXX XXXXh
047365h			
047366h			
047367h			
047368h	Gateway Routing Table Register 13L	GRM13L	XXXX XXXXh
047369h			
04736Ah			
04736Bh			
04736Ch	Gateway Routing Table Register 13H	GRM13H	XXXX XXXXh
04736Dh			
04736Eh			
04736Fh			
047370h	Gateway Routing Table Register 14L	GRM14L	XXXX XXXXh
047371h			
047372h			
047373h			
047374h	Gateway Routing Table Register 14H	GRM14H	XXXX XXXXh
047375h			
047376h			
047377h			
047378h	Gateway Routing Table Register 15L	GRM15L	XXXX XXXXh
047379h			
04737Ah			
04737Bh			
04737Ch	Gateway Routing Table Register 15H	GRM15H	XXXX XXXXh
04737Dh			
04737Eh			
04737Fh			
047380h	Gateway Bit Search Support Register 0	GBSR0	0000h
047381h			
047382h	Gateway Bit Search Status Register 0	GBSS0	1000 0000b
047383h	Gateway Bit Search Control Register 0	GBSC0	0000 0000b
047384h	Gateway Bit Search Support Register 1	GBSR1	0000h
047385h			
047386h	Gateway Bit Search Status Register 1	GBSS1	1000 0000b
047387h	Gateway Bit Search Control Register 1	GBSC1	0000 0000b
047388h			
047389h			
04738Ah			
04738Bh			
04738Ch			
04738Dh			
04738Eh			
04738Fh			
047390h to 0473FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.34 SFR List (34)

Address	Register	Symbol	Reset Value
047400h	CAN5 Mailbox 0: Message Identifier	C5MB0	XXXX XXXXh
047401h			
047402h			
047403h			
047404h			
047405h	CAN5 Mailbox 0: Data Length		XXh
047406h	CAN5 Mailbox 0: Data Field		XXXX XXXX
047407h			XXXX XXXXh
047408h			
047409h			
04740Ah			
04740Bh			
04740Ch			
04740Dh			
04740Eh	CAN5 Mailbox 0: Time Stamp		XXXXh
04740Fh			
047410h	CAN5 Mailbox 1: Message Identifier	C5MB1	XXXX XXXXh
047411h			
047412h			
047413h			
047414h			
047415h	CAN5 Mailbox 1: Data Length		XXh
047416h	CAN5 Mailbox 1: Data Field		XXXX XXXX
047417h			XXXX XXXXh
047418h			
047419h			
04741Ah			
04741Bh			
04741Ch			
04741Dh			
04741Eh	CAN5 Mailbox 1: Time Stamp		XXXXh
04741Fh			
047420h	CAN5 Mailbox 2: Message Identifier	C5MB2	XXXX XXXXh
047421h			
047422h			
047423h			
047424h			
047425h	CAN5 Mailbox 2: Data Length		XXh
047426h	CAN5 Mailbox 2: Data Field		XXXX XXXX
047427h			XXXX XXXXh
047428h			
047429h			
04742Ah			
04742Bh			
04742Ch			
04742Dh			
04742Eh	CAN5 Mailbox 2: Time Stamp		XXXXh
04742Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.35 SFR List (35)

Address	Register	Symbol	Reset Value
047430h	CAN5 Mailbox 3: Message Identifier	C5MB3	XXXX XXXXh
047431h			
047432h			
047433h			
047434h			
047435h	CAN5 Mailbox 3: Data Length		XXh
047436h	CAN5 Mailbox 3: Data Field		XXXX XXXX
047437h			XXXX XXXXh
047438h			
047439h			
04743Ah			
04743Bh			
04743Ch			
04743Dh			
04743Eh	CAN5 Mailbox 3: Time Stamp		XXXXh
04743Fh			
047440h	CAN5 Mailbox 4: Message Identifier	C5MB4	XXXX XXXXh
047441h			
047442h			
047443h			
047444h			
047445h	CAN5 Mailbox 4: Data Length		XXh
047446h	CAN5 Mailbox 4: Data Field		XXXX XXXX
047447h			XXXX XXXXh
047448h			
047449h			
04744Ah			
04744Bh			
04744Ch			
04744Dh			
04744Eh	CAN5 Mailbox 4: Time Stamp		XXXXh
04744Fh			
047450h	CAN5 Mailbox 5: Message Identifier	C5MB5	XXXX XXXXh
047451h			
047452h			
047453h			
047454h			
047455h	CAN5 Mailbox 5: Data Length		XXh
047456h	CAN5 Mailbox 5: Data Field		XXXX XXXX
047457h			XXXX XXXXh
047458h			
047459h			
04745Ah			
04745Bh			
04745Ch			
04745Dh			
04745Eh	CAN5 Mailbox 5: Time Stamp		XXXXh
04745Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.36 SFR List (36)

Address	Register	Symbol	Reset Value
047460h	CAN5 Mailbox 6: Message Identifier	C5MB6	XXXX XXXXh
047461h			
047462h			
047463h			
047464h			
047465h	CAN5 Mailbox 6: Data Length		XXh
047466h	CAN5 Mailbox 6: Data Field		XXXX XXXX
047467h			XXXX XXXXh
047468h			
047469h			
04746Ah			
04746Bh			
04746Ch			
04746Dh			
04746Eh	CAN5 Mailbox 6: Time Stamp		XXXXh
04746Fh			
047470h	CAN5 Mailbox 7: Message Identifier	C5MB7	XXXX XXXXh
047471h			
047472h			
047473h			
047474h			
047475h	CAN5 Mailbox 7: Data Length		XXh
047476h	CAN5 Mailbox 7: Data Field		XXXX XXXX
047477h			XXXX XXXXh
047478h			
047479h			
04747Ah			
04747Bh			
04747Ch			
04747Dh			
04747Eh	CAN5 Mailbox 7: Time Stamp		XXXXh
04747Fh			
047480h	CAN5 Mailbox 8: Message Identifier	C5MB8	XXXX XXXXh
047481h			
047482h			
047483h			
047484h			
047485h	CAN5 Mailbox 8: Data Length		XXh
047486h	CAN5 Mailbox 8: Data Field		XXXX XXXX
047487h			XXXX XXXXh
047488h			
047489h			
04748Ah			
04748Bh			
04748Ch			
04748Dh			
04748Eh	CAN5 Mailbox 8: Time Stamp		XXXXh
04748Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.37 SFR List (37)

Address	Register	Symbol	Reset Value
047490h	CAN5 Mailbox 9: Message Identifier	C5MB9	XXXX XXXXh
047491h			
047492h			
047493h			
047494h			
047495h	CAN5 Mailbox 9: Data Length		XXh
047496h	CAN5 Mailbox 9 Data Field		XXXX XXXX
047497h			XXXX XXXXh
047498h			
047499h			
04749Ah			
04749Bh			
04749Ch			
04749Dh			
04749Eh	CAN5 Mailbox 9: Time Stamp		XXXXh
04749Fh			
0474A0h	CAN5 Mailbox 10: Message Identifier	C5MB10	XXXX XXXXh
0474A1h			
0474A2h			
0474A3h			
0474A4h			
0474A5h	CAN5 Mailbox 10: Data Length		XXh
0474A6h	CAN5 Mailbox 10: Data Field		XXXX XXXX
0474A7h			XXXX XXXXh
0474A8h			
0474A9h			
0474AAh			
0474ABh			
0474ACh			
0474ADh			
0474AEh	CAN5 Mailbox 10: Time Stamp		XXXXh
0474AFh			
0474B0h	CAN5 Mailbox 11: Message Identifier	C5MB11	XXXX XXXXh
0474B1h			
0474B2h			
0474B3h			
0474B4h			
0474B5h	CAN5 Mailbox 11: Data Length		XXh
0474B6h	CAN5 Mailbox 11: Data Field		XXXX XXXX
0474B7h			XXXX XXXXh
0474B8h			
0474B9h			
0474BAh			
0474BBh			
0474BCh			
0474BDh			
0474BEh	CAN5 Mailbox 11: Time Stamp		XXXXh
0474BFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.38 SFR List (38)

Address	Register	Symbol	Reset Value
0474C0h	CAN5 Mailbox 12: Message Identifier	C5MB12	XXXX XXXXh
0474C1h			
0474C2h			
0474C3h			
0474C4h			
0474C5h	CAN5 Mailbox 12 Data Length		XXh
0474C6h	CAN5 Mailbox 12: Data Field		XXXX XXXX
0474C7h			XXXX XXXXh
0474C8h			
0474C9h			
0474CAh			
0474CBh			
0474CCh			
0474CDh			
0474CEh	CAN5 Mailbox 12: Time Stamp		XXXXh
0474CFh			
0474D0h	CAN5 Mailbox 13: Message Identifier	C5MB13	XXXX XXXXh
0474D1h			
0474D2h			
0474D3h			
0474D4h			
0474D5h	CAN5 Mailbox 13: Data Length		XXh
0474D6h	CAN5 Mailbox 13: Data Field		XXXX XXXX
0474D7h			XXXX XXXXh
0474D8h			
0474D9h			
0474DAh			
0474DBh			
0474DCh			
0474DDh			
0474DEh	CAN5 Mailbox 13: Time Stamp		XXXXh
0474DFh			
0474E0h	CAN5 Mailbox 14: Message Identifier	C5MB14	XXXX XXXXh
0474E1h			
0474E2h			
0474E3h			
0474E4h			
0474E5h	CAN5 Mailbox 14: Data Length		XXh
0474E6h	CAN5 Mailbox 14: Data Field		XXXX XXXX
0474E7h			XXXX XXXXh
0474E8h			
0474E9h			
0474EAh			
0474EBh			
0474ECh			
0474EDh			
0474EEh	CAN5 Mailbox 14: Time Stamp		XXXXh
0474EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.39 SFR List (39)

Address	Register	Symbol	Reset Value
0474F0h	CAN5 Mailbox 15: Message Identifier	C5MB15	XXXX XXXXh
0474F1h			
0474F2h			
0474F3h			
0474F4h			
0474F5h	CAN5 Mailbox 15: Data Length		XXh
0474F6h	CAN5 Mailbox 15: Data Field		XXXX XXXX
0474F7h			XXXX XXXXh
0474F8h			
0474F9h			
0474FAh			
0474FBh			
0474FCh			
0474FDh			
0474FEh	CAN5 Mailbox 15: Time Stamp		XXXXh
0474FFh			
047500h to 04750Fh			
047510h	CAN5 Mask Register 0	C5MKR0	XXXX XXXXh
047511h			
047512h			
047513h			
047514h	CAN5 Mask Register 1	C5MKR1	XXXX XXXXh
047515h			
047516h			
047517h			
047518h	CAN5 Mask Register 2	C5MKR2	XXXX XXXXh
047519h			
04751Ah			
04751Bh			
04751Ch	CAN5 Mask Register 3	C5MKR3	XXXX XXXXh
04751Dh			
04751Eh			
04751Fh			
047520h	CAN5 FIFO Receive ID Compare Register 0	C5FIDCR0	XXXX XXXXh
047521h			
047522h			
047523h			
047524h	CAN5 FIFO Receive ID Compare Register 1	C5FIDCR1	XXXX XXXXh
047525h			
047526h			
047527h			
047528h			
047529h			
04752Ah	CAN5 Mask Invalid Register	C5MKIVLR	XXXXh
04752Bh			
04752Ch			
04752Dh			
04752Eh	CAN5 Mailbox Interrupt Enable Register	C5MIER	XXXXh
04752Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.40 SFR List (40)

Address	Register	Symbol	Reset Value
047530h	CAN5 Message Control Register 0	C5MCTL0	00h
047531h	CAN5 Message Control Register 1	C5MCTL1	00h
047532h	CAN5 Message Control Register 2	C5MCTL2	00h
047533h	CAN5 Message Control Register 3	C5MCTL3	00h
047534h	CAN5 Message Control Register 4	C5MCTL4	00h
047535h	CAN5 Message Control Register 5	C5MCTL5	00h
047536h	CAN5 Message Control Register 6	C5MCTL6	00h
047537h	CAN5 Message Control Register 7	C5MCTL7	00h
047538h	CAN5 Message Control Register 8	C5MCTL8	00h
047539h	CAN5 Message Control Register 9	C5MCTL9	00h
04753Ah	CAN5 Message Control Register 10	C5MCTL10	00h
04753Bh	CAN5 Message Control Register 11	C5MCTL11	00h
04753Ch	CAN5 Message Control Register 12	C5MCTL12	00h
04753Dh	CAN5 Message Control Register 13	C5MCTL13	00h
04753Eh	CAN5 Message Control Register 14	C5MCTL14	00h
04753Fh	CAN5 Message Control Register 15	C5MCTL15	00h
047540h	CAN5 Control Register	C5CTLR	0000 0101b
047541h			0000 0000b
047542h	CAN5 Status Register	C5STR	0000 0101b
047543h			0000 0000b
047544h	CAN5 Bit Configuration Register	C5BCR	00 0000h
047545h			
047546h			
047547h	CAN5 Clock Select Register	C5CLKR	000X 0000b
047548h	CAN5 Receive FIFO Control Register	C5RFCR	1000 0000b
047549h	CAN5 Receive FIFO Pointer Control Register	C5RFPCR	XXh
04754Ah	CAN5 Transmit FIFO Control Register	C5TFCR	1000 0000b
04754Bh	CAN5 Transmit FIFO Pointer Control Register	C5TFPCR	XXh
04754Ch	CAN5 Error Interrupt Enable Register	C5EIER	00h
04754Dh	CAN5 Error Interrupt Factor Judge Register	C5EIFR	00h
04754Eh	CAN5 Receive Error Count Register	C5RECR	00h
04754Fh	CAN5 Transmit Error Count Register	C5TECR	00h
047550h	CAN5 Error Code Store Register	C5ECSR	00h
047551h	CAN5 Channel Search Support Register	C5CSSR	XXh
047552h	CAN5 Mailbox Search Status Register	C5MSSR	1000 0000b
047553h	CAN5 Mailbox Search Mode Register	C5MSMR	0000 0000b
047554h	CAN5 Time Stamp Register	C5TSR	0000h
047555h			
047556h	CAN5 Acceptance Filter Support Register	C5AFSR	XXXXh
047557h			
047558h	CAN5 Test Control Register	C5TCR	00h
047559h			
04755Ah			
04755Bh			
04755Ch to 0475FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.41 SFR List (41)

Address	Register	Symbol	Reset Value
047600h	CAN4 Mailbox 0: Message Identifier	C4MB0	XXXX XXXXh
047601h			
047602h			
047603h			
047604h			
047605h	CAN4 Mailbox 0: Data Length		XXh
047606h	CAN4 Mailbox 0: Data Field		XXXX XXXX
047607h			XXXX XXXXh
047608h			
047609h			
04760Ah			
04760Bh			
04760Ch			
04760Dh			
04760Eh	CAN4 Mailbox 0: Time Stamp		XXXXh
04760Fh			
047610h	CAN4 Mailbox 1: Message Identifier	C4MB1	XXXX XXXXh
047611h			
047612h			
047613h			
047614h			
047615h	CAN4 Mailbox 1: Data Length		XXh
047616h	CAN4 Mailbox 1: Data Field		XXXX XXXX
047617h			XXXX XXXXh
047618h			
047619h			
04761Ah			
04761Bh			
04761Ch			
04761Dh			
04761Eh	CAN4 Mailbox 1: Time Stamp		XXXXh
04761Fh			
047620h	CAN4 Mailbox 2: Message Identifier	C4MB2	XXXX XXXXh
047621h			
047622h			
047623h			
047624h			
047625h	CAN4 Mailbox 2: Data Length		XXh
047626h	CAN4 Mailbox 2: Data Field		XXXX XXXX
047627h			XXXX XXXXh
047628h			
047629h			
04762Ah			
04762Bh			
04762Ch			
04762Dh			
04762Eh	CAN4 Mailbox 2: Time Stamp		XXXXh
04762Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.42 SFR List (42)

Address	Register	Symbol	Reset Value
047630h	CAN4 Mailbox 3: Message Identifier	C4MB3	XXXX XXXXh
047631h			
047632h			
047633h			
047634h			
047635h	CAN4 Mailbox 3: Data Length		XXh
047636h	CAN4 Mailbox 3: Data Field		XXXX XXXX
047637h			XXXX XXXXh
047638h			
047639h			
04763Ah			
04763Bh			
04763Ch			
04763Dh			
04763Eh	CAN4 Mailbox 3: Time Stamp		XXXXh
04763Fh			
047640h	CAN4 Mailbox 4: Message Identifier	C4MB4	XXXX XXXXh
047641h			
047642h			
047643h			
047644h			
047645h	CAN4 Mailbox 4: Data Length		XXh
047646h	CAN4 Mailbox 4: Data Field		XXXX XXXX
047647h			XXXX XXXXh
047648h			
047649h			
04764Ah			
04764Bh			
04764Ch			
04764Dh			
04764Eh	CAN4 Mailbox 4: Time Stamp		XXXXh
04764Fh			
047650h	CAN4 Mailbox 5: Message Identifier	C4MB5	XXXX XXXXh
047651h			
047652h			
047653h			
047654h			
047655h	CAN4 Mailbox 5: Data Length		XXh
047656h	CAN4 Mailbox 5: Data Field		XXXX XXXX
047657h			XXXX XXXXh
047658h			
047659h			
04765Ah			
04765Bh			
04765Ch			
04765Dh			
04765Eh	CAN4 Mailbox 5: Time Stamp		XXXXh
04765Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.43 SFR List (43)

Address	Register	Symbol	Reset Value
047660h	CAN4 Mailbox 6: Message Identifier	C4MB6	XXXX XXXXh
047661h			
047662h			
047663h			
047664h			
047665h	CAN4 Mailbox 6: Data Length		XXh
047666h	CAN4 Mailbox 6: Data Field		XXXX XXXX
047667h			XXXX XXXXh
047668h			
047669h			
04766Ah			
04766Bh			
04766Ch			
04766Dh			
04766Eh	CAN4 Mailbox 6: Time Stamp		XXXXh
04766Fh			
047670h	CAN4 Mailbox 7: Message Identifier	C4MB7	XXXX XXXXh
047671h			
047672h			
047673h			
047674h			
047675h	CAN4 Mailbox 7: Data Length		XXh
047676h	CAN4 Mailbox 7: Data Field		XXXX XXXX
047677h			XXXX XXXXh
047678h			
047679h			
04767Ah			
04767Bh			
04767Ch			
04767Dh			
04767Eh	CAN4 Mailbox 7: Time Stamp		XXXXh
04767Fh			
047680h	CAN4 Mailbox 8: Message Identifier	C4MB8	XXXX XXXXh
047681h			
047682h			
047683h			
047684h			
047685h	CAN4 Mailbox 8: Data Length		XXh
047686h	CAN4 Mailbox 8: Data Field		XXXX XXXX
047687h			XXXX XXXXh
047688h			
047689h			
04768Ah			
04768Bh			
04768Ch			
04768Dh			
04768Eh	CAN4 Mailbox 8:Time Stamp		XXXXh
04768Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.44 SFR List (44)

Address	Register	Symbol	Reset Value
047690h	CAN4 Mailbox 9: Message Identifier	C4MB9	XXXX XXXXh
047691h			
047692h			
047693h			
047694h			
047695h	CAN4 Mailbox 9: Data Length		XXh
047696h	CAN4 Mailbox 9: Data Field		XXXX XXXX
047697h			XXXX XXXXh
047698h			
047699h			
04769Ah			
04769Bh			
04769Ch			
04769Dh			
04769Eh	CAN4 Mailbox 9: Time Stamp		XXXXh
04769Fh			
0476A0h	CAN4 Mailbox 10: Message Identifier	C4MB10	XXXX XXXXh
0476A1h			
0476A2h			
0476A3h			
0476A4h			
0476A5h	CAN4 Mailbox 10: Data Length		XXh
0476A6h	CAN4 Mailbox 10: Data Field		XXXX XXXX
0476A7h			XXXX XXXXh
0476A8h			
0476A9h			
0476AAh			
0476ABh			
0476ACh			
0476ADh			
0476AEh	CAN4 Mailbox 10: Time Stamp		XXXXh
0476AFh			
0476B0h	CAN4 Mailbox 11: Message Identifier	C4MB11	XXXX XXXXh
0476B1h			
0476B2h			
0476B3h			
0476B4h			
0476B5h	CAN4 Mailbox 11: Data Length		XXh
0476B6h	CAN4 Mailbox 11: Data Field		XXXX XXXX
0476B7h			XXXX XXXXh
0476B8h			
0476B9h			
0476BAh			
0476BBh			
0476BCh			
0476BDh			
0476BEh	CAN4 Mailbox 11: Time Stamp		XXXXh
0476BFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.45 SFR List (45)

Address	Register	Symbol	Reset Value
0476C0h	CAN4 Mailbox 12: Message Identifier	C4MB12	XXXX XXXXh
0476C1h			
0476C2h			
0476C3h			
0476C4h			
0476C5h	CAN4 Mailbox 12: Data Length		XXh
0476C6h	CAN4 Mailbox 12: Data Field		XXXX XXXX
0476C7h			XXXX XXXXh
0476C8h			
0476C9h			
0476CAh			
0476CBh			
0476CCh			
0476CDh			
0476CEh	CAN4 Mailbox 12: Time Stamp		XXXXh
0476CFh			
0476D0h	CAN4 Mailbox 13: Message Identifier	C4MB13	XXXX XXXXh
0476D1h			
0476D2h			
0476D3h			
0476D4h			
0476D5h	CAN4 Mailbox 13: Data Length		XXh
0476D6h	CAN4 Mailbox 13: Data Field		XXXX XXXX
0476D7h			XXXX XXXXh
0476D8h			
0476D9h			
0476DAh			
0476DBh			
0476DCh			
0476DDh			
0476DEh	CAN4 Mailbox 13: Time Stamp		XXXXh
0476DFh			
0476E0h	CAN4 Mailbox 14: Message Identifier	C4MB14	XXXX XXXXh
0476E1h			
0476E2h			
0476E3h			
0476E4h			
0476E5h	CAN4 Mailbox 14: Data Length		XXh
0476E6h	CAN4 Mailbox 14: Data Field		XXXX XXXX
0476E7h			XXXX XXXXh
0476E8h			
0476E9h			
0476EAh			
0476EBh			
0476ECh			
0476EDh			
0476EEh	CAN4 Mailbox 14: Time Stamp		XXXXh
0476EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.46 SFR List (46)

Address	Register	Symbol	Reset Value
0476F0h	CAN4 Mailbox 15: Message Identifier	C4MB15	XXXX XXXXh
0476F1h			
0476F2h			
0476F3h			
0476F4h			
0476F5h	CAN4 Mailbox 15: Data Length		XXh
0476F6h	CAN4 Mailbox 15: Data Field		XXXX XXXX
0476F7h			XXXX XXXXh
0476F8h			
0476F9h			
0476FAh			
0476FBh			
0476FCh			
0476FDh			
0476FEh	CAN4 Mailbox 15: Time Stamp		XXXXh
0476FFh			
047700h to 04770Fh			
047710h	CAN4 Mask Register 0	C4MKR0	XXXX XXXXh
047711h			
047712h			
047713h			
047714h	CAN4 Mask Register 1	C4MKR1	XXXX XXXXh
047715h			
047716h			
047717h			
047718h	CAN4 Mask Register 2	C4MKR2	XXXX XXXXh
047719h			
04771Ah			
04771Bh			
04771Ch	CAN4 Mask Register 3	C4MKR3	XXXX XXXXh
04771Dh			
04771Eh			
04771Fh			
047720h	CAN4 FIFO Receive ID Compare Register 0	C4FIDCR0	XXXX XXXXh
047721h			
047722h			
047723h			
047724h	CAN4 FIFO Receive ID Compare Register 1	C4FIDCR1	XXXX XXXXh
047725h			
047726h			
047727h			
047728h			
047729h			
04772Ah	CAN4 Mask Invalid Register	C4MKIVLR	XXXXh
04772Bh			
04772Ch			
04772Dh			
04772Eh	CAN4 Mailbox Interrupt Enable Register	C4MIER	XXXXh
04772Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.47 SFR List (47)

Address	Register	Symbol	Reset Value
047730h	CAN4 Message Control Register 0	C4MCTL0	00h
047731h	CAN4 Message Control Register 1	C4MCTL1	00h
047732h	CAN4 Message Control Register 2	C4MCTL2	00h
047733h	CAN4 Message Control Register 3	C4MCTL3	00h
047734h	CAN4 Message Control Register 4	C4MCTL4	00h
047735h	CAN4 Message Control Register 5	C4MCTL5	00h
047736h	CAN4 Message Control Register 6	C4MCTL6	00h
047737h	CAN4 Message Control Register 7	C4MCTL7	00h
047738h	CAN4 Message Control Register 8	C4MCTL8	00h
047739h	CAN4 Message Control Register 9	C4MCTL9	00h
04773Ah	CAN4 Message Control Register 10	C4MCTL10	00h
04773Bh	CAN4 Message Control Register 11	C4MCTL11	00h
04773Ch	CAN4 Message Control Register 12	C4MCTL12	00h
04773Dh	CAN4 Message Control Register 13	C4MCTL13	00h
04773Eh	CAN4 Message Control Register 14	C4MCTL14	00h
04773Fh	CAN4 Message Control Register 15	C4MCTL15	00h
047740h	CAN4 Control Register	C4CTLR	0000 0101b
047741h			0000 0000b
047742h	CAN4 Status Register	C4STR	0000 0101b
047743h			0000 0000b
047744h	CAN4 Bit Configuration Register	C4BCR	00 0000h
047745h			
047746h			
047747h	CAN4 Clock Select Register	C4CLKR	000X 0000b
047748h	CAN4 Receive FIFO Control Register	C4RFCR	1000 0000b
047749h	CAN4 Receive FIFO Pointer Control Register	C4RFPCR	XXh
04774Ah	CAN4 Transmit FIFO Control Register	C4TFCR	1000 0000b
04774Bh	CAN4 Transmit FIFO Pointer Control Register	C4TFPCR	XXh
04774Ch	CAN4 Error Interrupt Enable Register	C4EIER	00h
04774Dh	CAN4 Error Interrupt Factor Judge Register	C4EIFR	00h
04774Eh	CAN4 Receive Error Count Register	C4RECR	00h
04774Fh	CAN4 Transmit Error Count Register	C4TECR	00h
047750h	CAN4 Error Code Store Register	C4ECSR	00h
047751h	CAN4 Channel Search Support Register	C4CSSR	XXh
047752h	CAN4 Mailbox Search Status Register	C4MSSR	1000 0000b
047753h	CAN4 Mailbox Search Mode Register	C4MSMR	0000 0000b
047754h	CAN4 Time Stamp Register	C4TSR	0000h
047755h			
047756h	CAN4 Acceptance Filter Support Register	C4AFSR	XXXXh
047757h			
047758h	CAN4 Test Control Register	C4TCR	00h
047759h			
04775Ah			
04775Bh			
04775Ch to 0477FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.48 SFR List (48)

Address	Register	Symbol	Reset Value
047800h	CAN3 Mailbox 0: Message Identifier	C3MB0	XXXX XXXXh
047801h			
047802h			
047803h			
047804h			
047805h	CAN3 Mailbox 0: Data Length		XXh
047806h	CAN3 Mailbox 0: Data Field		XXXX XXXX
047807h			XXXX XXXXh
047808h			
047809h			
04780Ah			
04780Bh			
04780Ch			
04780Dh			
04780Eh	CAN3 Mailbox 0: Time Stamp		XXXXh
04780Fh			
047810h	CAN3 Mailbox 1: Message Identifier	C3MB1	XXXX XXXXh
047811h			
047812h			
047813h			
047814h			
047815h	CAN3 Mailbox 1: Data Length		XXh
047816h	CAN3 Mailbox 1: Data Field		XXXX XXXX
047817h			XXXX XXXXh
047818h			
047819h			
04781Ah			
04781Bh			
04781Ch			
04781Dh			
04781Eh	CAN3 Mailbox 1: Time Stamp		XXXXh
04781Fh			
047820h	CAN3 Mailbox 2: Message Identifier	C3MB2	XXXX XXXXh
047821h			
047822h			
047823h			
047824h			
047825h	CAN3 Mailbox 2: Data Length		XXh
047826h	CAN3 Mailbox 2: Data Field		XXXX XXXX
047827h			XXXX XXXXh
047828h			
047829h			
04782Ah			
04782Bh			
04782Ch			
04782Dh			
04782Eh	CAN3 Mailbox 2: Time Stamp		XXXXh
04782Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.49 SFR List (49)

Address	Register	Symbol	Reset Value
047830h	CAN3 Mailbox 3: Message Identifier	C3MB3	XXXX XXXXh
047831h			
047832h			
047833h			
047834h			
047835h	CAN3 Mailbox 3: Data Length		XXh
047836h	CAN3 Mailbox 3: Data Field		XXXX XXXX
047837h			XXXX XXXXh
047838h			
047839h			
04783Ah			
04783Bh			
04783Ch			
04783Dh			
04783Eh	CAN3 Mailbox 3: Time Stamp		XXXXh
04783Fh			
047840h	CAN3 Mailbox 4: Message Identifier	C3MB4	XXXX XXXXh
047841h			
047842h			
047843h			
047844h			
047845h	CAN3 Mailbox 4: Data Length		XXh
047846h	CAN3 Mailbox 4: Data Field		XXXX XXXX
047847h			XXXX XXXXh
047848h			
047849h			
04784Ah			
04784Bh			
04784Ch			
04784Dh			
04784Eh	CAN3 Mailbox 4: Time Stamp		XXXXh
04784Fh			
047850h	CAN3 Mailbox 5: Message Identifier	C3MB5	XXXX XXXXh
047851h			
047852h			
047853h			
047854h			
047855h	CAN3 Mailbox 5: Data Length		XXh
047856h	CAN3 Mailbox 5: Data Field		XXXX XXXX
047857h			XXXX XXXXh
047858h			
047859h			
04785Ah			
04785Bh			
04785Ch			
04785Dh			
04785Eh	CAN3 Mailbox 5: Time Stamp		XXXXh
04785Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.50 SFR List (50)

Address	Register	Symbol	Reset Value
047860h	CAN3 Mailbox 6: Message Identifier	C3MB6	XXXX XXXXh
047861h			
047862h			
047863h			
047864h			
047865h	CAN3 Mailbox 6: Data Length		XXh
047866h	CAN3 Mailbox 6: Data Field		XXXX XXXX
047867h			XXXX XXXXh
047868h			
047869h			
04786Ah			
04786Bh			
04786Ch			
04786Dh			
04786Eh	CAN3 Mailbox 6: Time Stamp		XXXXh
04786Fh			
047870h	CAN3 Mailbox 7: Message Identifier	C3MB7	XXXX XXXXh
047871h			
047872h			
047873h			
047874h			
047875h	CAN3 Mailbox 7: Data Length		XXh
047876h	CAN3 Mailbox 7: Data Field		XXXX XXXX
047877h			XXXX XXXXh
047878h			
047879h			
04787Ah			
04787Bh			
04787Ch			
04787Dh			
04787Eh	CAN3 Mailbox 7: Time Stamp		XXXXh
04787Fh			
047880h	CAN3 Mailbox 8: Message Identifier	C3MB8	XXXX XXXXh
047881h			
047882h			
047883h			
047884h			
047885h	CAN3 Mailbox 8: Data Length		XXh
047886h	CAN3 Mailbox 8: Data Field		XXXX XXXX
047887h			XXXX XXXXh
047888h			
047889h			
04788Ah			
04788Bh			
04788Ch			
04788Dh			
04788Eh	CAN3 Mailbox 8:Time Stamp		XXXXh
04788Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.51 SFR List (51)

Address	Register	Symbol	Reset Value
047890h	CAN3 Mailbox 9: Message Identifier	C3MB9	XXXX XXXXh
047891h			
047892h			
047893h			
047894h			
047895h	CAN3 Mailbox 9: Data Length		XXh
047896h	CAN3 Mailbox 9: Data Field		XXXX XXXX
047897h			XXXX XXXXh
047898h			
047899h			
04789Ah			
04789Bh			
04789Ch			
04789Dh			
04789Eh	CAN3 Mailbox 9: Time Stamp		XXXXh
04789Fh			
0478A0h	CAN3 Mailbox 10: Message Identifier	C3MB10	XXXX XXXXh
0478A1h			
0478A2h			
0478A3h			
0478A4h			
0478A5h	CAN3 Mailbox 10: Data Length		XXh
0478A6h	CAN3 Mailbox 10: Data Field		XXXX XXXX
0478A7h			XXXX XXXXh
0478A8h			
0478A9h			
0478AAh			
0478ABh			
0478ACh			
0478ADh			
0478AEh	CAN3 Mailbox 10: Time Stamp		XXXXh
0478AFh			
0478B0h	CAN3 Mailbox 11: Message Identifier	C3MB11	XXXX XXXXh
0478B1h			
0478B2h			
0478B3h			
0478B4h			
0478B5h	CAN3 Mailbox 11: Data Length		XXh
0478B6h	CAN3 Mailbox 11: Data Field		XXXX XXXX
0478B7h			XXXX XXXXh
0478B8h			
0478B9h			
0478BAh			
0478BBh			
0478BCh			
0478BDh			
0478BEh	CAN3 Mailbox 11: Time Stamp		XXXXh
0478BFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.52 SFR List (52)

Address	Register	Symbol	Reset Value
0478C0h	CAN3 Mailbox 12: Message Identifier	C3MB12	XXXX XXXXh
0478C1h			
0478C2h			
0478C3h			
0478C4h			
0478C5h	CAN3 Mailbox 12: Data Length		XXh
0478C6h	CAN3 Mailbox 12: Data Field		XXXX XXXX
0478C7h			XXXX XXXXh
0478C8h			
0478C9h			
0478CAh			
0478CBh			
0478CCh			
0478CDh			
0478CEh	CAN3 Mailbox 12: Time Stamp		XXXXh
0478CFh			
0478D0h	CAN3 Mailbox 13: Message Identifier	C3MB13	XXXX XXXXh
0478D1h			
0478D2h			
0478D3h			
0478D4h			
0478D5h	CAN3 Mailbox 13: Data Length		XXh
0478D6h	CAN3 Mailbox 13: Data Field		XXXX XXXX
0478D7h			XXXX XXXXh
0478D8h			
0478D9h			
0478DAh			
0478DBh			
0478DCh			
0478DDh			
0478DEh	CAN3 Mailbox 13: Time Stamp		XXXXh
0478DFh			
0478E0h	CAN3 Mailbox 14: Message Identifier	C3MB14	XXXX XXXXh
0478E1h			
0478E2h			
0478E3h			
0478E4h			
0478E5h	CAN3 Mailbox 14: Data Length		XXh
0478E6h	CAN3 Mailbox 14: Data Field		XXXX XXXX
0478E7h			XXXX XXXXh
0478E8h			
0478E9h			
0478EAh			
0478EBh			
0478ECh			
0478EDh			
0478EEh	CAN3 Mailbox 14: Time Stamp		XXXXh
0478EFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.53 SFR List (53)

Address	Register	Symbol	Reset Value
0478F0h	CAN3 Mailbox 15: Message Identifier	C3MB15	XXXX XXXXh
0478F1h			
0478F2h			
0478F3h			
0478F4h			
0478F5h	CAN3 Mailbox 15: Data Length		XXh
0478F6h	CAN3 Mailbox 15: Data Field		XXXX XXXX
0478F7h			XXXX XXXXh
0478F8h			
0478F9h			
0478FAh			
0478FBh			
0478FCh			
0478FDh			
0478FEh	CAN3 Mailbox 15: Time Stamp		XXXXh
0478FFh			
047900h to 04790Fh			
047910h	CAN3 Mask Register 0	C3MKR0	XXXX XXXXh
047911h			
047912h			
047913h			
047914h	CAN3 Mask Register 1	C3MKR1	XXXX XXXXh
047915h			
047916h			
047917h			
047918h	CAN3 Mask Register 2	C3MKR2	XXXX XXXXh
047919h			
04791Ah			
04791Bh			
04791Ch	CAN3 Mask Register 3	C3MKR3	XXXX XXXXh
04791Dh			
04791Eh			
04791Fh			
047920h	CAN3 FIFO Receive ID Compare Register 0	C3FIDCR0	XXXX XXXXh
047921h			
047922h			
047923h			
047924h	CAN3 FIFO Receive ID Compare Register 1	C3FIDCR1	XXXX XXXXh
047925h			
047926h			
047927h			
047928h			
047929h			
04792Ah	CAN3 Mask Invalid Register	C3MKIVLR	XXXXh
04792Bh			
04792Ch			
04792Dh			
04792Eh	CAN3 Mailbox Interrupt Enable Register	C3MIER	XXXXh
04792Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.54 SFR List (54)

Address	Register	Symbol	Reset Value
047930h	CAN3 Message Control Register 0	C3MCTL0	00h
047931h	CAN3 Message Control Register 1	C3MCTL1	00h
047932h	CAN3 Message Control Register 2	C3MCTL2	00h
047933h	CAN3 Message Control Register 3	C3MCTL3	00h
047934h	CAN3 Message Control Register 4	C3MCTL4	00h
047935h	CAN3 Message Control Register 5	C3MCTL5	00h
047936h	CAN3 Message Control Register 6	C3MCTL6	00h
047937h	CAN3 Message Control Register 7	C3MCTL7	00h
047938h	CAN3 Message Control Register 8	C3MCTL8	00h
047939h	CAN3 Message Control Register 9	C3MCTL9	00h
04793Ah	CAN3 Message Control Register 10	C3MCTL10	00h
04793Bh	CAN3 Message Control Register 11	C3MCTL11	00h
04793Ch	CAN3 Message Control Register 12	C3MCTL12	00h
04793Dh	CAN3 Message Control Register 13	C3MCTL13	00h
04793Eh	CAN3 Message Control Register 14	C3MCTL14	00h
04793Fh	CAN3 Message Control Register 15	C3MCTL15	00h
047940h	CAN3 Control Register	C3CTLR	0000 0101b
047941h			0000 0000b
047942h	CAN3 Status Register	C3STR	0000 0101b
047943h			0000 0000b
047944h	CAN3 Bit Configuration Register	C3BCR	00 0000h
047945h			
047946h			
047947h	CAN3 Clock Select Register	C3CLKR	000X 0000b
047948h	CAN3 Receive FIFO Control Register	C3RFCR	1000 0000b
047949h	CAN3 Receive FIFO Pointer Control Register	C3RFPCR	XXh
04794Ah	CAN3 Transmit FIFO Control Register	C3TFCR	1000 0000b
04794Bh	CAN3 Transmit FIFO Pointer Control Register	C3TFPCR	XXh
04794Ch	CAN3 Error Interrupt Enable Register	C3EIER	00h
04794Dh	CAN3 Error Interrupt Factor Judge Register	C3EIFR	00h
04794Eh	CAN3 Receive Error Count Register	C3RECR	00h
04794Fh	CAN3 Transmit Error Count Register	C3TECR	00h
047950h	CAN3 Error Code Store Register	C3ECSR	00h
047951h	CAN3 Channel Search Support Register	C3CSSR	XXh
047952h	CAN3 Mailbox Search Status Register	C3MSSR	1000 0000b
047953h	CAN3 Mailbox Search Mode Register	C3MSMR	0000 0000b
047954h	CAN3 Time Stamp Register	C3TSR	0000h
047955h			
047956h	CAN3 Acceptance Filter Support Register	C3AFSR	XXXXh
047957h			
047958h	CAN3 Test Control Register	C3TCR	00h
047959h			
04795Ah			
04795Bh			
04795Ch to 0479FFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.55 SFR List (55)

Address	Register	Symbol	Reset Value
047A00h	CAN2 Mailbox 0: Message Identifier	C2MB0	XXXX XXXXh
047A01h			
047A02h			
047A03h			
047A04h			
047A05h	CAN2 Mailbox 0: Data Length		XXh
047A06h	CAN2 Mailbox 0: Data Field		XXXX XXXX
047A07h			XXXX XXXXh
047A08h			
047A09h			
047A0Ah			
047A0Bh			
047A0Ch			
047A0Dh			
047A0Eh	CAN2 Mailbox 0: Time Stamp		XXXXh
047A0Fh			
047A10h	CAN2 Mailbox 1: Message Identifier	C2MB1	XXXX XXXXh
047A11h			
047A12h			
047A13h			
047A14h			
047A15h	CAN2 Mailbox 1: Data Length		XXh
047A16h	CAN2 Mailbox 1: Data Field		XXXX XXXX
047A17h			XXXX XXXXh
047A18h			
047A19h			
047A1Ah			
047A1Bh			
047A1Ch			
047A1Dh			
047A1Eh	CAN2 Mailbox 1: Time Stamp		XXXXh
047A1Fh			
047A20h	CAN2 Mailbox 2: Message Identifier	C2MB2	XXXX XXXXh
047A21h			
047A22h			
047A23h			
047A24h			
047A25h	CAN2 Mailbox 2: Data Length		XXh
047A26h	CAN2 Mailbox 2: Data Field		XXXX XXXX
047A27h			XXXX XXXXh
047A28h			
047A29h			
047A2Ah			
047A2Bh			
047A2Ch			
047A2Dh			
047A2Eh	CAN2 Mailbox 2: Time Stamp		XXXXh
047A2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.56 SFR List (56)

Address	Register	Symbol	Reset Value
047A30h	CAN2 Mailbox 3: Message Identifier	C2MB3	XXXX XXXXh
047A31h			
047A32h			
047A33h			
047A34h			
047A35h	CAN2 Mailbox 3: Data Length		XXh
047A36h	CAN2 Mailbox 3: Data Field		XXXX XXXX
047A37h			XXXX XXXXh
047A38h			
047A39h			
047A3Ah			
047A3Bh			
047A3Ch			
047A3Dh			
047A3Eh	CAN2 Mailbox 3: Time Stamp		XXXXh
047A3Fh			
047A40h	CAN2 Mailbox 4: Message Identifier	C2MB4	XXXX XXXXh
047A41h			
047A42h			
047A43h			
047A44h			
047A45h	CAN2 Mailbox 4: Data Length		XXh
047A46h	CAN2 Mailbox 4: Data Field		XXXX XXXX
047A47h			XXXX XXXXh
047A48h			
047A49h			
047A4Ah			
047A4Bh			
047A4Ch			
047A4Dh			
047A4Eh	CAN2 Mailbox 4: Time Stamp		XXXXh
047A4Fh			
047A50h	CAN2 Mailbox 5: Message Identifier	C2MB5	XXXX XXXXh
047A51h			
047A52h			
047A53h			
047A54h			
047A55h	CAN2 Mailbox 5: Data Length		XXh
047A56h	CAN2 Mailbox 5: Data Field		XXXX XXXX
047A57h			XXXX XXXXh
047A58h			
047A59h			
047A5Ah			
047A5Bh			
047A5Ch			
047A5Dh			
047A5Eh	CAN2 Mailbox 5: Time Stamp		XXXXh
047A5Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.57 SFR List (57)

Address	Register	Symbol	Reset Value
047A60h	CAN2 Mailbox 6: Message Identifier	C2MB6	XXXX XXXXh
047A61h			
047A62h			
047A63h			
047A64h			
047A65h	CAN2 Mailbox 6: Data Length		XXh
047A66h	CAN2 Mailbox 6: Data Field		XXXX XXXX
047A67h			XXXX XXXXh
047A68h			
047A69h			
047A6Ah			
047A6Bh			
047A6Ch			
047A6Dh			
047A6Eh	CAN2 Mailbox 6: Time Stamp		XXXXh
047A6Fh			
047A70h	CAN2 Mailbox 7: Message Identifier	C2MB7	XXXX XXXXh
047A71h			
047A72h			
047A73h			
047A74h			
047A75h	CAN2 Mailbox 7: Data Length		XXh
047A76h	CAN2 Mailbox 7: Data Field		XXXX XXXX
047A77h			XXXX XXXXh
047A78h			
047A79h			
047A7Ah			
047A7Bh			
047A7Ch			
047A7Dh			
047A7Eh	CAN2Mailbox 7: Time Stamp		XXXXh
047A7Fh			
047A80h	CAN2 Mailbox 8: Message Identifier	C2MB8	XXXX XXXXh
047A81h			
047A82h			
047A83h			
047A84h			
047A85h	CAN2 Mailbox 8: Data Length		XXh
047A86h	CAN2 Mailbox 8: Data Field		XXXX XXXX
047A87h			XXXX XXXXh
047A88h			
047A89h			
047A8Ah			
047A8Bh			
047A8Ch			
047A8Dh			
047A8Eh	CAN2 Mailbox 8: Time Stamp		XXXXh
047A8Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.58 SFR List (58)

Address	Register	Symbol	Reset Value
047A90h	CAN2 Mailbox 9: Message Identifier	C2MB9	XXXX XXXXh
047A91h			
047A92h			
047A93h			
047A94h			
047A95h	CAN2 Mailbox 9: Data Length		XXh
047A96h	CAN2 Mailbox 9 Data Field		XXXX XXXX
047A97h			XXXX XXXXh
047A98h			
047A99h			
047A9Ah			
047A9Bh			
047A9Ch			
047A9Dh			
047A9Eh	CAN2 Mailbox 9: Time Stamp		XXXXh
047A9Fh			
047AA0h	CAN2 Mailbox 10: Message Identifier	C2MB10	XXXX XXXXh
047AA1h			
047AA2h			
047AA3h			
047AA4h			
047AA5h	CAN2 Mailbox 10: Data Length		XXh
047AA6h	CAN2 Mailbox 10: Data Field		XXXX XXXX
047AA7h			XXXX XXXXh
047AA8h			
047AA9h			
047AAAh			
047AABh			
047AACh			
047AADh			
047AAEh	CAN5 Mailbox 10: Time Stamp		XXXXh
047AAFh			
047AB0h	CAN5 Mailbox 11: Message Identifier	C2MB11	XXXX XXXXh
047AB1h			
047AB2h			
047AB3h			
047AB4h			
047AB5h	CAN2 Mailbox 11: Data Length		XXh
047AB6h	CAN2 Mailbox 11: Data Field		XXXX XXXX
047AB7h			XXXX XXXXh
047AB8h			
047AB9h			
047ABAh			
047ABBh			
047ABCh			
047ABDh			
047ABEh	CAN2 Mailbox 11: Time Stamp		XXXXh
047ABFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.59 SFR List (59)

Address	Register	Symbol	Reset Value
047AC0h	CAN2 Mailbox 12: Message Identifier	C2MB12	XXXX XXXXh
047AC1h			
047AC2h			
047AC3h			
047AC4h			
047AC5h	CAN2 Mailbox 12 Data Length		XXh
047AC6h	CAN2 Mailbox 12: Data Field		XXXX XXXX
047AC7h			XXXX XXXXh
047AC8h			
047AC9h			
047ACAh			
047ACBh			
047ACCh			
047ACDh			
047ACEh	CAN2 Mailbox 12: Time Stamp		XXXXh
047ACFh			
047AD0h	CAN2 Mailbox 13: Message Identifier	C2MB13	XXXX XXXXh
047AD1h			
047AD2h			
047AD3h			
047AD4h			
047AD5h	CAN2 Mailbox 13: Data Length		XXh
047AD6h	CAN2 Mailbox 13: Data Field		XXXX XXXX
047AD7h			XXXX XXXXh
047AD8h			
047AD9h			
047ADAh			
047ADBh			
047ADCh			
047ADDh			
047ADEh	CAN2 Mailbox 13: Time Stamp		XXXXh
047ADFh			
047AE0h	CAN2 Mailbox 14: Message Identifier	C2MB14	XXXX XXXXh
047AE1h			
047AE2h			
047AE3h			
047AE4h			
047AE5h	CAN2 Mailbox 14: Data Length		XXh
047AE6h	CAN2 Mailbox 14: Data Field		XXXX XXXX
047AE7h			XXXX XXXXh
047AE8h			
047AE9h			
047AEAh			
047AEBh			
047AECh			
047AEDh			
047AEEh	CAN5 Mailbox 14: Time Stamp		XXXXh
047AEFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.60 SFR List (60)

Address	Register	Symbol	Reset Value
047AF0h	CAN2 Mailbox 15: Message Identifier	C2MB15	XXXX XXXXh
047AF1h			
047AF2h			
047AF3h			
047AF4h			
047AF5h	CAN2 Mailbox 15: Data Length		XXh
047AF6h	CAN2 Mailbox 15: Data Field		XXXX XXXX
047AF7h			XXXX XXXXh
047AF8h			
047AF9h			
047AFAh			
047AFBh			
047AFCh			
047AFDh			
047AFEh	CAN2 Mailbox 15: Time Stamp		XXXXh
047AFFh			
047B00h to 047B0Fh			
047B10h	CAN2 Mask Register 0	C2MKR0	XXXX XXXXh
047B11h			
047B12h			
047B13h			
047B14h	CAN2 Mask Register 1	C2MKR1	XXXX XXXXh
047B15h			
047B16h			
047B17h			
047B18h	CAN2 Mask Register 2	C2MKR2	XXXX XXXXh
047B19h			
047B1Ah			
047B1Bh			
047B1Ch	CAN2 Mask Register 3	C2MKR3	XXXX XXXXh
047B1Dh			
047B1Eh			
047B1Fh			
047B20h	CAN2 FIFO Receive ID Compare Register 0	C2FIDCR0	XXXX XXXXh
047B21h			
047B22h			
047B23h			
047B24h	CAN2 FIFO Receive ID Compare Register 1	C2FIDCR1	XXXX XXXXh
047B25h			
047B26h			
047B27h			
047B28h			
047B29h			
047B2Ah	CAN2 Mask Invalid Register	C2MKIVLR	XXXXh
047B2Bh			
047B2Ch			
047B2Dh			
047B2Eh	CAN2 Mailbox Interrupt Enable Register	C2MIER	XXXXh
047B2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.61 SFR List (61)

Address	Register	Symbol	Reset Value
047B30h	CAN2 Message Control Register 0	C2MCTL0	00h
047B31h	CAN2 Message Control Register 1	C2MCTL1	00h
047B32h	CAN2 Message Control Register 2	C2MCTL2	00h
047B33h	CAN2 Message Control Register 3	C2MCTL3	00h
047B34h	CAN2 Message Control Register 4	C2MCTL4	00h
047B35h	CAN2 Message Control Register 5	C2MCTL5	00h
047B36h	CAN2 Message Control Register 6	C2MCTL6	00h
047B37h	CAN2 Message Control Register 7	C2MCTL7	00h
047B38h	CAN2 Message Control Register 8	C2MCTL8	00h
047B39h	CAN2 Message Control Register 9	C2MCTL9	00h
047B3Ah	CAN2 Message Control Register 10	C2MCTL10	00h
047B3Bh	CAN2 Message Control Register 11	C2MCTL11	00h
047B3Ch	CAN2 Message Control Register 12	C2MCTL12	00h
047B3Dh	CAN2 Message Control Register 13	C2MCTL13	00h
047B3Eh	CAN2 Message Control Register 14	C2MCTL14	00h
047B3Fh	CAN2 Message Control Register 15	C2MCTL15	00h
047B40h	CAN2 Control Register	C2CTLR	0000 0101b
047B41h			0000 0000b
047B42h	CAN2 Status Register	C2STR	0000 0101b
047B43h			0000 0000b
047B44h	CAN2 Bit Configuration Register	C2BCR	00 0000h
047B45h			
047B46h			
047B47h	CAN2 Clock Select Register	C2CLKR	000X 0000b
047B48h	CAN2 Receive FIFO Control Register	C2RFCR	1000 0000b
047B49h	CAN2 Receive FIFO Pointer Control Register	C2RFPCR	XXh
047B4Ah	CAN2 Transmit FIFO Control Register	C2TFCR	1000 0000b
047B4Bh	CAN2 Transmit FIFO Pointer Control Register	C2TFPCR	XXh
047B4Ch	CAN2 Error Interrupt Enable Register	C2EIER	00h
047B4Dh	CAN2 Error Interrupt Factor Judge Register	C2EIFR	00h
047B4Eh	CAN2 Receive Error Count Register	C2RECR	00h
047B4Fh	CAN2 Transmit Error Count Register	C2TECR	00h
047B50h	CAN2 Error Code Store Register	C2ECSR	00h
047B51h	CAN2 Channel Search Support Register	C2CSSR	XXh
047B52h	CAN2 Mailbox Search Status Register	C2MSSR	1000 0000b
047B53h	CAN2 Mailbox Search Mode Register	C2MSMR	0000 0000b
047B54h	CAN2 Time Stamp Register	C2TSR	0000h
047B55h			
047B56h	CAN2 Acceptance Filter Support Register	C2AFSR	XXXXh
047B57h			
047B58h	CAN2 Test Control Register	C2TCR	00h
047B59h			
047B5Ah			
047B5Bh			
047B5Ch to 047BFFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.62 SFR List (62)

Address	Register	Symbol	Reset Value
047C00h	CAN1 Mailbox 0: Message Identifier	C1MB0	XXXX XXXXh
047C01h			
047C02h			
047C03h			
047C04h			
047C05h	CAN1 Mailbox 0: Data Length		XXh
047C06h	CAN1 Mailbox 0: Data Field		XXXX XXXX
047C07h			XXXX XXXXh
047C08h			
047C09h			
047C0Ah			
047C0Bh			
047C0Ch			
047C0Dh			
047C0Eh	CAN1 Mailbox 0: Time Stamp		XXXXh
047C0Fh			
047C10h	CAN1 Mailbox 1: Message Identifier	C1MB1	XXXX XXXXh
047C11h			
047C12h			
047C13h			
047C14h			
047C15h	CAN1 Mailbox 1: Data Length		XXh
047C16h	CAN1 Mailbox 1: Data Field		XXXX XXXX
047C17h			XXXX XXXXh
047C18h			
047C19h			
047C1Ah			
047C1Bh			
047C1Ch			
047C1Dh			
047C1Eh	CAN1 Mailbox 1: Time Stamp		XXXXh
047C1Fh			
047C20h	CAN1 Mailbox 2: Message Identifier	C1MB2	XXXX XXXXh
047C21h			
047C22h			
047C23h			
047C24h			
047C25h	CAN1 Mailbox 2: Data Length		XXh
047C26h	CAN1 Mailbox 2: Data Field		XXXX XXXX
047C27h			XXXX XXXXh
047C28h			
047C29h			
047C2Ah			
047C2Bh			
047C2Ch			
047C2Dh			
047C2Eh	CAN1 Mailbox 2: Time Stamp		XXXXh
047C2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.63 SFR List (63)

Address	Register	Symbol	Reset Value
047C30h	CAN1 Mailbox 3: Message Identifier	C1MB3	XXXX XXXXh
047C31h			
047C32h			
047C33h			
047C34h			
047C35h	CAN1 Mailbox 3: Data Length		XXh
047C36h	CAN1 Mailbox 3: Data Field		XXXX XXXX
047C37h			XXXX XXXXh
047C38h			
047C39h			
047C3Ah			
047C3Bh			
047C3Ch			
047C3Dh			
047C3Eh	CAN1 Mailbox 3: Time Stamp		XXXXh
047C3Fh			
047C40h	CAN1 Mailbox 4: Message Identifier	C1MB4	XXXX XXXXh
047C41h			
047C42h			
047C43h			
047C44h			
047C45h	CAN1 Mailbox 4: Data Length		XXh
047C46h	CAN1 Mailbox 4: Data Field		XXXX XXXX
047C47h			XXXX XXXXh
047C48h			
047C49h			
047C4Ah			
047C4Bh			
047C4Ch			
047C4Dh			
047C4Eh	CAN1 Mailbox 4: Time Stamp		XXXXh
047C4Fh			
047C50h	CAN1 Mailbox 5: Message Identifier	C1MB5	XXXX XXXXh
047C51h			
047C52h			
047C53h			
047C54h			
047C55h	CAN1 Mailbox 5: Data Length		XXh
047C56h	CAN1 Mailbox 5: Data Field		XXXX XXXX
047C57h			XXXX XXXXh
047C58h			
047C59h			
047C5Ah			
047C5Bh			
047C5Ch			
047C5Dh			
047C5Eh	CAN1 Mailbox 5: Time Stamp		XXXXh
047C5Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.64 SFR List (64)

Address	Register	Symbol	Reset Value
047C60h	CAN1 Mailbox 6: Message Identifier	C1MB6	XXXX XXXXh
047C61h			
047C62h			
047C63h			
047C64h			
047C65h	CAN1 Mailbox 6: Data Length		XXh
047C66h	CAN1 Mailbox 6: Data Field		XXXX XXXX
047C67h			XXXX XXXXh
047C68h			
047C69h			
047C6Ah			
047C6Bh			
047C6Ch			
047C6Dh			
047C6Eh	CAN1 Mailbox 6: Time Stamp		XXXXh
047C6Fh			
047C70h	CAN1 Mailbox 7: Message Identifier	C1MB7	XXXX XXXXh
047C71h			
047C72h			
047C73h			
047C74h			
047C75h	CAN1 Mailbox 7: Data Length		XXh
047C76h	CAN1 Mailbox 7: Data Field		XXXX XXXX
047C77h			XXXX XXXXh
047C78h			
047C79h			
047C7Ah			
047C7Bh			
047C7Ch			
047C7Dh			
047C7Eh	CAN1 Mailbox 7: Time Stamp		XXXXh
047C7Fh			
047C80h	CAN1 Mailbox 8: Message Identifier	C1MB8	XXXX XXXXh
047C81h			
047C82h			
047C83h			
047C84h			
047C85h	CAN1 Mailbox 8: Data Length		XXh
047C86h	CAN1 Mailbox 8: Data Field		XXXX XXXX
047C87h			XXXX XXXXh
047C88h			
047C89h			
047C8Ah			
047C8Bh			
047C8Ch			
047C8Dh			
047C8Eh	CAN1 Mailbox 8: Time Stamp		XXXXh
047C8Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.65 SFR List (65)

Address	Register	Symbol	Reset Value
047C90h	CAN1 Mailbox 9: Message Identifier	C1MB9	XXXX XXXXh
047C91h			
047C92h			
047C93h			
047C94h			
047C95h	CAN1 Mailbox 9: Data Length		XXh
047C96h	CAN1 Mailbox 9: Data Field		XXXX XXXX
047C97h			XXXX XXXXh
047C98h			
047C99h			
047C9Ah			
047C9Bh			
047C9Ch			
047C9Dh			
047C9Eh	CAN1 Mailbox 9: Time Stamp		XXXXh
047C9Fh			
047CA0h	CAN1 Mailbox 10: Message Identifier	C1MB10	XXXX XXXXh
047CA1h			
047CA2h			
047CA3h			
047CA4h			
047CA5h	CAN1 Mailbox 10: Data Length		XXh
047CA6h	CAN1 Mailbox 10: Data Field		XXXX XXXX
047CA7h			XXXX XXXXh
047CA8h			
047CA9h			
047CAAh			
047CABh			
047CACh			
047CADh			
047CAEh	CAN1 Mailbox 10: Time Stamp		XXXXh
047CAFh			
047CB0h	CAN1 Mailbox 11: Message Identifier	C1MB11	XXXX XXXXh
047CB1h			
047CB2h			
047CB3h			
047CB4h			
047CB5h	CAN1 Mailbox 11: Data Length		XXh
047CB6h	CAN1 Mailbox 11: Data Field		XXXX XXXX
047CB7h			XXXX XXXXh
047CB8h			
047CB9h			
047CBAh			
047CBBh			
047CBCh			
047CBDh			
047CBEh	CAN1 Mailbox 11: Time Stamp		XXXXh
047CBFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.66 SFR List (66)

Address	Register	Symbol	Reset Value
047CC0h	CAN1 Mailbox 12: Message Identifier	C1MB12	XXXX XXXXh
047CC1h			
047CC2h			
047CC3h			
047CC4h			
047CC5h	CAN1 Mailbox 12: Data Length		XXh
047CC6h	CAN1 Mailbox 12: Data Field		XXXX XXXX
047CC7h			XXXX XXXXh
047CC8h			
047CC9h			
047CCAh			
047CCBh			
047CCCh			
047CCDh			
047CCEh	CAN1 Mailbox 12: Time Stamp		XXXXh
047CCFh			
047CD0h	CAN1 Mailbox 13: Message Identifier	C1MB13	XXXX XXXXh
047CD1h			
047CD2h			
047CD3h			
047CD4h			
047CD5h	CAN1 Mailbox 13: Data Length		XXh
047CD6h	CAN1 Mailbox 13: Data Field		XXXX XXXX
047CD7h			XXXX XXXXh
047CD8h			
047CD9h			
047CDAh			
047CDBh			
047CDCh			
047CDDh			
047CDEh	CAN1 Mailbox 13: Time Stamp		XXXXh
047CDFh			
047CE0h	CAN1 Mailbox 14: Message Identifier	C1MB14	XXXX XXXXh
047CE1h			
047CE2h			
047CE3h			
047CE4h			
047CE5h	CAN1 Mailbox 14: Data Length		XXh
047CE6h	CAN1 Mailbox 14: Data Field		XXXX XXXX
047CE7h			XXXX XXXXh
047CE8h			
047CE9h			
047CEAh			
047CEBh			
047CECh			
047CEDh			
047CEEh	CAN1 Mailbox 14: Time Stamp		XXXXh
047CEFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.67 SFR List (67)

Address	Register	Symbol	Reset Value
047CF0h	CAN1 Mailbox 15: Message Identifier	C1MB15	XXXX XXXXh
047CF1h			
047CF2h			
047CF3h			
047CF4h			
047CF5h	CAN1 Mailbox 15: Data Length		XXh
047CF6h	CAN1 Mailbox 15: Data Field		XXXX XXXX
047CF7h			XXXX XXXXh
047CF8h			
047CF9h			
047CFAh			
047CFBh			
047CFCh			
047CFDh			
047CFEh	CAN1 Mailbox 15: Time Stamp		XXXXh
047CFFh			
047D00h to 047D0Fh			
047D10h	CAN1 Mask Register 0	C1MKR0	XXXX XXXXh
047D11h			
047D12h			
047D13h			
047D14h	CAN1 Mask Register 1	C1MKR1	XXXX XXXXh
047D15h			
047D16h			
047D17h			
047D18h	CAN1 Mask Register 2	C1MKR2	XXXX XXXXh
047D19h			
047D1Ah			
047D1Bh			
047D1Ch	CAN1 Mask Register 3	C1MKR3	XXXX XXXXh
047D1Dh			
047D1Eh			
047D1Fh			
047D20h	CAN1 FIFO Receive ID Compare Register 0	C1FIDCR0	XXXX XXXXh
047D21h			
047D22h			
047D23h			
047D24h	CAN1 FIFO Receive ID Compare Register 1	C1FIDCR1	XXXX XXXXh
047D25h			
047D26h			
047D27h			
047D28h			
047D29h			
047D2Ah	CAN1 Mask Invalid Register	C1MKIVLR	XXXXh
047D2Bh			
047D2Ch			
047D2Dh			
047D2Eh	CAN1 Mailbox Interrupt Enable Register	C1MIER	XXXXh
047D2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.68 SFR List (68)

Address	Register	Symbol	Reset Value
047D30h	CAN1 Message Control Register 0	C1MCTL0	00h
047D31h	CAN1 Message Control Register 1	C1MCTL1	00h
047D32h	CAN1 Message Control Register 2	C1MCTL2	00h
047D33h	CAN1 Message Control Register 3	C1MCTL3	00h
047D34h	CAN1 Message Control Register 4	C1MCTL4	00h
047D35h	CAN1 Message Control Register 5	C1MCTL5	00h
047D36h	CAN1 Message Control Register 6	C1MCTL6	00h
047D37h	CAN1 Message Control Register 7	C1MCTL7	00h
047D38h	CAN1 Message Control Register 8	C1MCTL8	00h
047D39h	CAN1 Message Control Register 9	C1MCTL9	00h
047D3Ah	CAN1 Message Control Register 10	C1MCTL10	00h
047D3Bh	CAN1 Message Control Register 11	C1MCTL11	00h
047D3Ch	CAN1 Message Control Register 12	C1MCTL12	00h
047D3Dh	CAN1 Message Control Register 13	C1MCTL13	00h
047D3Eh	CAN1 Message Control Register 14	C1MCTL14	00h
047D3Fh	CAN1 Message Control Register 15	C1MCTL15	00h
047D40h	CAN1 Control Register	C1CTLR	0000 0101b
047D41h			0000 0000b
047D42h	CAN1 Status Register	C1STR	0000 0101b
047D43h			0000 0000b
047D44h	CAN1 Bit Configuration Register	C1BCR	00 0000h
047D45h			
047D46h			
047D47h	CAN1 Clock Select Register	C1CLKR	000X 0000b
047D48h	CAN1 Receive FIFO Control Register	C1RFCR	1000 0000b
047D49h	CAN1 Receive FIFO Pointer Control Register	C1RFPCR	XXh
047D4Ah	CAN1 Transmit FIFO Control Register	C1TFCR	1000 0000b
047D4Bh	CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	XXh
047D4Ch	CAN1 Error Interrupt Enable Register	C1EIER	00h
047D4Dh	CAN1 Error Interrupt Factor Judge Register	C1EIFR	00h
047D4Eh	CAN1 Receive Error Count Register	C1RECR	00h
047D4Fh	CAN1 Transmit Error Count Register	C1TECR	00h
047D50h	CAN1 Error Code Store Register	C1ECSR	00h
047D51h	CAN1 Channel Search Support Register	C1CSSR	XXh
047D52h	CAN1 Mailbox Search Status Register	C1MSSR	1000 0000b
047D53h	CAN1 Mailbox Search Mode Register	C1MSMR	0000 0000b
047D54h	CAN1 Time Stamp Register	C1TSR	0000h
047D55h			
047D56h	CAN1 Acceptance Filter Support Register	C1AFSR	XXXXh
047D57h			
047D58h	CAN1 Test Control Register	C1TCR	00h
047D59h			
047D5Ah			
047D5Bh			
047D5Ch to 047DFFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.69 SFR List (69)

Address	Register	Symbol	Reset Value
047E00h	CAN0 Mailbox 0: Message Identifier	C0MB0	XXXX XXXXh
047E01h			
047E02h			
047E03h			
047E04h			
047E05h	CAN0 Mailbox 0: Data Length		XXh
047E06h	CAN0 Mailbox 0: Data Field		XXXX XXXX
047E07h			XXXX XXXXh
047E08h			
047E09h			
047E0Ah			
047E0Bh			
047E0Ch			
047E0Dh			
047E0Eh	CAN0 Mailbox 0: Time Stamp		XXXXh
047E0Fh			
047E10h	CAN0 Mailbox 1: Message Identifier	C0MB1	XXXX XXXXh
047E11h			
047E12h			
047E13h			
047E14h			
047E15h	CAN0 Mailbox 1: Data Length		XXh
047E16h	CAN0 Mailbox 1: Data Field		XXXX XXXX
047E17h			XXXX XXXXh
047E18h			
047E19h			
047E1Ah			
047E1Bh			
047E1Ch			
047E1Dh			
047E1Eh	CAN0 Mailbox 1: Time Stamp		XXXXh
047E1Fh			
047E20h	CAN0 Mailbox 2: Message Identifier	C0MB2	XXXX XXXXh
047E21h			
047E22h			
047E23h			
047E24h			
047E25h	CAN0 Mailbox 2: Data Length		XXh
047E26h	CAN0 Mailbox 2: Data Field		XXXX XXXX
047E27h			XXXX XXXXh
047E28h			
047E29h			
047E2Ah			
047E2Bh			
047E2Ch			
047E2Dh			
047E2Eh	CAN0 Mailbox 2: Time Stamp		XXXXh
047E2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.70 SFR List (70)

Address	Register	Symbol	Reset Value
047E30h	CAN0 Mailbox 3: Message Identifier	C0MB3	XXXX XXXXh
047E31h			
047E32h			
047E33h			
047E34h			
047E35h	CAN0 Mailbox 3: Data Length		XXh
047E36h	CAN0 Mailbox 3: Data Field		XXXX XXXX
047E37h			XXXX XXXXh
047E38h			
047E39h			
047E3Ah			
047E3Bh			
047E3Ch			
047E3Dh			
047E3Eh	CAN0 Mailbox 3: Time Stamp		XXXXh
047E3Fh			
047E40h	CAN0 Mailbox 4: Message Identifier	C0MB4	XXXX XXXXh
047E41h			
047E42h			
047E43h			
047E44h			
047E45h	CAN0 Mailbox 4: Data Length		XXh
047E46h	CAN0 Mailbox 4: Data Field		XXXX XXXX
047E47h			XXXX XXXXh
047E48h			
047E49h			
047E4Ah			
047E4Bh			
047E4Ch			
047E4Dh			
047E4Eh	CAN0 Mailbox 4: Time Stamp		XXXXh
047E4Fh			
047E50h	CAN0 Mailbox 5: Message Identifier	C0MB5	XXXX XXXXh
047E51h			
047E52h			
047E53h			
047E54h			
047E55h	CAN0 Mailbox 5: Data Length		XXh
047E56h	CAN0 Mailbox 5: Data Field		XXXX XXXX
047E57h			XXXX XXXXh
047E58h			
047E59h			
047E5Ah			
047E5Bh			
047E5Ch			
047E5Dh			
047E5Eh	CAN0 Mailbox 5: Time Stamp		XXXXh
047E5Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.71 SFR List (71)

Address	Register	Symbol	Reset Value
047E60h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXXX XXXXh
047E61h			
047E62h			
047E63h			
047E64h			
047E65h	CAN0 Mailbox 6: Data Length		XXh
047E66h	CAN0 Mailbox 6: Data Field		XXXX XXXX
047E67h			XXXX XXXXh
047E68h			
047E69h			
047E6Ah			
047E6Bh			
047E6Ch			
047E6Dh			
047E6Eh	CAN0 Mailbox 6: Time Stamp		XXXXh
047E6Fh			
047E70h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXXX XXXXh
047E71h			
047E72h			
047E73h			
047E74h			
047E75h	CAN0 Mailbox 7: Data Length		XXh
047E76h	CAN0 Mailbox 7: Data Field		XXXX XXXX
047E77h			XXXX XXXXh
047E78h			
047E79h			
047E7Ah			
047E7Bh			
047E7Ch			
047E7Dh			
047E7Eh	CAN0 Mailbox 7: Time Stamp		XXXXh
047E7Fh			
047E80h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXXX XXXXh
047E81h			
047E82h			
047E83h			
047E84h			
047E85h	CAN0 Mailbox 8: Data Length		XXh
047E86h	CAN0 Mailbox 8: Data Field		XXXX XXXX
047E87h			XXXX XXXXh
047E88h			
047E89h			
047E8Ah			
047E8Bh			
047E8Ch			
047E8Dh			
047E8Eh	CAN0 Mailbox 8:Time Stamp		XXXXh
047E8Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.72 SFR List (72)

Address	Register	Symbol	Reset Value
047E90h	CAN0 Mailbox 9: Message Identifier	C0MB9	XXXX XXXXh
047E91h			
047E92h			
047E93h			
047E94h			
047E95h	CAN0 Mailbox 9: Data Length		XXh
047E96h	CAN0 Mailbox 9: Data Field		XXXX XXXX
047E97h			XXXX XXXXh
047E98h			
047E99h			
047E9Ah			
047E9Bh			
047E9Ch			
047E9Dh			
047E9Eh	CAN0 Mailbox 9: Time Stamp		XXXXh
047E9Fh			
047EA0h	CAN0 Mailbox 10: Message Identifier	C0MB10	XXXX XXXXh
047EA1h			
047EA2h			
047EA3h			
047EA4h			
047EA5h	CAN0 Mailbox 10: Data Length		XXh
047EA6h	CAN0 Mailbox 10: Data Field		XXXX XXXX
047EA7h			XXXX XXXXh
047EA8h			
047EA9h			
047EAAh			
047EABh			
047EACh			
047EADh			
047EAEh	CAN0 Mailbox 10: Time Stamp		XXXXh
047EAFh			
047EB0h	CAN0 Mailbox 11: Message Identifier	C0MB11	XXXX XXXXh
047EB1h			
047EB2h			
047EB3h			
047EB4h			
047EB5h	CAN0 Mailbox 11: Data Length		XXh
047EB6h	CAN0 Mailbox 11: Data Field		XXXX XXXX
047EB7h			XXXX XXXXh
047EB8h			
047EB9h			
047EBAh			
047EBBh			
047EBCh			
047EBDh			
047EBEh	CAN0 Mailbox 11: Time Stamp		XXXXh
047EBFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.73 SFR List (73)

Address	Register	Symbol	Reset Value
047EC0h	CAN0 Mailbox 12: Message Identifier	C0MB12	XXXX XXXXh
047EC1h			
047EC2h			
047EC3h			
047EC4h			
047EC5h	CAN0 Mailbox 12: Data Length		XXh
047EC6h	CAN0 Mailbox 12: Data Field		XXXX XXXX
047EC7h			XXXX XXXXh
047EC8h			
047EC9h			
047ECAh			
047ECBh			
047ECCh			
047ECDh			
047ECEh	CAN0 Mailbox 12: Time Stamp		XXXXh
047ECFh			
047ED0h	CAN0 Mailbox 13: Message Identifier	C0MB13	XXXX XXXXh
047ED1h			
047ED2h			
047ED3h			
047ED4h			
047ED5h	CAN0 Mailbox 13: Data Length		XXh
047ED6h	CAN0 Mailbox 13: Data Field		XXXX XXXX
047ED7h			XXXX XXXXh
047ED8h			
047ED9h			
047EDAh			
047EDBh			
047EDCh			
047EDDh			
047EDEh	CAN0 Mailbox 13: Time Stamp		XXXXh
047EDFh			
047EE0h	CAN0 Mailbox 14: Message Identifier	C0MB14	XXXX XXXXh
047EE1h			
047EE2h			
047EE3h			
047EE4h			
047EE5h	CAN0 Mailbox 14: Data Length		XXh
047EE6h	CAN0 Mailbox 14: Data Field		XXXX XXXX
047EE7h			XXXX XXXXh
047EE8h			
047EE9h			
047EEAh			
047EEBh			
047EECh			
047EEDh			
047EEEh	CAN0 Mailbox 14: Time Stamp		XXXXh
047EEFh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.74 SFR List (74)

Address	Register	Symbol	Reset Value
047EF0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXXX XXXXh
047EF1h			
047EF2h			
047EF3h			
047EF4h			
047EF5h	CAN0 Mailbox 15: Data Length		XXh
047EF6h	CAN0 Mailbox 15: Data Field		XXXX XXXX
047EF7h			XXXX XXXXh
047EF8h			
047EF9h			
047EFAh			
047EFBh			
047EFCh			
047EFDh			
047EFEh	CAN0 Mailbox 15: Time Stamp		XXXXh
047EFFh			
047F00h to 047F0Fh			
047F10h	CAN0 Mask Register 0	C0MKR0	XXXX XXXXh
047F11h			
047F12h			
047F13h			
047F14h	CAN0 Mask Register 1	C0MKR1	XXXX XXXXh
047F15h			
047F16h			
047F17h			
047F18h	CAN0 Mask Register 2	C0MKR2	XXXX XXXXh
047F19h			
047F1Ah			
047F1Bh			
047F1Ch	CAN0 Mask Register 3	C0MKR3	XXXX XXXXh
047F1Dh			
047F1Eh			
047F1Fh			
047F20h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXXX XXXXh
047F21h			
047F22h			
047F23h			
047F24h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXXX XXXXh
047F25h			
047F26h			
047F27h			
047F28h			
047F29h			
047F2Ah	CAN0 Mask Invalid Register	C0MKIVLR	XXXXh
047F2Bh			
047F2Ch			
047F2Dh			
047F2Eh	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXXXh
047F2Fh			

X: Undefined
Blanks are reserved. No access is allowed.

Table 4.75 SFR List (75)

Address	Register	Symbol	Reset Value
047F30h	CAN0 Message Control Register 0	C0MCTL0	00h
047F31h	CAN0 Message Control Register 1	C0MCTL1	00h
047F32h	CAN0 Message Control Register 2	C0MCTL2	00h
047F33h	CAN0 Message Control Register 3	C0MCTL3	00h
047F34h	CAN0 Message Control Register 4	C0MCTL4	00h
047F35h	CAN0 Message Control Register 5	C0MCTL5	00h
047F36h	CAN0 Message Control Register 6	C0MCTL6	00h
047F37h	CAN0 Message Control Register 7	C0MCTL7	00h
047F38h	CAN0 Message Control Register 8	C0MCTL8	00h
047F39h	CAN0 Message Control Register 9	C0MCTL9	00h
047F3Ah	CAN0 Message Control Register 10	C0MCTL10	00h
047F3Bh	CAN0 Message Control Register 11	C0MCTL11	00h
047F3Ch	CAN0 Message Control Register 12	C0MCTL12	00h
047F3Dh	CAN0 Message Control Register 13	C0MCTL13	00h
047F3Eh	CAN0 Message Control Register 14	C0MCTL14	00h
047F3Fh	CAN0 Message Control Register 15	C0MCTL15	00h
047F40h	CAN0 Control Register	C0CTLR	0000 0101b
047F41h			0000 0000b
047F42h	CAN0 Status Register	C0STR	0000 0101b
047F43h			0000 0000b
047F44h	CAN0 Bit Configuration Register	C0BCR	00 0000h
047F45h			
047F46h			
047F47h	CAN0 Clock Select Register	C0CLKR	000X 0000b
047F48h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
047F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
047F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
047F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
047F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
047F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
047F4Eh	CAN0 Receive Error Count Register	C0RECR	00h
047F4Fh	CAN0 Transmit Error Count Register	C0TECR	00h
047F50h	CAN0 Error Code Store Register	C0ECSR	00h
047F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
047F52h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
047F53h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
047F54h	CAN0 Time Stamp Register	C0TSR	0000h
047F55h			
047F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXXXh
047F57h			
047F58h	CAN0 Test Control Register	C0TCR	00h
047F59h			
047F5Ah			
047F5Bh			
047F5Ch			
047F5Eh			
047F5Eh			
047F5Fh			
047F60h to 04FFFFh			

X: Undefined
Blanks are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings (1)

Symbol	Characteristic		Condition	Value	Unit
V_{CC}	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.0	V
V_{CC0}	Supply voltage		$V_{CC0} \leq V_{CC}$	-0.3 to 6.0	V
AV_{CC}	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.0	V
V_I	Input voltage	XIN, $\overline{RESET}$, CNVSS, NSD, V_{REF}, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7		-0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7		-0.3 to V_{CC} + 0.3	V
P_d	Power consumption		T_a = 25°C	500	mW
			$T_a \geq$ 85°C	300	mW
—	Operating temperature range			-40 to 125	°C
T_{stg}	Storage temperature range			-65 to 150	°C

Note:

1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5.2 Operating Conditions (1/6) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
V_{CC}	Digital supply voltage		4.2	5.0	5.5	V
V_{CC0}	Digital supply voltage		3.0	3.3	V_{CC}	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{REF}	Reference voltage		4.2		V_{CC}	V
V_{SS}	Digital ground voltage			0		V
AV_{SS}	Analog ground voltage			0		V
dV_{CC}/dt	V_{CC} ramp up rate (V_{CC} < 2.0 V)		0.05		2.5	V/ms
dV_{CC0}/dt	V_{CC0} ramp up rate (V_{CC0} < 2.0 V)		0.05		2.5	V/ms
V_{IH}	High level input voltage	XIN, $\overline{RESET}$, CNVSS, NSD	0.8 × V_{CC}		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_1, P9_3 to P9_7, P10_0 to P10_7	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low level input voltage	XIN, $\overline{RESET}$, CNVSS, NSD	0		0.2 × V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7 (2), P9_1, P9_3 to P9_7, P10_0 to P10_7	0		0.3 × V_{CC}	V
T_{opr}	Operating temperature range	J version	-40		85	°C
		L version	-40		105	°C
		K version	-40		125	°C

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. V_{IH} and V_{IL} for P8_7 are specified for P8_7 as a programmable port. These values are not applicable for P8_7 as XCIN.

Table 5.3 Operating Conditions (2/6)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value (2)			Unit
			Min.	Typ.	Max.	
C_{VDC}	Decoupling capacitance for voltage regulator	Inter-pin voltage: 1.5 V	2.4		10.0	µF

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. This value should be met with due consideration to the following conditions: operating temperature, DC bias, aging, etc.

Table 5.4 Operating Conditions (3/6)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	High level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7			-10.0	mA
$I_{OH(avg)}$	High level average output current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7			-5.0	mA
$I_{OL(peak)}$	Low level peak output current (2)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7			10.0	mA
$I_{OL(avg)}$	Low level average output current (3)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7			5.0	mA

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. The following conditions should be satisfied:
   - The sum of $I_{OL(peak)}$ of ports P0, P1, P2, P8_6, P8_7, P9, and P10 is 80 mA or less.
   - The sum of $I_{OL(peak)}$ of ports P3, P4, P5, P6, P7, and P8_0 to P8_4 is 80 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P0, P1, and P2 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P8_6, P8_7, P9, and P10 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P3, P4, and P5 is -40 mA or less.
   - The sum of $I_{OH(peak)}$ of ports P6, P7, and P8_0 to P8_4 is -40 mA or less.
   - The sum of $I_{OL(peak)}$ of all ports is 80 mA or less.
   - The sum of $I_{OH(peak)}$ of all ports is -80 mA or less.
3. Average value within 100 ms.

Table 5.5 Operating Conditions (4/6)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and $T_a = T_{opr}$, unless otherwise noted) (1)

Symbol	Characteristic	Value			Unit
		Min.	Typ.	Max.	
$f_{(XIN)}$	Main clock oscillator frequency	4		8	MHz
$f_{(XRef)}$	Reference clock frequency	2		4	MHz
$f_{(PLL)}$	PLL clock oscillator frequency	96		128	MHz
$f_{(Base)}$	Base clock frequency			64	MHz
$t_{c(Base)}$	Base clock cycle time	15.625			ns
$f_{(CPU)}$	CPU operating frequency			64	MHz
$t_{C(CPU)}$	CPU clock cycle time	15.625			ns
$f_{(BCLK)}$	Peripheral bus clock operating frequency			32	MHz
$t_{C(BCLK)}$	Peripheral bus clock cycle time	31.25			ns
$f_{(PER)}$	Peripheral clock source frequency			32	MHz
$f_{(XCIN)}$	Sub clock oscillator frequency		32.768	50	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

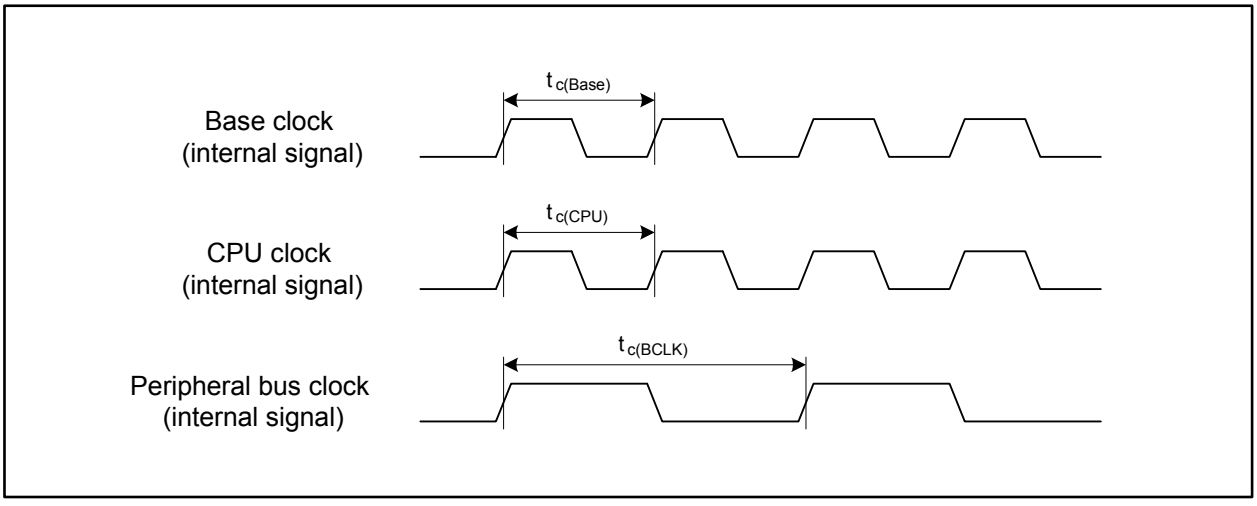


Figure 5.1 Clock Cycle Time

Table 5.6 Operating Conditions (5/6)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1, 2)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$I_{IC(H)}$	High input injection current	P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_5, P7_7, P8_0 to P8_4	$V_I > V_{CC}$			0.2	mA
$I_{IC(L)}$	Low input injection current	P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_5, P7_7, P8_0 to P8_4	$V_I < V_{SS}$			-0.2	mA
$\Sigma\|I_{IC}\|$	Total injection current					3.2	mA

Notes:
1. The device is operationally guaranteed under these operating conditions.
2. These conditions are applicable when each port is designated as input.

Table 5.7 Operating Conditions (6/6)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted) (1)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
$V_{r(VCC0)}$	Allowable ripple voltage	V_{CC0} = 5.0 V			0.5	Vp-p
		V_{CC0} = 3.3 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage gradient	V_{CC} = 5.0 V			±0.3	V/ms
$dV_{r(VCC0)}/dt$	Ripple voltage gradient	V_{CC0} = 5.0 V			±0.3	V/ms
		V_{CC0} = 3.3 V			±0.3	V/ms
$f_{r(VCC)}$	Allowable ripple frequency				10	kHz
$f_{r(VCC0)}$	Allowable ripple frequency				10	kHz

Note:
1. The device is operationally guaranteed under these operating conditions.

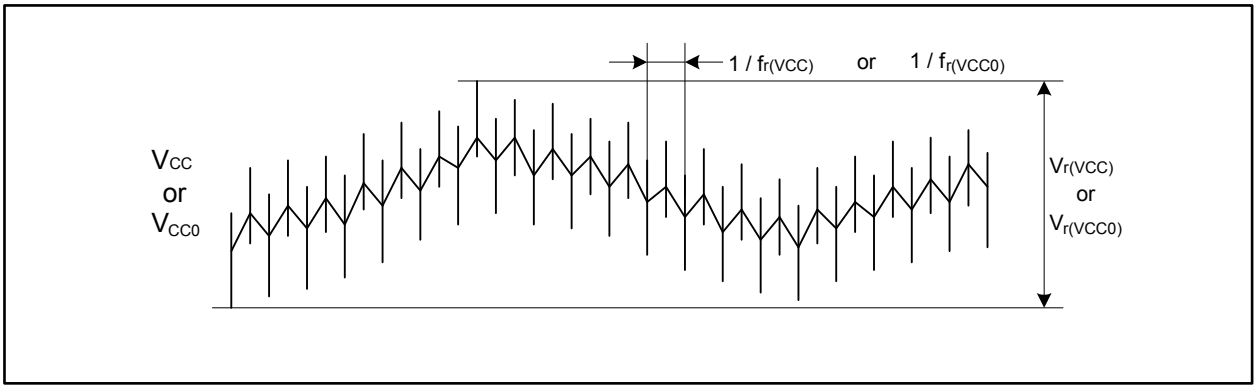


Figure 5.2 Ripple Waveform

Table 5.8 Electrical Characteristics of Flash Memory
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and Ta = T_{opr}, unless otherwise noted)

Symbol	Characteristic		Value			Unit
			Min.	Typ.	Max.	
—	Program and erase cycles (1)	Program area	100			Cycles
		Data area	100			Cycles
—	4-word program time	Program area		150	900	µs
		Data area		300	1700	µs
—	Lock bit-program time	Program area		70	500	µs
		Data area		140	1000	µs
—	Block erasure time	4-Kbyte block		0.12	3.0	s
		32-Kbyte block		0.17	3.0	s
		64-Kbyte block		0.20	3.0	s
—	Data retention (2)	T_a = 55°C (3, 4)	20			Years

Notes:
1. Program/erase definition
   This value represents the number of erasures per block.
   When the number of program and erase cycles is n, each block can be erased n times.
   For example, if a 4-word write is performed in 512 different addresses in the 4-Kbyte block A and then the block is erased, this is counted as a single program/erase operation.
   However, the same address cannot be written to more than once per erasure (overwrite disabled).
2. Data retention includes periods when no supply voltage is applied and no clock is provided.
3. This data retention includes 3000 hours in T_a = 125°C and 7000 hours in T_a = 85°C.
4. Contact a Renesas Electronics sales office for data retention times other than the above condition.

Table 5.9 Power Supply Circuit Timing Characteristics (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Internal power supply start-up stabilization time after the main power supply is turned on				2	ms

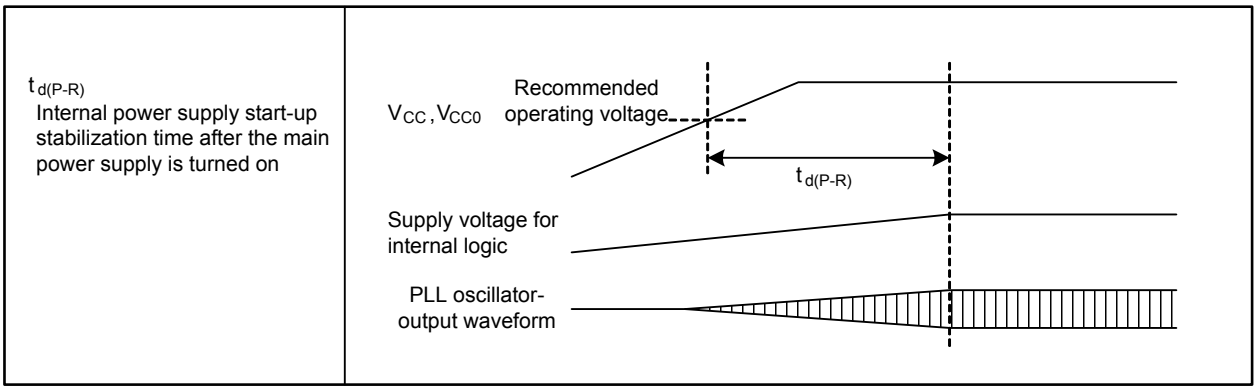


Figure 5.3 Power Supply Circuit Timing

Table 5.10 Electrical Characteristics of Voltage Regulator for Internal Logic (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
V_{VDC1}	Output voltage			1.5		V

Table 5.11 Electrical Characteristics of Oscillator (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$f_{SO(PLL)}$	PLL clock self-oscillation frequency		35	50	65	MHz
$t_{LOCK(PLL)}$	PLL lock time (1)				2	ms
$t_{jitter(p-p)}$	PLL jitter period (p-p)				2.0	ns
$f_{(OCO)}$	On-chip oscillator frequency		94	125	156	kHz

Note:
1. This value is applicable only when the main clock oscillation is stable.

Table 5.12 Electrical Characteristics of Clock Circuitry (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristics	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
$t_{rec(WAIT)}$	Recovery time from wait mode to low power mode				225	µs
$t_{rec(STOP)}$	Recovery time from stop mode (1)				225	µs

Note:
1. The stop mode recovery time does not include the main clock oscillation stabilization time. The CPU starts operating before the oscillator is stabilized.

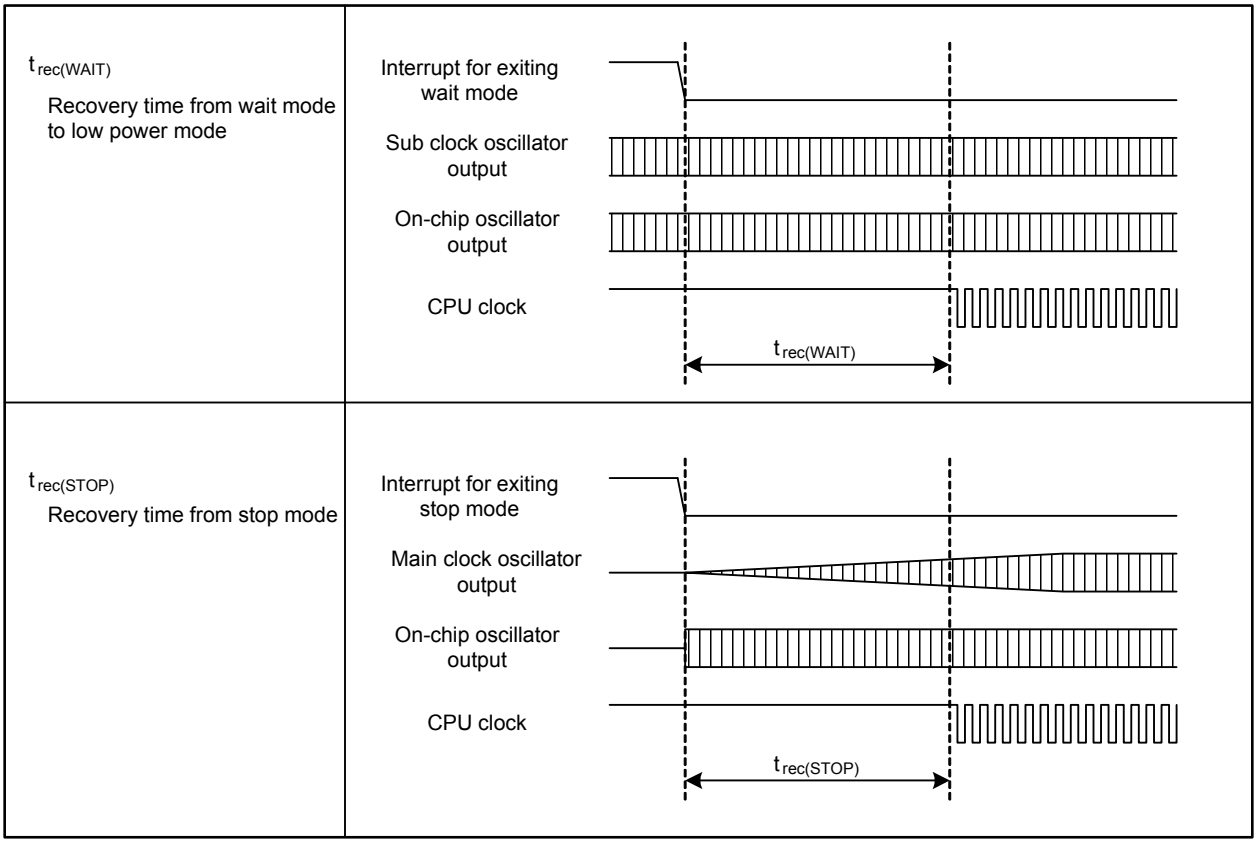


Figure 5.4 Clock Circuit Timing

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and Ta = T_{opr}, unless otherwise noted)

Table 5.13 Flash Memory CPU Rewrite Mode Timing

Symbol	Characteristics	Value		Unit
		Min.	Max.	
t_{cR}	Read cycle time	200		ns
$t_{su(S-R)}$	Chip-select setup time before read	200		ns
$t_{h(R-S)}$	Chip-select hold time after read	0		ns
$t_{su(A-R)}$	Address setup time before read	200		ns
$t_{h(R-A)}$	Address hold time after read	0		ns
$t_{w(R)}$	Read pulse width	100		ns
t_{cW}	Write cycle time	200		ns
$t_{su(S-W)}$	Chip-select setup time before write	0		ns
$t_{h(W-S)}$	Chip-select hold time after write	30		ns
$t_{su(A-W)}$	Address setup time before write	0		ns
$t_{h(W-A)}$	Address hold time after write	30		ns
$t_{w(W)}$	Write pulse width	50		ns

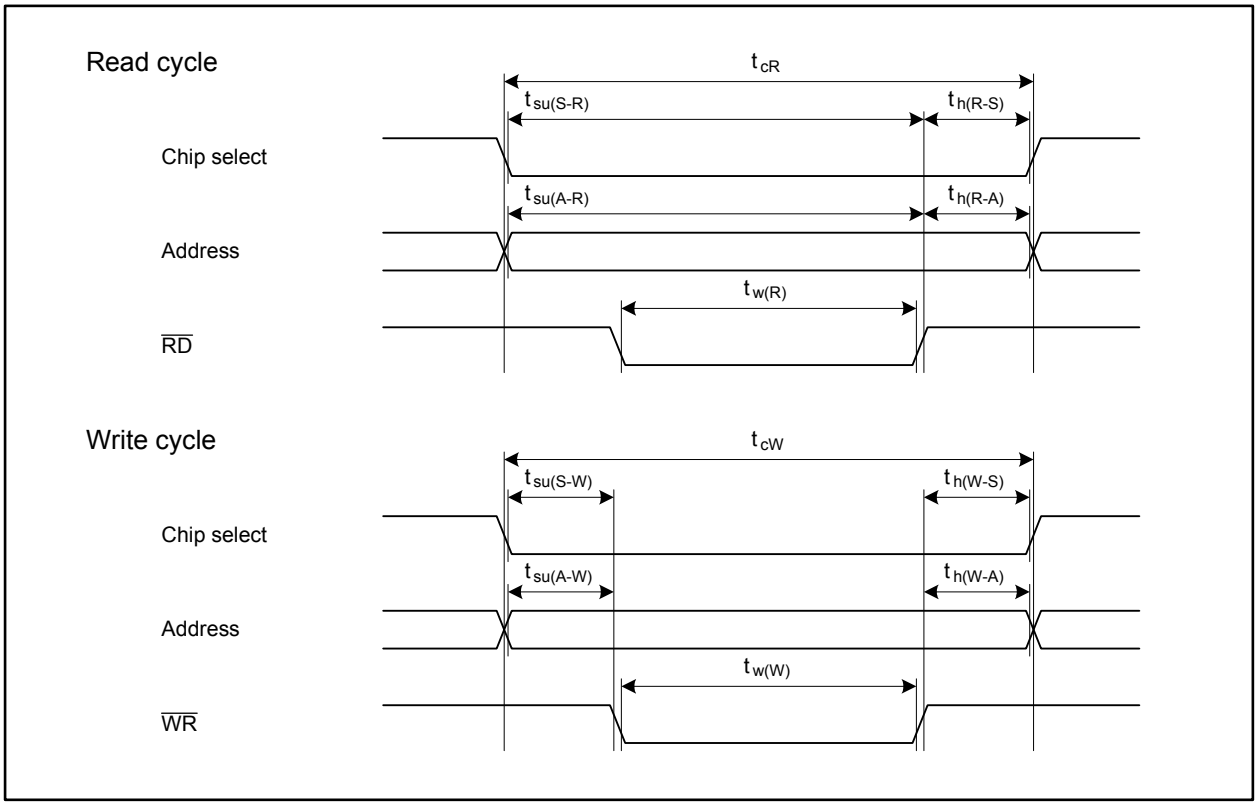


Figure 5.5 Flash Memory CPU Rewrite Mode Timing

V_{CC} = 5 V

Table 5.14 Electrical Characteristics (1/3)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
V_{OH}	High level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7	I_{OH} = -5 mA	V_{CC} - 2.0		V_{CC}	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7	I_{OH} = -200 µA	V_{CC} - 0.3		V_{CC}	V
V_{OL}	Low level output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7	I_{OL} = 5 mA			2.0	V
		P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_3 to P9_7, P10_0 to P10_7	I_{OL} = 200 µA			0.45	V

V_{CC} = 5 V

Table 5.15 Electrical Characteristics (2/3)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, T_a = T_{opr}, and $f_{(CPU)}$ = 64 MHz, unless otherwise noted)

Symbol	Characteristic		Measurement Condition	Value			Unit
				Min.	Typ.	Max.	
$V_{T+} - V_{T-}$	Hysteresis	NMI, INT0 to INT5, KI0 to KI3, TA0IN to TA4IN, TA0OUT to TA4OUT, TB0IN to TB5IN, CTS0 to CTS4, CLK0 to CLK4, RXD0 to RXD4, SCL0 to SCL2, SDA0 to SDA2, SS0 to SS2, SRXD0 to SRXD2, ADTRG, IIO0_0 to IIO0_7, IIO1_0 to IIO1_7, UD0A, UD0B, UD1A, UD1B, SCS0, SCS1, SSCK0, SSCK1, SSI0, SSI1, SSO0, SSO1, LIN0IN, LIN1IN, CAN0IN to CAN5IN, CAN0WU to CAN5WU (1)		0.2		1.0	V
		RESET		0.2		1.8	V
I_{IH}	High level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7	V_I = 5 V			1.0	µA
I_{IL}	Low level input current	XIN, RESET, CNVSS, NSD, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7	V_I = 0 V			-1.0	µA
R_{PULLUP}	Pull-up resistor	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_1, P9_3 to P9_7, P10_0 to P10_7	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistor	XIN			1.5		MΩ
R_{fXCIN}	Feedback resistor	XCIN			15		MΩ

Note:
1. Pins CAN0IN, CAN1IN, CAN4IN, CAN0WU, CAN1WU, and CAN4WU are not available in the R32C/142 Group.

V_{CC} = 5 V

Table 5.16 Electrical Characteristics (3/3)
(V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
I_{CC0} (1)	Power supply current (V_{CC0} pin)	In single-chip mode, output pins are left open and others are connected to V_{SS}	$f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, PLL, Stopped: XCIN, OCO		36	60	mA
$I_{CC(V+A)}$ (1)	Power supply current (Pins V_{CC} and AV_{cc})	XIN-XOUT Drive power: high	$f_{(CPU)}$ = 64 MHz, $f_{(BCLK)}$ = 32 MHz, $f_{(XIN)}$ = 8 MHz Active: XIN, PLL, Stopped: XCIN, OCO		10		mA
I_{CC}	Power supply current	XCIN-XCOUT Drive power: low	$f_{(CPU)}$ = $f_{SO(PLL)}$/24 MHz, Active: PLL (self-oscillation), Stopped: XIN, XCIN, OCO		7		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO		1.2		mA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown		220		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown		230		µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(XIN)}$/256 MHz, $f_{(XIN)}$ = 8 MHz, Active: XIN, Stopped: PLL, XCIN, OCO, T_a = 25°C, Wait mode		1070	2600	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = 32.768 kHz, Active: XCIN, Stopped: XIN, PLL, OCO, Main regulator: shutdown, T_a = 25°C, Wait mode		8	140	µA
			$f_{(CPU)}$ = $f_{(BCLK)}$ = $f_{(OCO)}$/4 kHz, Active: OCO, Stopped: XIN, PLL, XCIN, Main regulator: shutdown, T_a = 25°C, Wait mode		10	150	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 25°C		5	70	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 85°C			900	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 105°C			1800	µA
			Stopped: all clocks, Main regulator: shutdown, T_a = 125°C			3500	µA

Note:
1. The sum of V_{CC0} × I_{CC0} and V_{CC} × $I_{CC(V+A)}$ should be less than P_d.

V_{CC} = 5 V

Table 5.17 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = T_{opr}, and $f_{(BCLK)}$ = 32 MHz, unless otherwise noted)

Symbol	Characteristic	Measurement Condition		Value			Unit
				Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}				10	Bits
—	Absolute error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
INL	Integral non-linearity error	V_{REF} = V_{CC} = 5 V	AN_0 to AN_7, AN0_0 to AN0_7, AN2_0 to AN2_7, ANEX0, ANEX1			±3	LSB
			External op-amp connection mode			±7	LSB
DNL	Differential non-linearity error					±1	LSB
—	Offset error					±3	LSB
—	Gain error					±3	LSB
R_{LADDER}	Resistor ladder	V_{REF} = V_{CC}		4		20	kΩ
t_{CONV}	Conversion time (10 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		2.06			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.69			µs
t_{CONV}	Conversion time (8 bits)	ϕ_{AD} = 16 MHz, with sample and hold function		1.75			µs
		ϕ_{AD} = 16 MHz, without sample and hold function		3.06			µs
t_{SAMP}	Sampling time	ϕ_{AD} = 16 MHz		0.188			µs
V_{IA}	Analog input voltage			0		V_{REF}	V
ϕ_{AD}	Operating clock frequency	Without sample and hold function		0.25		16	MHz
		With sample and hold function		1		16	MHz
$R_{PU(AST)}$	Pull-up resistor for open-circuit detection			5	10	15	kΩ
$R_{PD(AST)}$	Pull-down resistor for open-circuit detection			5	10	15	kΩ

V_{CC} = 5 V

Table 5.18 D/A Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Symbol	Characteristic	Measurement Condition	Value			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute precision				1.0	%
t_S	Settling time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference input current	(1)			1.5	mA

Note:

1. One D/A converter is used. The DAi register (i = 0, 1) of the other unused converter is set to 00h. The resistor ladder for the A/D converter is not considered.
   Even when the VCUT bit in the AD0CON1 register is set to 0 (V_{REF} disconnected), I_{VREF} is supplied.

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.19 External Clock Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(X)}$	External clock input period	125	250	ns
$t_{w(XH)}$	External clock input high level pulse width	50		ns
$t_{w(XL)}$	External clock input low level pulse width	50		ns
$t_{r(X)}$	External clock input rise time		5	ns
$t_{f(X)}$	External clock input fall time		5	ns
t_W / t_C	External clock input duty	40	60	%

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.20 Timer A Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.21 Timer A Input (gating input in timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	400		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	180		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	180		ns

Table 5.22 Timer A Input (external trigger input in one-shot timer mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input clock cycle time	200		ns
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.23 Timer A Input (external trigger input in pulse-width modulation mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN input high level pulse width	80		ns
$t_{W(TAL)}$	TAiIN input low level pulse width	80		ns

Table 5.24 Timer A Input (increment/decrement switching input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT input clock cycle time	2000		ns
$t_{W(UPH)}$	TAiOUT input high level pulse width	1000		ns
$t_{W(UPL)}$	TAiOUT input low level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.25 Timer B Input (counting input in event counter mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time (one edge counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (one edge counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (one edge counting)	80		ns
$t_{c(TB)}$	TBiIN input clock cycle time (both edges counting)	200		ns
$t_{w(TBH)}$	TBiIN input high level pulse width (both edges counting)	80		ns
$t_{w(TBL)}$	TBiIN input low level pulse width (both edges counting)	80		ns

Table 5.26 Timer B Input (pulse period measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

Table 5.27 Timer B Input (pulse-width measure mode)

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input clock cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high level pulse width	180		ns
$t_{w(TBL)}$	TBiIN input low level pulse width	180		ns

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.28 Serial Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi input clock cycle time	200		ns
$t_{W(CKH)}$	CLKi input high level pulse width	80		ns
$t_{W(CKL)}$	CLKi input low level pulse width	80		ns
$t_{su(D-C)}$	RXDi input setup time	80		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

Table 5.29 A/D Trigger Input

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$t_{W(ADH)}$	$\overline{\text{ADTRG}}$ input high level pulse width Hardware trigger input high level pulse width	$\frac{3}{\phi_{AD}}$		ns
$t_{W(ADL)}$	$\overline{\text{ADTRG}}$ input low level pulse width Hardware trigger input high level pulse width	125		ns

Table 5.30 External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Characteristic		Value		Unit
			Min.	Max.	
$t_{W(INH)}$	$\overline{\text{INTi}}$ input high level pulse width (1)	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)}$ + 200		ns
$t_{W(INL)}$	$\overline{\text{INTi}}$ input low level pulse width (1)	Edge sensitive	250		ns
		Level sensitive	$t_{C(CPU)}$ + 200		ns

Note:
1. The values are applied in case the filtering function is disabled.

V_{CC} = 5 V

Timing Requirements (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.31 Serial Bus Interface

Symbol	Characteristic	Value		Unit
		Min.	Max.	
$f_{(SSCK)}$	SSCKi frequency		4	MHz
$t_{c(SSCK)}$	SSCKi clock cycle time	250		ns
$t_{w(SSCKH)}$	SSCKi input high level pulse width	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{w(SSCKL)}$	SSCKi input low level pulse width	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{r(SSCK)}$	SSCKi input rising time		1	µs
$t_{f(SSCK)}$	SSCKi input falling time		1	µs
$t_{su(SCS-SSCK)}$	SCSi input setup time	$t_{c(BCLK)}$ + 50		ns
$t_{h(SSCK-SCS)}$	SCSi input hold time	$t_{c(BCLK)}$ + 50		ns
$t_{su(SSI-SSCK)}$	SSI input setup time	80		ns
$t_{h(SSCK-SSI)}$	SSI input hold time	10		ns
$t_{su(SSO-SSCK)}$	SSO input setup time	80		ns
$t_{h(SSCK-SSO)}$	SSO input hold time	20		ns

V_{CC} = 5 V

Switching Characteristics (V_{CC} = 4.2 to 5.5 V, V_{CC0} = 3.0 V to V_{CC}, V_{SS} = 0 V, and T_a = T_{opr}, unless otherwise noted)

Table 5.32 Serial Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	Refer to Figure 5.6		80	ns
$t_{h(C-Q)}$	TXDi output hold time		0		ns

Table 5.33 Serial Bus Interface

Symbol	Characteristic	Measurement Condition	Value		Unit
			Min.	Max.	
$t_{w(SSCKH)}$	SSCKi output high level pulse width	Refer to Figure 5.6	0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{w(SSCKL)}$	SSCKi output low level pulse width		0.35 × $t_{c(SSCK)}$	0.6 × $t_{c(SSCK)}$	ns
$t_{r(SSCK)}$	SSCKi output rising time			20	ns
$t_{f(SSCK)}$	SSCKi output falling time			20	ns
$t_{d(SCS-SSCK)}$	SSCKi output delay time for SCSi			0.5 × $t_{c(SSCK)}$ + 20	ns
$t_{d(SSCK-SCS)}$	SCSi output delay time for SSCKi		0.5 × $t_{c(SSCK)}$ - 20		ns
$t_{en(SCS-SSO)}$	SSOi output enable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{dis(SCS-SSO)}$	SSOi output disable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{en(SCS-SSI)}$	SSIi output enable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{dis(SCS-SSI)}$	SSIi output disable time			1.5 × $t_{c(BCLK)}$ + 100	ns
$t_{d(SSCK-SSO)}$	SSOi output delay time for SSCKi			30	ns
$t_{d(SSCK-SSI)}$	SSIi output delay time for SSCKi			85	ns
$t_{rec(SCS)}$	SCSi output high level period in continuous transmission			0.625 × $t_{c(SSCK)}$	ns

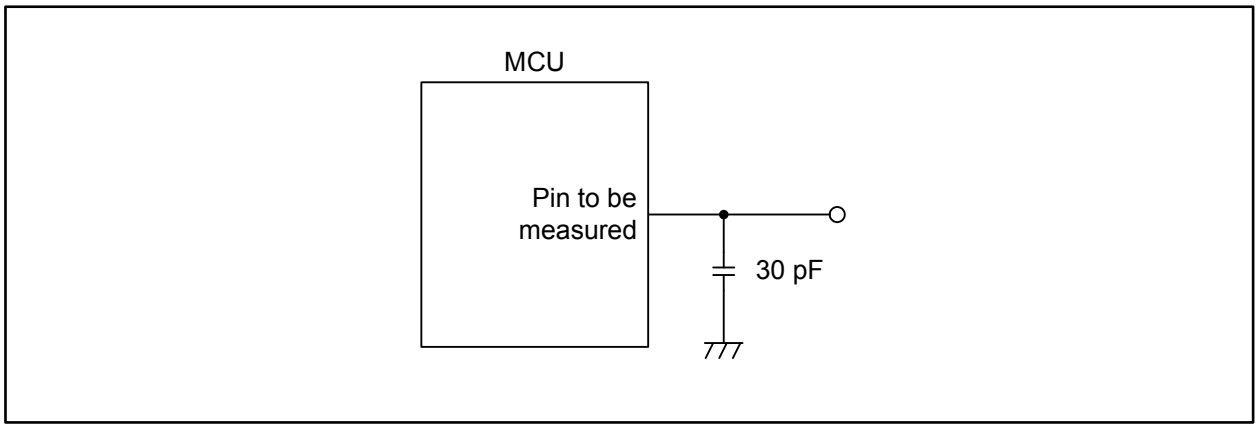


Figure 5.6 Switching Characteristic Measurement Circuit

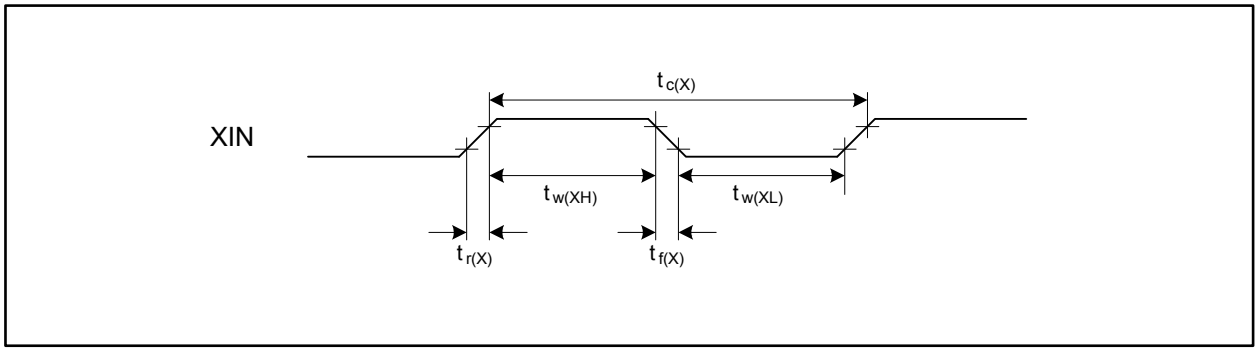


Figure 5.7 External Clock Input Timing

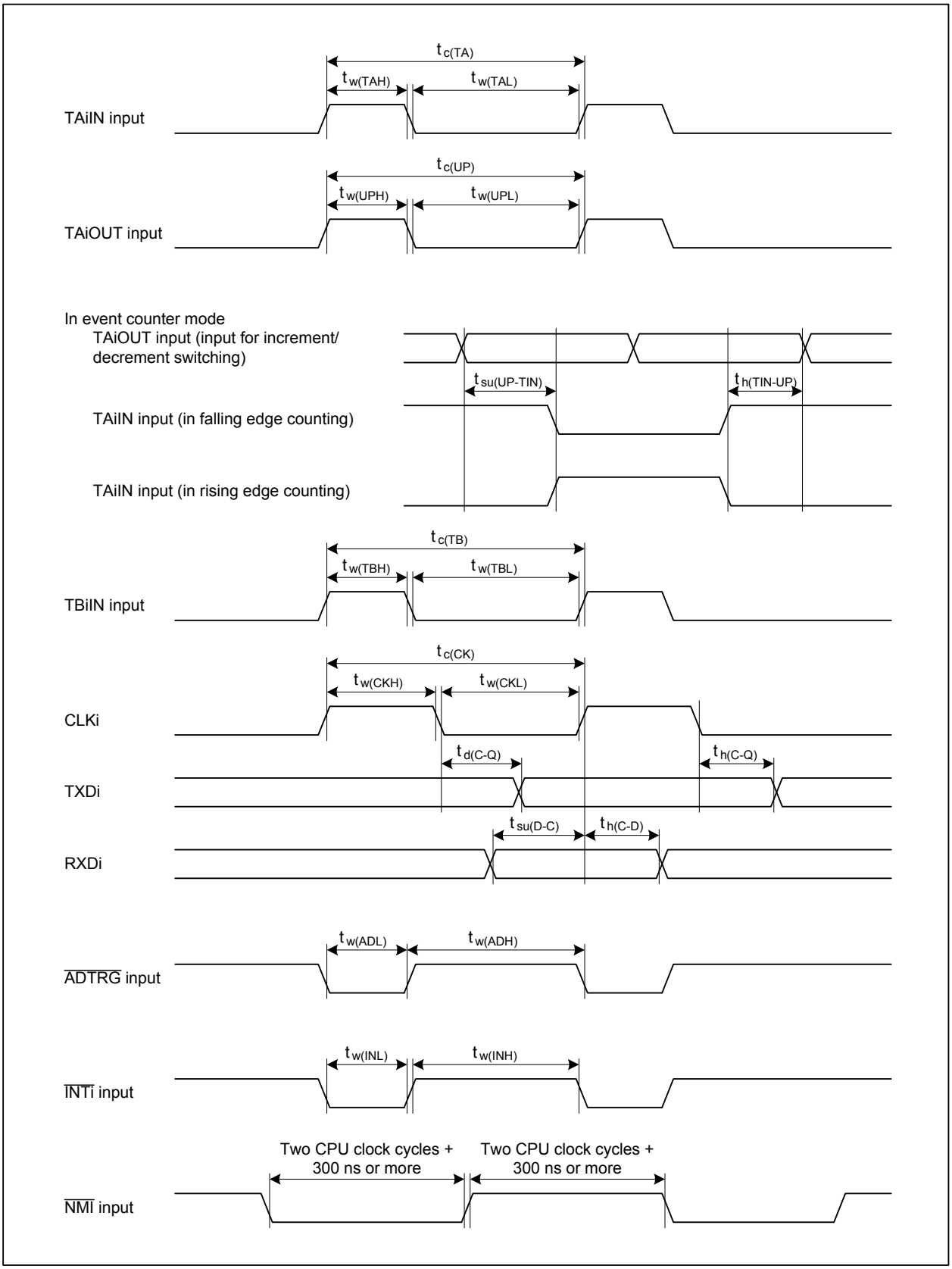


Figure 5.8 Timing of Peripheral Functions

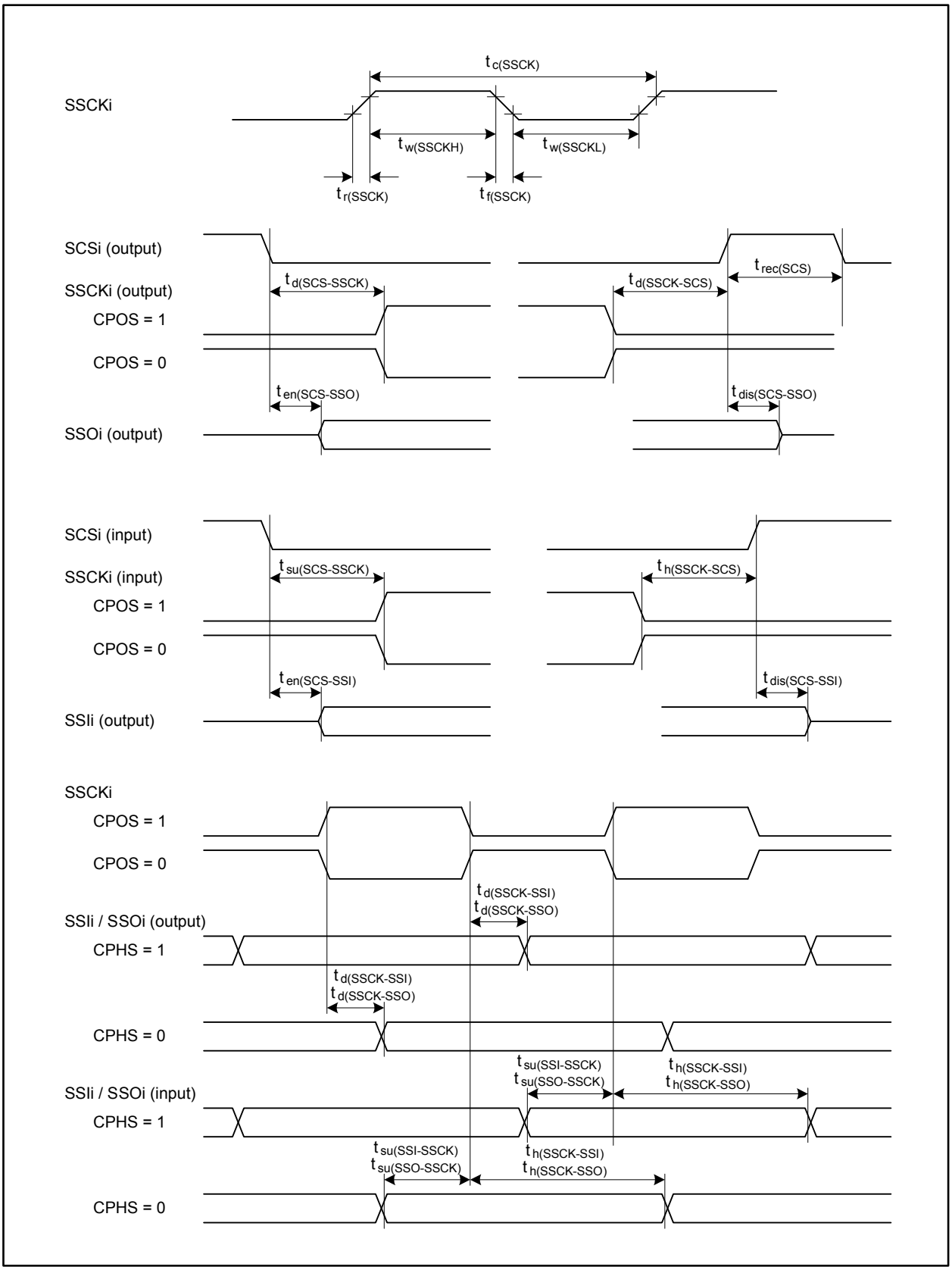
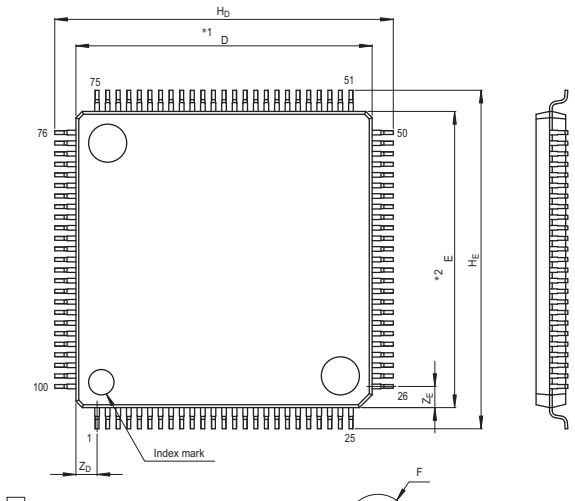
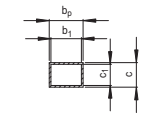


Figure 5.9 Timing of Serial Bus Interface

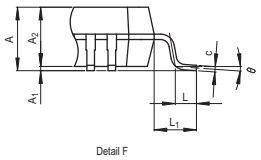
Appendix 1. Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Revision History	R32C/142 Group and R32C/145 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	Sep 09, 2011	—	Initial release

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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