RENESAS

Ultra low power 32 MHz Arm® Cortex®-M23 core, 16-KB code flash memory, 2-KB SRAM, 10-bit A/D Converter, Serial interfaces and Safety features.

Features

■ **Arm Cortex-M23 Core**
- Armv8-M architecture
- Maximum operating frequency: 32 MHz
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ **Memory**
- 16-KB code flash memory
- 2-KB SRAM
- Flash read protection (FRP)
- 128-bit unique ID

■ **Connectivity**
- Serial Array Unit (SAU)
  - Simplified SPI × 2
  - Simplified IIC × 2
  - UART × 1
  - UART (LIN-bus supported) × 1
- I^2C Bus interface (IICA) × 1

■ **Analog**
- 10-bit A/D Converter (ADC10)
- Temperature Sensor (TSN)

■ **Timers**
- 16-bit Timer Array Unit (TAU) × 8
- 32-bit interval timer (TML32) × 1
  - 1 channel in 32-bit counter mode
  - 2 channels in 16-bit counter mode
  - 4 channels in 8-bit counter mode

■ **Safety**
- Flash area protection
- ADC self-diagnosis function
- Cyclic Redundancy Check (CRC)
- Independent Watchdog Timer (IWDT)
- GPIO read-back level detection
- Register write protection
- Illegal memory access detection

■ **System and Power Management**
- Low power modes
- Data Transfer Controller (DTC)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ **Multiple Clock Sources**
- High-speed on-chip oscillator (HOCO) (32 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/LOCO
- Clock out support

■ **Up to 17 pins for general I/O ports**
- 5-V tolerance, open drain, input pull-up

■ **Operating Voltage**
- VCC: 1.6 to 5.5 V

■ **Operating Temperature and Packages**
- Ta = -40°C to +125°C
  - 20-pin TSSOP (4.4 mm × 6.5 mm, 0.65 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- 16-KB code flash memory
- 2-KB SRAM
- Serial Interface (SAU, IICA)
- General Purpose Timer (TAU, TML32)
- 10-bit A/D Converter (ADC10)

1.1 Function Outline

Table 1.1   Arm core

Feature	Functional description
Arm Cortex-M23 core	- Maximum operating frequency: up to 32 MHz - Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider - SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2   Memory

Feature	Functional description
Code flash memory	16-KB of code flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip SRAM

Table 1.3   System (1 of 2)

Feature	Functional description
Operating modes	Operating mode: Single-chip mode
Resets	The MCU provides 6 resets (RES pin reset, power-on reset, independent watchdog timer reset, voltage monitor 0/1 resets, software reset).
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of two separate voltage level detectors (LVD0, LVD1). LVD0 and LVD1 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	- High-speed on-chip oscillator (HOCO) - Low-speed on-chip oscillator (LOCO) - Clock output / Buzzer output support
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).

Table 1.3   **System (2 of 2)**

Feature	Functional description
Flash Read Protection	The MCU incorporates the flash read protection with one secure regions that include the code flash. The secure region can be protected from non-secure program accesses. A non-secure program cannot access a protected region.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with the LOCO, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4   **Direct memory access**

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.5   **Timers**

Feature	Functional description
Timer Array Unit (TAU)	The timer array unit has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be used to create a High functional timer.
32-bit Interval Timer (TML32)	The 32-bit interval timer is made up of four 8-bit interval timers (referred to as channels 0 to 3). Each is capable of operating independently and in that case they all have the same functions. Two 8-bit interval timer channels can be connected to operate as a 16-bit interval timer. Four 8-bit interval timer channels can be connected to operate as a 32-bit interval timer.

Table 1.6   **Communication interfaces**

Feature	Functional description
Serial Array Unit (SAU)	A Serial Array Unit (SAU) has one unit. Unit0 has four channels. Each channel can achieve simplified SPI, UART, or simplified IIC.
I^2C Bus Interface (IICA)	The I^2C Bus Interface (IICA) has 1 channel. The IICA module conforms I^2C (Inter-Integrated Circuit) Bus Interface functions.

Table 1.7   **Analog**

Feature	Functional description
10-bit A/D Converter (ADC10)	A 10-bit successive approximation A/D converter is provided. Up to 6 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC10 for conversion and can be further used by the end application.

Table 1.8   **Data processing**

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. Two CRC-generation polynomials (CRC-CCITT, CRC-32) are available.

Table 1.9   I/O ports

Feature	Functional description

I/O ports	● I/O ports for the 20-pin TSSOP
	  – I/O pins: 16
	  – Input pins: 1
	  – Pull-up resistors: 12
	  – N-ch open-drain outputs: 11

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.
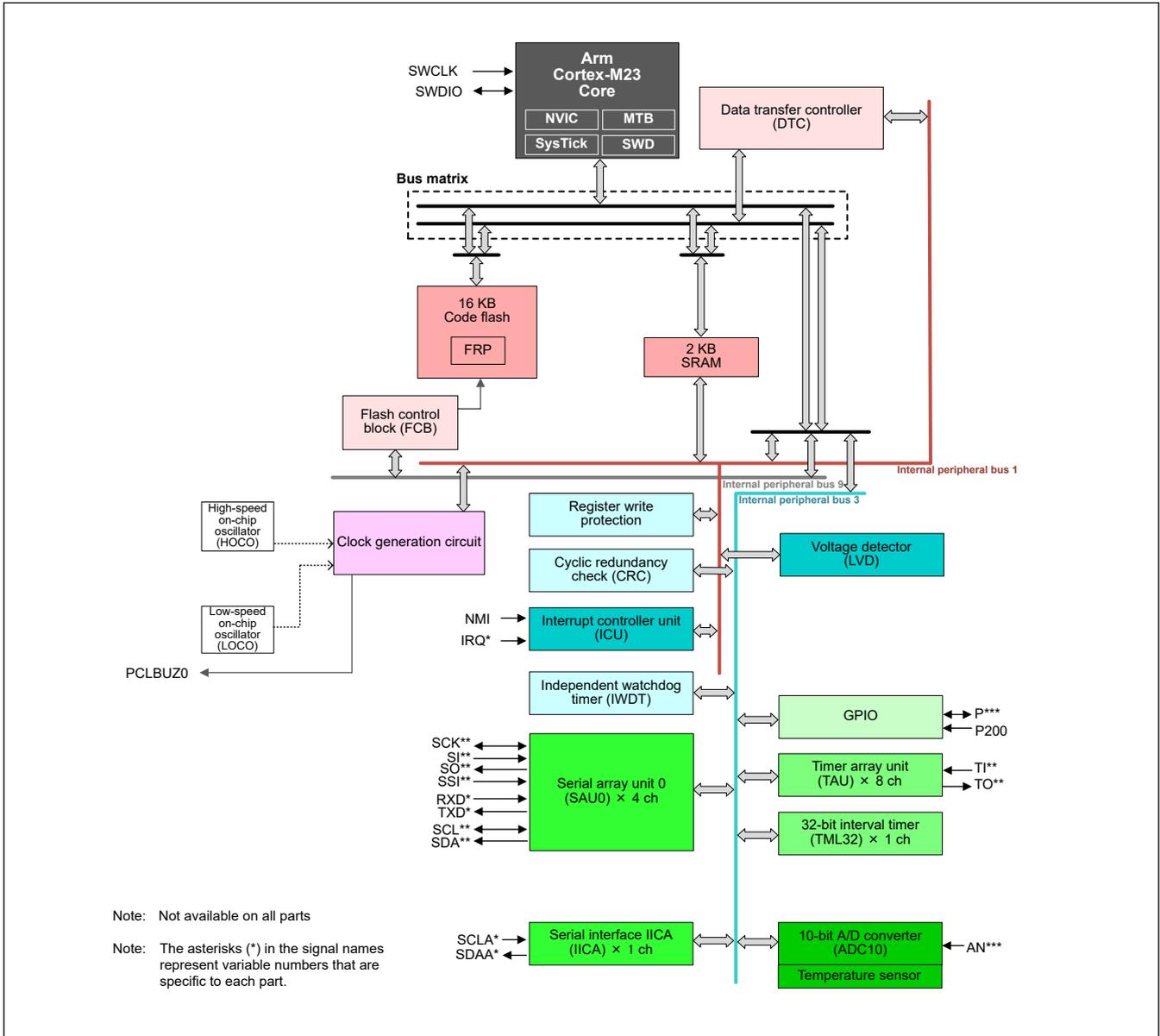

Figure 1.1   Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.10 shows a list of products.
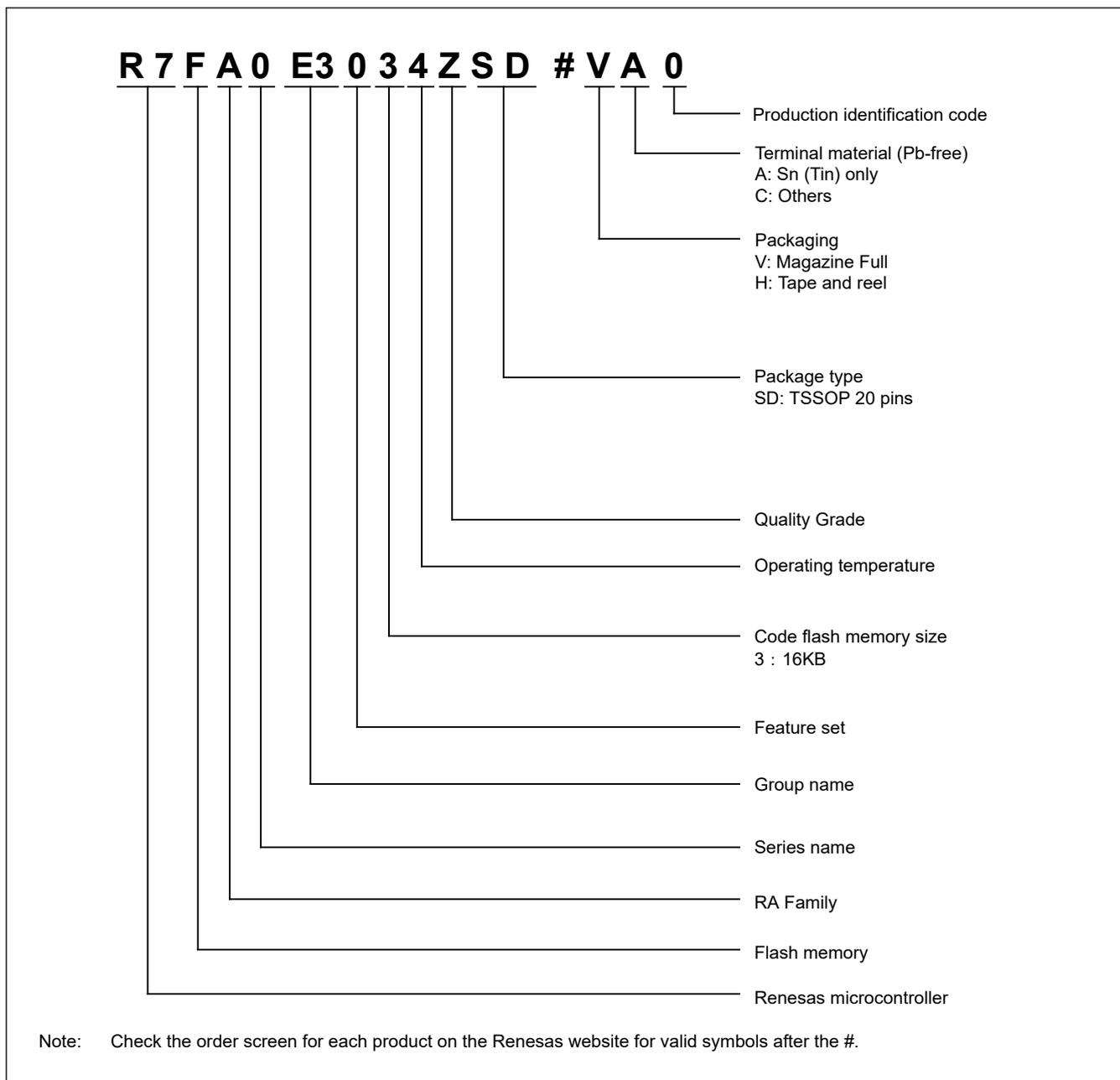
R 7 F A 0 E 3 0 3 4 Z S D # V A 0

— Production identification code

— Terminal material (Pb-free)
A: Sn (Tin) only
C: Others

— Packaging
V: Magazine Full
H: Tape and reel

— Package type
SD: TSSOP 20 pins

— Quality Grade

— Operating temperature

— Code flash memory size
3 : 16KB

— Feature set

— Group name

— Series name

— RA Family

— Flash memory

— Renesas microcontroller

Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2   Part numbering scheme

Table 1.10   Product list

Product part number	Package code	Code flash	SRAM	Operating temperature
R7FA0E3034ZSD	PTSP0020JI-A	16 KB	2 KB	-40 to +125°C

1.4 Function Comparison

Table 1.11 Function comparison

Parts number		R7FA0E3034ZSD
Pin count		20
Package		TSSOP
Code flash memory		16 KB
SRAM		2 KB
System	CPU clock	32 MHz
	ICU	Yes
DMA	DTC	Yes
Timers	TAU	8 (PWM outputs: 7)
	TML32	1 (32-bit counter mode), 2 (16-bit counter mode), 4 (8-bit counter mode)
	IWDT	Yes
Communication	SAU	2 (simplified SPI)[1], 2 (simplified IIC)[1], 1 (UART)[1], 1 (UART supporting LIN-bus)[1]
	IICA	1
Analog	ADC10	6
	TSN	Yes
Data processing	CRC	Yes
I/O ports	I/O pins	16
	Input pins	1
	Pull-up resistors	12
	N-ch open-drain outputs	11
	5-V tolerance	—

Note 1. SAU consists of several channels. Each channel can be assigned only one function at a time.

1.5 Pin Functions

Table 1.12   Pin functions

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-µF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	PCLBUZ0	Output	Clock output / Buzzer output
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ5	Input	Maskable interrupt request pins
TAU	TI00 to TI07	Input	Pins for inputting an external counting clock/capture trigger to 16-bit timers 00 to 07
	TO00 to TO07	I/O	Timer output pins for 16-bit timers 00 to 07
IICA	SCLAn (n = 0)	I/O	Input/output pins for the clock
	SDAAn (n = 0)	I/O	Input/output pins for data
SAU	SCK00, SCK11	I/O	Serial clock I/O pins for serial interfaces SPI00, SPI11
	SI00, SI11	Input	Serial data input pins for serial interfaces SPI00, SPI11
	SO00, SO11	Output	Serial data output pins for serial interfaces SPI00, SPI11
	SSI00	Input	Chip select pin for serial interfaces SPI00
	SCL00, SCL11	Output	Serial clock output pins for serial interfaces IIC00, IIC11
	SDA00, SDA11	I/O	Serial data I/O pins for serial interfaces IIC00, IIC11
	RXD0, RXD1	Input	Serial data input pins for serial interfaces UART0, UART1
	TXD0, TXD1	Output	Serial data output pins for serial interfaces UART0, UART1
Analog power supply	VREFH0	Input	Analog reference voltage supply pin for the ADC10. Connect this pin to external reference voltage or VCC.
	VREFL0	Input	Analog reference ground pin for the ADC10. Connect this pin to external reference voltage or VSS.
ADC10	AN000, AN001, AN004, AN005, AN021 to AN022	Input	Input pins for the analog signals to be processed by the A/D converter.
I/O ports	P010 to P013	I/O	General-purpose input/output pins
	P100 to P102, P108 to P110, P112	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P206, P212, P213	I/O	General-purpose input/output pins
	P300	I/O	General-purpose input/output pins

1.6   Pin Assignments

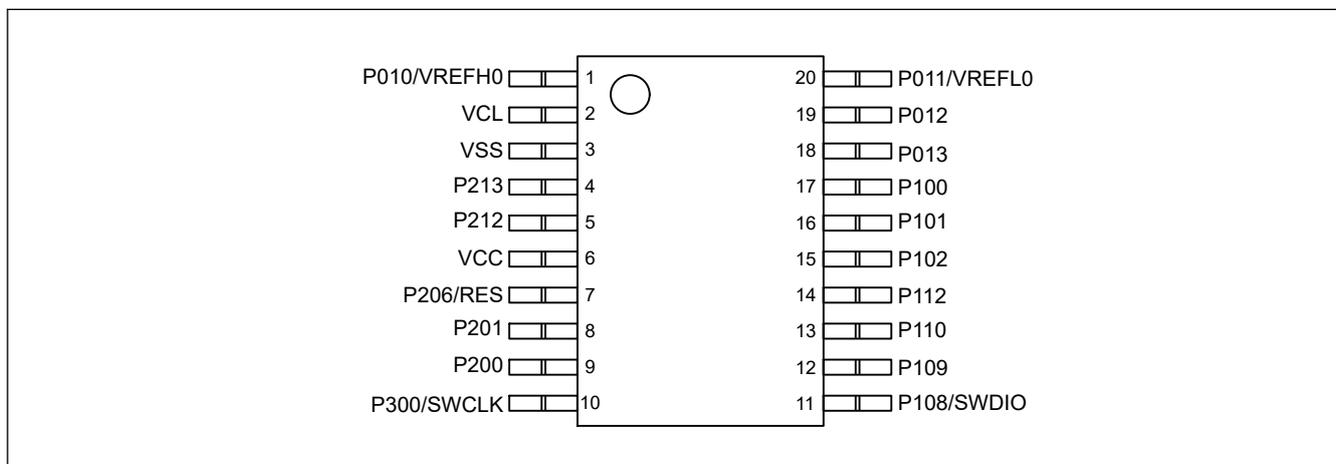Figure 1.3 shows the pin assignment from the top view.

Figure 1.3   Pin assignment for TSSOP 20-pin (top view)

1.7 Pin Lists

Table 1.13 Pin list

Pin number TSSOP 20-pin	Power, System, Clock, Debug	I/O ports	Interrupt	Timers TAU	Communication interfaces SAU	IICA	Analogs ADC
1	VREFH0	P010	—	—	—	—	AN000
2	VCL	—	—	—	—	—	—
3	VSS	—	—	—	—	—	—
4	—	P213	IRQ0_B	TI00_A/TI02_B/TO02_B	TXD1_A/SO11_A	SDAA0_B	—
5	—	P212	IRQ1_B	TO00_A/TI03_C/TO03_C	RXD1_A/SDA11_A/ SI11_A	SCLA0_B	—
6	VCC	—	—	—	—	—	—
7	RES	P206	IRQ1_C	—	—	—	—
8	PCLBUZ0_A	P201	IRQ5_B	TI05_B/TO05_B	SCL11_B/SSI00_B/ SCK11_B	—	—
9	—	P200	IRQ0_A/NMI	TI06_B	RXD1_B/SSI00_D	—	—
10	SWCLK	P300	—	TI04_B/TO04_B	TXD1_B	SDAA0_E	—
11	SWDIO/PCLBUZ0_D	P108	—	TI03_B/TO03_B	SCK00_C	SCLA0_E	—
12	—	P109	IRQ4_B	TI02_A/TO02_A	TXD0_B/SO00_B	SDAA0_C	—
13	—	P110	IRQ3_B	TI01_A/TO01_A	RXD0_B/SDA00_B/ SI00_B	SCLA0_C	—
14	—	P112	IRQ2_B	TI03_A/TO03_A	SCL00_B/SCK00_B/ SSI00_C	—	—
15	PCLBUZ0_B	P102	IRQ4_A	TI06_A/TO06_A/TO00_C	SCL00_A/SCK00_A	—	—
16	—	P101	IRQ3_A	TI07_A/TO07_A/TI00_C	TXD0_A/SO00_A	SDAA0_D	AN021
17	—	P100	IRQ2_A	TI04_A/TO04_A/TI01_B/ TO01_B	RXD0_A/SDA00_A/ SI00_A	SCLA0_D	AN022
18	—	P013	—	—	—	—	AN005
19	—	P012	—	—	—	—	AN004
20	VREFL0	P011	—	—	—	—	AN001

Note: Some signal names have _A, _B, _C, _D, or _E suffixes, but these suffixes can be ignored when assigning functionality, except for SAU and IICA. For SAU and IICA, only signals, except for SCL11, SCK11, SCK00, and SSI00, bearing the same suffix can be selected. Assigning the same function to two or more pins simultaneously is prohibited.

2.   Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC^{*1} = VREFH0 = 1.6 to 5.5 V

VSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1.   The typical condition is set to VCC = 3.3 V.
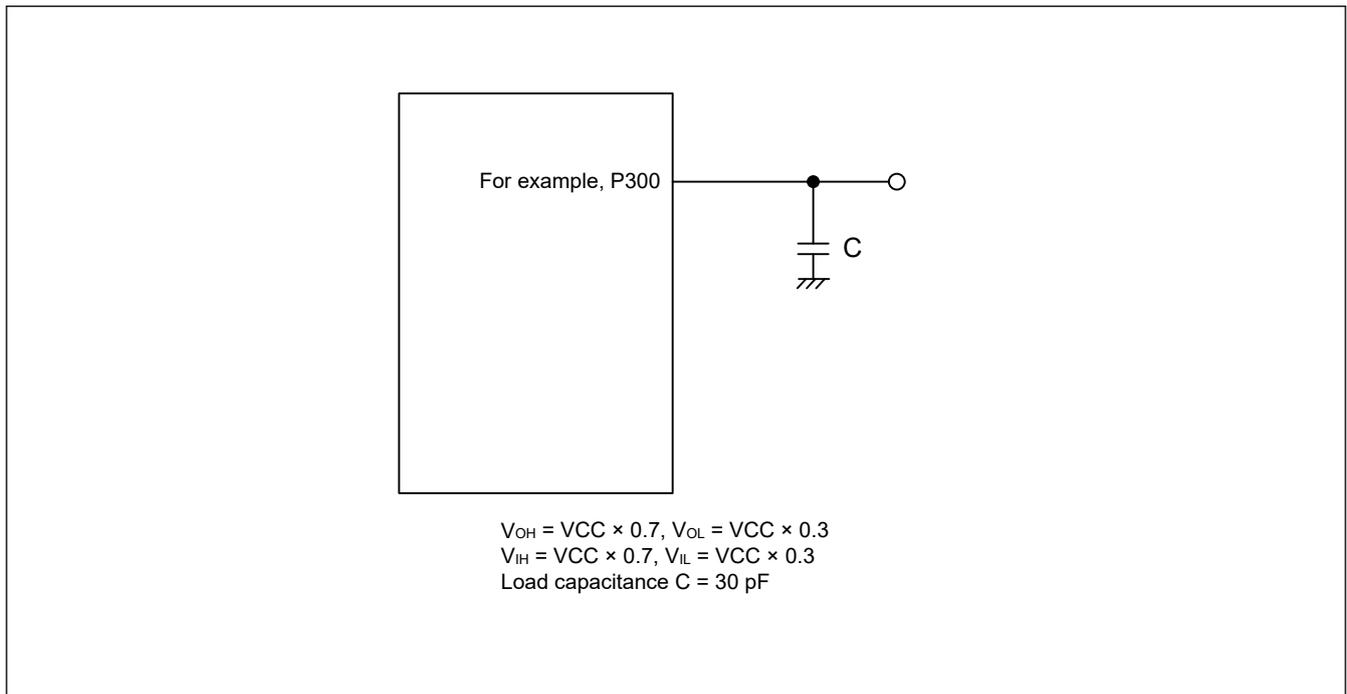
Figure 2.1 shows the timing conditions.

For example, P300

V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
Load capacitance C = 30 pF

Figure 2.1   Input or output timing measurement conditions

2.1   Absolute Maximum Ratings

Table 2.1   Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
VCL pin input voltage		V_{IVCL}	-0.3 to +2.1 and -0.3 to VCC + 0.3[*1]	V
Input voltage	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	V_{I1}	-0.3 to VCC + 0.3[*2]	V
	P010 to P013, P212, P213	V_{I2}	-0.3 to VCC + 0.3[*2]	V
Output voltage	P100 to P102, P108 to P110, P112, P201, P206, P300	V_{O1}	-0.3 to VCC + 0.3[*2]	V
	P010 to P013, P212, P213	V_{O2}	-0.3 to VCC + 0.3[*2]	V
Analog input voltage	AN000 to AN001, AN004 to AN005	V_{AI1}	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3[*2][*3]	V
	AN021 to AN022	V_{AI2}	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3[*2][*3]	V

Table 2.1   **Absolute maximum ratings (2 of 2)**

Parameter			Symbol	Value	Unit
High-level output current	P100 to P102, P108 to P110, P112, P201, P206, P300	Per pin	I_{OH1}	-40	mA
		Total of all pins		-100	mA
	P010 to P013, P212, P213	Per pin	I_{OH2}	-5	mA
		Total of all pins		-20	mA
Low-level output current	P100 to P102, P108 to P110, P112, P201, P206, P300	Per pin	I_{OL1}	40	mA
		Total of all pins		100	mA
	P010 to P013, P212, P213	Per pin	I_{OL2}	10	mA
		Total of all pins		20	mA
Ambient operating temperature	In normal operation mode		Ta	-40 to +125	°C
	In flash memory programming mode			-40 to +125	°C
Storage temperature			Tstg	-65 to +150	°C

Note 1.   Connect the VCL pin to VSS via a capacitor (0.47 to 1 µF). The listed value is the absolute maximum rating of the VCL pins. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2.   This voltage must be no higher than 6.5 V.

Note 3.   The voltage on a pin in use for A/D conversion must not exceed VREFH0 + 0.3.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note: VREFH0 refers to the positive reference voltage of the A/D converter.

Note: The reference voltage is VSS.

Caution: **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Table 2.2   **Recommended operating conditions**

Parameter	Symbol		Min.	Typ.	Max.	Unit
Power supply voltages	VCC		1.6	—	5.5	V
	VSS		—	0	—	V
Analog power supply voltages	VREFH0	When used as ADC10 Reference	1.6	—	VCC	V
	VREFL0		—	0	—	V

2.1.1   Tj/Ta Definition

Table 2.3   **Tj/Ta definition**

Conditions: Products with operating temperature Ta = -40 to +125°C

Parameter	Symbol	Typ.	Max.	Unit	Test conditions
Permissible junction temperature	Tj	—	140[*1]	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note 1.   The upper limit of operating temperature is 125°C.

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

2.2 Oscillators Characteristics

2.2.1 On-chip Oscillators Characteristics

Table 2.4   On-chip oscillators characteristics

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
High-speed on-chip oscillator clock frequency		f_{HOCO}	1	—	32	MHz	—
High-speed on-chip oscillator clock frequency accuracy	OSCSF.HOCOSF = 1	—	-1.0	—	+1.0	%	Ta = -40 to +125°C, 1.6 V ≤ VCC ≤ 5.5 V
High-speed on-chip oscillator clock frequency trimming resolution		—	—	0.05	—	%	—
High-speed on-chip oscillator clock oscillation stabilization time[3]		t_{HOCO}	—	—	4.4	µs	—
Low-speed on-chip oscillator clock frequency[1]		f_{LOCO}	—	32.768	—	kHz	—
Low-speed on-chip oscillator clock frequency accuracy		—	-15	—	15	%	—
Low-speed on-chip oscillator clock frequency trimming resolution		—	—	0.3	—	%	—
Low-speed on-chip oscillator clock oscillation stabilization time		t_{LOCO}	—	—	100	µs	—
Low-speed on-chip oscillator frequency temperature coefficient		—	—	—	±0.21[2]	%/°C	—

Note 1.   The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.
Note 2.   These values are the results of characteristic evaluation and are not checked for shipment.
Note 3.   Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

2.3 DC Characteristics

2.3.1 Pin Characteristics

Table 2.5   I/O I_{OH}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Allowable high-level output current[1]	Per pin for P100 to P102, P108 to P110, P112, P201, P206, P300	I_{OH1}	—	—	-10[2]	mA	1.6 V ≤ VCC ≤ 5.5 V
	Total of all pins (when duty ≤ 70%[3])		—	—	-80[4]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-19	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-10	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V
	Per pin for P010 to P013, P212, P213	I_{OH2}	—	—	-3[2]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-1[2]	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-1[2]	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-0.5[2]	mA	1.6 V ≤ VCC < 1.8 V
	Total of all pins (when duty ≤ 70%[3])		—	—	-20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	-10	mA	2.7 V ≤ VCC < 4.0 V
			—	—	-5	mA	1.8 V ≤ VCC < 2.7 V
			—	—	-5	mA	1.6 V ≤ VCC < 1.8 V

Note 1.   Device operation is guaranteed at the listed currents even if current is flowing from the VCC pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.
Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = $(I_{OH} × 0.7)/(n × 0.01)$
  Example when n = 80% and I_{OH} = -10.0 mA
  Total output current from the listed pins = $(-10.0 × 0.7)/(80 × 0.01) = -8.75$ mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -50 mA with an ambient operating temperature range of 85°C to 125°C.

Note: The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.

P100 to P102, P108 to P110, P112, P201, P212, P213, P300

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.6   I/O I_{OL}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Allowable low-level output current[1]	Per pin for P100 to P102, P108 to P110, P112, P201, P206, P300	I_{OL1}	—	—	20[2]	mA	—
	Total of all pins (when duty ≤ 70%[3])		—	—	80[4]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	35	mA	2.7 V ≤ VCC < 4.0 V
			—	—	20	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V
	Per pin for P010 to P013, P212, P213	I_{OL2}	—	—	8.5[2]	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	1.5[2]	mA	2.7 V ≤ VCC < 4.0 V
			—	—	0.6[2]	mA	1.8 V ≤ VCC < 2.7 V
			—	—	0.4[2]	mA	1.6 V ≤ VCC < 1.8 V
	Total of all pins (when duty ≤ 70%[3])		—	—	20	mA	4.0 V ≤ VCC ≤ 5.5 V
			—	—	20	mA	2.7 V ≤ VCC < 4.0 V
			—	—	15	mA	1.8 V ≤ VCC < 2.7 V
			—	—	10	mA	1.6 V ≤ VCC < 1.8 V

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to VSS pin.
Note 2. The combination of these and other pins must also not exceed the value for maximum total current.
Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = $(I_{OL} × 0.7)/(n × 0.01)$
  Example when n = 80% and I_{OL} = 10.0 mA
  Total output current from the listed pins = $(10.0 × 0.7)/(80 × 0.01) = 8.75$ mA
  Note that the duty cycle has no effect on the current that is allowed to flow into a single pin.
  A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is 40 mA with an ambient operating temperature range of 85°C to 125°C.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.7   I/O V_{IH}, V_{IL}

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input voltage, high	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	Normal input buffer	V_{IH1}	VCC × 0.8	—	VCC	V	—
	P100 to P102, P108 to P110, P112, P201, P300	TTL input buffer	V_{IH2}	2.2	—	VCC	V	4.0 V ≤ VCC ≤ 5.5 V
				2.0	—	VCC	V	3.3 V ≤ VCC < 4.0 V
				1.5	—	VCC	V	1.6 V ≤ VCC < 3.3 V
	P010 to P013		V_{IH3}	VCC × 0.7	—	VCC	V	—
	P212 to P213		V_{IH4}	VCC × 0.8	—	VCC	V	—
Input voltage, low	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	Normal input buffer	V_{IL1}	0	—	VCC × 0.2	V	—
	P100 to P102, P108 to P110, P112, P201, P300	TTL input buffer	V_{IL2}	0	—	0.8	V	4.0 V ≤ VCC ≤ 5.5 V
				0	—	0.5	V	3.3 V ≤ VCC < 4.0 V
				0	—	0.32	V	1.6 V ≤ VCC < 3.3 V
	P010 to P013		V_{IL3}	0	—	VCC × 0.3	V	—
	P212 to P213		V_{IL4}	0	—	VCC × 0.2	V	—

Note: The maximum value of V_{IH} of pins P100 to P102, P108 to P110, P112, P201, P212, P213, P300 is VCC, even in the N-ch open-drain mode.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.8   I/O V_{OH}, V_{OL} (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Output voltage, high	P100 to P102, P108 to P110, P112, P201, P206, P300	V_{OH1}	VCC - 1.5	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -10 mA
			VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -3 mA
			VCC - 0.6	—	—	V	2.7 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -2 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1.5 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC ≤ 5.5 V $I_{OH}1$ = -1 mA
	P010 to P013, P212, P213	V_{OH2}	VCC - 0.7	—	—	V	4.0 V ≤ VCC ≤ 5.5 V $I_{OH}2$ = -3 mA
			VCC - 0.5	—	—	V	2.7 V ≤ VCC < 4.0 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.8 V ≤ VCC < 2.7 V $I_{OH}2$ = -1 mA
			VCC - 0.5	—	—	V	1.6 V ≤ VCC < 1.8 V $I_{OH}2$ = -0.5 mA

Table 2.8   I/O V$_{OH}$, V$_{OL}$ (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Output voltage, low	P100 to P102, P108 to P110, P112, P201, P206, P300	V$_{OL1}$	—	—	1.3	V	4.0 V ≤ VCC ≤ 5.5 V I$_{OL}$1 = 20 mA
			—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V I$_{OL}$1 = 8.5 mA
			—	—	0.6	V	2.7 V ≤ VCC ≤ 5.5 V I$_{OL}$1 = 3 mA
			—	—	0.4	V	2.7 V ≤ VCC ≤ 5.5 V I$_{OL}$1 = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC ≤ 5.5 V I$_{OL}$1 = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC ≤ 5.5 V I$_{OL}$1 = 0.3 mA
	P010 to P013, P212, P213	V$_{OL2}$	—	—	0.7	V	4.0 V ≤ VCC ≤ 5.5 V I$_{OL}$2 = 8.5 mA
			—	—	0.5	V	2.7 V ≤ VCC < 4.0 V I$_{OL}$2 = 1.5 mA
			—	—	0.4	V	1.8 V ≤ VCC < 2.7 V I$_{OL}$2 = 0.6 mA
			—	—	0.4	V	1.6 V ≤ VCC < 1.8 V I$_{OL}$2 = 0.4 mA

Note: P100 to P102, P108 to P110, P112, P201, P212, P213, P300 do not output high-level signals in the N-ch open-drain mode.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Table 2.9   I/O other characteristics

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current, high	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	I$_{LIH1}$	—	—	1	µA	V$_I$ = VCC
	P010 to P013	I$_{LIH2}$	—	—	1	µA	V$_I$ = VCC
	P212 to P213	I$_{LIH3}$	—	—	1	µA	V$_I$ = VCC
Input leakage current, low	P100 to P102, P108 to P110, P112, P200, P201, P206, P300	I$_{LIL1}$	—	—	-1	µA	V$_I$ = VSS
	P010 to P013	I$_{LIL2}$	—	—	-1	µA	V$_I$ = VSS
	P212 to P213	I$_{LIL3}$	—	—	-1	µA	V$_I$ = VSS
On-chip pull-up resistance	P100 to P102, P108 to P110, P112, P201, P206, P300	R$_U$	10	20	100	kΩ	V$_I$ = VSS In input port
Input capacitance	P200	Cin	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	Other input pins		—	—	15		

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter					Symbol	Typ.[*4]	Max.	Unit	Test Conditions
Supply current[*1]	High-speed mode[*2]	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 32 MHz	Icc	2.6	—	mA	—
			All peripheral clocks enabled, CoreMark code executing from flash[*5]	ICLK = 32 MHz		—	3.5		—
		Sleep mode	All peripheral clocks disabled	ICLK = 32 MHz		0.82	—		—
			All peripheral clocks enabled[*5]	ICLK = 32 MHz		—	1.4		—
	Middle-speed mode[*2]	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 16 MHz		1.5	—		—
				ICLK = 8 MHz		0.9	—		—
				ICLK = 4 MHz		0.70	—		—
			All peripheral clocks enabled, CoreMark code executing from flash[*5]	ICLK = 16 MHz		—	2.0		—
				ICLK = 8 MHz		—	1.3		—
				ICLK = 4 MHz		—	0.9		—
		Sleep mode	All peripheral clocks disabled	ICLK = 16 MHz		0.61	—		—
				ICLK = 8 MHz		0.50	—		—
				ICLK = 4 MHz		0.44	—		—
			All peripheral clocks enabled[*5]	ICLK = 16 MHz		—	0.9		—
				ICLK = 8 MHz		—	0.7		—
				ICLK = 4 MHz		—	0.6		—
	Low-speed mode[*2]	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash	ICLK = 2 MHz		450	—	µA	—
			All peripheral clocks enabled, CoreMark code executing from flash[*5]	ICLK = 2 MHz		—	600		—
		Sleep mode	All peripheral clocks disabled	ICLK = 2 MHz		324	—		—
			All peripheral clocks enabled[*5]	ICLK = 2 MHz		—	448		—

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter						Symbol	Typ.[4]	Max.	Unit	Test Conditions
Supply current[1]	Subosc-speed mode[3]	Normal mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C	Icc	2.8	—	µA	—
					Ta = 25°C		3.0	—		
					Ta = 50°C		3.2	—		
					Ta = 70°C		3.3	—		
					Ta = 85°C		3.6	—		
					Ta = 105°C		4.2	—		
					Ta = 125°C		5.5	—		
			Peripheral clocks enabled[6]	ICLK = 32.768 kHz	Ta = -40°C		—	6.0		
					Ta = 25°C		—	6.2		
					Ta = 50°C		—	9.2		
					Ta = 70°C		—	12.6		
					Ta = 85°C		—	15.9		
					Ta = 105°C		—	21.7		
					Ta = 125°C		—	42.0		
		Sleep mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C		0.8	—		—
					Ta = 25°C		0.9	—		
					Ta = 50°C		1.0	—		
					Ta = 70°C		1.1	—		
					Ta = 85°C		1.3	—		
					Ta = 105°C		1.7	—		
					Ta = 125°C		2.9	—		
			Peripheral clocks enabled[6]	ICLK = 32.768 kHz	Ta = -40°C		—	3.6		
					Ta = 25°C		—	3.8		
					Ta = 50°C		—	6.2		
					Ta = 70°C		—	9.3		
					Ta = 85°C		—	12.6		
					Ta = 105°C		—	18.7		
					Ta = 125°C		—	38.5		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is high-speed on-chip oscillator (HOCO).
Note 3. The clock source is LOCO.
Note 4. VCC = 3.3 V.
Note 5. Includes operating current for PCLBUZ, TAU, SAU, and IICA functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 2.12.
Note 6. Includes operating current for PCLBUZ, TAU and SAU functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 2.12.

Table 2.11   Operating and standby current (2)

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Typ.[3]	Max.	Unit	Test conditions
Supply current[1]	Software Standby mode[2]	Peripheral modules stop	Ta = -40°C	Icc	0.2	0.9	µA	—
			Ta = 25°C		0.2	0.9		
			Ta = 50°C		0.3	2.2		
			Ta = 70°C		0.4	4.7		
			Ta = 85°C		0.5	8.1		
			Ta = 105°C		1.1	17		
			Ta = 125℃		2.3	35		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.

Table 2.12   Peripheral Functions Supply current

Conditions: VCC = 1.6 to 5.5 V

Parameter				Symbol	Typ.[10]	Max.	Unit	Test conditions
Peripheral Functions Supply current[1]	High-speed on chip oscillator operating current[1]		OFS1.HOCOFRQ1[2:0] are 010b	I_{HOCO}	320	—	µA	—
	Low-speed on chip oscillator operating current[1]			I_{LOCO}	0.24	—	µA	—
	32-bit interval timer operating current[1][2][3]			I_{IT}	0.06	—	µA	—
	Independent watchdog timer operating current[1][2][4]		f_{LOCO} = 32.768 kHz (typ.)	I_{IWDT}	0.03	—	µA	—
	A/D converter operating current[1][5]	When conversion at maximum speed	Normal mode, VREFH0 = VCC = 5.0 V	I_{ADC}	1.3	1.7	mA	—
			Low voltage mode, VREFH0 = VCC = 3.0 V		0.5	0.7	mA	—
	A/D converter internal reference voltage current[1]			I_{ADREF}	100	—	µA	—
	Temperature sensor operating current[1]			I_{TMPS}	100	—	µA	—
	LVD operating current[1]	LVD0 is enabled[7]		I_{LVD0}	0.03	—	µA	—
		LVD1 is enabled[8]		I_{LVD1}	0.03	—	µA	—
	Self-programming operating current[1][9]			I_{FSP}	—	12.2	mA	—
	DTC	Data transfer to RAM		I_{DTC}	1.82	—	mA	—

Note 1.   This current flows into V_{CC}.
Note 2.   The listed currents apply when the high-speed on-chip oscillator (HOCO) is stopped.
Note 3.   This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator (LOCO).
         The supply current of the RA0 microcontrollers is the sum of either Icc and I_{IT}.
         When the low-speed on-chip oscillator (LOCO) is selected, I_{LOCO} should be included in the supply current.
Note 4.   This current only flows to the independent watchdog timer. It does not include the operating current of the low-speed on-chip oscillator (LOCO) .
         The supply current of the RA0 microcontrollers is the sum of either Icc, I_{IWDT} and I_{LOCO}.
Note 5.   This current only flows to the A/D converter. The supply current of the RA0 microcontrollers is the sum of Icc and I_{ADC} when the A/D converter is operating or in the SLEEP mode.
Note 6.   This current flows into VREFH0.
Note 7.   This current only flows to the LVD0 circuit. The supply current of the RA0 microcontrollers is the sum of Icc and I_{LVD0} when the LVD0 circuit is in operation.
Note 8.   This current only flows to the LVD1 circuit. The supply current of the RA0 microcontrollers is the sum of Icc and I_{LVD1} when the LVD1 circuit is in operation.
Note 9.   This current only flows during self programming.
Note 10. VCC = 3.3 V.

2.3.3 Thermal Characteristics

The maximum value of junction temperature (Tj) must not exceed the value specified in the

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption

- Tj = Tt + Ψjt × Total power consumption
  Tj : Junction Temperature (°C)
  Ta : Ambient Temperature (°C)
  Tt : Top Center Case Temperature (°C)
  θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)

- Total power consumption = Voltage × (Leakage current + Dynamic current)

- Leakage current of IO = Σ (I_{OL} × V_{OL}) / Voltage + Σ ($|I_{OH}|$ × $|VCC – V_{OH}|$) / Voltage

- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage
  Cin: Input capacitance
  Cload: Output capacitance

Regarding θja and Ψjt, see Table 2.13.

Table 2.13   Thermal resistance

Parameter	Package	Symbol	Value[1]	Unit	Test condition
Thermal resistance	20-pin TSSOP	θja	76.0	°C/W	JESD 51-2 and 51-7 compliant
	20-pin TSSOP	Ψjt	2.95	°C/W	JESD 51-2 and 51-7 compliant

Note 1.   The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.4   AC Characteristics

Table 2.14   AC characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Instruction cycle (minimum instruction execution time)	Main system clock (FMAIN) operation	High-speed mode	T_{CY}	0.03125	—	1	µs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	µs	1.6 V ≤ VCC < 1.8 V
		Middle-speed mode		0.0625	—	1	µs	1.8 V ≤ VCC ≤ 5.5 V
				0.25	—	1	µs	1.6 V ≤ VCC < 1.8 V
		Low-speed mode		0.5	—	1	µs	1.6 V ≤ VCC ≤ 5.5 V
	Subsystem clock (FSUB) operation			26.041	30.5	31.3	µs	1.6 V ≤ VCC ≤ 5.5 V
	In the self-programming mode	High-speed mode		0.03125	—	1	µs	1.8 V ≤ VCC ≤ 5.5 V
		Middle-speed mode		0.0625	—	1	µs	1.8 V ≤ VCC ≤ 5.5 V
TI00 to TI07 input high-level width, low-level width			t_{TIH} t_{TIL}	1/f_{MCK} +10[1]	—	—	ns	

Table 2.14   AC characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
TO00 to TO07 output frequency	High-speed mode Middle-speed mode	f_{TO}	—	—	16[*2]	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	Low-speed mode		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
PCLBUZ0 output frequency	High-speed mode Middle-speed mode	f_{PCL}	—	—	16[*2]	MHz	4.0 V ≤ VCC ≤ 5.5 V
			—	—	8	MHz	2.7 V ≤ VCC < 4.0 V
			—	—	4	MHz	1.8 V ≤ VCC < 2.7 V
			—	—	2	MHz	1.6 V ≤ VCC < 1.8 V
	Low-speed mode		—	—	2	MHz	1.6 V ≤ VCC ≤ 5.5 V
Interrupt input high-level width, low-level width	NMI/IRQ0, IRQ1 to IRQ5	f_{IRQH} f_{IRQL}	1	—	—	µs	1.6 V ≤ VCC ≤ 5.5 V

Note 1. f_{MCK}: Timer array unit operating clock frequency
To set this operating clock, use the CKS[1:0] bits of the timer mode register 0n (TMR0n).
m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Note 2. The maximum value is 12MHz with an ambient operating temperature range of 105°C to 125°C.
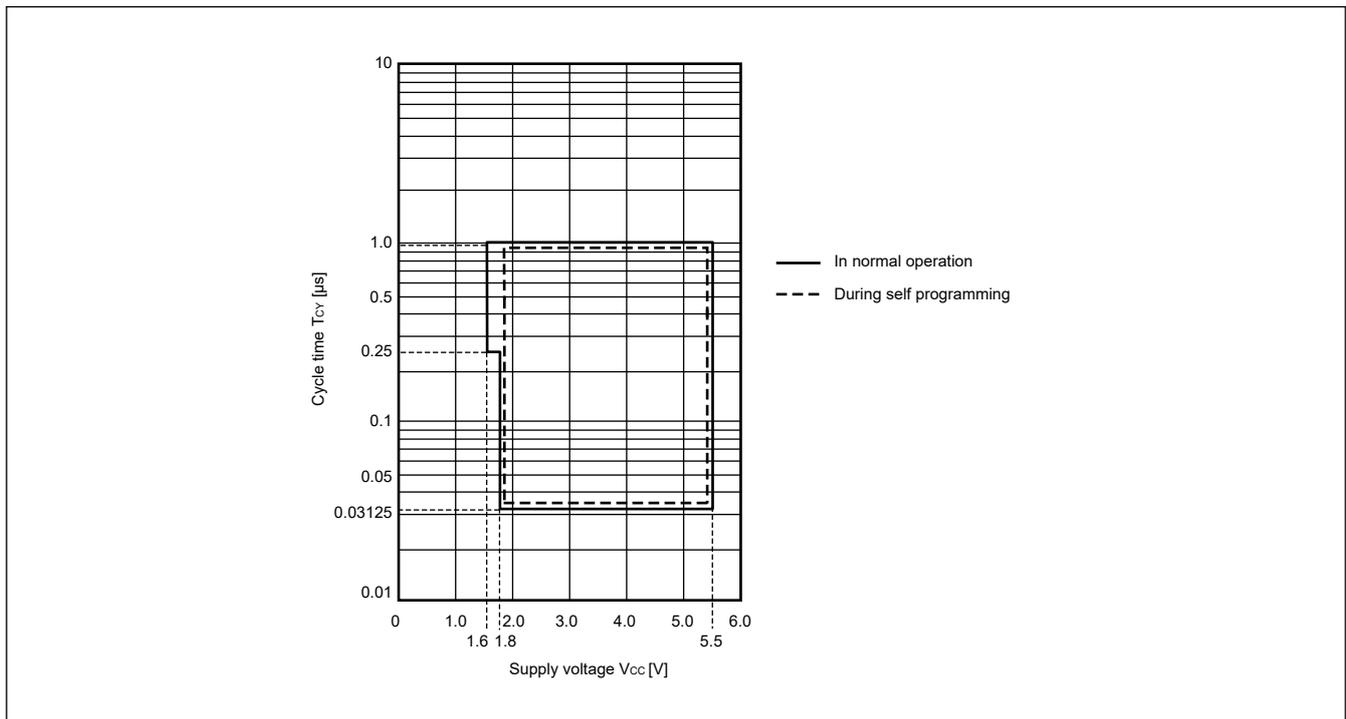
Figure 2.2 T_{CY} vs V_{CC} in High-speed mode
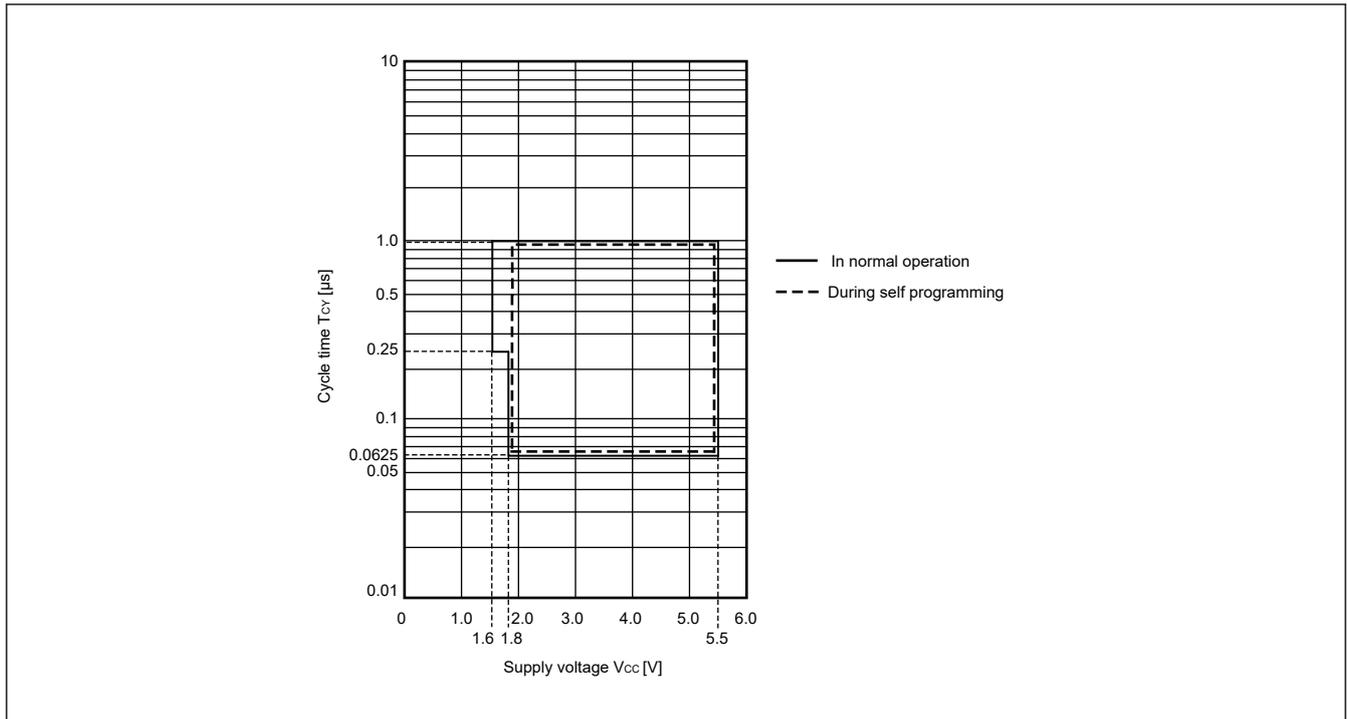
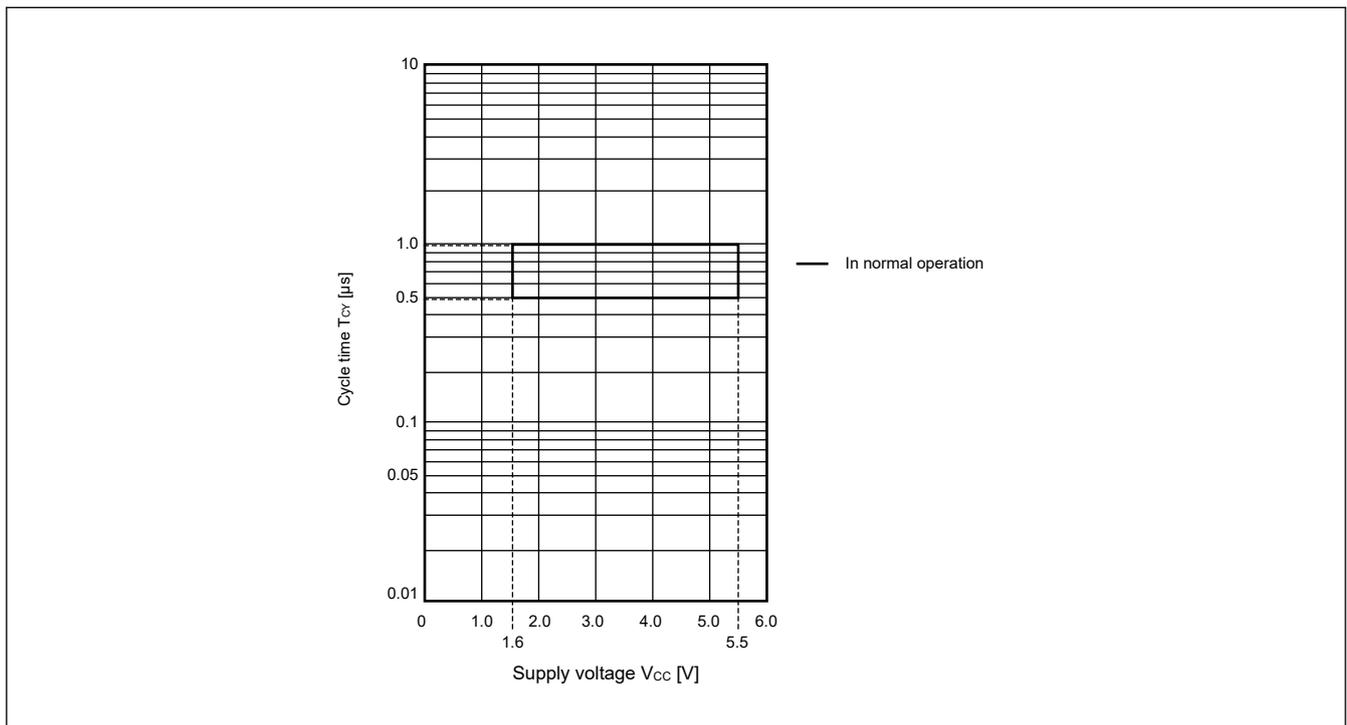**Figure 2.3   T_{CY} vs V_{CC} in Middle-speed mode**

Figure 2.4   T_{CY} vs V_{CC} in Low-speed mode
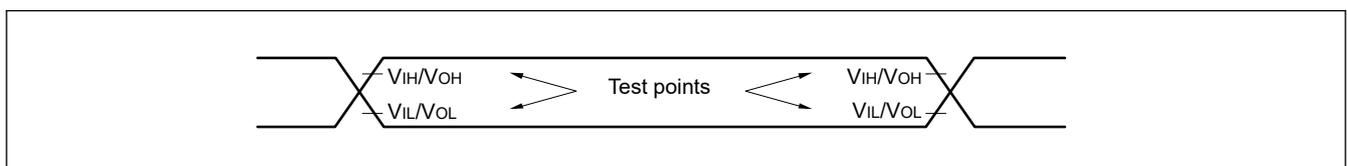

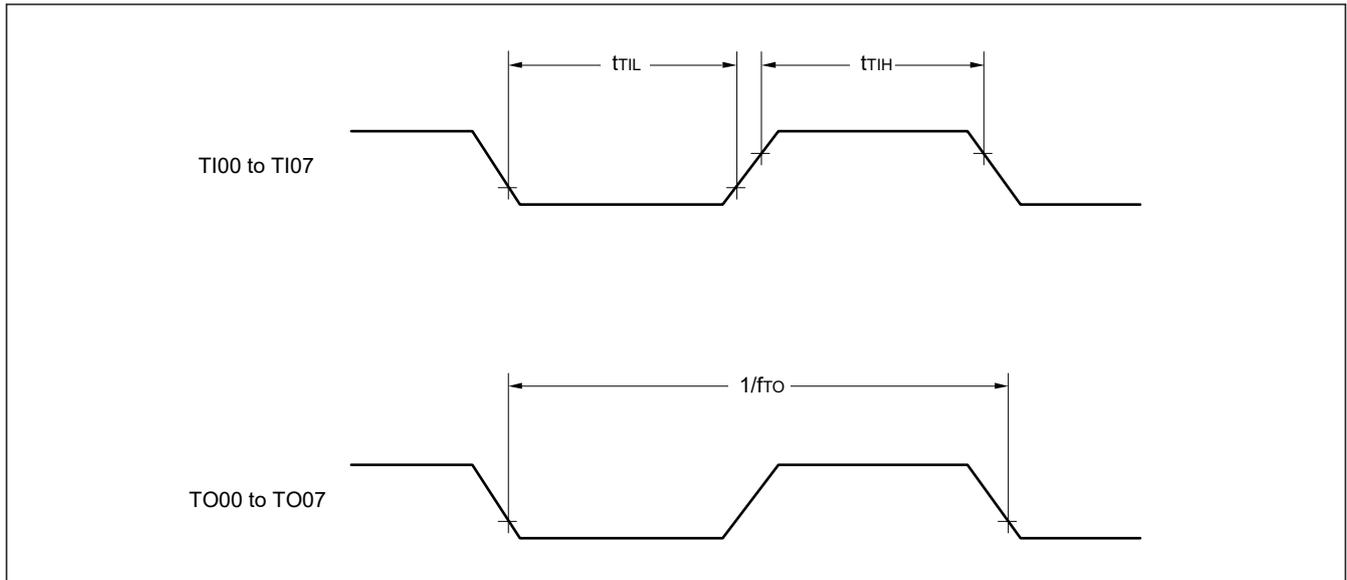**Figure 2.5   AC timing test points**

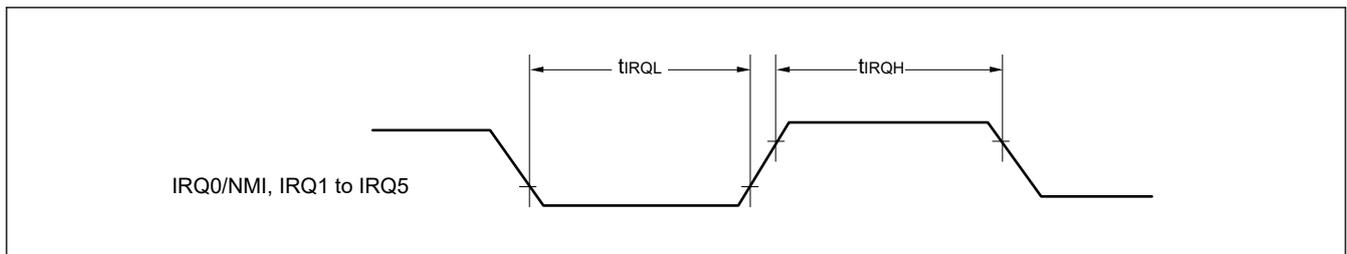**Figure 2.6   TI/TO timing**

Figure 2.7   IRQ interrupt input timing

2.4.1   Reset Timing

Table 2.15   Reset timing

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
RES pulse width	At power-on[3]	t_{RESWP}	9.9	—	—	ms	—
	Not at power-on	t_{RESW}	10	—	—	µs	—
Wait time after RES cancellation (at power-on)	LVD0 enabled[1]	t_{RESWT}	—	0.506	0.694	ms	—
	LVD0 disabled[2]		—	0.201	0.335	ms	—
Wait time after RES cancellation (during powered-on state)	LVD0 enabled[1]	t_{RESWT2}	—	0.476	0.616	ms	—
	LVD0 disabled[2]		—	0.170	0.257	ms	—
Internal reset by Independent watch dog timer reset, software reset		t_{RESW2}	—	0.04	0.041	ms	—

Note 1.   When OFS1.LVDAS = 0.
Note 2.   When OFS1.LVDAS = 1.
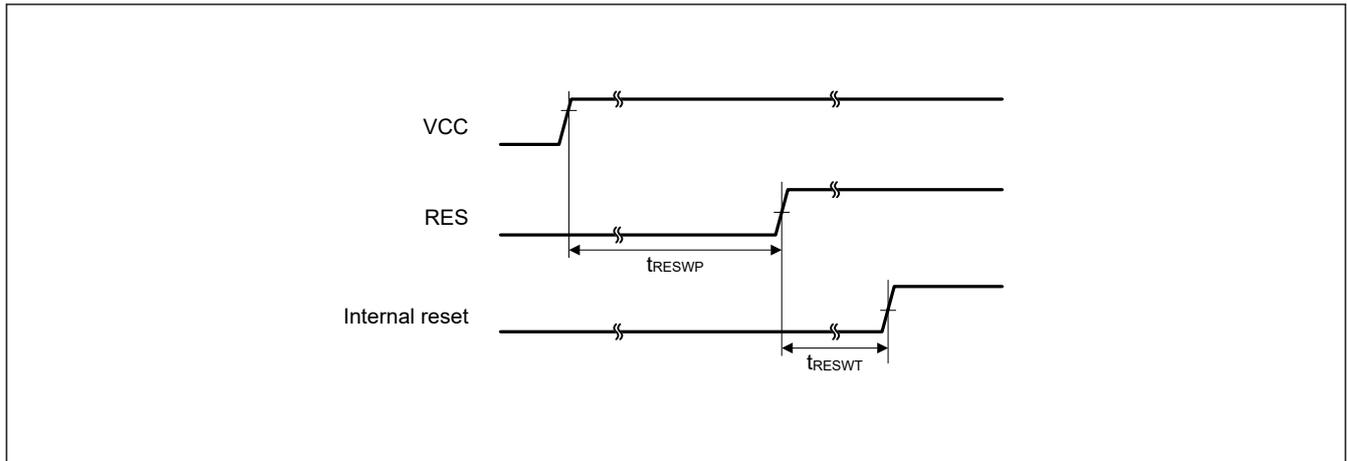Note 3.   When RES pin is not used as the external reset input, this specification can be ignored.

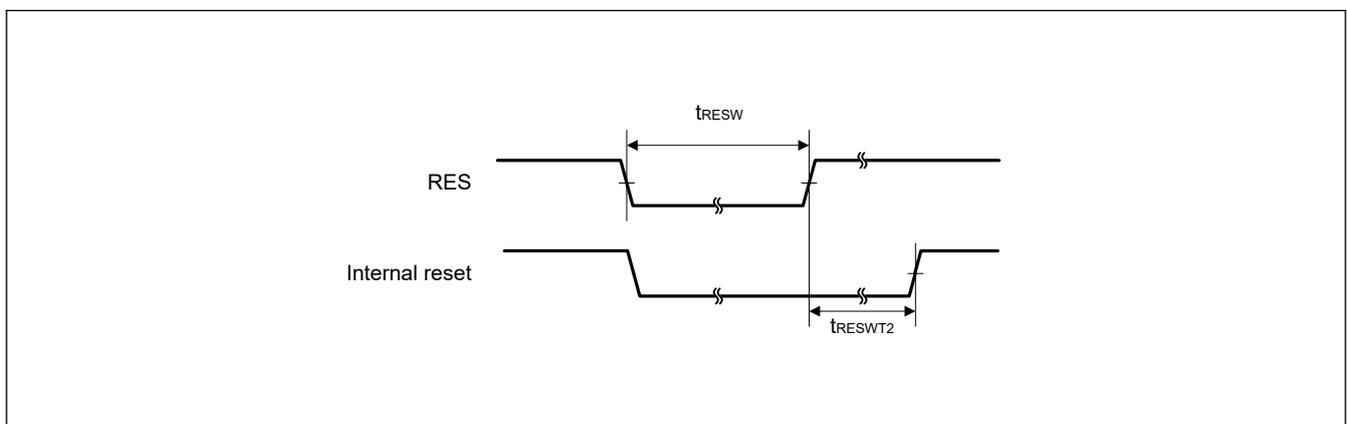**Figure 2.8   Reset input timing at power-on**
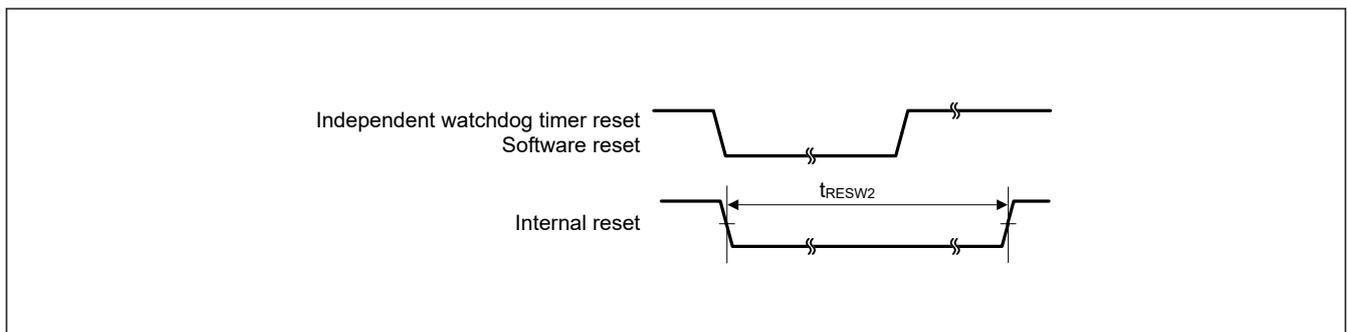

Figure 2.9   Reset input timing (1)

Figure 2.10   Reset input timing (2)

2.4.2   Wakeup Time

Table 2.16   Timing of recovery from low power modes (1)

Parameter				Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode[*1]	High-speed mode	System clock source is HOCO	System clock source is HOCO (32 MHz) VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.3	5.7	µs	Figure 2.11
			System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V		—	7.3	7.7	µs	

Note 1.   The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Table 2.17   Timing of recovery from low power modes (2)

Parameter				Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode[1]	Middle-speed mode	System clock source is HOCO	System clock source is HOCO (16 MHz) VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.5	5.8	µs	Figure 2.11
			System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V			—	7.3	7.7	µs	

Note 1.   The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Table 2.18   Timing of recovery from low power modes (3)

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode[1]	Low-speed mode	System clock source is HOCO (2 MHz)	t_{SBYHO}	—	10.0	10.5	µs	Figure 2.11

Note 1.   The division ratio of ICLK is the minimum division ratio within the allowable frequency range.
The recovery time is determined by the system clock source.

Table 2.19   Timing of recovery from low power modes (4)

Parameter			Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode[1]	Subosc-speed mode	System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.29	0.36	ms	Figure 2.11

Note 1.   The LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.
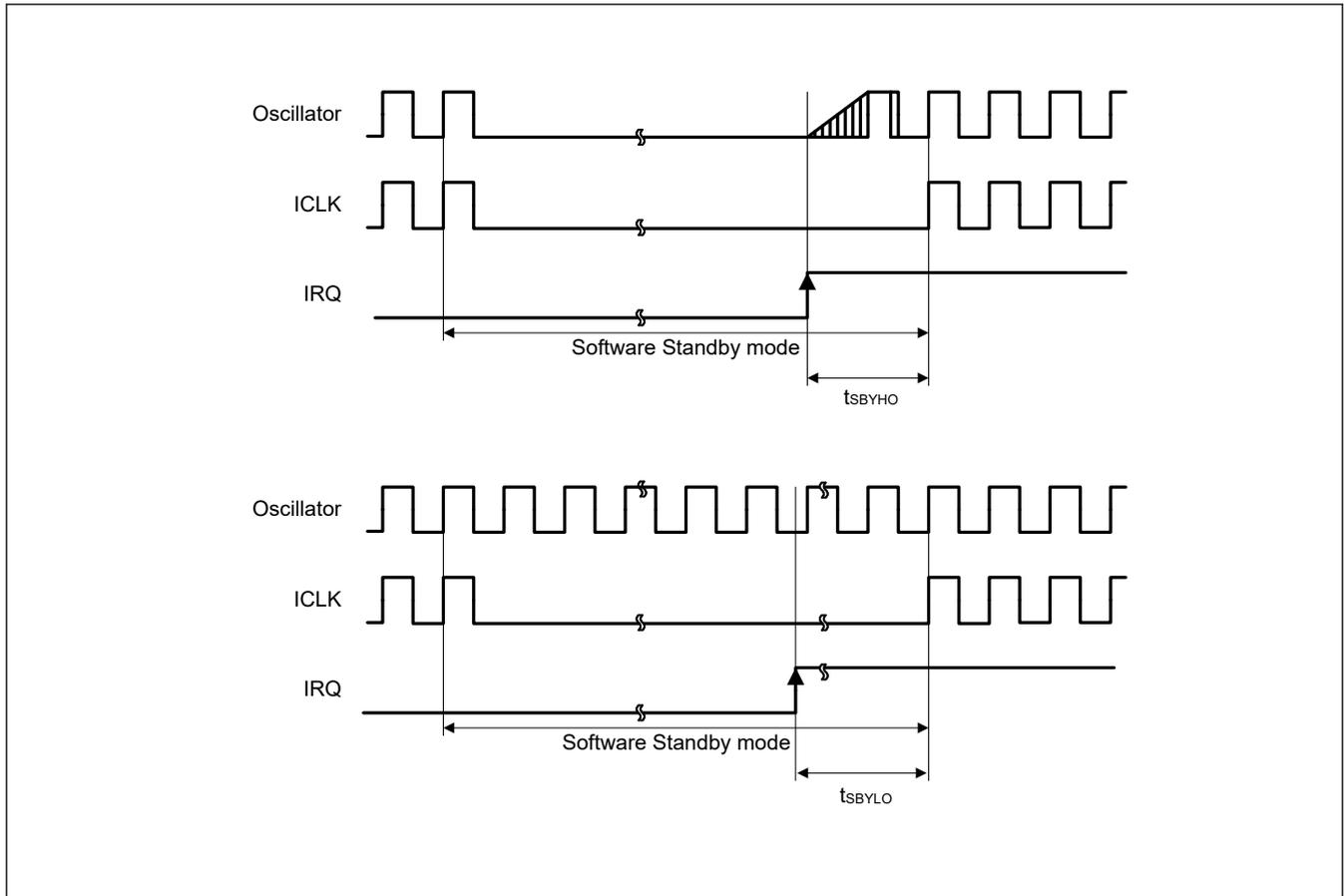
Figure 2.11   Software Standby mode cancellation timing

Table 2.20   Timing of recovery from low power modes (5)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	5.3	5.7	µs	Figure 2.12
	Middle-speed mode System clock source is HOCO (16 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	5.5	5.8	µs	
	Middle-speed mode System clock source is HOCO (4 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	6.3	6.7	µs	
	Low-speed mode System clock source is HOCO (2 MHz)	t_{SNZ}	—	8.0	8.4	µs	

Note 1. When SBYEDCR0.DTCED bit is set to 1, ICLK is supplied to DTC and SRAM.

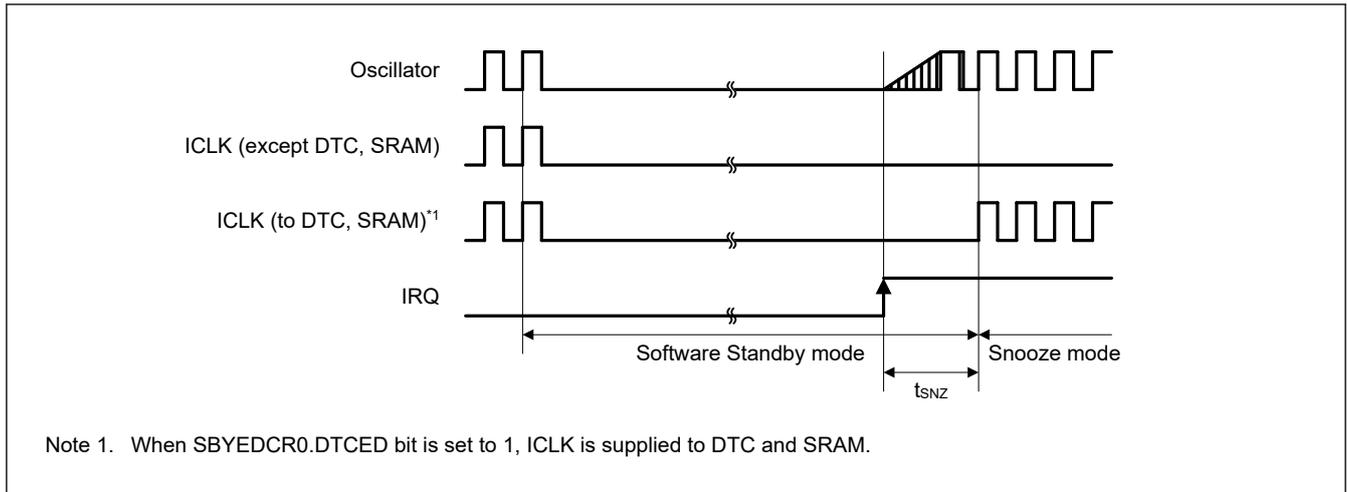**Figure 2.12   Recovery timing from Software Standby mode to Snooze mode**

2.5   Peripheral Function Characteristics

2.5.1   Serial Array Unit (SAU)

Table 2.21   In UART communications with devices operating at the same voltage levels

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate[1]	1.6 V ≤ VCC ≤ 5.5 V		—	—	$f_{MCK}/6$	—	$f_{MCK}/6$	—	$f_{MCK}/6$	bps	Figure 2.14
		Theoretical value of the maximum transfer rate f_{MCK} = PCLKB[2]		—	5.3	—	4	—	0.33	Mbps	

Note 1. The transfer rate in SNOOZE mode is within the range from 4800 to 9600 bps when SBYCR.FWKUP = 0, and within the range from 4800 to 115200 bps when SBYCR.FWKUP = 1.

Note 2. The maximum operating frequencies of the peripheral module clock (PCLKB) are as follows.
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 16 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

Note: Select the normal input buffer for the RXDq pin and the normal output mode for the TXDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

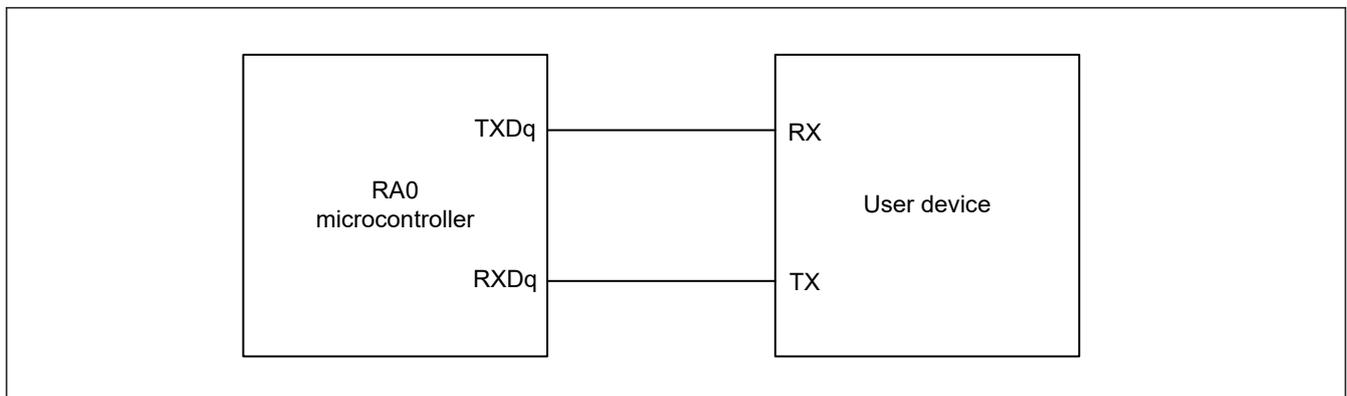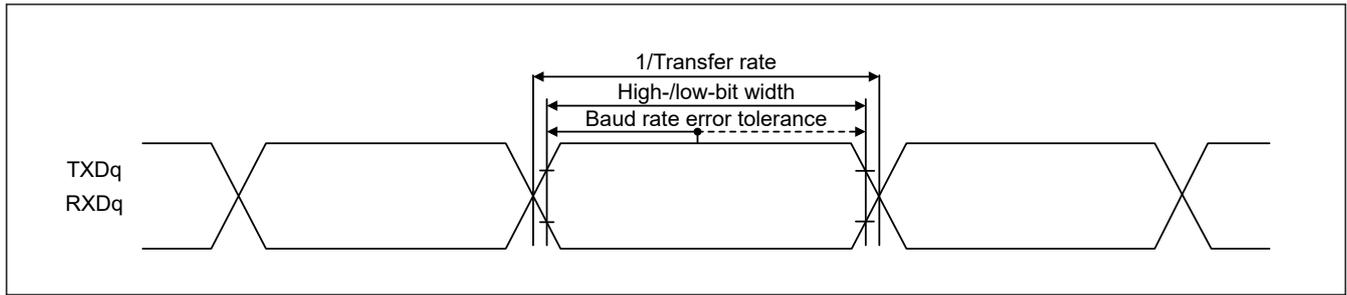gh: Port number (gh = 100, 101, 109, 110, 200, 212, 213, 300)

Figure 2.13   Connection in the UART communications with devices operating at the same voltage levels

Figure 2.14   Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)

Note: ● q: UART number (q = 0, 1), gh: Port number (gh = 100, 101, 109, 110, 200, 212, 213, 300)

● f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, set the CKS bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 03)

Table 2.22   In simplified SPI communications in the master mode with devices operating at the same voltage levels with the internal SCKp clock (the ratings below are only applicable to SPI00)

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +85℃

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	$t_{KCY1} \geq 2/$ PCLKB	4.0 V ≤ VCC ≤ 5.5 V	t_{KCY1}	62.5	—	125	—	1000	—	ns	Figure 2.16 Figure 2.17
		2.7 V ≤ VCC ≤ 5.5 V		125	—	125	—	1000	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	$t_{KCY1}/2 - 7$	—	$t_{KCY1}/2 - 10$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 10$	—	$t_{KCY1}/2 - 15$	—	$t_{KCY1}/2 - 50$	—	ns	
SIp setup time (to SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	23	—	33	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			33	—	50	—	110	—	ns	
SIp hold time (from SCKp↑)[*1]	2.7 V ≤ VCC ≤ 5.5 V		t_{KSI1}	10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output[*2]	C = 20 pF[*3]		t_{KSO1}	—	10	—	10	—	10	ns	

Note 1.   The setting applies when SCRmn.DCP0[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP0[1:0] = 01b or 10b.

Note 2.   This setting applies when SCRmn.DCP0[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP0[1:0] = 01b or 10b.

Note 3.   C is the load capacitance of the SCKp and SOp output lines.

Note: Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note: ● The listed times are only valid when the peripheral I/O redirect function of SPI00 is not in use.

● p: Simplified SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (gh = 100 to 102, 108 to 110, 112, 200)

● f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00)

Table 2.23   In simplified SPI communications in the master mode with devices operating at the same voltage levels with the internal SCKp clock

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	$t_{KCY1} \geq 4/$ PCLKB	2.7 V ≤ VCC ≤ 5.5 V	t_{KCY1}	125	—	166	—	2000	—	ns	Figure 2.16 Figure 2.17
		2.4 V ≤ VCC ≤ 5.5 V		250	—	250	—	2000	—	ns	
		1.8 V ≤ VCC ≤ 5.5 V		500	—	500	—	2000	—	ns	
		1.6 V ≤ VCC ≤ 5.5 V		1000	—	1000	—	2000	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH1}, t_{KL1}	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 21$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 25$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 38$	—	$t_{KCY1}/2 - 38$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$t_{KCY1}/2 - 100$	—	$t_{KCY1}/2 - 100$	—	$t_{KCY1}/2 - 100$	—	ns	
SIp setup time (to SCKp↑)[1]	4.0 V ≤ VCC ≤ 5.5 V		t_{SIK1}	44	—	54	—	110	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			44	—	54	—	110	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			75	—	75	—	110	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			110	—	110	—	110	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			220	—	220	—	220	—	ns	
SIp hold time (from SCKp↑)[1]	1.6 V ≤ VCC ≤ 5.5 V		t_{KSI1}	19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output[2]	1.6 V ≤ VCC ≤ 5.5 V C = 30 pF[3]		t_{KSO1}	—	25	—	25	—	25	ns	

Note 1.   This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 2.   This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note 3.   C is the load capacitance of the SCKp and SOp output lines.

Note: Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note: ● p: Simplified SPI number (p = 00, 11), m: Unit number (m = 0), n: Channel number (n = 0, 3), gh: Port number (gh = 100 to 102, 108 to 110, 112, 200, 201, 212, 213)

        ● f_{MCK}: Serial array unit operation clock frequency
        To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
        m: Unit number, n: Channel number (mn = 00, 03)

Table 2.24 In simplified SPI communications in the slave mode with devices operating at the same voltage levels with the SCKp external clock

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Item	Conditions		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time[4]	4.0 V ≤ VCC ≤ 5.5 V	20 MHz < f_{MCK}	t_{KCY2}	$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	Figure 2.16 Figure 2.17
		f_{MCK} ≤ 20 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V	16 MHz < f_{MCK}		$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 16 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$6/f_{MCK}$	—	ns	
	2.4 V ≤ VCC ≤ 5.5 V			Greater of: $6/f_{MCK}$ or 500	—	Greater of: $6/f_{MCK}$ or 500	—	Greater of: $6/f_{MCK}$ or 500	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			Greater of: $6/f_{MCK}$ or 750	—	Greater of: $6/f_{MCK}$ or 750	—	Greater of: $6/f_{MCK}$ or 750	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			Greater of: $6/f_{MCK}$ or 1500	—	Greater of: $6/f_{MCK}$ or 1500	—	Greater of: $6/f_{MCK}$ or 1500	—	ns	
SCKp high-/low-level width	4.0 V ≤ VCC ≤ 5.5 V		t_{KH2}, t_{KL2}	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	$t_{KCY2}/2 - 7$	—	ns	
	2.7 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	$t_{KCY2}/2 - 8$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	$t_{KCY2}/2 - 18$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	$t_{KCY2}/2 - 66$	—	ns	
SIp setup time (to SCKp↑)[1]	2.7 V ≤ VCC ≤ 5.5 V		t_{SIK2}	$1/f_{MCK} + 20$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	$1/f_{MCK} + 30$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	$1/f_{MCK} + 40$	—	ns	
SIp hold time (from SCKp↑)[1]	1.8 V ≤ VCC ≤ 5.5 V		t_{KSI2}	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	$1/f_{MCK} + 31$	—	ns	
	1.6 V ≤ VCC ≤ 5.5 V			$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	$1/f_{MCK} + 250$	—	ns	
Delay time from SCKp↓ to SOp output[2]	C = 30 pF[3]	2.7 V ≤ VCC ≤ 5.5 V	t_{KSO2}	—	$2/f_{MCK} + 44$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		2.4 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 75$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.8 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	—	$2/f_{MCK} + 110$	ns	
		1.6 V ≤ VCC ≤ 5.5 V		—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	—	$2/f_{MCK} + 220$	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the SIp setup time becomes to SCKp↓ and that for the SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 2. This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The setting for the delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note 3. C is the load capacitance of the SOp output line.

Note 4. Transfer rate in the Snooze mode is 1 Mbps at the maximum.

Note: Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Note: ● p: Simplified SPI number (p = 00, 11), m: Unit number (m = 0, 1), n: Channel number (n = 0, 3), gh: Port number (gh = 100 to 102, 108 to 110, 112, 200, 201, 212, 213)

         ● f_{MCK}: Serial array unit operation clock frequency
           To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
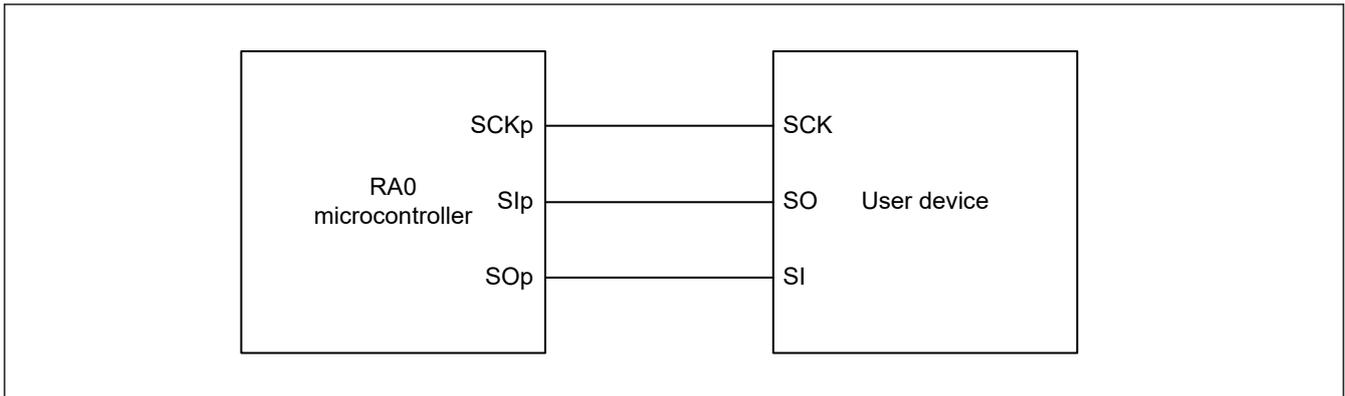   m: Unit number, n: Channel number (mn = 00, 03)

Figure 2.15   Connection in the simplified SPI communications with devices operating at the same voltage levels
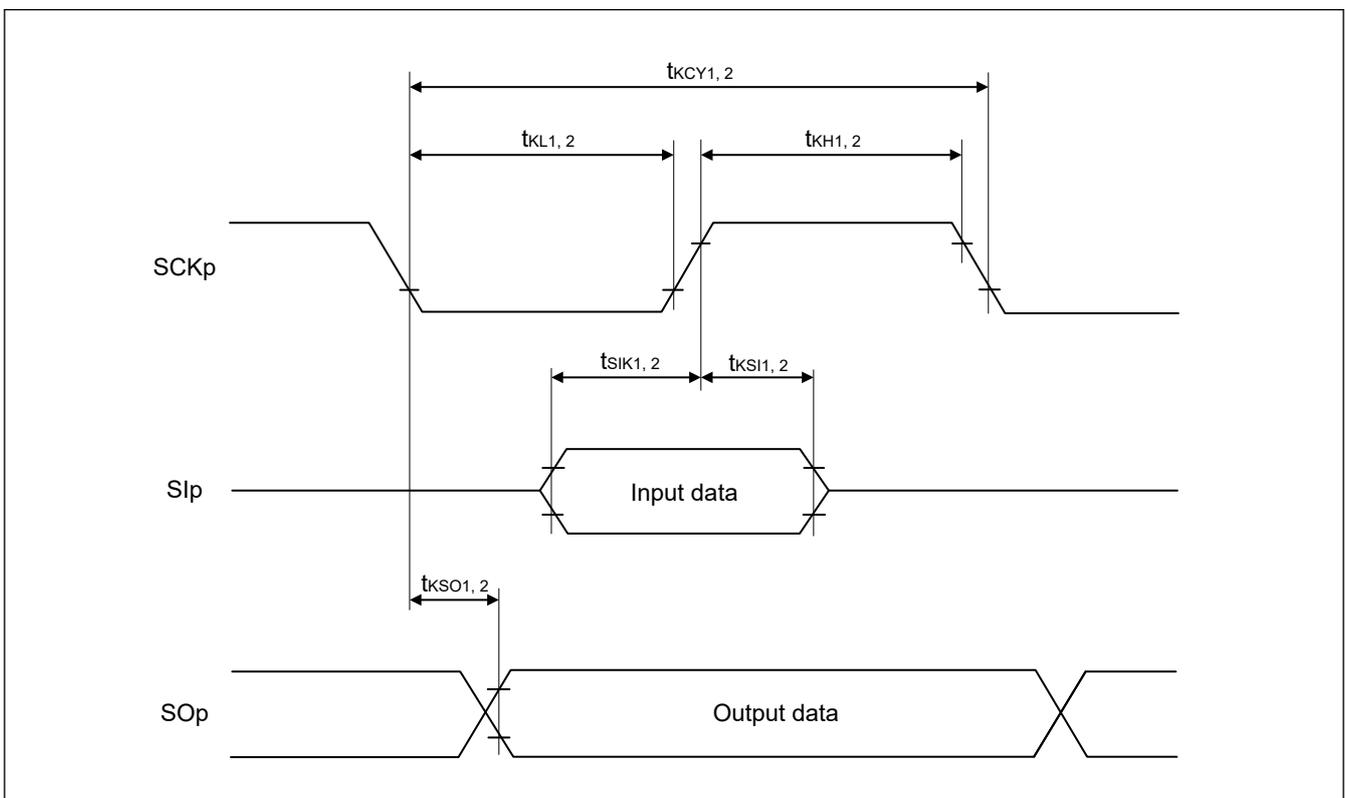

Figure 2.16   Timing of serial transfer in the simplified SPI communications with devices operating at the same voltage levels when SCRmn.DCP[1:0] = 00b or 11b
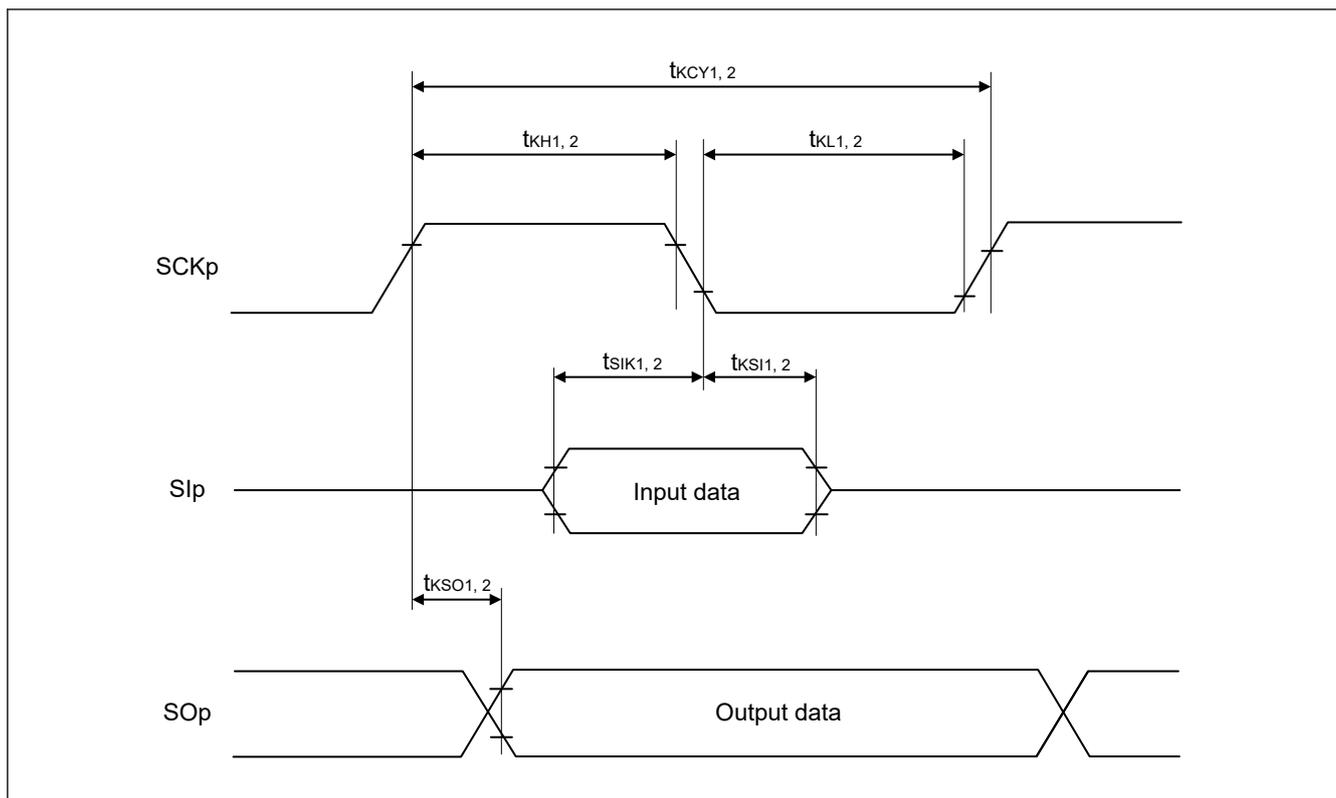
Figure 2.17 Timing of serial transfer in the simplified SPI communications with devices operating at the same voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note:
- p: Simplified SPI number (p = 00, 11)

- m: Unit number, n: Channel number (mn = 00, 03)

Table 2.25   In simplified IIC communications with devices operating at the same voltage levels (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SCLr clock frequency	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	f_{SCL}	—	1000[1]	—	1000[1]	—	400[1]	kHz	Figure 2.19
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		—	400[1]	—	400[1]	—	400[1]	kHz	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		—	300[1]	—	300[1]	—	300[1]	kHz	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—	250[1]	—	250[1]	—	250[1]	kHz	
Hold time when SCLr is low	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{LOW}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	
Hold time when SCLr is high	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{HIGH}	475	—	475	—	1150	—	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		1150	—	1150	—	1150	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		1550	—	1550	—	1550	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		1850	—	1850	—	1850	—	ns	

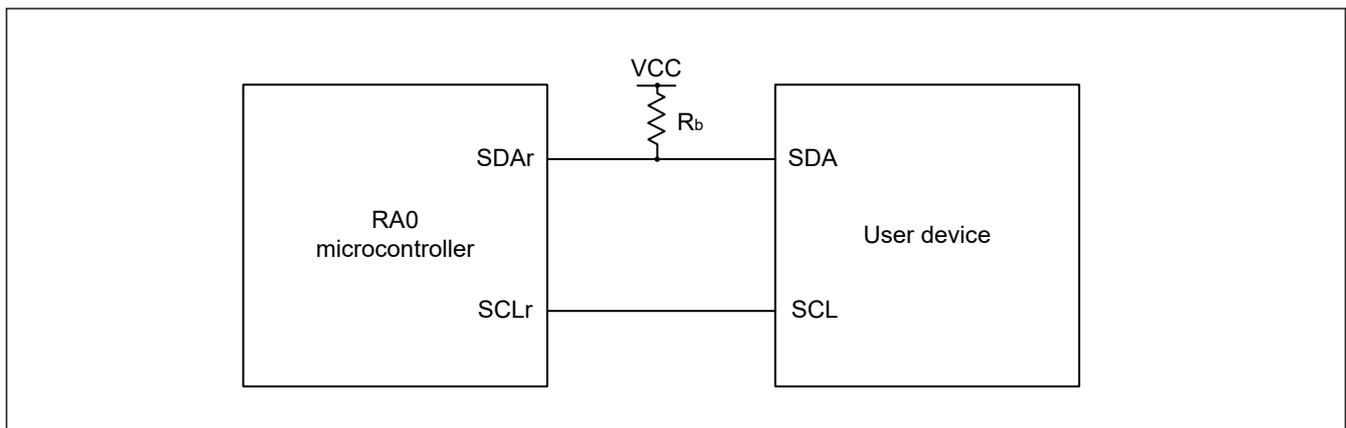**Table 2.25   In simplified IIC communications with devices operating at the same voltage levels (2 of 2)**

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

| Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{SU:DAT}$	$1/f_{MCK} + 85$[*2]	—	$1/f_{MCK} + 85$[*2]	—	$1/f_{MCK} + 145$[*2]	—	ns	Figure 2.19
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		$1/f_{MCK} + 145$[*2]	—	$1/f_{MCK} + 145$[*2]	—	$1/f_{MCK} + 145$[*2]	—	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		$1/f_{MCK} + 230$[*2]	—	$1/f_{MCK} + 230$[*2]	—	$1/f_{MCK} + 230$[*2]	—	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		$1/f_{MCK} + 290$[*2]	—	$1/f_{MCK} + 290$[*2]	—	$1/f_{MCK} + 290$[*2]	—	ns	
Data hold time (transmission)	2.7 V ≤ VCC ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	1.8 V ≤ VCC ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		0	405	0	405	0	405	ns	
	1.6 V ≤ VCC < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		0	405	0	405	0	405	ns	

Note 1. The listed times must be no greater than f_{MCK}/4.

Note 2. Set f_{MCK} so that it does not exceed the hold time when SCLr is low or high.

Note: Select the normal input buffer and the N-ch open drain output [withstand voltage of VCC] mode for the SDAr pin and the normal output mode for the SCLr pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR).

Figure 2.18   Connection in the simplified IIC communications with devices operating at the same voltage levels
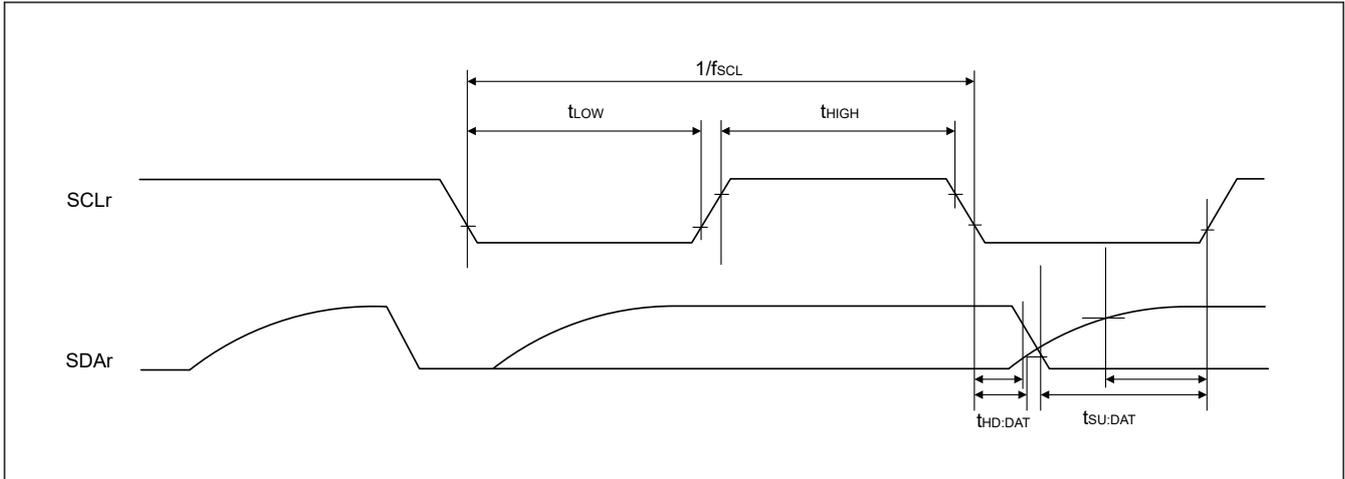
Figure 2.19 Timing of serial transfer in the simplified IIC communications with devices operating at the same voltage levels

Note:
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
- r: IIC number (r = 00, 11), gh: Port number (gh = 100, 102, 110, 112, 201, 212)
- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)

Table 2.26 In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V) (1)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter				Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
					Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate	Reception	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		—	—	$f_{MCK}/6$[*1]	—	$f_{MCK}/6$[*1]	—	$f_{MCK}/6$[*1]	bps	Figure 2.21
			Theoretical value of the maximum transfer rate f_{MCK} = PCLKB[*3]		—	5.3	—	4	—	0.33	Mbps	
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			—	$f_{MCK}/6$[*1]	—	$f_{MCK}/6$[*1]	—	$f_{MCK}/6$[*1]	bps	
			Theoretical value of the maximum transfer rate f_{MCK}[*3] = PCLKB[*3]		—	5.3	—	4	—	0.33	Mbps	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			—	$f_{MCK}/6$[*1] [*2]	—	$f_{MCK}/6$[*1] [*2]	—	$f_{MCK}/6$[*1] [*2]	bps	
			Theoretical value of the maximum transfer rate f_{MCK} = PCLKB[*3]		—	5.3	—	4	—	0.33	Mbps	

Note 1. Transfer rate in the Snooze mode is within the range from 4800 to 9600 bps.
Note 2. Use this rate with VCC ≥ V_b.
Note 3. The maximum operating frequencies of the system clock (PCLKB) are:
High-speed mode: 32 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Middle-speed mode: 16 MHz (1.8 V ≤ VCC ≤ 5.5 V), 4 MHz (1.6 V ≤ VCC ≤ 5.5 V)
Low-speed mode: 2 MHz (1.6 V ≤ VCC ≤ 5.5 V)

Note: Select the TTL input buffer for the RXDq pin and the N-ch open drain output [withstand voltage of VCC] mode for the TXDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Note:
- $V_b[V]$: Communication line voltage
- q: UART number (q = 0, 1), gh: Port number (gh = 100, 101, 109, 110, 212, 213, 300)
- f_{MCK}: Serial array unit operation clock frequency

To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 03)

● Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.27   In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V) (2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode Min.	High-speed mode Max.	Middle-speed mode Min.	Middle-speed mode Max.	Low-speed mode Min.	Low-speed mode Max.	Unit	Test Conditions
Transfer rate	Transmission	$4.0\ V \le VCC \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$	—	—	*1	—	*1	—	*1	bps	Figure 2.21
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		—	2.8[*2]	—	2.8[*2]	—	2.8[*2]	Mbps	
		$2.7\ V \le VCC < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$		—	*3	—	*3	—	*3	bps	
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		—	1.2[*4]	—	1.2[*4]	—	1.2[*4]	Mbps	
		$1.8\ V \le VCC < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$		—	*5 *6	—	*5 *6	—	*5 *6	bps	
		Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		—	0.43[*7]	—	0.43[*7]	—	0.43[*7]	Mbps	

Note 1.   The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $4.0\ V \le VCC \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\left\{ -C_b \times R_b \times \ln\left(1 - \frac{2.2}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \left\{-C_b \times R_b \times \ln\left(1 - \frac{2.2}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2.   This rate is calculated as an example when the conditions described in the Conditions column are met. See [*1] above to calculate the maximum transfer rate under the conditions of the customer.

Note 3.   The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $2.7\ V \le VCC < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$

$$\text{Maximum transfer rate} = \frac{1}{\left\{ -C_b \times R_b \times \ln\left(1 - \frac{2.0}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \left\{-C_b \times R_b \times \ln\left(1 - \frac{2.0}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4.   This rate is calculated as an example when the conditions described in the Conditions column are met. See [*3] above to calculate the maximum transfer rate under the conditions of the customer.

Note 5.   Use this rate with $VCC \ge V_b$.

Note 6.   The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $1.8\ V \le VCC < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\left\{ -C_b \times R_b \times \ln\left(1 - \frac{1.5}{V_b}\right)\right\} \times 3}[\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \left\{-C_b \times R_b \times \ln\left(1 - \frac{1.5}{V_b}\right)\right\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100[\%]$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 7.   This rate is calculated as an example when the conditions described in the Conditions column are met. See [6] above to calculate the maximum transfer rate under the conditions of the customer.

Note: Select the TTL input buffer for the RXDq pin and the N-ch open drain output [withstand voltage of VCC] mode for the TXDq pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.
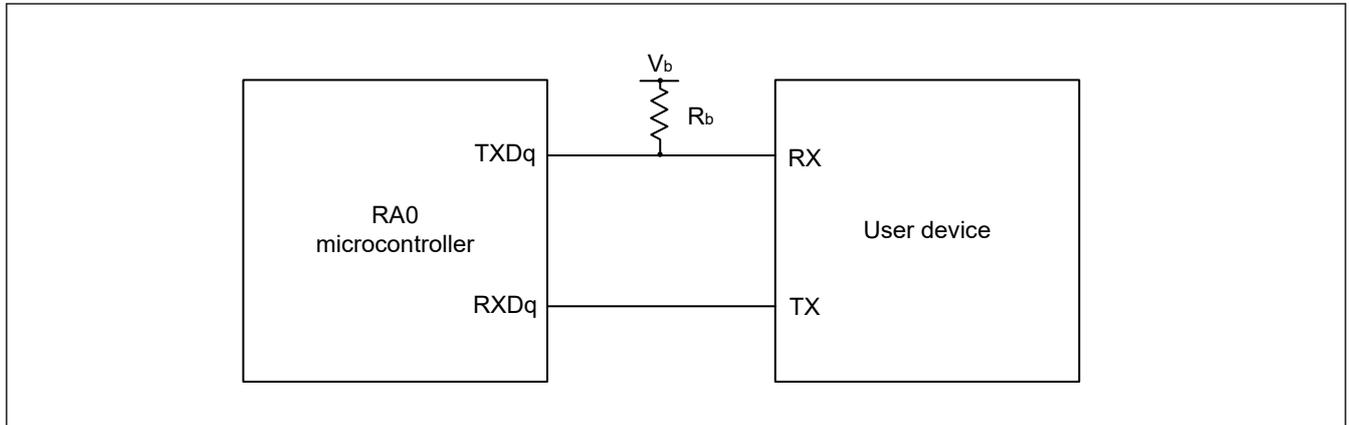

Figure 2.20   In UART communications with devices operating at different voltage levels
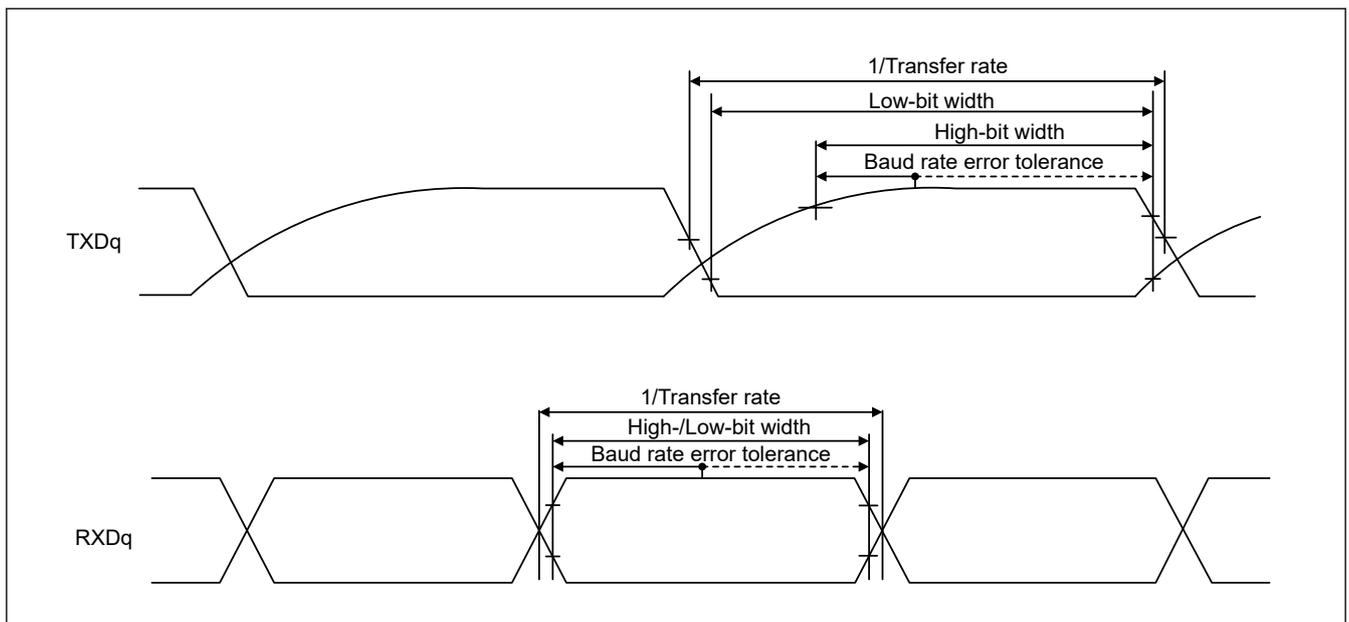

Figure 2.21   Bit width in the UART communications with devices operating at different voltage levels (reference)

Note: ● $R_b[\Omega]$: Communication line (TXDq) pull-up resistance, $C_b[F]$: Communication line (TXDq) load capacitance, $V_b[V]$: Communication line voltage

          ● q: UART number (q = 0, 1), gh: Port number (gh = 100, 101, 109, 110, 212, 213, 300)

          ● f_{MCK}: Serial array unit operation clock frequency
          To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
          m: Unit number, n: Channel number (mn = 00, 01, 02, 03)

          ● Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.28   In simplified SPI communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to SPI00)

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +105℃

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	$t_{KCY1} \geq$ 2/PCLKB	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}	200	—	200	—	2300	—	ns	Figure 2.23 Figure 2.24
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		300	—	300	—	2300	—	ns	
SCKp high-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KH1}	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			t_{KCY1}/2 - 120	—	t_{KCY1}/2 - 120	—	t_{KCY1}/2 - 120	—	ns	
SCKp low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KL1}	t_{KCY1}/2 -7	—	t_{KCY1}/2 -7	—	t_{KCY1}/2 - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 10	—	t_{KCY1}/2 - 50	—	ns	
SIp setup time (to SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{SIK1}	58	—	58	—	479	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			121	—	121	—	479	—	ns	
SIp hold time (from SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
Delay time from SCKp↓ to SOp output[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSO1}	—	60	—	60	—	60	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			—	130	—	130	—	130	ns	
SIp setup time (to SCKp↓)[*2]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{SIK1}	23	—	23	—	110	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			33	—	33	—	110	—	ns	
SIp hold time (from SCKp↓)[*2]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSI1}	10	—	10	—	10	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	—	10	—	10	—	ns	
Delay time from SCKp↑ to SOp output[*2]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KSO1}	—	10	—	10	—	10	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			—	10	—	10	—	10	ns	

Note 1.   This setting applies when SCRmn.DCP[1:0] = 00b or 11b.
Note 2.   This setting applies when SCRmn.DCP[1:0] = 01b or 10b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Note: ● R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

   ● p: Simplified SPI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), gh: Port number (gh = 100 to 102, 108 to 110, 112)

   ● f_{MCK}: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00)

Table 2.29   In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (1)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	$t_{KCY1} \geq 4/$ PCLKB	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}	300	—	300	—	2300	—	ns	Figure 2.23 Figure 2.24
		2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		500	—	500	—	2300	—	ns	
		1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*1], C_b = 30 pF, R_b = 5.5 kΩ		1150	—	1150	—	2300	—	ns	
SCKp high-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KH1}	$t_{KCY1}/2 - 75$	—	$t_{KCY1}/2 - 75$	—	$t_{KCY1}/2 - 75$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			$t_{KCY1}/2 - 170$	—	$t_{KCY1}/2 - 170$	—	$t_{KCY1}/2 - 170$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*1], C_b = 30 pF, R_b = 5.5 kΩ			$t_{KCY1}/2 - 458$	—	$t_{KCY1}/2 - 458$	—	$t_{KCY1}/2 - 458$	—	ns	
SCKp low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KL1}	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 12$	—	$t_{KCY1}/2 - 50$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 18$	—	$t_{KCY1}/2 - 50$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*1], C_b = 30 pF, R_b = 5.5 kΩ			$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	$t_{KCY1}/2 - 50$	—	ns	

Note 1.   Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Table 2.30 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SIp setup time (to SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{SIK1}	81	—	81	—	479	—	ns	Figure 2.23 Figure 2.24
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		177	—	177	—	479	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		479	—	479	—	479	—	ns	
SIp hold time (from SCKp↑)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
Delay time from SCKp↓ to SOp output[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSO1}	—	100	—	100	—	100	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		—	195	—	195	—	195	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		—	483	—	483	—	483	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 00b or 11b.
Note 2. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.

Table 2.31 In simplified SPI communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock (3)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
SIp setup time (to SCKp↓)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{SIK1}	44	—	44	—	110	—	ns	Figure 2.23 Figure 2.24
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		44	—	44	—	110	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		110	—	110	—	110	—	ns	
SIp hold time (from SCKp↓)[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSI1}	19	—	19	—	19	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		19	—	19	—	19	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		19	—	19	—	19	—	ns	
Delay time from SCKp↑ to SOp output[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KSO1}	—	25	—	25	—	25	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		—	25	—	25	—	25	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ		—	25	—	25	—	25	ns	

Note 1. This setting applies when SCRmn.DCP[1:0] = 01b or 10b.
Note 2. Use this setting with VCC ≥ V_b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.
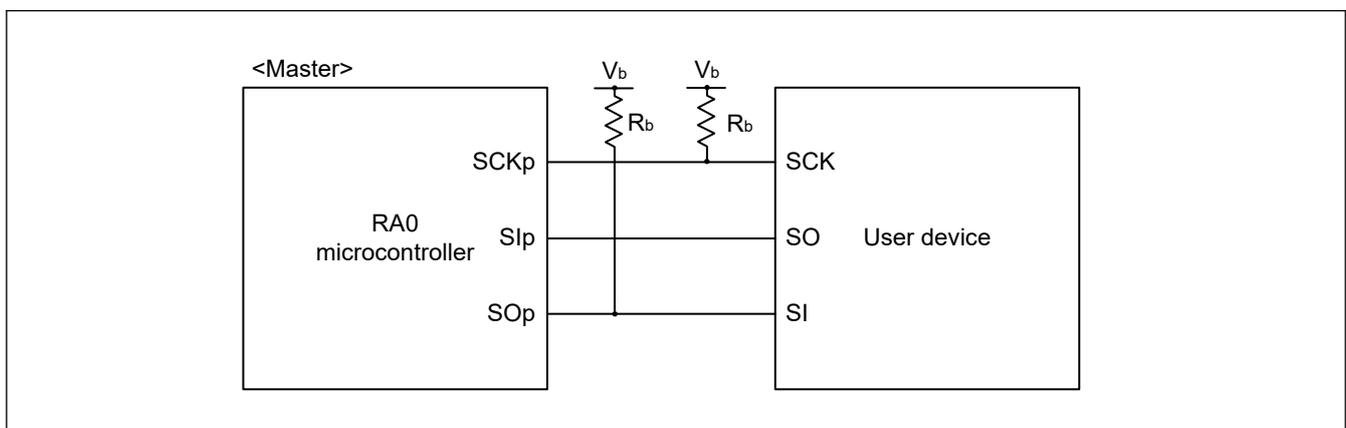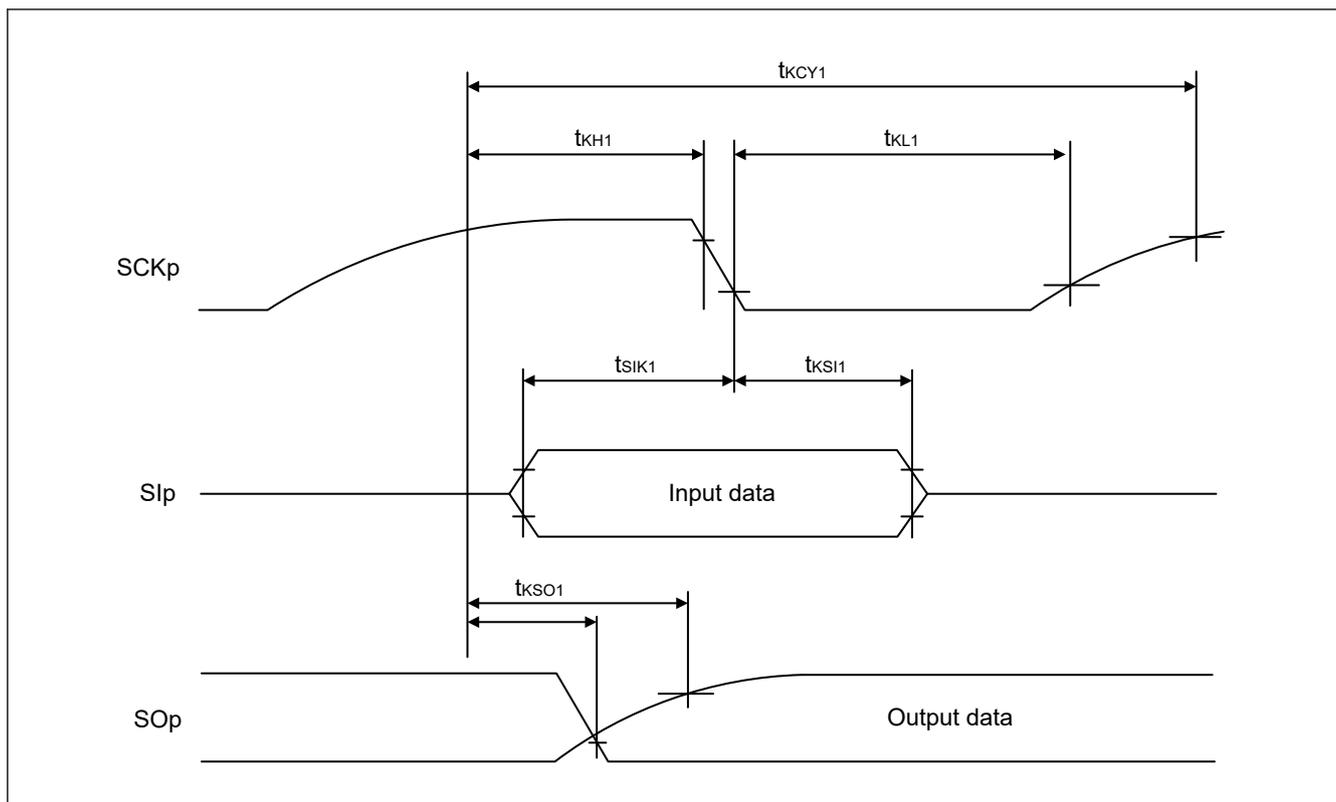

Figure 2.22 Connection in the simplified SPI communications with devices operating at different voltage levels

Note: ● R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)

- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03)

- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.
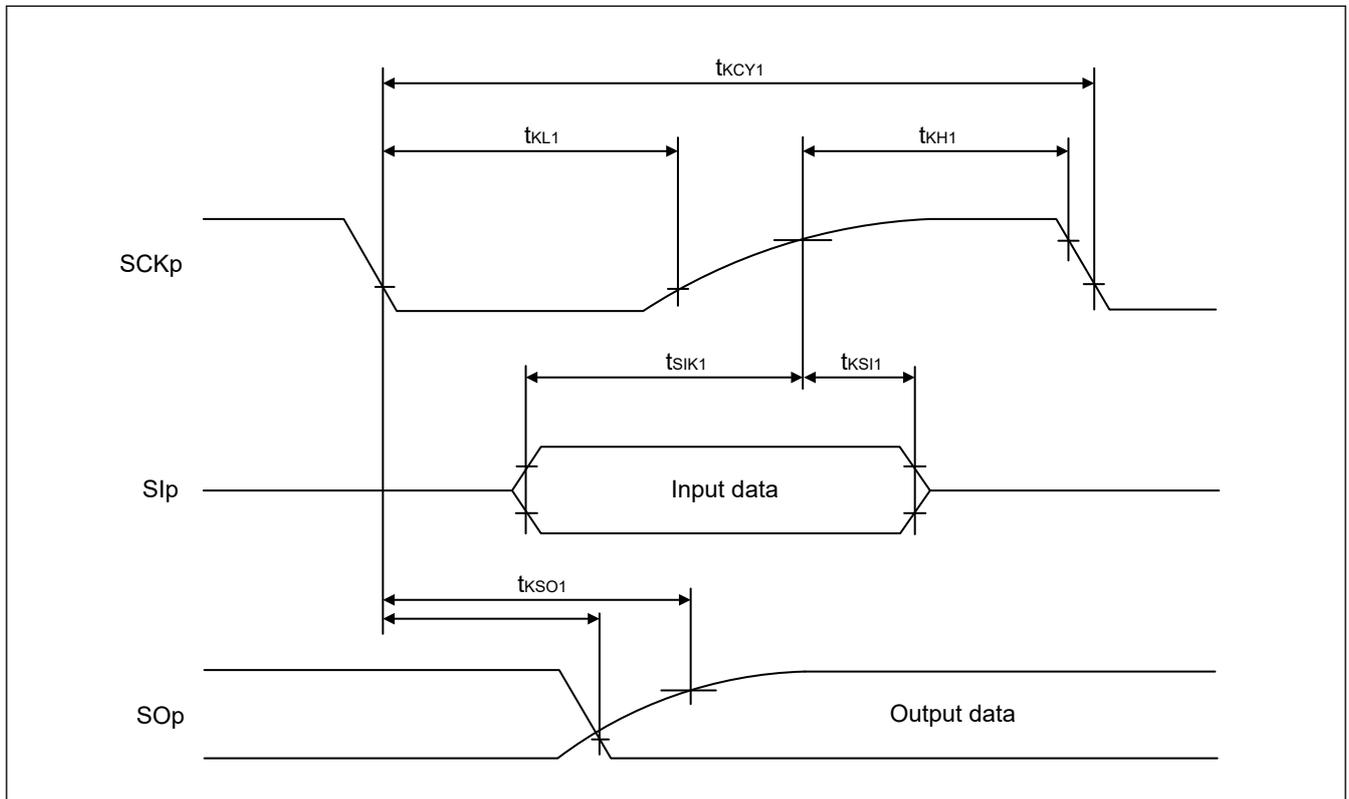
Figure 2.23 **Timing of serial transfer in the simplified SPI communications in the master mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 00b or 11b**

Figure 2.24   Timing of serial transfer in the simplified SPI communications in the master mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note: ● p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)

   ● Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.32   In simplified SPI communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

| Parameter			Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time[*1]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	f_{MCK} = 32 MHz	t_{KCY2}	$14/f_{MCK}$	—	—	—	—	—	ns	Figure 2.26 Figure 2.27
		8 MHz < f_{MCK} ≤ 16 MHz		$10/f_{MCK}$	—	$10/f_{MCK}$	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$10/f_{MCK}$	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	f_{MCK} = 32 MHz		$20/f_{MCK}$	—	—	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		$12/f_{MCK}$	—	$12/f_{MCK}$	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		$8/f_{MCK}$	—	$8/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		$6/f_{MCK}$	—	$6/f_{MCK}$	—	$10/f_{MCK}$	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2]	f_{MCK} = 32 MHz		$48/f_{MCK}$	—	—	—	—	—	ns	
		8 MHz < f_{MCK} ≤ 16 MHz		$26/f_{MCK}$	—	$26/f_{MCK}$	—	—	—	ns	
		4 MHz < f_{MCK} ≤ 8 MHz		$16/f_{MCK}$	—	$16/f_{MCK}$	—	—	—	ns	
		f_{MCK} ≤ 4 MHz		$10/f_{MCK}$	—	$10/f_{MCK}$	—	$10/f_{MCK}$	—	ns	
SCKp high-/ low-level width	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KH2}, t_{KL2}	$t_{KCY2}/2$ - 12	—	$t_{KCY2}/2$ - 12	—	$t_{KCY2}/2$ - 50	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$t_{KCY2}/2$ - 18	—	$t_{KCY2}/2$ - 18	—	$t_{KCY2}/2$ - 50	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2]			$t_{KCY2}/2$ - 50	—	$t_{KCY2}/2$ - 50	—	$t_{KCY2}/2$ - 50	—	ns	
SIp setup time (to SCKp↑)[*3]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{SIK2}	$1/f_{MCK}$ + 20	—	$1/f_{MCK}$ + 20	—	$1/f_{MCK}$ + 30	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			$1/f_{MCK}$ + 20	—	$1/f_{MCK}$ + 20	—	$1/f_{MCK}$ + 30	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2]			$1/f_{MCK}$ + 30	—	$1/f_{MCK}$ + 30	—	$1/f_{MCK}$ + 30	—	ns	
SIp hold time (from SCKp↑)[*3]			t_{KSI2}	$1/f_{MCK}$ + 31	—	$1/f_{MCK}$ + 31	—	$1/f_{MCK}$ + 31	—	ns	
Delay time from SCKp↓ to SOp output[*4]	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KSO2}	—	$2/f_{MCK}$ + 120	—	$2/f_{MCK}$ + 120	—	$2/f_{MCK}$ + 573	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			—	$2/f_{MCK}$ + 214	—	$2/f_{MCK}$ + 214	—	$2/f_{MCK}$ + 573	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 30 pF, R_b = 5.5 kΩ			—	$2/f_{MCK}$ + 573	—	$2/f_{MCK}$ + 573	—	$2/f_{MCK}$ + 573	ns	

Note 1.   Transfer rate in the Snooze mode: 1 Mbps (max.)

Note 2.   Use this setting with VCC ≥ V_b.

Note 3.   This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The SIp setup time becomes to SCKp↓ and SIp hold time becomes from SCKp↓ when SCRmn.DCP[1:0] = 01b or 10b.

Note 4.   This setting applies when SCRmn.DCP[1:0] = 00b or 11b. The delay time to SOp output becomes from SCKp↑ when SCRmn.DCP[1:0] = 01b or 10b.

Note: Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VCC] mode for the SOp pin and SCKp pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.
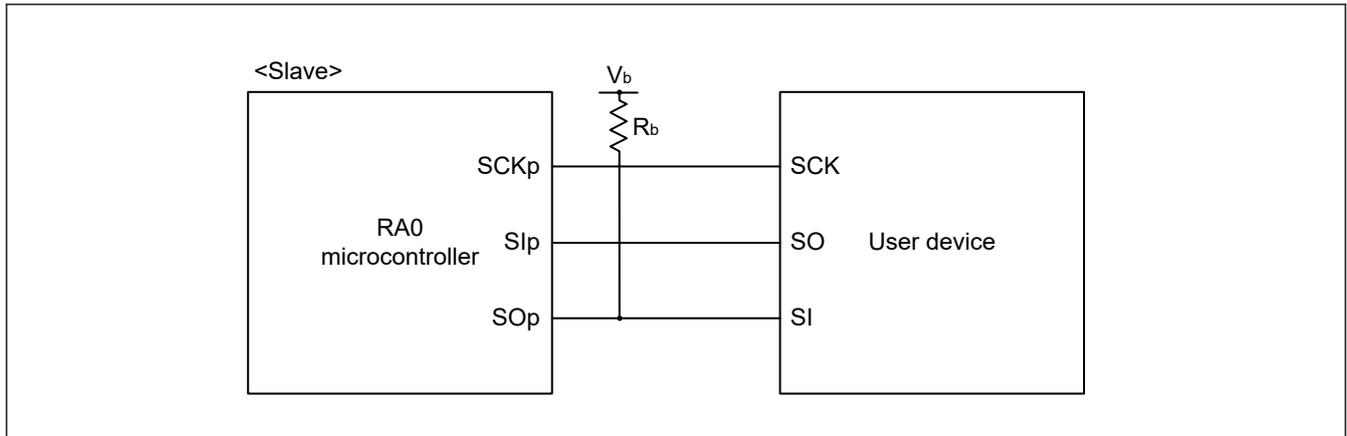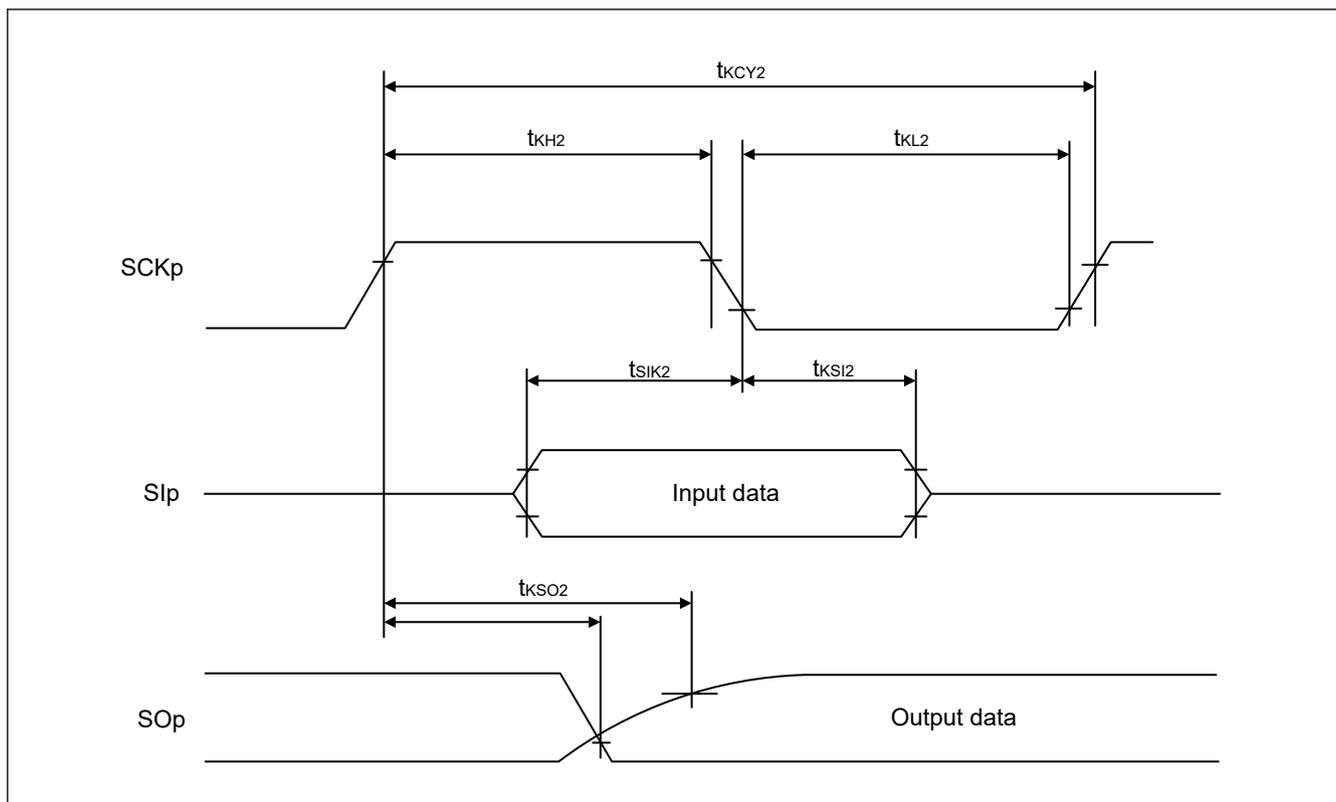
Figure 2.25 Connection in the simplified SPI communications with devices operating at different voltage levels

Note:
- $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage

- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)

- f_{MCK}: Serial array unit operation clock frequency
  To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
  m: Unit number, n: Channel number (mn = 00, 03, 10, 11)

- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.
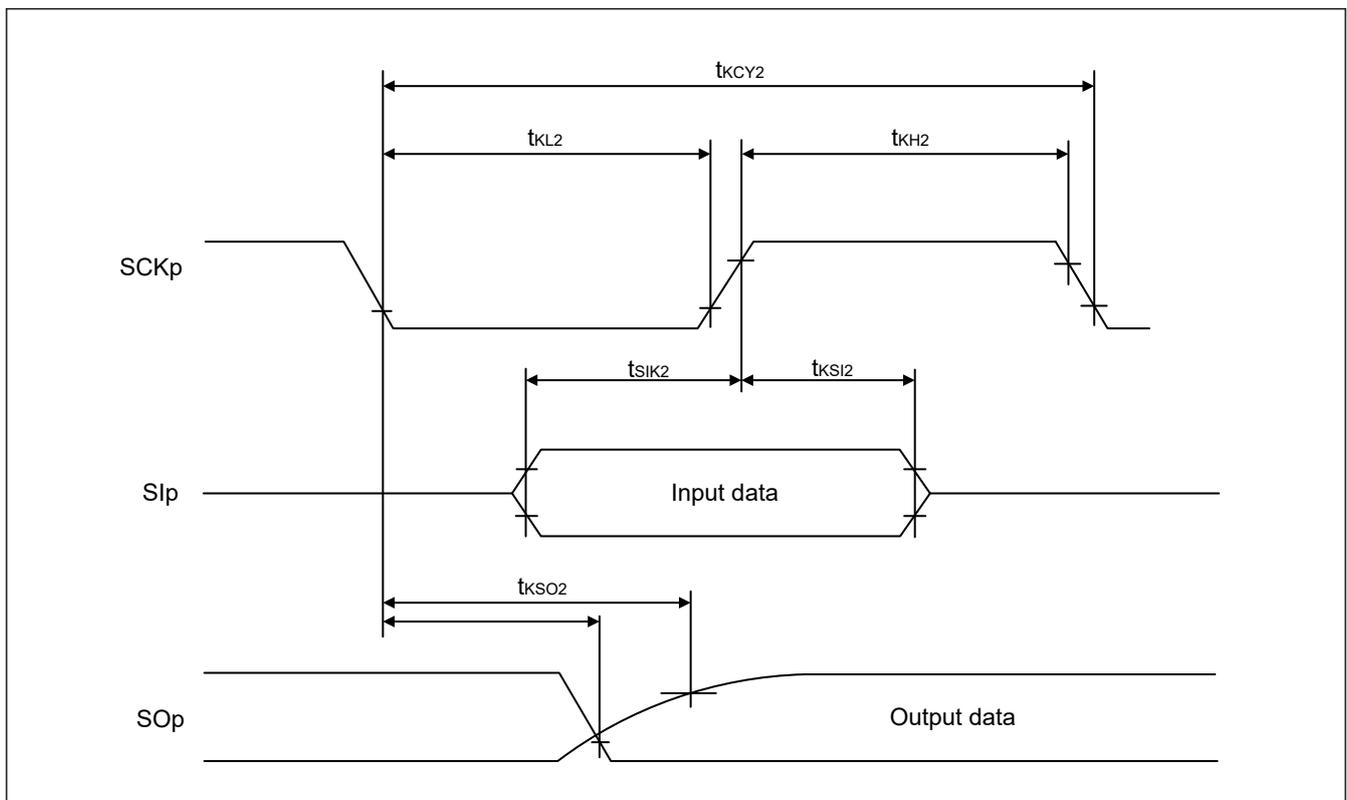
Figure 2.26 Timing of serial transfer in the simplified SPI communications in the slave mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 00b or 11b

Figure 2.27   Timing of serial transfer in the simplified SPI communications in the slave mode with devices operating at different voltage levels when SCRmn.DCP[1:0] = 01b or 10b

Note:
- p: Simplified SPI number (p = 00, 11), m: Unit number, n: Channel number (mn = 00, 03), gh: Port number (gh = 100 to 102, 108 to 110, 112, 201, 212, 213)

- Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Table 2.33 Simplified IIC communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) (1 of 2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode Min.	Max.	Middle-speed mode Min.	Max.	Low-speed mode Min.	Max.	Unit	Test Conditions
SCLr clock frequency	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	f_{SCL}	—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	Figure 2.29
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		—	1000[*1]	—	1000[*1]	—	300[*1]	kHz	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		—	400[*1]	—	400[*1]	—	300[*1]	kHz	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		—	300[*1]	—	300[*1]	—	300[*1]	kHz	
Hold time when SCLr is low	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{LOW}	475	—	475	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		475	—	475	—	1550	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		1150	—	1550	—	1550	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		1150	—	1550	—	1550	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		1550	—	1550	—	1550	—	ns	
Hold time when SCLr is high	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	t_{HIGH}	245	—	245	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		200	—	200	—	610	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		675	—	675	—	610	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		600	—	600	—	610	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		610	—	610	—	610	—	ns	

Table 2.33   Simplified IIC communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) (2 of 2)

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	High-speed mode		Middle-speed mode		Low-speed mode		Unit	Test Conditions
			Min.	Max.	Min.	Max.	Min.	Max.		
Data setup time (reception)	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{SU:DAT}$	$1/f_{MCK}$ + 135[*3]	—	$1/f_{MCK}$ + 135[*3]	—	$1/f_{MCK}$ + 190[*3]	—	ns	Figure 2.29
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		$1/f_{MCK}$ + 135[*3]	—	$1/f_{MCK}$ + 135[*3]	—	$1/f_{MCK}$ + 190[*3]	—	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		$1/f_{MCK}$ + 190[*3]	—	$1/f_{MCK}$ + 190[*3]	—	$1/f_{MCK}$ + 190[*3]	—	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		$1/f_{MCK}$ + 190[*3]	—	$1/f_{MCK}$ + 190[*3]	—	$1/f_{MCK}$ + 190[*3]	—	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		$1/f_{MCK}$ + 190[*3]	—	$1/f_{MCK}$ + 190[*3]	—	$1/f_{MCK}$ + 190[*3]	—	ns	
Data hold time (transmission)	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$t_{HD:DAT}$	0	305	0	305	0	305	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		0	305	0	305	0	305	ns	
	4.0 V ≤ VCC ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		0	355	0	355	0	355	ns	
	2.7 V ≤ VCC < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		0	355	0	355	0	355	ns	
	1.8 V ≤ VCC < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[*2], C_b = 100 pF, R_b = 5.5 kΩ		0	405	0	405	0	405	ns	

Note 1.   The listed times must be no greater than f_{MCK}/4.
Note 2.   Use this setting with VCC ≥ V_b.
Note 3.   Set f_{MCK} so that it does not exceed the hold time when SCLr is low or high.

Note: Select the TTL input buffer and the N-ch open drain output [withstand voltage of VCC] mode for the SDAr pin and the N-ch open drain output [withstand voltage of VCC] mode for the SCLr pin by using the Port gh Pin Function Select Register (PghPFS_A.PIM and PghPFS_A.NCODR). For V_{IH} and V_{IL}, see the DC characteristics with the TTL input buffer selected.
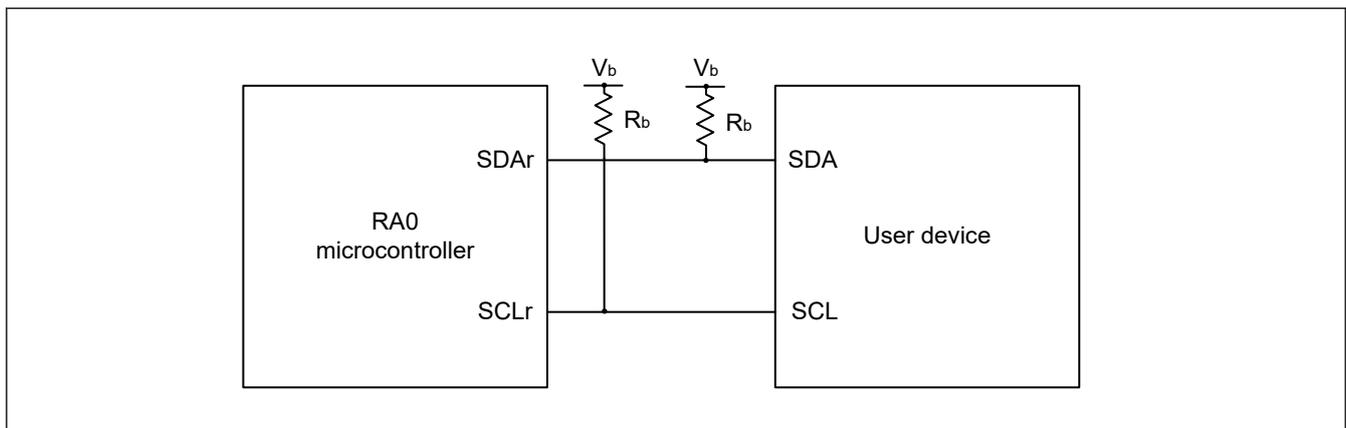
Figure 2.28   Connection in the IIC communications with devices operating at different voltage levels
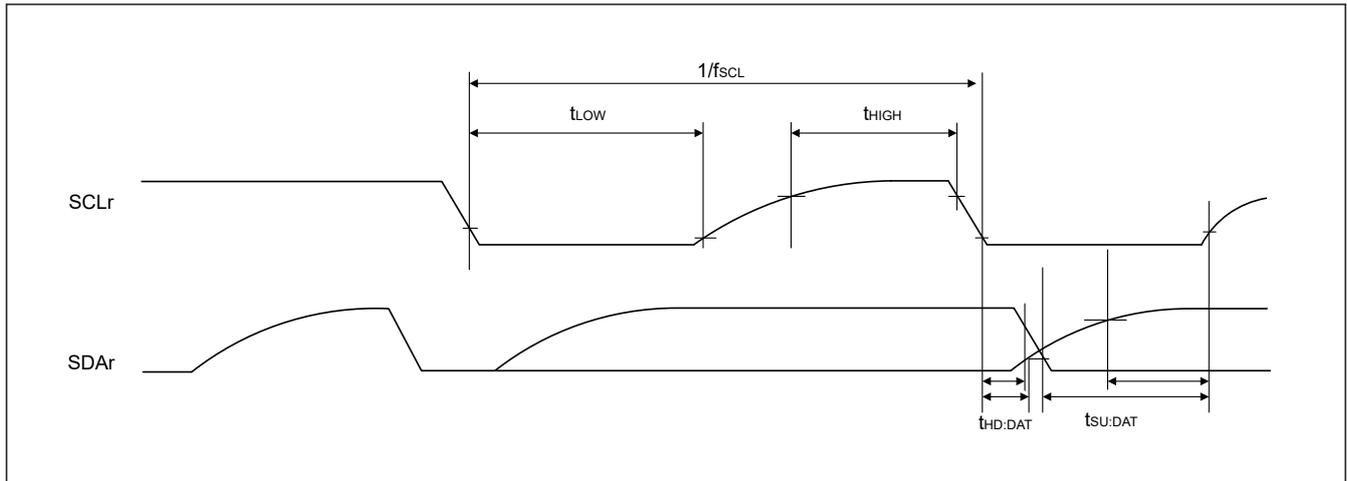
Figure 2.29   Timing of serial transfer in simplified IIC communications with devices operating at different voltage levels

Note: ● $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

● r: Simplified IIC number (r = 00, 11), gh: Port number (gh = 100, 102, 110, 112, 201, 212)

● f_{MCK}: Serial array unit operation clock frequency
To set this operating clock, use the CKS bit in the serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 03)

2.5.2 I^2C Bus Interface (IICA)

Table 2.34 I^2C standard mode

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Standard mode: PCLKB ≥ 1 MHz	f_{SCL}	0	—	100	kHz	Figure 2.30
Setup time of restart condition	—	$t_{SU:STA}$	4.7	—	—	µs	
Hold time[*1]	—	$t_{HD:STA}$	4	—	—	µs	
Hold time when SCLAn is low	—	t_{LOW}	4.7	—	—	µs	
Hold time when SCLAn is high	—	t_{HIGH}	4	—	—	µs	
Data setup time (reception)	—	$t_{SU:DAT}$	250	—	—	ns	
Data hold time (transmission)[*2]	—	$t_{HD:DAT}$	0	—	3.45	µs	
Setup time of stop condition	—	$t_{SU:STO}$	4	—	—	µs	
Bus-free time	—	t_{BUF}	4.7	—	—	µs	

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: n: Unit number (0)

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 400 pF, R_b = 2.7 kΩ

Table 2.35   I²C fast mode

Conditions: VCC = 1.8 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Fast mode: PCLKB ≥ 3.5 MHz 1.8 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	400	kHz	Figure 2.30
Setup time of restart condition	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:STA}$	0.6	—	—	µs	
Hold time[*1]	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.6	—	—	µs	
Hold time when SCLAn is low	1.8 V ≤ VCC ≤ 5.5 V	t_{LOW}	1.3	—	—	µs	
Hold time when SCLAn is high	1.8 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.6	—	—	µs	
Data setup time (reception)	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:DAT}$	100	—	—	ns	
Data hold time (transmission)[*2]	1.8 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.9	µs	
Setup time of stop condition	1.8 V ≤ VCC ≤ 5.5 V	$t_{SU:STO}$	0.6	—	—	µs	
Bus-free time	1.8 V ≤ VCC ≤ 5.5 V	t_{BUF}	1.3	—	—	µs	

Note 1.   The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2.   The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.

C_b = 320 pF, R_b = 1.1 kΩ

Table 2.36   I²C fast mode plus

Conditions: VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
SCLAn clock frequency	Fast mode plus: PCLKB ≥ 10 MHz 2.7 V ≤ VCC ≤ 5.5 V	f_{SCL}	0	—	1000	kHz	Figure 2.30
Setup time of restart condition	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:STA}$	0.26	—	—	µs	
Hold time[*1]	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:STA}$	0.26	—	—	µs	
Hold time when SCLAn is low	2.7 V ≤ VCC ≤ 5.5 V	t_{LOW}	0.5	—	—	µs	
Hold time when SCLAn is high	2.7 V ≤ VCC ≤ 5.5 V	t_{HIGH}	0.26	—	—	µs	
Data setup time (reception)	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:DAT}$	50	—	—	ns	
Data hold time (transmission)[*2]	2.7 V ≤ VCC ≤ 5.5 V	$t_{HD:DAT}$	0	—	0.45	µs	
Setup time of stop condition	2.7 V ≤ VCC ≤ 5.5 V	$t_{SU:STO}$	0.26	—	—	µs	
Bus-free time	2.7 V ≤ VCC ≤ 5.5 V	t_{BUF}	0.5	—	—	µs	

Note 1.   The first clock pulse is generated after this period when the start or restart condition is detected.
Note 2.   The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Note: Communications by using P212 and P213 with devices operating at different voltage levels are not possible since P212PFS_A and P213PFS_A registers do not have PIM bit.

Note: The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
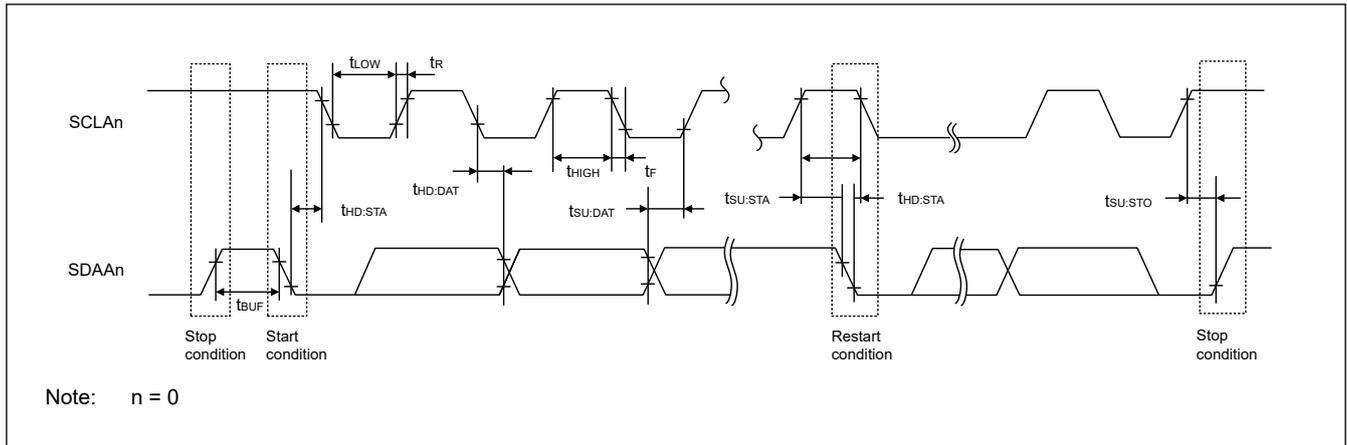
C_b = 120 pF, R_b = 1.1 kΩ

Note: n = 0

Figure 2.30   IICA serial transfer timing

2.6   Analog Characteristics

2.6.1   A/D Converter Characteristics for T_A = -40 to +85°C

Table 2.37   Reference for the characteristics of the A/D converter

Input channel	Reference Voltage		
	Reference voltage (+) = VREFH0 Reference voltage (–) = VREFL0	Reference voltage (+) = VCC Reference voltage (–) = VSS	Reference voltage (+) = V_{BGR} Reference voltage (–) = VREFL0
AN000, AN001, AN004, AN005	Refer to Table 2.38.	Refer to Table 2.40.	Refer to Table 2.41.
AN021, AN022	Refer to Table 2.39.		
Internal reference voltage Temperature sensor output voltage	Refer to Table 2.38.		—

Table 2.38   A/D conversion characteristics (AN004, AN005, internal reference voltage, and temperature sensor output voltage) (1 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN004, AN005, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[1][2][3]	AINL	—	1.2	±3.5	LSB	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±7.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[6]

Table 2.38 A/D conversion characteristics (AN004, AN005, internal reference voltage, and temperature sensor output voltage) (2 of 2)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN004, AN005, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Conversion time	t_{CONV}	2.125	—	39	µs	10-bit resolution Target pin: AN004, AN005	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	µs		1.6 V ≤ VCC ≤ 5.5 V
		2.375	—	39	µs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.50	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Full-scale error[1][2][3][4]	E_{FS}	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.50	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Integral linearity error[1][2][3]	ILE	—	—	±2.5	LSB	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±5.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Differential linearity error[1][2][3]	DLE	—	—	±1.5	LSB	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±2.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN004, AN005	
		V_{BGR}[7]			V	Internal reference voltage (1.8 V ≤ VCC ≤ 5.5 V)	
		V_{TMPS25}[7]			V	Temperature sensor output voltage (1.8 V ≤ VCC ≤ 5.5 V)	

Note 1.   The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2.   These values are the results of characteristic evaluation and are not checked for shipment.
Note 3.   This value does not include the quantization error (±1/2 LSB).
Note 4.   This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5.   When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ± 1.0 LSB to the maximum value when VCC = VREFH0.
- Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when VCC = VREFH0.
- Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Note 6. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 µs and 95 µs.

Note 7. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

Table 2.39   A/D conversion characteristics (AN021 to AN022)

Conditions: 1.6 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN021 to AN022
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[1][2][3]	AINL	—	1.2	±5.0	LSB	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±8.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Conversion time	tCONV	2.125	—	39	µs	10-bit resolution Target pin: AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	µs		1.6 V ≤ VCC ≤ 5.5 V
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.60	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Full-scale error[1][2][3][4]	E_{FS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±0.60	%FSR		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Integral linearity error[1][2][3]	ILE	—	—	±3.5	LSB	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±6.0	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Differential linearity error[1][2][3]	DLE	—	—	±2.0	LSB	10-bit resolution VREFH0 = VCC[5]	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	—	±2.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[6]
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN021, AN022	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.

Note 2. These values are the results of characteristic evaluation and are not checked for shipment.

Note 3. This value does not include the quantization error (±1/2 LSB).

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 5. When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ± 1.0 LSB to the maximum value when VCC = VREFH0.

- Zero-scale/full-scale error: Add ±0.05% FSR to the maximum value when VCC = VREFH0.
- Integral linearity error/differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Note 6. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 µs and 95 µs.

Table 2.40   A/D conversion characteristics (AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage) (1 of 2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage[7], and temperature sensor output voltage[7]
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[1][2][3]	AINL	—	1.2	±7.0	LSB	10-bit resolution	1.8 V ≤ VREFH0 ≤ 5.5 V
		—	1.2	±10.5	LSB		1.6 V ≤ VREFH0 ≤ 5.5 V[5]
Conversion time	tCONV	2.125	—	39	µs	10-bit resolution Target pin: AN000, AN001, AN004, AN005, AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
		57	—	95	µs		1.6 V ≤ VCC ≤ 5.5 V
		2.375	—	39	µs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		1.8 V ≤ VCC ≤ 5.5 V
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.60	%FSR	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±0.85	%FSR		1.6 V ≤ VCC ≤ 5.5 V[5]
Full-scale error[1][2][3][4]	E_{FS}	—	—	±0.60	%FSR	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±0.85	%FSR		1.6 V ≤ VCC ≤ 5.5 V[5]
Integral linearity error[1][2][3]	ILE	—	—	±4.0	LSB	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±6.0	LSB		1.6 V ≤ VCC ≤ 5.5 V[5]
Differential linearity error[1][2][3]	DLE	—	—	±2.0	LSB	10-bit resolution	1.8 V ≤ VCC ≤ 5.5 V
		—	—	±2.5	LSB		1.6 V ≤ VCC ≤ 5.5 V[5]

Table 2.40   A/D conversion characteristics (AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage) (2 of 2)

Conditions: 1.6 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage[7], and temperature sensor output voltage[7]
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Analog input voltage	V_{AIN}	0	—	VCC	V	AN000, AN001, AN004, AN005, AN021, AN022
		V_{BGR}[6]			V	Internal reference voltage (1.8 V ≤ VCC ≤ 5.5 V)
		V_{TMPS25}[6]			V	Temperature sensor output voltage (1.8 V ≤ VCC ≤ 5.5 V)

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 µs and 95 µs.
Note 6. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.
Note 7. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VCC must be at least 1.8 V.

Table 2.41   A/D conversion characteristics (AN000, AN004, AN005, AN021, AN022)

Conditions: 1.8 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +85°C
Reference voltage range applied to the VBGR (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).
Target pins: AN000, AN004, AN005, AN021, AN022
(Reference voltage (+) = V_{BGR}[5], Reference voltage (–) = VREFL0[6] = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resolution	RES	8			bit	—
Conversion time	tCONV	17	—	39	µs	—
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.60	%FSR	—
Integral linearity error[1][2][3]	ILE	—	—	±2.0	LSB	—
Differential linearity error[1][2][3]	DLE	—	—	±1.0	LSB	—
Analog input voltage	V_{AIN}	0	—	V_{BGR}[5]	V	—

Note 1. The Typ. value is an average value at TA = 25°C. The MAX. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.
Note 6. ● Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (–) = VREFL0.
         ● Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (–) = VREFL0.
         ● Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (–) = VREFL0.

2.6.2   A/D Converter Characteristics for T_A = -40 to +125°C

Table 2.42   Reference for the characteristics of the A/D converter

Input channel	Reference Voltage		
	Reference voltage (+) = VREFH0 Reference voltage (–) = VREFL0	Reference voltage (+) = VCC Reference voltage (–) = VSS	Reference voltage (+) = V_{BGR} Reference voltage (–) = VREFL0
AN000, AN001, AN004, AN005	Refer to Table 2.43.	Refer to Table 2.45.	Refer to Table 2.46.
AN021, AN022	Refer to Table 2.44.		
Internal reference voltage Temperature sensor output voltage	Refer to Table 2.43.		—

Table 2.43   A/D conversion characteristics

Conditions: 2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN004, AN005, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[1][2][3]	AINL	—	1.2	±3.5	LSB	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Conversion time	tCONV	2.125	—	39	µs	10-bit resolution Target pin: AN004, AN005	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		2.4 V ≤ VCC ≤ 5.5 V
		2.375	—	39	µs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		2.4 V ≤ VCC ≤ 5.5 V
Zero-scale error[1][2][3][4]	EZS	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Full-scale error[1][2][3][4]	EFS	—	—	±0.25	%FSR	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Integral linearity error[1][2][3]	ILE	—	—	±2.5	LSB	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Differential linearity error[1][2][3]	DLE	—	—	±1.5	LSB	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Analog input voltage	VAIN	0	—	VREFH0	V	AN004, AN005	
		VBGR[6]			V	Internal reference voltage	
		VTMPS25[6]			V	Temperature sensor output voltage	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ±1.0 LSB to the maximum value when VCC = VREFH0.
- Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when VCC = VREFH0.
- Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Note 6. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

Table 2.44   A/D conversion characteristics (AN021 to AN022)

Conditions: 2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VREFH0 (ADREFP[1:0] = 01b) and VREFL0 (ADREFM = 1b).
Target pins: AN021 to AN022
(Reference voltage (+) = VREFH0, Reference voltage (–) = VREFL0 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[1][2][3]	AINL	—	1.2	±5.0	LSB	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Conversion time	tCONV	2.125	—	39	µs	10-bit resolution Target pin: AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	µs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	µs		2.4 V ≤ VCC ≤ 5.5 V
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Full-scale error[1][2][3][4]	E_{FS}	—	—	±0.35	%FSR	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Integral linearity error[1][2][3]	ILE	—	—	±3.5	LSB	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Differential linearity error[1][2][3]	DLE	—	—	±2.0	LSB	10-bit resolution VREFH0 = VCC[5]	2.4 V ≤ VREFH0 ≤ 5.5 V
Analog input voltage	V_{AIN}	0	—	VREFH0	V	AN021, AN022	

Note 1.   The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2.   These values are the results of characteristic evaluation and are not checked for shipment.
Note 3.   This value does not include the quantization error (±1/2 LSB).
Note 4.   This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5.   When VREFH0 < VCC, the maximum values are as follows.

- Overall error: Add ±1.0 LSB to the maximum value when VCC = VREFH0.
- Zero-scale/full-scale error: Add ±0.05%FSR to the maximum value when VCC = VREFH0.
- Integral linearity error and differential linearity error: Add ±0.5 LSB to the maximum value when VCC = VREFH0.

Table 2.45   A/D conversion characteristics (1 of 2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Resolution	RES	8	—	10	bit	—	
Overall error[1][2][3]	AINL	—	1.2	±7.0	LSB	10-bit resolution	2.4 V ≤ VREFH0 ≤ 5.5 V

Table 2.45 A/D conversion characteristics (2 of 2)

Conditions: 2.4 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VCC (ADREFP[1:0] = 00b) and VSS (ADREFM = 0b).
Target pins: AN000, AN001, AN004, AN005, AN021, AN022, internal reference voltage, and temperature sensor output voltage
(Reference voltage (+) = VCC, Reference voltage (–) = VSS)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Conversion time	tCONV	2.125	—	39	μs	10-bit resolution Target pin: AN000, AN001, AN004, AN005, AN021, AN022	3.6 V ≤ VCC ≤ 5.5 V
		3.1875	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
		2.375	—	39	μs	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ VCC ≤ 5.5 V
		3.5625	—	39	μs		2.7 V ≤ VCC ≤ 5.5 V
		17	—	39	μs		2.4 V ≤ VCC ≤ 5.5 V
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.60	%FSR	10-bit resolution	2.4 V ≤ VCC ≤ 5.5 V
Full-scale error[1][2][3][4]	E_{FS}	—	—	±0.60	%FSR	10-bit resolution	2.4 V ≤ VCC ≤ 5.5 V
Integral linearity error[1][2][3]	ILE	—	—	±4.0	LSB	10-bit resolution	2.4 V ≤ VREFH0 ≤ 5.5 V
Differential linearity error[1][2][3]	DLE	—	—	±2.0	LSB	10-bit resolution	2.4 V ≤ VREFH0 ≤ 5.5 V
Analog input voltage	V_{AIN}	0	—	VCC	V	AN000, AN001, AN004, AN005, AN021, AN022	
		V_{BGR}[5]			V	Internal reference voltage	
		V_{TMPS25}[5]			V	Temperature sensor output voltage	

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).
Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.
Note 5. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

Table 2.46 A/D conversion characteristics (AN000, AN004, AN005, AN021, AN022)

Conditions: 2.4 V ≤ VREFH0 ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C
Reference voltage range applied to the VBGR (ADREFP[1:0] = 10b) and VREFL0 (ADREFM = 1b).
Target pins: AN000, AN004, AN005, AN021, AN022
(Reference voltage (+) = V_{BGR}[5], Reference voltage (–) = VREFL0[6] = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resolution	RES	8			bit	—
Conversion time	tCONV	17	—	39	μs	—
Zero-scale error[1][2][3][4]	E_{ZS}	—	—	±0.60	%FSR	—
Integral linearity error[1][2][3]	ILE	—	—	±2.0	LSB	—
Differential linearity error[1][2][3]	DLE	—	—	±1.0	LSB	—
Analog input voltage	V_{AIN}	0	—	V_{BGR}[5]	V	—

Note 1. The Typ. value is an average value at TA = 25°C. The Max. value is an average value ±3σ at normal distribution.
Note 2. These values are the results of characteristic evaluation and are not checked for shipment.
Note 3. This value does not include the quantization error (±1/2 LSB).

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 5. See section 2.6.3. Temperature Sensor/Internal Reference Voltage Characteristics.

Note 6.
- Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (−) = VREFL0.
- Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (−) = VREFL0.
- Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (−) = VREFL0.

2.6.3 Temperature Sensor/Internal Reference Voltage Characteristics

Table 2.47 Temperature sensor/internal reference voltage characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Temperature sensor output voltage	V_{TMPS25}	—	1.05	—	V	at = 25°C
Internal reference voltage	V_{BGR}	1.40	1.48	1.56	V	—
Temperature coefficient	F_{VTMPS}	—	-3.3	—	mV/°C	—
Operation stabilization wait time	t_{AMP}	5	—	—	µs	—

2.6.4 POR Characteristics

Table 2.48 POR characteristics

Conditions: VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	VPOR VPDR	1.43	1.50	1.57	V	—
Minimum pulse width[1]	TPW	300	—	—	µs	—

Note 1. This width is the minimum time required for a POR reset when VCC falls below VPDR. This width is also the minimum time required for a POR reset from when VCC falls below 0.7 V to when VCC exceeds VPOR in the Software standby mode or while the main system clock is stopped through setting HOCOCR.HCSTOP bit.
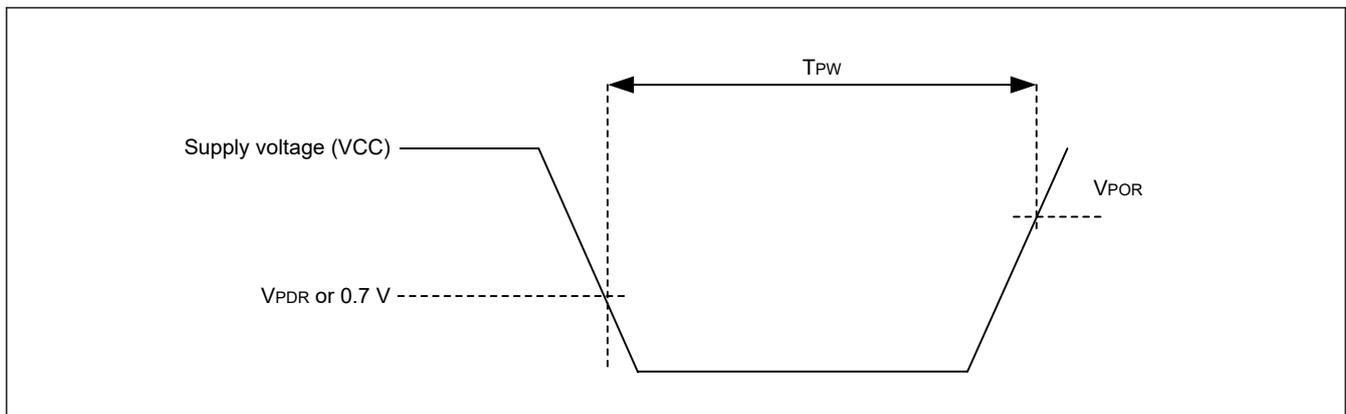
Figure 2.31 Minimum VCC pulse width

2.6.5 LVD Characteristics

Table 2.49 LVD0 characteristics

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det0_0}	3.84	3.96	4.08	V	The power supply voltage is rising.
			3.76	3.88	4.00	V	The power supply voltage is falling.
		V_{det0_1}	2.88	2.97	3.06	V	The power supply voltage is rising.
			2.82	2.91	3.00	V	The power supply voltage is falling.
		V_{det0_2}	2.59	2.67	2.75	V	The power supply voltage is rising.
			2.54	2.62	2.70	V	The power supply voltage is falling.
		V_{det0_3}	2.31	2.38	2.45	V	The power supply voltage is rising.
			2.26	2.33	2.40	V	The power supply voltage is falling.
		V_{det0_4}	1.84	1.90	1.95	V	The power supply voltage is rising.
			1.80	1.86	1.91	V	The power supply voltage is falling.
		V_{det0_5}	1.64	1.69	1.74	V	The power supply voltage is rising.
			1.60	1.65	1.70	V	The power supply voltage is falling.
Minimum pulse width		t_{LW0}	500	—	—	µs	—
Detection delay time		t_{det0}	—	—	500	µs	—

Table 2.50 LVD1 characteristics (1 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_0}	4.08	4.16	4.24	V	The power supply voltage is rising.
			4.00	4.08	4.16	V	The power supply voltage is falling.
		V_{det1_1}	3.88	3.96	4.04	V	The power supply voltage is rising.
			3.80	3.88	3.96	V	The power supply voltage is falling.
		V_{det1_2}	3.68	3.75	3.82	V	The power supply voltage is rising.
			3.60	3.67	3.74	V	The power supply voltage is falling.
		V_{det1_3}	3.48	3.55	3.62	V	The power supply voltage is rising.
			3.40	3.47	3.54	V	The power supply voltage is falling.
		V_{det1_4}	3.28	3.35	3.42	V	The power supply voltage is rising.
			3.20	3.27	3.34	V	The power supply voltage is falling.
		V_{det1_5}	3.07	3.13	3.19	V	The power supply voltage is rising.
			3.00	3.06	3.12	V	The power supply voltage is falling.
		V_{det1_6}	2.91	2.97	3.03	V	The power supply voltage is rising.
			2.85	2.91	2.97	V	The power supply voltage is falling.
		V_{det1_7}	2.76	2.82	2.87	V	The power supply voltage is rising.
			2.70	2.76	2.81	V	The power supply voltage is falling.
		V_{det1_8}	2.61	2.66	2.71	V	The power supply voltage is rising.
			2.55	2.60	2.65	V	The power supply voltage is falling.
		V_{det1_9}	2.45	2.50	2.55	V	The power supply voltage is rising.
			2.40	2.45	2.50	V	The power supply voltage is falling.
		V_{det1_A}	2.35	2.40	2.45	V	The power supply voltage is rising.
			2.30	2.35	2.40	V	The power supply voltage is falling.

Table 2.50   LVD1 characteristics (2 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_B}	2.25	2.30	2.34	V	The power supply voltage is rising.
			2.20	2.25	2.29	V	The power supply voltage is falling.
		V_{det1_C}	2.15	2.20	2.24	V	The power supply voltage is rising.
			2.10	2.15	2.19	V	The power supply voltage is falling.
		V_{det1_D}	2.05	2.09	2.13	V	The power supply voltage is rising.
			2.00	2.04	2.08	V	The power supply voltage is falling.
		V_{det1_E}	1.94	1.98	2.02	V	The power supply voltage is rising.
			1.90	1.94	1.98	V	The power supply voltage is falling.
		V_{det1_F}	1.84	1.88	1.91	V	The power supply voltage is rising.
			1.80	1.84	1.87	V	The power supply voltage is falling.
		V_{det1_10}	1.74	1.78	1.81	V	The power supply voltage is rising.
			1.70	1.74	1.77	V	The power supply voltage is falling.
		V_{det1_11}	1.64	1.67	1.70	V	The power supply voltage is rising.
			1.60	1.63	1.66	V	The power supply voltage is falling.
Minimum pulse width		t_{LW1}	500	—	—	µs	—
Detection delay time		t_{det1}	—	—	500	µs	—
LVD1 detection voltage stabilization time (after changing the LVD1 detection voltage)		$t_{d(E-A)}$	—	—	1500	µs	—
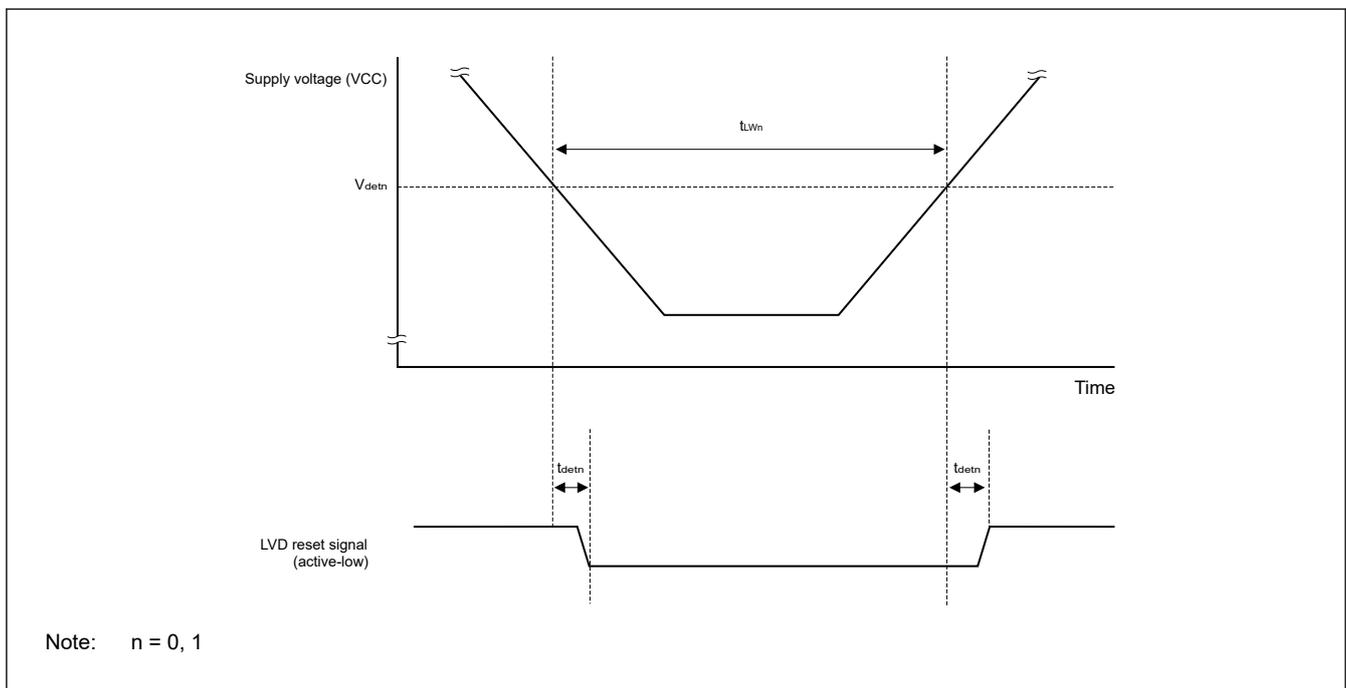
Figure 2.32   Voltage detection circuit timing

2.6.6 Power Supply Voltage Rising Slope Characteristics

Table 2.51   Power supply voltage rising slope characteristics

Conditions: VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage rising slope	S_{VCC}	—	—	54	V/ms	—

Note: Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VCC reaches the operating voltage range shown in AC characteristics.
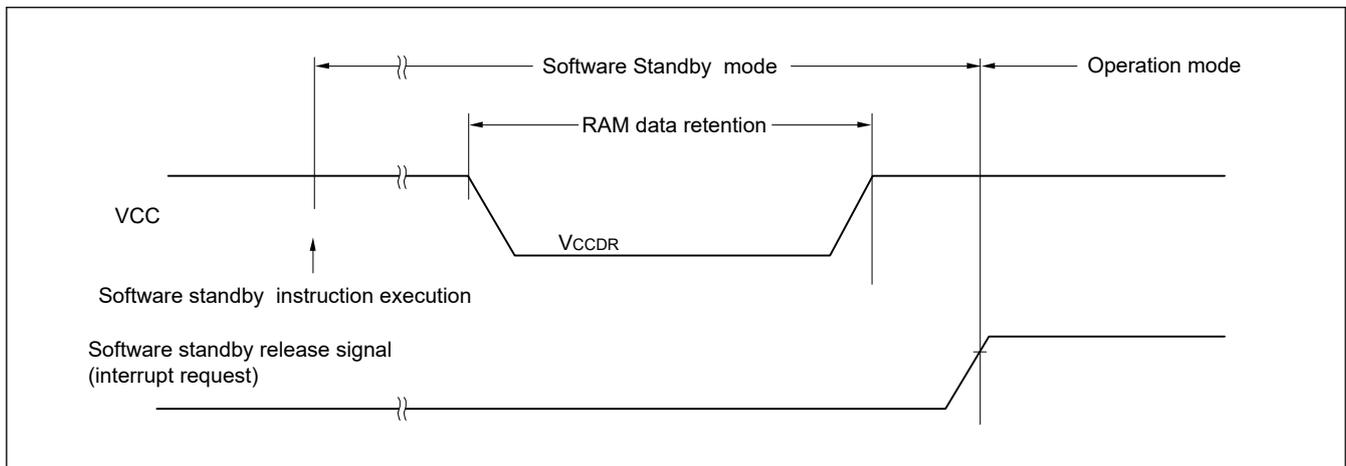
2.7 RAM Data Retention Characteristics

Table 2.52   RAM data retention characteristics

Conditions: VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	1.43[*1]	—	5.5	V	—

Note 1.   This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.

Figure 2.33   RAM data retention

2.8 Flash Memory Programming Characteristics

Table 2.53   Flash memory programming characteristics

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CPU/peripheral hardware clock frequency	I_{CLK}	1	—	32	MHz	—
Number of code flash rewrites[*1] [*2] [*3]	Cerwr	10000	—	—	Times	Retained for 10 years Ta = 85°C
		1000	—	—		Retained for 20 years Ta = 85°C

Note 1.   1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
Note 2.   The listed numbers of times apply when using the flash memory programmer and self-programming.
Note 3.   These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Table 2.54   Code flash memory characteristics (1 of 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs

Table 2.54   Code flash memory characteristics (2 of 2)

Conditions: 1.8 V ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +125°C

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz, 3 MHz			4 MHz ≤ ICLK < 8 MHz			8 MHz ≤ ICLK < 32 MHz			ICLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Security setting time		t_{AWSSAS}	—	18.0	525.5	—	14.3	468.7	—	12.5	440.7	—	11.6	426.7	—	11.3	422.3	ms
Time until programming starts following cancellation of the Software standby instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	2	—	—	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	15	—	—	15	—	—	15	—	—	µs

Note: The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9   Serial Wire Debug (SWD)

Table 2.55   SWD characteristics (1)

Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.34
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SECKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.35
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.56   SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

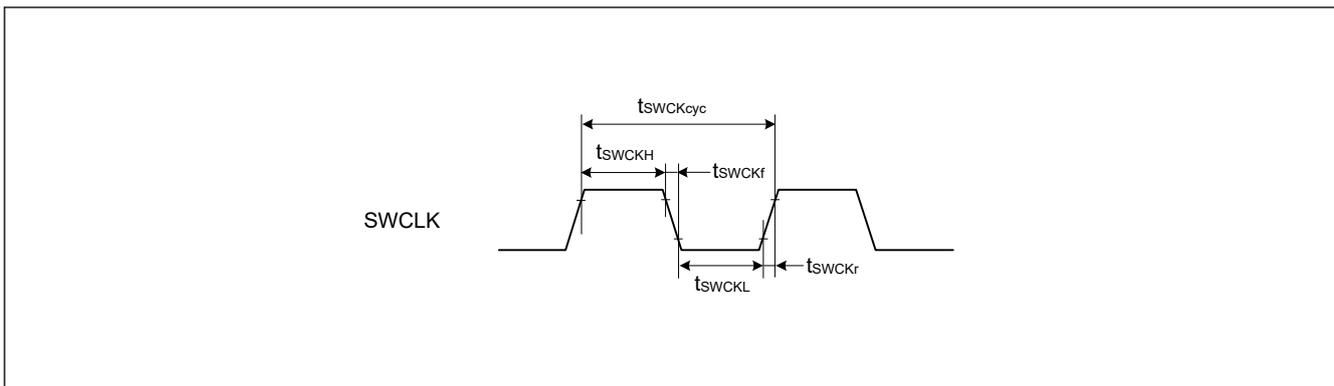| Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.34
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SECKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.35
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

Figure 2.34   SWD SWCLK timing
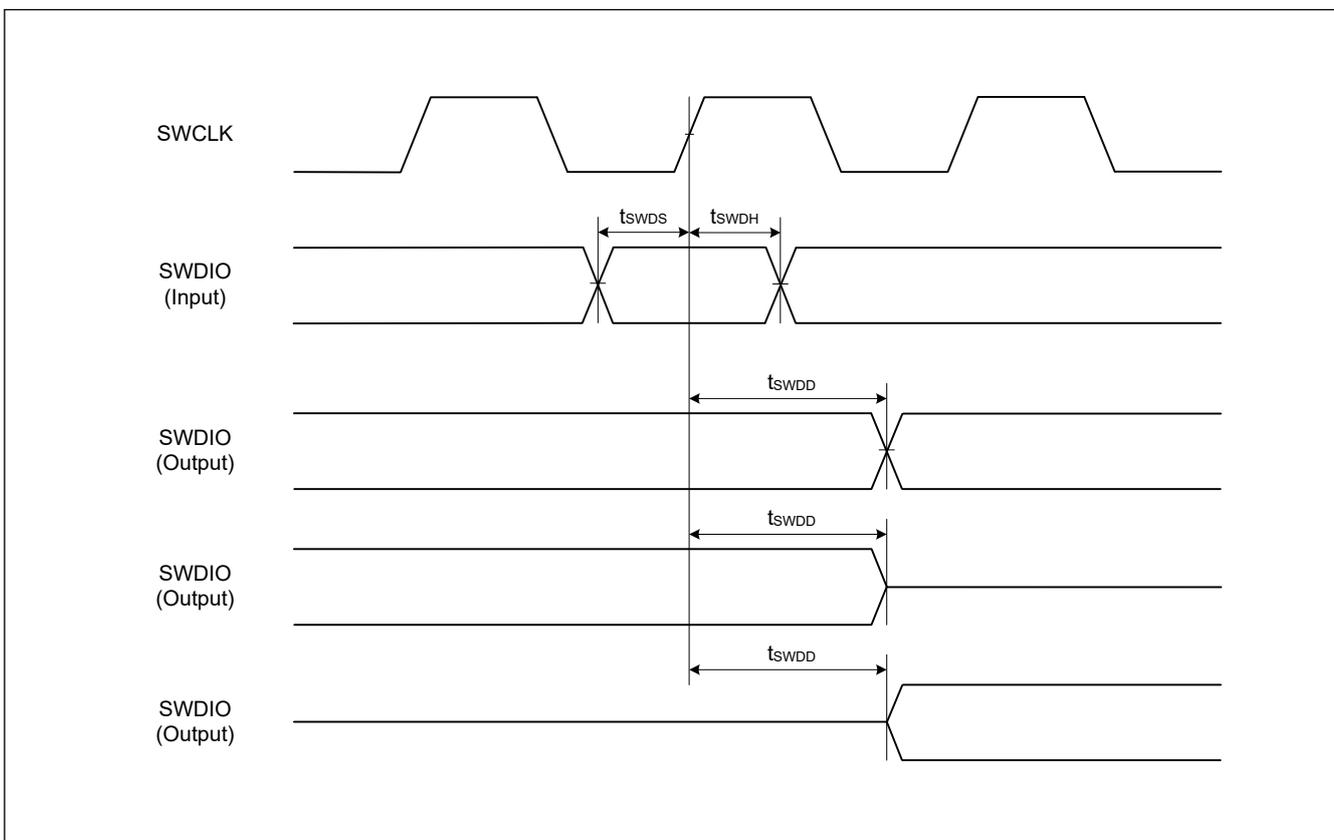
Figure 2.35   SWD input/output timing

Appendix 1. Port States in each Processing Mode

Table A1.1 Port states in each processing mode (1 of 2)

Port name	Reset	Software Standby Mode
P010/VREFH0/AN000	Hi-Z	Keep-O
P011/VREFL0/AN001	Hi-Z	Keep-O
P012/AN004	Hi-Z	Keep-O
P013/AN005	Hi-Z	Keep-O
P100/AN022/IRQ2_A/TI04_A/TO04_A/TI01_B/TO01_B/RXD0_A/SI00_A/SDA00_A/SCLA0_D	Hi-Z	[IRQ2_A selected] IRQ2_A input [SCLA0_D selected] SCLA0_D inout [Other than the above] Keep-O
P101/AN021/IRQ3_A/TI07_A/TO07_A/TI00_C/TXD0_A/SO00_A/SDAA0_D	Hi-Z	[IRQ3_A selected] IRQ3_A input [SDAA0_D selected] SDAA0_D inout [Other than the above] Keep-O
P102/IRQ4_A/TI06_A/TO06_A/TO00_C/PCLBUZ0_B/SCK00_A/SCL00_A	Hi-Z	[IRQ4_A selected] IRQ4_A input [PCLBUZ0_B selected] PCLBUZ0_B output [Other than the above] Keep-O
P108/SWDIO/TI03_B/TO03_B/PCLBUZ0_D/SCLA0_E/SCK00_C	Pull-up	[SCLA0_E selected] SCLA0_E inout [PCLBUZ0_D selected] PCLBUZ0_D output Keep-O
P109/IRQ4_B/TI02_A/TO02_A/TXD0_B/SO00_B/SDAA0_C	Hi-Z	[IRQ4_B selected] IRQ4_B input [SDAA0_C selected] SDAA0_C inout [Other than the above] Keep-O
P110/IRQ3_B/TI01_A/TO01_A/RXD0_B/SI00_B/SDA00_B/SCLA0_C	Hi-Z	[IRQ3_B selected] IRQ3_B input [SCLA0_C selected] SCLA0_C inout [Other than the above] Keep-O
P112/IRQ2_B/TI03_A/TO03_A/SCK00_B/SCL00_B/SSI00_C	Hi-Z	[IRQ2_B selected] IRQ2_B input [Other than the above] Keep-O
P200/NMI/IRQ0_A/TI06_B/SSI00_D/RXD1_B	Hi-Z	[NMI/IRQ0_A selected] NMI/IRQ0_A input [Other than the above] Hi-Z
P201/IRQ5_B/TI05_B/TO05_B/PCLBUZ0_A/SSI00_B/SCK11_B/SCL11_B	Hi-Z	[IRQ5_B selected] IRQ5_B input [PCLBUZ0_A selected] PCLBUZ0_A output [Other than the above] Keep-O

Table A1.1   Port states in each processing mode (2 of 2)

Port name	Reset	Software Standby Mode
P206/RES/IRQ1_C	Pull-up	[IRQ1_C selected] IRQ1_C input [RES (OFS1.PORTSELB = 1) selected] RES input [P206 (OFS1.PORTSELB = 0) selected] Keep-O
P212/IRQ1_B/TO00_A/TI03_C/TO03_C/RXD1_A/SI11_A/SDA11_A/SCLA0_B	Hi-Z	[IRQ1_B selected] IRQ1_B input [SCLA0_B selected] SCLA0_B inout [Other than the above] Keep-O
P213/IRQ0_B/TI00_A/TI02_B/TO02_B/TXD1_A/SO11_A/SDAA0_B	Hi-Z	[IRQ0_B selected] IRQ0_B input [SDAA0_B selected] SDAA0_B inout [Other than the above] Keep-O
P300/SWCLK/TI04_B/TO04_B/SDAA0_E/TXD1_B	Pull-up	[SDAA0_E selected] SDAA0_E inout [Other than the above] Keep-O

Note: Hi-Z: High-impedance
          Keep-O: Output pins retain their previous values. Input pins become high-impedance.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in "Packages" on the Renesas Electronics Corporation website.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TSSOP20-4.40x6.50-0.65	PTSP0020JI-A	0.08

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	0.127	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	—	—
θ	0°	—	8°
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		

NOTES:
1. DIMENSION 'D' AND 'E1' DOES NOT INCLUDE MOLD FLASH.
2. DIMENSION 'b' DOES NOT INCLUDE TRIM OFFSET.
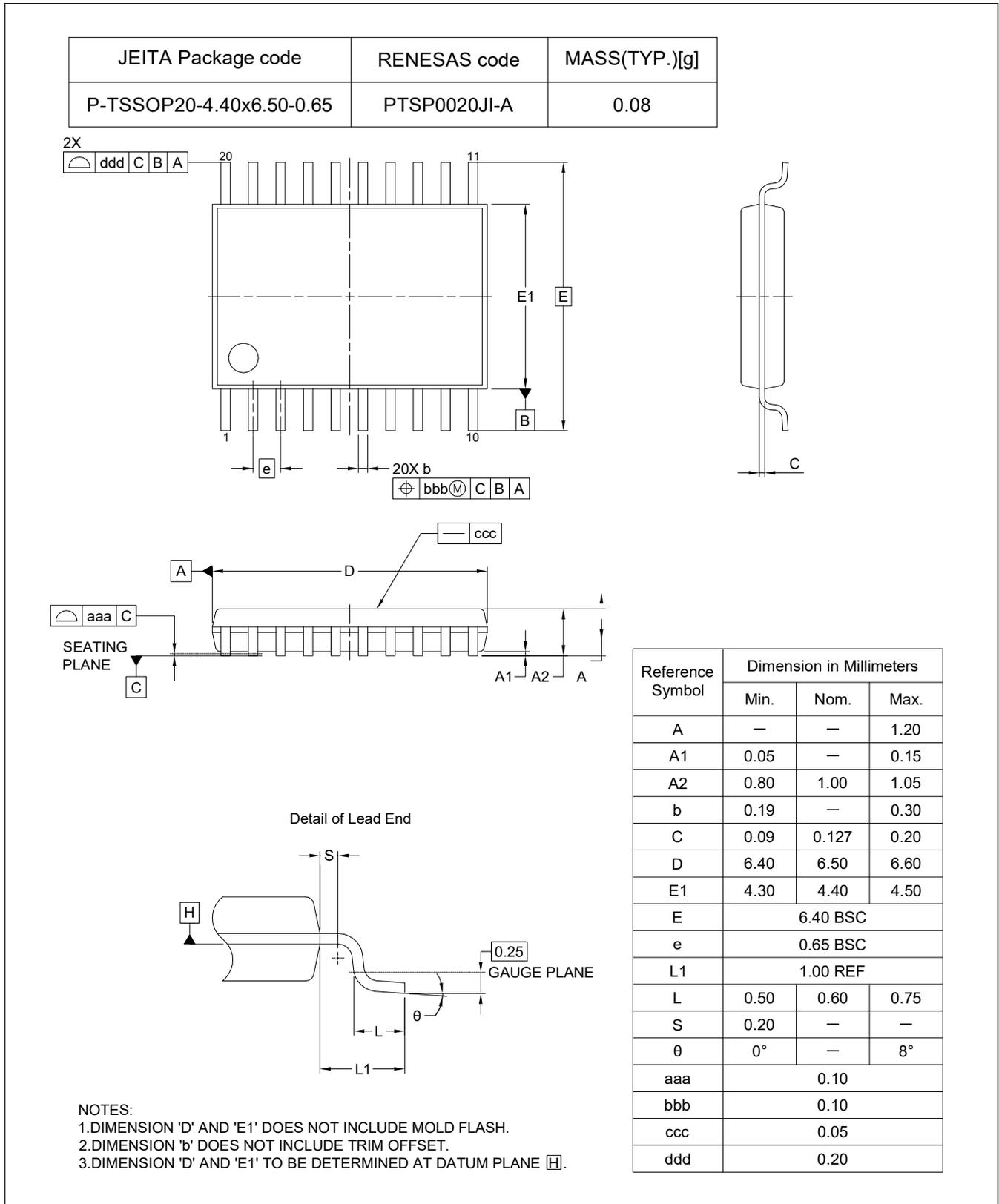3. DIMENSION 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

Figure A2.1   TSSOP 20-pin

Appendix 3.   I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1   Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1   Peripheral base address

Name	Description	Base address
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
IWDT	Independent Watchdog Timer	0x4004_4400
MSTP	Module Stop Control	0x4004_7000
CRC	CRC Calculator	0x4007_4000
PORT0	Port 0 Control	0x400A_0000
PORT1	Port 1 Control	0x400A_0020
PORT2	Port 2 Control	0x400A_0040
PORT3	Port 3 Control	0x400A_0060
PFS_A	Pmn Pin Function Select	0x400A_0200
PORGA	Product Organize	0x400A_1000
ADC_D	10-bit A/D Converter	0x400A_1800
SAU0	Serial Array Unit 0	0x400A_2000
TAU	Timer Array Unit	0x400A_2600
IICA	I^{2}C Bus Interface	0x400A_3000
TML32	32-bit Interval Timer	0x400A_3800
PCLBUZ	Clock Output/Buzzer Output Controller	0x400A_3B00
FLCN	Flash I/O Registers	0x407E_C000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2   Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table A3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

shows the register access cycles.

Table A3.2   Access cycles

Peripherals	Address		Number of access cycles			Related function
	From	To	Read	Write	Cycle unit	
BUS, DTC, ICU, DBG	0x4000_3000	0x4001_BFFF	3		ICLK	Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSC	0x4001_E000	0x4001_E6FF	2		ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
IWDT, MSTP	0x4004_0000	0x4004_7FFF	3		PCLKB	Watchdog Timer, Module Stop Control
CRC	0x4007_4000	0x4007_4FFF	3		PCLKB	CRC Calculator
PORT, PFS_A, PORGA, ADC10, SAU0, TAU, IICA, TML32, PCLBUZ	0x400A_0000	0x400A_3FFF	2		PCLKB	I/O Ports, 10-bit A/D Converter, Serial Array Unit 0, Timer Array Unit, I^{2}C Bus Interface, 32-bit Interval Timer, Clock/ Buzzer Output Controller
FLCN	0x407E_C000	0x407E_FFFF	7		ICLK	Flash Control

Appendix 4. Peripheral Variant

Table A4.1 shows the correspondence between the module name used in this manual and the peripheral variant.

Table A4.1 Module name vs peripheral variant

Module name	Peripheral variant
ADC10	ADC_D

Revision History

Revision 1.00 — Oct 29, 2025

Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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