RA4C1 Group
Renesas Microcontrollers

R01DS0457EJ0110
Rev.1.10
Jul 4, 2025

The RA4C1 group are low power, 32-bit microcontrollers (MCUs) based on the Arm® Cortex®-M33 (CM33) core with TrustZone®, delivering an ideal balance of low voltage operation, low power consumption and high performance combined with an advanced security engine needed by many security sensitive applications. The RA4C1 offers up to 512 KB of code flash memory, 8 KB of data flash memory and 96 KB of SRAM. The RA4C1 offers a wide range of peripheral features including 2 × I²C, CANFD, 3 × SPI, Quad SPI, a segment LCD controller and an RTC with independent power supply, and comes in 64 and 100 pin LQFP packages.

Features

■ Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 80 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

■ Memory

- Up to 512 KB code flash memory
- 8 KB data flash memory (100,000 program/erase (P/E) cycles)
- 96 KB SRAM

■ Connectivity

- Serial Communications Interface (SCI) × 6
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Simple LIN (SCI1)
  - Manchester coding (SCI3, SCI4)
- IrDA interface (IrDA)
- I²C bus interface (IIC) × 2
- Serial Interface UARTA (UARTA) × 2
- Serial Peripheral Interface (SPI) × 3
- Quad Serial Peripheral Interface (QSPI)
- CAN with Flexible Data-rate (CANFD)

■ Analog

- 12-bit A/D Converter (ADC12)
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-bit (GPT32) × 2
- General PWM Timer 16-bit (GPT16) × 4
- Low Power Asynchronous General Purpose Timer (AGT) × 2

■ Security and Encryption

- Renesas Secure IP (RSIP-E31A)
  - Symmetric algorithms: AES
  - Asymmetric algorithms: ECC
  - Hash-value generation: SHA224, SHA256
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to three or six regions for the code flash, depending on the bank mode
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- Device lifecyle management
- Pin function
  - Up to three tamper pins
  - Secure pin multiplexing

■ System and Power Management

- Low power modes
- Independent power supply Realtime Clock (RTC)
- Independent power supply (VRTC) domain power-on reset (VRTC_POR) circuit
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Low Voltage Detection for EXLVDVBAT pin
- Low Voltage Detection for VRTC pin
- Low Voltage Detection for EXLVD pin
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

■ Human Machine Interface (HMI)

- Segment LCD Controller (SLCDC)

■ Multiple Clock Sources

- Main clock oscillator (MOSC) (1 to 20 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (48/64/80 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- PLL_RTC
- Clock out support

■ General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up

■ Operating Voltage

- VCC: 1.6 to 3.6 V

■ Operating Temperature and Packages

- Ta = -40 °C to +105 °C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 80 MHz with the following features:

- Up to 512 KB code flash memory
- 96 KB SRAM
- Quad Serial Peripheral Interface (QSPI)
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 80 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel1 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB of code flash memory.
Data flash memory	8 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/SWD boot mode
Resets	The MCU provides 13 resets.

Table 1.3 System (2 of 2)

Feature	Functional description
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the following pins: ● VCC ● EXLVDVBAT ● VRTC ● EXLVD The detection level can be selected by register settings. The LVD module consists of six separate low voltage detectors: ● LVD0 ● LVD1 ● LVD2 ● LVD_EXLVDVBAT ● LVD_VRTC ● LVD_EXLVD LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD_EXLVDVBAT measures the voltage level input to the EXLVDVBAT pin. LVD_VRTC measures the voltage level input to the VRTC pin. LVD2 and LVD_EXLVD measure the voltage level input to the EXLVD pin. LVD registers allow your application to configure detection of VCC, EXLVDVBAT, VRTC, and EXLVD changes at various voltage thresholds.
Clocks	● Main clock oscillator (MOSC) ● Sub-clock oscillator (SOSC) ● High-speed on-chip oscillator (HOCO) ● Middle-speed on-chip oscillator (MOCO) ● Low-speed on-chip oscillator (LOCO) ● IWDT-dedicated on-chip oscillator ● PLL ● PLL_RTC ● Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External bus	● QSPI area (EQBIU): Connected to the QSPI (external device interface)

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 4 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state.
Low Power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two operation modes, normal operation mode and low-consumption clock mode. In each of the operation mode, the RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface ● Simple LIN The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3 to 5, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
IrDA Interface	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI5 based on the IrDA (Infrared Data Association) standard 1.0.
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has two channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
Serial Interface UARTA (UARTA)	The serial interface UARTA (UARTA) has two channels. The UARTA supports the following modes: ● Operation stop mode ● UART mode

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has three channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network with Flexible Data-Rate Module (CAN-FD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 16 receive buffers.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface.

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter (ADC12) is provided. Analog input channels are selectable up to 16. The temperature sensor output and an internal reference voltage are selectable for conversion.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.10 Human machine interfaces

Feature	Functional description
Segment LCD Controller (SLCDC)	The SLCDC provides the following functions: ● Internal voltage boosting method, capacitor split method, and external resistance division method are switchable ● VL1 or VL2 reference mode is selectable under internal voltage boosting method ● VCC or VL4 reference mode is selectable under capacitor split method ● Segment signal output: 48 (44) ● Common signal output: 4 (8) ● Waveform A or B selectable ● The LCD can be made to blink Note: The values in parentheses are the number of signal outputs when 8 com is used.

Table 1.11 Data processing

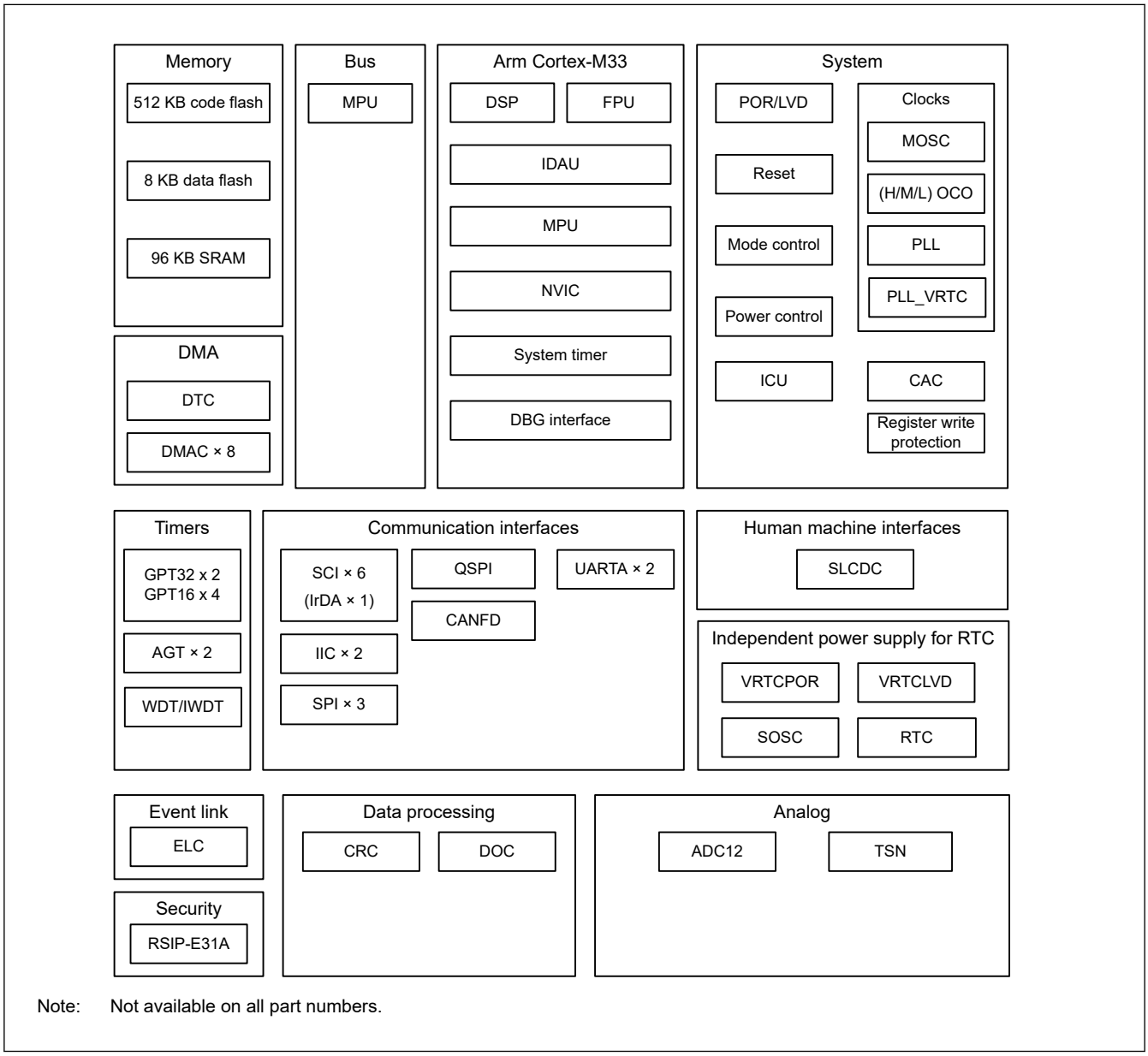
Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 32-bit data. When a selected condition applies, 32-bit data is compared and an interrupt can be generated.

Table 1.12 I/O ports

Feature	Functional description
Programmable I/O ports	● I/O ports for the 100-pin LQFP – I/O pins: 80 – Input pins: 3 – Pull-up resistors: 80 – N-ch open-drain outputs: 73 – 5-V tolerance: 4 ● I/O ports for the 64-pin LQFP – I/O pins: 46 – Input pins: 3 – Pull-up resistors: 46 – N-ch open-drain outputs: 39 – 5-V tolerance: 4

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

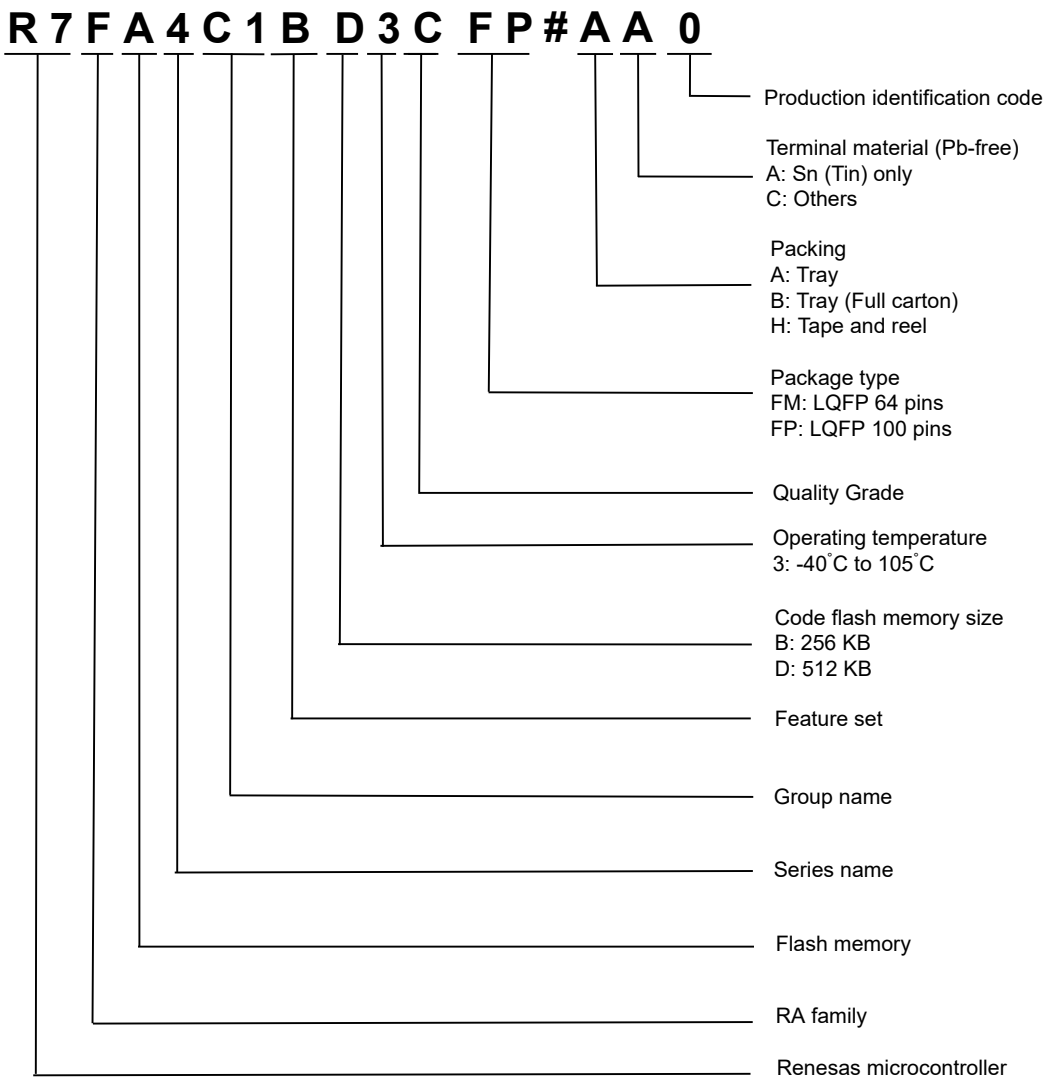


Note: Not available on all part numbers.

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.13 shows a list of products.



Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.13 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA4C1BD3CFP	PLQP0100KB-B	512 KB	8 KB	96 KB	-40 to +105 °C
R7FA4C1BD3CFM	PLQP0064KB-C				
R7FA4C1BB3CFP	PLQP0100KB-B	256 KB	8 KB	96 KB	-40 to +105 °C
R7FA4C1BB3CFM	PLQP0064KB-C				

1.4 Function Comparison

Table 1.14 Function comparison

Parts number		R7FA4C1BD3CFP R7FA4C1BB3CFP	R7FA4C1BD3CFM R7FA4C1BB3CFM
Pin count		100	64
Package		LQFP	LQFP
Code flash memory		512 KB 256 KB	
Data flash memory		8 KB	
SRAM		96 KB	
	Parity	64 KB	
	ECC	32 KB	
DMA	DTC	Yes	
	DMAC	8	
System	CPU clock	80 MHz (max.)	
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	
	CAC	Yes	
	WDT/IWDT	Yes	
Communication	SCI*1	6	
	IIC	2	
	UARTA	2	
	SPI	3	
	CANFD	1	
	QSPI	Yes	
Timers	GPT32*1	2	
	GPT16*1	4	
	AGT*1	2	
	RTC	Yes	
Analog	ADC12	Unit 0: 16	Unit 0: 12
	TSN	Yes	
HMI	SLCDC	48 seg × 4 com 44 seg × 8 com	20 seg × 4 com 16 seg × 8 com
Data processing	CRC	Yes	
	DOC	Yes	
Event control	ELC	Yes	
Security		RSIP-E31A, TrustZone, and Lifecycle management	
I/O ports	I/O pins	80	46
	Input pins	3	3
	Pull-up resistors	80	46
	N-ch open-drain outputs	73	39
	5-V tolerance	4	4

Note 1. Available pins depend on the pin count. For details, see section 1.7. Pin Lists.

1.5 Pin Functions

Table 1.15 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL/VCL0	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VRTC	Input	Independent power supply for sub-clock oscillator (XCIN, XCOUT) and RTC (RTCIC0).
Voltage detector	EXLVD	Input	Low voltage detector for external pin.
	EXLVDVBAT	Input	Low voltage detector for battery backup.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins

Table 1.15 Pin functions (2 of 3)

Function	Signal	I/O	Description
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCIC0	Input	Time capture event input pin
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	RXDXn	Input	Input pins for received data (Simple LIN Mode)
	TXDXn	Output	Output pins for transmitted data (Simple LIN Mode)
	SIOXn	I/O	Input/output pins for received or transmitted data (Simple LIN Mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
UARTA	RxDAn	Input	Serial data input signal
	TxDAn	Output	Serial data output signal
	CLKAn	Output	Serial clock output signal
SPI	RSPCKA, RSPCKB, RSPCKC	I/O	Clock input/output pin
	MOSIA, MOSIB, MOSIC	I/O	Input or output pin for data output from the master
	MISOA, MISOB, MISOC	I/O	Input or output pin for data output from the slave
	SSLA0, SSLB0, SSLC0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3, SSLC1 to SSLC3	Output	Output pins for slave selection
CANFD	CRXn	Input	Receive data
	CTXn	Output	Transmit data
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3

Table 1.15 Pin functions (3 of 3)

Function	Signal	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
SLCDC	VL1, VL2, VL3, VL4	I/O	Voltage pin for driving the LCD
	CAPH, CAPL	I/O	Capacitor connection for the LCD controller/driver
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver
	SEG0 to SEG47	Output	Segment signal output pins for the LCD controller/driver
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

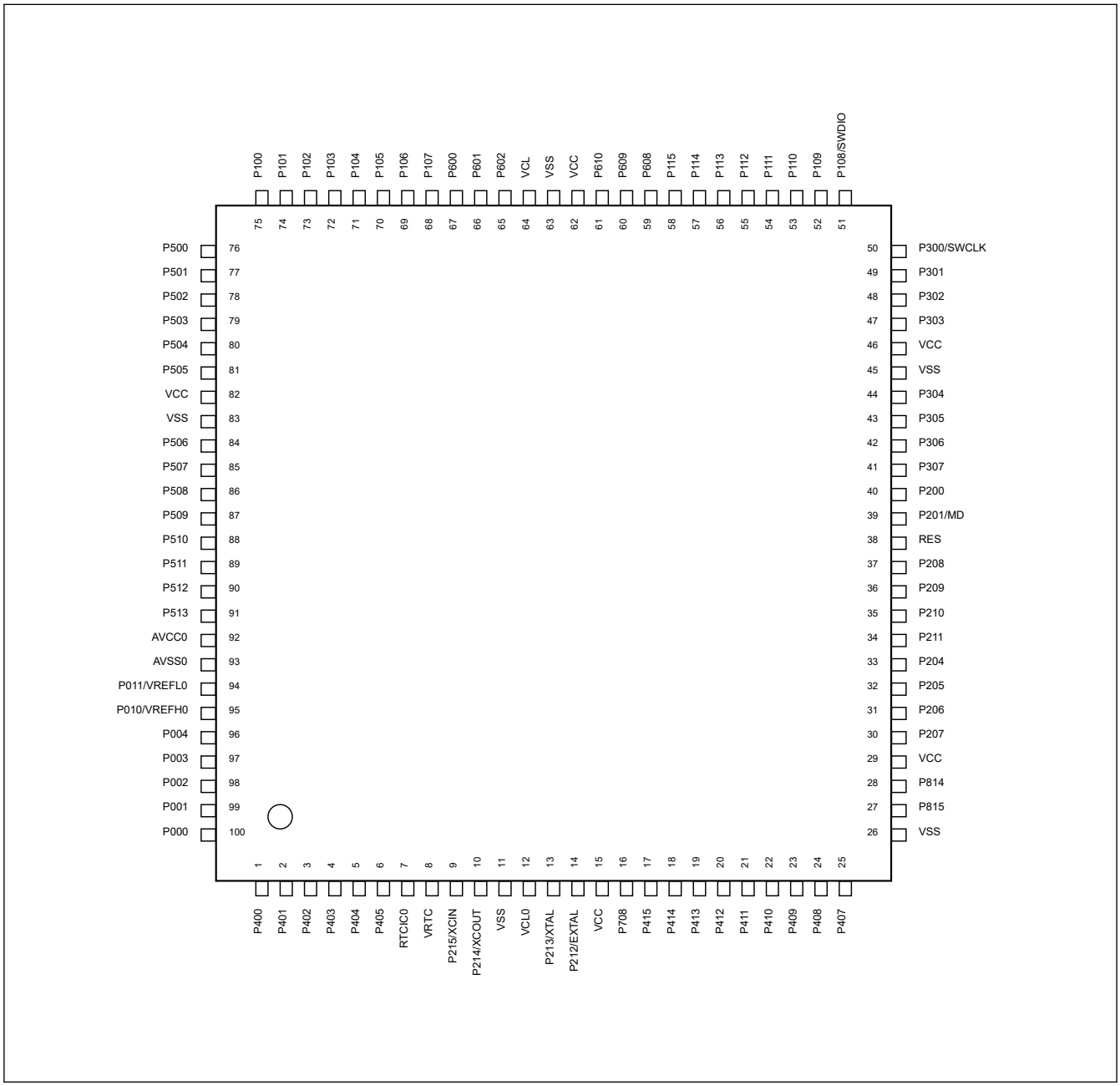


Figure 1.3 Pin assignment for LQFP 100-pin

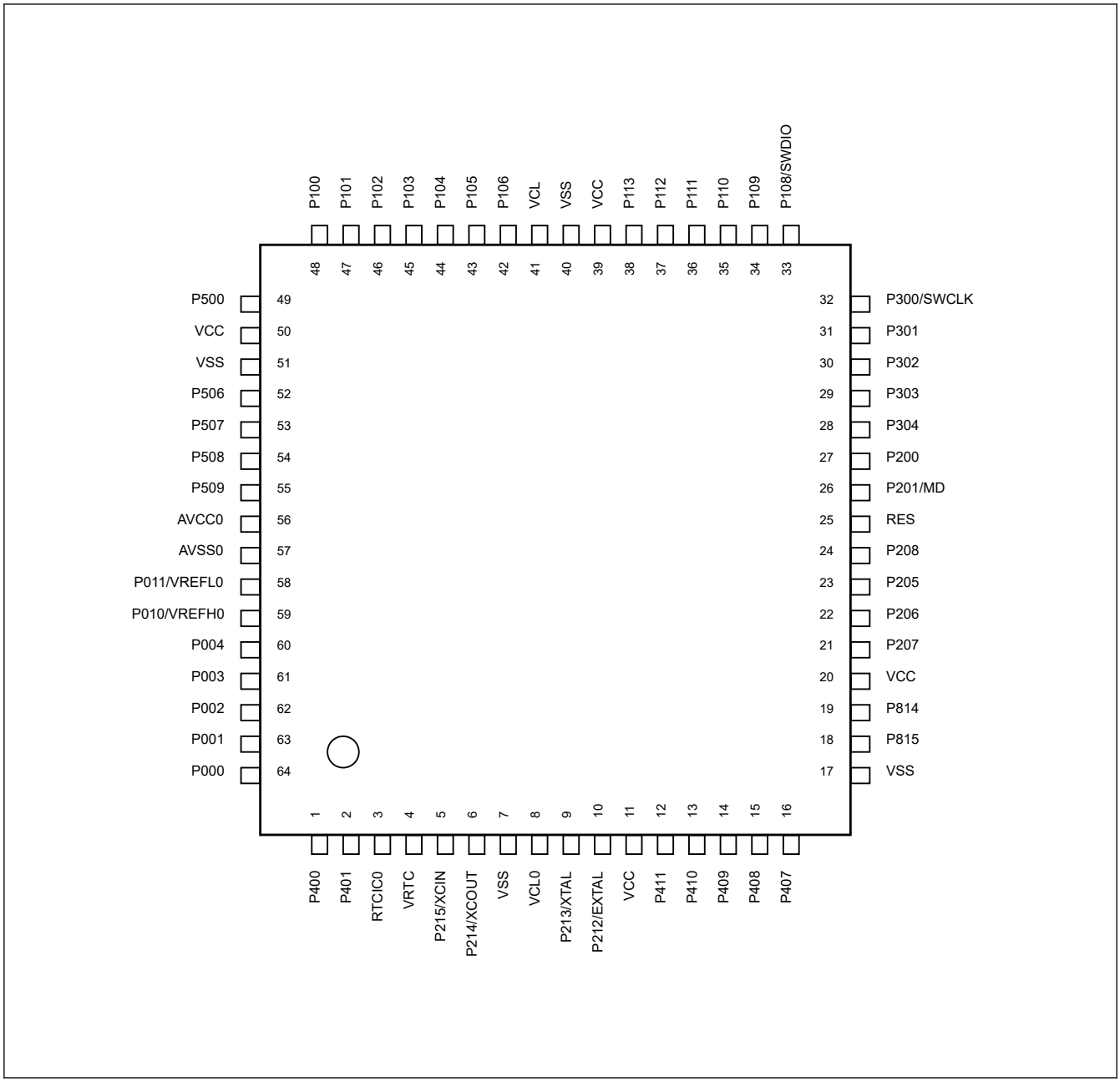


Figure 1.4 Pin assignment for LQFP 64-pin

1.7 Pin Lists

Table 1.16 Pin list (1 of 4)

LQFP100	LQFP64	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/IIC/ CANFD/SPI/QSPI/ UARTA	GPT/AGT/RTC	ADC12	SLCDC
1	1	—	P400	IRQ0	TXD1/SDA1/ MOSI1/TXDX1/ SIOX1/SCL1_A	GTETRGB/ GTIOC2A/AGTIO1	—	SEG4
2	2	—	P401	IRQ5	RXD1/SCL1/ MISO1/RXDX1/ SDA1_A/CRX0	GTETRGA/ GTIOC2B	—	SEG5
3	—	CACREF	P402	IRQ4	CTS_RTS1/SS1/ CTX0	GTETRGC/ AGTIO0/AGTIO1	—	SEG6
4	—	—	P403	IRQ14	SCK1	AGTIO0/AGTIO1	—	SEG7
5	—	—	P404	IRQ15	TXD5/SDA5/ MOSI5	GTIOC1B/ AGTIO0/AGTIO1	—	SEG23
6	—	—	P405	—	RXD5/SCL5/ MISO5	GTIOC1A	—	SEG24
7	3	RTCIC0	—	—	—	—	—	—
8	4	VRTC	—	—	—	—	—	—
9	5	XCIN	P215	—	—	—	—	—
10	6	XCOUT	P214	—	—	—	—	—
11	7	VSS	—	—	—	—	—	—
12	8	VCL0	—	—	—	—	—	—
13	9	XTAL	P213	IRQ2	TXD0/SDA0/ MOSI0	GTETRGC/ GTIOC0A	—	—
14	10	EXTAL	P212	IRQ3	RXD0/SCL0/ MISO0	GTETRGD/ GTIOC0B/ AGTEE1	—	—
15	11	VCC	—	—	—	—	—	—
16	—	CACREF	P708	IRQ11	—	—	—	SEG8
17	—	—	P415	IRQ8	—	GTIOC0A	—	SEG9
18	—	—	P414	IRQ9	SSLB3_A	GTIOC0B	—	SEG10
19	—	—	P413	—	SSLB2_A	GTOUUP	—	SEG11
20	—	—	P412	—	CTS3/SSLB1_A	GTOULO/AGTEE1	—	SEG12
21	12	—	P411	IRQ4	CTS_RTS3/SS3/ SSLB0_A	GTOVUP/AGTOA1	—	VL1
22	13	—	P410	IRQ5	SCK3/MOSIB_A	GTOVLO/AGTOB1	—	VL2
23	14	—	P409	IRQ6	TXD3/SDA3/ MOSI3/MISO_A	GTOWUP	—	VL4
24	15	—	P408	IRQ7	CTS_RTS4/SS4/ RXD3/SCL3/ MISO3/ RSPCKB_A	GTOWLO/ GTIOC2B	—	VL3
25	16	—	P407	—	CTS4	GTIOC2A/ AGTIO0/RTCOUT	ADTRG0	SEG13
26	17	VSS	—	—	—	—	—	—
27	18	—	P815	—	CRX0/TxDA1	—	—	CAPH
28	19	—	P814	—	CTX0/RxDA1	—	—	CAPL

Table 1.16 Pin list (2 of 4)

LQFP100	LQFP64	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/IIC/ CANFD/SPI/QSPI/ UARTA	GPT/AGT/RTC	ADC12	SLCDC
29	20	VCC	—	—	—	—	—	—
30	21	—	P207	—	TXD4/SDA4/ MOSI4/QSSL	GTIOC3A	—	—
31	22	—	P206	IRQ0	RXD4/SCL4/ MISO4	GTIU/GTIOC3B	—	—
32	23	CLKOUT	P205	IRQ1	SCK4	GTIV/GTIOC4A/ AGTO1	—	COM0
33	—	—	P204	—	CTS_RTS4/SS4/ SSLA0_A/ QSPCLK	GTIU	—	SEG14
34	—	—	P211	—	MOSIA_A/QIO0	GTIV	—	SEG15
35	—	—	P210	—	MISOA_A/QIO1	GTIW	—	SEG16
36	—	—	P209	—	RSPCKA_A/QIO2	GTOVUP	—	SEG17
37	24	—	P208	IRQ12	QIO3	GTOVLO	—	COM1
38	25	RES	—	—	—	—	—	—
39	26	MD	P201	—	—	—	—	—
40	27	—	P200	NMI	—	—	—	—
41	—	—	P307	—	—	GTOUUP	—	SEG18
42	—	—	P306	—	TxDA0	GTOULO	—	SEG19
43	—	—	P305	IRQ8	RxDA0	GTOWUP	—	SEG20
44	28	—	P304	IRQ9	CTS_RTS5/SS5/ CLKA0	GTOWLO/ GTIOC3A	—	COM2
45	—	VSS	—	—	—	—	—	—
46	—	VCC	—	—	—	—	—	—
47	29	—	P303	—	SCK5	GTIOC3B	—	COM3
48	30	—	P302	IRQ5	TXD5/SDA5/ MOSI5/SCL0_A/ SSLA3_B	GTOUUP/ GTIOC4A	ADTRG0	SEG21
49	31	—	P301	IRQ6	RXD5/SCL5/ MISO5/SDA0_A/ SSLA2_B	GTOULO/ GTIOC4B/AGTIO0	—	SEG22
50	32	SWCLK	P300	—	CTS5/SSLA1_B	GTOUUP/ GTIOC0A	—	SEG23
51	33	SWDIO	P108	—	CTS_RTS9/SS9/ SSLA0_B	GTOULO/ GTIOC0B	—	SEG24
52	34	CLKOUT	P109	—	TXD9/SDA9/ MOSI9/MOSIA_B	GTOVUP/ GTIOC1A	—	COM4/ SEG0
53	35	—	P110	IRQ3	RXD9/SCL9/ MISO9/MISOA_B	GTOVLO/ GTIOC1B	—	COM5/ SEG1
54	36	—	P111	IRQ4	SCK9/RSPCKA_B	—	—	COM6/ SEG2
55	37	—	P112	—	CTS_RTS9/SS9/ SSLA0_B/QSSL	—	—	COM7/ SEG3
56	38	—	P113	IRQ10	—	AGTIO1	—	SEG25
57	—	—	P114	—	CTS9	—	—	SEG26

Table 1.16 Pin list (3 of 4)

LQFP100	LQFP64	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/IIC/ CANFD/SPI/QSPI/ UARTA	GPT/AGT/RTC	ADC12	SLCDC
58	—	—	P115	—	TXD1/SDA1/ MOSI1/TXDX1/ SIOX1	GTIOC4A	—	SEG27
59	—	—	P608	—	RXD1/SCL1/ MISO1/RXDX1	GTIOC4B	—	SEG28
60	—	—	P609	—	SCK1	GTIOC5A	—	SEG29
61	—	—	P610	—	CTS_RTS1/SS1	GTIOC5B	—	SEG30
62	39	VCC	—	—	—	—	—	—
63	40	VSS	—	—	—	—	—	—
64	41	VCL	—	—	—	—	—	—
65	—	—	P602	—	—	—	—	SEG31
66	—	—	P601	—	—	GTIOC2A	—	SEG32
67	—	CACREF/ CLKOUT	P600	—	—	GTIOC2B	—	SEG33
68	—	—	P107	—	—	AGTOA0	—	SEG34
69	42	—	P106	—	CTS3/SSLC3_A	GTETRGD/ AGTOB0	—	SEG35
70	43	—	P105	IRQ0	CTS_RTS3/SS3/ SSLC2_A	GTETRGA/ GTIOC1A	—	SEG36
71	44	—	P104	IRQ1	SCK3/SSLC1_A/ QSPCLK	GTETRGB/ GTIOC1B	—	SEG37
72	45	—	P103	—	CTS_RTS0/SS0/ TXD3/SDA3/ MOSI3/CRX0/ SSLC0_A/QIO2	GTOWUP	—	SEG38
73	46	—	P102	—	SCK0/RXD3/ SCL3/MISO3/ CTX0/RSPCKC_A/ QIO3	GTOWLO/AGTO0	ADTRG0	SEG39
74	47	—	P101	IRQ1	TXD0/SDA0/ MOSI0/SCL0_B/ MOSIC_A/QIO0	GTETRGB/ GTIOC5A/ AGTEE0	—	SEG40
75	48	—	P100	IRQ2	RXD0/SCL0/ MISO0/SDA0_B/ MISOC_A/QIO1	GTETRGA/ GTIOC5B/AGTIO0	—	SEG41
76	49	CACREF	P500	—	CTS0/QSPCLK	GTIU/AGTOA0	AN021	SEG42
77	—	—	P501	IRQ11	QSSL	GTIV/AGTOB0	—	SEG43
78	—	—	P502	IRQ12	QIO0	GTIW	—	SEG44
79	—	—	P503	—	QIO1	GTETRGC	—	SEG45
80	—	—	P504	—	QIO2	GTETRGD	—	SEG46
81	—	—	P505	IRQ14	QIO3	—	—	SEG47
82	50	VCC	—	—	—	—	—	—
83	51	VSS	—	—	—	—	—	—
84	52	—	P506	IRQ13	TXD5/SDA5/ MOSI5/MOSIC_B	GTIOC4A	AN020	—

Table 1.16 Pin list (4 of 4)

LQFP100	LQFP64	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/IIC/ CANFD/SPI/QSPI/ UARTA	GPT/AGT/RTC	ADC12	SLCDC
85	53	—	P507	—	RXD5/SCL5/ MISO5/MISOC_B/ CLKA0	GTIOC4B	AN019	—
86	54	EXLVDVBAT	P508	—	CTS_RTS5/SS5/ RSPCKC_B/ TxDA0	—	AN018	—
87	55	EXLVD	P509	—	SCK5/SSLC0_B/ RxDA0	—	AN017	—
88	—	—	P510	—	TXD9/SDA9/ MOSI9/SSLC1_B	—	AN025	—
89	—	—	P511	—	RXD9/SCL9/ MISO9/SSLC2_B/ CLKA1	—	AN024	—
90	—	—	P512	—	CTS_RTS9/SS9/ SSLC3_B/TxDA1	—	AN023	—
91	—	—	P513	IRQ15	SCK9/RxDA1	—	AN022	—
92	56	AVCC0	—	—	—	—	—	—
93	57	AVSS0	—	—	—	—	—	—
94	58	VREFL0	P011	IRQ11	—	—	AN004	—
95	59	VREFH0	P010	IRQ10	—	—	AN003	—
96	60	—	P004	IRQ9	—	—	AN002	—
97	61	—	P003	—	—	—	AN001	—
98	62	—	P002	IRQ8	—	—	AN000	—
99	63	—	P001	IRQ7	—	—	AN006	—
100	64	—	P000	IRQ6	—	—	AN005	—

2. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC^{*1} = AVCC0 = 1.6 to 3.6 V, VRTC = 1.6 to 3.6 V, VREFH0 = 1.6 V to AVCC0

VSS = AVSS0 = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.

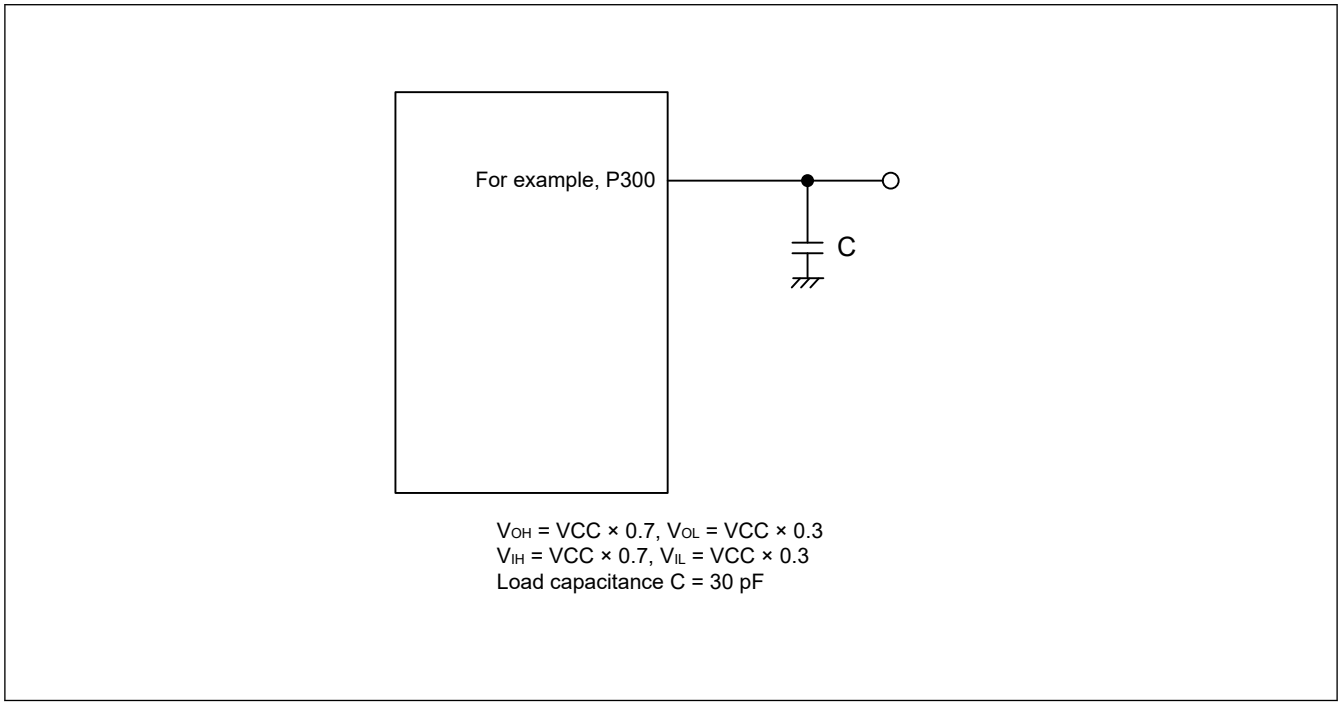


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +4.0	V
RTC power supply voltage		VRTC	-0.5 to +4.0	V
Input voltage	5V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P000 to P004, P010, P011	V_{in}	-0.3 to AVCC0 + 0.3	V
	P214, P215, RTCIC0	V_{in}	-0.3 to VRTC + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +4.0	V
Analog power supply voltage		AVCC0*2	-0.5 to +4.0	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter		Symbol	Value	Unit
Analog input voltage	When AN000 to AN006 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN017 to AN025 are used		-0.3 to VCC + 0.3	V
Operating temperature*3		T_{opr}	-40 to +105	°C
Storage temperature		T_{stg}	-55 to +125	°C

Note 1. Ports P301, P302, P400, and P401 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. Connect AVCC0 to VCC
Note 3. See section 2.2.1. Tj/Ta Definition.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **VRTC and VSS: about 0.1 µF**
- **AVCC0 and AVSS0: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin and VCL0 pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC*1 *2		1.6	—	3.6	V
	VSS		—	0	—	V
RTC power supply voltage	VRTC		1.6	—	3.6	V
Analog power supply voltages	AVCC0*1 *2		1.6	—	3.6	V
	AVSS0		—	0	—	V
	VREFH0	When used as ADC12 Reference	1.6	—	AVCC0	V
	VREFL0		—	0	—	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 = VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pins.
When powering off the VCC and AVCC0 pins, power them off at the same time or the AVCC0 pin first and then the VCC pins.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +105 °C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	125*1	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.
Note 1. The upper limit of operating temperature is 125 °C, depending on the product. If the part number shows the operation temperature at 105 °C, then the maximum value of Tj is 125 °C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC0 = 1.6 to 3.6 V, VRTC = 1.6 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (SDA0_A, SCL0_A, SDA1_A, SCL1_A) (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
		ΔV_T	VCC × 0.10	—	—		VCC = 2.7 V to 3.6 V
			VCC × 0.05	—	—		VCC = 1.6 V to2.7 V
	RES, NMI Other peripheral input pins excluding IIC (SDA0_A, SCL0_A, SDA1_A, SCL1_A)	V_{IH}	VCC × 0.8	—	—		—
		V_{IL}	—	—	VCC × 0.2		
		ΔV_T	VCC × 0.10	—	—		VCC = 2.7 V to 3.6 V
			VCC × 0.05	—	—		VCC = 1.6 V to 2.7 V
	RTCIC0	V_{IH}	VRTC × 0.8	—	—		—
		V_{IL}	—	—	VRTC × 0.2		—
		ΔV_T	—	0.71	—		—
Input voltage except for Schmitt trigger input pin	IIC (SMBus)*2	V_{IH}	2.0	—	—		VCC = 1.8 to 3.6 V
		V_{IL}	—	—	0.5		VCC = 1.8 to 3.6 V
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	—	5.8		—
		V_{IL}	—	—	VCC × 0.2		
	P000 to P004, P010, P011	V_{IH}	AVCC0 × 0.8	—	—		
		V_{IL}	—	—	AVCC0 × 0.2		
	P214, P215	V_{IH}	VRTC × 0.8	—	—		
		V_{IL}	—	—	VRTC × 0.2		
	Input port pins except for P000 to P004, P010, P011	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, SDA1_A, SCL1_A (total 4 pins)
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, SDA1_A, SCL1_A (total 6 pins)
Note 3. P400, P401, P301, P302 (total 4 pins)

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 4)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (average value per pin)	I_{OH}	—	—	−4.0	mA	
	I_{OL}	—	—	8.0	mA	
Permissible output current (max value per pin)	I_{OH}	—	—	−4.0	mA	
	I_{OL}	—	—	8.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 4)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	All products	Total of ports P000 to P004, P010, P011	ΣI_{OH} (max)	—	—	−30	mA	AVCC0 = 2.7 to 3.6 V
				—	—	−8	mA	AVCC0 = 1.8 to 2.7 V
				—	—	−4	mA	AVCC0 = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	AVCC0 = 2.7 to 3.6 V
				—	—	4	mA	AVCC0 = 1.8 to 2.7 V
				—	—	2	mA	AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	ΣI_{OH}	—	—	−8.0	mA	VCC = 2.7 to 3.6 V
				—	—	−2	mA	VCC = 1.8 to 2.7 V
				—	—	−1	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL}	—	—	16.0	mA	VCC = 2.7 to 3.6 V
				—	—	1.2	mA	VCC = 1.8 to 2.7 V
				—	—	0.6	mA	VCC = 1.6 to 1.8 V
	100 pin products	Total of ports P400 to P406, P408 to P415, P708	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (3 of 4)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	100 pin products	Total of ports P204 to P211, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P108 to P112, P201, P300 to P307	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P100 to P107, P113 to P115, P600 to P602, P608 to P610	ΣI_{OH}	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL}	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P500 to P513	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−100	mA	
			ΣI_{OL} (max)	—	—	100	mA	

Table 2.5 I/O I_{OH}, I_{OL} (4 of 4)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	64 pin LQFP	Total of ports P400, P401, P407 to P411	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P201, P205 to P208, P303, P304, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P105, P106, P108 to P113, P300 to P302	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P100 to P104, P500, P506 to P509	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−60	mA	
			ΣI_{OL} (max)	—	—	100	mA	

Note 1. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = AVCC0 = 2.7 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	P400, P401	V_{OH}	VCC − 0.27	—	—	V	I_{OH} = −3.0 mA
			VCC − 0.8	—	—		I_{OH} = −4.0 mA
	Ports P000 to P004, P010, P011	V_{OH}	AVCC0 − 0.8	—	—		I_{OH} = −4.0 mA
	Output pins except for P000 to P004 and P010, P011, P400, P401*1	V_{OH}	VCC − 0.8	—	—		I_{OH} = −4.0 mA
	P400, P401	V_{OL}	—	—	0.27		I_{OL} = 3.0 mA
			—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
			—	—	0.8		I_{OL} = 8.0 mA
	P301, P302	V_{OL}	—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
			—	—	0.8		I_{OL} = 8.0 mA
	Ports P000 to P004, P010, P011	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P004 and P010, P011, P301, P302, P400, P401*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, P215, and RTCIC0, which are input ports.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010, P011	V_{OH}	AVCC0 − 0.5	—	—	V	I_{OH} = −1.0 mA
	Output pins except for P000 to P004 and P010, P011*1	V_{OH}	VCC − 0.5	—	—		I_{OH} = −1.0 mA
	P301, P302, P400, P401	V_{OL}	—	0.4	—		I_{OL} = 3.0 mA
			—	0.6	—		I_{OL} = 6.0 mA
			—	—	0.4		I_{OL} = 0.6 mA
	Ports P000 to P004, P010, P011	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA
	Output pins except for P000 to P004 and P010, P011, P301, P302, P400, P401*1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA

Note 1. Except for Ports P200, P214, P215, and RTCIC0, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC0 = 1.6 to 1.8 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010, P011	V_{OH}	AVCC0 − 0.5	—	—	V	I_{OH} = −0.5 mA
	Output pins except for P000 to P004 and P010, P011*1	V_{OH}	VCC − 0.5	—	—		I_{OH} = −0.5 mA
	Ports P000 to P004, P010, P011	V_{OL}	—	—	0.4		I_{OL} = 0.3 mA
	Output pins except for P000 to P004 and P010, P011*1	V_{OL}	—	—	0.4		I_{OL} = 0.3 mA

Note 1. Except for Ports P200, P214, P215, and RTCIC0, which are input ports.

Table 2.9 I/O other characteristics

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	P214, P215, RTCIC0		—	—	1.0	µA	V_{in} = 0 V V_{in} = VRTC
Three-state leakage current (off state)	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, P214, P215, RTCIC0, and 5V-tolerant ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215, RTCIC0)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V, f = 1 MHz T_a = 25 °C
	Other input pins		—	—	15		

Note 1. P301, P302, P400, and P401 (total 4 pins)

2.2.5 Operating and Standby Current

Table 2.10 High-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test Conditions
Maximum*1 *2		ICC*3	—	77.0	mA	ICLK = 80 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 40 MHz PCLKD = 80 MHz FCLK = 40 MHz
CoreMark®*4 *5			20.5	—	mA	
			256.3	—	uA/MHz	
Normal mode	All peripheral clocks enabled, and cache disabled. While (1) code is executing from flash*5		29.1	—	mA	
			364.1	—	uA/MHz	
	All peripheral clocks disabled, and cache disabled. While (1) code is executing from flash*4 *5		13.5	—	mA	
			168.3	—	uA/MHz	
Sleep mode	All peripheral clocks enabled, and cache disabled*5		21.2	—	mA	
	All peripheral clocks disabled, and cache disabled*4 *5		5.65	—	mA	
Increase during BGO operation*6			2.67	—	mA	

Note: Supply current is the total current flowing into VCC and VRTC. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note 1. Measured with clocks supplied to the peripheral functions.
Note 2. PLL output frequency = 80 MHz. The clock source is MOSC.

Note 3. ICC depends on f (ICLK) as follows (reference data).
ICC Max. = 0.83 × f + 10.44 (max. operation)
ICC Typ. = 0.16 × f + 0.82 (normal operation, all peripheral clocks disabled and cache disabled)
ICC Typ. = 0.22 × f + 3.64 (Sleep mode, all peripheral clocks enabled and cache disabled)
Note 4. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.25 MHz).
Note 5. PLL is stopped, and HOCO output frequency = 80 MHz
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Table 2.11 Middle-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
Normal mode	All peripheral clocks enabled, and cache disabled. While (1) code is executing from flash	ICC*1	4.49	—	mA	ICLK = 8 MHz PCLKA = 8 MHz PCLKB = 8 MHz PCLKC = 8 MHz PCLKD = 8 MHz FCLK = 8 MHz
	All peripheral clocks disabled, and cache disabled. While (1) code is executing from flash*2		1.79	—		
Sleep mode	All peripheral clocks enabled, and cache disabled		3.50	—		
	All peripheral clocks disabled, and cache disabled*2		0.81	—		
Increase during BGO operation*3			2.10	—		

Note: Supply current is the total current flowing into VCC and VRTC. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note: The clock source is MOCO.
Note 1. ICC depends on f (ICLK) as follows (reference data).
ICC Typ. = 0.45 × f + 0.94 (normal operation, all peripheral clocks enabled and cache disabled)
Note 2. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (125 kHz).
Note 3. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Table 2.12 Low-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
Normal mode	All peripheral clocks enabled, and cache disabled. While (1) code is executing from flash	ICC*1	1.20	—	mA	ICLK = 1 MHz PCLKA = 1 MHz PCLKB = 1 MHz PCLKC = 1 MHz PCLKD = 1 MHz FCLK = 1 MHz
	All peripheral clocks disabled, and cache disabled. While (1) code is executing from flash*2		0.38	—		
Sleep mode	All peripheral clocks enabled, and cache disabled		1.07	—		
	All peripheral clocks disabled, and cache disabled*2		0.24	—		

Note: Supply current is the total current flowing into VCC and VRTC. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note: The clock source is MOSC.
Note 1. ICC depends on f (ICLK) as follows (reference data).
ICC Typ. = 0.47 × f + 0.43 (normal operation, all peripheral clocks disabled and cache disabled)
Note 2. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.625 kHz).

Table 2.13 Subosc-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
Normal mode	All peripheral clocks enabled, and cache disabled. While (1) code is executing from flash	ICC	18.44	—	µA	ICLK = 32.768 kHz PCLKA = 32.768 kHz PCLKB = 32.768 kHz PCLKC = 32.768 kHz PCLKD = 32.768 kHz FCLK = 32.768 kHz
	All peripheral clocks disabled, and cache disabled. While (1) code is executing from flash*1		9.86	—		
Sleep mode	All peripheral clocks enabled, and cache disabled		13.71	—		
	All peripheral clocks disabled, and cache disabled*1		5.17	—		

Note: Supply current is the total current flowing into VCC and VRTC. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note: The clock source is LOCO.
Note 1. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz).

Table 2.14 Software Standby mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
All SRAMs (0x2000_00 00 to 0x2001_7FFF) are on	Ta = 25 °C	ICC	1.79	—	µA	—
	Ta = 55 °C		5.82	—		
	Ta = 85 °C		22.1	—		
	Ta = 105 °C		50.7	—		
Only 16 KB SRAM (0x2000_0000 to 0x2000_3FFF) is on	Ta = 25 °C		1.73	—		

Note: Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state. Supply current is the total current flowing into VCC and VRTC.
Note: The IWDT and LVD are not operating.
Note: If you want to operate RTC, add the value of Table 2.15.

Table 2.15 Increase current by RTC operation

Parameter		Symbol	Typ	Max	Unit	Test conditions
SOSC*1 (normal mode)	RTC (normal operation mode)	ICC	1.25	—	µA	SOMCR.SODRV[1:0] = 00b RCR4.ROPSEL = 0
	RTC (low-consumption clock mode)		1.08	—		SOMCR.SODRV[1:0] = 00b RCR4.ROPSEL = 1
SOSC*1 (Low power mode 3)	RTC (normal operation mode)		0.55	—		SOMCR.SODRV[1:0] = 11b RCR4.ROPSEL = 0
	RTC (low-consumption clock mode)		0.38	—		SOMCR.SODRV[1:0] = 11b RCR4.ROPSEL = 1

Note: Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state. The supply current is total current flowing into VRTC.
Note 1. Includes the sub-clock oscillation circuit current.

Table 2.16 Analog current

Parameter			Symbol	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed A/D conversion mode)		I_{AVCC0}	0.50	1	mA	—
	During 12-bit A/D conversion (at low-power A/D conversion mode)			0.27	0.8	mA	—
	Waiting for 12-bit A/D conversion*1			—	4	µA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion		I_{REFH0}	—	150	µA	—
	Waiting for 12-bit A/D conversion			—	0.30	µA	—
Temperature Sensor (TSN) operating current			I_{TSN}	98	—	µA	—
LCD operating current	External resistance division method*2		I_{LCD}*3	0.04	—	µA	$f_{LCD} = f_{SUB}$ (32.768 kHz) LCD clock = 128 Hz (LCDC0 = 0x07) 1/3 bias four-time-slices VCC = 3.0 V VL4 = 3.0 V
	Internal voltage boosting method	VL1 reference VL1AMP enabled (VLCD = 0x04)		0.68	—	µA	
		VL2 reference VL2AMP enabled (VLCD = 0x84)		0.62	—	µA	
	Capacitor split method	VCC reference		0.12	—	µA	
		VL4 reference VL4AMP enabled		0.63	—	µA	

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.

Note 2. Not including the current flowing into the external division resistor when using the external resistance division method.
Note 3. Setting 20 pins as the segment function and blinking all.

Figure 2.2 shows the temperature dependency in Software Standby mode.

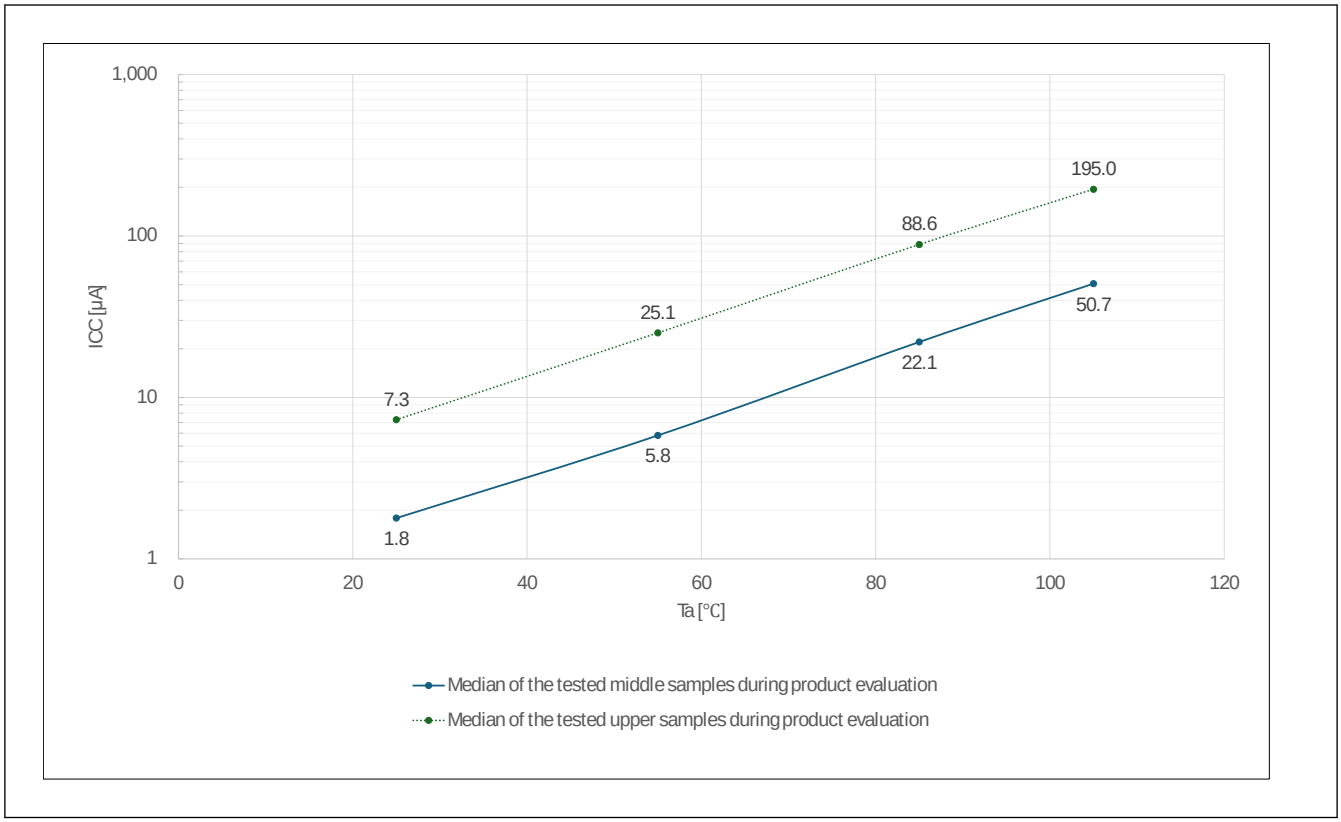


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

Figure 2.3 shows the frequency dependency in High-speed mode (reference data).

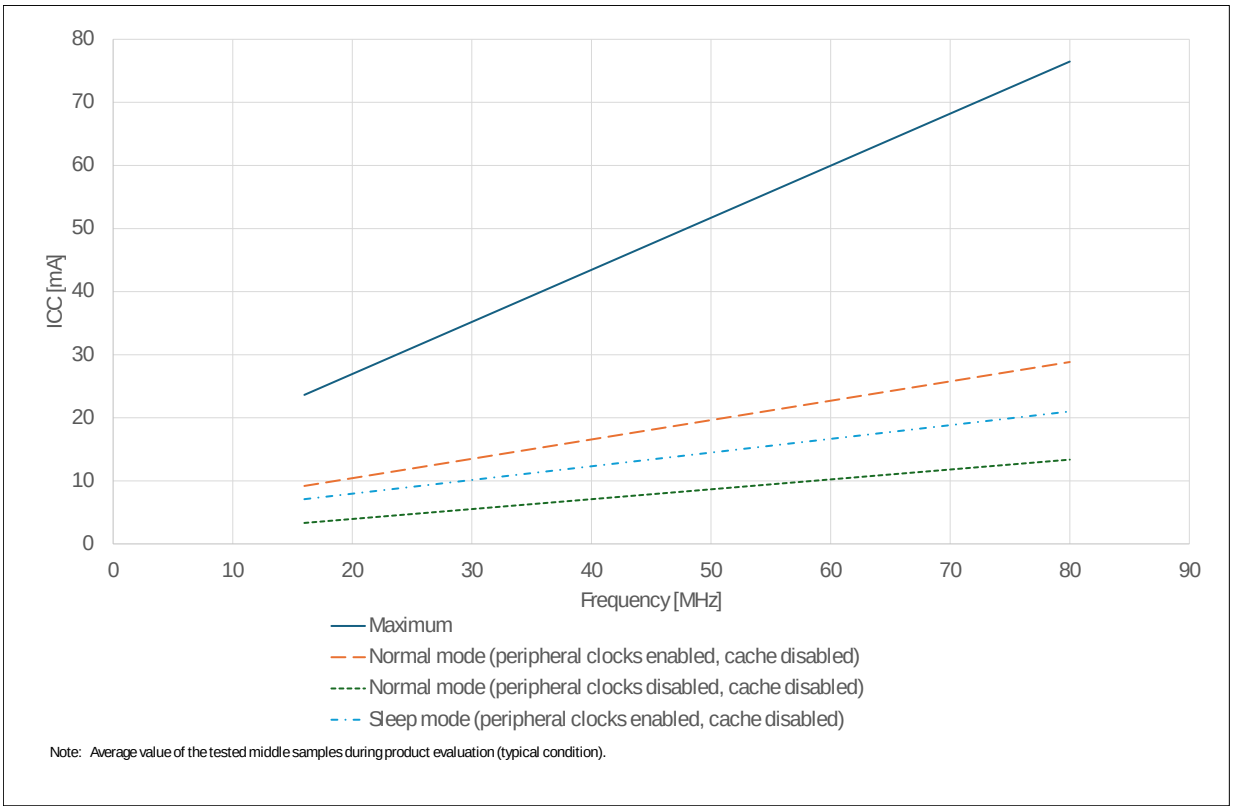


Figure 2.3 Frequency dependency in High-speed mode (reference data)

Figure 2.4 shows the frequency dependency in Middle-speed mode.

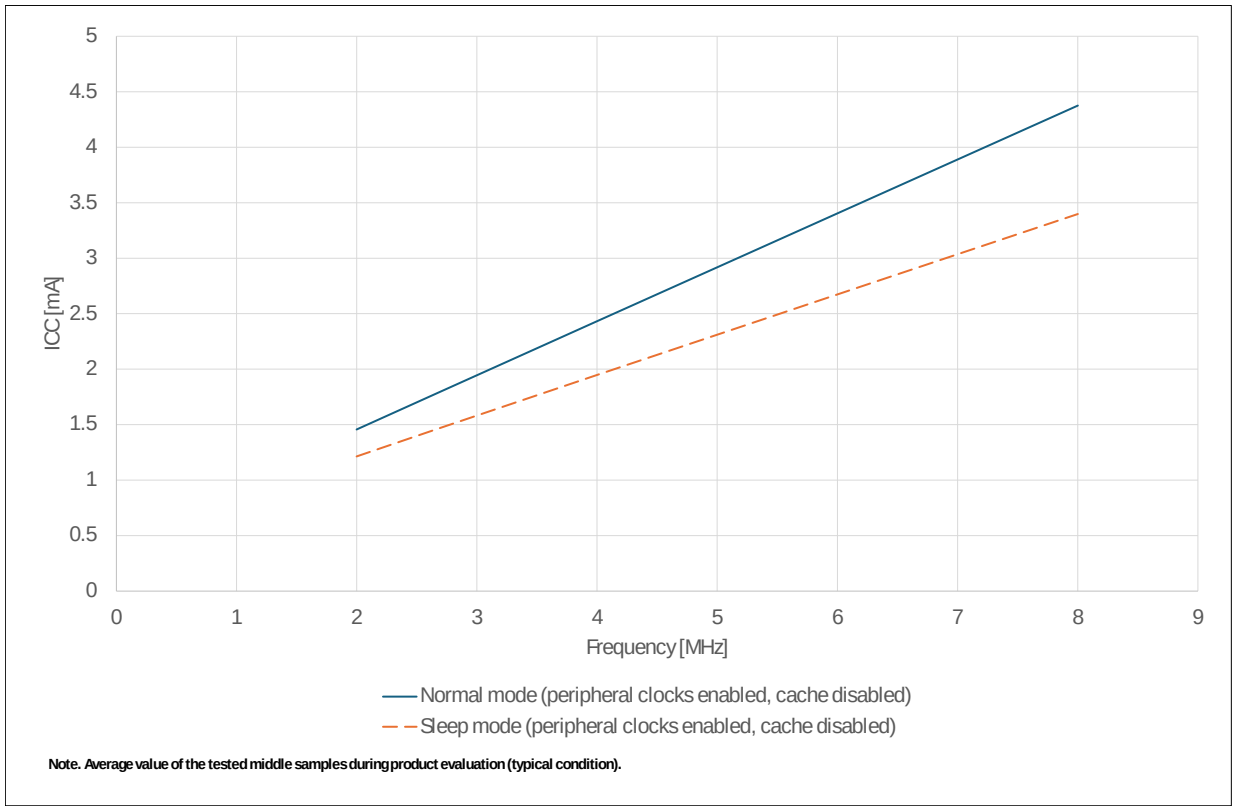


Figure 2.4 Frequency dependency in Middle-speed mode (reference data)

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.17 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI/SWD boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.18 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 3.6 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.5 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.5 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.5 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

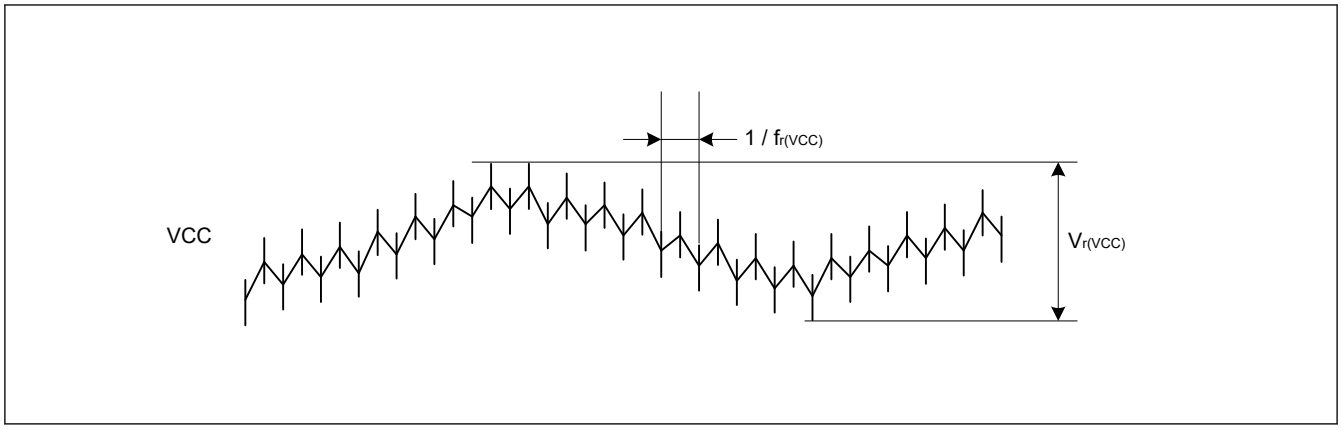


Figure 2.5 Ripple waveform

2.2.7 VRTC Rise and Fall Gradient

Table 2.19 VRTC rise and fall gradient characteristics

Conditions: VRTC = 0 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VRTC rising gradient	SrVRTC	0.02	—	20	ms/V	—

2.2.8 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption

  Tj : Junction temperature (°C)

  Ta : Ambient temperature (°C)

  Tt : Top center case temperature (°C)

  θja : Thermal resistance of “Junction”-to-“Ambient” (°C/W)

  Ψjt : Thermal resistance of “Junction”-to-“Top center case” (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (IOL × VOL) / Voltage + Σ (|IOH| × |VCC – VOH|) / Voltage
- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

  Cin: Input capacitance

  Cload: Output capacitance

Regarding θja and Ψjt, see Table 2.20.

Table 2.20 Thermal resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal resistance	64-pin LQFP	θja	43.8	°C/W	JESD 51-2 and 51-7 compliant
	100-pin LQFP		44.3		
	64-pin LQFP	Ψjt	0.70	°C/W	JESD 51-2 and 51-7 compliant
	100-pin LQFP		0.70		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, see the JEDEC standards.

2.2.8.1 Calculation Guide of ICCmax

Table 2.21 shows the power consumption of each unit and Table 2.22 shows the outline of operation for each unit.

Table 2.21 Power consumption of each unit

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [µA/ MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 25 °C*3	—	—	2.54
			Ta = 55 °C*3	—	—	2.59
			Ta = 75 °C*3	—	—	2.68
			Ta = 85 °C*3	—	—	2.76
			Ta = 95 °C*3	—	—	2.88
			Ta = 105 °C*3	—	—	3.07
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	80	271	21.7
	Peripheral Unit	Timer	GPT16 (4ch)*4	80	18.7	1.49
			GPT32 (2ch)*4	80	10.8	0.86
			POEG (4 Groups)*4	40	4.82	0.19
			AGT (2ch)*4	40	8.03	0.32
			RTC*6	40	4.54	0.18
			WDT	40	2.36	0.09
			IWDT	40	0.78	0.03
		Communication interfaces	SCI (6ch)*4	80	47.8	3.82
			IrDA*5	80	7.88	0.63
			IIC (2ch)*4	40	10.2	0.41
			CANFD	40	19.0	0.76
			SPI (3ch)*4	80	27.6	2.21
			QSPI	80	5.99	0.48
			UARTA (2ch)*4	40	15.3	0.61
		Analog	ADC12	80	6.26	0.50
		Human machine interfaces	SLCDC	40	7.96	0.32
		Event link	ELC	40	2.01	0.08
		Security	RSIP-E31A	40	488	19.5
		Data processing	CRC	80	5.64	0.45
			DOC	80	0.79	0.06
		System	CAC	40	2.88	0.12
		DMA	DMAC (per 1ch)	80	23.6	1.89
			DTC	80	22.3	1.78

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current. It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel, group or unit, divide Current [mA] by the number of channels, groups or units.
Note 5. Includes current for 1 channel of SCI.
Note 6. RTC operationg current flow into VRTC power supply.

Table 2.22 Outline of operation for each unit

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.
RTC	RTC is operating with SOSC.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
SCI	SCI is transmitting data in clock synchronous mode.
IrDA	SCI is transmitting data in clock asynchronous mode. IrDA is only clear module stop bit.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 32-bit width data.
QSPI	QSPI is issuing Fast Read Quad I/O Instruction.
UARTA	UARTA is transmitting 8-bit width data.
ADC12	Resolution is set to 12-bit accuracy. Data registers is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
SLCDC	SLCDC is operating in A wave, 1/2 bias method, 2-time slice and External resistance division method.
ELC	Only clear module stop bit.
RSPI-E31A	RSIP is doing self-test operation.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data comparison mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.3 AC Characteristics

2.3.1 Frequency

Table 2.23 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1 *2	1.8 to 3.6 V	f	0.03277	—	80*5	MHz
		1.6 to 1.8 V		0.03277	—	4	
	Peripheral module clock (PCLKA)	1.8 to 3.6 V		—	—	80*5	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKB)	1.8 to 3.6 V		—	—	40	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKC)*3	1.8 to 3.6 V		—	—	48	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)	1.8 to 3.6 V		—	—	80*5	
		1.6 to 1.8 V		—	—	4	
	Flash IF clock (FCLK)	1.8 to 3.6 V		—	—	48	
		1.6 to 1.8 V		—	—	4	

Note: Set LDOCR.CHG0 = 0 when ICLK < 8MHz, and LDOCR.CHG0 = 1 when 8MHz ≤ ICLK.
Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.27.
Note 5. This is the condition when Tj = 105 °C. Specifications at Tj = 125 °C are 79.2 MHz.

Table 2.24 Operation frequency in middle-speed mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1 *2	1.8 to 3.6 V	f	0.03277	—	8	MHz
		1.6 to 1.8 V		0.03277	—	4	
	Peripheral module clock (PCLKA)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKB)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKC)*3	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Flash IF clock (FCLK)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.27.

Table 2.25 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1 *2	1.6 to 3.6 V	f	0.03277	—	1	MHz
	Peripheral module clock (PCLKA)	1.6 to 3.6 V		—	—	1	
	Peripheral module clock (PCLKB)	1.6 to 3.6 V		—	—	1	
	Peripheral module clock (PCLKC)*3	1.6 to 3.6 V		—	—	1	
	Peripheral module clock (PCLKD)	1.6 to 3.6 V		—	—	1	
	Flash IF clock (FCLK)	1.6 to 3.6 V		—	—	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.27.

Table 2.26 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 3.6 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKA)	1.6 to 3.6 V		—	—	37.6832	
	Peripheral module clock (PCLKB)	1.6 to 3.6 V		—	—	37.6832	
	Peripheral module clock (PCLKC)	1.6 to 3.6 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2	1.6 to 3.6 V		—	—	37.6832	
	Flash IF clock (FCLK)	1.6 to 3.6 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.27 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.6
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 3.6
		—	—	4		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 3.6
		1	—	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f_{LOCO}	27.853	32.77	37.683	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	μs	Figure 2.7
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—

Table 2.27 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	µs	—
HOCO clock oscillation frequency	f_{HOCO24}	23.76	24	24.24	MHz	—
	f_{HOCO32}	31.68	32	32.32		—
	f_{HOCO40}	39.6	40	40.4		—
	f_{HOCO48}	47.52	48	48.48		—
	f_{HOCO64}	63.36	64	64.64		—
	f_{HOCO80}	79.2	80	80.8		—
HOCO clock oscillation stabilization time*3	t_{HOCO}	—	1.9	—	µs	Figure 2.8
PLL clock frequency	f_{PLL}	24	—	80	MHz	—
PLL clock oscillation stabilization time	t_{PLL}	—	—	70	µs	Figure 2.9
PLL_RTC clock frequency	f_{PLLR}	—	26	—	MHz	—
PLL_RTC clock oscillation stabilization time	t_{PLLR}	—	—	10	ms	Figure 2.10
Sub-clock oscillator oscillation frequency*4	f_{SUB}	—	32.77	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 2.11

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.
Note 4. The power supply of sub-clock oscillator is VRTC.

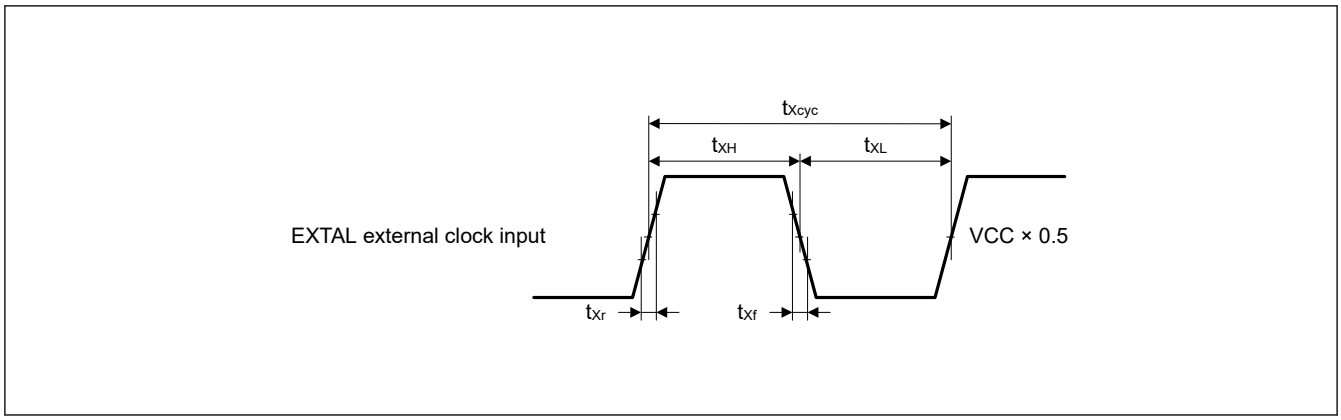


Figure 2.6 EXTAL external clock input timing

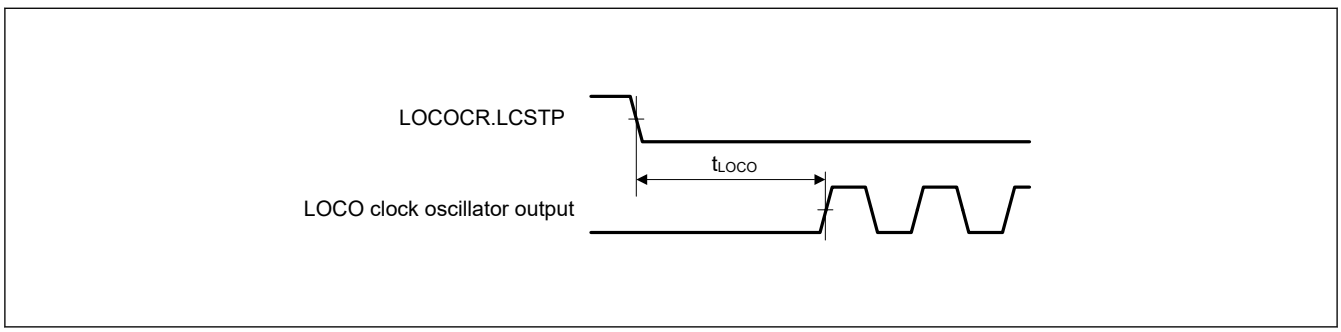


Figure 2.7 LOCO clock oscillation start timing

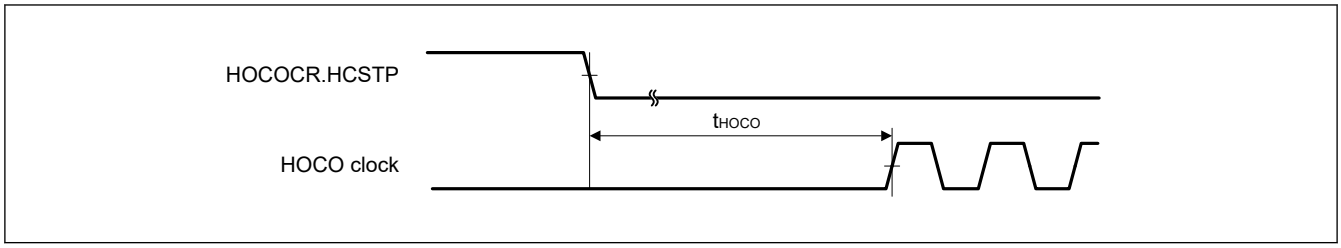


Figure 2.8 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

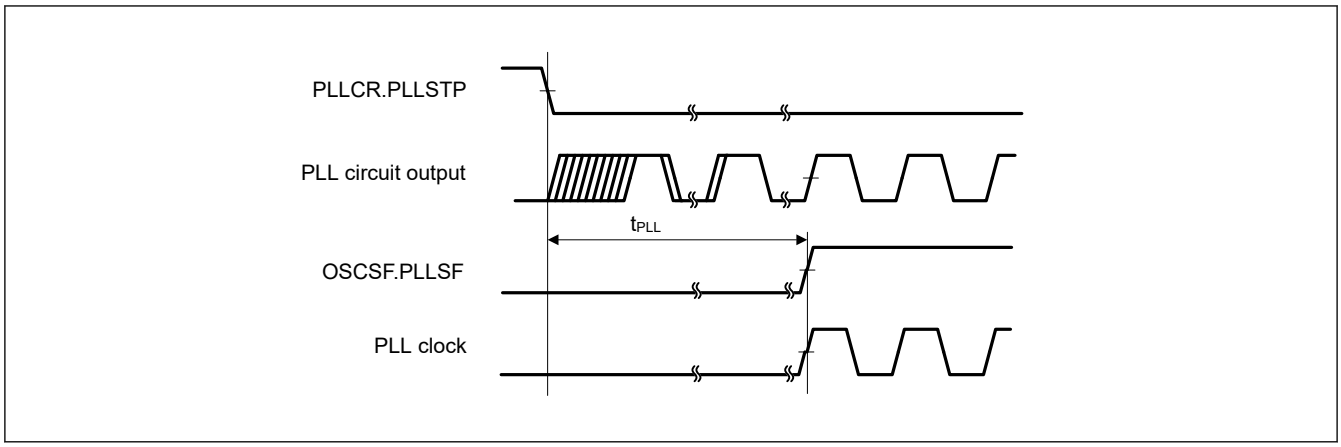


Figure 2.9 PLL clock oscillation start timing (PLL is operated after main clock oscillation has settled)

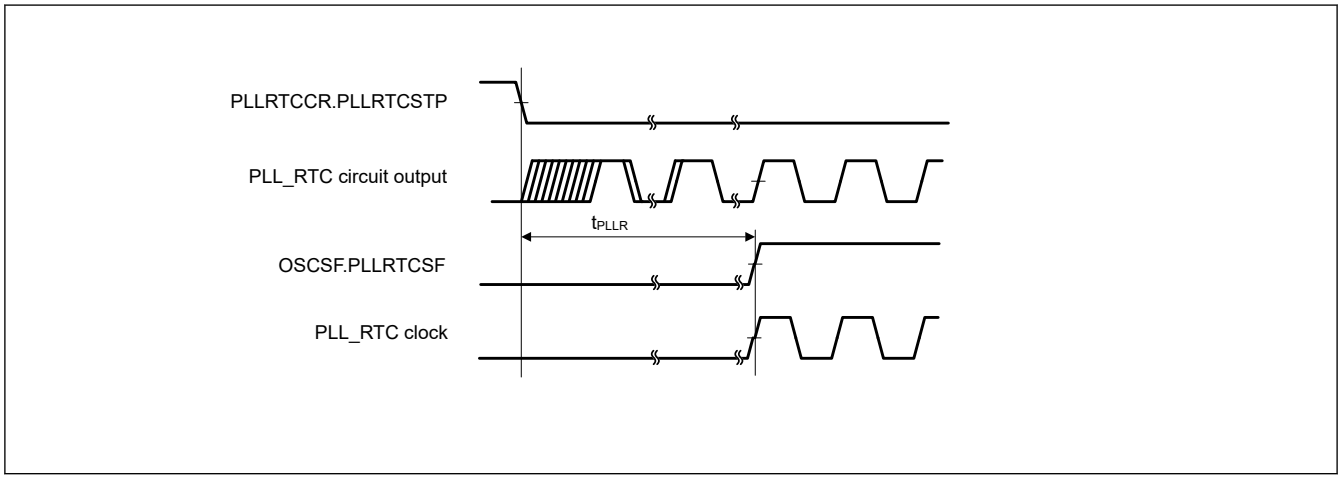


Figure 2.10 PLL_RTC clock oscillation start timing (PLL_RTC is operated after sub-clock oscillation has settled)

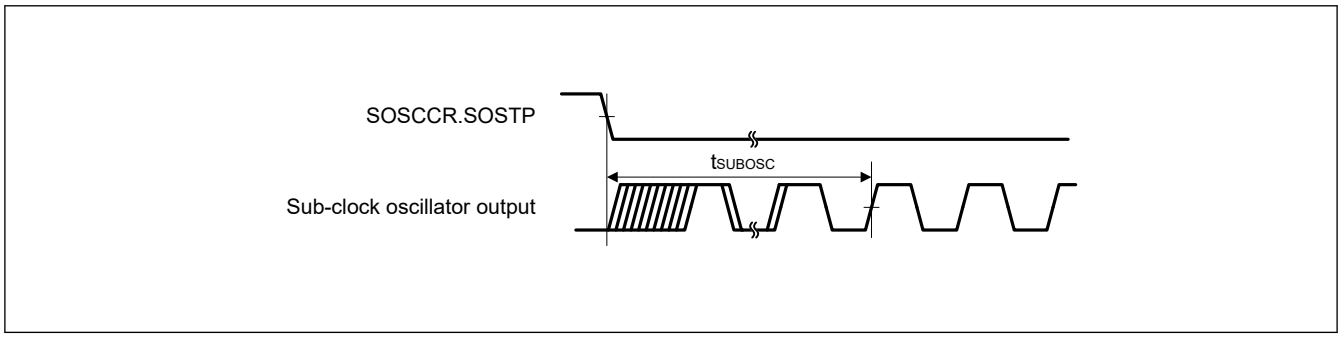


Figure 2.11 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.28 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	13	—	—	ms	Figure 2.12
	Not at power-on	t_{RESW}	30	—	—	µs	Figure 2.13
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	1.0	—	ms	Figure 2.12
	LVD0 disabled*2		—	0.3	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.13
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (IWDT reset, WDT reset, RAM parity error reset, RAM ECC error reset, Bus master MPU error reset, TrustZonre error reset, Cache parity error reset, Software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.14
	LVD0 disabled*2		—	0.2	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

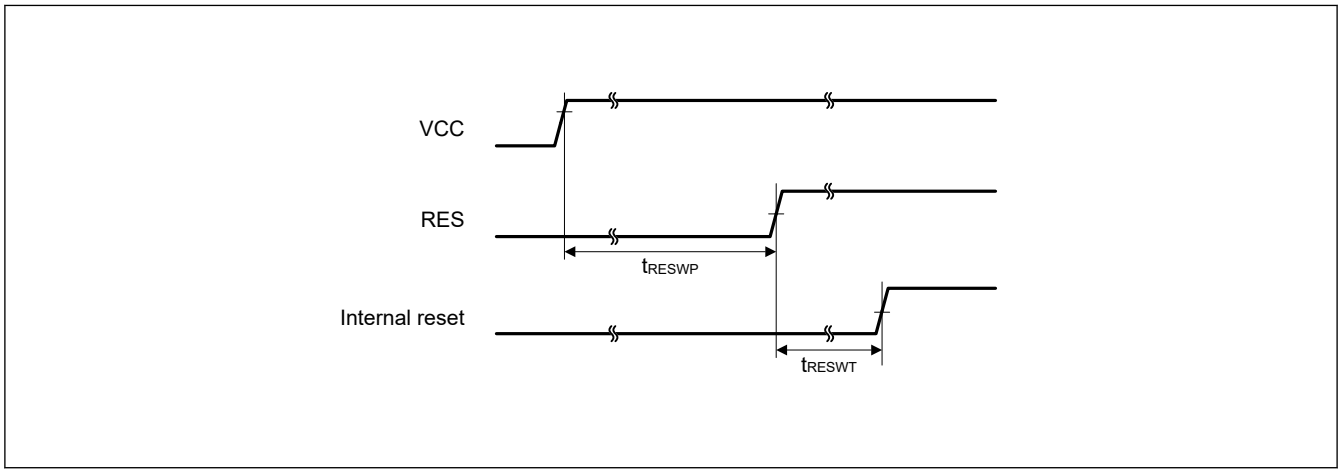


Figure 2.12 Reset input timing at power-on

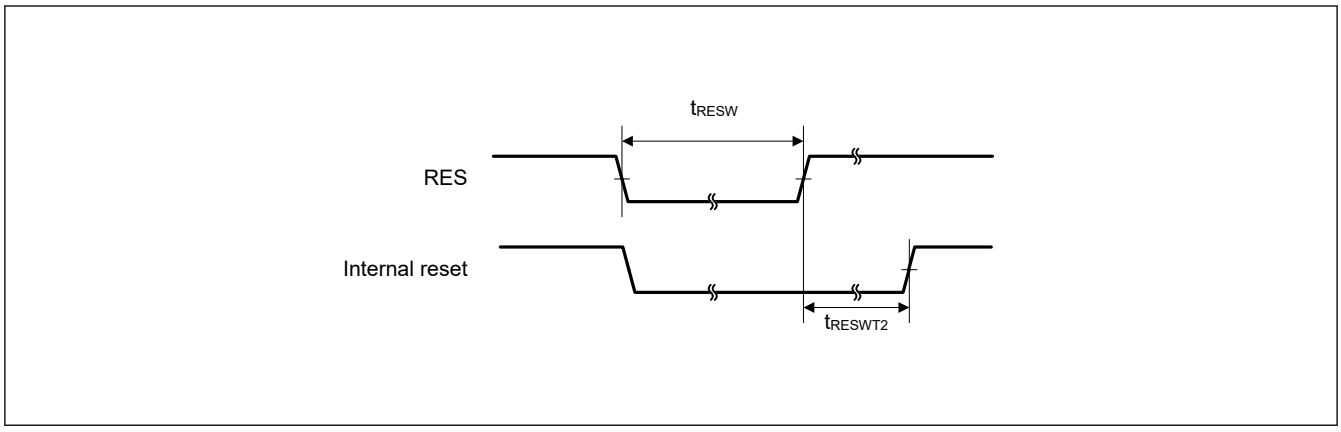


Figure 2.13 Reset input timing (1)

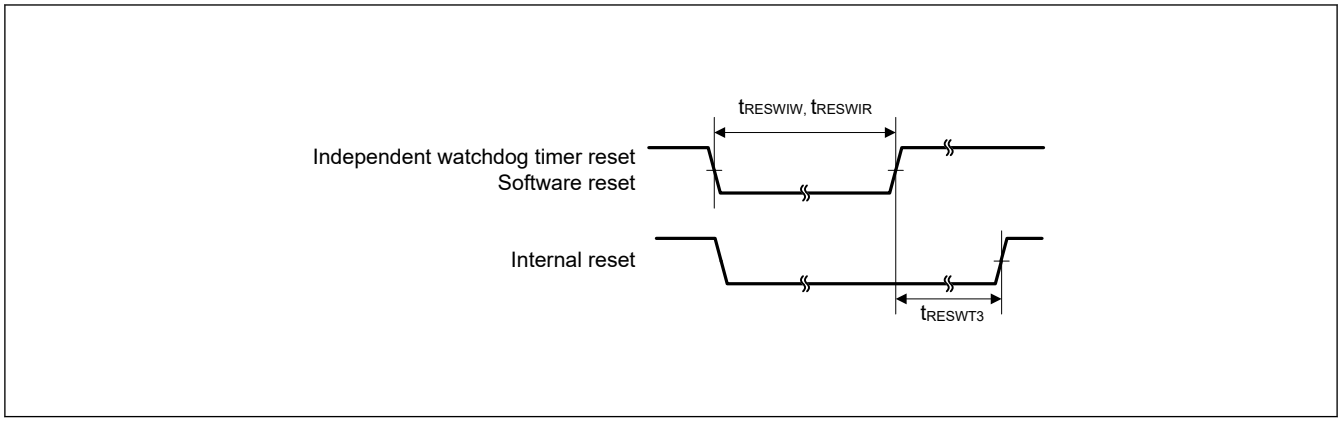


Figure 2.14 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.29 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2 *4	t_{SBYMC}	—	2.1	2.7	ms	Figure 2.15
			System clock source is PLL (48 MHz) with Main clock oscillator*2 *5	t_{SBYPC}	—	2.1	2.8	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 *4	t_{SBYEX}	—	8.5	11	µs	
			System clock source is PLL (48 MHz) with Main clock oscillator*3 *5	t_{SBYEX}	—	66	85	µs	
		System clock source is HOCO (HOCO clock is 32 MHz)*6		t_{SBYHO}	—	13.5	17.8	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)*5		t_{SBYHO}	—	13.2	17.5	µs	
		System clock source is MOCO (8 MHz)*7		t_{SBYMO}	—	3.5	5.1	µs	

Note 1. The division ratio of ICLK, FCLK, and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The ICLK is 20 MHz
Note 5. The ICLK is 48 MHz
Note 6. The ICLK is 32 MHz
Note 7. The ICLK is 8 MHz

Table 2.30 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2 *4	t_{SBYMC}	—	2.1	2.7	ms	Figure 2.15
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 *4 VCC = 1.8 V to 3.6 V	t_{SBYEX}	—	6	7.4	µs	
			System clock source is main clock oscillator (4 MHz)*3 *5 VCC = 1.6 V to 1.8 V		—	7.3	8.8	µs	
		System clock source is HOCO (32 MHz) *4	VCC = 1.8 V to 3.6 V*6	t_{SBYHO}	—	10	13	µs	
			VCC = 1.6 V to 1.8 V*7		—	13	16		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 3.6 V*8	t_{SBYMO}	—	3.5	5.1	µs	
			VCC = 1.6 V to 1.8 V*9		—	6.3	8.7		

Note 1. The division ratio of ICLK, FCLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The ICLK is 5 MHz (20 MHz/4)
Note 5. The ICLK is 4 MHz
Note 6. The ICLK is 8 MHz (32 MHz/4)
Note 7. The ICLK is 4 MHz (32 MHz/8)
Note 8. The ICLK is 8 MHz
Note 9. The ICLK is 4 MHz (8 MHz/2)

Table 2.31 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2 *4	t_{SBYMC}	—	2.1	2.7	ms	Figure 2.15
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 *4	t_{SBYEX}	—	41	46	µs	
		System clock source is MOCO (8 MHz)*5		t_{SBYMO}	—	23	30	µs	

Note 1. The division ratio of ICLK, FCLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The ICLK is 0.625 MHz (20/32 MHz)
Note 5. The ICLK is 1 MHz (8 MHz/8)

Table 2.32 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.8	0.9	ms	Figure 2.15
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.8	1	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

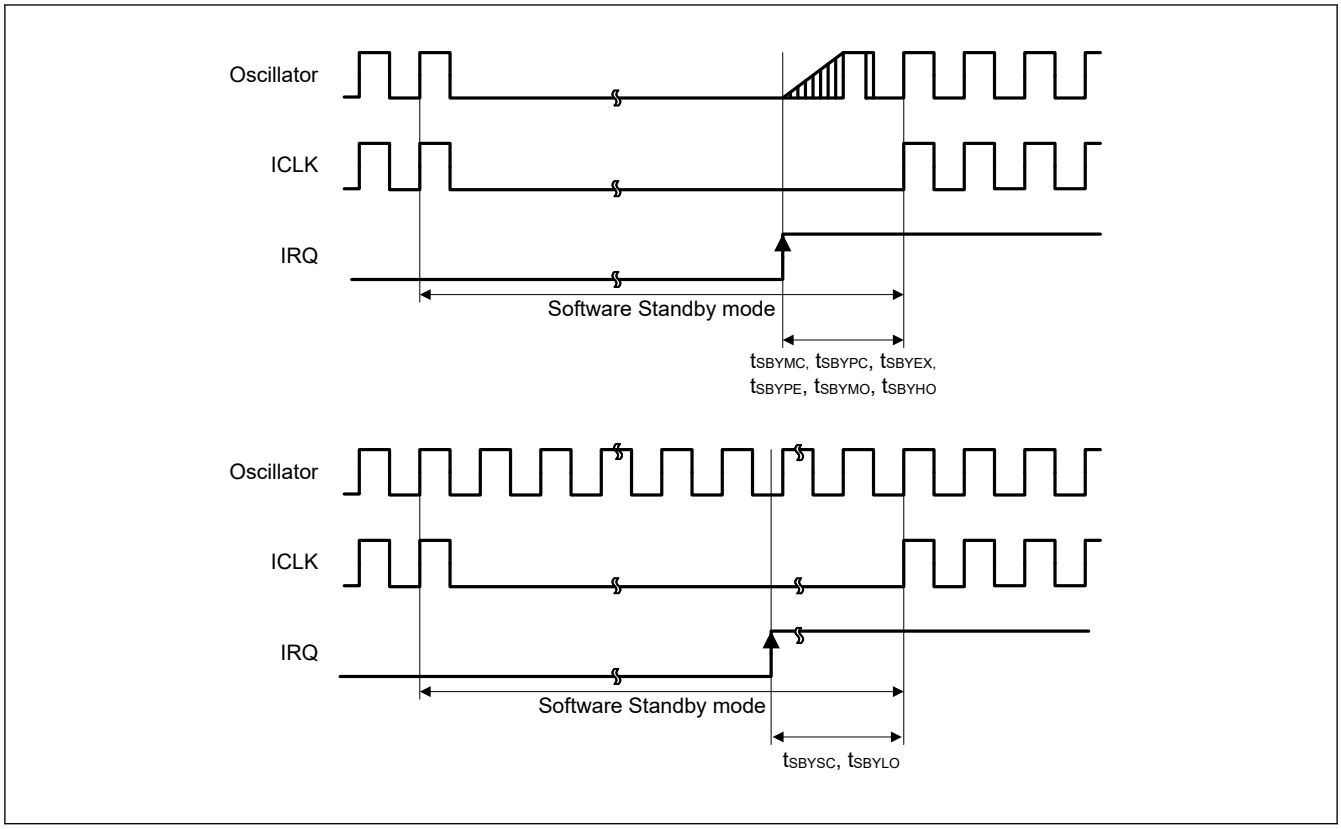
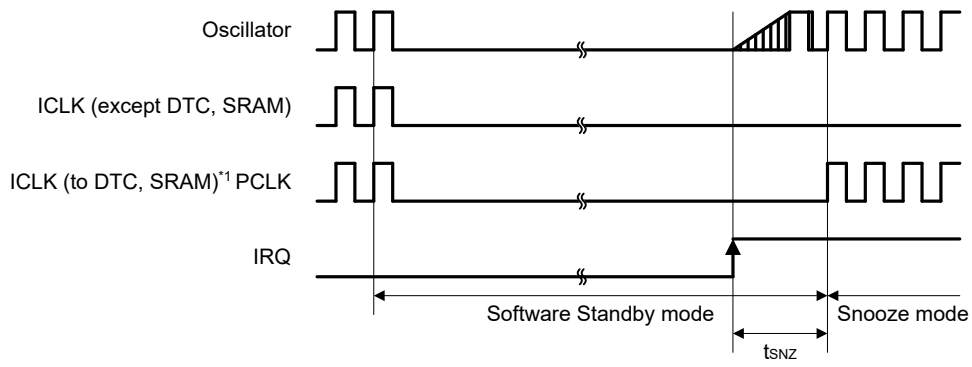


Figure 2.15 Software Standby mode cancellation timing

Table 2.33 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode System clock source is HOCO (32 MHz)*1	t_{SNZ}	—	7.4	9.3	µs	Figure 2.16
	Middle-speed mode System clock source is HOCO (24 MHz)*2 VCC = 1.8 V to 3.6 V	t_{SNZ}	—	8.3	10.4	µs	
	Middle-speed mode System clock source is HOCO (24 MHz)*3 VCC = 1.6 V to 1.8 V	t_{SNZ}	—	9.5	11.8	µs	
	Low-speed mode System clock source is MOCO (8 MHz)*4	t_{SNZ}	—	11.8	15.6	µs	

Note 1. The ICLK is 32 MHz
Note 2. The ICLK is 8 MHz (24 MHz/4)
Note 3. The ICLK is 4 MHz (24 MHz/8)
Note 4. The ICLK is 1 MHz (8 MHz/8)



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.16 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.34 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

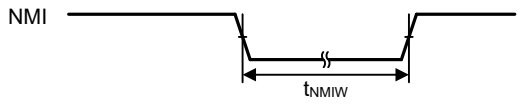


Figure 2.17 NMI interrupt input timing

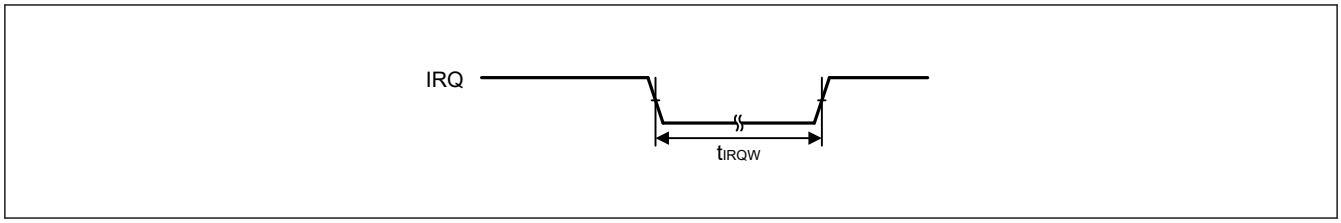


Figure 2.18 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.35 I/O Ports, POEG, GPT, AGT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.19
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.20
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.21
		Dual edge		2.5	—		
AGT	AGTIO, AGTEE input cycle	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC} *1	250	—	ns	Figure 2.22
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO, AGTEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 2.22
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.23

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

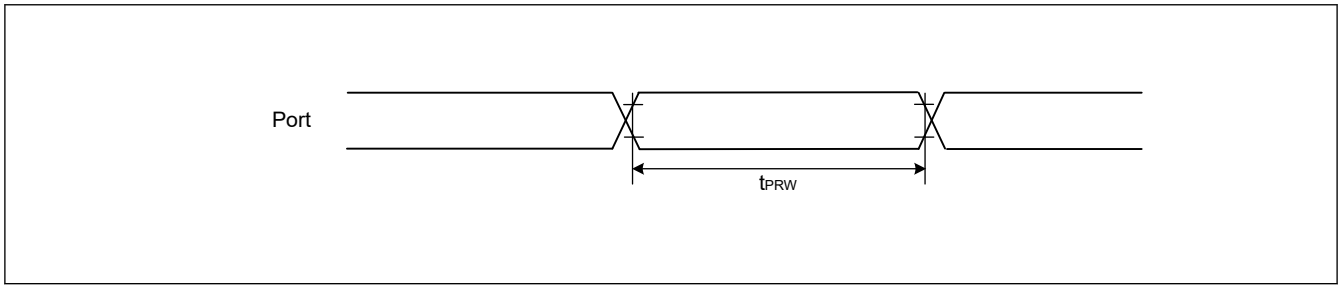


Figure 2.19 I/O ports input timing

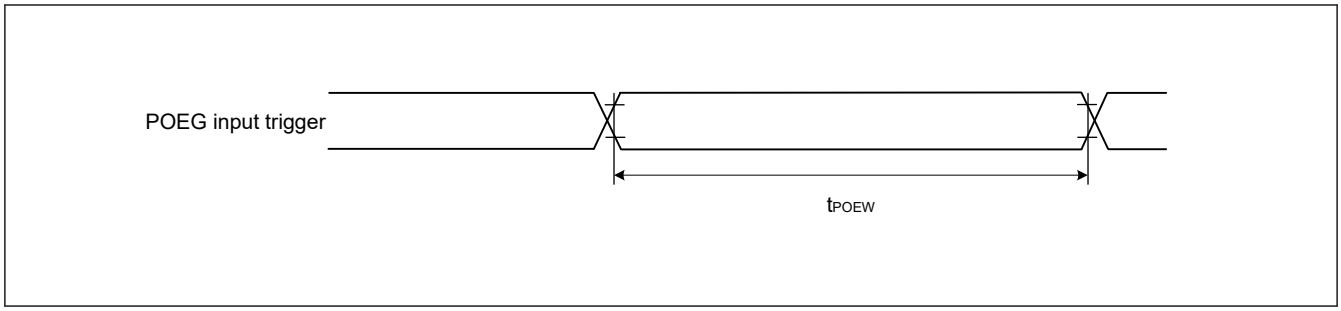


Figure 2.20 POEG input trigger timing

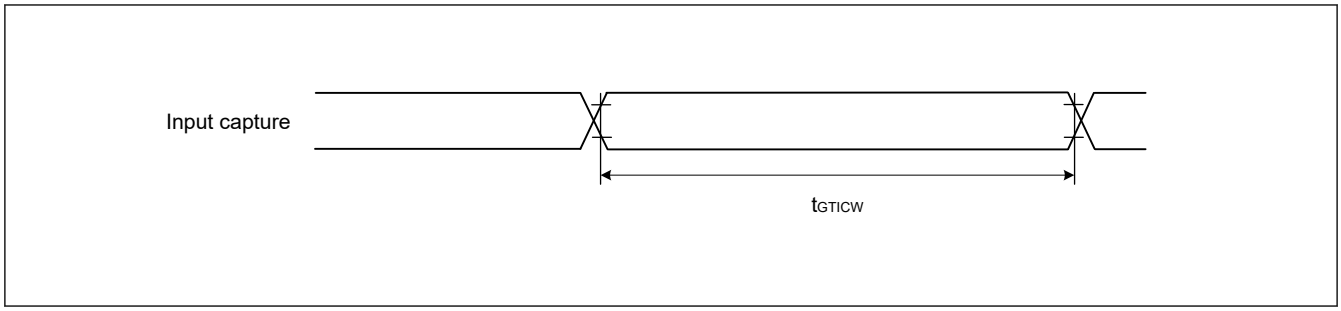


Figure 2.21 GPT input capture timing

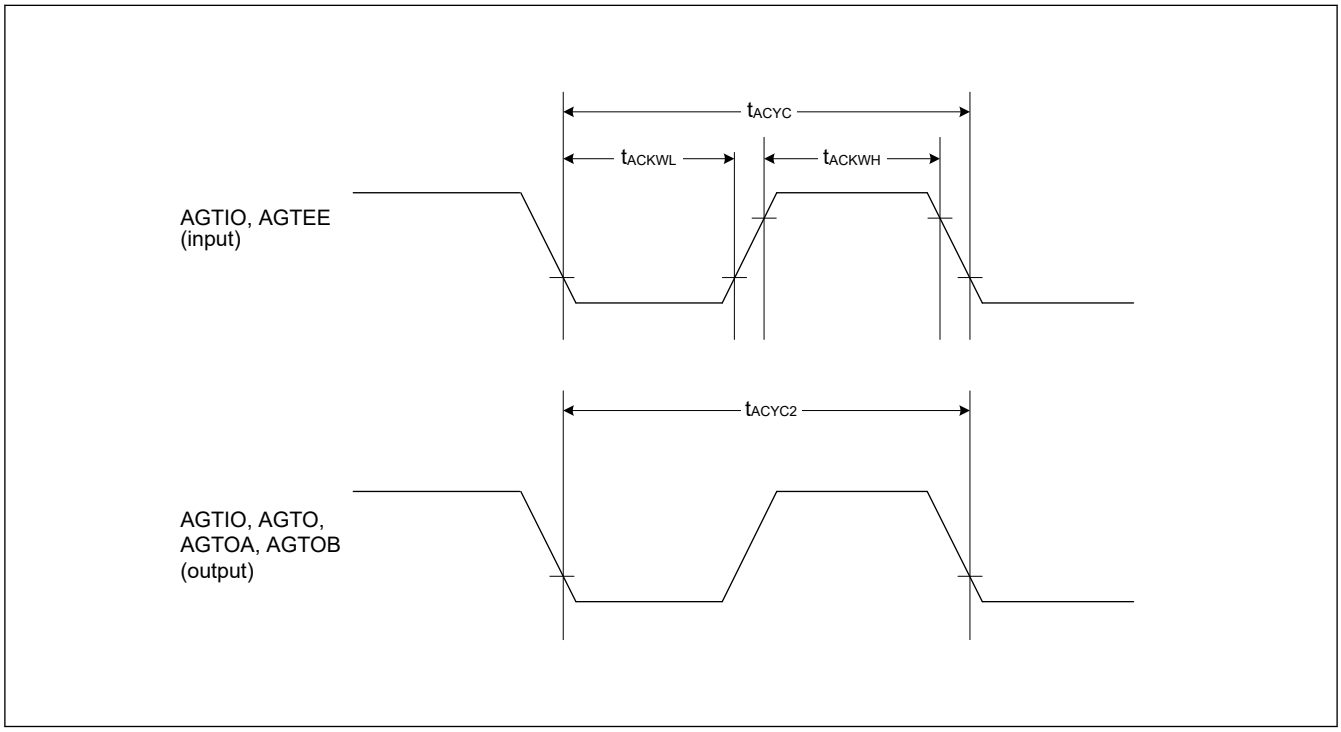


Figure 2.22 AGT I/O timing

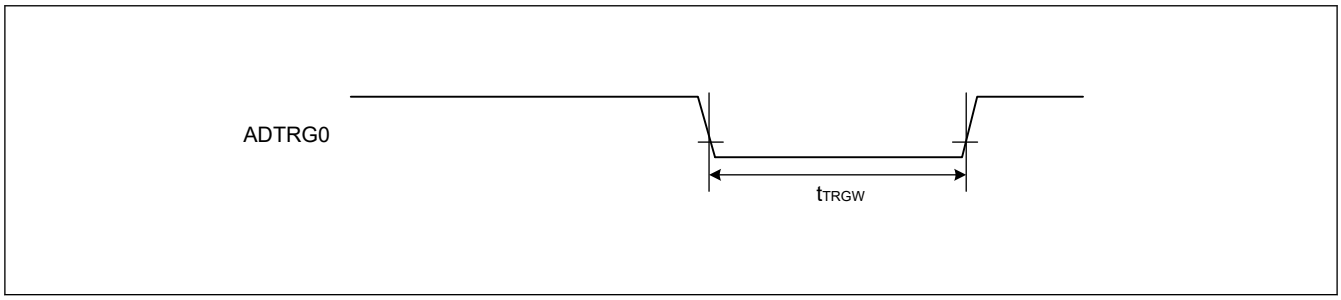


Figure 2.23 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.36 CAC timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
CACREF input pulse width	$t_{PBcyc} \leq t_{CAC}$ *1	t_{CACREF}	$4.5 \times t_{CAC} + 3 \times t_{PBcyc}$	—	—	ns	—
	$t_{PBcyc} > t_{CAC}$ *1		$5 \times t_{CAC} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{CAC}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.37 SCI timing (1) (1 of 2)

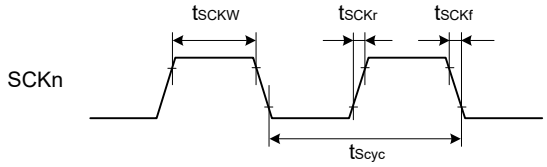
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 3.6 V	t_{Scyc}	75	—	ns	Figure 2.24
			2.4 V ≤ VCC < 2.7 V		150	—		
			1.8 V ≤ VCC < 2.4 V		300	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 3.6 V		100	—		
			2.4 V ≤ VCC < 2.7 V		200	—		
			1.8 V ≤ VCC < 2.4 V		400	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	10	ns	
	Input clock fall time			t_{SCKf}	—	10	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 3.6 V	t_{Scyc}	75 (exclude SCI1) 100 (SCI1)	—	ns	
			2.4 V ≤ VCC < 2.7 V		150 (exclude SCI1) 200 (SCI1)	—		
			1.8 V ≤ VCC < 2.4 V		300 (exclude SCI1) 400 (SCI1)	—		
			1.6 V ≤ VCC < 1.8 V		1500 (exclude SCI1) 2000 (SCI1)	—		
		Clock synchronous	1.8 V ≤ VCC ≤ 3.6 V		75	—		
			2.4 V ≤ VCC < 2.7 V		150	—		
			1.8 V ≤ VCC < 2.4 V		300	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 3.6 V	t_{SCKr}	—	7.5	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 3.6 V	t_{SCKf}	—	7.5	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 3.6 V	t_{TXD}	—	25	ns	Figure 2.25
			2.4 V ≤ VCC < 2.7 V		—	30		
			1.8 V ≤ VCC < 2.4 V		—	65		
			1.6 V ≤ VCC < 1.8 V		—	110		
	Transmit data delay time (slave)	Clock synchronous	1.8 V ≤ VCC ≤ 3.6 V		—	35	ns	
			2.4 V ≤ VCC < 2.7 V		—	40		
			1.8 V ≤ VCC < 2.4 V		—	65		
			1.6 V ≤ VCC < 1.8 V		—	95		

Table 2.37 SCI timing (1) (2 of 2)

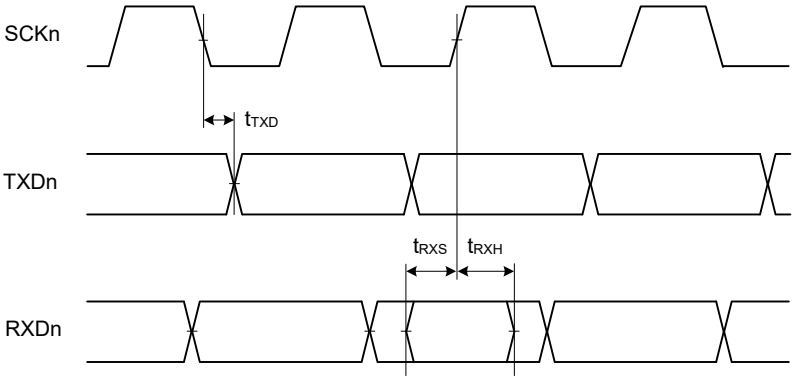
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Receive data setup time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 3.6 V	t_{RXS}	35	—	ns	Figure 2.25
			2.4 V ≤ VCC < 2.7 V		40	—		
			1.8 V ≤ VCC < 2.4 V		65	—		
			1.6 V ≤ VCC < 1.8 V		90	—		
	Receive data setup time (slave)	Clock synchronous	2.4 V ≤ VCC ≤ 3.6 V		10	—	ns	
			1.8 V ≤ VCC ≤ 2.4 V		15	—		
			1.6 V ≤ VCC < 1.8 V		20	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	5	—	ns	



Note: n = 0, 1, 3 to 5, 9

Figure 2.24 SCK clock input timing



Note: n = 0, 1, 3 to 5, 9

Figure 2.25 SCI input/output timing in clock synchronous mode

Table 2.38 SCI timing (2) (1 of 2)

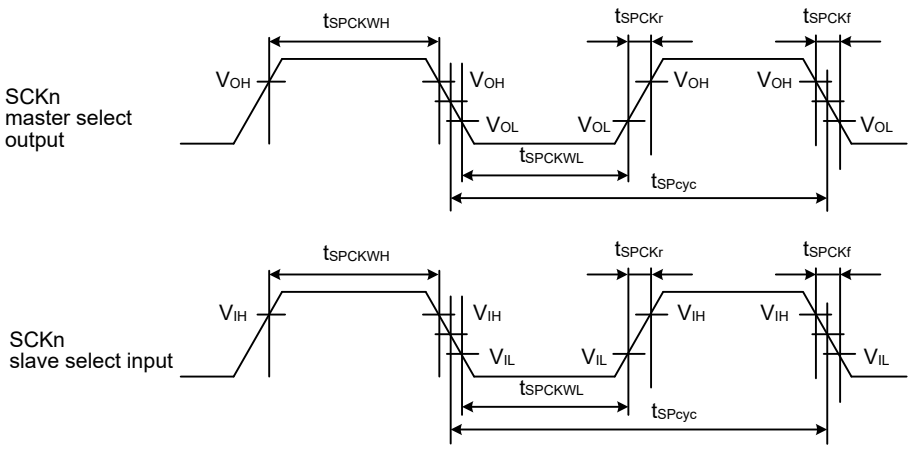
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter				Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		1.8 V ≤ VCC ≤ 3.6 V	t_{SPcyc}	75	—	ns	Figure 2.26
			2.4 V ≤ VCC < 2.7 V		150	—		
			1.8 V ≤ VCC < 2.4 V		300	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		1.8 V ≤ VCC ≤ 3.6 V		100	—		
			2.4 V ≤ VCC < 2.7 V		200	—		
			1.8 V ≤ VCC < 2.4 V		400	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time			t_{SPCKr}, t_{SPCKf}	—	10	ns	
	Data input setup time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	35	—	ns	Figure 2.27 to Figure 2.30
			2.4 V ≤ VCC < 2.7 V		40	—		
			1.8 V ≤ VCC < 2.4 V		65	—		
			1.6 V ≤ VCC < 1.8 V		90	—		
		Slave	1.8 V ≤ VCC ≤ 3.6 V		5	—		
			1.6 V ≤ VCC < 1.8 V		15	—		
	Data input hold time	Master		t_H	0	—	ns	
		Slave			18	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	2.4 V ≤ VCC ≤ 3.6 V	t_{OD}	—	25	ns	
			2.4 V ≤ VCC ≤ 2.7 V		—	32		
			1.8 V ≤ VCC ≤ 2.4 V		—	65		
			1.6 V ≤ VCC < 1.8 V		—	110		
		Slave	2.7 V ≤ VCC ≤ 3.6 V		—	38		
			2.4 V ≤ VCC ≤ 2.7 V		—	42		
			1.8 V ≤ VCC < 2.4 V		—	70		
			1.6 V ≤ VCC < 1.8 V		—	95		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{OH}	-5	—	ns	
			2.4 V ≤ VCC < 2.7 V		-10	—		
			1.8 V ≤ VCC < 2.4 V		-10	—		
			1.6 V ≤ VCC < 1.8 V		-15	—		
		Slave			-5	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 3.6 V	t_{Dr}, t_{Df}	—	5	ns	
		Slave	1.8 V ≤ VCC ≤ 3.6 V		—	5		

Table 2.38 SCI timing (2) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

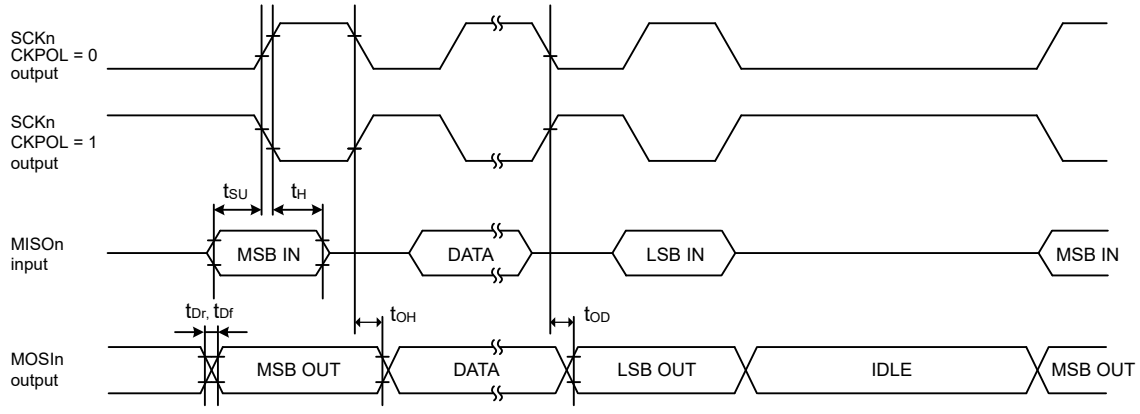
Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	Slave access time	2.7 V ≤ VCC ≤ 3.6 V	t_{SA}	—	8	t_{Pcyc}	Figure 2.27 to Figure 2.30
		2.4 V ≤ VCC < 2.7 V		—	9		
		1.8 V ≤ VCC < 2.4 V		—	13		
		1.6 V ≤ VCC < 1.8 V		—	6		
	Slave output release time	1.8 V ≤ VCC ≤ 3.6 V	t_{REL}	—	8	t_{Pcyc}	
		2.4 V ≤ VCC < 2.7 V		—	9		
		1.8 V ≤ VCC < 2.4 V		—	13		
		1.6 V ≤ VCC < 1.8 V		—	6		



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

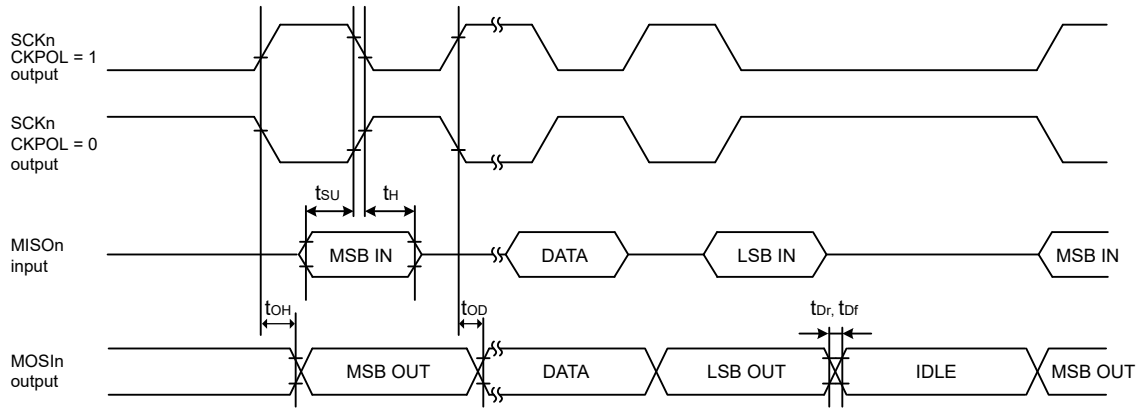
Note: n = 0, 1, 3 to 5, 9

Figure 2.26 SCI simple SPI mode clock timing



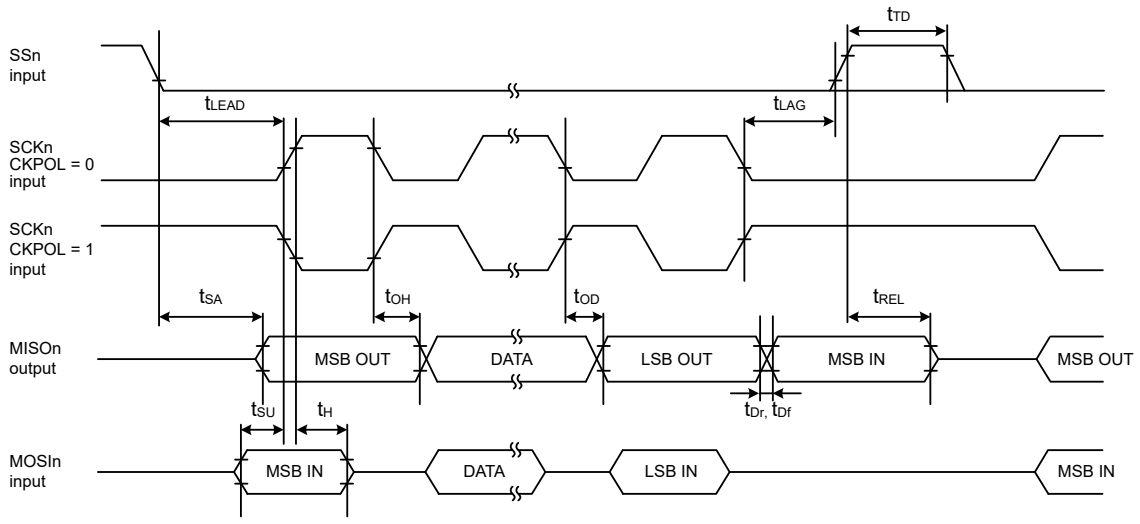
Note: n = 0, 1, 3 to 5, 9

Figure 2.27 SCI simple SPI mode timing (master, CKPH = 1)



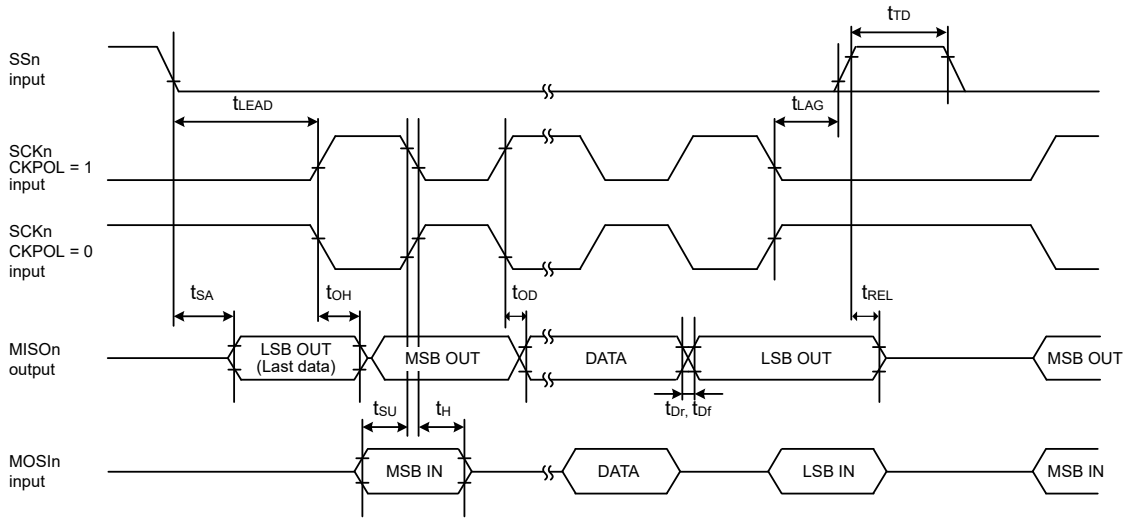
Note: n = 0, 1, 3 to 5, 9

Figure 2.28 SCI simple SPI mode timing (master, CKPH = 0)



Note: n = 0, 1, 3 to 5, 9

Figure 2.29 SCI simple SPI mode timing (slave, CKPH = 1)



Note: n = 0, 1, 3 to 5, 9

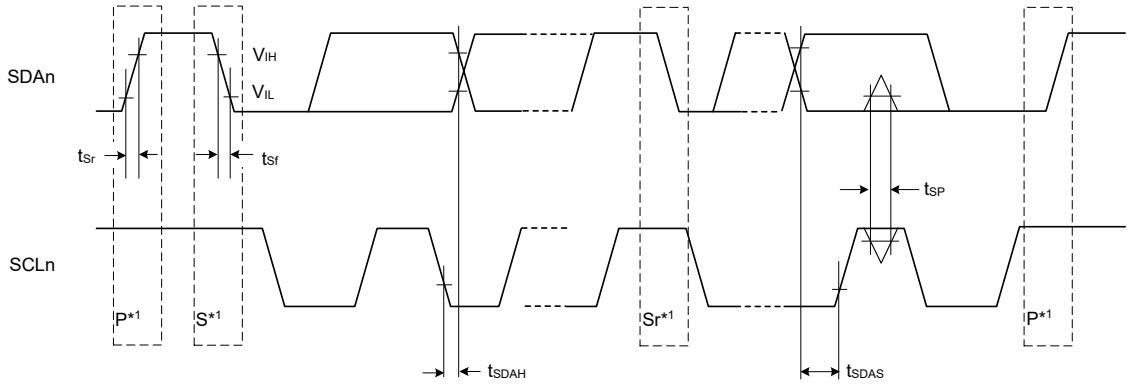
Figure 2.30 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.39 SCI timing (3)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.31
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.31
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 1, 3 to 5, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.31 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.40 SPI timing (1 of 3)

Parameter			Symbol	Min	Max	Unit	Test conditions
RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{SPcyc} *1	50	—	ns	Figure 2.32 C = 30 pF
		2.4 V ≤ VCC < 2.7 V		100	—		
		1.8 V ≤ VCC < 2.4 V		200	—		
		1.6 V ≤ VCC < 1.8 V		500	—		
	Slave	2.7 V ≤ VCC ≤ 3.6 V		100	—		
		2.4 V ≤ VCC < 2.7 V		200	—		
		1.8 V ≤ VCC < 2.4 V		400	—		
		1.6 V ≤ VCC < 1.8 V		1500	—		
RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
	Slave			0.4 × t_{SPcyc}	0.6 × t_{SPcyc}		
RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
	Slave			0.4 × t_{SPcyc}	0.6 × t_{SPcyc}		
RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 3.6 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
		2.4 V ≤ VCC < 2.7 V		—	15		
		1.8 V ≤ VCC ≤ 2.4 V		—	20		
		1.6 V ≤ VCC < 1.8 V		—	30		
	Input			—	1	µs	

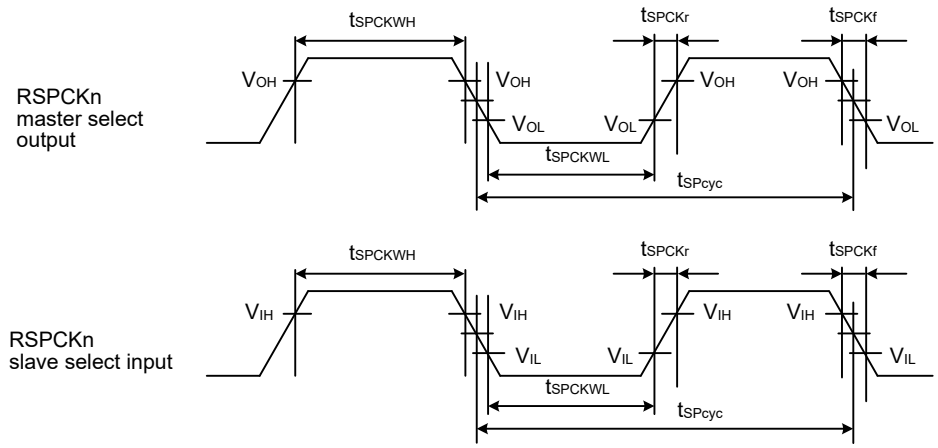
Table 2.40 SPI timing (2 of 3)

Parameter			Symbol	Min	Max	Unit	Test conditions
Data input setup time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	15	—	ns	Figure 2.33 to Figure 2.38 C = 30 pF
		2.4 V ≤ VCC < 2.7 V		25	—		
		1.8 V ≤ VCC < 2.4 V		38	—		
		1.6 V ≤ VCC < 1.8 V		0	—		
	Slave	2.4 V ≤ VCC ≤ 3.6 V		10	—		
		1.8 V ≤ VCC < 2.4 V		14	—		
		1.6 V ≤ VCC < 1.8 V		17	—		
Data input hold time	Master (RSPCK is PCLKA/2)		t_{HF}	0	—	ns	
	Master (RSPCK is not PCLKA/2)		t_{H}	t_{Pcyc}	—		
	Slave		t_{H}	10	—		
SSL setup time	Master	1.8 V ≤ VCC ≤ 3.6 V	t_{LEAD}	$-30 + N \times t_{Spcyc}$ *1	—	ns	
		1.6 V ≤ VCC < 1.8 V		$-34 + N \times t_{Spcyc}$ *1	—		
	Slave			$5 \times t_{Pcyc}$	—	ns	
SSL hold time	Master		t_{LAG}	$-30 + N \times t_{Spcyc}$ *2	—	ns	
	Slave			$5 \times t_{Pcyc}$	—	ns	
Data output delay time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{OD}	—	12	ns	
		2.4 V ≤ VCC < 2.7 V		—	12		
		1.8 V ≤ VCC < 2.4 V		—	12		
		1.6 V ≤ VCC < 1.8 V		—	12		
	Slave	2.7 V ≤ VCC ≤ 3.6 V		—	45		
		2.4 V ≤ VCC < 2.7 V		—	50		
		1.8 V ≤ VCC < 2.4 V		—	70		
		1.6 V ≤ VCC < 1.8 V		—	85		
Data output hold time	Master		t_{OH}	0	—	ns	
	Slave			0	—		
Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
	Slave			$6 \times t_{Pcyc}$	—		
MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 3.6 V	t_{Dr}, t_{Df}	—	5	ns	Figure 2.33 to Figure 2.38 C = 30 pF
		2.4 V ≤ VCC < 2.7 V		—	15		
		1.8 V ≤ VCC < 2.4 V		—	20		
		1.6 V ≤ VCC < 1.8 V		—	30		
	Input			—	1		
SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 3.6 V	t_{SSLr}, t_{SSLf}	—	5	ns	
		2.4 V ≤ VCC < 2.7 V		—	15		
		1.8 V ≤ VCC < 2.4 V		—	20		
		1.6 V ≤ VCC < 1.8 V		—	30		
	Input			—	1		

Table 2.40 SPI timing (3 of 3)

Parameter		Symbol	Min	Max	Unit	Test conditions
Slave access time	2.7 V ≤ VCC ≤ 3.6 V	t_{SA}	—	2 × t_{Pcyc} + 11	ns	Figure 2.37 and Figure 2.38 C = 30 pF
	2.4 V ≤ VCC < 2.7 V		—	2 × t_{Pcyc} + 15		
	1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 35		
	1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 55		
Slave output release time	2.7 V ≤ VCC ≤ 3.6 V	t_{REL}	—	2 × t_{Pcyc} + 11	ns	
	2.4 V ≤ VCC < 2.7 V		—	2 × t_{Pcyc} + 15		
	1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 35		
	1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 55		

Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set as an integer from 1 to 8 by the SPCKD register.
Note 2. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A or B

Figure 2.32 SPI clock timing

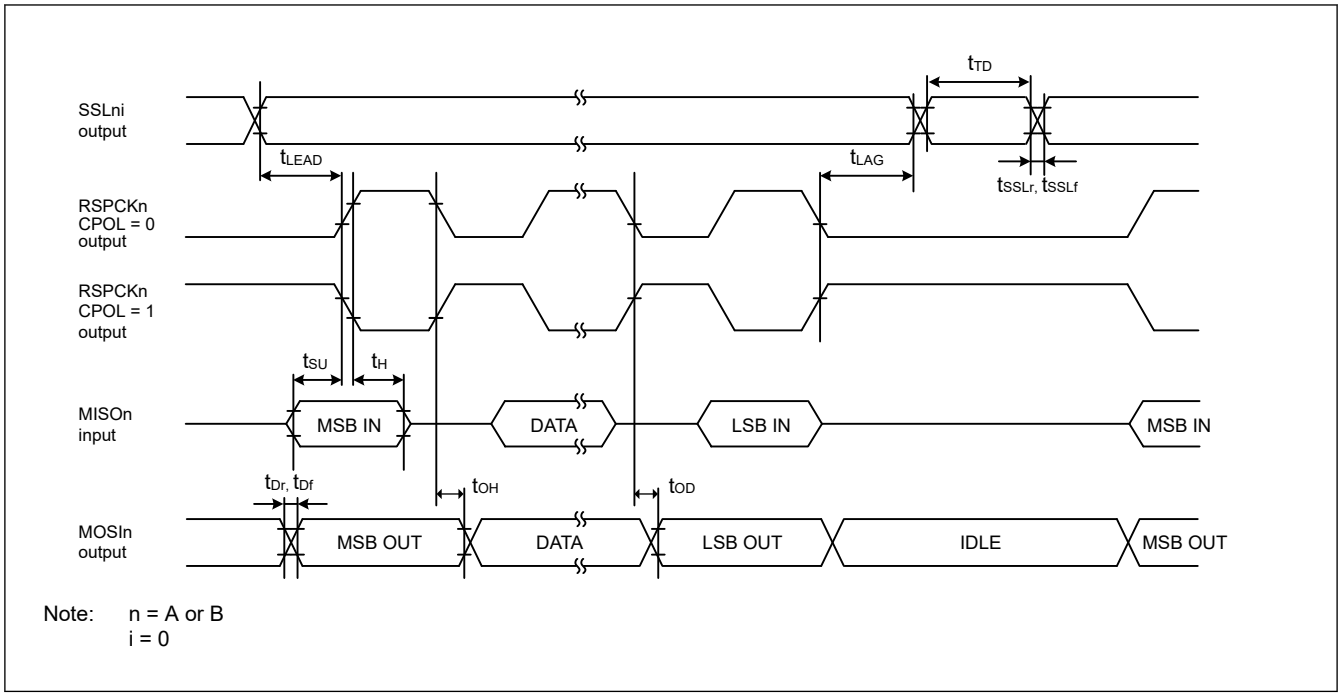


Figure 2.33 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

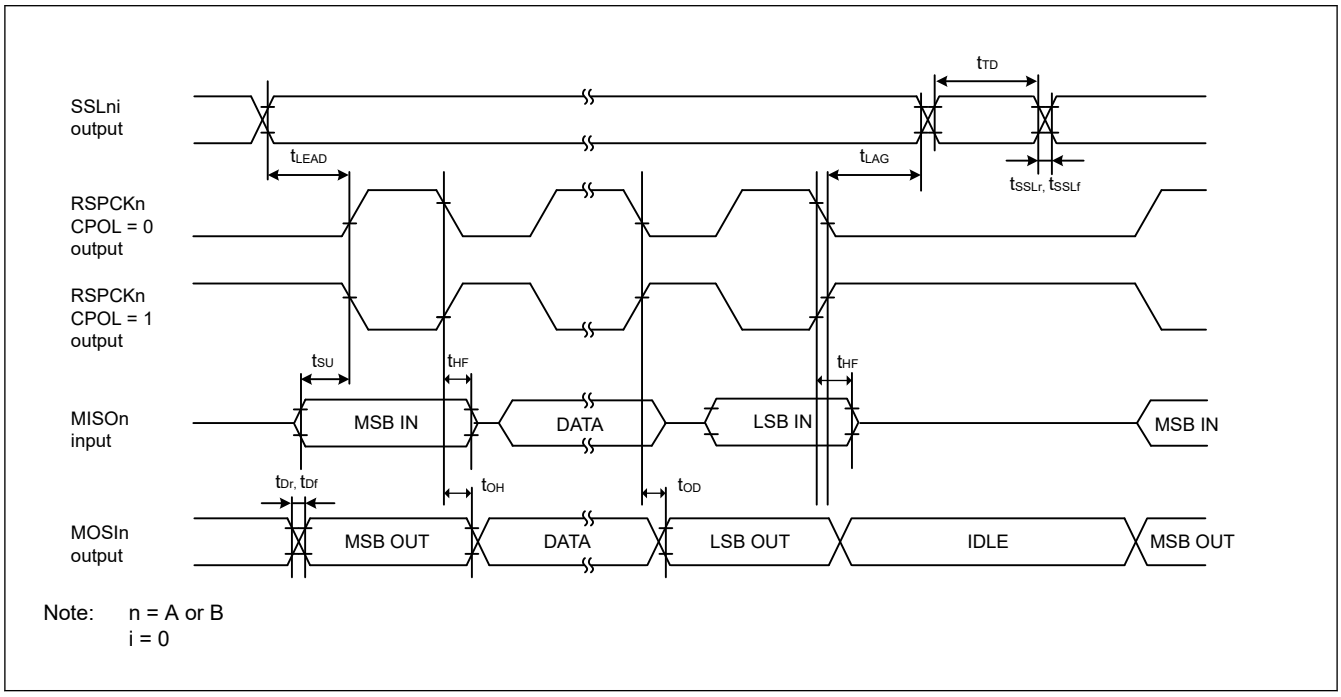
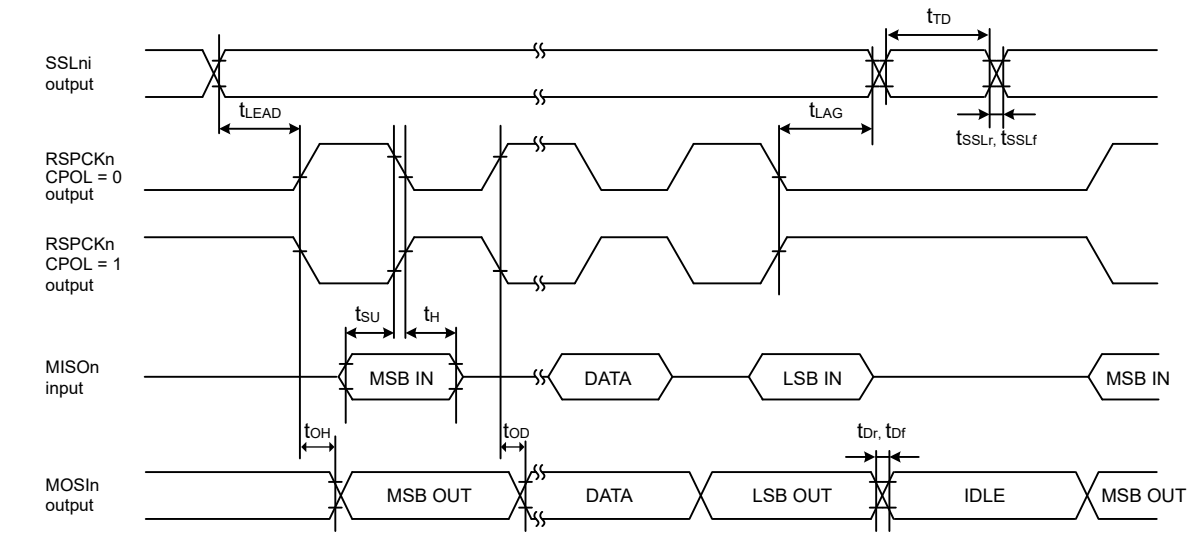
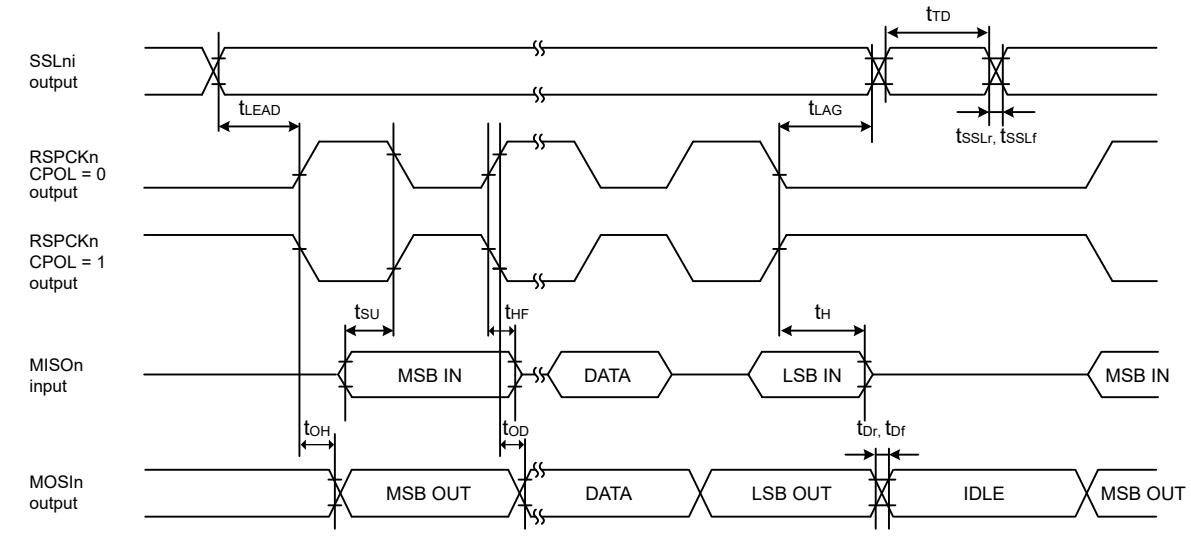


Figure 2.34 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)



Note: n = A or B
i = 0

Figure 2.35 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)



Note: n = A or B
i = 0

Figure 2.36 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

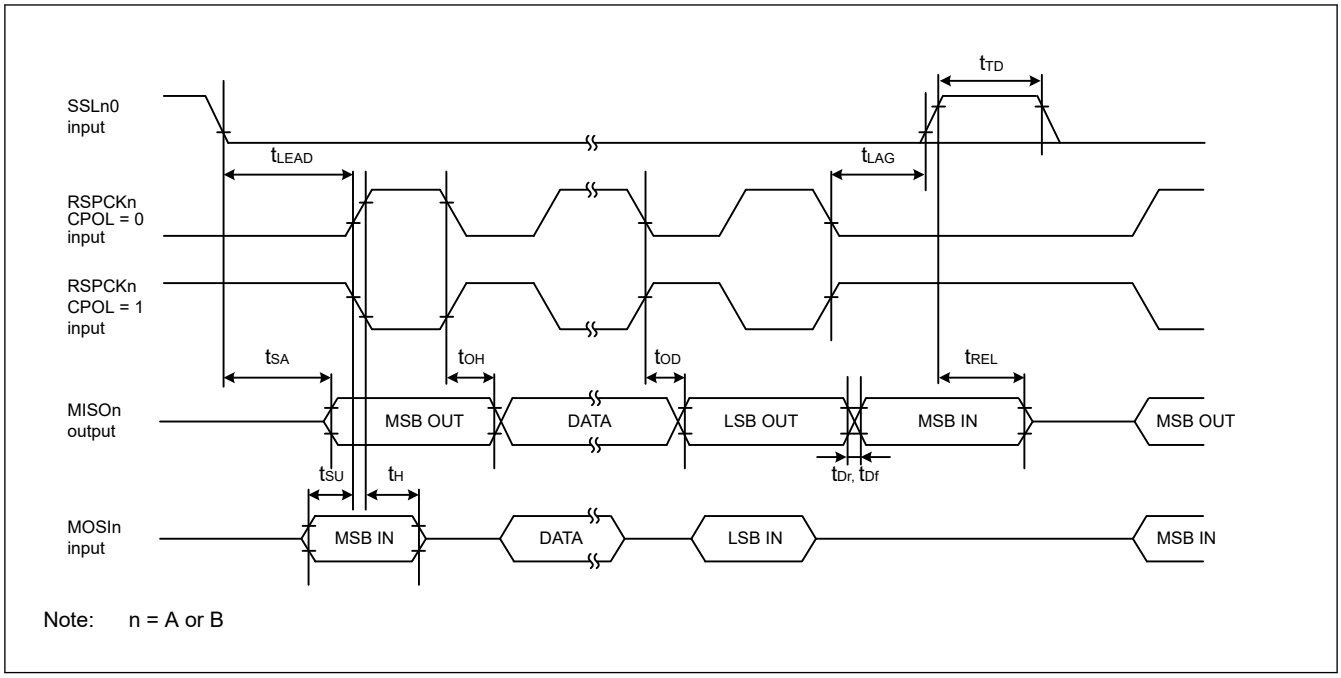


Figure 2.37 SPI timing (slave, CPHA = 0)

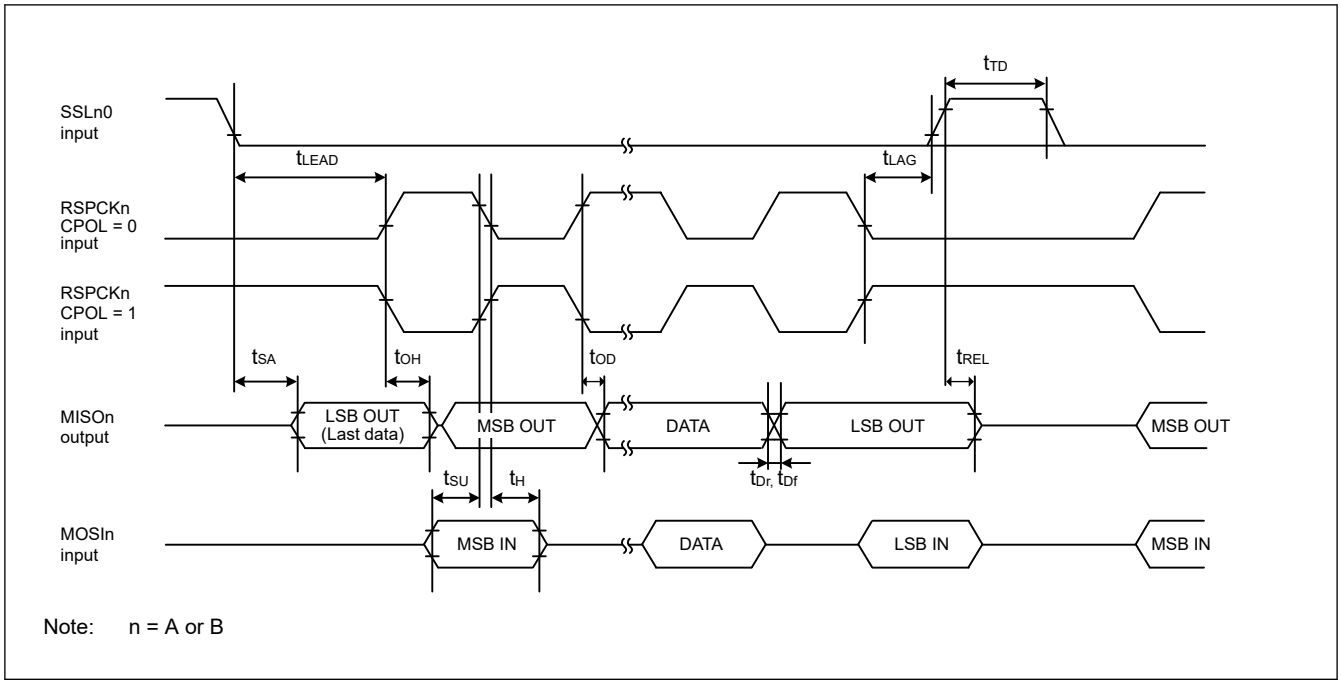


Figure 2.38 SPI timing (slave, CPHA = 1)

2.3.10 QSPI Timing

Table 2.41 QSPI timing (1 of 2)

Parameter		Symbol	Min	Max	Unit	Test conditions
QSPCK clock cycle	2.4 V ≤ VCC ≤ 3.6 V	t_{QScyc}	50	—	ns	Figure 2.39
	1.8 V ≤ VCC < 2.4 V		100	—	ns	
	1.6 V ≤ VCC < 1.8 V		500	—	ns	
QSPCK clock high pulse width		t_{QSWH}	t_{QScyc} × 0.4	—	ns	
QSPCK clock low pulse width		t_{QSWL}	t_{QScyc} × 0.4	—	ns	

Table 2.41 QSPI timing (2 of 2)

Parameter		Symbol	Min	Max	Unit	Test conditions
Data input setup time	2.4 V ≤ VCC ≤ 3.6 V	t_{Su}	10	—	ns	Figure 2.40
	1.8 V ≤ VCC < 2.4 V		15	—	ns	
	1.6 V ≤ VCC < 1.8 V		15	—	ns	
Data input hold time	1.8 V ≤ VCC < 3.6 V	t_{IH}	0	—	ns	
	1.6 V ≤ VCC < 1.8 V		4	—	ns	
QSSL setup time	2.4 V ≤ VCC ≤ 3.6 V	t_{Su}	(N + 0.5) × t_{Qscyc} − 9*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	1.8 V ≤ VCC < 2.4 V		(N + 0.5) × t_{Qscyc} − 15*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	1.6 V ≤ VCC < 1.8 V		(N + 0.5) × t_{Qscyc} − 24*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
QSSL hold time	1.8 V ≤ VCC ≤ 3.6 V	t_{LAG}	(N + 0.5) × t_{Qscyc} − 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	1.6 V ≤ VCC < 1.8 V		(N + 0.5) × t_{Qscyc} − 8*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
Data output delay	2.4 V ≤ VCC ≤ 3.6 V	t_{OD}	—	9	ns	
	1.8 V ≤ VCC < 2.4 V		—	16	ns	
	1.6 V ≤ VCC < 1.8 V		—	24	ns	
Data output hold time	1.8 V ≤ VCC ≤ 3.6 V	t_{OH}	−3.3	—	ns	
	1.6 V ≤ VCC < 1.8 V		−6.3	—	ns	
Successive transmission delay		t_{TD}	1	16	t_{QScyc}	

Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.

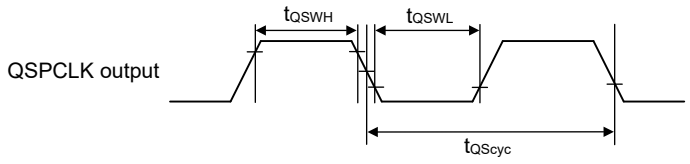


Figure 2.39 QSPI clock timing

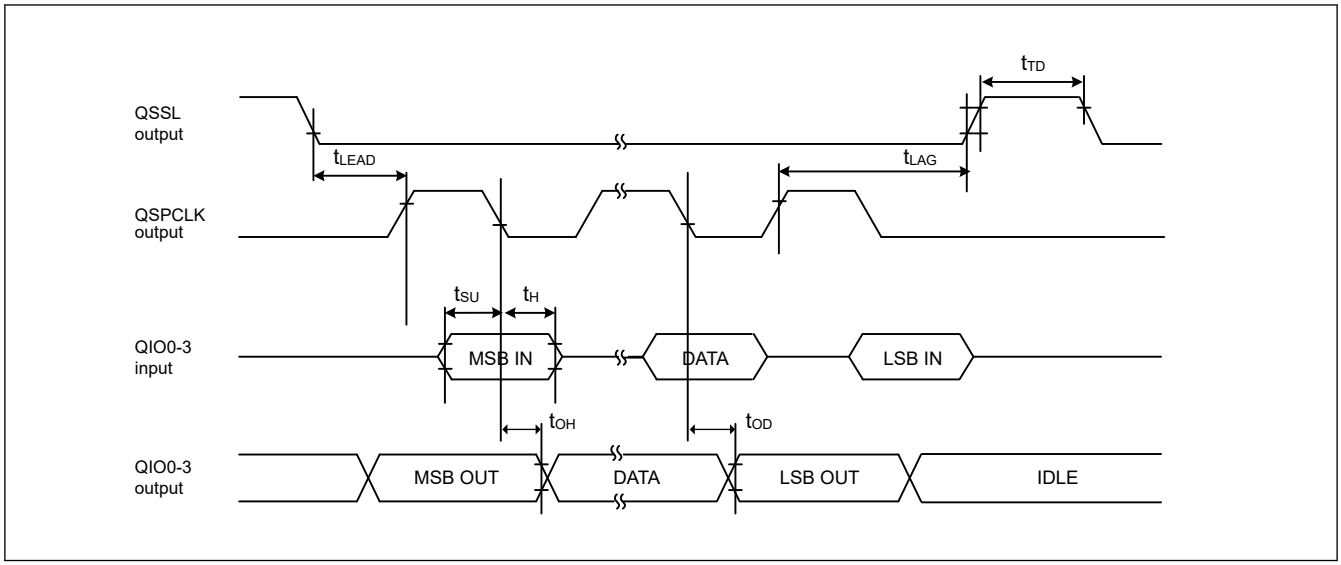


Figure 2.40 Transmit and receive timing

2.3.11 IIC Timing

Table 2.42 IIC timing (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit	Test conditions
IIC (standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.41
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Table 2.42 IIC timing (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit	Test conditions
IIC (Fast mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.41
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc}+ 300	—	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: Use pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership.The AC portion of the electrical characteristics is measured for each group.

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

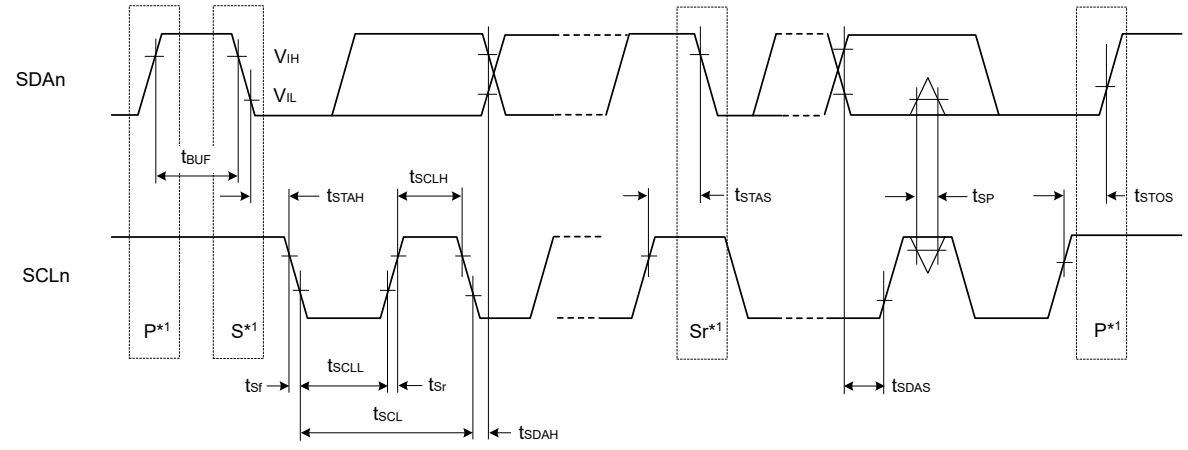
Note 2. C_b indicates the total capacity of the bus line.

Table 2.43 IIC timing (2)

Conditions: VCC = AVCC0 = 2.7 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	—	ns	Figure 2.41
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	—	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note: The Fast-mode Plus enable bit (FMPE) is supported by IIC0 (SCL0_A, SDA0_A) and IIC1 (SCL1_A, SDA1_A).
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. C_b indicates the total capacity of the bus line.



Note: n = 0, 1
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.41 I²C bus interface input/output timing

2.3.12 UARTA Timing

Table 2.44 UARTA interface timing

Parameter	Symbol	Min.	Max.	Unit	Test conditions
Transfer rate	—	200	153600	bps	—

2.3.13 CANFD Timing

Table 2.45 CANFD interface timing

Parameter	Symbol	CAN		CANFD		Unit	Test conditions
		Min	Max	Min	Max		
Internal delay time	t_{node}	—	100	—	75	ns	Figure 2.42

Note: $t_{node} = t_{d(CTX)} + t_{d(CRX)}$

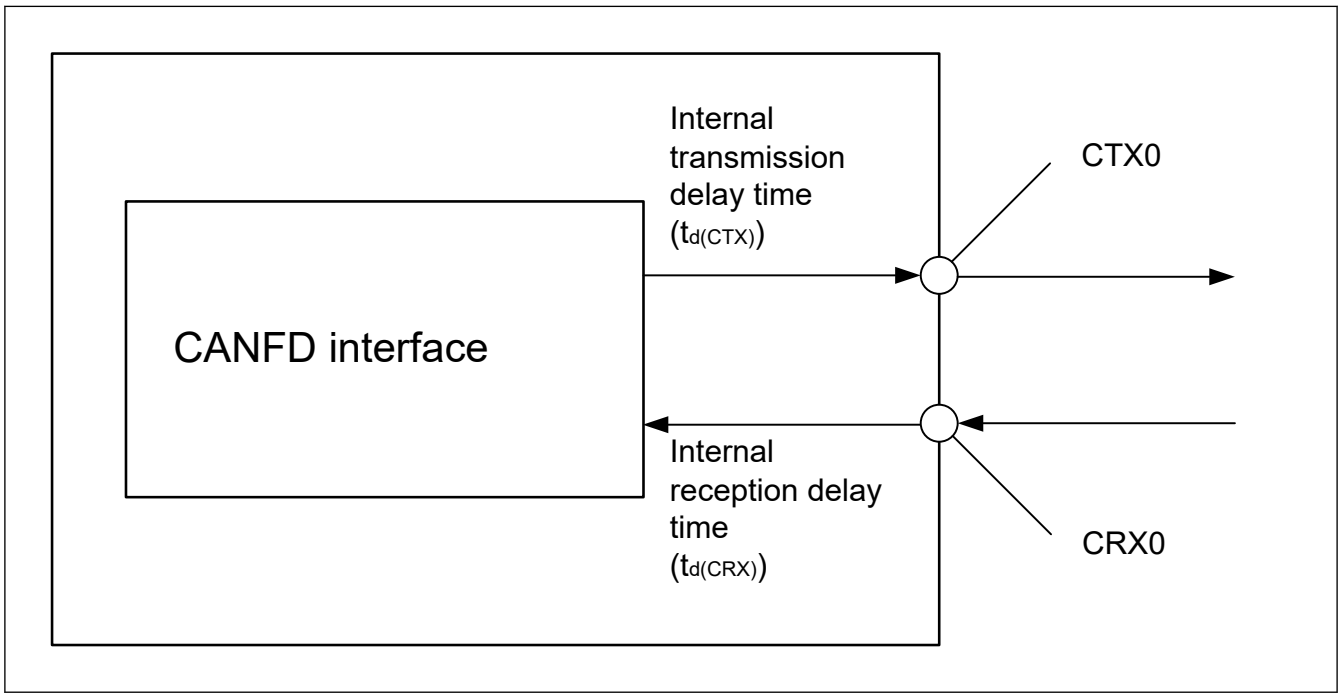


Figure 2.42 CANFD interface condition

2.4 ADC12 Characteristics

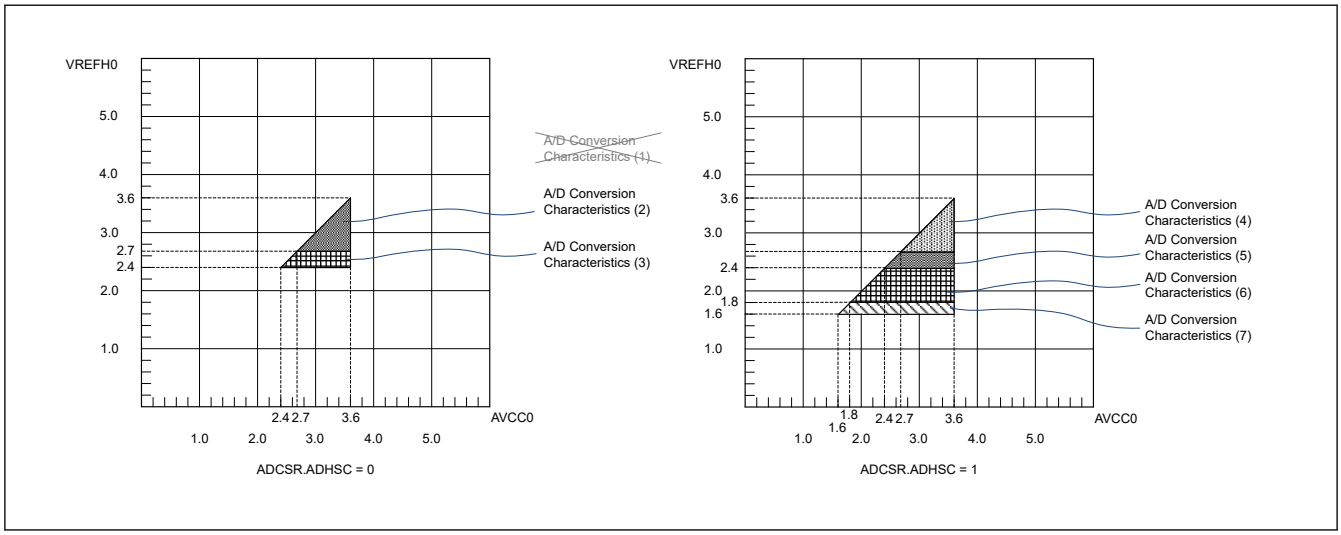


Figure 2.43 AVCC0 to VREFH0 voltage range

Table 2.46 A/D conversion characteristics (1) in high-speed A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.47 A/D conversion characteristics (2) in high-speed A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
		—	—	7.0*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)*4	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.50	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.48 A/D conversion characteristics (3) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency	1	—	24	MHz	—

Table 2.48 A/D conversion characteristics (3) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.49 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.49 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±7.0	LSB	High-precision channel
				±10.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.50 A/D conversion characteristics (5) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 3.6 V[*5] (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	6[*3]	kΩ	High-precision channel
		—	—	14[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1

Table 2.50 A/D conversion characteristics (5) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 3.6 V[*5] (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Offset error	—	±1.25	±7.5	LSB	High-precision channel
			±10.0	LSB	Other than specified
Full-scale error	—	±1.5	±7.5	LSB	High-precision channel
			±10.0	LSB	Other than specified
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±3.75	±9.5	LSB	High-precision channel
			±13.5	LSB	Other than specified
DNL differential nonlinearity error	—	±2.0	—	LSB	—
INL integral nonlinearity error	—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.51 A/D conversion characteristics (6) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 3.6 V[*5] (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	12[*3]	kΩ	High-precision channel
		—	—	28[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—

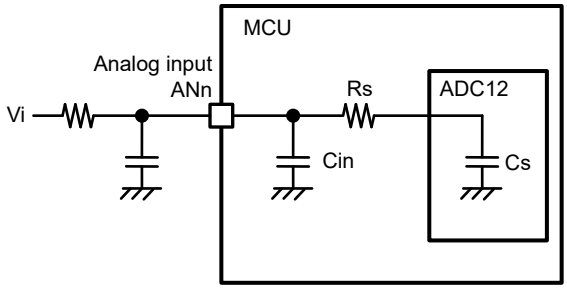
Table 2.51 A/D conversion characteristics (6) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 3.6 V*5 (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Absolute accuracy	—	±3.75	±9.5	LSB	High-precision channel
			±13.5	LSB	Other than specified
DNL differential nonlinearity error	—	±2.0	—	LSB	—
INL integral nonlinearity error	—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.44 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.44 Equivalent circuit for analog input

Table 2.52 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN006	AVCC0 = 1.6 to 3.6 V	Pins AN000 to AN006 cannot be used as general I/O, when the A/D converter is in use.
Normal-precision channel	AN017 to AN025		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.8 to 3.6 V	—
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.8 to 3.6 V	—

Table 2.53 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 3.6 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKC (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 1.8 V.

Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.

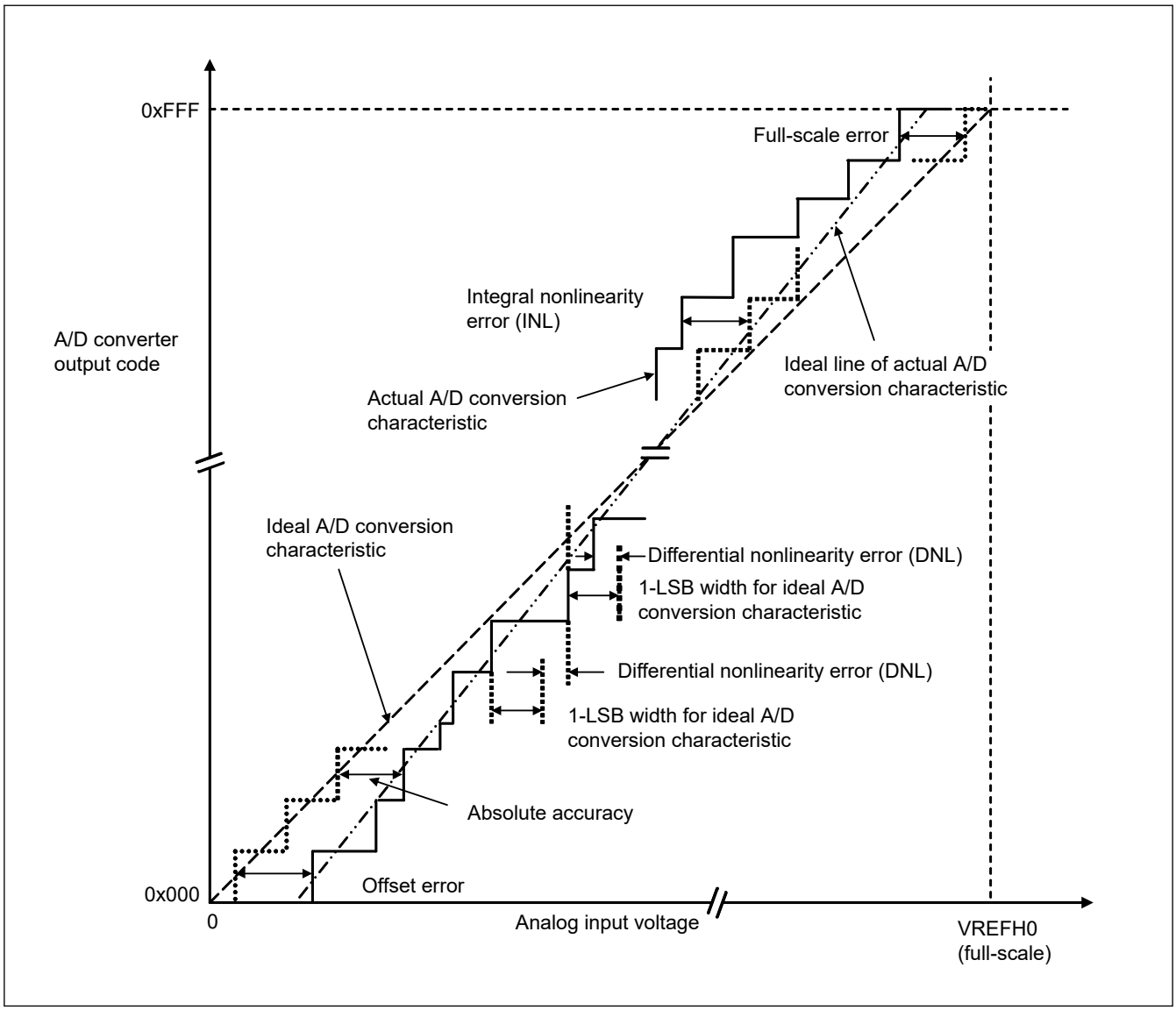


Figure 2.45 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 TSN Characteristics

Table 2.54 TSN characteristics

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	±1.5	—	°C	VCC = AVCC0 ≥ 2.4 V*1
		—	±2.0	—	°C	VCC = AVCC0 < 2.4 V*1
		—	±1.0	—	°C	VCC = AVCC0 ≥ 2.4 V*2
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

Note 1. Temperature slope used -3.3 mV/°C
Note 2. Temperature slope calculation points used the evaluated 2 points. Refer to .

2.6 OSC Stop Detect Characteristics

Table 2.55 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.46

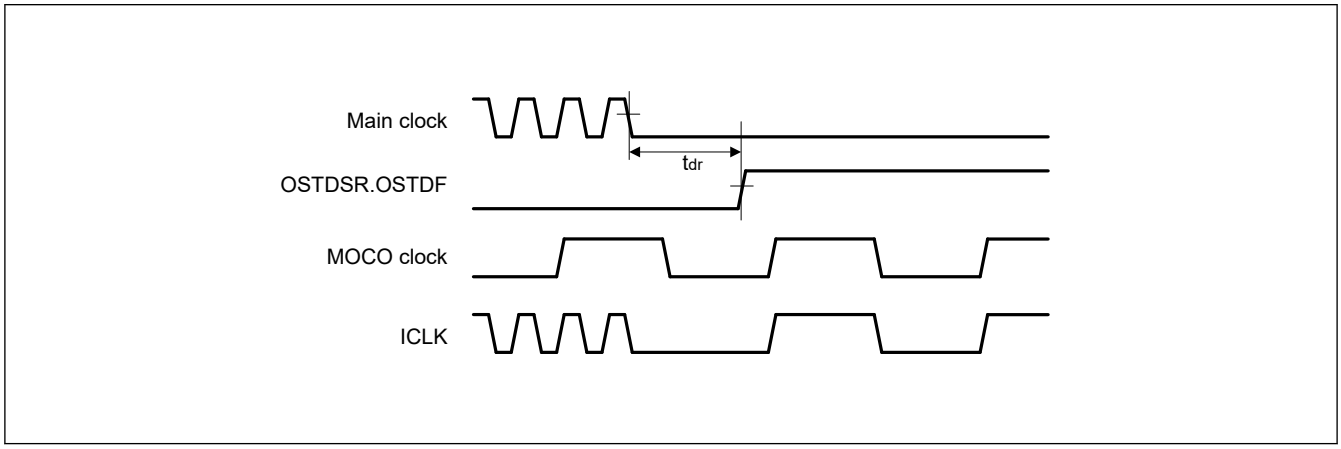


Figure 2.46 Oscillation stop detection timing

2.7 POR and LVD Characteristics

Table 2.56 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.47, Figure 2.48
	When power supply fall	V_{POR}	1.46	1.50	1.54		Figure 2.47
Voltage detection circuit (LVD0)*1	When power supply rise	V_{det0_0}	2.73	2.9	3.01	V	Figure 2.49
	When power supply fall		2.68	2.85	2.96		
	When power supply rise	V_{det0_1}	2.44	2.59	2.70		
	When power supply fall		2.38	2.53	2.64		
	When power supply rise	V_{det0_2}	1.83	1.95	2.07		
	When power supply fall		1.78	1.90	2.02		
	When power supply rise	V_{det0_3}	1.66	1.75	1.88		
	When power supply fall		1.60	1.69	1.82		
Voltage detection circuit (LVD1)*2	When power supply rise	V_{det1_0}	3.05	3.17	3.29	V	Figure 2.50
	When power supply fall		2.98	3.10	3.22		
	When power supply rise	V_{det1_1}	2.95	3.06	3.17		
	When power supply fall		2.89	3.00	3.11		
	When power supply rise	V_{det1_2}	2.86	2.97	3.08		
	When power supply fall		2.79	2.90	3.01		
	When power supply rise	V_{det1_3}	2.74	2.85	2.96		
	When power supply fall		2.68	2.79	2.90		
	When power supply rise	V_{det1_4}	2.63	2.75	2.85		
	When power supply fall		2.58	2.68	2.78		
	When power supply rise	V_{det1_5}	2.54	2.64	2.75		
	When power supply fall		2.48	2.58	2.68		
	When power supply rise	V_{det1_6}	2.43	2.53	2.63		
	When power supply fall		2.38	2.48	2.58		
	When power supply rise	V_{det1_7}	2.16	2.26	2.36		
	When power supply fall		2.10	2.20	2.30		
	When power supply rise	V_{det1_8}	1.88	2	2.09		
	When power supply fall		1.84	1.96	2.05		
	When power supply rise	V_{det1_9}	1.78	1.9	1.99		
	When power supply fall		1.74	1.86	1.95		
	When power supply rise	V_{det1_A}	1.67	1.79	1.88		
	When power supply fall		1.63	1.75	1.84		
	When power supply rise	V_{det1_B}	1.65	1.7	1.78		
	When power supply fall		1.60	1.65	1.73		

Table 2.56 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection circuit (LVD2)*3	When power supply rise	V_{det2_0}	3.06	3.19	3.32	V	Figure 2.51
	When power supply fall		3.00	3.13	3.26		
	When power supply rise	V_{det2_1}	2.86	2.98	3.10		
	When power supply fall		2.80	2.92	3.04		
	When power supply rise	V_{det2_2}	2.66	2.78	2.90		
	When power supply fall		2.60	2.71	2.82		
	When power supply rise	V_{det2_3}	2.46	2.57	2.68		
	When power supply fall		2.40	2.50	2.60		
	When power supply rise	V_{det2_4}	2.26	2.36	2.46		
	When power supply fall		2.20	2.30	2.40		
	When power supply rise	V_{det2_5}	2.06	2.15	2.24		
	When power supply fall		2.00	2.09	2.18		
	When power supply rise	V_{det2_6}	1.86	1.94	2.02		
	When power supply fall		1.80	1.88	1.96		
	When power supply rise	V_{det2_7}	1.66	1.73	1.80		
	When power supply fall		1.60	1.67	1.74		

Note: These characteristics apply when noise is not superimposed on the power supply.
Note 1. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL0[1:0] bits.
Note 2. # in the symbol $V_{det1\_\#}$ denotes the value of the LVD1CMPCR.LVD1LVL[3:0] bits.
Note 3. # in the symbol $V_{det2\_\#}$ denotes the value of the LVD2CMPCR.LVD2LVL[2:0] bits.

Table 2.57 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.9	—	ms	—
	LVD0: disable	t_{POR}	—	4.2	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	0.94	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.25	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.47, Figure 2.48
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.49
LVD1 response delay time*3		t_{det}	—	—	600	µs	Figure 2.50
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.51
Minimum VCC down time	POR	t_{VOFF}	500	—	—	µs	Figure 2.47
	LVD0		300	—	—	µs	Figure 2.49
	LVD1		300	—	—	µs	Figure 2.50
	LVD2		600	—	—	µs	Figure 2.51
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.48, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)		$T_{d\ (E-A)}$	—	—	350	µs	Figure 2.50
LVD2 operation stabilization time (after LVD2 is enabled)		$T_{d\ (E-A)}$	—	—	600	µs	Figure 2.51
Hysteresis width (POR)		V_{PORH}	—	10	—	mV	—

Table 2.57 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	60	—	mV	LVD0 selected
		—	70	—		V_{det1_0} to V_{det1_5} selected
		—	60	—		V_{det1_6} to V_{det1_7} selected
		—	50	—		V_{det1_8} to V_{det1_B} selected
		—	70	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

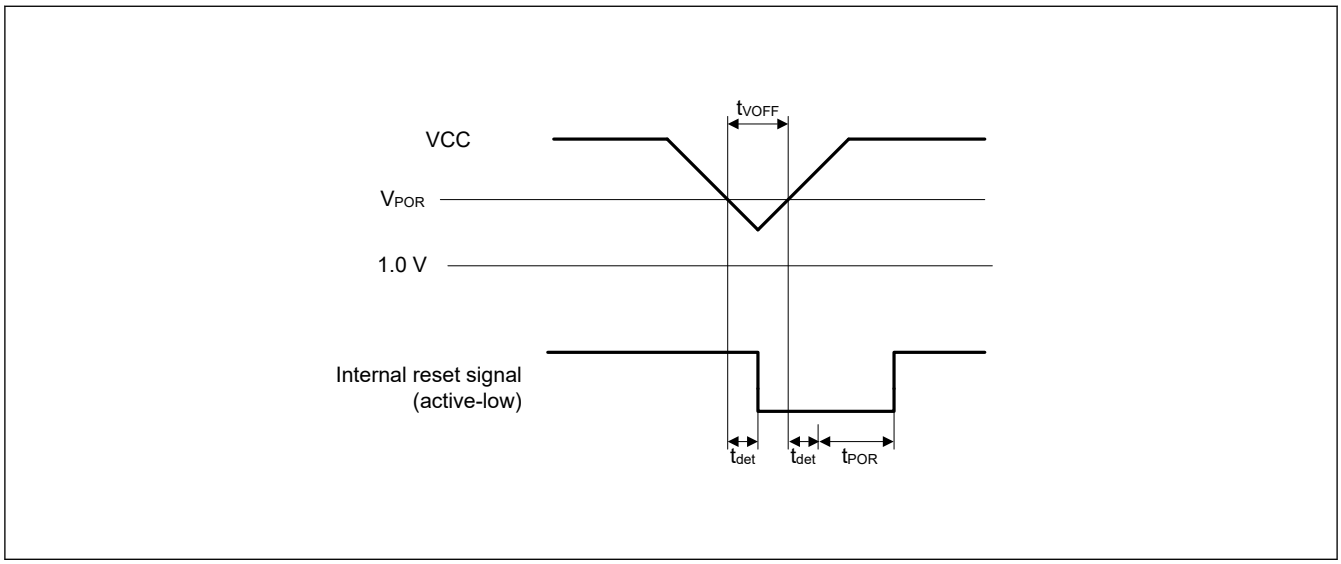
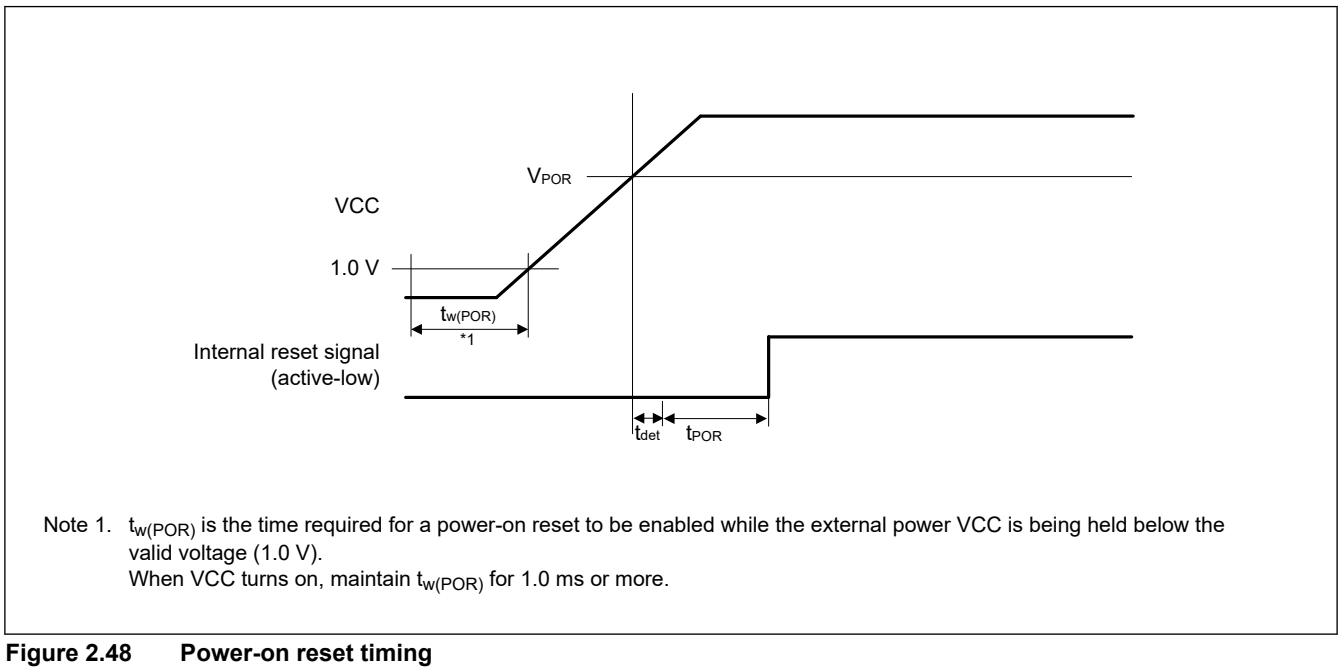


Figure 2.47 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.48 Power-on reset timing

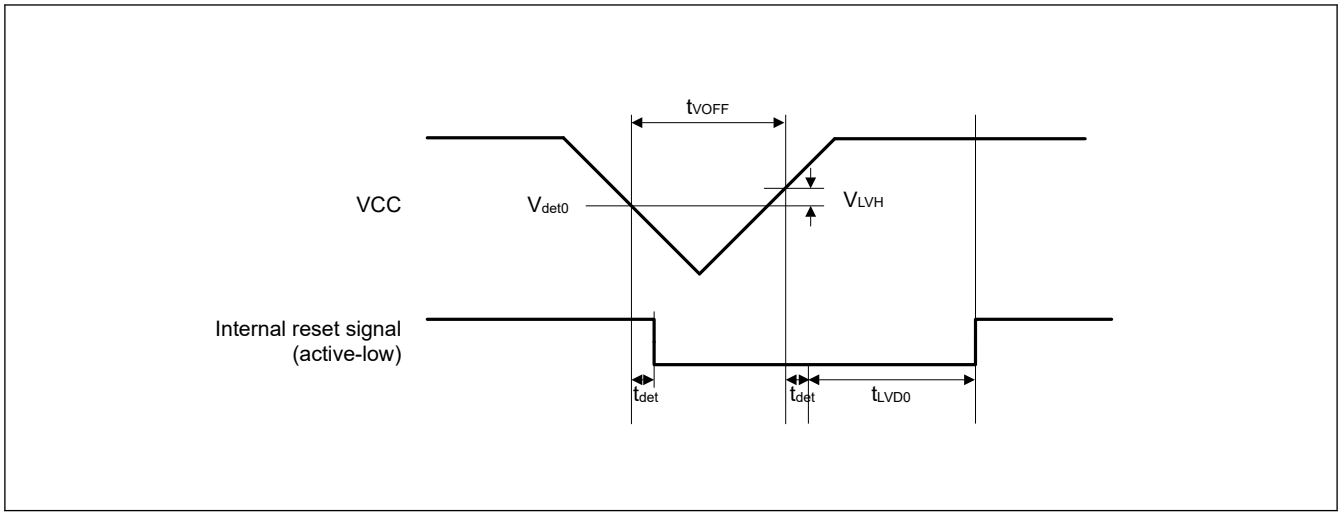


Figure 2.49 Voltage detection circuit timing (V_{det0})

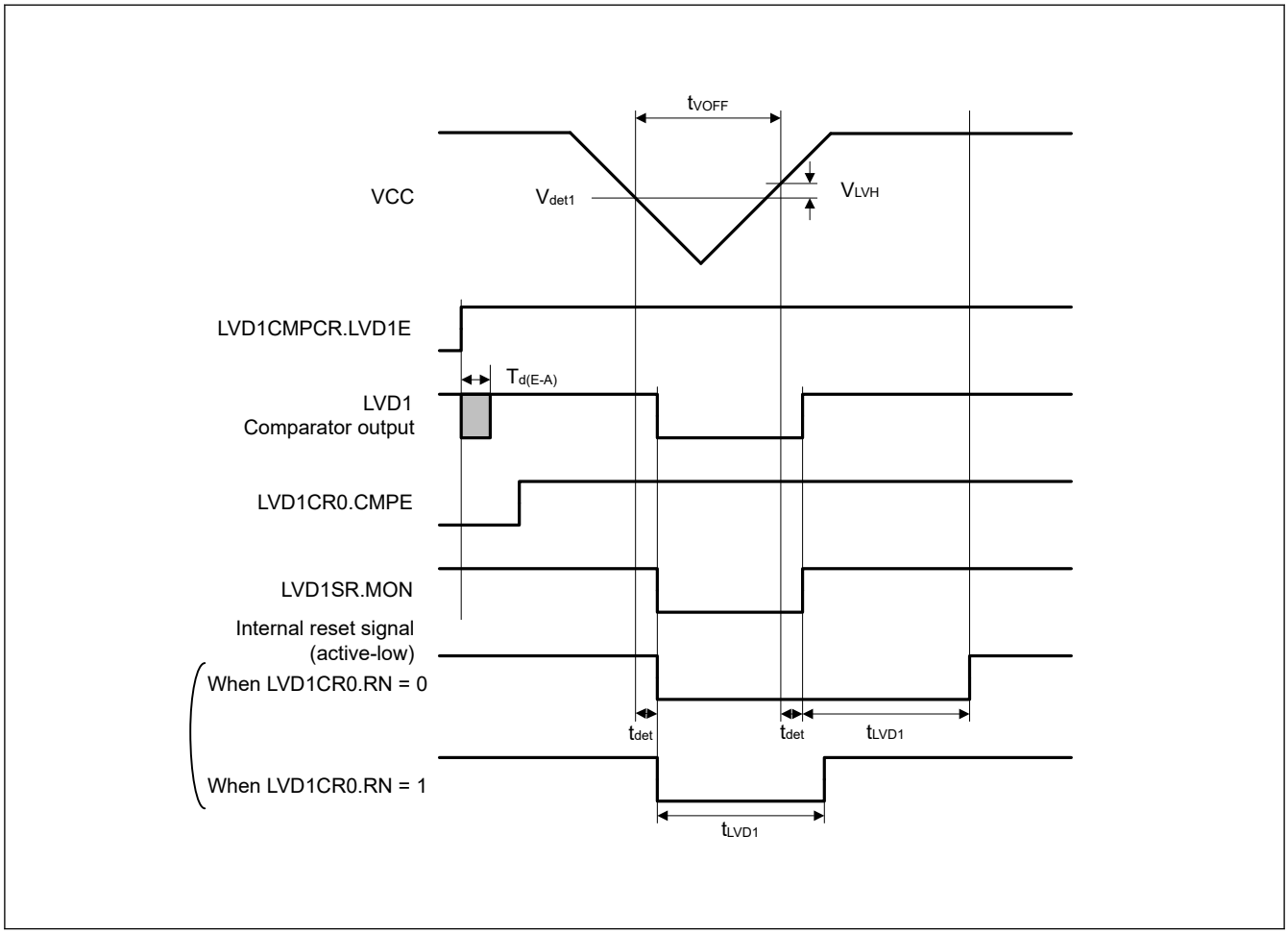


Figure 2.50 Voltage detection circuit timing (V_{det1})

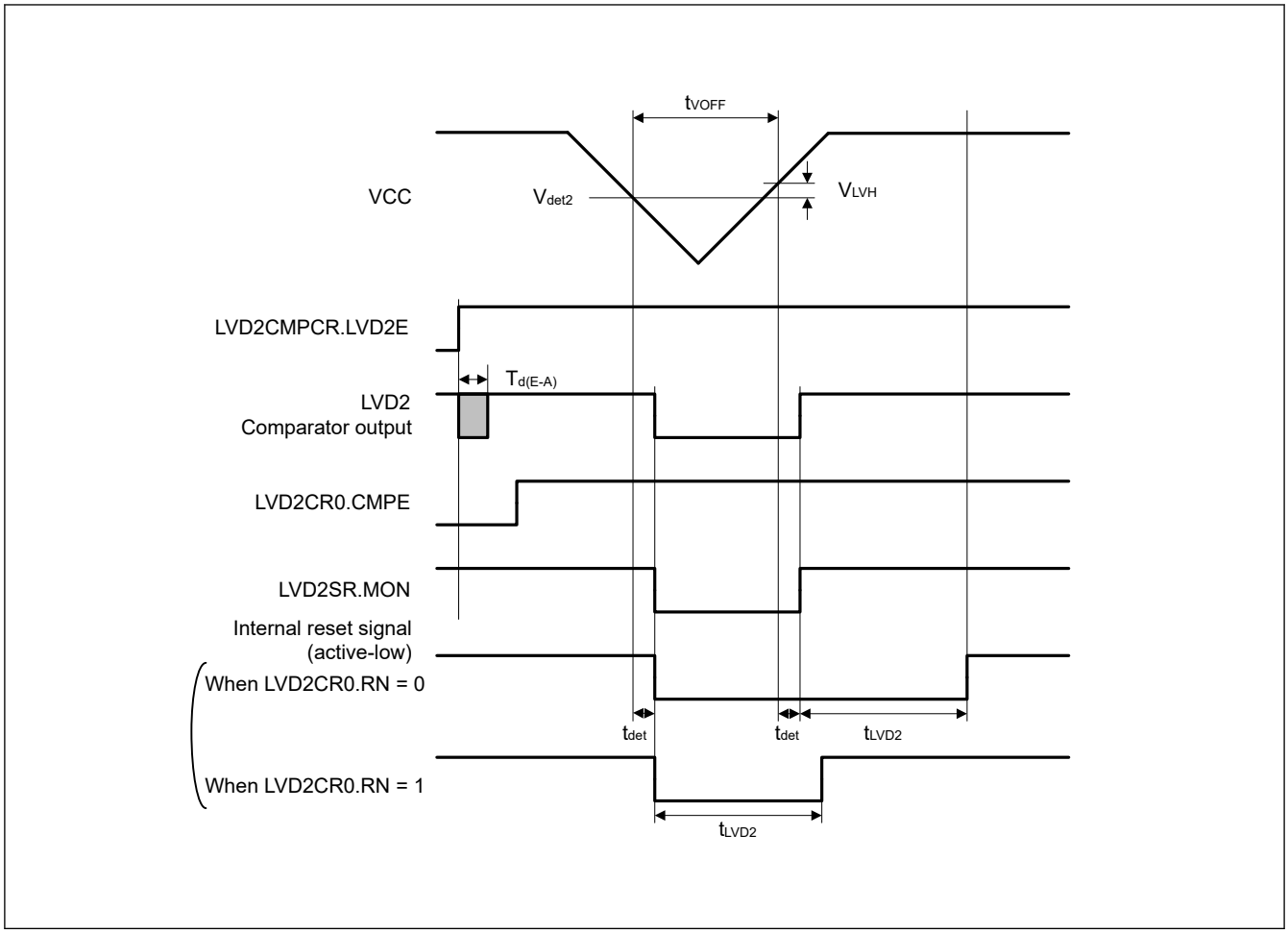


Figure 2.51 Voltage detection circuit timing (V_{det2})

2.8 VRTC POR Characteristics

Table 2.58 Power-on reset circuit of VRTC characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level	Power-on reset of VRTC (VRTC_POR)	When power supply rise	V_{RTCPOR}	1.51	1.55	1.59	V	Figure 2.52
		When power supply fall	V_{RTCPDR}	1.49	1.53	1.57		
Minimum pulse width	$t_{RTCVOFF}$		—	500	—	—	µs	Figure 2.52
Hysteresis width of VRTC (VRTC_POR)			$V_{RTCPORH}$	—	20	—	mV	—
Wait time after power-on reset cancellation			t_{RTCPOR}	—	—	12	ms	Figure 2.52
Power-on reset of VRTC response delay time*1			t_{rtcdet}	—	—	500	µs	Figure 2.52
Power-on reset of VRTC enable time*1			$t_{W\ (VRTC\_POR)}$	1	—	—	ms	Figure 2.52, VRTC = below 1.0 V

Note 1. The minimum VRTC down time indicates the time when VRTC is below the minimum value of the voltage detection level of VRTC_POR.

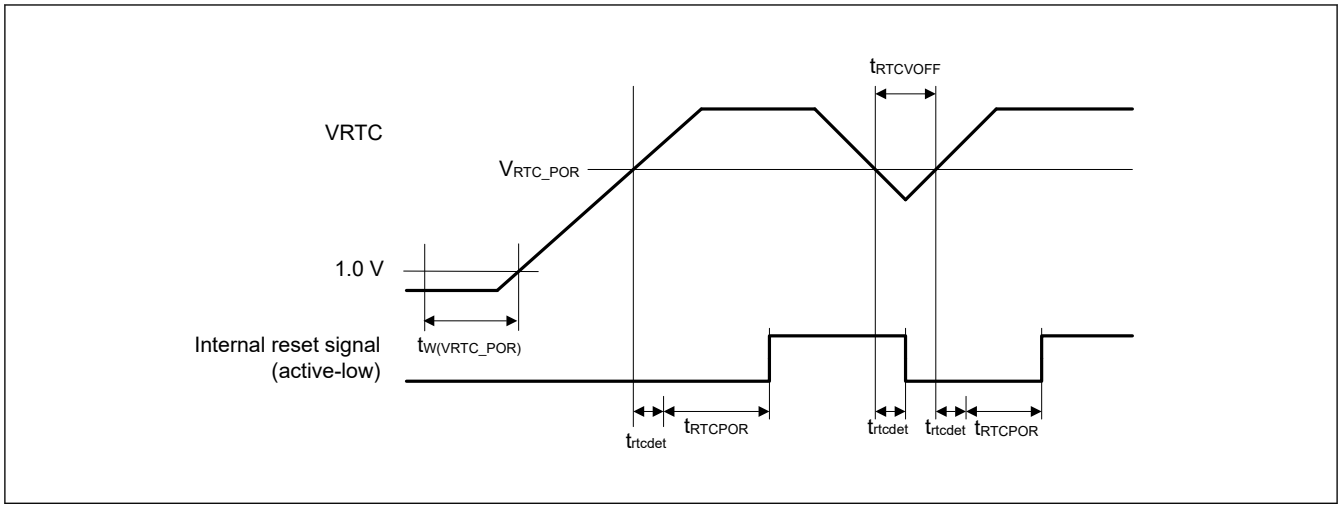


Figure 2.52 Voltage detection reset timing and power-on reset timing of VRTC

2.9 EXLVDVBAT Pin Voltage Detection Characteristics

Table 2.59 EXLVDVBAT pin voltage detection characteristics

Conditions: VCC = AVCC = 1.6 to 3.6 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
Internal reference voltage	$V_{LVDVBAT0}$	Rising	1.61	1.65	1.70	V	—
		Falling	1.55	1.59	1.63		—
	$V_{LVDVBAT1}$	Rising	2.17	2.24	2.31		—
		Falling	2.12	2.18	2.24		—
	$V_{LVDVBAT2}$	Rising	2.37	2.44	2.51		—
		Falling	2.31	2.38	2.45		—
	$V_{LVDVBAT3}$	Rising	2.56	2.64	2.72		—
		Falling	2.50	2.58	2.66		—
	$V_{LVDVBAT4}$	Rising	2.66	2.74	2.82		—
		Falling	2.60	2.68	2.76		—
	$V_{LVDVBAT5}$	Rising	2.76	2.84	2.92		—
		Falling	2.70	2.78	2.86		—
	$V_{LVDVBAT6}$	Rising	3.05	3.14	3.23		—
		Falling	2.99	3.08	3.17		—
Minimum pulse width	$t_{pw\_lvdvbat}$	—	500	—	—	µs	Figure 2.53
Detection delay time	$t_{d\_lvdvbat}$	—	—	—	500	µs	Figure 2.53
Operation stabilization time (after EXLVDVBAT is enabled)	$t_{d(E-A)\_lvdvbat}$	—	—	—	500	µs	Figure 2.53
Setting change stabilization time	$t_{d\_set\_lvdvbat}$	—	—	—	500	µs	—
Pin resistor	$r_{in\_lvdvbat}$	VBTLVDCR.LVDE = 1	80	150	280	MΩ	—

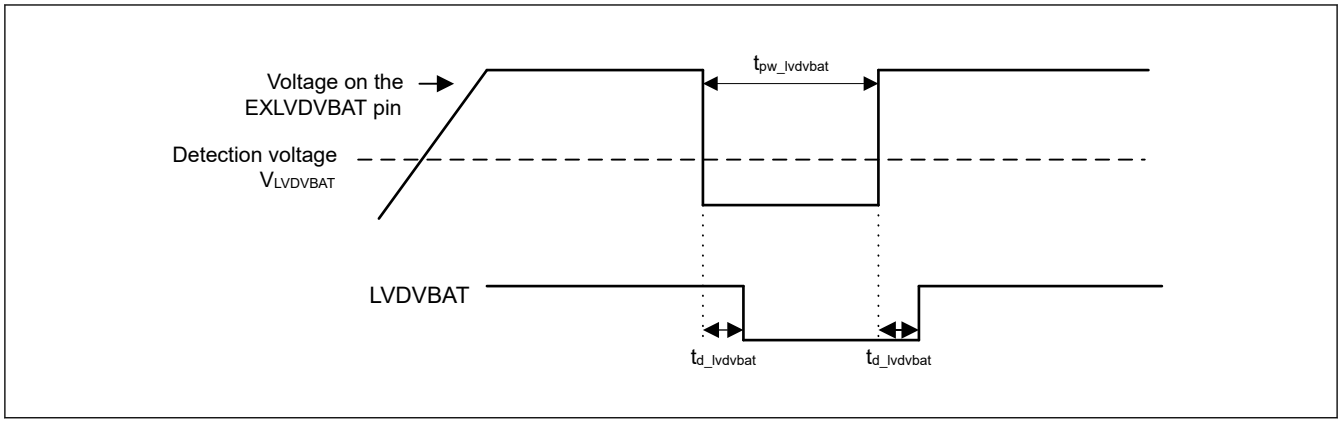


Figure 2.53 EXLVDVBAT pin voltage detection circuit timing

2.10 VRTC Pin Voltage Detection Characteristics

Table 2.60 VRTC pin voltage detection characteristics

Conditions: VCC = AVCC = 1.6 to 3.6 V, VRTC = 1.6 to 3.6 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
Internal reference voltage	$V_{LVDVRTC0}$	Rising	1.61	1.65	1.70	V	—
		Falling	1.55	1.59	1.63		—
	$V_{LVDVRTC1}$	Rising	1.80	1.85	1.90		—
		Falling	1.74	1.79	1.84		—
	$V_{LVDVRTC2}$	Rising	1.99	2.05	2.11		—
		Falling	1.94	1.99	2.05		—
	$V_{LVDVRTC3}$	Rising	2.19	2.25	2.31		—
		Falling	2.13	2.19	2.25		—
	$V_{LVDVRTC4}$	Rising	2.38	2.45	2.52		—
		Falling	2.33	2.39	2.46		—
	$V_{LVDVRTC5}$	Rising	2.58	2.65	2.72		—
		Falling	2.52	2.59	2.66		—
	$V_{LVDVRTC6}$	Rising	2.77	2.85	2.93		—
		Falling	2.71	2.79	2.87		—
	$V_{LVDVRTC7}$	Rising	2.97	3.05	3.13		—
		Falling	2.91	2.99	3.07		—
Minimum pulse width	$t_{pw\_lvdvrtc}$	—	500	—	—	µs	Figure 2.54
Detection delay time	$t_{d\_lvdvrtc}$	—	—	—	500	µs	Figure 2.54
Operation stabilization time (after LVDVRTC is enabled)	$t_{d(E-A)\_lvdvrtc}$	—	—	—	300	µs	Figure 2.54
Setting change stabilization time	$t_{d\_set\_lvdvrtc}$	—	—	—	1	ms	—
Pin resistor	$r_{in\_lvdvrtc}$	VBTLVDCR.LVDE = 1	80	150	280	MΩ	—

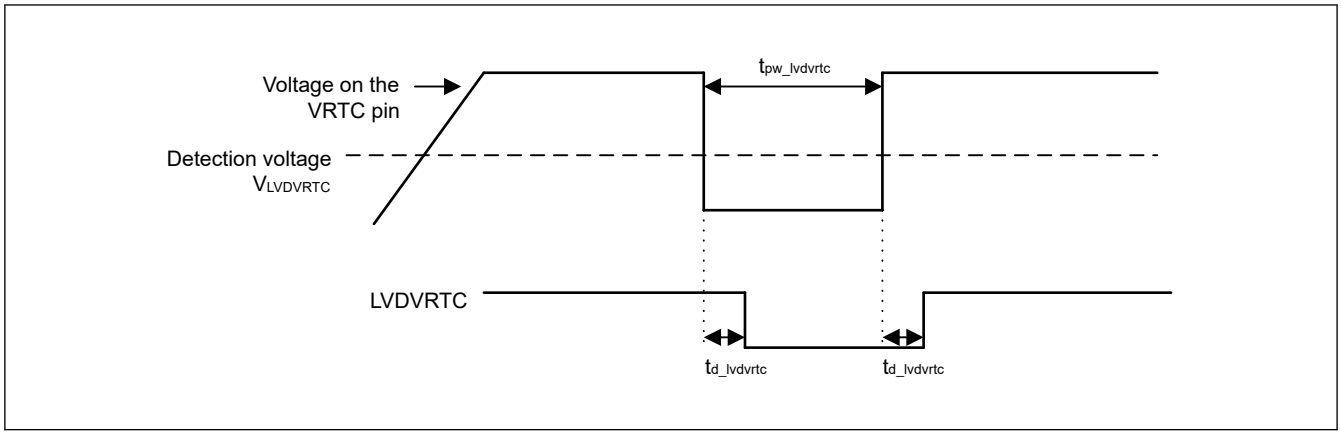


Figure 2.54 VRTC pin voltage detection circuit timing

2.11 EXLVD Pin Voltage Detections

Table 2.61 EXLVD pin voltage detection characteristics

Conditions: VCC = AVCC = 1.6 to 3.6 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
Internal reference voltage	$V_{LVDEXLVD}$	Rising	1.25	1.33	1.41	V	—
		Falling	1.20	1.28	1.36		—
Minimum pulse width	$t_{pw\_lvdexlvd}$	—	500	—	—	µs	Figure 2.55
Detection delay time	t_{d_exlvd}	—	—	—	500	µs	Figure 2.55
Operation stabilization time (after EXLVD is enabled)	$t_{d(E-A)\_exlvd}$	—	—	—	300	µs	Figure 2.55
Pin resistor	r_{in_exlvd}	EXLVDCR.LVDE = 1	30	60	115	MΩ	—

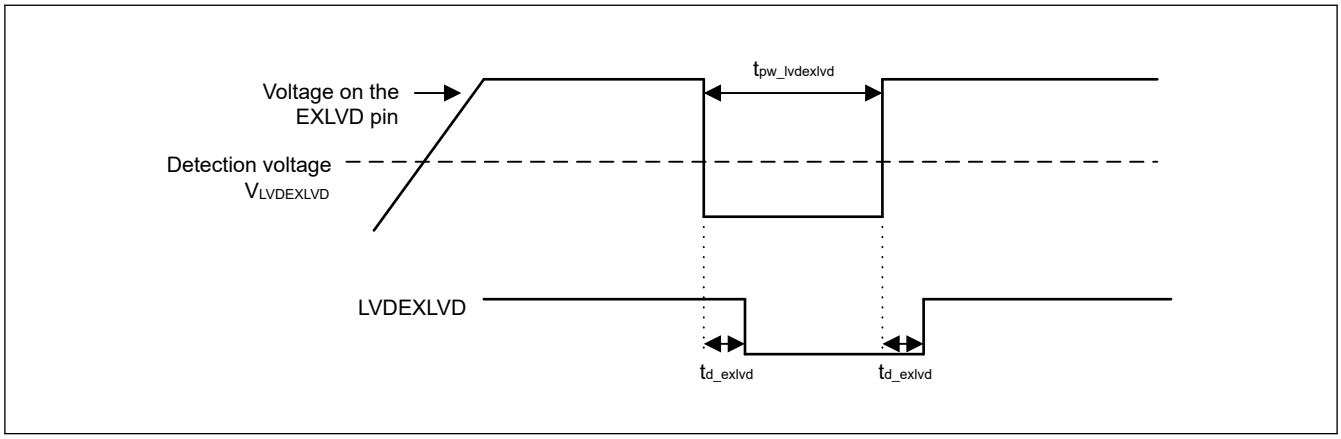


Figure 2.55 EXLVD pin voltage detection circuit timing

2.12 Segment LCD Controller Characteristics

2.12.1 External Resistance Division Method

(1) Static display mode

Table 2.62 External resistance division method LCD characteristics (1)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	—	VCC	V	—

(2) 1/2 bias method, 1/4 bias method

Table 2.63 External resistance division method LCD characteristics (2)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	—	VCC	V	—

(3) 1/3 bias method

Table 2.64 External resistance division method LCD characteristics (3)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	—	VCC	V	—

2.12.2 Internal Voltage Boosting Method (VL1 Reference)

(1) 1/3 bias method

Table 2.65 Internal voltage boosting method LCD characteristics (1)

Conditions: VCC = AVCC = 1.8 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4[*5] = 0.47 µF	VLCD[*1] = 0x04	0.97	1.01	1.04	V	—
			VLCD = 0x05	1.00	1.04	1.08	V	—
			VLCD = 0x06	1.04	1.07	1.11	V	—
			VLCD = 0x07	1.07	1.11	1.14	V	—
			VLCD = 0x08	1.10	1.14	1.18	V	—
			VLCD = 0x09	1.13	1.17	1.21	V	—
			VLCD = 0x0A	1.16	1.21	1.25	V	—
			VLCD = 0x0B	1.20	1.24	1.28	V	—
			VLCD = 0x0C	1.23	1.27	1.32	V	—
			VLCD = 0x0D	1.26	1.31	1.35	V	—
			VLCD = 0x0E	1.29	1.34	1.38	V	—
			VLCD = 0x0F	1.33	1.37	1.42	V	—
			VLCD = 0x10	1.36	1.40	1.45	V	—
			VLCD = 0x11	1.39	1.44	1.49	V	—
			VLCD = 0x12	1.42	1.47	1.52	V	—
			VLCD = 0x13	1.45	1.50	1.55	V	—
			VLCD = 0x14	1.49	1.54	1.59	V	—
			VLCD = 0x15	1.52	1.57	1.62	V	
			VLCD = 0x16	1.55	1.60	1.66	V	—
			VLCD = 0x17	1.58	1.64	1.69	V	—
			VLCD = 0x18	1.61	1.67	1.73	V	—
			VLCD = 0x19	1.65	1.70	1.76	V	—
			VLCD = 0x1A[*4]	1.68	1.74	1.79	V	—
Double output voltage	V_{L2}	C1 to C4[*5] = 0.47 µF		$2 \times V_{L1}$ - 5%	$2 \times V_{L1}$	$2 \times V_{L1}$ + 5%	V	—
Triple output voltage	V_{L4}	C1 to C4[*5] = 0.47 µF		$3 \times V_{L1}$ - 6%	$3 \times V_{L1}$	$3 \times V_{L1}$ + 6%	V	—
Reference voltage setup time[*2]	t_{VL1S}	—		10	—	—	ms	Figure 2.56
Voltage boost wait time[*3]	t_{VLWT}	—		500	—	—	ms	Figure 2.56

Note: 0x0E to 0x1A setting is permitted when using 5V LCD panel, 0x04 to 0x07 setting is permitted when using 3V LCD panel at 1/3 bias.

Note 1. Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL1 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 0) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. This setting is only available when VCC ≥ VL1.

Note 5. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

(2) 1/4 bias method

Table 2.66 Internal voltage boosting method LCD characteristics (2)

Conditions: VCC = AVCC = 1.8 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C5*1 = 0.47 µF	VLCD*2 = 0x04	0.97	1.01	1.04	V	—
			VLCD = 0x05	1.00	1.04	1.08	V	—
			VLCD = 0x06	1.04	1.07	1.11	V	—
			VLCD = 0x07	1.07	1.11	1.14	V	—
			VLCD = 0x08	1.10	1.14	1.18	V	—
			VLCD = 0x09	1.13	1.17	1.21	V	—
			VLCD = 0x0A	1.16	1.21	1.25	V	—
			VLCD = 0x0B	1.20	1.24	1.28	V	—
			VLCD = 0x0C	1.23	1.27	1.32	V	—
			VLCD = 0x0D	1.26	1.31	1.35	V	—
Double output voltage	V_{L2}	C1 to C5*1 = 0.47 µF		2 × V_{L1} - 5%	2 × V_{L1}	2 × V_{L1} + 5%	V	—
Triple output voltage	V_{L3}	C1 to C5*1 = 0.47 µF		3 × V_{L1} - 6%	3 × V_{L1}	3 × V_{L1} + 6%	V	—
Quadruple output voltage	V_{L4}*5	C1 to C5*1 = 0.47 µF		4 × V_{L1} - 6%	4 × V_{L1}	4 × V_{L1} + 6%	V	—
Reference voltage setup time*3	t_{VL1S}	—		10	—	—	ms	Figure 2.56
Voltage boost wait time*4	t_{VLWT}	—		500	—	—	ms	Figure 2.56

Note 1. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL3 and GND

C5: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = C5 = 0.47 µF ±30%

Note 2. Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL1 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 3. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 0) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 5. V_{L4} must be 3.6 V or lower.

2.12.3 Internal Voltage Boosting Method (VL2 Reference)

(1) 1/3 bias method

Table 2.67 Internal voltage boosting method LCD characteristics (3) (1 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
Half output voltage	V_{L1}	C1 to C4*1 = 0.47 µF	1/2 × VL2 - 5%	1/2 × VL2	1/2 × VL2 + 5%	V	—

Table 2.67 Internal voltage boosting method LCD characteristics (3) (2 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L2}	C1 to C4[*1] = 0.47 µF	VLCD[*2] = 0x84	1.94	2.02	2.11	V	—
			VLCD = 0x85	2.00	2.09	2.18	V	—
			VLCD = 0x86	2.07	2.16	2.25	V	—
			VLCD = 0x87	2.13	2.22	2.32	V	—
			VLCD = 0x88	2.19	2.29	2.39	V	—
			VLCD = 0x89	2.26	2.36	2.46	V	—
			VLCD = 0x8A	2.32	2.42	2.53	V	—
			VLCD = 0x8B	2.39	2.49	2.59	V	—
			VLCD = 0x8C	2.45	2.56	2.66	V	—
			VLCD = 0x8D	2.51	2.62	2.73	V	—
			VLCD = 0x8E	2.58	2.69	2.80	V	—
			VLCD = 0x8F	2.64	2.76	2.87	V	—
			VLCD = 0x90	2.70	2.82	2.94	V	—
			VLCD = 0x91	2.77	2.89	3.01	V	—
			VLCD = 0x92	2.83	2.96	3.08	V	—
			VLCD = 0x93	2.90	3.02	3.15	V	—
			VLCD = 0x94	2.96	3.09	3.22	V	—
			VLCD = 0x95	3.02	3.15	3.29	V	—
			VLCD = 0x96	3.09	3.22	3.35	V	—
			VLCD = 0x97	3.15	3.29	3.42	V	—
			VLCD = 0x98	3.21	3.35	3.49	V	—
			VLCD = 0x99	3.28	3.42	3.56	V	—
			VLCD = 0x9A	3.34	3.49	3.63	V	—
Two-thirds output voltage	V_{L4}[*5]	C1 to C4[*1] = 0.47 µF		2/3 × V_{L2} - 6%	2/3 × V_{L2}	2/3 × V_{L2} + 6%	V	—
Reference voltage setup time[*3]	t_{VL2S}	—		10	—	—	ms	Figure 2.56
Voltage boost wait time[*4]	t_{VLWT}	—		500	—	—	ms	Figure 2.56

Note: 0x8E to 0x9A setting is permitted when using 5V LCD panel, 0x84 to 0x87 setting is permitted when using 3V LCD panel at 1/3 bias.

Note 1. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 2. Bit [7] (MDSET[2]) of register VLCD is set to 1 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL2 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 3. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 1) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 5. V_{L4} must be 3.6 V or lower.

2.12.4 Capacitor Split Method (VCC Reference)

(1) 1/3 bias method

Table 2.68 Capacitor split method LCD characteristics (1)

Conditions: VCC = AVCC = 2.2 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage	V_{L4}	C1 to C4*2 = 0.47 µF	—	VCC	—	V	—
VL2 voltage	V_{L2}	C1 to C4*2 = 0.47 µF	2 / 3 × V_{L4} - 3%	2 / 3 × V_{L4}	2 / 3 × V_{L4} + 3%	V	—
VL1 voltage	V_{L1}	C1 to C4*2 = 0.47 µF	1 / 3 × V_{L4} - 3%	1 / 3 × V_{L4}	1 / 3 × V_{L4} + 3%	V	—
Capacitor split wait time*1	t_{WAIT}	—	100	—	—	ms	Figure 2.56

Note: Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 10 for capacitor split method (VCC reference).
Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

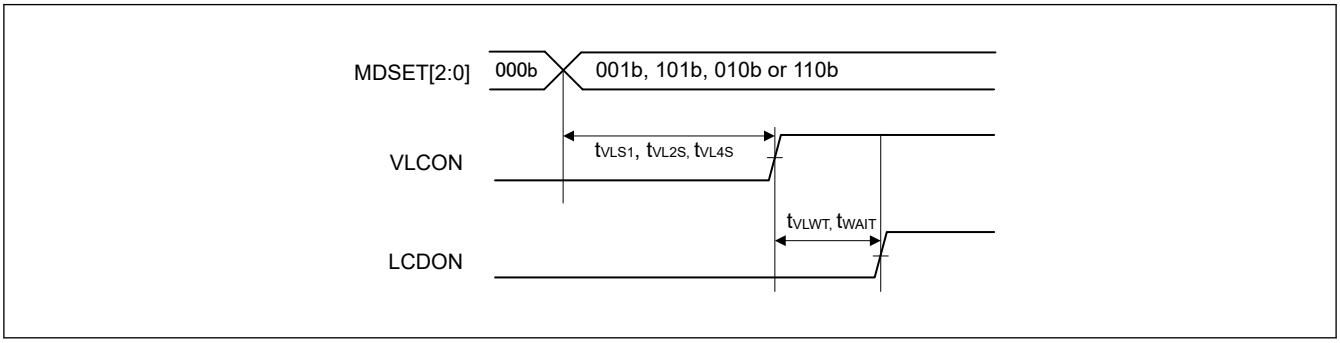


Figure 2.56 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time

2.12.5 Capacitor Split Method (VL4 Reference)

(1) 1/3 bias method

Table 2.69 Capacitor split method LCD characteristics (3)

Conditions: VCC = AVCC = 3.2 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage	V_{L4}	C1 to C4*2 = 0.47 µF	2.89	3.04	3.20	V	—
VL2 voltage	V_{L2}	C1 to C4*2 = 0.47 µF	1.89	2.03	2.17	V	—
VL1 voltage	V_{L1}	C1 to C4*2 = 0.47 µF	0.94	1.01	1.08	V	—
Reference voltage setup time*3	t_{VL4S}	—	10	—	—	ms	Figure 2.56
Capacitor split wait time*1	t_{WAIT}	—	100	—	—	ms	Figure 2.56

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 3. Bit [7] (MDSET[2]) of register VLCD is set to 1 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 10 for capacitor split method (VL4 reference).

2.13 Flash Memory Characteristics

2.13.1 Code Flash Memory Characteristics

Table 2.70 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +85 °C T_a = +105 °C
			10	—	—	Year	T_a = +125 °C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.71 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	—	128	1064	—	44.2	420	µs
Erasure time	2-KB	t_{E2K}	—	14.1	390	—	5.5	214	ms
Blank check time	8-byte	t_{BC8}	—	—	67.7	—	—	8.6	µs
	2-KB	t_{BC2K}	—	—	7538	—	—	272	µs
Erase suspended time		t_{SED}	—	—	33.4	—	—	10.7	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	10.7	µs
Configuration Set time		t_{CFGS}	—	27	494	—	11	255	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.

Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.72 Code flash characteristics (3) (1 of 2)

Middle-speed operating mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	—	128	1064	—	50.6	468	µs
Erasure time	2-KB	t_{E2K}	—	14.1	390	—	6.32	231	ms

Table 2.72 Code flash characteristics (3) (2 of 2)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Blank check time	8-byte	t_{BC8}	—	—	67.7	—	—	13.3	µs
	2-KB	t_{BC2K}	—	—	7538	—	—	947	µs
Erase suspended time		t_{SED}	—	—	33.4	—	—	13.1	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	13.1	µs
Configuration Set time		t_{CFGS}	—	27	494	—	12	277	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 3.6 V

Table 2.73 Code flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	8-byte	t_{P8}	—	128	1064	µs
Erasure time	2-KB	t_{E2K}	—	14.1	390	ms
Blank check time	8-byte	t_{BC8}	—	—	67.7	µs
	2-KB	t_{BC2K}	—	—	7538	µs
Erase suspended time		t_{SED}	—	—	33.4	µs
Forced stop time		t_{FD}	—	—	33.4	µs
Configuration Set time		t_{CFGS}	—	27	494	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.13.2 Data Flash Memory Characteristics

Table 2.74 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2 *3	—	—	Year	Ta = +85 °C
			10*2 *3	—	—		Ta = +105 °C
	After 100000 times of N_{DPEC}		5*2 *3	—	—		Ta = +105 °C
	After 1000000 times of N_{DPEC}		—	1*2 *3	—		Ta = +25 °C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 256 times for different

addresses in 256-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.75 Data flash characteristics (2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	112	903	—	33.9	317	µs
Erasure time	256-byte	t_{DE256}	—	14.1	390	—	5.50	214	ms
Blank check time	1-byte	t_{DBC1}	—	—	67.7	—	—	8.6	µs
	256-byte	t_{DBC256}	—	—	7538	—	—	272	µs
Suspended time during erasing		t_{DSED}	—	—	33.4	—	—	10.7	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	10.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.

Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.76 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	112	903	—	39.7	359	µs
Erasure time	256-byte	t_{DE256}	—	14.1	390	—	6.32	231	ms
Blank check time	1-byte	t_{DBC1}	—	—	67.7	—	—	13.3	µs
	256-byte	t_{DBC256}	—	—	7538	—	—	947	µs
Suspended time during erasing		t_{DSED}	—	—	33.4	—	—	13.1	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	13.1	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.

Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 3.6 V

Table 2.77 Data flash characteristics (4) (1 of 2)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	112	903	µs
Erasure time	256-byte	t_{DE256}	—	14.1	390	ms
Blank check time	1-byte	t_{DBC1}	—	—	67.7	µs
	256-byte	t_{DBC256}	—	—	7538	µs
Suspended time during erasing		t_{DSED}	—	—	33.4	µs
Forced stop time		t_{FD}	—	—	33.4	µs

Table 2.77 Data flash characteristics (4) (2 of 2)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter	Symbol	ICLK = 1 MHz			Unit
		Min	Typ	Max	
Data flash STOP recovery time	t_{DSTOP}	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.13.3 Serial Wire Debug (SWD)

Table 2.78 SWD characteristics (1)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	50	—	—	ns	Figure 2.57
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	3	—	—	ns	Figure 2.58
SWDIO hold time	t_{SWDH}	13	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	45	ns	

Table 2.79 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.57
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.58
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

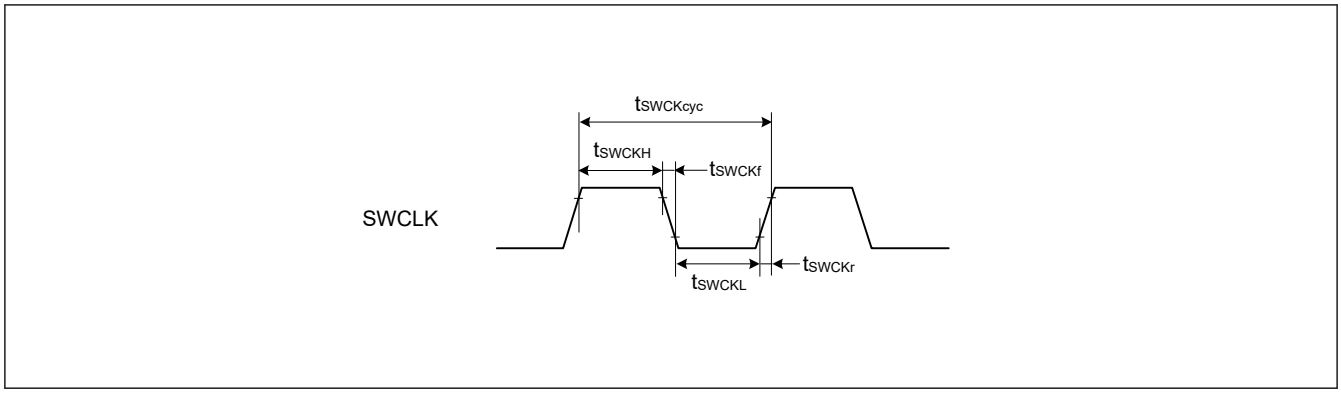


Figure 2.57 SWD SWCLK timing

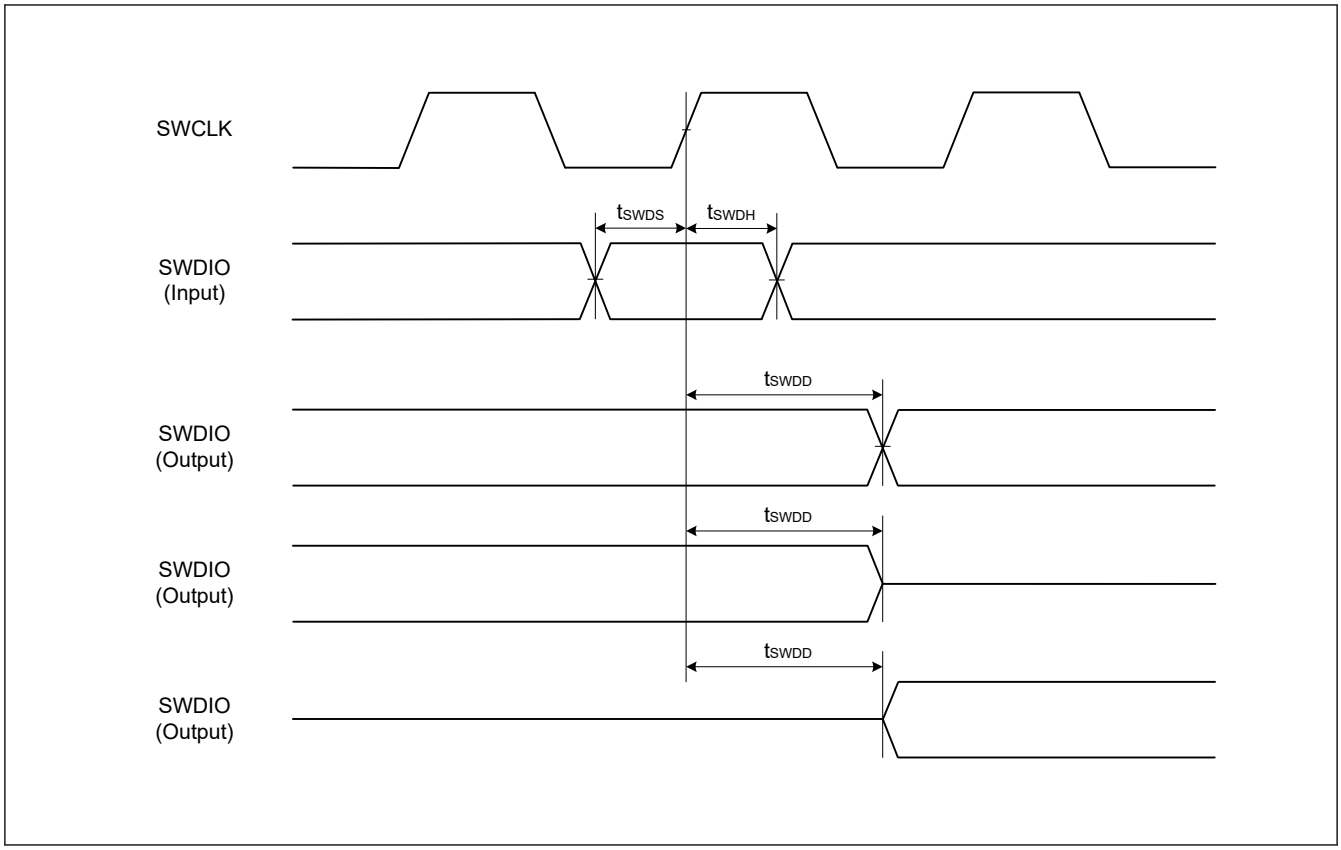


Figure 2.58 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode
Mode	MD	Pull-up	Keep-O
IRQ	IRQx	Hi-Z	Keep-O*1
AGT	AGTIOn	Hi-Z	AGTIOn input
	AGTOn/AGTOAn/AGTOBn	Hi-Z	AGTOn/AGTOAn/AGTOBn output
SCI	RXD0	Hi-Z	Keep-O*1
IIC	SCLn/SDAn	Hi-Z	Keep-O*1
UARTA	CLKAn	Hi-Z	CLKAn output
	RxDAn	Hi-Z	RxDAn input
RTC	RTCIC0	Hi-Z	RTCIC0 input
	RTCOUT	Hi-Z	RTCOUT output
CLKOUT	CLKOUT	Hi-Z	CLKOUT output
SLCDC	SEGx/COMx	Hi-Z	SEGx/COMx output
	VLx/CAPH/CAPL	Hi-Z	VLx/CAPH/CAPL input
Others	—	Hi-Z	Keep-O

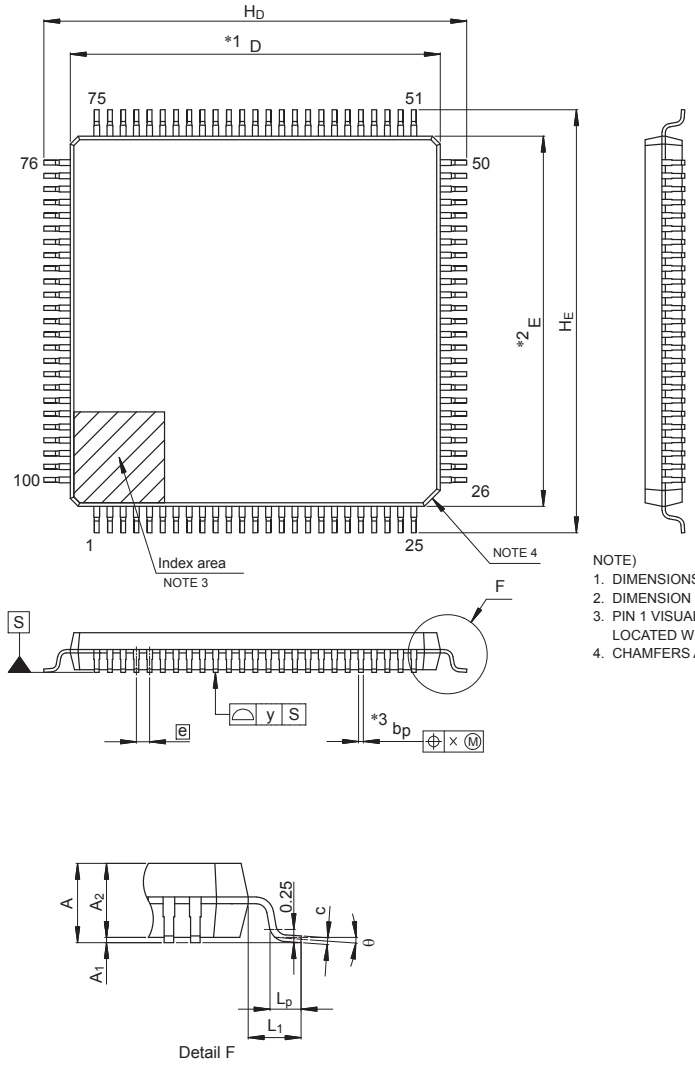
Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Note 1. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



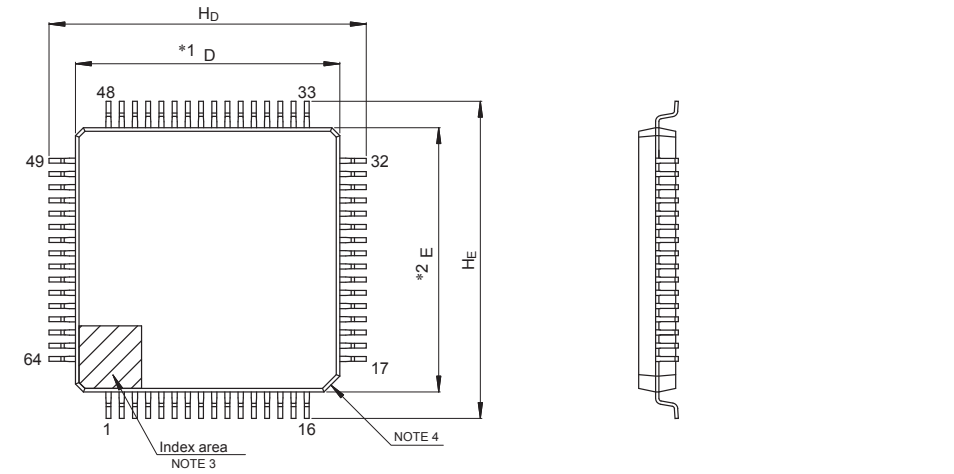
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

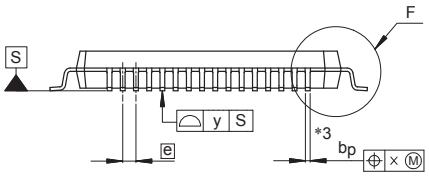
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

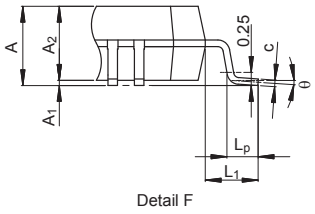
Figure A2.1 LQFP 100-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A2.2 LQFP 64-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Master Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	Special Function Register	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x4001_B000
FCACHE	Flash Cache	0x4001_C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4001_F000
PORT1	Port 1 Control Registers	0x4001_F020
PORT2	Port 2 Control Registers	0x4001_F040
PORT3	Port 3 Control Registers	0x4001_F060
PORT4	Port 4 Control Registers	0x4001_F080
PORT5	Port 5 Control Registers	0x4001_F0A0
PORT6	Port 6 Control Registers	0x4001_F0C0
PORT7	Port 7 Control Registers	0x4001_F0E0
PORT8	Port 8 Control Registers	0x4001_F100
PFS	Pmn Pin Function Control Register	0x4001_F800
ELC	Event Link Controller	0x4008_2000
RTC	Realtime Clock	0x4008_3000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600

Table A3.1 Peripheral base address (2 of 2)

Name	Description	Base address
MSTP	Module Stop Control A, B, C, D, E	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000
UARTA	Serial Interface UARTA	0x4009_7000
IIC0	Inter-Integrated Circuit 0	0x4009_F000
IIC1	Inter-Integrated Circuit 1	0x4009_F100
CANFD	CANFD Module	0x400B_0000
SLCDC	Segment LCD Controller/Driver	0x400D_4000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI1	Serial Communication Interface 1	0x4011_8100
SCI3	Serial Communication Interface 3	0x4011_8300
SCI4	Serial Communication Interface 4	0x4011_8400
SCI5	Serial Communication Interface 5	0x4011_8500
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000
SPI1	Serial Peripheral Interface 1	0x4011_A100
SPI2	Serial Peripheral Interface 2	0x4011_A200
ECCMB	Error correction circuit for MBRAM	0x4012_F000
GPT320	General PWM 32-Bit Timer 0	0x4016_9000
GPT321	General PWM 32-Bit Timer 1	0x4016_9100
GPT162	General PWM 16-Bit Timer 2	0x4016_9200
GPT163	General PWM 16-Bit Timer 3	0x4016_9300
GPT164	General PWM 16-Bit Timer 4	0x4016_9400
GPT165	General PWM 16-Bit Timer 5	0x4016_9500
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
FLCN	Flash I/O Registers	0x407E_C000
FACI	Flash Application Command Interface	0x407F_E000
QSPI	Quad-SPI	0x6400_0000
CPU_OCD	On-Chip Debug	0x8000_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.

- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table A3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	4	5	4	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E5FF	6	5	6	5	ICLK	System Control
PORTn, PFS	0x4001_F000	0x4001_FFFF	5*2	4	5*2	4	ICLK	Port n Control Registers, Pmn Pin Function Control Register
ELC, RTC, IWDT, WDT, CAC, MSTP, POEG	0x4008_2000	0x4008_AFFF	5	4	2 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control, Port Output Enable Module for GPT
UARTA	0x4009_7000	0x4009_7FFF	4	3	1 to 4	1 to 3	PCLKB	Serial Interface UARTA
IICn, IIC0WU, CANFD	0x4009_D000	0x400D_0FFF	5	4	2 to 5	2 to 4	PCLKB	Serial Sound Interface Enhanced, Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit, CANFD Module
SLCDC	0x400D_4000	0x400D_4FFF	4	3	1 to 4	1 to 3	PCLKB	Segment LCD Controller/Driver
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	4 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n

Table A3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*4	4*4	2 to 5*4	2 to 4*4	PCLKA	Serial Peripheral Interface n
ECCMB	0x4011_F000	0x4012_FFFF	5	4	2 to 5	2 to 4	PCLKA	Error correction circuit for MBRAM
GPT32n, GPT16n, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC120	0x4017_0000	0x4017_1FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter 0
QSPI	0x6400_0000	0x6400_000F	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0010	0x6400_0013	25 to *5	6 to *5	25 to *5	5 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	4	3	1 to 4	1 to 3	PCLKA	Quad-SPI

Table A3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = FCLK		ICLK > FCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
FLCN, FACI	0x407E_C000	0x407F_EFFF	5	4	3 to 5	2 to 4	FCLK	Flash I/O Registers, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.
Note 2. The access cycles of the PRCNT2 and PFS registers depend on PRWCNTR.
Note 3. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table A3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table A3.2.
Note 4. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table A3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table A3.2.
Note 5. The access cycles depend on the QSPI bus cycles.

Revision History

Revision 1.00 — May 28, 2025

Initial release

Revision 1.10 — Jul 4, 2025

2. Electrical Characteristics:

- Updated Table 2.20 Thermal resistance
- Added 2.2.8.1 Calculation Guide of ICCmax.
- Updated Table 2.54 TSN characteristics.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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