RA4L1 Group
Renesas Microcontrollers

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The RA4L1 group features low power, 32-bit microcontrollers (MCUs) based on the Arm® Cortex®-M33 (CM33) core with TrustZone®, delivering an ideal balance of low voltage operation, low power consumption, and high performance. The RA4L1 offers operation down to 1.6V combined with a low power standby current of as little as 1.65µA and a multitude of low power features enabling the user to dynamically optimize power/performance to their application requirements.

Features

Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 80 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

Memory

- Up to 512-KB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 64-KB SRAM

Connectivity

- Serial Communications Interface (SCI) × 6
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Simple LIN (SCI1)
  - Manchester coding (SCI3, SCI4)
- IrDA interface (IrDA)
- I^2C bus interface (IIC)
- I3C bus interface (I3C)
- Serial Interface UARTA (UARTA) × 2
- Serial Peripheral Interface (SPI)
- Quad Serial Peripheral Interface (QSPI)
- USB 2.0 Full-Speed Module (USBFS)
- CAN with Flexible Data-rate (CANFD)
- Serial Sound Interface Enhanced (SSIE)

Analog

- 12-bit A/D Converter (ADC12)
- 12-bit D/A Converter (DAC12)
- Low-Power Analog Comparator (ACMPLP) × 2
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) × 2
- General PWM Timer 16-bit (GPT16) × 4
- Low Power Asynchronous General Purpose Timer (AGT) × 2

Security and Encryption

- Renesas Secure IP (RSIP-E11A)
  - Symmetric algorithms: AES
  - Asymmetric algorithms: ECC
  - Hash-value generation: SHA224, SHA256
  - 128-bit unique ID
- Arm® TrustZone®
  - Up to three or six regions for the code flash, depending on the bank mode
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- Device lifecycle management
- Pin function
  - Up to three tamper pins
  - Secure pin multiplexing

System and Power Management

- Low power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

Human Machine Interface (HMI)

- Capacitive Touch Sensing Unit (CTSU)
- Segment LCD Controller (SLCDC)

Multiple Clock Sources

- Main clock oscillator (MOSC) (1 to 20 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (48/64/80 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- Clock out support

General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up

Operating Voltage

- VCC: 1.6 to 3.6 V

Operating Temperature and Packages

- Ta = -40 °C to +125 °C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 100-pin BGA (7 mm × 7 mm, 0.5 mm pitch)
  - 64-pin BGA (5.5 mm × 5.5 mm, 0.65 mm pitch)
  - 72-pin WLCSP (3.64 mm × 4.28 mm, 0.4 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 80 MHz with the following features:

- Up to 512 KB code flash memory
- 64 KB SRAM
- Quad Serial Peripheral Interface (QSPI)
- USBFS
- Capacitive Touch Sensing Unit (CTSU)
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 80 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel1 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB of code flash memory.
Data flash memory	8 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/USB/SWD boot mode
Resets	The MCU provides 13 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC and EXLVD pins. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC and to the EXLVD pins for LVD2. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.

Table 1.3 System (2 of 2)

Feature	Functional description
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL • Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External bus	• QSPI area (EQBIU): Connected to the QSPI (external device interface)

Table 1.7 Timers (1 of 2)

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 2 channels and a 16-bit timer with GPT16 × 4 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state.
Low Power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.

Table 1.7 Timers (2 of 2)

Feature	Functional description
Realtime Clock (RTC)	The Realtime Clock (RTC) has two operation modes, normal operation mode and low-consumption clock mode. In each of the operation mode, the RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 6 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface ● Simple LIN The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 3 to 5, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
IrDA Interface	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI5 based on the IrDA (Infrared Data Association) standard 1.0.
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has one channel. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
I3C bus interface (I3C)	The I3C bus interface (I3C) has one channel. The I3C module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Interface UARTA (UARTA)	The serial interface UARTA (UARTA) has two channels. The UARTA supports the following modes: ● Operation stop mode ● UART mode
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has one channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network with Flexible Data-Rate Module (CAN-FD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 16 receive buffers.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system.

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I^2S/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 40 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission.

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter (ADC12) is provided. Analog input channels are selectable up to 16. The temperature sensor output and an internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage with an analog input voltage. Comparator channels ACMPLP0 and ACMPLP1 are independent of each other. The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin or from the internal reference voltage (V_{REF}) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption.

Table 1.10 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical conductor so that a finger does not come into direct contact with the electrode.
Segment LCD Controller (SLCDC)	The SLCDC provides the following functions: ● Internal voltage boosting method, capacitor split method, and external resistance division method are switchable ● VL1 or VL2 reference mode is selectable under internal voltage boosting method ● VCC or VL4 reference mode is selectable under capacitor split method ● Segment signal output: 52 (48) ● Common signal output: 4 (8) ● Waveform A or B selectable ● The LCD can be made to blink Note: The values in parentheses are the number of signal outputs when 8 com is used.

Table 1.11 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 32-bit data. When a selected condition applies, 32-bit data is compared and an interrupt can be generated.

Table 1.12 Security

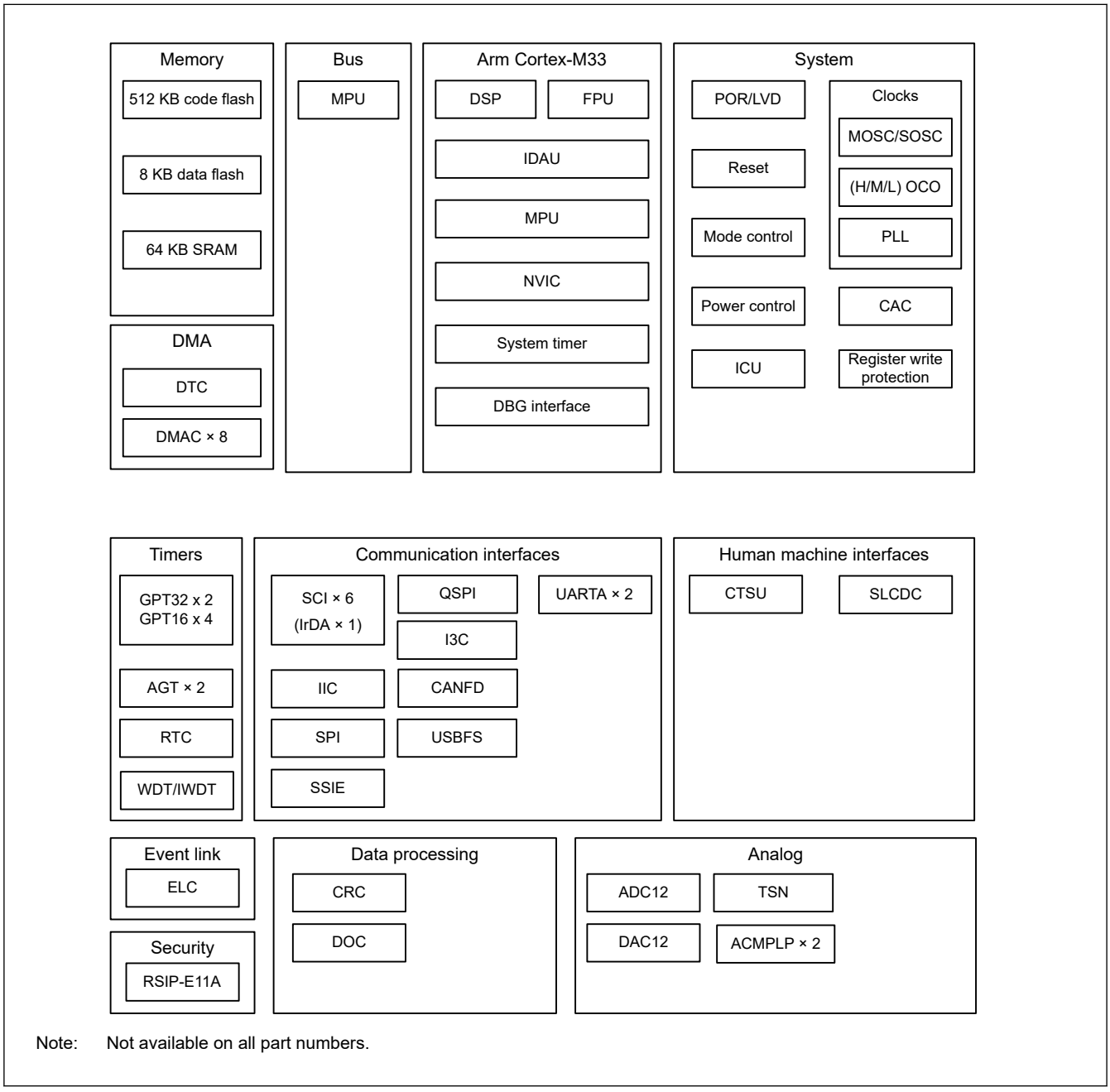
Feature	Functional description
Security function	• ARMv8-M TrustZone security • Device lifecycle management • Debug access level • Key injection • Secure pin multiplexing
Renesas Secure IP (RSIP-E11A)	• Symmetric algorithms: AES • Asymmetric algorithms: ECC • Hash value generation: SHA224, SHA256 • True random number generator • 128-bit unique ID.

Table 1.13 I/O ports

Feature	Functional description
Programmable I/O ports	• I/O ports for the 100-pin LQFP, 100-pin BGA – I/O pins: 82 – Input pins: 3 – Pull-up resistors: 82 – N-ch open-drain outputs: 75 – 5-V tolerance: 5 • I/O ports for the 72-pin WLCSP – I/O pins: 53 – Input pins: 3 – Pull-up resistors: 53 – N-ch open-drain outputs: 46 – 5-V tolerance: 5 • I/O ports for the 64-pin LQFP – I/O pins: 48 – Input pins: 3 – Pull-up resistors: 48 – N-ch open-drain outputs: 41 – 5-V tolerance: 5 • I/O ports for the 64-pin BGA – I/O pins: 52 – Input pins: 3 – Pull-up resistors: 52 – N-ch open-drain outputs: 45 – 5-V tolerance: 5 • I/O ports for the 48-pin LQFP, 48-pin QFN – I/O pins: 34 – Input pins: 3 – Pull-up resistors: 34 – N-ch open-drain outputs: 29 – 5-V tolerance: 5

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

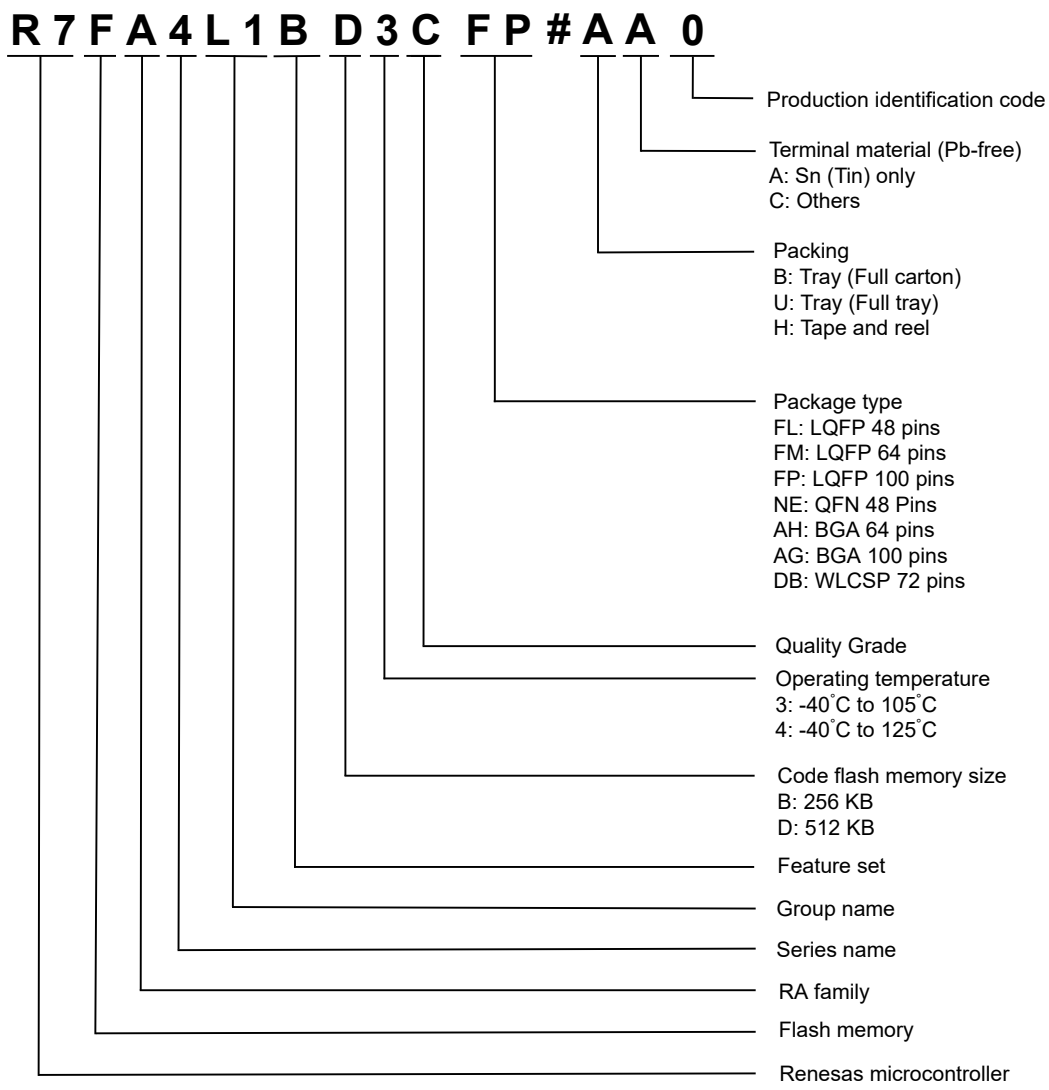


Note: Not available on all part numbers.

Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.14 shows a list of products.



Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.14 Product list (1 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA4L1BD4CFP	PLQP0100KB-B	512 KB	8 KB	64 KB	-40 to +125 °C
R7FA4L1BD4CFM	PLQP0064KB-C				
R7FA4L1BD4CFL	PLQP0048KB-B				
R7FA4L1BD4CNE	PWQN0048KC-A				
R7FA4L1BD3CAG	PLBG0100KB-A				-40 to +105 °C
R7FA4L1BD3CAH	PLBG0064JD-A				
R7FA4L1BD4CDB	SUBG0072LB-A				-40 to +125 °C

Table 1.14 Product list (2 of 2)

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA4L1BB4CFP	PLQP0100KB-B	256 KB	8 KB	64 KB	-40 to +125 °C
R7FA4L1BB4CFM	PLQP0064KB-C				
R7FA4L1BB4CFL	PLQP0048KB-B				
R7FA4L1BB4CNE	PWQN0048KC-A				
R7FA4L1BB3CAG	PLBG0100KB-A				-40 to +105 °C
R7FA4L1BB3CAH	PLBG0064JD-A				
R7FA4L1BB4CDB	SUBG0072LB-A				-40 to +125 °C

1.4 Function Comparison

Table 1.15 Function comparison (1 of 2)

Parts number		R7FA4L1BD4CFP R7FA4L1BD3CAG R7FA4L1BB4CFP R7FA4L1BB3CAG	R7FA4L1BD4CDB R7FA4L1BB4CDB	R7FA4L1BD4CFM R7FA4L1BB4CFM	R7FA4L1BD3CAH R7FA4L1BB3CAH	R7FA4L1BD4CFL R7FA4L1BD4CNE R7FA4L1BB4CFL R7FA4L1BB4CNE
Pin count		100	72	64	64	48
Package		LQFP/BGA	WLCSP	LQFP	BGA	LQFP/QFN
Code flash memory		512 KB 256 KB				
Data flash memory		8 KB				
SRAM		64 KB				
	Parity	32 KB				
	ECC	32 KB				
DMA	DTC	Yes				
	DMAC	8				
System	CPU clock	80 MHz (max.)				
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL				
	CAC	Yes				
	WDT/IWDT	Yes				
Communication	SCI[*1]	6				
	IIC	1				
	I3C	1				
	UARTA	2				
	SPI	1				
	CANFD	1				
	USBFS	Yes				
	QSPI	Yes				
	SSIE	Yes		No	Yes	No
Timers	GPT32[*1]	2				
	GPT16[*1]	4				
	AGT[*1]	2				
	RTC	Yes				
Analog	ADC12	Unit 0: 16	Unit 0: 13	Unit 0: 12	Unit 0: 12	Unit 0: 10
	DAC12	1				
	ACMPLP	2				
	TSN	Yes				
HMI	CTSU	12	9	8	8	8
	SLCDC	52 seg × 4 com 48 seg × 8 com	26 seg × 4 com 22 seg × 8 com	22 seg × 4 com 18 seg × 8 com	26 seg × 4 com 22 seg × 8 com	No
Data processing	CRC	Yes				
	DOC	Yes				
Event control	ELC	Yes				
Security		RSIP-E11A, TrustZone, and Lifecycle management				

Table 1.15 Function comparison (2 of 2)

Parts number		R7FA4L1BD4CFP R7FA4L1BD3CAG R7FA4L1BB4CFP R7FA4L1BB3CAG	R7FA4L1BD4CDB R7FA4L1BB4CDB	R7FA4L1BD4CFM R7FA4L1BB4CFM	R7FA4L1BD3CAH R7FA4L1BB3CAH	R7FA4L1BD4CFL R7FA4L1BD4CNE R7FA4L1BB4CFL R7FA4L1BB4CNE
I/O ports	I/O pins	82	53	48	52	34
	Input pins	3	3	3	3	3
	Pull-up resistors	82	53	48	52	34
	N-ch open-drain outputs	75	46	41	45	29
	5-V tolerance	5	5	5	5	5

Note 1. Available pins depend on the pin count. For details, see section 1.7. Pin Lists.

1.5 Pin Functions

Table 1.16 Pin functions (1 of 4)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL/VCL0	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Voltage detector	EXLVD	Input	Low voltage detector for external pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCICn	Input	Time capture event input pins

Table 1.16 Pin functions (2 of 4)

Function	Signal	I/O	Description
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	RXDXn	Input	Input pins for received data (Simple LIN Mode)
	TXDXn	Output	Output pins for transmitted data (Simple LIN Mode)
	SIOXn	I/O	Input/output pins for received or transmitted data (Simple LIN Mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
I3C	I3C_SCL0	I/O	Input/output pin for clock
	I3C_SDA0	I/O	Input/output pin for data
UARTA	RxDAn	Input	Serial data input signal
	TxDAn	Output	Serial data output signal
	CLKAn	Output	Serial clock output signal
SPI	RSPCKA	I/O	Clock input/output pin
	MOSIA	I/O	Input or output pin for data output from the master
	MISOA	I/O	Input or output pin for data output from the slave
	SSLA0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3	Output	Output pins for slave selection
CANFD	CRXn	Input	Receive data
	CTXn	Output	Transmit data

Table 1.16 Pin functions (3 of 4)

Function	Signal	I/O	Description
USBFS	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3
SSIE	SSIBCK0	I/O	SSIE serial bit clock pin
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pin
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
DAC12	DA0	Output	Output pin for the analog signals processed by the D/A converter.
ACMPLP	VCOUT	Output	Comparator output pin
	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
SLCDC	VL1, VL2, VL3, VL4	I/O	Voltage pin for driving the LCD
	CAPH, CAPL	I/O	Capacitor connection for the LCD controller/driver
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver
	SEG0 to SEG51	Output	Segment signal output pins for the LCD controller/driver

Table 1.16 Pin functions (4 of 4)

Function	Signal	I/O	Description
CTSU	TSn	Input	Capacitive touch detection pins (touch pins)
	TSCAP	I/O	Secondary power supply pin for the touch driver
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

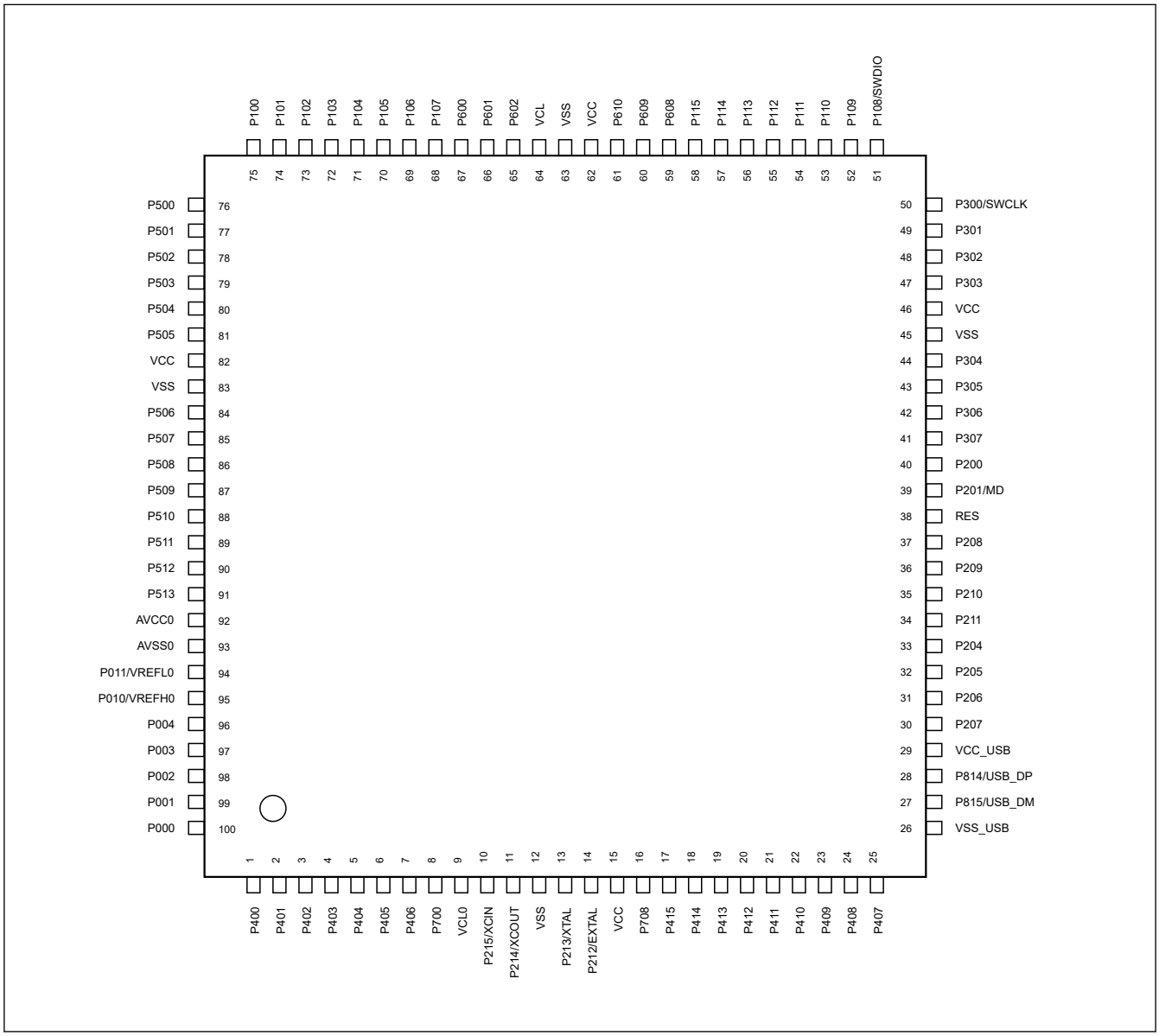
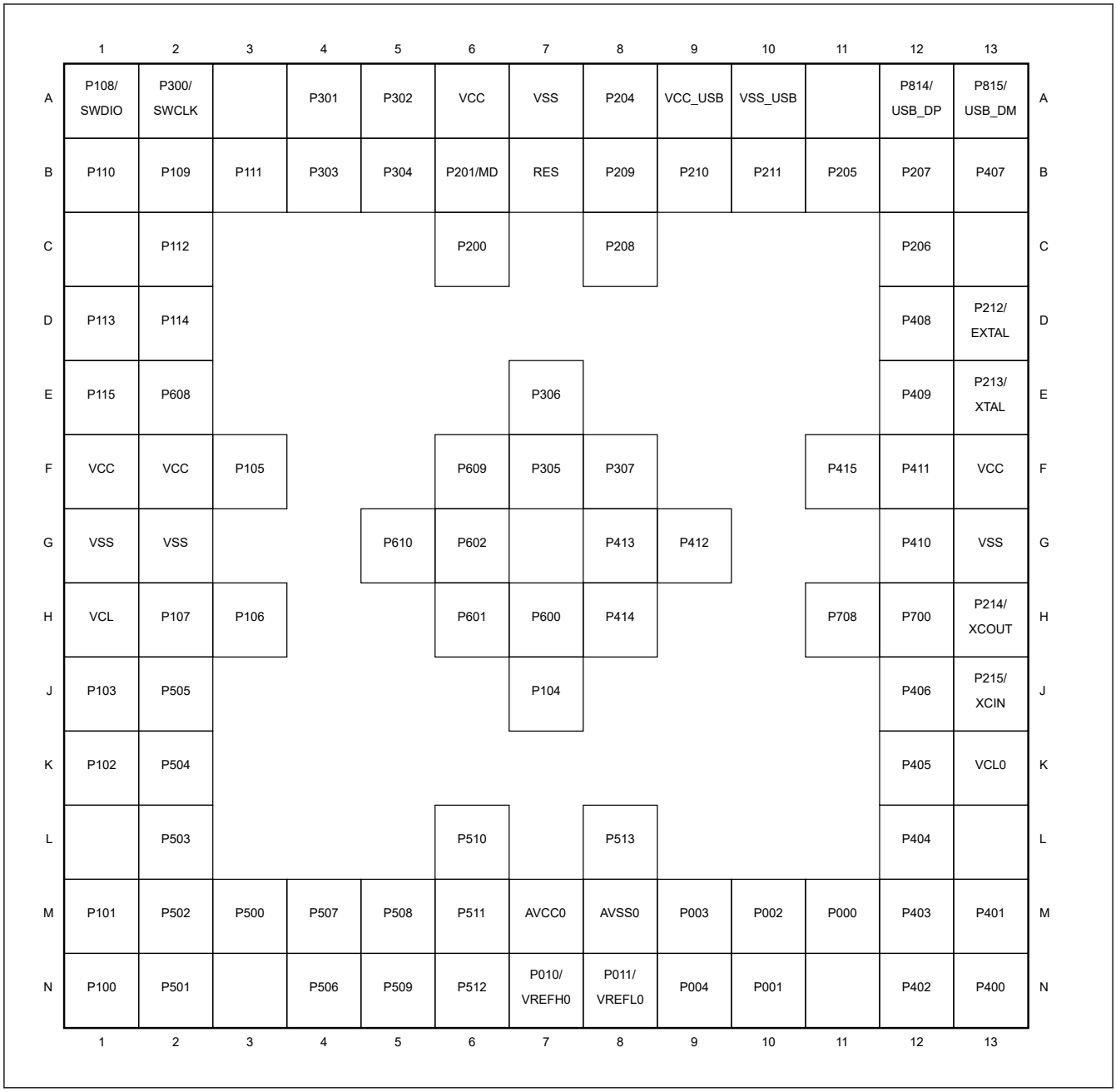
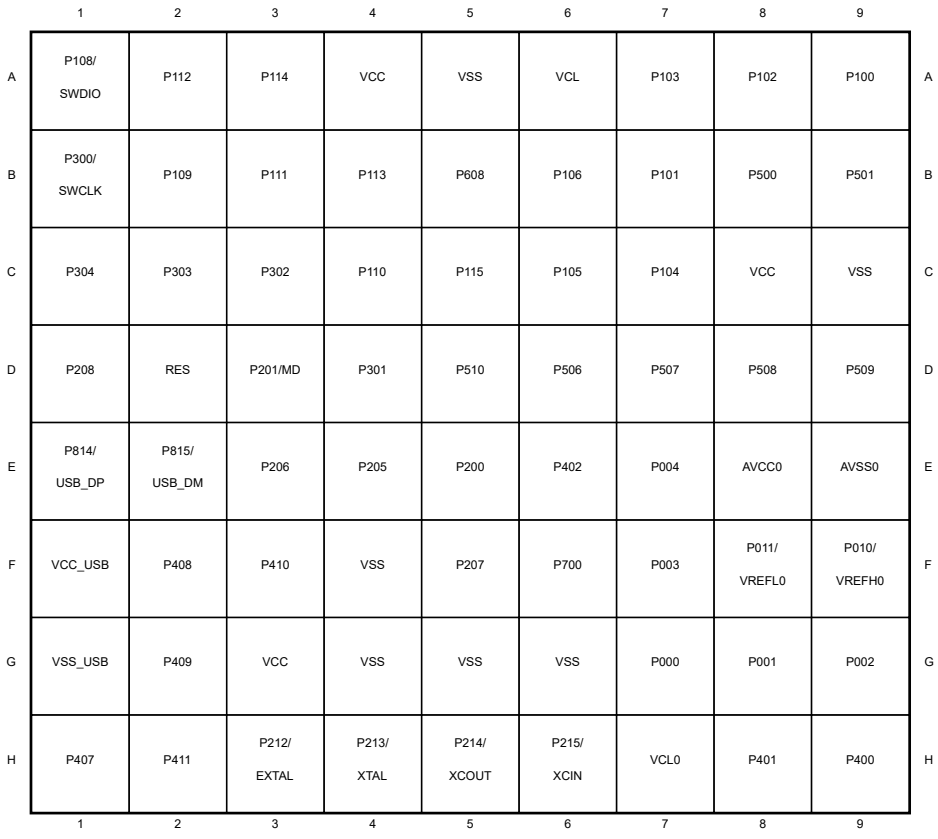


Figure 1.3 Pin assignment for LQFP 100-pin



	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	P108/ SWDIO	P300/ SWCLK		P301	P302	VCC	VSS	P204	VCC_USB	VSS_USB		P814/ USB_DP	P815/ USB_DM	A
B	P110	P109	P111	P303	P304	P201/MD	RES	P209	P210	P211	P205	P207	P407	B
C		P112				P200		P208				P206		C
D	P113	P114										P408	P212/ EXTAL	D
E	P115	P608					P306					P409	P213/ XTAL	E
F	VCC	VCC	P105			P609	P305	P307			P415	P411	VCC	F
G	VSS	VSS			P610	P602		P413	P412			P410	VSS	G
H	VCL	P107	P106			P601	P600	P414			P708	P700	P214/ XCOUT	H
J	P103	P505					P104					P406	P215/ XCIN	J
K	P102	P504										P405	VCL0	K
L		P503				P510		P513				P404		L
M	P101	P502	P500	P507	P508	P511	AVCC0	AVSS0	P003	P002	P000	P403	P401	M
N	P100	P501		P506	P509	P512	P010/ VREFH0	P011/ VREFL0	P004	P001		P402	P400	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 1.4 Pin assignment for BGA 100-pin



	1	2	3	4	5	6	7	8	9	
A	P108/ SWDIO	P112	P114	VCC	VSS	VCL	P103	P102	P100	A
B	P300/ SWCLK	P109	P111	P113	P608	P106	P101	P500	P501	B
C	P304	P303	P302	P110	P115	P105	P104	VCC	VSS	C
D	P208	RES	P201/MD	P301	P510	P506	P507	P508	P509	D
E	P814/ USB_DP	P815/ USB_DM	P206	P205	P200	P402	P004	AVCC0	AVSS0	E
F	VCC_USB	P408	P410	VSS	P207	P700	P003	P011/ VREFL0	P010/ VREFH0	F
G	VSS_USB	P409	VCC	VSS	VSS	VSS	P000	P001	P002	G
H	P407	P411	P212/ EXTAL	P213/ XTAL	P214/ XCOUT	P215/ XCIN	VCL0	P401	P400	H
	1	2	3	4	5	6	7	8	9	

Figure 1.5 Pin assignment for WLCSP 72-pin

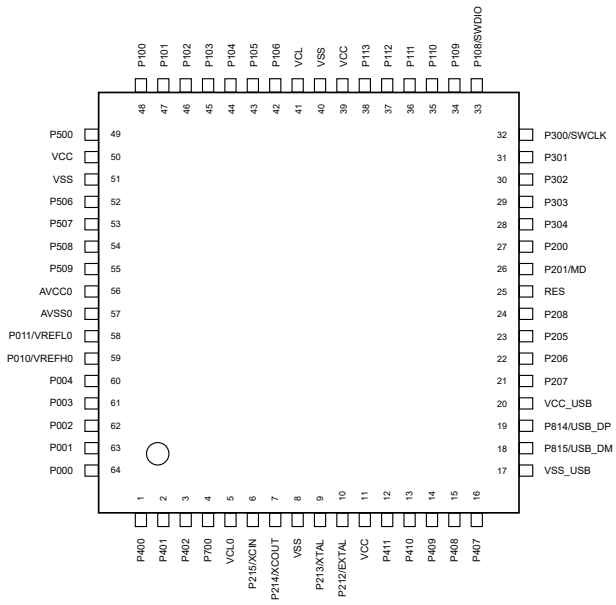
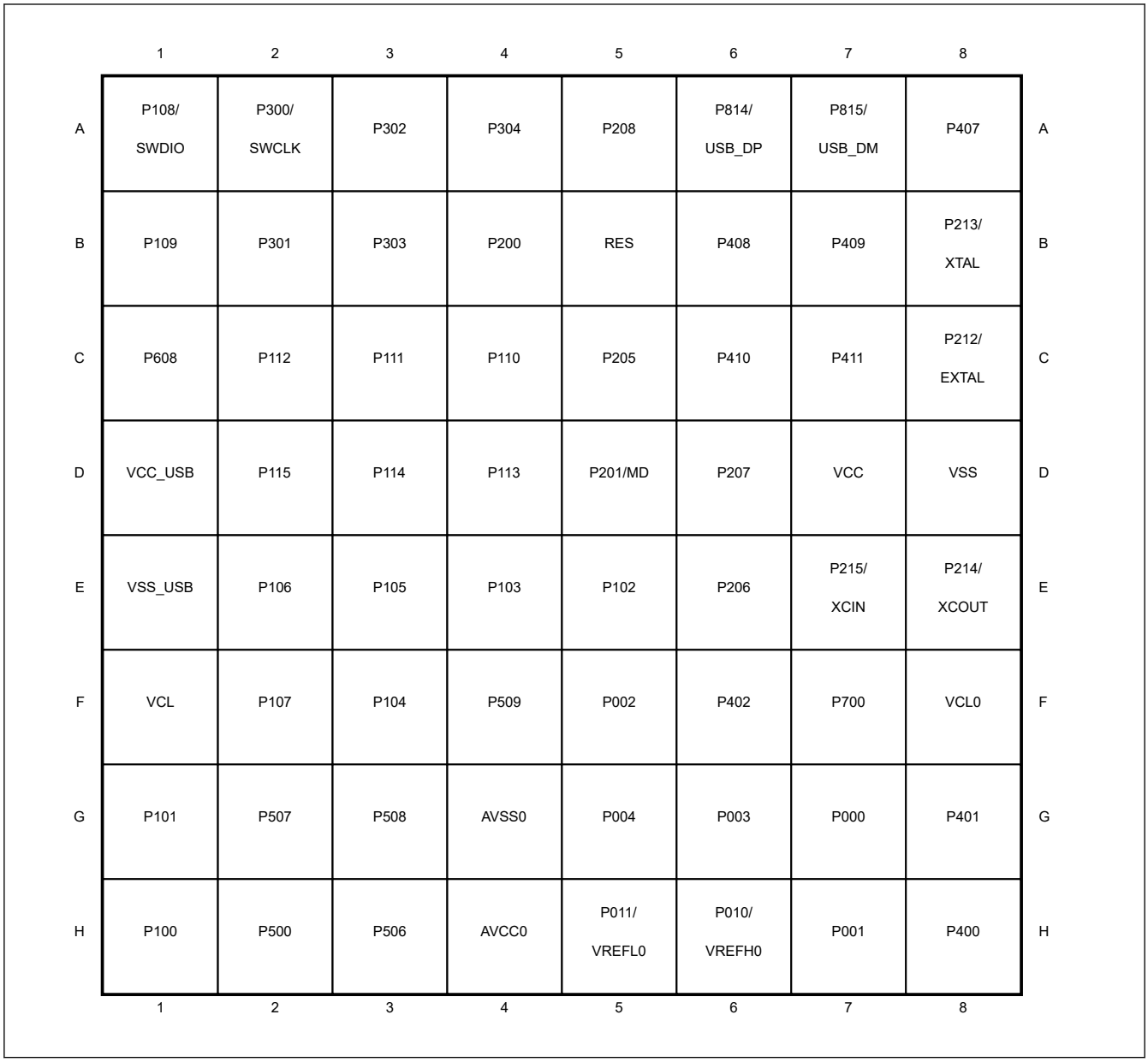


Figure 1.6 Pin assignment for LQFP 64-pin



	1	2	3	4	5	6	7	8	
A	P108/ SWDIO	P300/ SWCLK	P302	P304	P208	P814/ USB_DP	P815/ USB_DM	P407	A
B	P109	P301	P303	P200	RES	P408	P409	P213/ XTAL	B
C	P608	P112	P111	P110	P205	P410	P411	P212/ EXTAL	C
D	VCC_USB	P115	P114	P113	P201/MD	P207	VCC	VSS	D
E	VSS_USB	P106	P105	P103	P102	P206	P215/ XCIN	P214/ XCOUT	E
F	VCL	P107	P104	P509	P002	P402	P700	VCL0	F
G	P101	P507	P508	AVSS0	P004	P003	P000	P401	G
H	P100	P500	P506	AVCC0	P011/ VREFL0	P010/ VREFH0	P001	P400	H
	1	2	3	4	5	6	7	8	

Figure 1.7 Pin assignment for BGA 64-pin

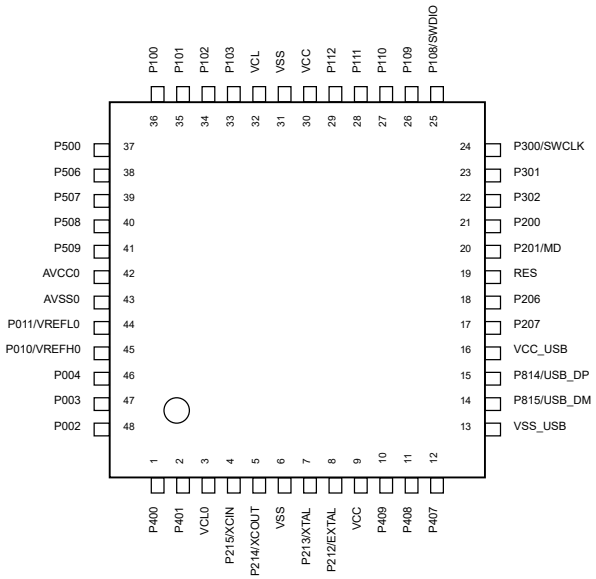
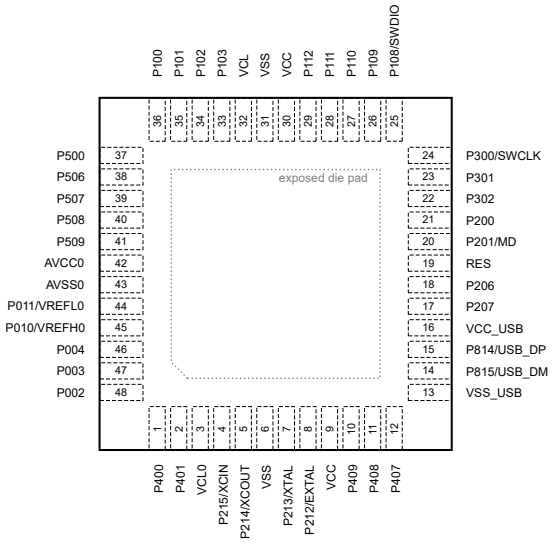


Figure 1.8 Pin assignment for LQFP 48-pin



Note: Exposed die pad is recommended to connect to VSS.

Figure 1.9 Pin assignment for QFN 48-pin

1.7 Pin Lists

Table 1.17 Pin list (1 of 3)

LQFP100	BGA100	WLCSP72	LQFP64	BGA64	LQFP48/ QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. interrupt	SCI/IIC/I3C/CANFD/ USBFS/SPI/QSPI/UARTA/ SSIE	GPT/AGT/RTC	ADC12/ DAC12	ACMPLP	SLCDC	CTSU
1	N13	H9	1	H8	1	—	P400	IRQ0	TXD1/SDA1/MOSI1/TXDX1/ SIOX1/I3C_SCL0/AUDIO_CLK	GTETRGB/ GTIOC2A/AGTIO1	—	—	SEG4	—
2	M13	H8	2	G8	2	—	P401	IRQ5	RXD1/SCL1/MISO1/RXDX1/ I3C_SDA0/CRX0	GTETRGA/ GTIOC2B	—	—	SEG5	—
3	N12	E6	3	F6	—	CACREF	P402	IRQ4	CTS1_RTS1/SS1/CTX0/ AUDIO_CLK	GTETRGC/AGTIO0/ AGTIO1/RTCIC0	—	—	SEG6	—
4	M12	—	—	—	—	—	P403	IRQ14	SCK1/SSIBCK0_A	AGTIO0/AGTIO1/ RTCIC1	—	—	SEG7	—
5	L12	—	—	—	—	—	P404	IRQ15	SSILRCK0_A/SSIFS0_A	AGTIO0/AGTIO1/ RTCIC2	—	—	SEG8	—
6	K12	—	—	—	—	—	P405	—	SSITXD0_A	GTIOC1A	—	—	SEG9	—
7	J12	—	—	—	—	—	P406	—	SSIRXD0_A	GTIOC1B	—	—	SEG10	—
8	H12	F6	4	F7	—	—	P700	—	—	—	—	—	SEG11	—
9	K13	H7	5	F8	3	VCL0	—	—	—	—	—	—	—	—
10	J13	H6	6	E7	4	XCIN	P215	—	—	—	—	—	—	—
11	H13	H5	7	E8	5	XCOUT	P214	—	—	—	—	—	—	—
12	G13	G4	8	D8	6	VSS	—	—	—	—	—	—	—	—
13	E13	H4	9	B8	7	XTAL	P213	IRQ2	TXD0/SDA0/MOSI0	GTETRGC/ GTIOC0A	—	—	—	—
14	D13	H3	10	C8	8	EXTAL	P212	IRQ3	RXD0/SCL0/MISO0	GTETRGD/ GTIOC0B/AGTEE1	—	—	—	—
15	F13	G3	11	D7	9	VCC	—	—	—	—	—	—	—	—
16	H11	—	—	—	—	CACREF	P708	IRQ11	AUDIO_CLK	—	—	—	SEG12	—
17	F11	—	—	—	—	—	P415	IRQ8	USB_VBUSEN	GTIOC0A	—	—	SEG13	—
18	H8	—	—	—	—	—	P414	IRQ9	—	GTIOC0B	—	—	SEG14	—
19	G8	—	—	—	—	—	P413	—	—	GTOUUP	—	—	SEG15	—
20	G9	—	—	—	—	—	P412	—	CTS3	GTOULO/AGTEE1	—	—	SEG16	—
21	F12	H2	12	C7	—	—	P411	IRQ4	CTS3_RTS3/SS3	GTOVUP/AGTOA1	—	—	VL1	—
22	G12	F3	13	C6	—	—	P410	IRQ5	SCK3	GTOVLO/AGTOB1	—	—	VL2	—
23	E12	G2	14	B7	10	—	P409	IRQ6	TXD3/SDA3/MOSI3/ USB_EXICEN	GTOWUP	—	—	VL4	—
24	D12	F2	15	B6	11	—	P408	IRQ7	CTS4_RTS4/SS4/RXD3/SCL3/ MISO3/USB_ID	GTOWLO/ GTIOC2B/RTCIC0	—	—	VL3	—
25	B13	H1	16	A8	12	—	P407	—	CTS4/USB_VBUS	GTIOC2A/AGTIO0/ RTCOUT	ADTRG0	—	SEG17	—
26	A10	G1	17	E1	13	VSS_USB	—	—	—	—	—	—	—	—
27	A13	E2	18	A7	14	USB_DM	P815	—	TxDA1	—	—	—	—	—
28	A12	E1	19	A6	15	USB_DP	P814	—	RxDA1	—	—	—	—	—
29	A9	F1	20	D1	16	VCC_USB	—	—	—	—	—	—	—	—
30	B12	F5	21	D6	17	—	P207	—	TXD4/SDA4/MOSI4/ USB_OVRCURB/QSSL	GTIOC3A	—	—	CAPH	—
31	C12	E3	22	E6	18	—	P206	IRQ0	RXD4/SCL4/MISO4/ USB_VBUSEN	GTIU/GTIOC3B	—	—	CAPL	—
32	B11	E4	23	C5	—	CLKOUT	P205	IRQ1	SCK4/USB_OVRCURA	GTIV/GTIOC4A/ AGTO1	—	—	COM0	—
33	A8	—	—	—	—	—	P204	—	CTS4_RTS4/SS4/SSLA0_A/ QSPCLK	GTIU	—	—	SEG18	—
34	B10	—	—	—	—	—	P211	—	MOSIA_A/QIO0	GTIV	—	—	SEG19	—
35	B9	—	—	—	—	—	P210	—	MISOA_A/QIO1	GTIW	—	—	SEG20	—
36	B8	—	—	—	—	—	P209	—	RSPCKA_A/QIO2	GTOVUP	—	—	SEG21	—
37	C8	D1	24	A5	—	—	P208	IRQ12	QIO3	GTOVLO	—	—	COM1	—
38	B7	D2	25	B5	19	RES	—	—	—	—	—	—	—	—
39	B6	D3	26	D5	20	MD	P201	—	—	—	—	—	—	—

Table 1.17 Pin list (2 of 3)

LQFP100	BGA100	WLCSP72	LQFP64	BGA64	LQFP48/ QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. interrupt	SCI/IIC/I3C/CANFD/ USBFS/SPI/QSPI/UARTA/ SSIE	GPT/AGT/RTC	ADC12/ DAC12	ACMPLP	SLCDC	CTSU
40	C6	E5	27	B4	21	—	P200	NMI	—	—	—	—	—	—
41	F8	—	—	—	—	—	P307	—	—	GTOUUP	—	—	SEG22	—
42	E7	—	—	—	—	—	P306	—	TxDA0	GTOULO	—	—	SEG23	—
43	F7	—	—	—	—	—	P305	IRQ8	RxDA0	GTOWUP	—	—	SEG24	—
44	B5	C1	28	A4	—	—	P304	IRQ9	CTS5_RTS5/SS5/CLKA0	GTOWLO/GTIOC3A	—	—	COM2	—
45	A7	—	—	—	—	VSS	—	—	—	—	—	—	—	—
46	A6	—	—	—	—	VCC	—	—	—	—	—	—	—	—
47	B4	C2	29	B3	—	—	P303	—	SCK5	GTIOC3B	—	—	COM3	—
48	A5	C3	30	A3	22	—	P302	IRQ5	TXD5/SDA5/MOSI5/SCL0_A/ SSLA3_B	GTOUUP/GTIOC4A	ADTRG0	—	SEG25	—
49	A4	D4	31	B2	23	—	P301	IRQ6	RXD5/SCL5/MISO5/SDA0_A/ SSLA2_B	GTOULO/GTIOC4B/ AGTIO0	—	—	SEG26	—
50	A2	B1	32	A2	24	SWCLK	P300	—	CTS5/SSLA1_B	GTOUUP/GTIOC0A	—	—	SEG27	—
51	A1	A1	33	A1	25	SWDIO	P108	—	CTS9_RTS9/SS9/SSLA0_B	GTOULO/GTIOC0B	—	—	SEG28	—
52	B2	B2	34	B1	26	CLKOUT	P109	—	TXD9/SDA9/MOSI9/MOSIA_B	GTOVUP/GTIOC1A	—	—	COM4/SEG0	—
53	B1	C4	35	C4	27	—	P110	IRQ3	RXD9/SCL9/MISO9/MISOA_B	GTOVLO/GTIOC1B	—	—	COM5/SEG1	—
54	B3	B3	36	C3	28	—	P111	IRQ4	SCK9/RSPCKA_B	—	—	VCOUT	COM6/SEG2	—
55	C2	A2	37	C2	29	—	P112	—	CTS9_RTS9/SS9/SSLA0_B/ QSSL	—	—	—	COM7/SEG3	—
56	D1	B4	38	D4	—	—	P113	—	SSIBCK0_B	—	—	—	SEG29	—
57	D2	A3	—	D3	—	—	P114	—	CTS9/SSILRCK0_B/SSIFS0_B	—	—	—	SEG30	—
58	E1	C5	—	D2	—	—	P115	—	TXD1/SDA1/MOSI1/TXDX1/ SIOX1/SSIRXD0_B	GTIOC4A	—	—	SEG31	—
59	E2	B5	—	C1	—	—	P608	—	RXD1/SCL1/MISO1/RXDX1/ SSITXD0_B	GTIOC4B	—	—	SEG32	—
60	F6	—	—	—	—	—	P609	—	SCK1	GTIOC5A	—	—	SEG33	—
61	G5	—	—	—	—	—	P610	—	CTS1_RTS1/SS1	GTIOC5B	—	—	SEG34	—
62	F1	A4	39	—	30	VCC	—	—	—	—	—	—	—	—
63	G1	A5	40	—	31	VSS	—	—	—	—	—	—	—	—
64	H1	A6	41	F1	32	VCL	—	—	—	—	—	—	—	—
65	G6	—	—	—	—	—	P602	—	—	—	—	—	SEG35	—
66	H6	—	—	—	—	—	P601	—	—	GTIOC2A	—	—	SEG36	—
67	H7	—	—	—	—	CACREF/ CLKOUT	P600	—	—	GTIOC2B	—	—	SEG37	—
68	H2	—	—	F2	—	—	P107	—	—	AGTOA0	—	—	SEG38	—
69	H3	B6	42	E2	—	—	P106	—	CTS3	GTETRGD/AGTOB0	—	—	SEG39	—
70	F3	C6	43	E3	—	—	P105	IRQ0	CTS3_RTS3/SS3	GTETRGA/ GTIOC1A	—	—	SEG40	—
71	J7	C7	44	F3	—	—	P104	IRQ1	SCK3/QSPCLK	GTETRGB/ GTIOC1B	—	—	SEG41	—
72	J1	A7	45	E4	33	—	P103	—	CTS0_RTS0/SS0/TXD3/SDA3/ MOSI3/CRX0/QIO2	GTOWUP	—	CMPREF1	SEG42	TS0
73	K1	A8	46	E5	34	—	P102	—	SCK0/RXD3/SCL3/MISO3/ CTX0/QIO3	GTOWLO/AGTO0	ADTRG0	CMPIN1	SEG43	TS1
74	M1	B7	47	G1	35	—	P101	IRQ1	TXD0/SDA0/MOSI0/SCL0_B/ QIO0	GTETRGB/ GTIOC5A/AGTEE0	—	CMPREF0	SEG44	TS2
75	N1	A9	48	H1	36	—	P100	IRQ2	RXD0/SCL0/MISO0/SDA0_B/ QIO1	GTETRGA/ GTIOC5B/AGTIO0	—	CMPIN0	SEG45	TS3
76	M3	B8	49	H2	37	CACREF	P500	—	CTS0/USB_VBUSEN/QSPCLK	GTIU/AGTOA0	AN021	VCOUT	SEG46	TSCAP
77	N2	B9	—	—	—	—	P501	IRQ11	USB_OVRCURA/QSSL	GTIV/AGTOB0	—	—	SEG47	TS4
78	M2	—	—	—	—	—	P502	IRQ12	USB_OVRCURB/QIO0	GTIW	—	—	SEG48	TS5
79	L2	—	—	—	—	—	P503	—	USB_EXICEN/QIO1	GTETRGC	—	—	SEG49	TS6
80	K2	—	—	—	—	—	P504	—	USB_ID/QIO2	GTETRGD	—	—	SEG50	TS7
81	J2	—	—	—	—	—	P505	IRQ14	QIO3	—	—	VCOUT	SEG51	—

Table 1.17 Pin list (3 of 3)

LQFP100	BGA100	WLCSP72	LQFP64	BGA64	LQFP48/ QFN48	Power, System, Clock, Debug, CAC	I/O ports	Ex. interrupt	SCI/IIC/I3C/CANFD/ USBFS/SPI/QSPI/UARTA/ SSIE	GPT/AGT/RTC	ADC12/ DAC12	ACMPLP	SLCDC	CTSU
82	F2	C8	50	—	—	VCC	—	—	—	—	—	—	—	—
83	G2	C9	51	—	—	VSS	—	—	—	—	—	—	—	—
84	N4	D6	52	H3	38	—	P506	IRQ13	TXD5/SDA5/MOSI5	GTIOC4A	AN020	—	—	TS8
85	M4	D7	53	G2	39	—	P507	—	RXD5/SCL5/MISO5/CLKA0	GTIOC4B	AN019	—	—	TS9
86	M5	D8	54	G3	40	—	P508	—	CTS5_RTS5/SS5/TxDA0	—	AN018	—	—	TS10
87	N5	D9	55	F4	41	EXLVD	P509	—	SCK5/RxDA0	—	AN017	—	—	TS11
88	L6	D5	—	—	—	—	P510	—	TXD9/SDA9/MOSI9	—	AN025	—	—	—
89	M6	—	—	—	—	—	P511	—	RXD9/SCL9/MISO9/CLKA1	—	AN024	—	—	—
90	N6	—	—	—	—	—	P512	—	CTS9_RTS9/SS9/TxDA1	—	AN023	—	—	—
91	L8	—	—	—	—	—	P513	—	SCK9/RxDA1	—	AN022	—	—	—
92	M7	E8	56	H4	42	AVCC0	—	—	—	—	—	—	—	—
93	M8	E9	57	G4	43	AVSS0	—	—	—	—	—	—	—	—
94	N8	F8	58	H5	44	VREFL0	P011	IRQ11	—	—	AN004	—	—	—
95	N7	F9	59	H6	45	VREFH0	P010	IRQ10	—	—	AN003	—	—	—
96	N9	E7	60	G5	46	—	P004	IRQ9	—	—	AN002/DA0	—	—	—
97	M9	F7	61	G6	47	—	P003	—	—	—	AN001	—	—	—
98	M10	G9	62	F5	48	—	P002	IRQ8	—	—	AN000	—	—	—
99	N10	G8	63	H7	—	—	P001	IRQ7	—	—	AN006	—	—	—
100	M11	G7	64	G7	—	—	P000	IRQ6	—	—	AN005	—	—	—
—	—	G5	—	—	—	VSS	—	—	—	—	—	—	—	—
—	—	G6	—	—	—	VSS	—	—	—	—	—	—	—	—
—	—	F4	—	—	—	VSS	—	—	—	—	—	—	—	—

2. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC[*1] = AVCC0 = VCC_USB = 1.6 to 3.6 V, VREFH0 = 1.6 V to AVCC0

VSS = AVSS0 = VREFL0 = VSS_USB = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.

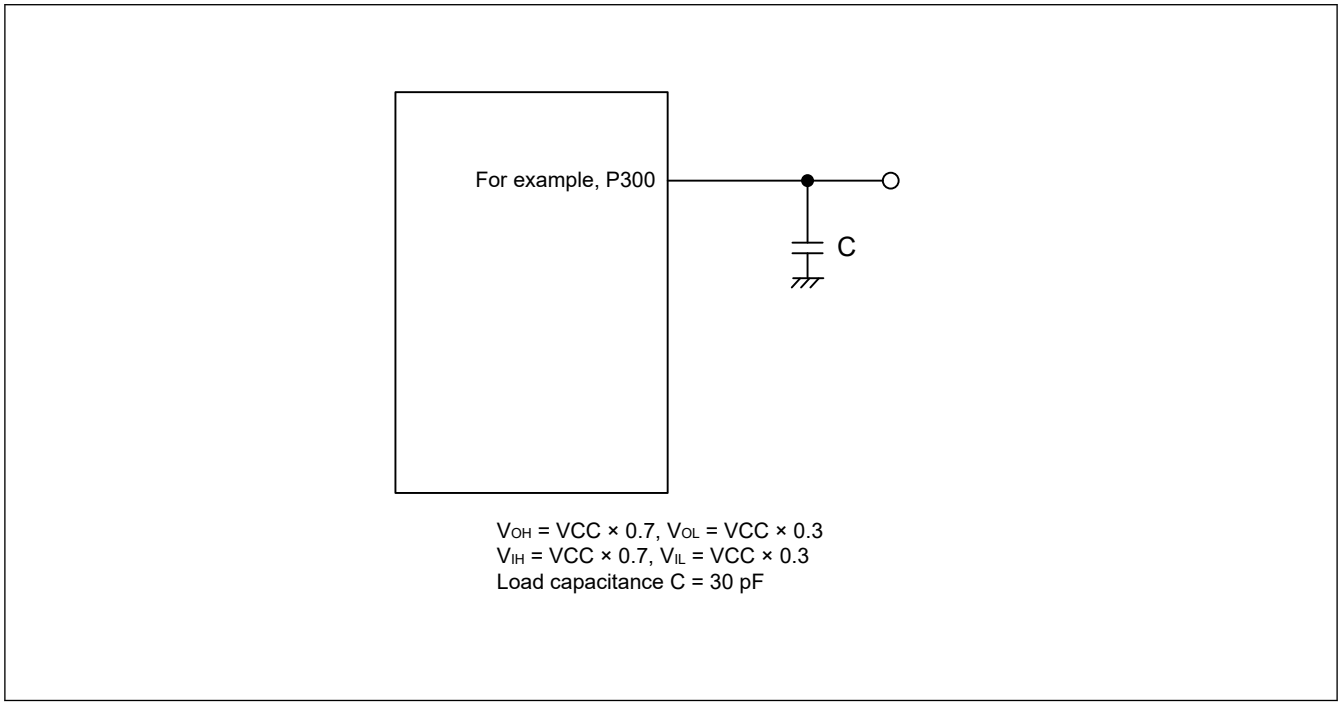


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB[*2]	-0.5 to +4.0	V
Input voltage	5V-tolerant ports[*1]	V_{in}	-0.3 to +6.5	V
	P000 to P004, P010, P011	V_{in}	-0.3 to AVCC0 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +4.0	V
Analog power supply voltage		AVCC0[*2]	-0.5 to +4.0	V
Analog input voltage	When AN000 to AN006 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN017 to AN025 are used		-0.3 to VCC + 0.3	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter		Symbol	Value	Unit
LCD voltage	VL1 voltage	V_{L1}	-0.3 to V_{L4} + 0.3*5	V
	VL2 voltage	V_{L2}	-0.3 to V_{L4} + 0.3*5	V
	VL3 voltage	V_{L3}	-0.3 to V_{L4} + 0.3*5	V
	VL4 voltage	V_{L4}	-0.3 to +6.5	V
Operating temperature*3 *4		T_{opr}	-40 to +105 -40 to +125	°C
Storage temperature		T_{stg}	-55 to +140	°C

Note 1. Ports P301, P302, P400, P401, and P407 are 5V-tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. Connect AVCC0 and VCC_USB to VCC
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. The upper limit of the operating temperature is 105 °C or 125 °C, depending on the product.
Note 5. Must be 6.5 V or lower.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **AVCC0 and AVSS0: about 0.1 µF**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin and VCL0 pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC*1 *2	When USB is not used	1.6	—	3.6	V
		When USB is used	3.0	—	3.6	V
	VSS		—	0	—	V
USB power supply voltage	VCC_USB		—	VCC	—	V
	VSS_USB		—	0	—	V
Analog power supply voltages	AVCC0*1 *2		1.6	—	3.6	V
	AVSS0		—	0	—	V
	VREFH0	When used as ADC12 Reference	1.6	—	AVCC0	V
	VREFL0		—	0	—	V

Note 1. Use AVCC0 and VCC under the following conditions:
AVCC0 = VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pins.
When powering off the VCC and AVCC0 pins, power them off at the same time or the AVCC0 pin first and then the VCC pins.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +125 °C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	140	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is 105 °C or 125 °C, depending on the product. If the part number shows the operation temperature at 85 °C, then the maximum value of Tj is 105 °C, otherwise it is 140 °C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (SDA0_A, SCL0_A)/I3C (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8	V	—
		V_{IL}	—	—	VCC × 0.3		
		ΔV_T	VCC × 0.10	—	—		VCC = 2.7 V to 3.6 V
			VCC × 0.05	—	—		VCC = 1.6 V to2.7 V
	RES, NMI Other peripheral input pins excluding IIC (SDA0_A, SCL0_A)/I3C	V_{IH}	VCC × 0.8	—	—		—
		V_{IL}	—	—	VCC × 0.2		
		ΔV_T	VCC × 0.10	—	—		VCC = 2.7 V to 3.6 V
			VCC × 0.05	—	—		VCC = 1.6 V to 2.7 V
Input voltage except for Schmitt trigger input pin	IIC/I3C (SMBus)*2	V_{IH}	2.0	—	—		VCC = 1.8 to 3.6 V
		V_{IL}	—	—	0.5		VCC = 1.8 to 3.6 V
	5V-tolerant ports*3	V_{IH}	VCC × 0.8	—	5.8		—
		V_{IL}	—	—	VCC × 0.2		
	P000 to P004, P010, P011	V_{IH}	AVCC0 × 0.8	—	—		
		V_{IL}	—	—	AVCC0 × 0.2		
	Input port pins except for P000 to P004, P010, P011	V_{IH}	VCC × 0.8	—	—		
		V_{IL}	—	—	VCC × 0.2		

Note 1. SCL0_A, SDA0_A, I3C_SCL, I3C_SDA (total 4 pins)
Note 2. SCL0_A, SDA0_A, SCL0_B, SDA0_B, I3C_SCL, I3C_SDA (total 6 pins)
Note 3. P400, P401, P407, P301, P302 (total 5 pins)

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (average value per pin)	I_{OH}	—	—	−4.0	mA	
	I_{OL}	—	—	8.0	mA	
Permissible output current (max value per pin)	I_{OH}	—	—	−4.0	mA	
	I_{OL}	—	—	8.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	All products	Total of ports P000 to P004, P010, P011	ΣI_{OH} (max)	—	—	−30	mA	AVCC0 = 2.7 to 3.6 V
				—	—	−8	mA	AVCC0 = 1.8 to 2.7 V
				—	—	−4	mA	AVCC0 = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	AVCC0 = 2.7 to 3.6 V
				—	—	4	mA	AVCC0 = 1.8 to 2.7 V
				—	—	2	mA	AVCC0 = 1.6 to 1.8 V
		Total of ports P212, P213	ΣI_{OH}	—	—	−8.0	mA	VCC = 2.7 to 3.6 V
				—	—	−2	mA	VCC = 1.8 to 2.7 V
				—	—	−1	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL}	—	—	16.0	mA	VCC = 2.7 to 3.6 V
				—	—	1.2	mA	VCC = 1.8 to 2.7 V
				—	—	0.6	mA	VCC = 1.6 to 1.8 V
	100 pin QFP, 100 pin BGA	Total of ports P400 to P415, P700, P708	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (3 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	100 pin QFP, 100 pin BGA	Total of ports P204 to P211, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P108 to P112, P201, P300 to P307	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P100 to P107, P113 to P115, P600 to P602, P608 to P610	ΣI_{OH}	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL}	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P500 to P513	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−100	mA	
			ΣI_{OL} (max)	—	—	100	mA	

Table 2.5 I/O I_{OH}, I_{OL} (4 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	72 pin WLCSP	Total of ports P400 to P402, P407 to P411, P700	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P201, P205 to P208, P303, P304, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P300 to P302, P105, P106, P108 to P115, P608	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (5 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	72 pin WLCSP	Total of ports P100 to P104, P500, P501, P506 to P510	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−60	mA	
			ΣI_{OL} (max)	—	—	100	mA	
	64 pin LQFP	Total of ports P400 to P402, P407 to P411, P700	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P201, P205 to P208, P303, P304, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (6 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	64 pin LQFP	Total of ports P300 to P302, P105, P106, P108 to P115	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P100 to P104, P500, P506 to P509	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−60	mA	
			ΣI_{OL} (max)	—	—	100	mA	
	64 pin BGA	Total of ports P400 to P402, P407 to P411, P700	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (7 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	64 pin BGA	Total of ports P201, P205 to P208, P303, P304, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P300 to P302, P105 to P115, P608	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P100 to P104, P500, P506 to P509	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−60	mA	
			ΣI_{OL} (max)	—	—	100	mA	

Table 2.5 I/O I_{OH}, I_{OL} (8 of 8)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*1	48 pin products	Total of ports P400, P401, P407 to P409, P814, P815	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P108 to P112, P201, P206, P207, P300 to P302	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of ports P100 to P103, P500, P506 to P509	ΣI_{OH} (max)	—	—	−30	mA	VCC = 2.7 to 3.6 V
				—	—	−8	mA	VCC = 1.8 to 2.7 V
				—	—	−4	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL} (max)	—	—	50	mA	VCC = 2.7 to 3.6 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
		Total of all output pin	ΣI_{OH} (max)	—	—	−60	mA	
			ΣI_{OL} (max)	—	—	100	mA	

Note 1. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = AVCC0 = 2.7 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	P400, P401	V_{OH}	VCC − 0.27	—	—	V	I_{OH} = −3.0 mA
			VCC − 0.8	—	—		I_{OH} = −4.0 mA
	Ports P000 to P004, P010, P011	V_{OH}	AVCC0 − 0.8	—	—		I_{OH} = −4.0 mA
	Output pins except for P000 to P004 and P010, P011, P400, P401*1	V_{OH}	VCC − 0.8	—	—		I_{OH} = −4.0 mA
	P400, P401	V_{OL}	—	—	0.27		I_{OL} = 3.0 mA
			—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
			—	—	0.8		I_{OL} = 8.0 mA
	P301, P302	V_{OL}	—	0.4	—		I_{OL} = 20 mA (ICFER.FMPE = 1)
			—	—	0.8		I_{OL} = 8.0 mA
	Ports P000 to P004, P010, P011	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Output pins except for P000 to P004 and P010, P011, P301, P302, P400, P401*1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC0 = 1.8 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010, P011	V_{OH}	AVCC0 − 0.5	—	—	V	I_{OH} = −1.0 mA
	Output pins except for P000 to P004 and P010, P011*1	V_{OH}	VCC − 0.5	—	—		I_{OH} = −1.0 mA
	P301, P302, P400, P401	V_{OL}	—	0.4	—		I_{OL} = 3.0 mA
			—	0.6	—		I_{OL} = 6.0 mA
			—	—	0.4		I_{OL} = 0.6 mA
	Ports P000 to P004, P010, P011	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA
	Output pins except for P000 to P004 and P010, P011, P301, P302, P400, P401*1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC0 = 1.6 to 1.8 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P004, P010, P011	V_{OH}	AVCC0 − 0.5	—	—	V	I_{OH} = −0.5 mA
	Output pins except for P000 to P004 and P010, P011*1	V_{OH}	VCC − 0.5	—	—		I_{OH} = −0.5 mA
	Ports P000 to P004, P010, P011	V_{OL}	—	—	0.4		I_{OL} = 0.3 mA
	Output pins except for P000 to P004 and P010, P011*1	V_{OL}	—	—	0.4		I_{OL} = 0.3 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.9 I/O other characteristics

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200, P214, P215	$\|I_{in}\|$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports*1	$\|I_{TSI}\|$	—	—	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, P214, P215, and 5V-tolerant ports)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V, f = 1 MHz T_a = 25 °C
	Other input pins		—	—	15		

Note 1. P301, P302, P400, P401, and P407 (total 5 pins)

2.2.5 Operating and Standby Current

Table 2.10 High-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test Conditions
Maximum*1 *2		ICC*3	—	75	mA	ICLK = 80 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 40 MHz PCLKD = 80 MHz FCLK = 40 MHz
CoreMark®*4 *5			20.4	—	mA	
			255	—	uA/MHz	
Normal mode	All peripheral clocks enabled, and cache disable. While (1) code is executing from flash*5		30.7	—	mA	
			384	—	uA/MHz	
	All peripheral clocks disabled, and cache disable. While (1) code is executing from flash*4 *5		13.4	—	mA	
			168	—	uA/MHz	
Sleep mode	All peripheral clocks enabled, and cache disable*5		22.8	—	mA	
	All peripheral clocks disabled, and cache disable.*4 *5		5.63	—	mA	
Increase during BGO operation*6			2.74		mA	

Note: Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note 1. Measured with clocks supplied to the peripheral functions.
Note 2. PLL output frequency = 80MHz. The clock source is MOSC.
Note 3. ICC depends on f (ICLK) as follows (reference data).
ICC Max. = 0.80 × f + 9.51 (max. operation)
ICC Typ. = 0.15 × f + 2.37 (normal operation, all peripheral clocks disabled and cache disabled)
ICC Typ. = 0.26 × f + 3.39 (sleep mode, all peripheral clocks enabled and cache disabled)
Note 4. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.25 MHz).
Note 5. PLL is stopped, and HOCO output frequency = 80 MHz
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Table 2.11 Middle-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
Normal mode	All peripheral clocks enabled, and cache disable. While (1) code is executing from flash	ICC*1	4.38	—	mA	ICLK = 8 MHz PCLKA = 8 MHz PCLKB = 8 MHz PCLKC = 8 MHz PCLKD = 8 MHz FCLK = 8 MHz
	All peripheral clocks disabled, and cache disable. While (1) code is executing from flash*2		1.79	—		
Sleep mode	All peripheral clocks enabled, and cache disable.		3.40	—		
	All peripheral clocks disabled, and cache disable.*2		0.81	—		
Increase during BGO operation*3			2			

Note: Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note: The clock source is MOCO.
Note 1. ICC depends on f (ICLK) as follows (reference data).
ICC Typ. = 0.49 × f + 0.48 (normal operation, all peripheral clocks disabled and cache disabled)
Note 2. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (125 kHz).
Note 3. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Table 2.12 Low-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
Normal mode	All peripheral clocks enabled, and cache disable. While (1) code is executing from flash	ICC*1	1.10	—	mA	ICLK = 1 MHz PCLKA = 1 MHz PCLKB = 1 MHz PCLKC = 1 MHz PCLKD = 1 MHz FCLK = 1 MHz
	All peripheral clocks disabled, and cache disable. While (1) code is executing from flash*2		0.33	—		
Sleep mode	All peripheral clocks enabled, and cache disable.		0.94	—		
	All peripheral clocks disabled, and cache disable.*2		0.22	—		

Note: Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note: The clock source is MOSC.
Note 1. ICC depends on f (ICLK) as follows (reference data).
ICC Typ. = 0.33 × f + 0.02 (normal operation, all peripheral clocks disabled and cache disabled)
Note 2. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.625 kHz).

Table 2.13 Subosc-speed mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
Normal mode	All peripheral clocks enabled, and cache disable. While (1) code is executing from flash	ICC	20	—	µA	ICLK = 32.768 kHz PCLKA = 32.768 kHz PCLKB = 32.768 kHz PCLKC = 32.768 kHz PCLKD = 32.768 kHz FCLK = 32.768 kHz
	All peripheral clocks disabled, and cache disable. While (1) code is executing from flash*1		8.73	—		
Sleep mode	All peripheral clocks enabled, and cache disable.		15	—		
	All peripheral clocks disabled, and cache disable.*1		4.26	—		

Note: Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note: This does not include the BGO operation.
Note: The clock source is LOCO.
Note 1. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz).

Table 2.14 Software Standby mode current

Parameter		Symbol	Typ	Max	Unit	Test conditions
All SRAMs (0x2000_0000 to 0x2000_FFFF) are on	Ta = 25°C	ICC	1.70	—	µA	—
	Ta = 55°C		6.00	—		
	Ta = 85°C		21.40	—		
	Ta = 105°C		50.00	—		
	Ta = 125°C		117.00	—		
Only 16KB SRAM (0x2000_0000 to 0x2000_3FFF) is on	Ta = 25°C		1.65	—		

Note: Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state. The supply current is total current flowing into VCC.
Note: The IWDT and LVD are not operating.
Note: If you want to operate RTC, please add the value of Table 2.15.

Table 2.15 Increase current by RTC operation

Parameter		Symbol	Typ	Max	Unit	Test conditions
LOCO*1		ICC	0.47	—	µA	
SOSC*2 (normal mode)	RTC (normal operation mode)		0.89	—		SOMCR.SODRV[1:0] = 00b RCR4.ROPSEL = 0
	RTC (low-consumption clock mode)		0.79	—		SOMCR.SODRV[1:0] = 00b RCR4.ROPSEL = 1
SOSC*2 (Low power mode 3)	RTC (normal operation mode)		0.27	—		SOMCR.SODRV[1:0] = 11b RCR4.ROPSEL = 0
	RTC (low-consumption clock mode)		0.11	—		SOMCR.SODRV[1:0] = 11b RCR4.ROPSEL = 1

Note 1. Includes the low-speed on-chip oscillator current.
Note 2. Includes the sub-clock oscillation circuit current.

Table 2.16 Analog current (1 of 2)

Parameter		Symbol	Typ	Max	Unit	Test conditions
Analog power supply current	During 12-bit A/D conversion (at high-speed A/D conversion mode)	I_{AVCC0}	0.57	1	mA	—
	During 12-bit A/D conversion (at low-power A/D conversion mode)		0.24	0.8	mA	—
	During 12-bit D/A conversion*1		0.45	1	mA	—
	Waiting for 12-bit A/D and 12-bit D/A conversion*2		—	4	µA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion	I_{REFH0}	—	150	µA	—
	Waiting for 12-bit A/D conversion		—	0.5	µA	—
Temperature Sensor (TSN) operating current		I_{TSN}	110	—	µA	—
Low-power Analog Comparator (ACMPLP) operating current	Window comparator (high-speed mode)	I_{ACMPLP}	12.5	25	µA	—
	Comparator (high-speed mode)		6.7	20	µA	—
	Comparator (low-speed mode)		1.86	6	µA	—

Table 2.16 Analog current (2 of 2)

Parameter			Symbol	Typ	Max	Unit	Test conditions
LCD operating current	External resistance division method*3		I_{LCD}*4	0.04	—	µA	fLCD = fSUB (32.768 kHz) LCD clock = 128 Hz (LCDC0 = 0x07) 1/3 bias four-time-slices VCC = 3.0 V VL4 = 3.0 V
	Internal voltage boosting method	VL1 reference VL1AMP enabled (VLCD = 0x04)		0.59	—	µA	
		VL2 reference VL2AMP enabled (VLCD = 0x84)		0.48	—	µA	
	Capacitor split method	VCC reference		0.3	—	µA	
		VL4 reference VL4AMP enabled		0.47	—	µA	
USBFS operating current	Low speed	Operating	I_{USBFS}	1.36	6	mA	—
		Standby		69	200	µA	—
	Full speed	Operating		1.68	8	mA	—
		Standby		551	860	µA	—

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.
Note 3. Not including the current flowing into the external division resistor when using the external resistance division method.
Note 4. Setting 20 pins as the segment function and blinking all

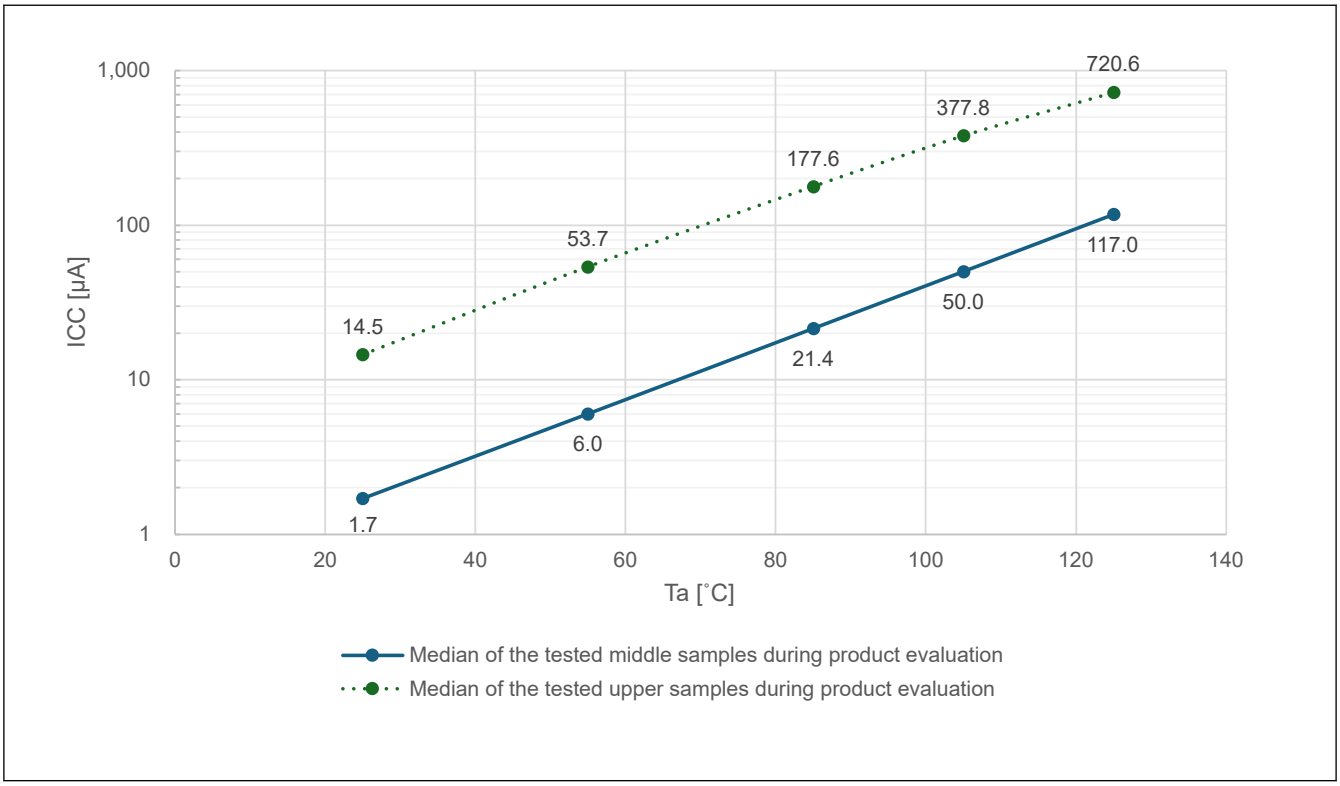
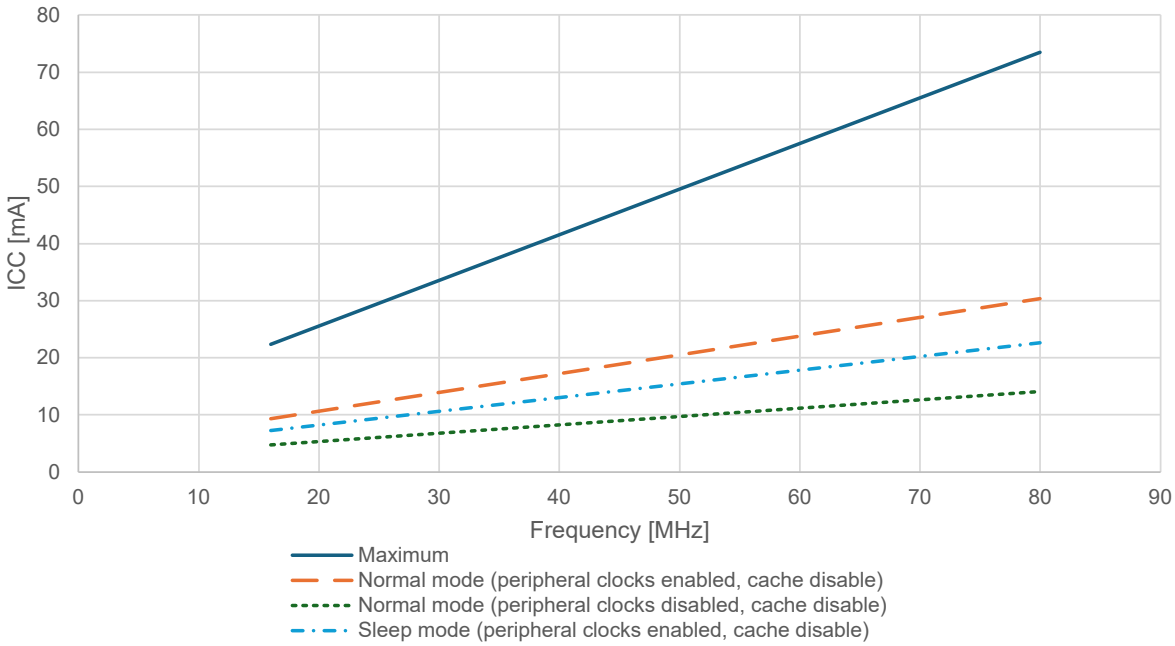
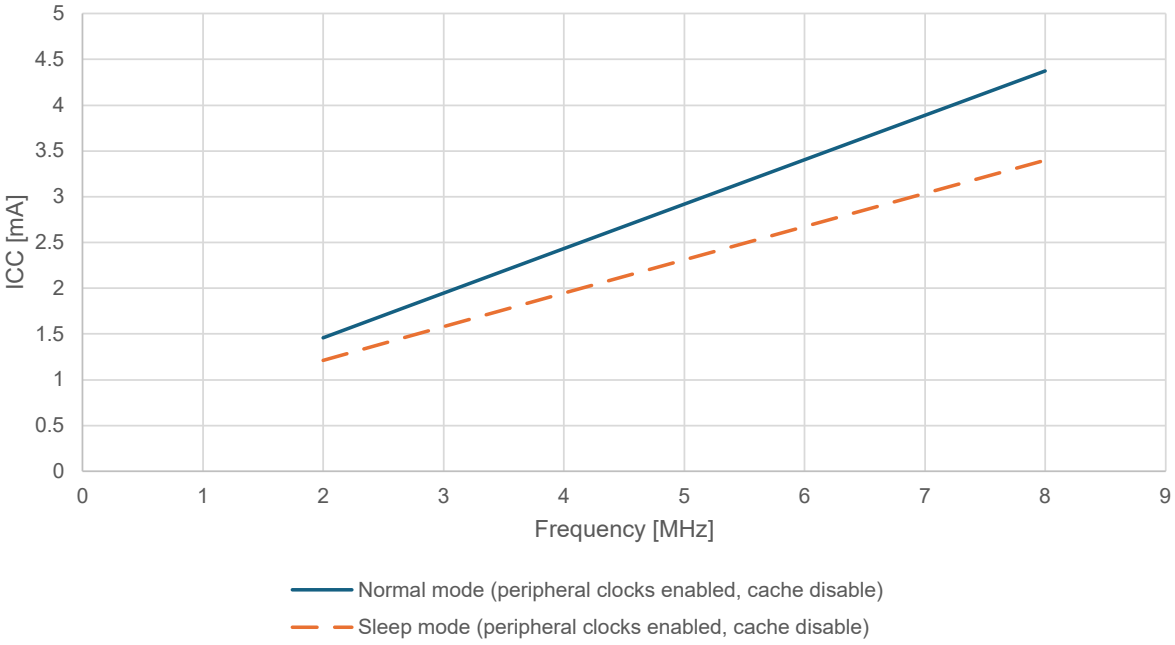


Figure 2.2 Temperature dependency in Software Standby mode (reference data)



Note: Average value of the tested middle samples during product evaluation (typical condition).

Figure 2.3 Frequency dependency in High-speed mode (reference data)



Note: Average value of the tested middle samples during product evaluation (typical condition).

Figure 2.4 Frequency dependency in Middle-speed mode (reference data)

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.17 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 3.6 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI/USB/SWD boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.18 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = 1.6 to 3.6 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.5 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.5 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.5 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

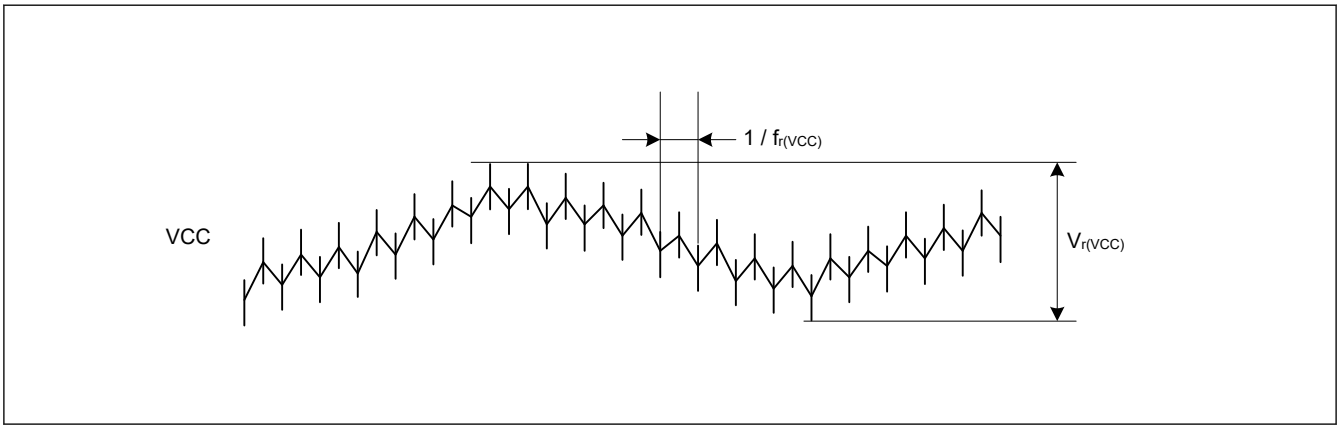


Figure 2.5 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption

  Tj : Junction temperature (°C)

  Ta : Ambient temperature (°C)

  Tt : Top center case temperature (°C)

  θja : Thermal resistance of “Junction”-to-“Ambient” (°C/W)

  Ψjt : Thermal resistance of “Junction”-to-“Top center case” (°C/W)

- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (IOL × VOL) / Voltage + Σ (|IOH| × |VCC – VOH|) / Voltage
- Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

  Cin: Input capacitance

  Cload: Output capacitance

Regarding θja and Ψjt, see Table 2.19.

Table 2.19 Thermal resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal resistance	48-pin QFN	θja	17.7	°C/W	JESD 51-2 and 51-7 compliant
	48-pin LQFP		49.8		
	64-pin LQFP		42.3		
	100-pin LQFP		47.1		
	48-pin QFN	Ψjt	0.05	°C/W	JESD 51-2 and 51-7 compliant
	48-pin LQFP		1.21		
	64-pin LQFP		0.71		
	100-pin LQFP		0.71		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, see the JEDEC standards.

2.2.7.1 Calculation guide of I_{CC}max

Table 2.20 shows the power consumption of each unit.

Table 2.20 Power consumption of each unit (1 of 2)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 25 °C*3	—	—	1.81
			Ta = 55 °C*3	—	—	1.87
			Ta = 75 °C*3	—	—	1.96
			Ta = 85 °C*3	—	—	2.07
			Ta = 95 °C*3	—	—	2.15
			Ta = 105 °C*3	—	—	2.34
			Ta = 115 °C*3	—	—	2.55
			Ta = 125 °C*3	—	—	2.83

Table 2.20 Power consumption of each unit (2 of 2)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	80	84.16	6.73
	Peripheral Unit	Timer	GPT16 (4ch)*4	80	19.02	1.52
			GPT32 (2ch)*4	80	10.87	0.87
			POEG (4 Groups)*4	40	7.45	0.30
			AGT (2ch)*4	40	8.08	0.32
			RTC	40	3.82	0.15
			WDT	40	2.91	0.12
			IWDT	40	1.31	0.05
		Communication interfaces	USBFS	40	35.13	1.41
			SCI (6ch)*4	80	56.32	4.51
			Irda*5	80	10.49	0.84
			IIC	40	6.33	0.25
			I3C	80	30.35	2.43
			CANFD	40	19.97	0.80
			SPI	80	12.31	0.98
			QSPI	80	6.35	0.51
			SSIE	40	8.49	0.34
			UARTA (2ch)*4	40	16.70	0.67
		Analog	ACMPLP (2ch)*4	40	3.41	0.14
			ADC12	80	8.01	0.64
			DAC12	80	2.02	0.16
		Human machine interfaces	CTSU	40	7.08	0.28
			SLCDC	40	9.54	0.38
		Event link	ELC	40	5.25	0.21
		Security	RSIP-E04A	40	300.61	12.02
		Data processing	CRC	80	6.17	0.49
			DOC	80	0.90	0.07
		System	CAC	40	3.24	0.13
		DMA	DMAC (per 1ch)	80	24.96	2.00
			DTC	80	41.83	3.35

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are internal voltage regulator's current and MCU's leakage current. It is selected according to the temperature of Ta.
Note 3. Δ(Tj-Ta) = 20 °C is considered to measure the current.
Note 4. To determine the current consumption per channel, group or unit, divide Current [mA] by the number of channels, groups or units.
Note 5. Includes current for 1 channel of SCI

Table 2.21 shows the outline of operation for each unit.

Table 2.21 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.
AGT	AGT is operating with PCLKB.

Table 2.21 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
RTC	RTC is operating with LOCO.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
USBFS	Transfer type is set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps).
SCI	SCI is transmitting data in clock synchronous mode.
IrDA	SCI is transmitting data in clock asynchronous mode. IrDA is only clear module stop bit.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
I3C	Communication format is set to I3C SDR format. I3C is transmitting data in master mode (5 MHz).
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 32-bit width data.
QSPI	QSPI is issuing Fast Read Quad I/O Instruction.
SSIE	Communication mode is set to Master. System word length is set to 32 bits. Data word length is set to 20 bits. SSIE is transmitting data using I2S format.
UARTA	UARTA is transmitting 8-bit width data.
ACMPLP	ACMPLP is operating.
ADC12	Resolution is set to 12-bit accuracy. Data register is set to A/D-converted value addition mode. ADC12 is converting the analog input in continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
CTSU	CTSU is operating in self-capacitance single scan mode.
SLCDC	SLCDC is operating in A wave, 1/2 bias method, 2-time slice and External resistance division method
ELC	Only clear module stop bit.
RSIP-E04A	RSIP is doing self-test operation.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data comparison mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.3 AC Characteristics

2.3.1 Frequency

Table 2.22 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max[*4]	Unit
Operation frequency	System clock (ICLK)[*1 *2]	1.8 to 3.6 V	f	0.03277	—	80[*5]	MHz
		1.6 to 1.8 V		0.03277	—	4	
	Peripheral module clock (PCLKA)	1.8 to 3.6 V		—	—	80[*5]	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKB)	1.8 to 3.6 V		—	—	40	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKC)[*3]	1.8 to 3.6 V		—	—	48	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)	1.8 to 3.6 V		—	—	80[*5]	
		1.6 to 1.8 V		—	—	4	
	Flash IF clock (FCLK)	1.8V to 3.6V		—	—	48	
		1.6 to 1.8 V		—	—	4	

Note: Set LDOCR.CHG0 = 0 when ICLK < 8MHz, and LDOCR.CHG0 = 1 when 8MHz ≤ ICLK.
Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.26.
Note 5. This is the condition when Tj = 105 °C. Specifications at Tj = 140 °C are 78MHz.

Table 2.23 Operation frequency in middle-speed mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max[*4]	Unit
Operation frequency	System clock (ICLK)[*1 *2]	1.8 to 3.6 V	f	0.03277	—	8	MHz
		1.6 to 1.8 V		0.03277	—	4	
	Peripheral module clock (PCLKA)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKB)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKC)[*3]	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	
	Flash IF clock (FCLK)	1.8 to 3.6 V		—	—	8	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.26.

Table 2.24 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1 *2	1.6 to 3.6 V	f	0.03277	—	1	MHz
	Peripheral module clock (PCLKA)	1.6 to 3.6 V		—	—	1	
	Peripheral module clock (PCLKB)	1.6 to 3.6 V		—	—	1	
	Peripheral module clock (PCLKC)*3	1.6 to 3.6 V		—	—	1	
	Peripheral module clock (PCLKD)	1.6 to 3.6 V		—	—	1	
	FlashIF clock (FCLK)	1.6 to 3.6 V		—	—	1	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.26.

Table 2.25 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 3.6 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKA)	1.6 to 3.6 V		—	—	37.6832	
	Peripheral module clock (PCLKB)	1.6 to 3.6 V		—	—	37.6832	
	Peripheral module clock (PCLKC)	1.6 to 3.6 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2	1.6 to 3.6 V		—	—	37.6832	
	FlashIF clock (FCLK)	1.6 to 3.6 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.26 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.6
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 3.6
		—	—	4		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 3.6
		1	—	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f_{LOCO}	27.853	32.77	37.683	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	μs	Figure 2.7
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—

Table 2.26 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	µs	—
HOCO clock oscillation frequency	f_{HOCO24}	23.76	24	24.24	MHz	—
	f_{HOCO32}	31.68	32	32.32		—
	f_{HOCO40}	39.6	40	40.4		—
	f_{HOCO48}	47.52	48	48.48		—
	f_{HOCO64}	63.36	64	64.64		—
	f_{HOCO80}	79.2	80	80.8		—
HOCO clock oscillation frequency*3	f_{HOCOWT}	—	1.9	—	µs	Figure 2.8
PLL input frequency	f_{PLLIN}	4	—	12.5	MHz	—
PLL clock frequency	f_{PLL}	24	—	80	MHz	—
PLL clock oscillation stabilization time	f_{PLL}	—	—	70	µs	Figure 2.9
Sub-clock oscillator oscillation frequency	f_{SUB}	—	32.77	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 2.10

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

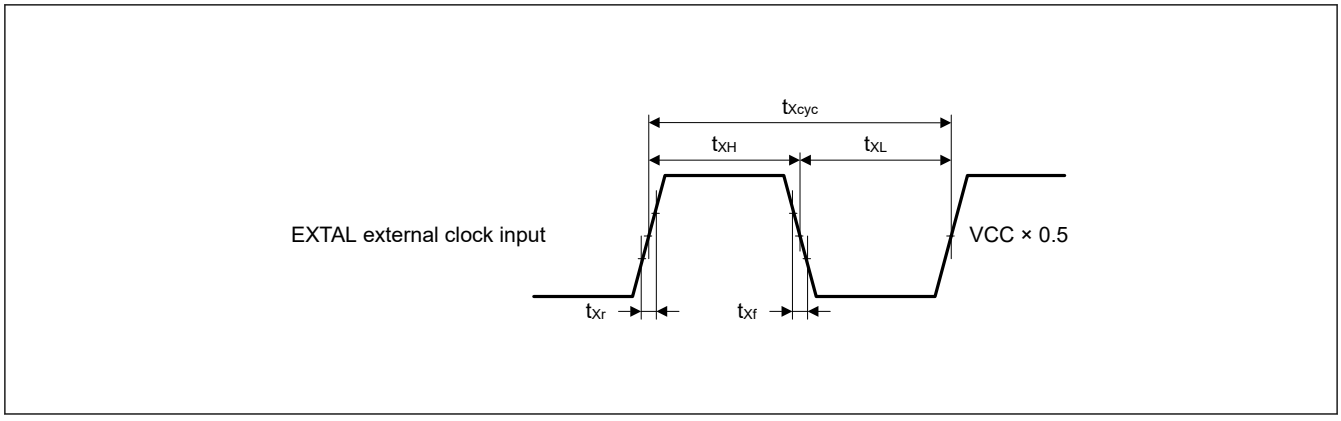


Figure 2.6 EXTAL external clock input timing

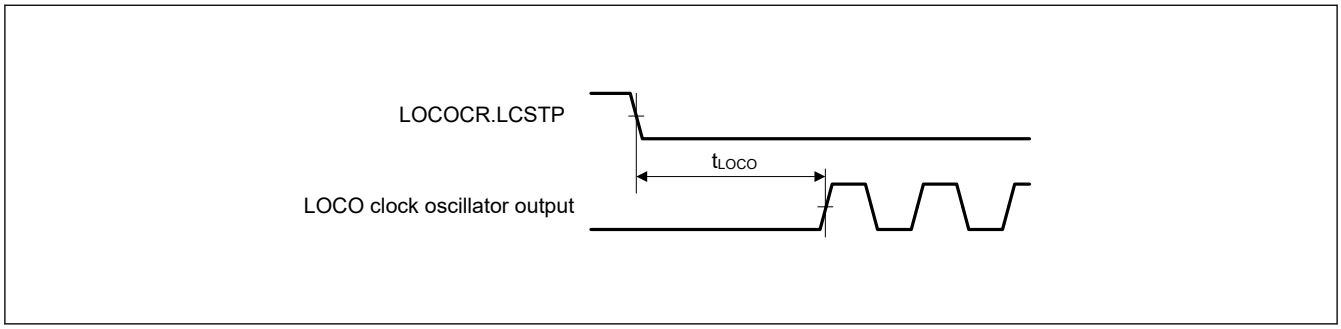


Figure 2.7 LOCO clock oscillation start timing

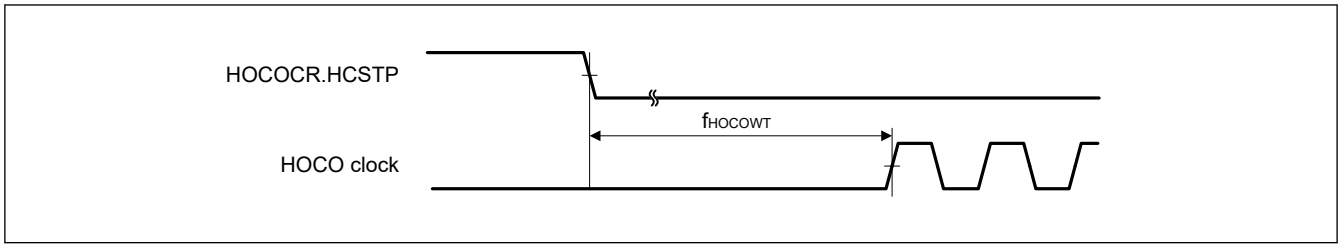


Figure 2.8 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

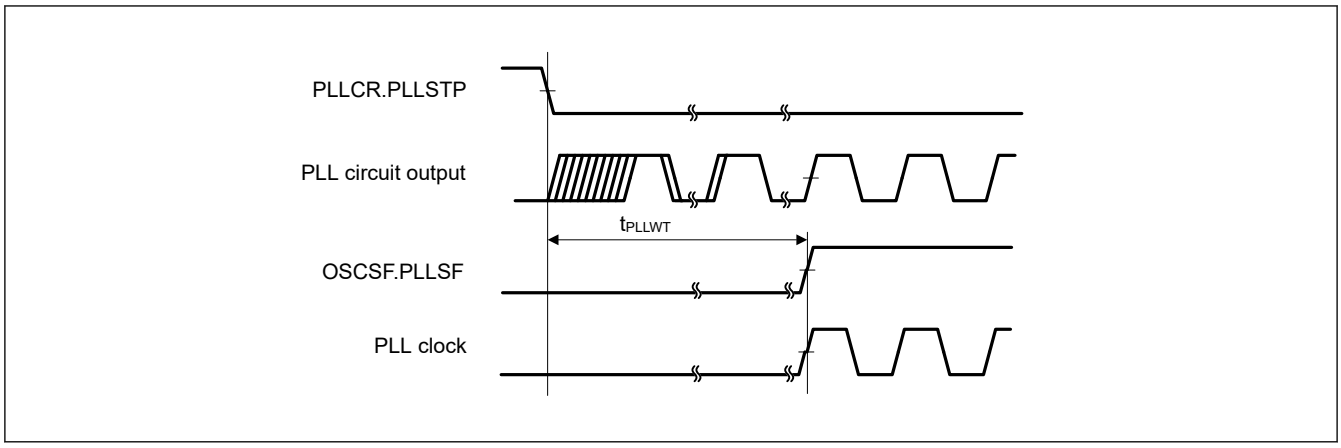


Figure 2.9 PLL clock oscillation start timing (PLL is Operated after Main Clock Oscillation Has Settled)

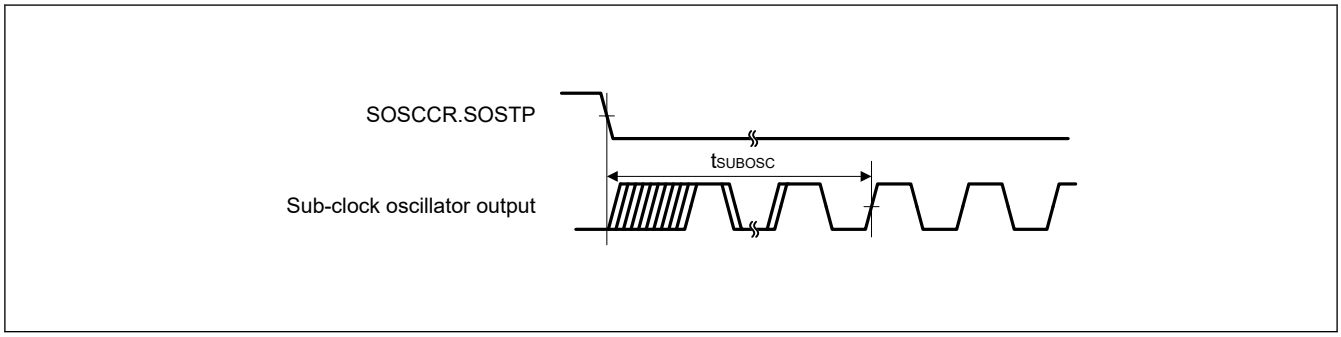


Figure 2.10 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.27 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	13	—	—	ms	Figure 2.11
	Not at power-on	t_{RESW}	30	—	—	μs	Figure 2.12
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	1.0	—	ms	Figure 2.11
	LVD0 disabled*2		—	0.3	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.12
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (IWDT reset, WDT reset, RAM parity error reset, RAM ECC error reset, Bus master MPU error reset, TrustZone error reset, Cache parity error reset, Software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.13
	LVD0 disabled*2		—	0.2	—		

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

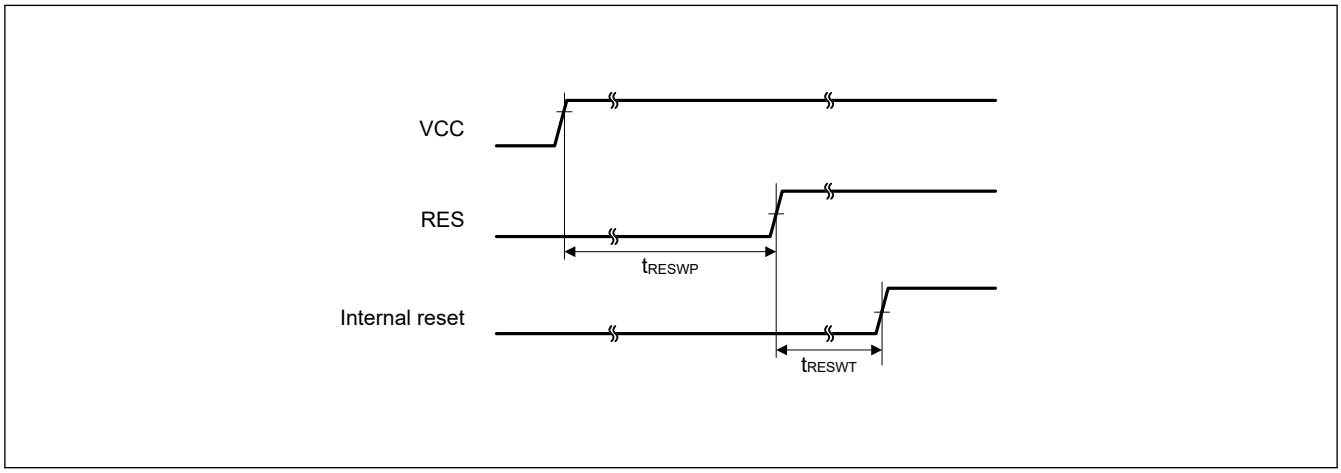


Figure 2.11 Reset input timing at power-on

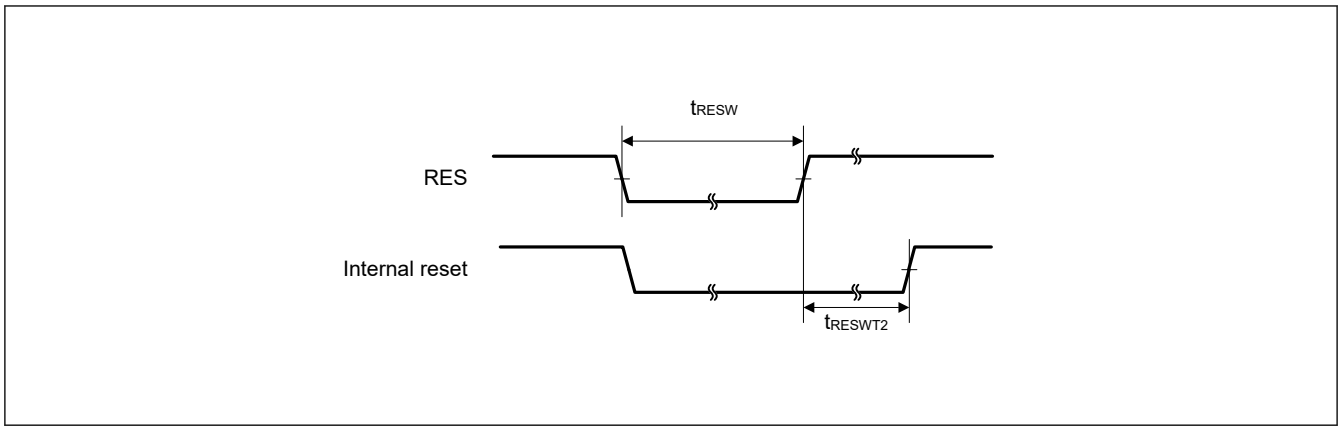


Figure 2.12 Reset input timing (1)

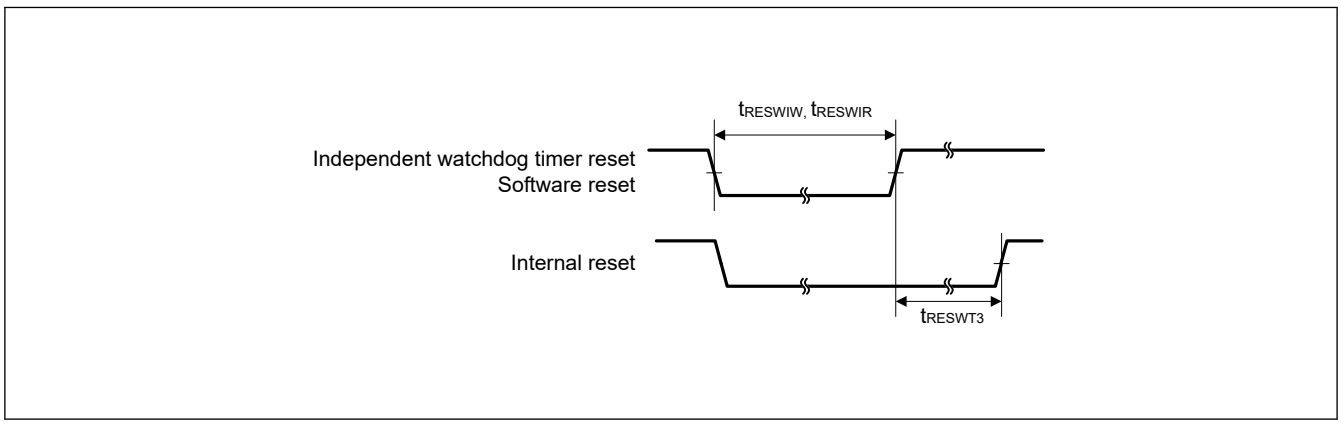


Figure 2.13 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.28 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2 *4	t_{SBYMC}	—	2.1	2.7	ms	Figure 2.14
			System clock source is PLL (48 MHz) with Main clock oscillator*2 *5	t_{SBYPC}	—	2.1	2.8	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 *4	t_{SBYEX}	—	8.5	11	µs	
			System clock source is PLL (48 MHz) with Main clock oscillator*3 *5	t_{SBYEX}	—	66	85	µs	
		System clock source is HOCO (HOCO clock is 32 MHz)*6		t_{SBYHO}	—	13.5	17.8	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)*5		t_{SBYHO}	—	13.2	17.5	µs	
		System clock source is MOCO (8 MHz)*7		t_{SBYMO}	—	3.5	5.1	µs	

Note 1. The division ratio of ICLK, FCLK, and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The ICLK is 20 MHz
Note 5. The ICLK is 48 MHz
Note 6. The ICLK is 32 MHz
Note 7. The ICLK is 8 MHz

Table 2.29 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2 *4	t_{SBYMC}	—	2.1	2.7	ms	Figure 2.14
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 *4 VCC = 1.8 V to 3.6 V	t_{SBYEX}	—	6	7.4	µs	
			System clock source is main clock oscillator (4 MHz)*3 *5 VCC = 1.6 V to 1.8 V		—	7.3	8.8	µs	
		System clock source is HOCO (32 MHz) *4	VCC = 1.8 V to 3.6 V*6	t_{SBYHO}	—	10	13	µs	
			VCC = 1.6 V to 1.8 V*7		—	13	16		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 3.6 V*8	t_{SBYMO}	—	3.5	5.1	µs	
			VCC = 1.6 V to 1.8 V*9		—	6.3	8.7		

Note 1. The division ratio of ICLK, FCLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The ICLK is 5 MHz (20 MHz/4)
Note 5. The ICLK is 4 MHz
Note 6. The ICLK is 8 MHz (32 MHz/4)
Note 7. The ICLK is 4 MHz (32 MHz/8)
Note 8. The ICLK is 8 MHz
Note 9. The ICLK is 4 MHz (8 MHz/2)

Table 2.30 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2 *4	t_{SBYMC}	—	2.1	2.7	ms	Figure 2.14
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 *4	t_{SBYEX}	—	41	46	µs	
		System clock source is MOCO (8 MHz)*5		t_{SBYMO}	—	23	30	µs	

Note 1. The division ratio of ICLK, FCLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The ICLK is 0.625 MHz (20/32 MHz)
Note 5. The ICLK is 1 MHz (8 MHz/8)

Table 2.31 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.8	0.9	ms	Figure 2.14
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.8	1	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

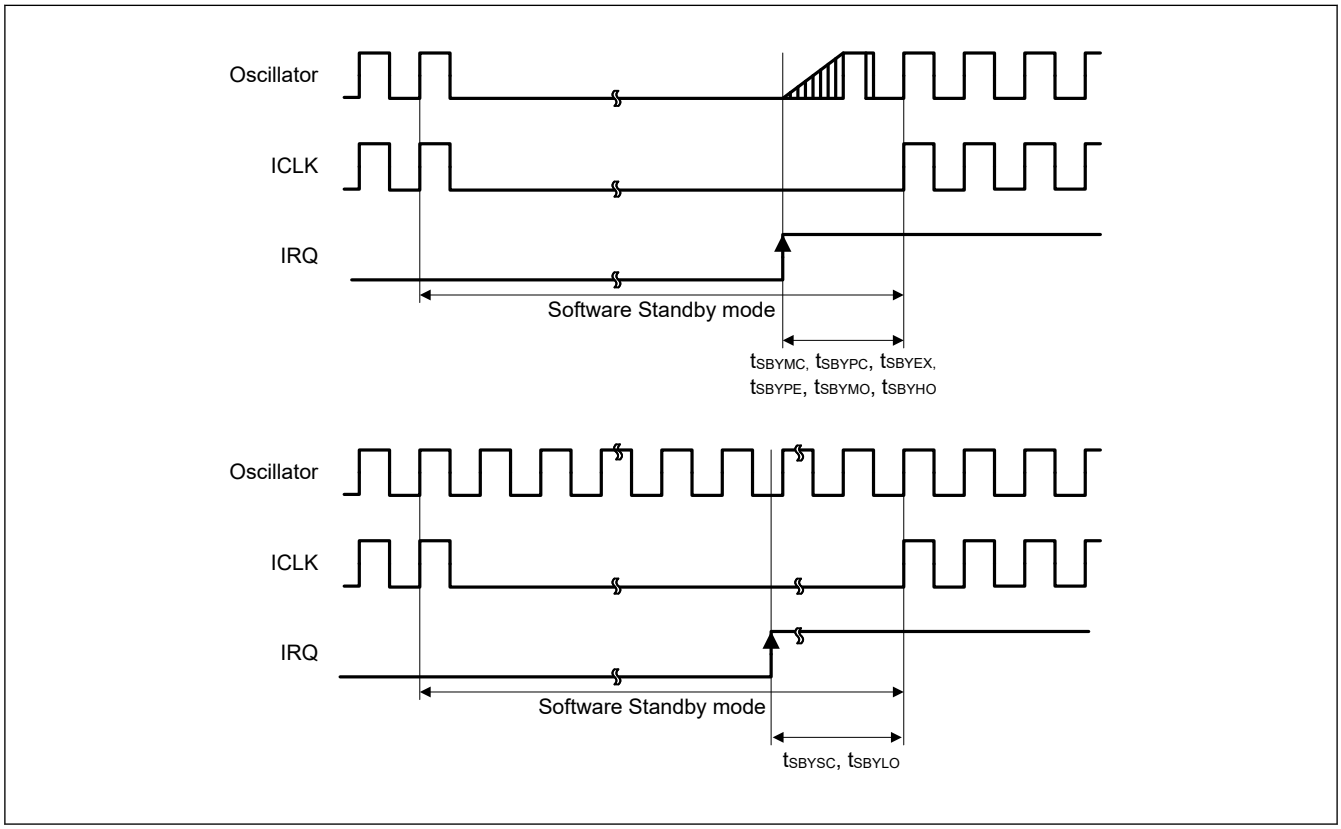
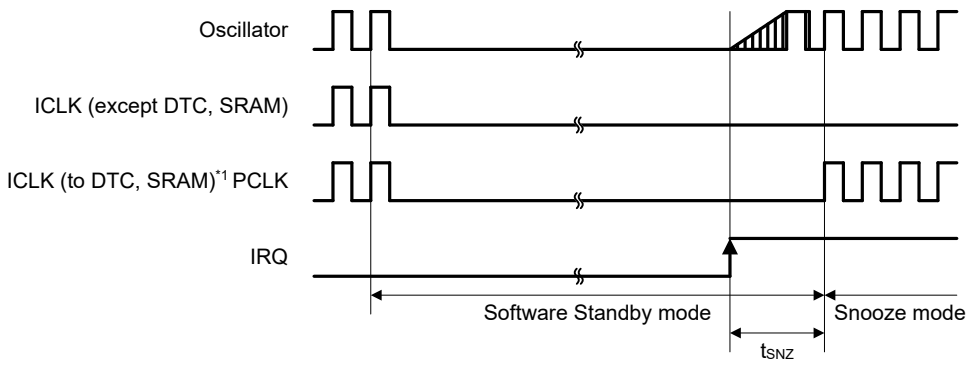


Figure 2.14 Software Standby mode cancellation timing

Table 2.32 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode System clock source is HOCO (32 MHz)*1	t_{SNZ}	—	7.4	9.3	µs	Figure 2.15
	Middle-speed mode System clock source is HOCO (24 MHz)*2 VCC = 1.8 V to 3.6 V	t_{SNZ}	—	8.3	10.4	µs	
	Middle-speed mode System clock source is HOCO (24 MHz)*3 VCC = 1.6 V to 1.8 V	t_{SNZ}	—	9.5	11.8	µs	
	Low-speed mode System clock source is MOCO (8 MHz)*4	t_{SNZ}	—	11.8	15.6	µs	

Note 1. The ICLK is 32 MHz
Note 2. The ICLK is 8 MHz (24 MHz/4)
Note 3. The ICLK is 4 MHz (24 MHz/8)
Note 4. The ICLK is 1 MHz (8 MHz/8)



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.15 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.33 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.

Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

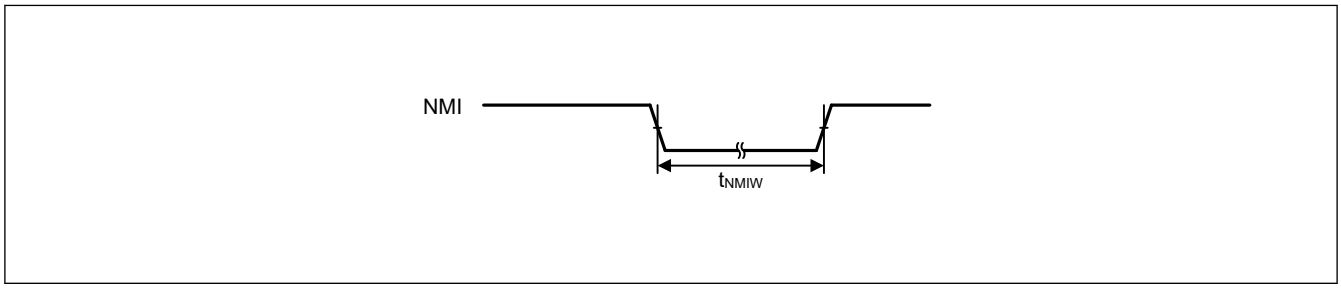


Figure 2.16 NMI interrupt input timing

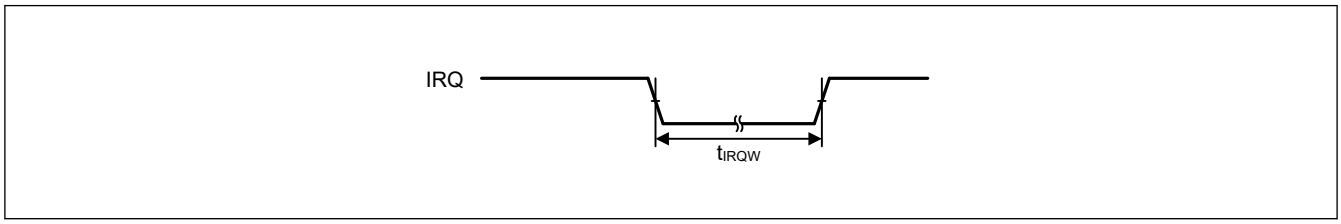


Figure 2.17 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.34 I/O Ports, POEG, GPT, AGT, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 3.6 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.18
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.19
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.20
		Dual edge		2.5	—		
AGT	AGTIO, AGTEE input cycle	1.8 V ≤ VCC ≤ 3.6 V	t_{ACYC}*1	250	—	ns	Figure 2.21
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO, AGTEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 3.6 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 3.6 V	t_{ACYC2}	62.5	—	ns	Figure 2.21
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.22

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

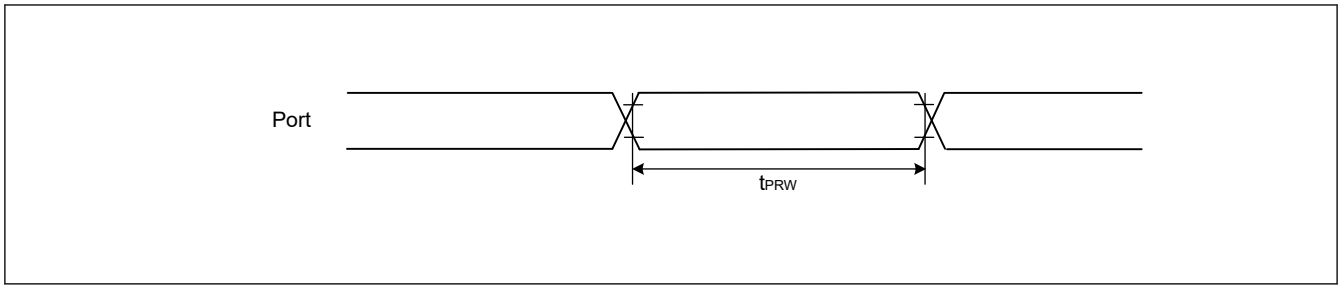


Figure 2.18 I/O ports input timing

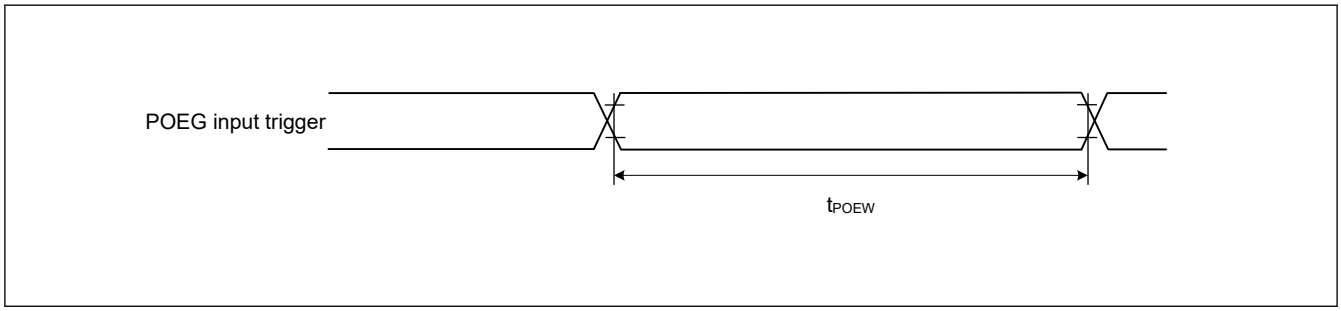


Figure 2.19 POEG input trigger timing

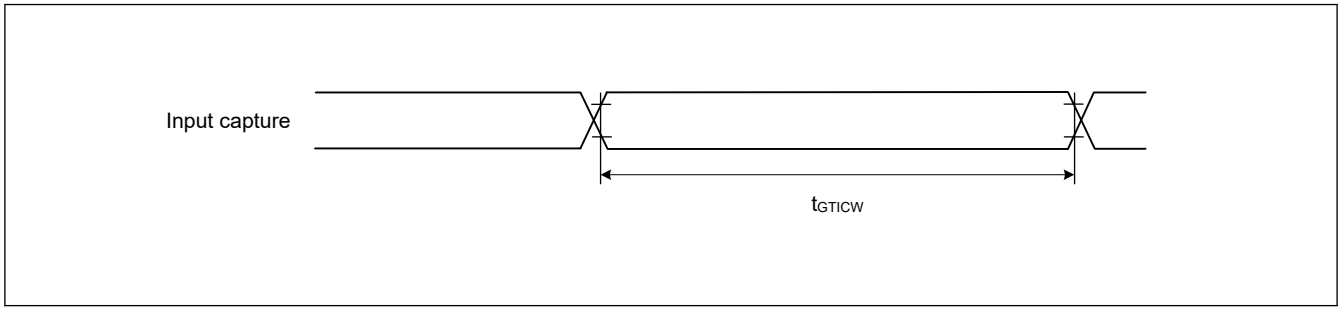


Figure 2.20 GPT input capture timing

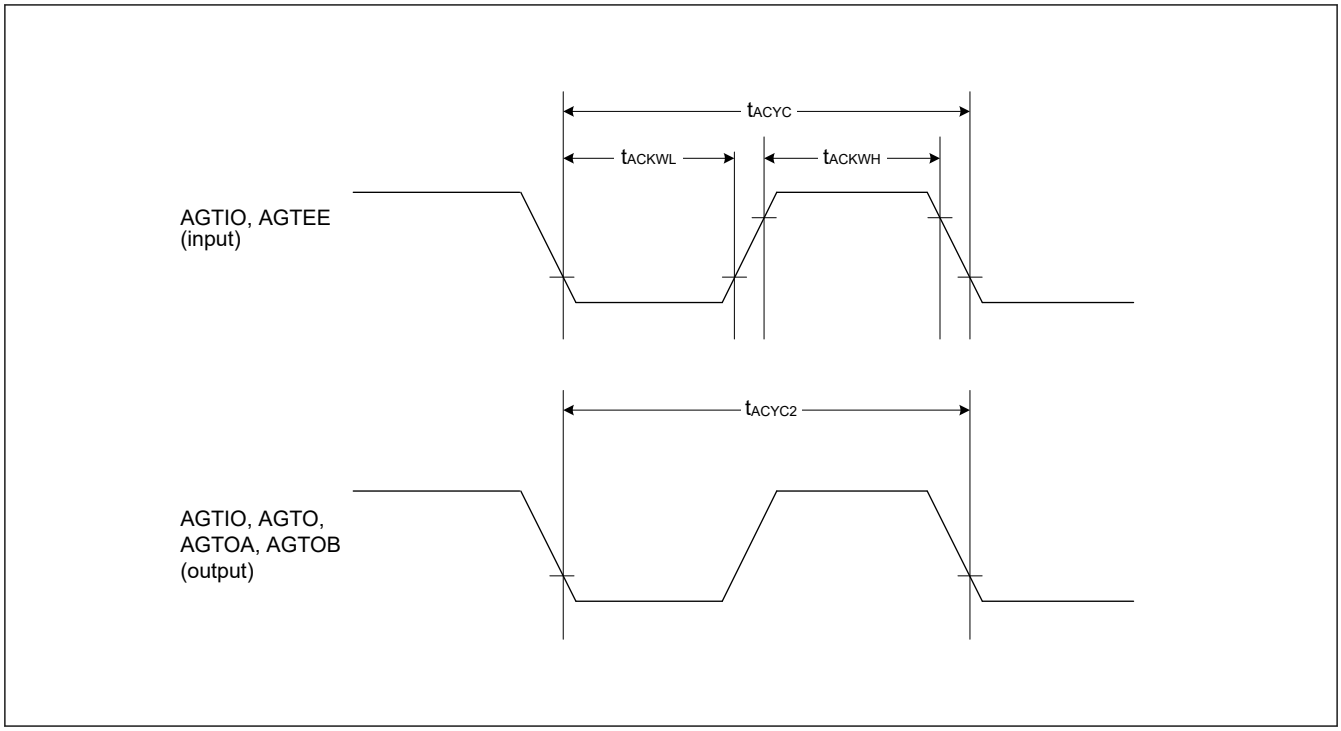


Figure 2.21 AGT I/O timing

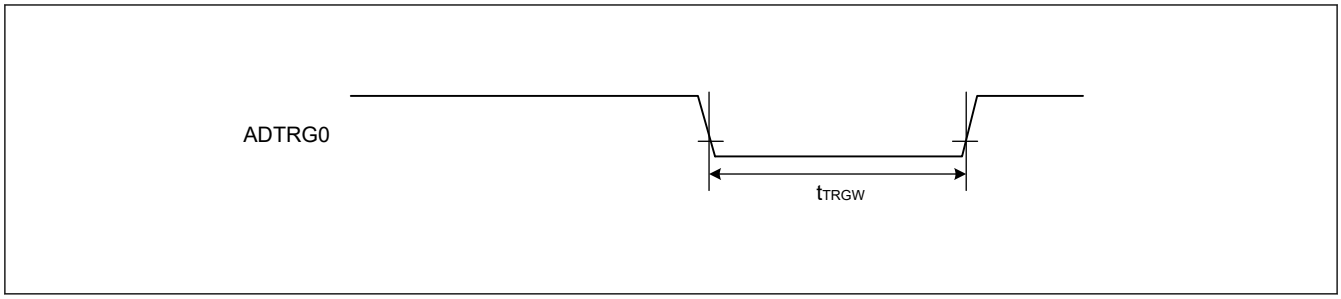


Figure 2.22 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.35 CAC timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
CACREF input pulse width	$t_{PBcyc} \leq t_{CAC}$*1	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{PBcyc}	—	—	ns	—
	$t_{PBcyc} > t_{CAC}$*1		5 × t_{CAC} + 6.5 × t_{PBcyc}	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{CAC}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.36 SCI timing (1) (1 of 2)

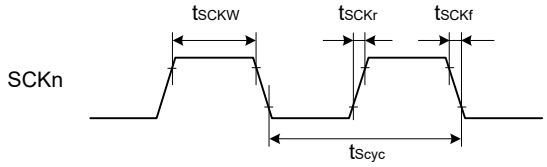
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 3.6 V	t_{Scyc}	75	—	ns	Figure 2.23
			2.4 V ≤ VCC < 2.7 V		150	—		
			1.8 V ≤ VCC < 2.4 V		300	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 3.6 V		100	—		
			2.4 V ≤ VCC < 2.7 V		200	—		
			1.8 V ≤ VCC < 2.4 V		400	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	10	ns	
	Input clock fall time			t_{SCKf}	—	10	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 3.6 V	t_{Scyc}	75 (exclude SCI1) 100 (SCI1)	—	ns	
			2.4 V ≤ VCC < 2.7 V		150 (exclude SCI1) 200 (SCI1)	—		
			1.8 V ≤ VCC < 2.4 V		300 (exclude SCI1) 400 (SCI1)	—		
			1.6 V ≤ VCC < 1.8 V		1500 (exclude SCI1) 2000 (SCI1)	—		
		Clock synchronous	1.8 V ≤ VCC ≤ 3.6 V		75	—		
			2.4 V ≤ VCC < 2.7 V		150	—		
			1.8 V ≤ VCC < 2.4 V		300	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 3.6 V	t_{SCKr}	—	7.5	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 3.6 V	t_{SCKf}	—	7.5	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 3.6 V	t_{TXD}	—	30	ns	Figure 2.24
			2.4 V ≤ VCC < 2.7 V		—	35		
			1.8 V ≤ VCC < 2.4 V		—	75		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Transmit data delay time (slave)	Clock synchronous	1.8 V ≤ VCC ≤ 3.6 V		—	40	ns	
			2.4 V ≤ VCC < 2.7 V		—	45		
			1.8 V ≤ VCC < 2.4 V		—	70		
			1.6 V ≤ VCC < 1.8 V		—	105		

Table 2.36 SCI timing (1) (2 of 2)

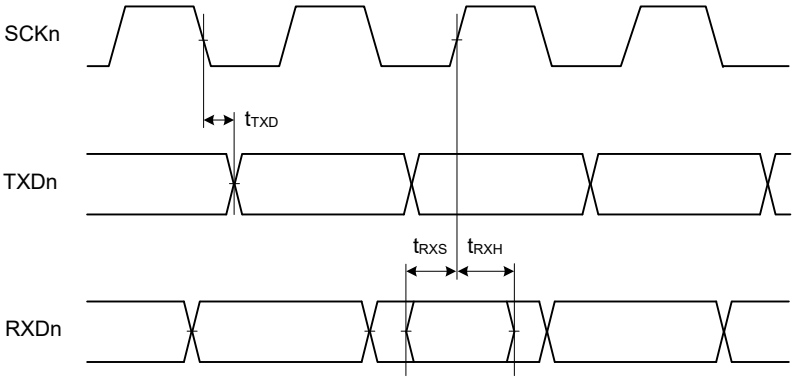
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Receive data setup time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 3.6 V	t_{RXS}	40	—	ns	Figure 2.24
			2.4 V ≤ VCC < 2.7 V		50	—		
			1.8 V ≤ VCC < 2.4 V		70	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Receive data setup time (slave)	Clock synchronous	2.4 V ≤ VCC ≤ 3.6 V		10	—	ns	
			1.8 V ≤ VCC ≤ 2.4 V		15	—		
			1.6 V ≤ VCC < 1.8 V		45	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	5	—	ns	



Note: n = 0, 1, 3 to 5, 9

Figure 2.23 SCK clock input timing



Note: n = 0, 1, 3 to 5, 9

Figure 2.24 SCI input/output timing in clock synchronous mode

Table 2.37 SCI timing (2) (1 of 2)

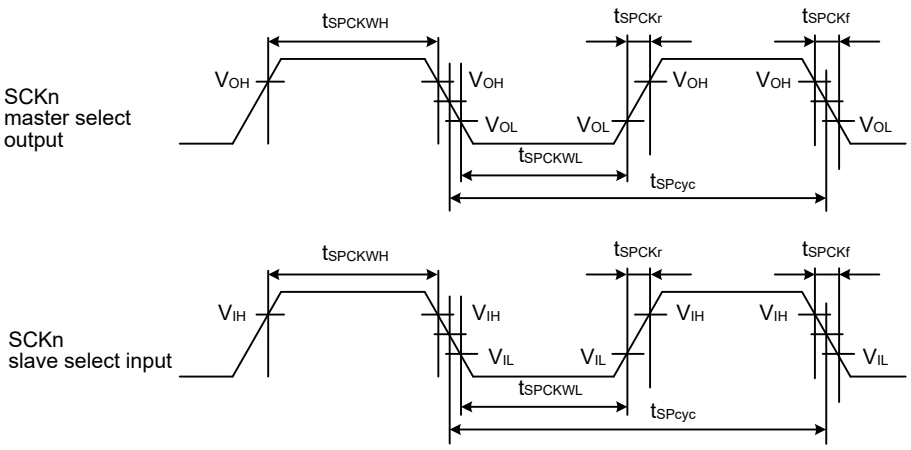
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter				Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		1.8 V ≤ VCC ≤ 3.6 V	t_{SPcyc}	75	—	ns	Figure 2.25
			2.4 V ≤ VCC < 2.7 V		150	—		
			1.8 V ≤ VCC < 2.4 V		300	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		1.8 V ≤ VCC ≤ 3.6 V		100	—		
			2.4 V ≤ VCC < 2.7 V		200	—		
			1.8 V ≤ VCC < 2.4 V		400	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time			t_{SPCKr}, t_{SPCKf}	—	10	ns	
	Data input setup time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	40	—	ns	Figure 2.26 to Figure 2.29
			2.4 V ≤ VCC < 2.7 V		50	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	1.8 V ≤ VCC ≤ 3.6 V		10	—		
			1.6 V ≤ VCC < 1.8 V		45	—		
	Data input hold time	Master		t_H	5	—	ns	
		Slave			18	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	2.4 V ≤ VCC ≤ 3.6 V	t_{OD}	—	35	ns	
			2.4 V ≤ VCC ≤ 2.7 V		—	35		
			1.8 V ≤ VCC ≤ 2.4 V		—	75		
			1.6 V ≤ VCC < 1.8 V		—	125		
		Slave	2.7 V ≤ VCC ≤ 3.6 V		—	40		
			2.4 V ≤ VCC ≤ 2.7 V		—	40		
			1.8 V ≤ VCC < 2.4 V		—	45		
			1.6 V ≤ VCC < 1.8 V		—	100		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{OH}	-5	—	ns	
			2.4 V ≤ VCC < 2.7 V		-10	—		
			1.8 V ≤ VCC < 2.4 V		-20	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-5	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 3.6 V	t_{Dr}, t_{Df}	—	5	ns	
		Slave	1.8 V ≤ VCC ≤ 3.6 V		—	5		

Table 2.37 SCI timing (2) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

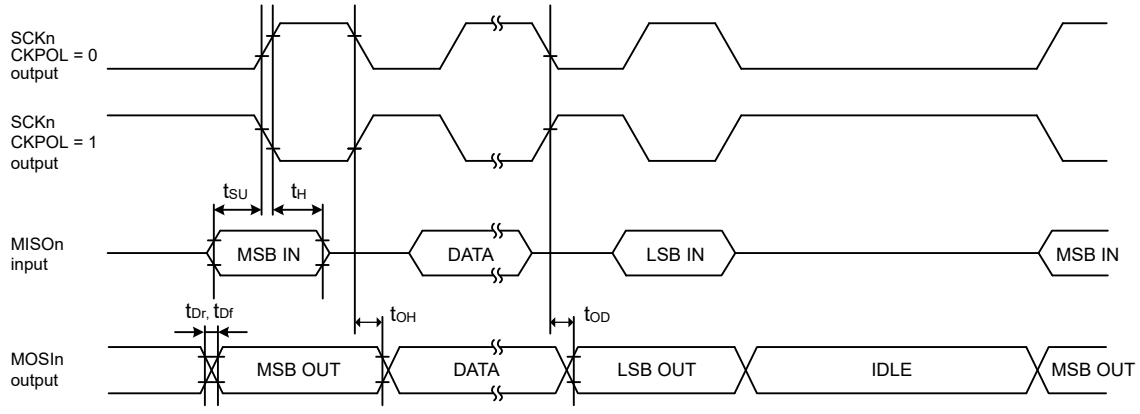
Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	Slave access time	2.7 V ≤ VCC ≤ 3.6 V	t_{SA}	—	8	t_{Pcyc}	Figure 2.26 to Figure 2.29
		2.4 V ≤ VCC < 2.7 V		—	9		
		1.8 V ≤ VCC < 2.4 V		—	13		
		1.6 V ≤ VCC < 1.8 V		—	6		
	Slave output release time	1.8 V ≤ VCC ≤ 3.6 V	t_{REL}	—	8	t_{Pcyc}	
		2.4 V ≤ VCC < 2.7 V		—	9		
		1.8 V ≤ VCC < 2.4 V		—	13		
		1.6 V ≤ VCC < 1.8 V		—	6		



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

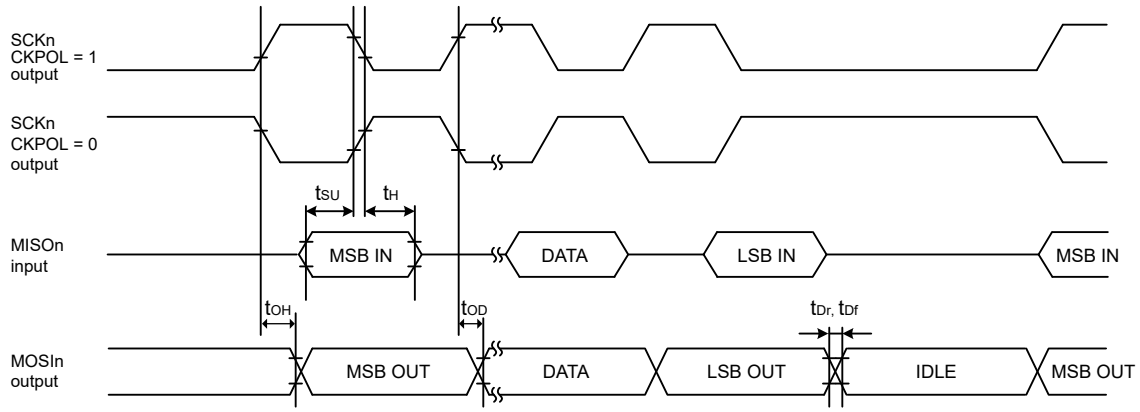
Note: n = 0, 1, 3 to 5, 9

Figure 2.25 SCI simple SPI mode clock timing



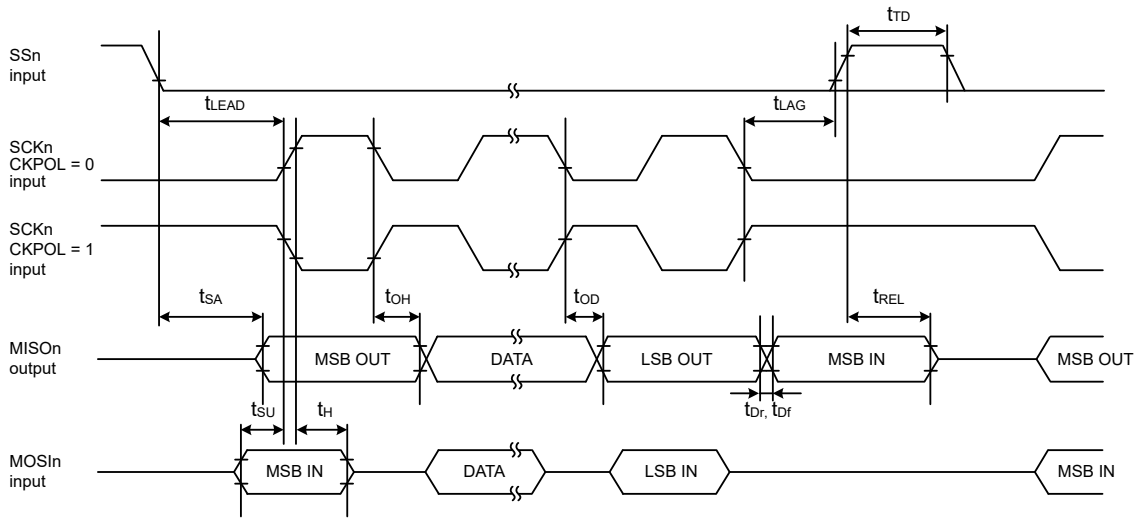
Note: n = 0, 1, 3 to 5, 9

Figure 2.26 SCI simple SPI mode timing (master, CKPH = 1)



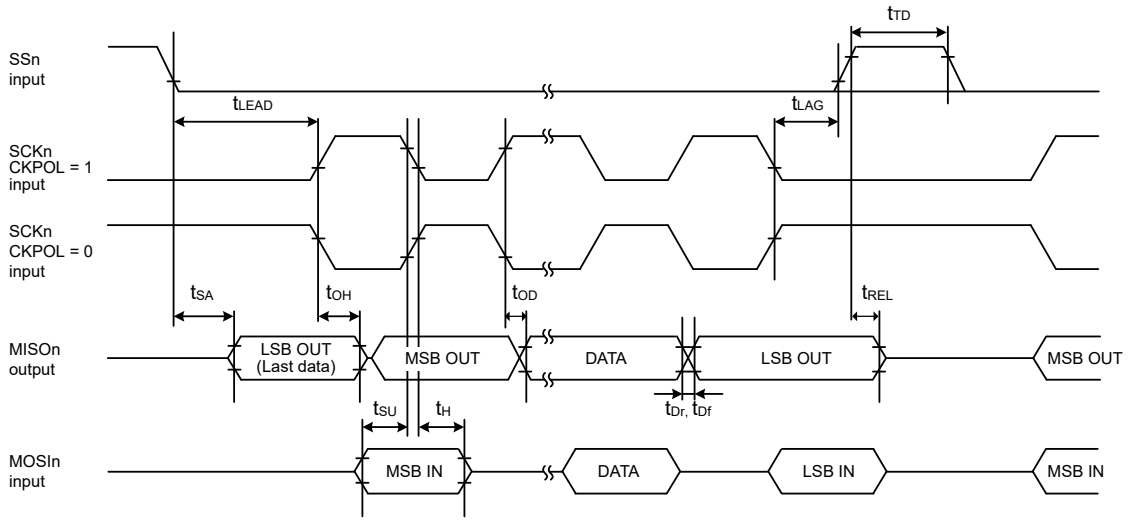
Note: n = 0, 1, 3 to 5, 9

Figure 2.27 SCI simple SPI mode timing (master, CKPH = 0)



Note: n = 0, 1, 3 to 5, 9

Figure 2.28 SCI simple SPI mode timing (slave, CKPH = 1)



Note: n = 0, 1, 3 to 5, 9

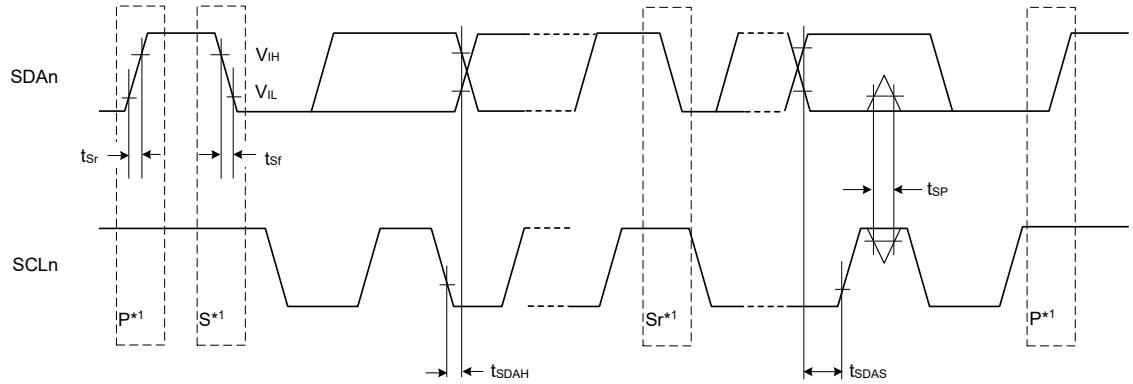
Figure 2.29 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.38 SCI timing (3)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.30
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.30
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 1, 3 to 5, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.30 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.39 SPI timing (1 of 3)

Parameter			Symbol	Min	Max	Unit	Test conditions
RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{SPcyc} *1	50	—	ns	Figure 2.31 C = 30 pF
		2.4 V ≤ VCC < 2.7 V		100	—		
		1.8 V ≤ VCC < 2.4 V		200	—		
		1.6 V ≤ VCC < 1.8 V		500	—		
	Slave	2.7 V ≤ VCC ≤ 3.6 V		100	—		
		2.4 V ≤ VCC < 2.7 V		200	—		
		1.8 V ≤ VCC < 2.4 V		400	—		
		1.6 V ≤ VCC < 1.8 V		1500	—		
RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
	Slave			0.4 × t_{SPcyc}	0.6 × t_{SPcyc}		
RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
	Slave			0.4 × t_{SPcyc}	0.6 × t_{SPcyc}		
RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 3.6 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
		2.4 V ≤ VCC < 2.7 V		—	15		
		1.8 V ≤ VCC ≤ 2.4 V		—	20		
		1.6 V ≤ VCC < 1.8 V		—	30		
	Input			—	1	µs	

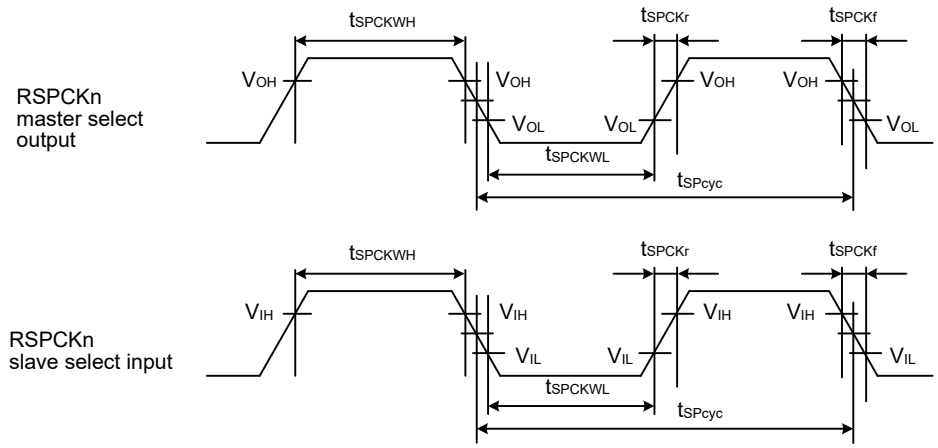
Table 2.39 SPI timing (2 of 3)

Parameter			Symbol	Min	Max	Unit	Test conditions
Data input setup time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{SU}	20	—	ns	Figure 2.32 to Figure 2.37 C = 30 pF
		2.4 V ≤ VCC < 2.7 V		22	—		
		1.8 V ≤ VCC < 2.4 V		37	—		
		1.6 V ≤ VCC < 1.8 V		10	—		
	Slave	2.4 V ≤ VCC ≤ 3.6 V		10	—		
		1.8 V ≤ VCC < 2.4 V		15	—		
		1.6 V ≤ VCC < 1.8 V		20	—		
Data input hold time	Master (RSPCK is PCLKA/2)		t_{HF}	0	—	ns	
	Master (RSPCK is not PCLKA/2)		t_{H}	t_{Pcyc}	—		
	Slave		t_{H}	20	—		
SSL setup time	Master	1.8 V ≤ VCC ≤ 3.6 V	t_{LEAD}	$-30 + N \times t_{Spcyc}$ *1	—	ns	
		1.6 V ≤ VCC < 1.8 V		$-50 + N \times t_{Spcyc}$ *1	—		
	Slave			$6 \times t_{Pcyc}$	—	ns	
SSL hold time	Master		t_{LAG}	$-30 + N \times t_{Spcyc}$ *2	—	ns	
	Slave			$6 \times t_{Pcyc}$	—	ns	
Data output delay time	Master	2.7 V ≤ VCC ≤ 3.6 V	t_{OD}	—	14	ns	
		2.4 V ≤ VCC < 2.7 V		—	14		
		1.8 V ≤ VCC < 2.4 V		—	14		
		1.6 V ≤ VCC < 1.8 V		—	14		
	Slave	2.7 V ≤ VCC ≤ 3.6 V		—	41		
		2.4 V ≤ VCC < 2.7 V		—	45		
		1.8 V ≤ VCC < 2.4 V		—	65		
		1.6 V ≤ VCC < 1.8 V		—	82		
Data output hold time	Master		t_{OH}	0	—	ns	
	Slave			0	—		
Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
	Slave			$4 \times t_{SPcyc}$	—		
MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 3.6 V	t_{Dr}, t_{Df}	—	5	ns	Figure 2.32 to Figure 2.37 C = 30 pF
		2.4 V ≤ VCC < 2.7 V		—	15		
		1.8 V ≤ VCC < 2.4 V		—	20		
		1.6 V ≤ VCC < 1.8 V		—	30		
	Input			—	1		
SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 3.6 V	t_{SSLr}, t_{SSLf}	—	5	ns	
		2.4 V ≤ VCC < 2.7 V		—	15		
		1.8 V ≤ VCC < 2.4 V		—	20		
		1.6 V ≤ VCC < 1.8 V		—	30		
	Input			—	1		

Table 2.39 SPI timing (3 of 3)

Parameter		Symbol	Min	Max	Unit	Test conditions
Slave access time	2.7 V ≤ VCC ≤ 3.6 V	t_{SA}	—	2 × t_{Pcyc} + 11	ns	Figure 2.36 and Figure 2.37 C = 30 pF
	2.4 V ≤ VCC < 2.7 V		—	2 × t_{Pcyc} + 15		
	1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 35		
	1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 55		
Slave output release time	2.7 V ≤ VCC ≤ 3.6 V	t_{REL}	—	2 × t_{Pcyc} + 11	ns	
	2.4 V ≤ VCC < 2.7 V		—	2 × t_{Pcyc} + 15		
	1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 35		
	1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 55		

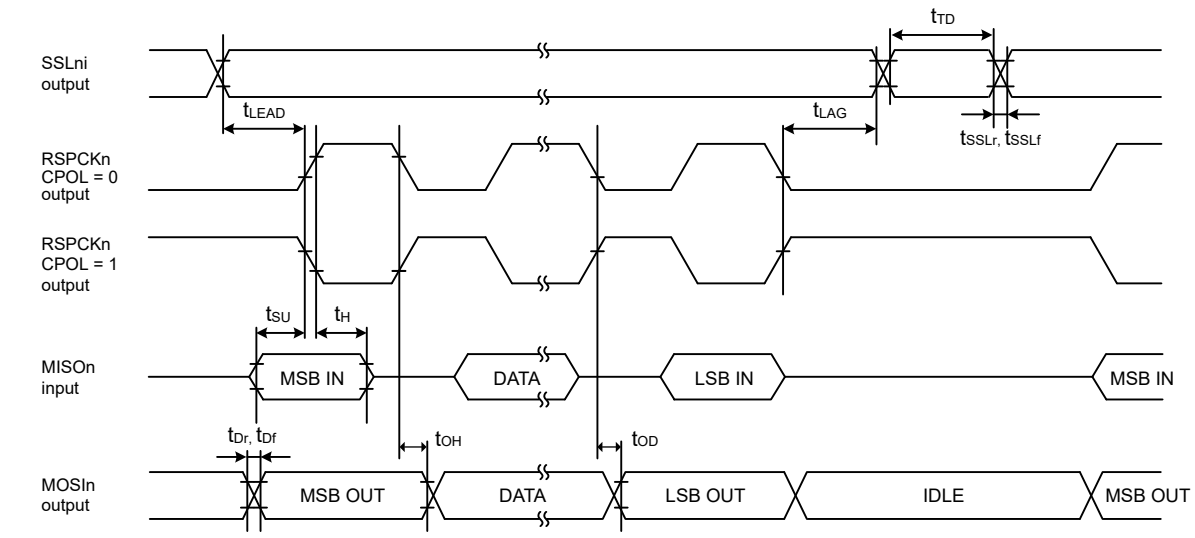
Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set as an integer from 1 to 8 by the SPCKD register.
Note 2. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

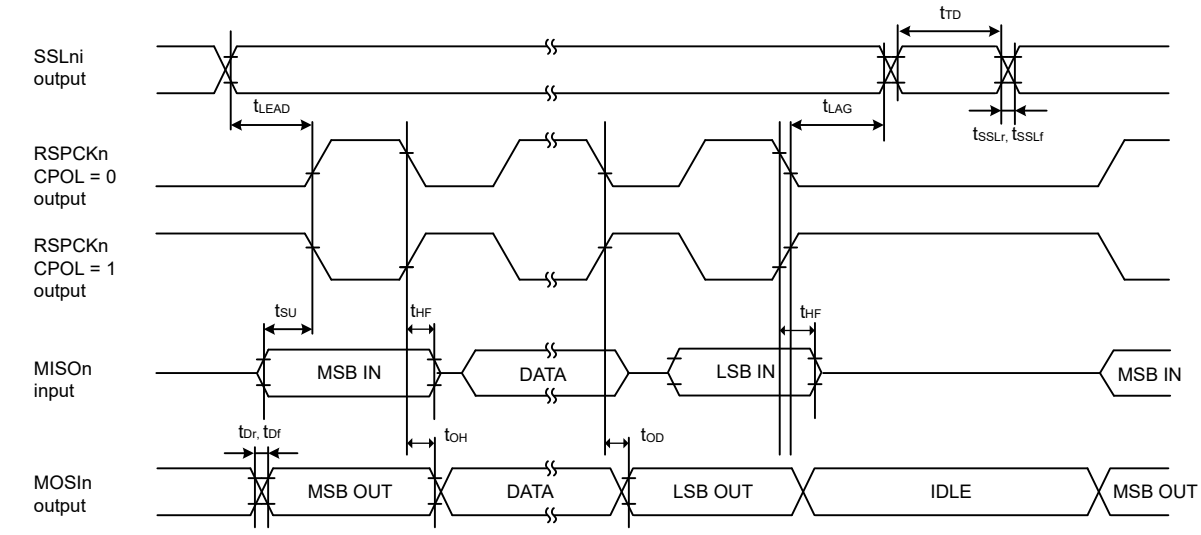
Note: n = A or B

Figure 2.31 SPI clock timing



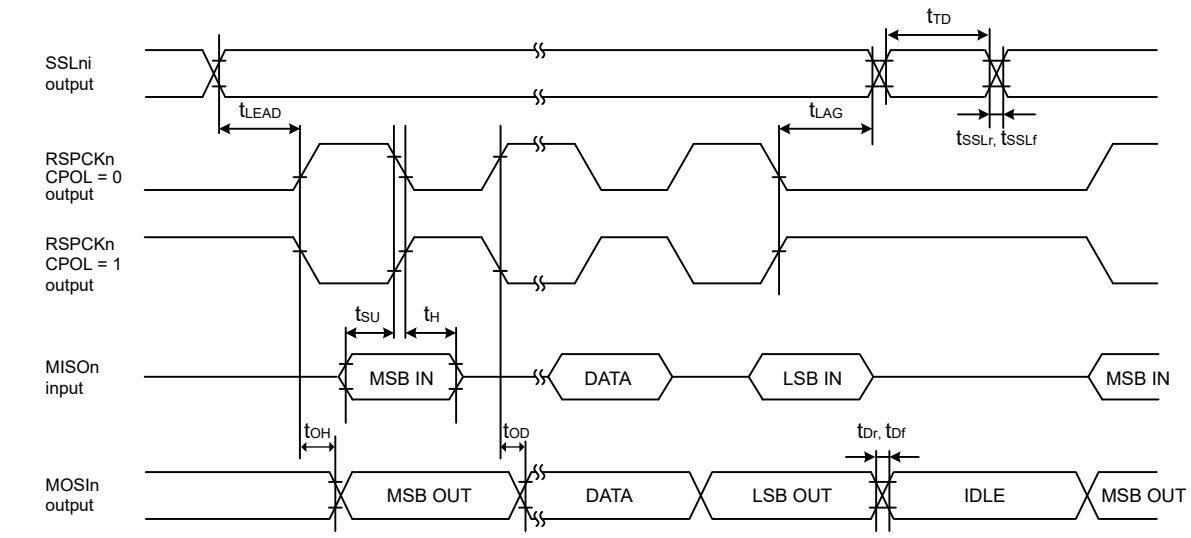
Note: n = A or B
i = 0

Figure 2.32 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)



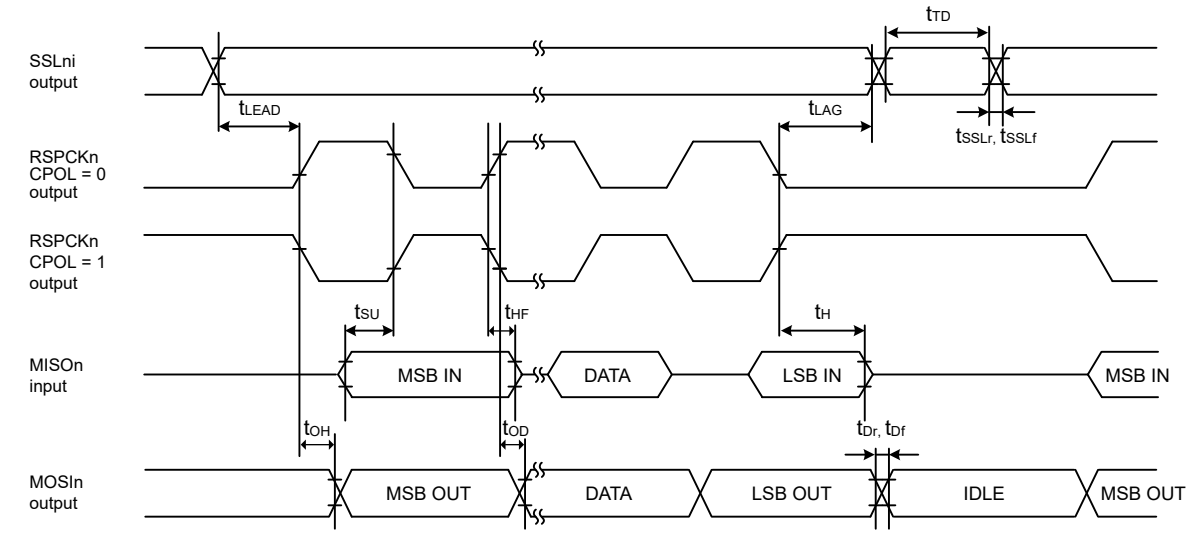
Note: n = A or B
i = 0

Figure 2.33 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)



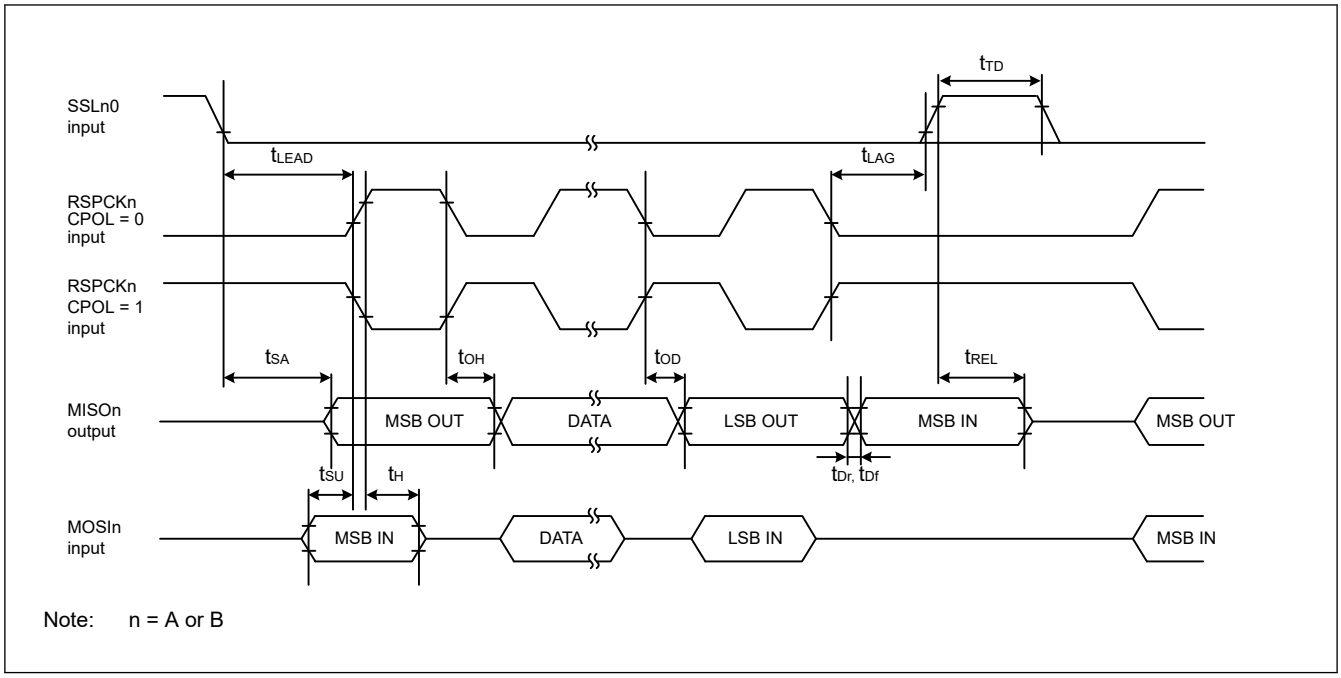
Note: n = A or B
i = 0

Figure 2.34 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)



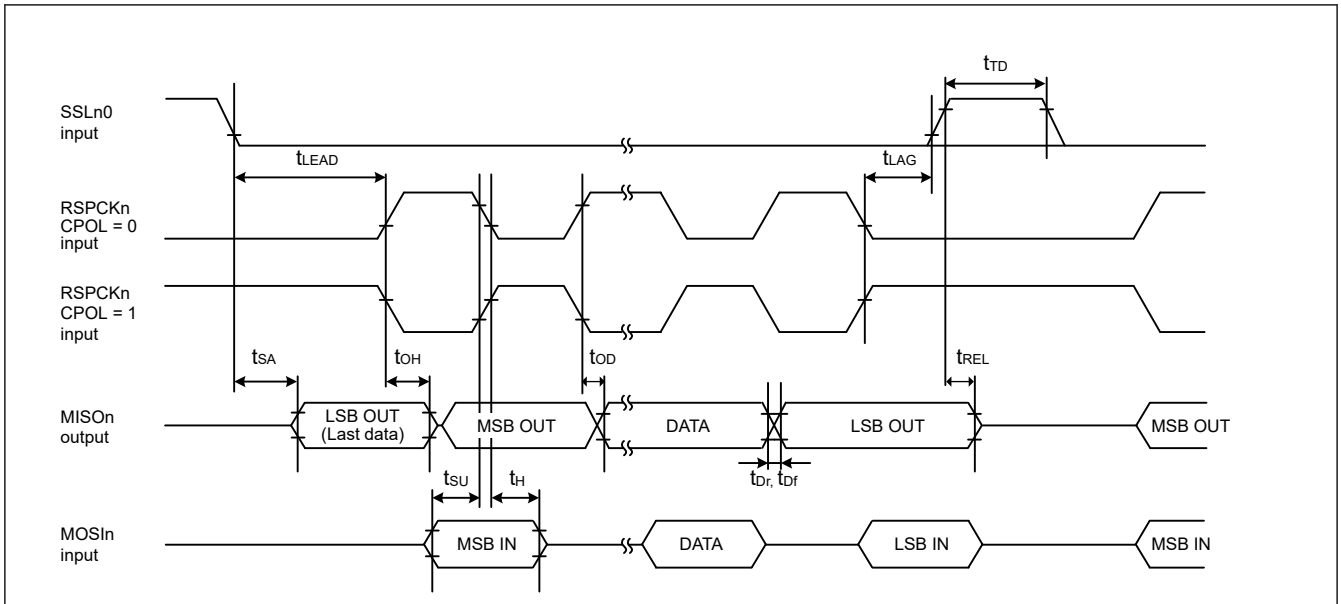
Note: n = A or B
i = 0

Figure 2.35 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)



Note: n = A or B

Figure 2.36 SPI timing (slave, CPHA = 0)



Note: n = A or B

Figure 2.37 SPI timing (slave, CPHA = 1)

2.3.10 QSPI Timing

Table 2.40 QSPI timing (1 of 2)

Parameter		Symbol	Min	Max	Unit	Test conditions
QSPCK clock cycle	2.4 ≤ VCC ≤ 3.6	t_{QScyc}	50	—	ns	Figure 2.38
	1.8 ≤ VCC < 2.4		100	—	ns	
	1.6 ≤ VCC < 1.8		500	—	ns	
QSPCK clock high pulse width		t_{QSWH}	t_{QScyc} × 0.4	—	ns	
QSPCK clock low pulse width		t_{QSWL}	t_{QScyc} × 0.4	—	ns	

Table 2.40 QSPI timing (2 of 2)

Parameter		Symbol	Min	Max	Unit	Test conditions
Data input setup time	2.4 ≤ VCC ≤ 3.6	t_{Su}	10	—	ns	Figure 2.39
	1.8 ≤ VCC < 2.4		15	—	ns	
	1.6 ≤ VCC < 1.8		15	—	ns	
Data input hold time	1.8 ≤ VCC < 3.6	t_{IH}	0	—	ns	
	1.6 ≤ VCC < 1.8		4	—	ns	
QSSL setup time	2.4 ≤ VCC ≤ 3.6	t_{Su}	(N + 0.5) × t_{Qscyc} − 9*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	1.8 ≤ VCC < 2.4		(N + 0.5) × t_{Qscyc} − 15*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
	1.6 ≤ VCC < 1.8		(N + 0.5) × t_{Qscyc} − 24*1	(N + 0.5) × t_{Qscyc} + 100*1	ns	
QSSL hold time	1.8 ≤ VCC ≤ 3.6	t_{LAG}	(N + 0.5) × t_{Qscyc} − 5*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	1.6 ≤ VCC < 1.8		(N + 0.5) × t_{Qscyc} − 8*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
Data output delay	2.4 ≤ VCC ≤ 3.6	t_{OD}	—	9	ns	
	1.8 ≤ VCC < 2.4		—	16	ns	
	1.6 ≤ VCC < 1.8		—	24	ns	
Data output hold time	1.8 ≤ VCC ≤ 3.6	t_{OH}	−3.3	—	ns	
	1.6 ≤ VCC < 1.8		−6.3	—	ns	
Successive transmission delay		t_{TD}	1	16	t_{QScyc}	

Note: t_{Pcyc}: PCLKA cycle.
Note 1. N is set to 0 or 1 in SFMSLD.
Note 2. N is set to 0 or 1 in SFMSHD.

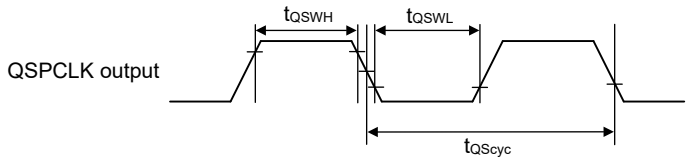


Figure 2.38 QSPI clock timing

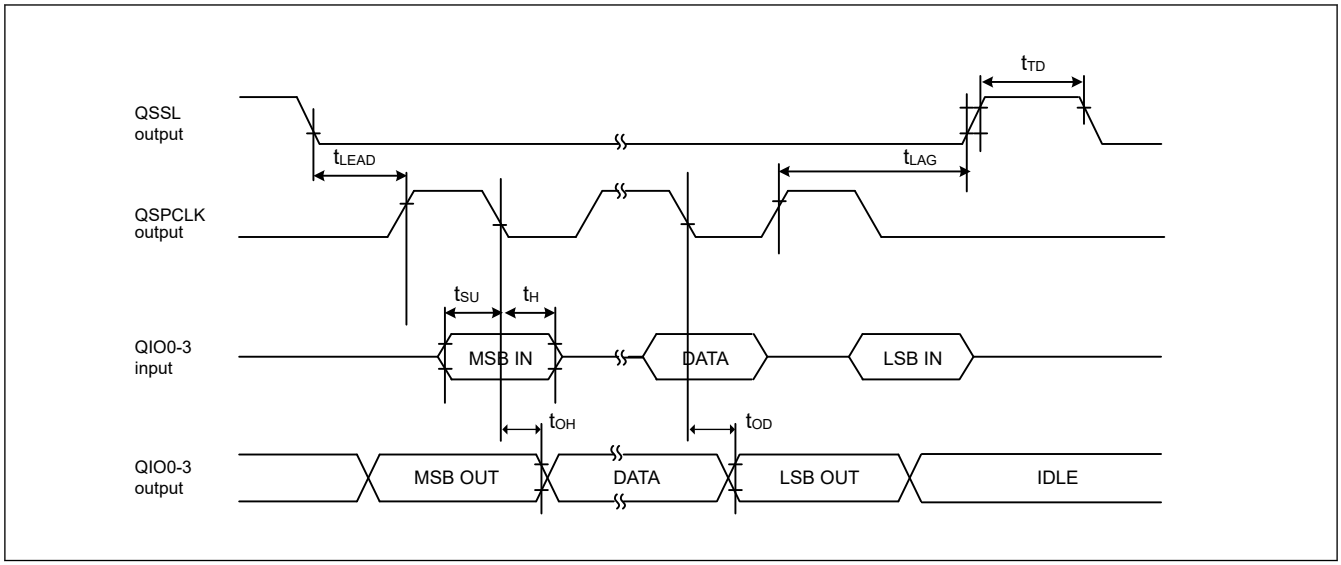


Figure 2.39 Transmit and receive timing

2.3.11 IIC Timing

Table 2.41 IIC timing (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit	Test conditions
IIC (standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.40
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Table 2.41 IIC timing (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit	Test conditions
IIC (Fast mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.40
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc}+ 300	—	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. The AC portion of the electrical characteristics is measured for each group.

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle

Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

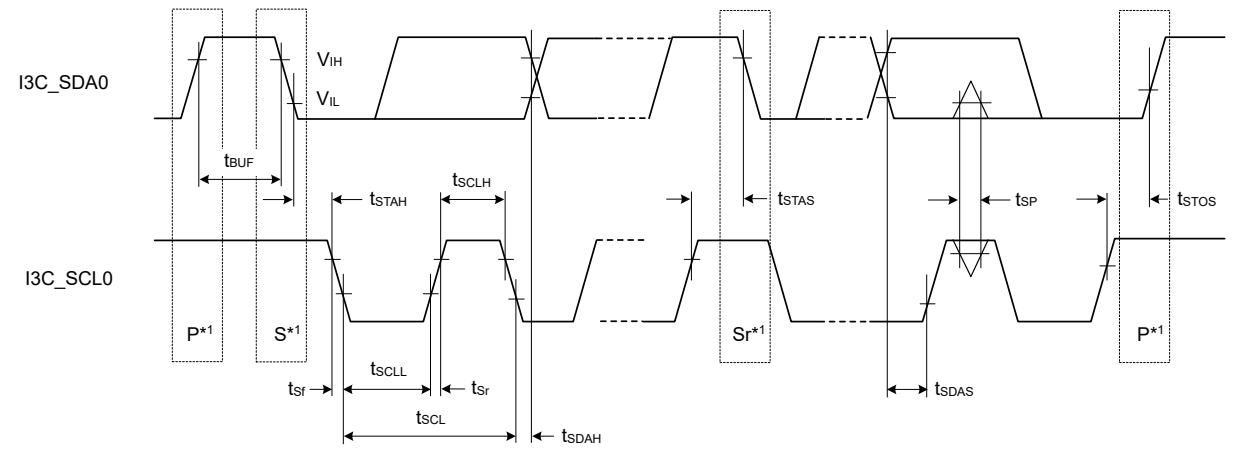
Note 2. C_b indicates the total capacity of the bus line.

Table 2.42 IIC timing (2)

Conditions: VCC = AVCC0 = 2.7 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	—	ns	Figure 2.40
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA rise time	t_{Sr}	—	120	ns	
	SCL, SDA fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	—	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	—	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	—	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. C_b indicates the total capacity of the bus line.



Note: n = 0
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.40 I²C bus interface input/output timing

2.3.12 I3C Timing

Table 2.43 IIC timing(1)

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	—	1000	ns
	SCL, SDA fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	1000	—	ns
	STOP condition input setup time	t_{STOS}	1000	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*2	—	400	pF
IIC (Fast-mode) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5 V)	1000	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	300	—	ns
	STOP condition input setup time	t_{STOS}	300	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*2	—	400	pF

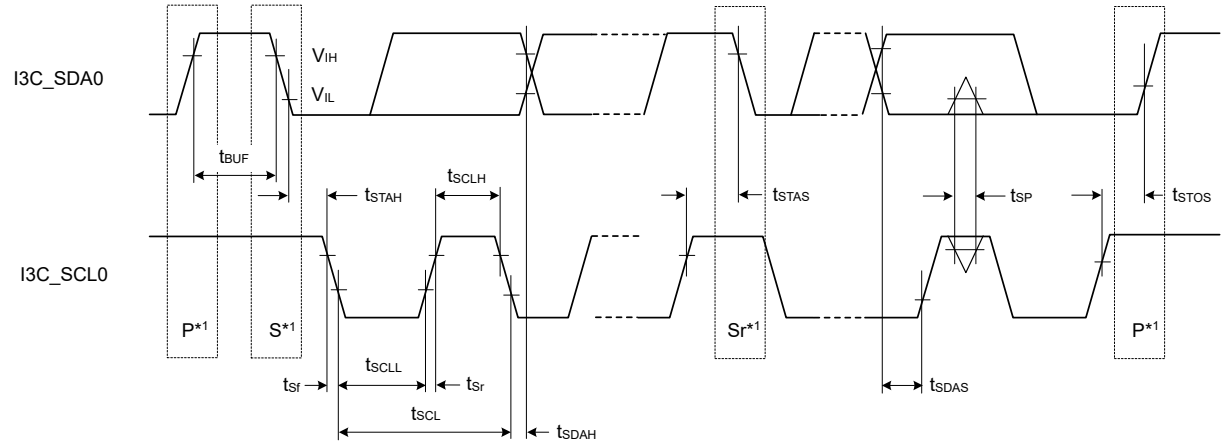
Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 2. C_b indicates the total capacity of the bus line.

Table 2.44 IIC timing (Fast-mode+)

Conditions: VCC = AVCC0 = 2.7 to 3.6 V

Parameter		Symbol	Min*1	Max*1	Unit
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	—	120	ns
	SCL, SDA fall time	t_{Sf}	—	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 120	—	ns
	Restart condition input setup time	t_{STAS}	120	—	ns
	Stop condition input setup time	t_{STOS}	120	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*2	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 2. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.41 I²C bus interface input/output timing

Table 2.45 IIC timing (HS-mode)

Conditions: VCC = 2.7 to 3.60 V

Parameter			Symbol	Min*1	Max*1	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	55(57) × t_{I3Ccyc}	—	ns
					—	
	SCL input high pulse width	C_b = 400 pF	t_{SCLH}	43(44) × t_{I3Ccyc}	—	ns
		C_b = 100 pF		23(24) × t_{I3Ccyc}	—	
	SCL input low pulse width	C_b = 400 pF	t_{SCLL}	64(65) × t_{I3Ccyc}	—	ns
		C_b = 100 pF		32(33) × t_{I3Ccyc}	—	
	SCL rise time	C_b = 400 pF	t_{SrCL}	—	80	ns
		C_b = 100 pF		—	40	
	SDA rise time	C_b = 400 pF	t_{SrDA}	—	160	ns
		C_b = 100 pF		—	80	
	SCL fall time	C_b = 400 pF	t_{SfCL}	—	80	ns
		C_b = 100 pF		—	40	
	SDA fall time	C_b = 400 pF	t_{SfDA}	—	160	ns
		C_b = 100 pF		—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{I3Ccyc}	ns
	Repeated START condition input setup time		t_{STAS}	40	—	ns
	STOP condition input setup time		t_{STOS}	40	—	ns
	Data input setup time		t_{SDAS}	0	—	ns
	Data input hold time	C_b = 400 pF	t_{SDAH}	0	150	ns
		C_b = 100 pF		0	70	
	SCL, SDA capacitive load		C_b*2	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.

Note 1. Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.

Note 2. C_b indicates the total capacity of the bus line.

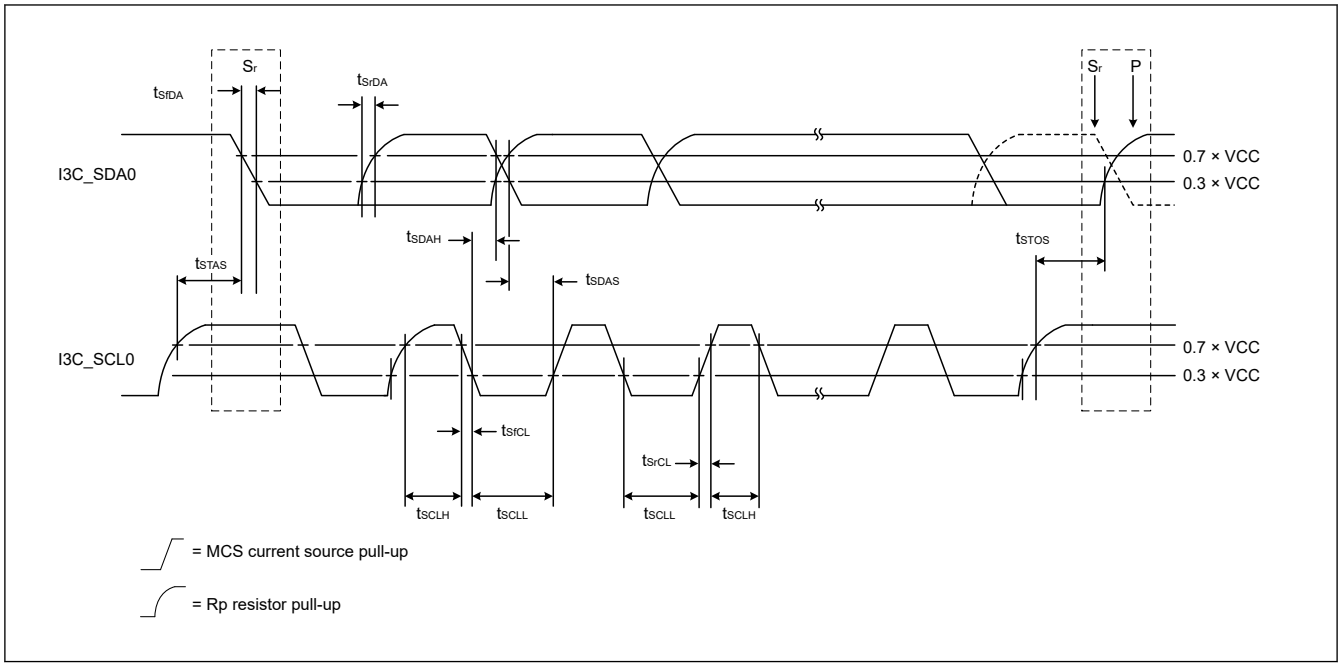


Figure 2.42 I²C bus interface input/output timing (Hs-mode)

Table 2.46 I3C timing (open drain timing parameters)

Conditions: VCC = 3.0 to 3.60 V

Parameter		Symbol	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	200	—	ns	Figure 2.45
		$t_{DIG\_OD\_L}$	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—	ns	Figure 2.45
	SCL Clock High Period	t_{HIGH} *3 *4	—	41	ns	Figure 2.43
		t_{DIG_H}	—	$t_{HIGH} + t_{CF}$	ns	Figure 2.43
	SDA Signal Fall Time	t_{fDA_OD}	t_{CF}	33	ns	Figure 2.45
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	24	—	ns	Figure 2.44
	Clock After START (S) Condition	t_{CAS} *5 *6	38.4 nano	ENAS0: 1 µ	seconds	Figure 2.45
				ENAS1: 100 µ		
				ENAS2: 2 milli		
				ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	t_{CASmin} / 2	—	seconds	Figure 2.46
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 2.51
	Bus Available Condition	t_{AVAL} *7	1	—	µs	—
	Bus Idle Condition	t_{IDLE}	1	—	ms	—
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	Figure 2.51

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_Odmin}$.

Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH.

Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I²C Devices, and/or in consideration of the interconnect (e.g., a short Bus).

As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.

Note 5. On a legacy bus where I^2C devices need to see Start

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3

Note 7. On a mixed bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.47 I3C timing (push-pull timing parameters for SDR mode)

Conditions: VCC = 3.0 to 3.60 V

Parameter			Symbol	Min	Max	Unit
I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes	SCL Clock Frequency		f_{SCL} *1	0.01	6.38	MHz
	SCL Clock Low Period		t_{LOW}	71	—	ns
			t_{DIG_L} *2 *4	79	—	ns
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	60	—	ns
			$t_{DIG\_H\_MIXED}$ *2 *3	68	—	ns
	SCL Clock High Period		t_{HIGH}	60	—	ns
			t_{DIG_H} *2	68	—	ns
	Clock in to Data Out for Slave		t_{SCO}	—	33	ns
	SCL Clock Rise Time		t_{CR}	—	150 × 1 /f_{SCL}(capped at 60)	ns
	SCL Clock Fall Time		t_{CF}	—	150 × 1 /f_{SCL}(capped at 60)	µs
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4	t_{CR} + 3, t_{CF} +3	—	—
		Slave	t_{HD_PP}	0	—	—
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	27	N/A	ns
	Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns
	Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns
	Capacitive Load per Bus Line (SDA/SCL)		C_b	—	50	pF

Note 1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$

Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.

Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.

Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

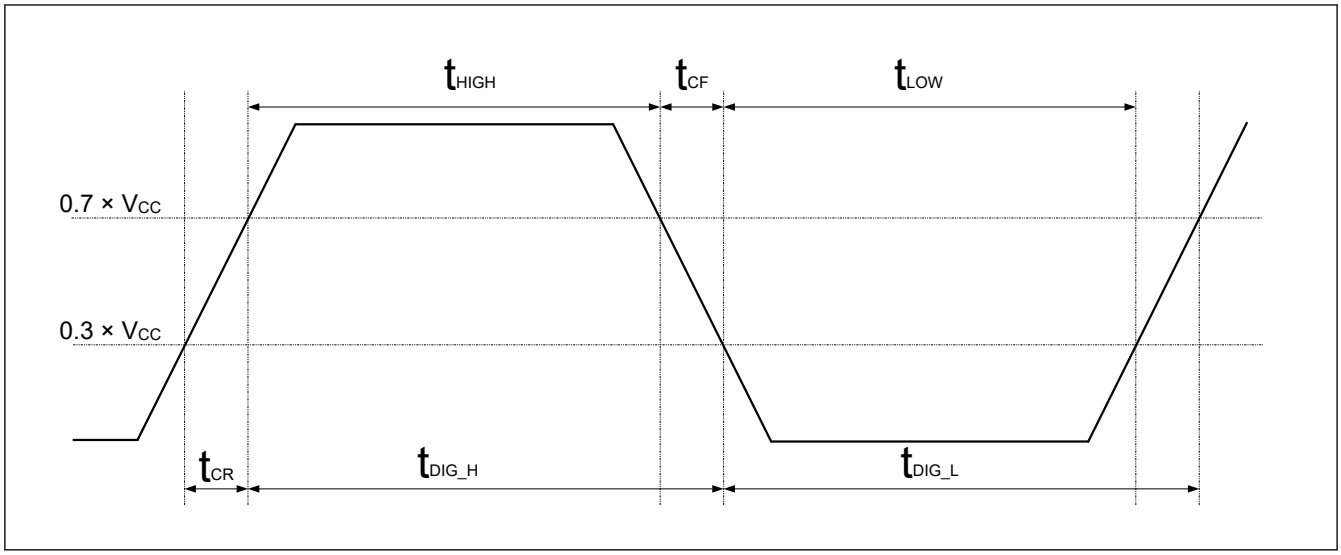


Figure 2.43 t_{DIG_H} and t_{DIG_L}

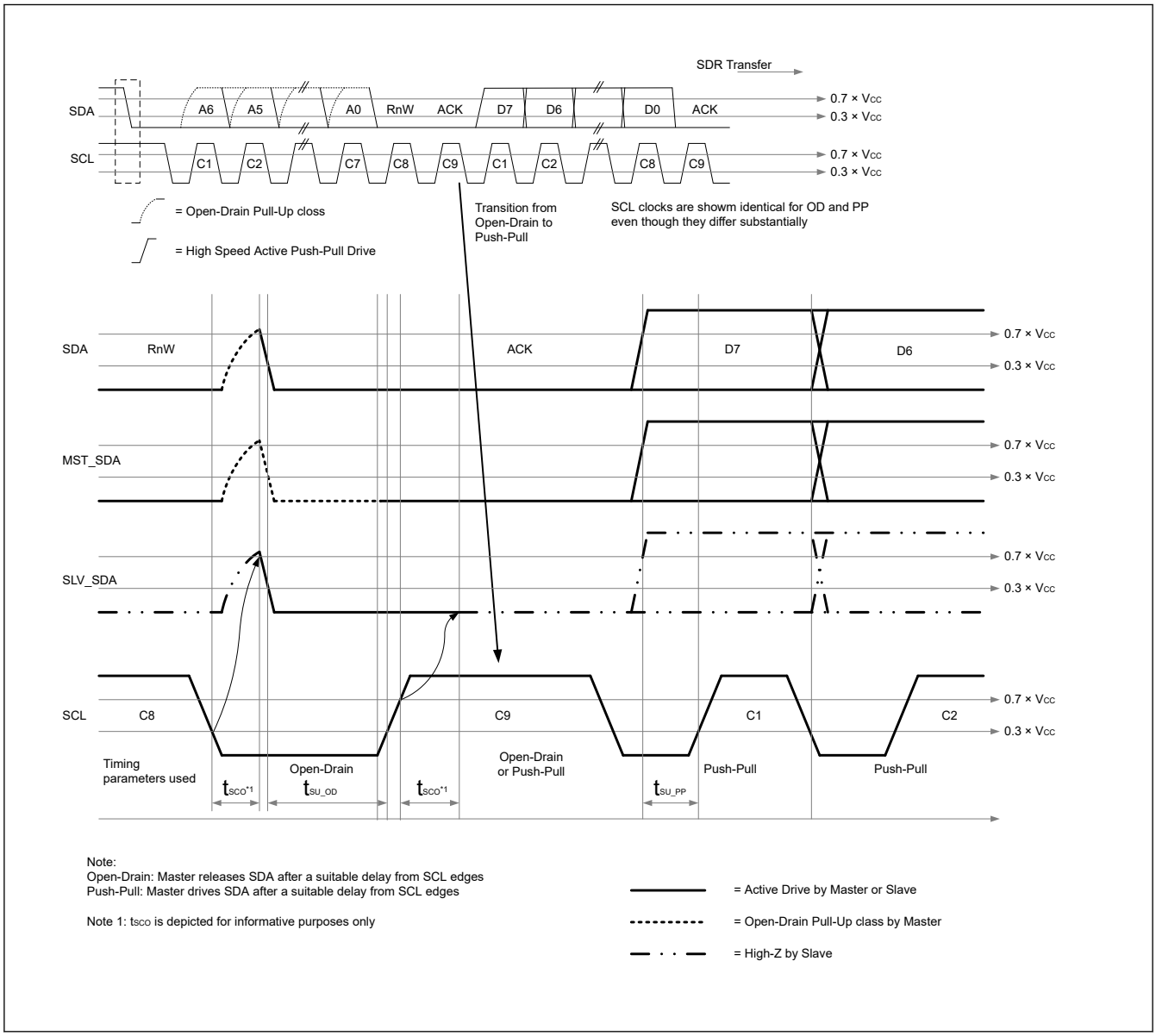


Figure 2.44 **I3C data transfer – ACK by slave**

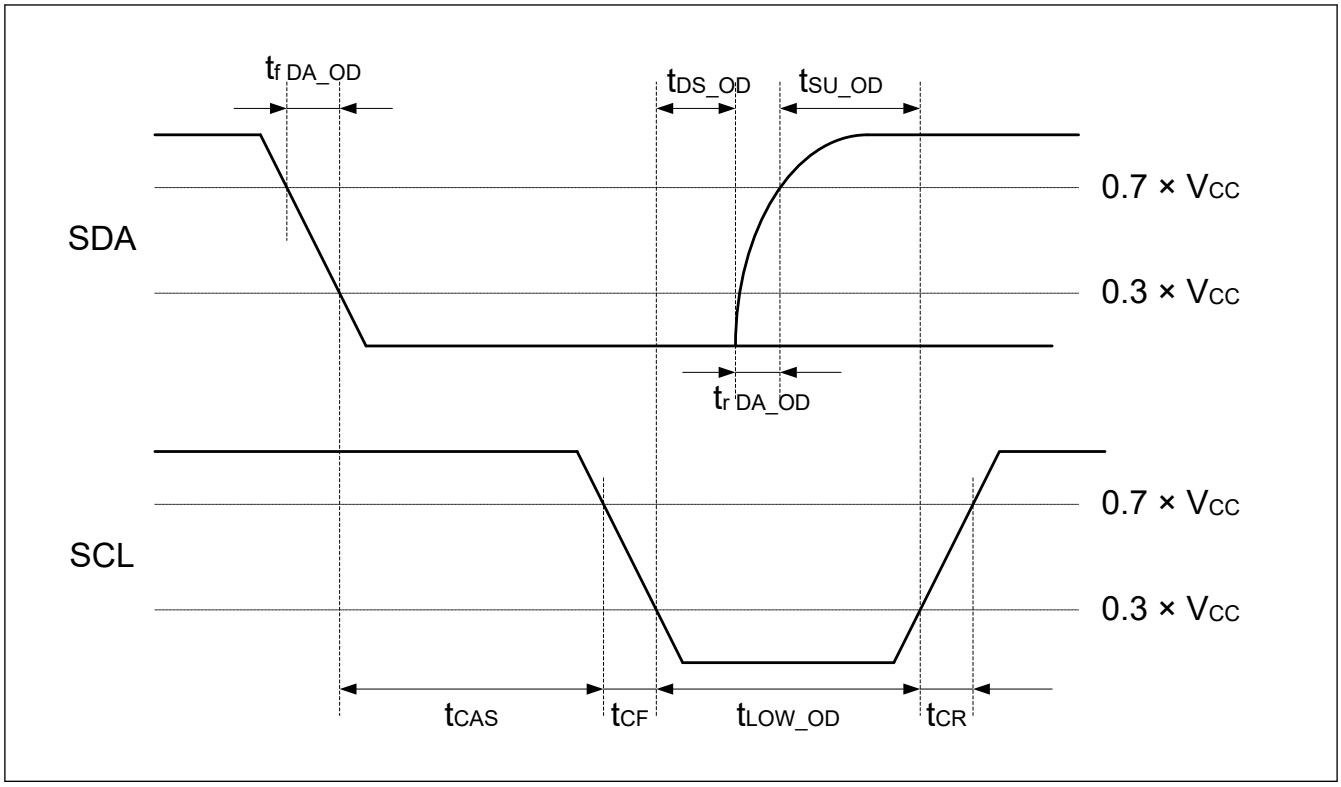


Figure 2.45 I3C START condition timing

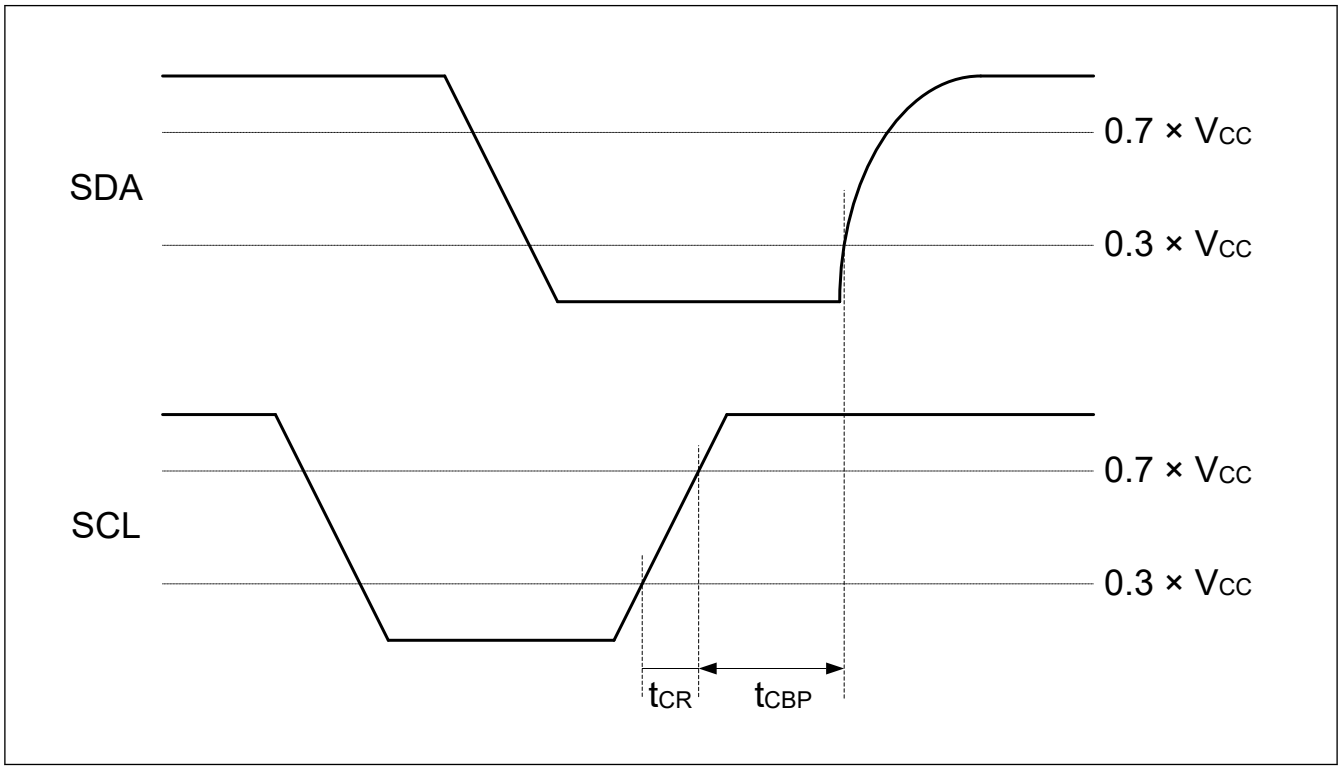


Figure 2.46 I3C STOP condition timing

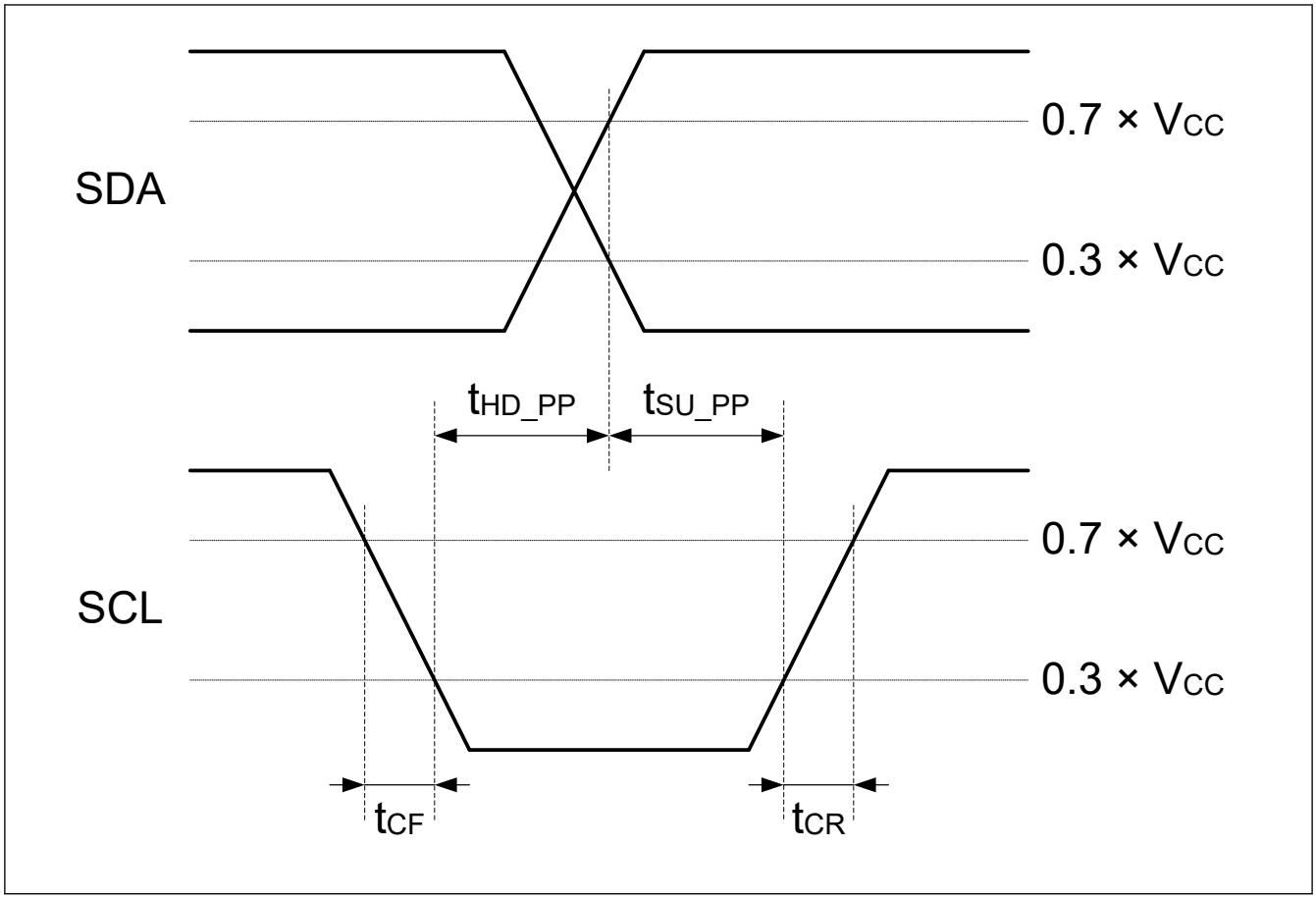


Figure 2.47 I3C master out timing

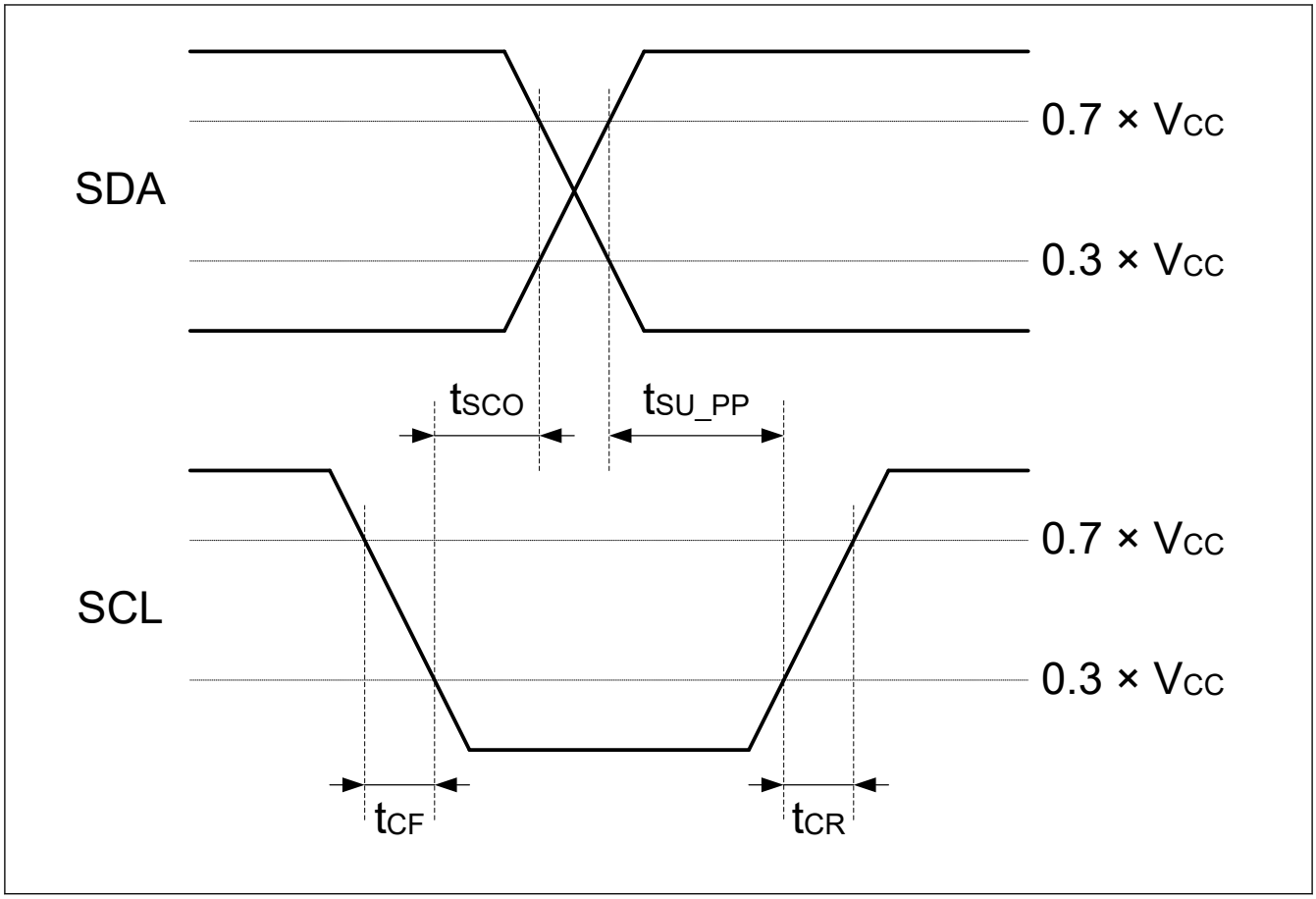


Figure 2.48 I3C slave out timing

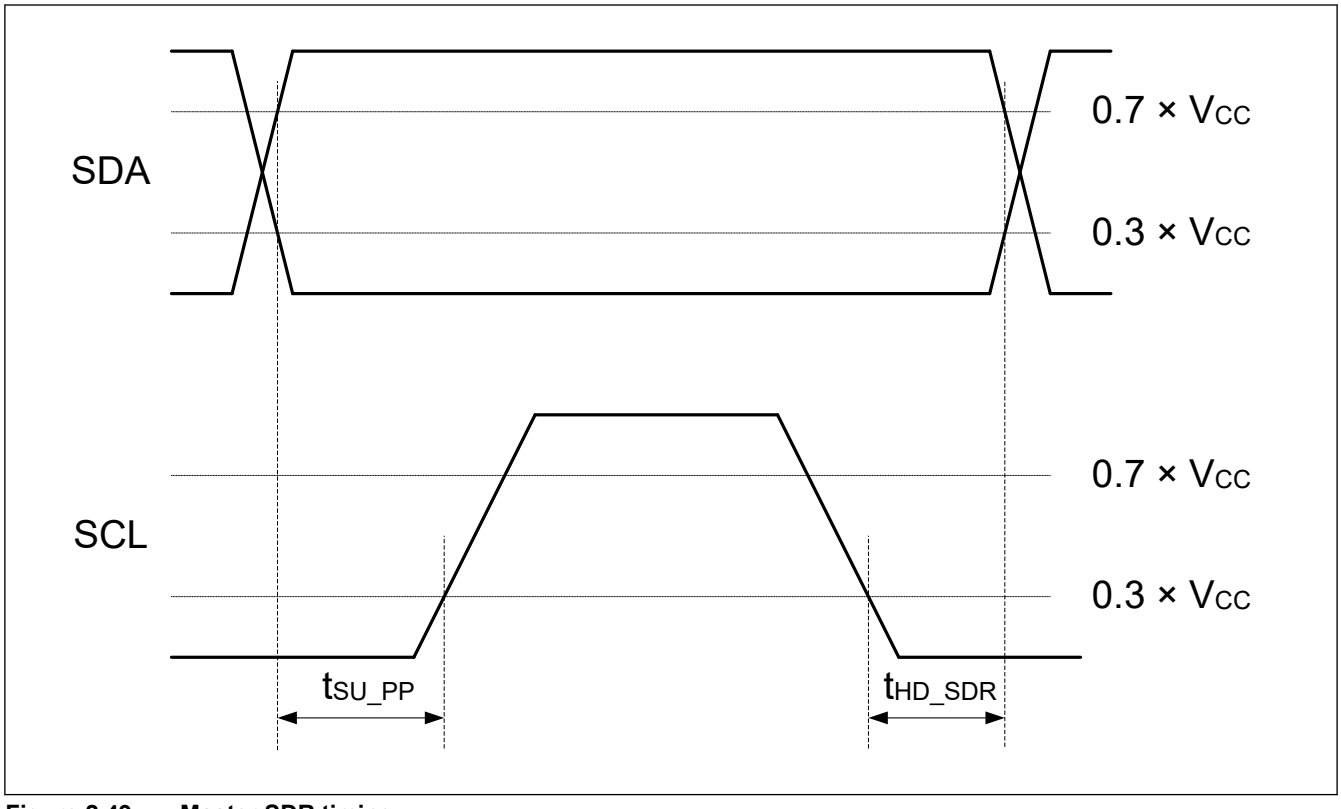


Figure 2.49 Master SDR timing

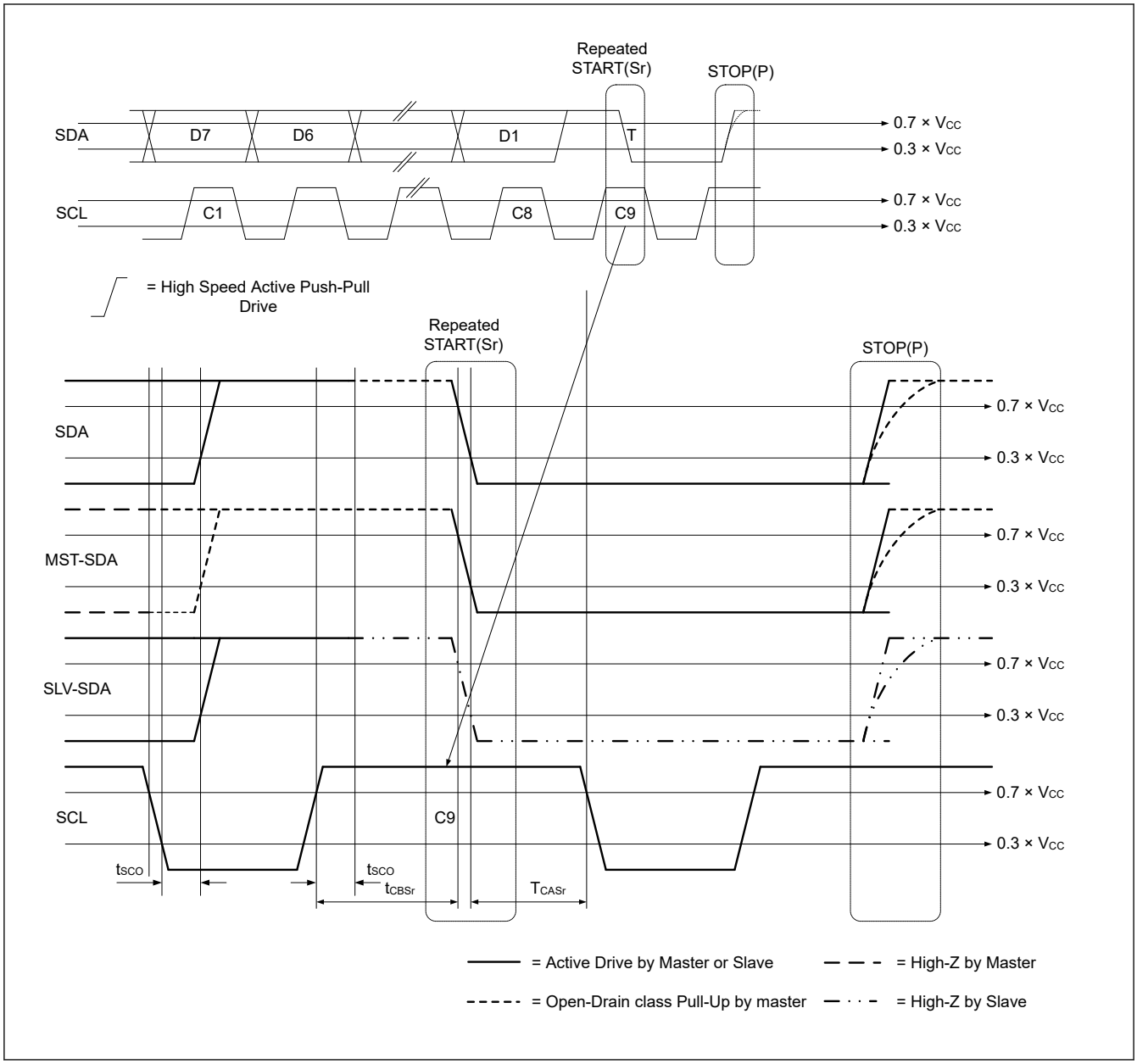


Figure 2.50 T-bit when master ends read with repeated START and STOP

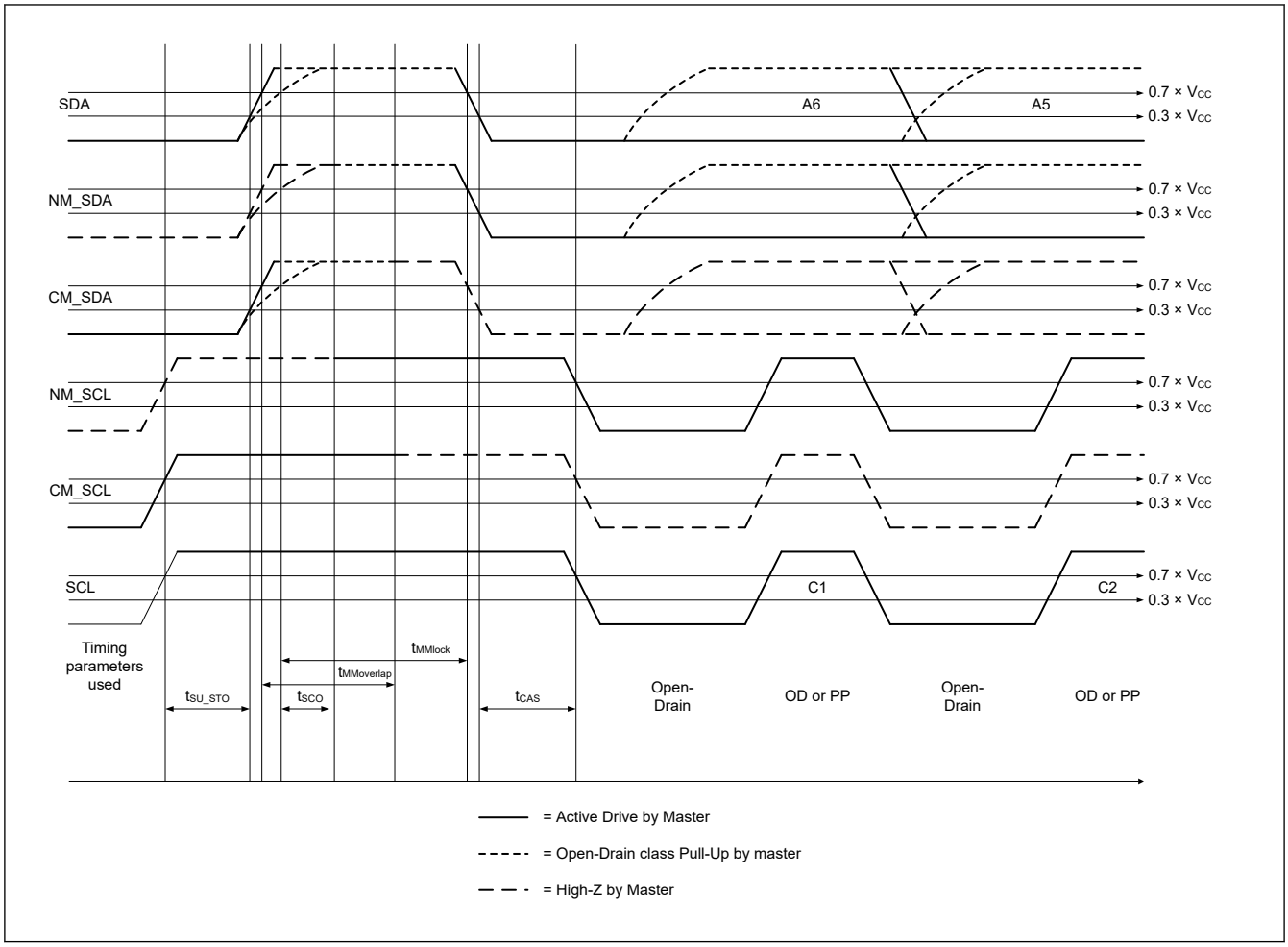


Figure 2.51 I3C timing (open drain timing parameters)

2.3.13 SSIE Timing

Table 2.48 SSIE timing (1 of 2)

(1) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter				Symbol	Target specification		Unit	Test conditions
					Min	Max		
SSIBCK0	Cycle	Master	2.7v ≤ VCC ≤ 3.6	t_O	150	—	ns	Figure 2.52
			2.4 ≤ VCC < 2.7		200	—	ns	
			1.8 ≤ VCC < 2.4		250	—	ns	
			1.6 ≤ VCC < 1.8		1000	—	ns	
		Slave	2.7v ≤ VCC ≤ 3.6	t_I	150	—	ns	
			2.4 ≤ VCC < 2.7		200	—	ns	
			1.8 ≤ VCC < 2.4		250	—	ns	
			1.6 ≤ VCC < 1.8		1000	—	ns	
	High level/ Low level	Master		t_{HC}/t_{LC}	0.35	—	t_O	
		Slave			0.35	—	t_I	
	Rising time/ falling time	Master		t_{RC}/t_{FC}	—	0.15	t_O / t_I	
		Slave			—	0.15	t_O / t_I	

Table 2.48 SSIE timing (2 of 2)

(1) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter				Symbol	Target specification		Unit	Test conditions
					Min	Max		
SSILRCK0/ SSIFS0, SSITXD0, SSIRXD0	Input set up time	Master	2.7v ≤ VCC ≤ 3.6	t_{SR}	30	—	ns	Figure 2.54, Figure 2.55
			2.4 ≤ VCC < 2.7		30	—	ns	
			1.8 ≤ VCC < 2.4		45	—	ns	
			1.6 ≤ VCC < 1.8		60	—	ns	
		Slave	2.7v ≤ VCC ≤ 3.6		10	—	ns	
			1.8 ≤ VCC < 2.7		10	—	ns	
			1.8 ≤ VCC < 2.7		10	—	ns	
			1.6 ≤ VCC < 1.8		10	—	ns	
	Input hold time	Master		t_{HR}	10	—	ns	
		Slave			18	—	ns	
	Output delay time	Master	2.7v ≤ VCC ≤ 3.6	t_{DTR}	0	15	ns	
			2.4 ≤ VCC < 2.7		0	15		
			1.8 ≤ VCC < 2.4		0	15		
			1.6 ≤ VCC < 1.8		0	15		
		Slave	2.7v ≤ VCC ≤ 3.6		8	35	ns	
			2.4 ≤ VCC < 2.7		10	40		
			1.8 ≤ VCC < 2.4		10	55		
			1.6 ≤ VCC < 1.8		10	65		
	Output delay time from SSILRCK0/ SSIFS0 change	Slave	2.7v ≤ VCC ≤ 3.6	t_{DTRW}	10	35	ns	Figure 2.55, Figure 2.56*1
			2.4 ≤ VCC < 2.7		10	35		
			1.8 ≤ VCC < 2.4		10	48		
			1.6 ≤ VCC < 1.8		10	60		
GTIOC2A, AUDIO_CLK	Cycle		1.8 ≤ VCC < 3.6	t_{EXcyc}	25	—	ns	Figure 2.53
			1.6 ≤ VCC < 1.8		250	—		
	High level/ Low level			t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK0/SSIFS0 pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 pin.

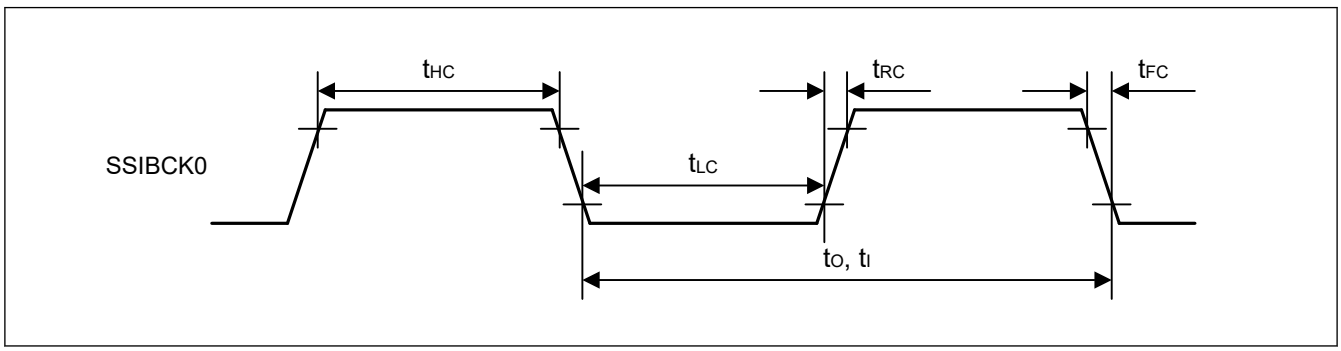


Figure 2.52 SSIE clock input/output timing

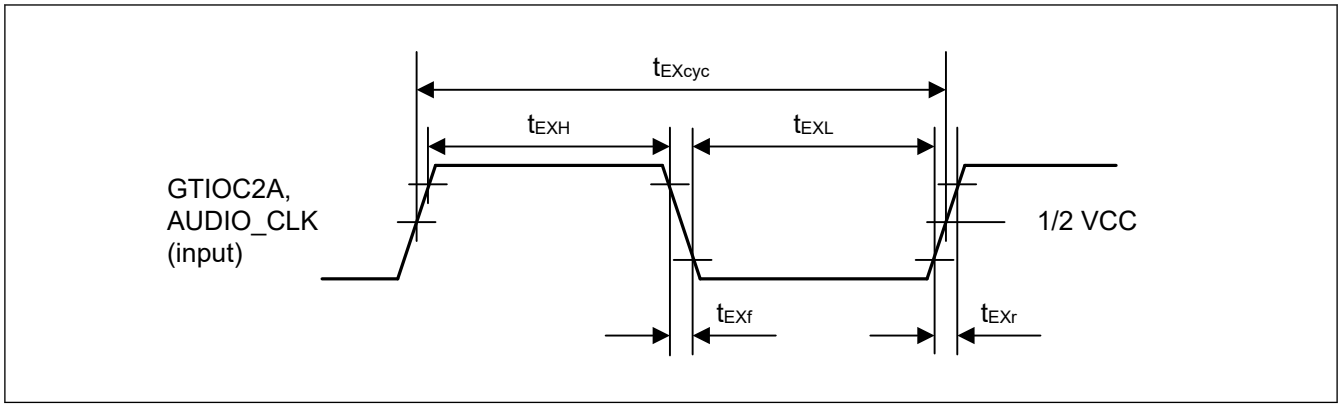


Figure 2.53 Clock input timing

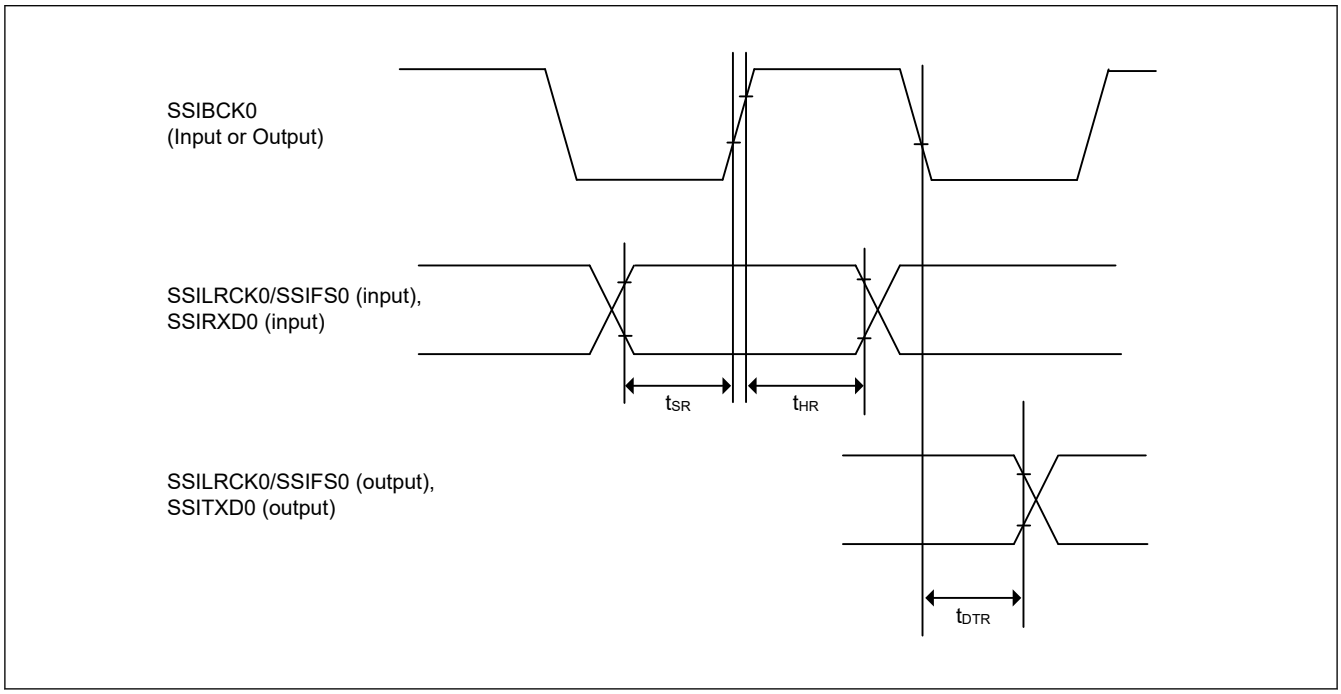


Figure 2.54 SSIE data transmit and receive timing when SSICR.BCKP = 0

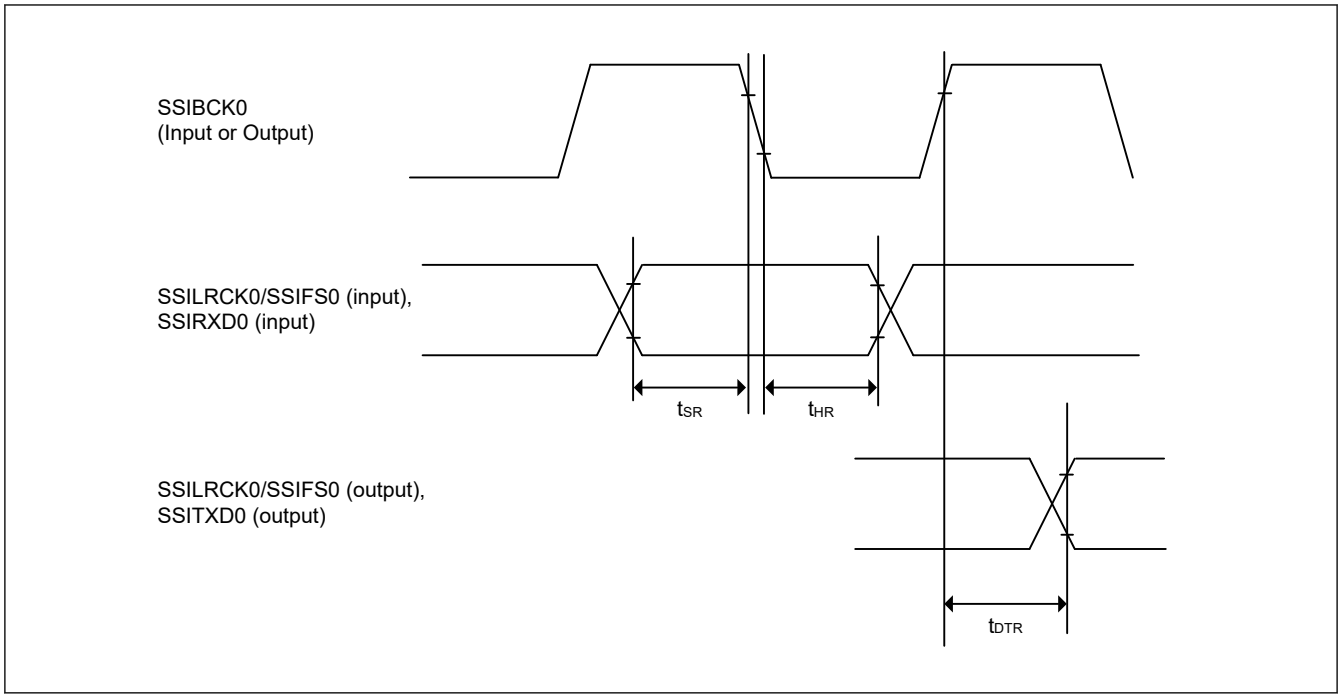


Figure 2.55 SSIE data transmit and receive timing when SSICR.BCKP = 1

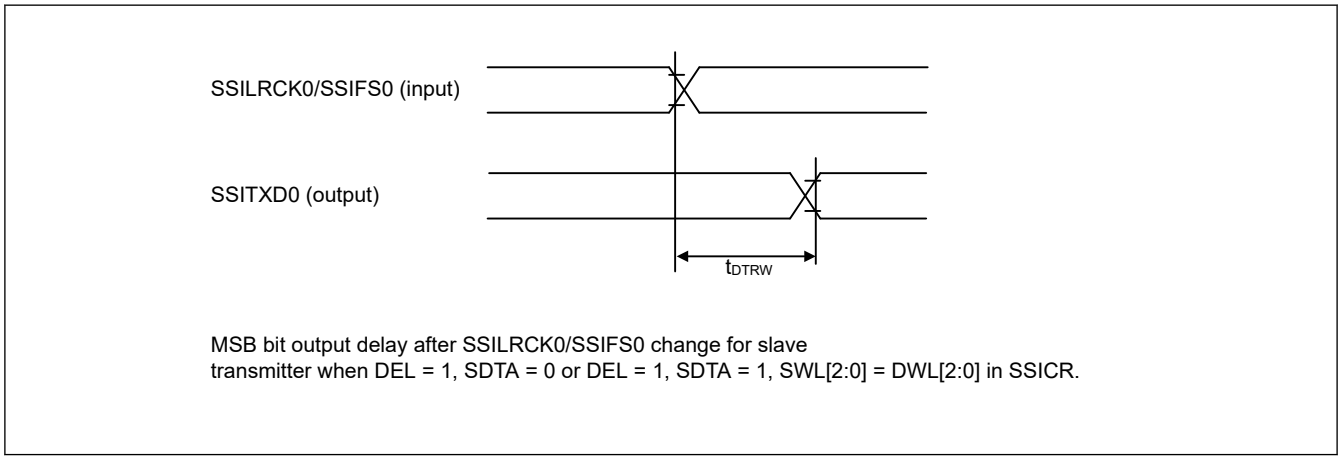


Figure 2.56 SSIE data output delay after SSILRCK0/SSIFS0 change

2.3.14 UARTA Timing

Table 2.49 UARTA interface timing

Parameter	Symbol	Min.	Max.	Unit	Test conditions
Transfer rate	—	200	153600	bps	—

2.3.15 CANFD Timing

Table 2.50 CANFD interface timing

Parameter	Symbol	CAN		CANFD		Unit	Test conditions
		Min	Max	Min	Max		
Internal delay time	t_{node}	—	100	—	75	ns	Figure 2.57

Note: $t_{node} = t_{d(CTX)} + t_{d(CRX)}$

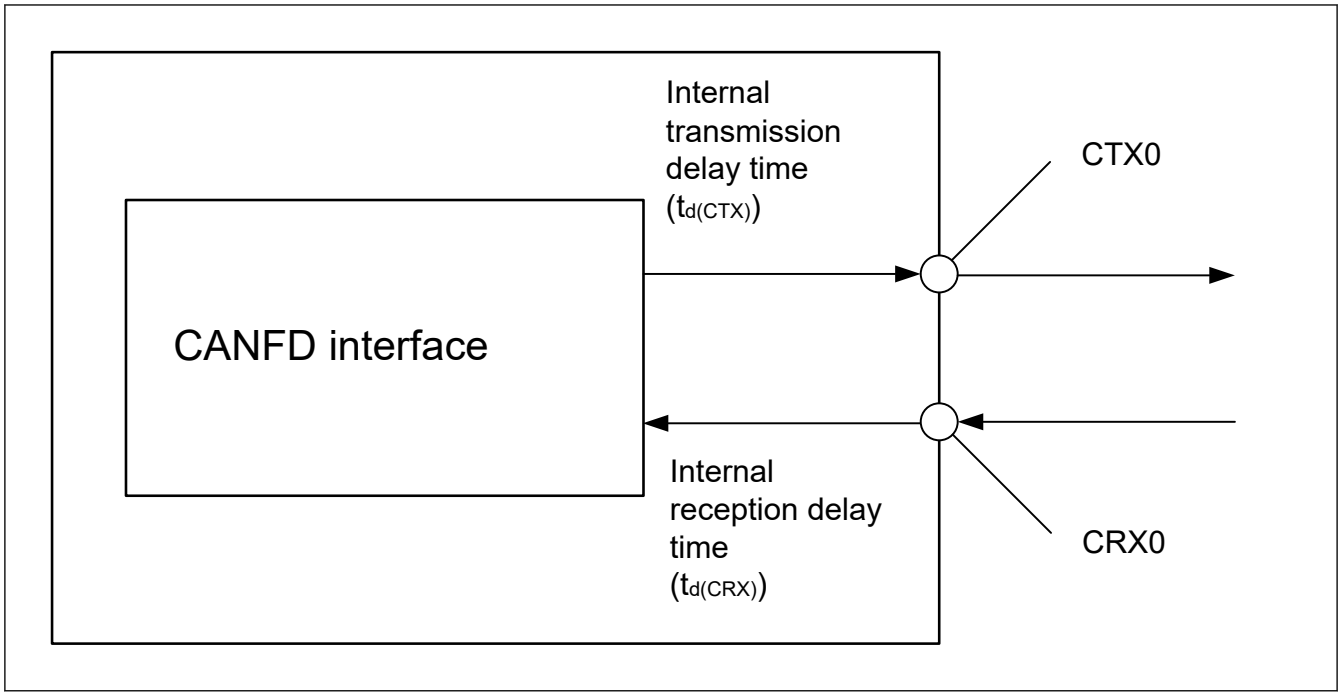


Figure 2.57 CANFD interface condition

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.51 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)

Conditions: VCC = AVCC0 = VCC_USB = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.58
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

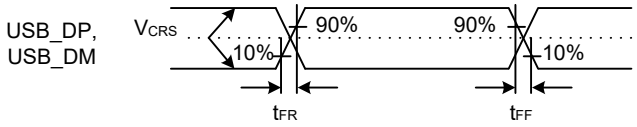


Figure 2.58 USB_DP and USB_DM output timing in full-speed mode

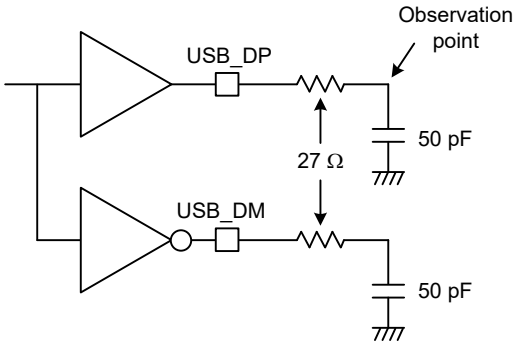


Figure 2.59 Test circuit in full-speed mode

2.5 ADC12 Characteristics

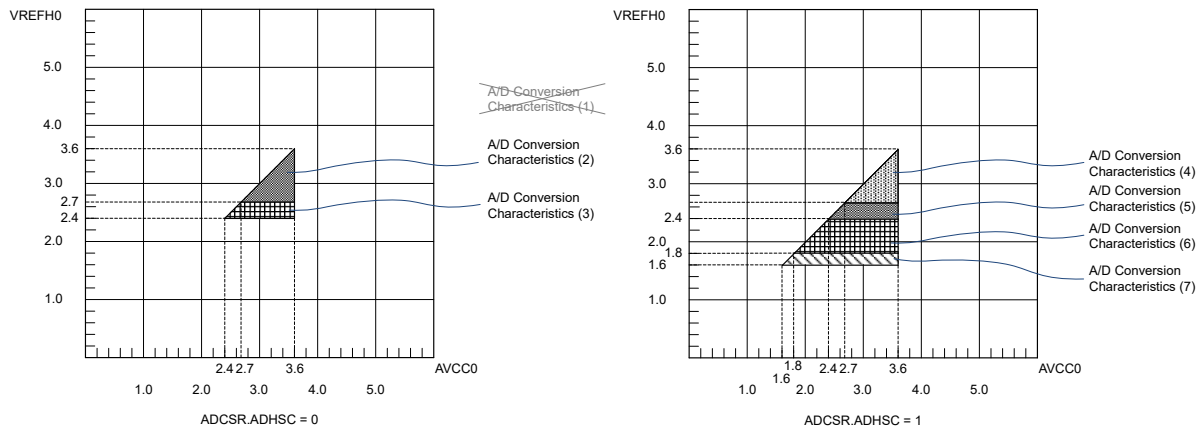


Figure 2.60 AVCC0 to VREFH0 voltage range

Table 2.52 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
		—	—	6.0*3	kΩ	Normal-precision channel

Table 2.52 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.29 (0.844)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.53 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7.0[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.53 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		1.94 (1.266)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x28 ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
				±7.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.50	±6.0	LSB	High-precision channel
				±9.0	LSB	Other than specified
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.54 A/D conversion characteristics (3) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
		—	—	6[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		2.0 (0.854)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1

Table 2.54 A/D conversion characteristics (3) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Offset error	—	±1.25	±6.0	LSB	High-precision channel
			±7.5	LSB	Other than specified
Full-scale error	—	±1.25	±6.0	LSB	High-precision channel
			±7.5	LSB	Other than specified
Quantization error	—	±0.5	—	LSB	—
Absolute accuracy	—	±3.25	±7.0	LSB	High-precision channel
			±10.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.5	—	LSB	—
INL integral nonlinearity error	—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.55 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
		—	—	7[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		3.0 (1.281)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Full-scale error		—	±1.25	±6.0	LSB	High-precision channel
				±7.5	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—

Table 2.55 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = VREFH0 = 2.4 to 3.6 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions
Absolute accuracy	—	±3.25	±7.0	LSB	High-precision channel
			±10.0	LSB	Other than specified
DNL differential nonlinearity error	—	±1.5	—	LSB	—
INL integral nonlinearity error	—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.56 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 3.6 V[*5] (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
		—	—	10[*3]	pF	Normal-precision channel
Analog input resistance	Rs	—	—	6[*3]	kΩ	High-precision channel
		—	—	14[*3]	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		6.0 (2.563)[*4]	—	—	µs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

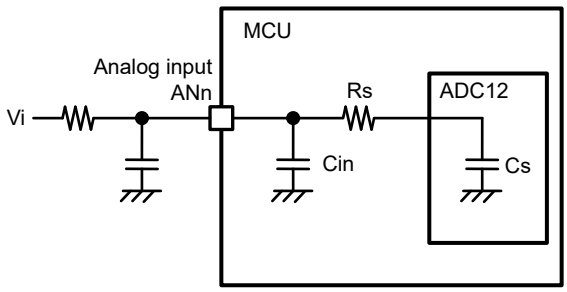
Table 2.57 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = AVCC0 = VREFH0 = 1.6 to 3.6 V*5 (AVCC0 = VCC when VCC < 2.0 V), VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKC (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
		—	—	10*3	pF	Normal-precision channel
Analog input resistance	Rs	—	—	12*3	kΩ	High-precision channel
		—	—	28*3	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKC = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
		12.0 (5.125)*4	—	—	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x14 ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than specified
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
				±13.5	LSB	Other than specified
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O V_{OH}, V_{OL}, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC0, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.75 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC0 and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Figure 2.61 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.61 Equivalent circuit for analog input

Table 2.58 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN006	AVCC0 = 1.6 to 3.6 V	Pins AN000 to AN006 cannot be used as general I/O, when the A/D converter is in use.
Normal-precision channel	AN017 to AN025		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 1.8 to 3.6 V	—
Temperature sensor input channel	Temperature sensor output	AVCC0 = 1.8 to 3.6 V	—
Input channel from CTSU	CTSU TSCAP voltage	AVCC0 = 1.6 to 3.6 V	—

Table 2.59 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 1.8 to 3.6 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKC (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.

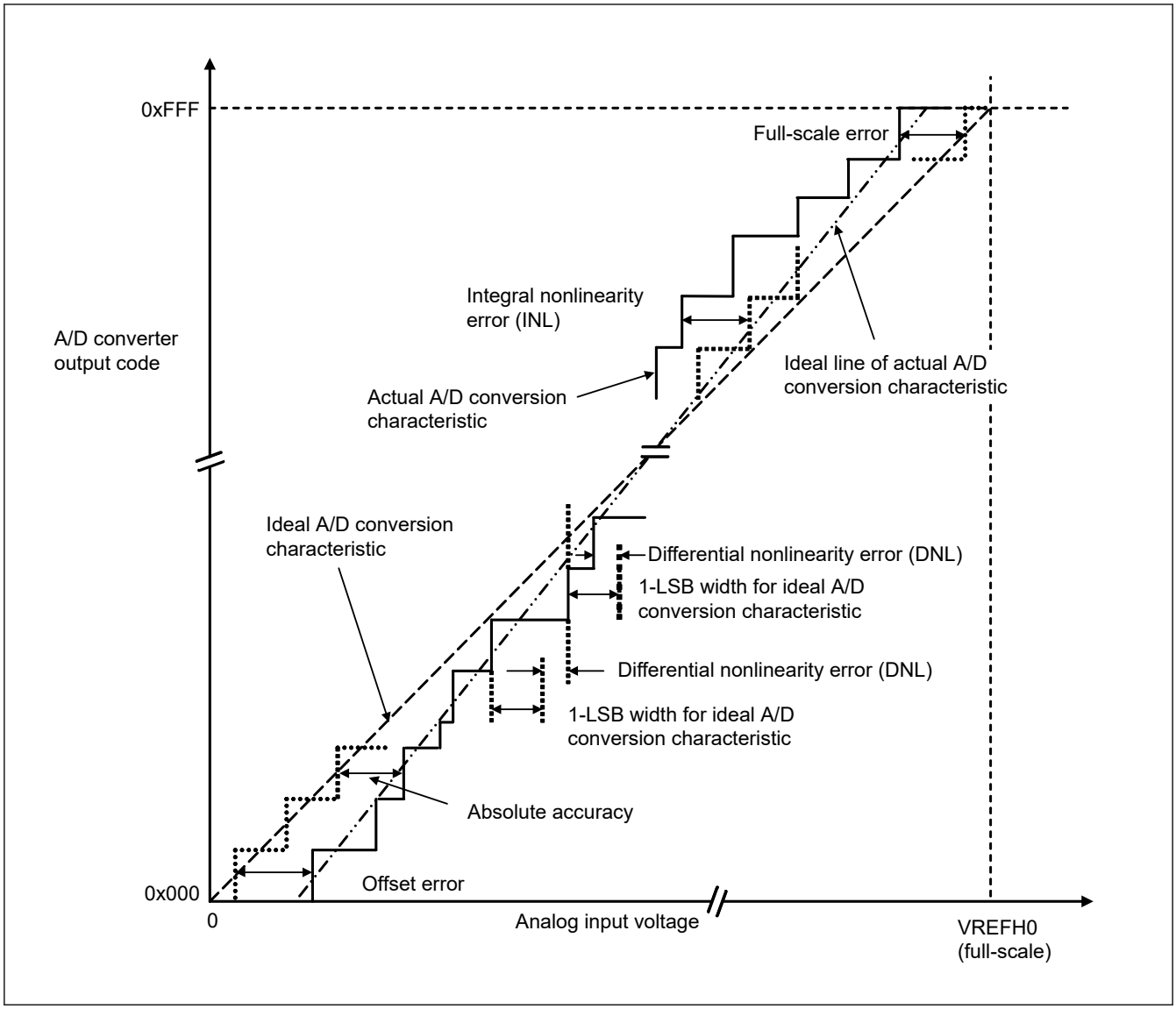


Figure 2.62 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

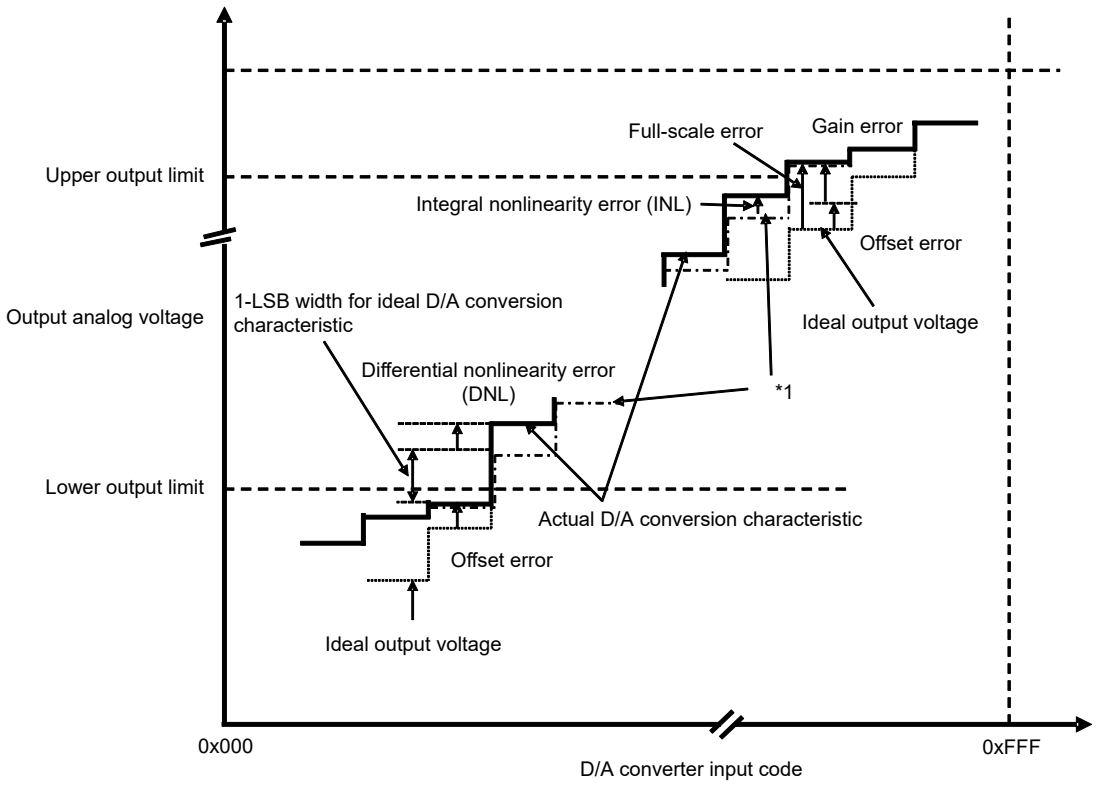
Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.60 12-bit D/A conversion characteristics

Conditions: VCC = AVCC0 = 1.8 to 3.6 V
Reference voltage = AVCC0 or AVSS0 selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	bit	—
Resistive load	30	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.35	—	AVCC0-0.47	V	—
DNL differential nonlinearity error	—	±0.5	±2.0	LSB	—
INL integral nonlinearity error	—	±2.0	±8.0	LSB	—
Offset error	—	—	±30	mV	—
Full-scale error	—	—	±30	mV	—
Output impedance	—	5	—	Ω	—
Conversion time	—	—	30	µs	—



Note 1. Ideal D/A conversion output voltage that is adjusted so that offset and full scale errors are zeroed.

Figure 2.63 Illustration of D/A converter characteristic terms

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

2.7 TSN Characteristics

Table 2.61 TSN characteristics

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—	°C	Below 2.4 V
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

2.8 OSC Stop Detect Characteristics

Table 2.62 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.64

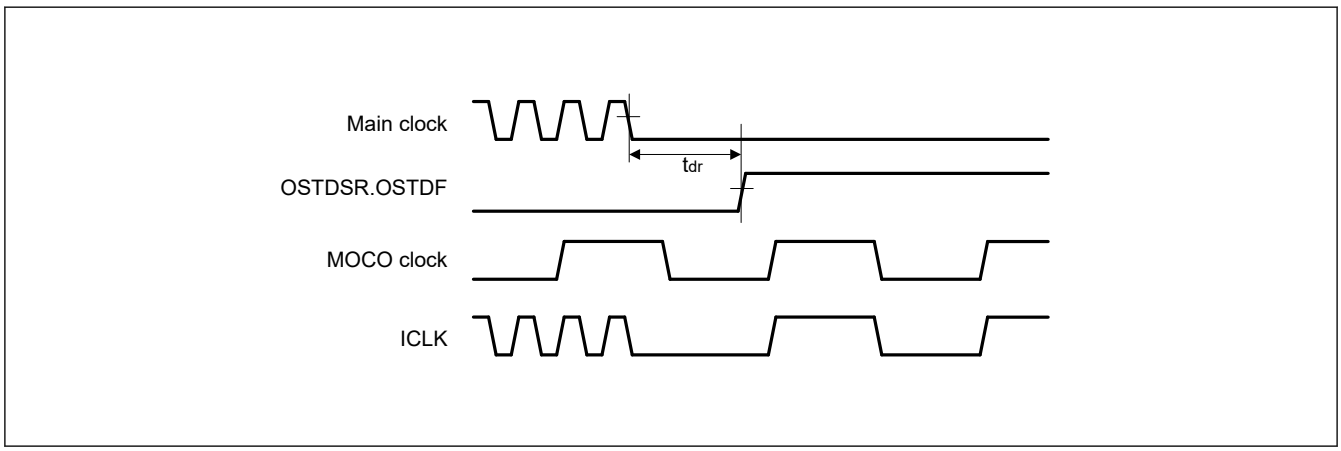


Figure 2.64 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.63 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.65, Figure 2.66
	When power supply fall	V_{POR}	1.46	1.50	1.54		Figure 2.65
Voltage detection circuit (LVD0)*1	When power supply rise	V_{det0_0}	2.73	2.9	3.01	V	Figure 2.67
	When power supply fall		2.68	2.85	2.96		
	When power supply rise	V_{det0_1}	2.44	2.59	2.70		
	When power supply fall		2.38	2.53	2.64		
	When power supply rise	V_{det0_2}	1.83	1.95	2.07		
	When power supply fall		1.78	1.90	2.02		
	When power supply rise	V_{det0_3}	1.66	1.75	1.88		
	When power supply fall		1.60	1.69	1.82		
Voltage detection circuit (LVD1)*2	When power supply rise	V_{det1_0}	3.05	3.17	3.29	V	Figure 2.68
	When power supply fall		2.98	3.10	3.22		
	When power supply rise	V_{det1_1}	2.95	3.06	3.17		
	When power supply fall		2.89	3.00	3.11		
	When power supply rise	V_{det1_2}	2.86	2.97	3.08		
	When power supply fall		2.79	2.90	3.01		
	When power supply rise	V_{det1_3}	2.74	2.85	2.96		
	When power supply fall		2.68	2.79	2.90		
	When power supply rise	V_{det1_4}	2.63	2.75	2.85		
	When power supply fall		2.58	2.68	2.78		
	When power supply rise	V_{det1_5}	2.54	2.64	2.75		
	When power supply fall		2.48	2.58	2.68		
	When power supply rise	V_{det1_6}	2.43	2.53	2.63		
	When power supply fall		2.38	2.48	2.58		
	When power supply rise	V_{det1_7}	2.16	2.26	2.36		
	When power supply fall		2.10	2.20	2.30		
	When power supply rise	V_{det1_8}	1.88	2	2.09		
	When power supply fall		1.84	1.96	2.05		
	When power supply rise	V_{det1_9}	1.78	1.9	1.99		
	When power supply fall		1.74	1.86	1.95		
	When power supply rise	V_{det1_A}	1.67	1.79	1.88		
	When power supply fall		1.63	1.75	1.84		
	When power supply rise	V_{det1_B}	1.65	1.7	1.78		
	When power supply fall		1.60	1.65	1.73		

Table 2.63 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection circuit (LVD2)*3	When power supply rise	V_{det2_0}	3.06	3.19	3.32	V	Figure 2.69
	When power supply fall		3.00	3.13	3.26		
	When power supply rise	V_{det2_1}	2.86	2.98	3.10		
	When power supply fall		2.80	2.92	3.04		
	When power supply rise	V_{det2_2}	2.66	2.78	2.90		
	When power supply fall		2.60	2.71	2.82		
	When power supply rise	V_{det2_3}	2.46	2.57	2.68		
	When power supply fall		2.40	2.50	2.60		
	When power supply rise	V_{det2_4}	2.26	2.36	2.46		Figure 2.69
	When power supply fall		2.20	2.30	2.40		
	When power supply rise	V_{det2_5}	2.06	2.15	2.24		
	When power supply fall		2.00	2.09	2.18		
	When power supply rise	V_{det2_6}	1.86	1.94	2.02		
	When power supply fall		1.80	1.88	1.96		
	When power supply rise	V_{det2_7}	1.66	1.73	1.80		
	When power supply fall		1.60	1.67	1.74		

Note: These characteristics apply when noise is not superimposed on the power supply.
Note 1. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL0[1:0] bits.
Note 2. # in the symbol $V_{det1\_\#}$ denotes the value of the LVD1CMPCR.LVD1LVL[3:0] bits.
Note 3. # in the symbol $V_{det2\_\#}$ denotes the value of the LVD2CMPCR.LVD2LVL[2:0] bits.

Table 2.64 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.9	—	ms	—
	LVD0: disable	t_{POR}	—	4.2	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	0.94	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.25	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.65, Figure 2.66
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.67
LVD1 response delay time*3		t_{det}	—	—	600	µs	Figure 2.68
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.69
Minimum VCC down time	POR	t_{VOFF}	500	—	—	µs	Figure 2.65
	LVD0		300	—	—	µs	Figure 2.67
	LVD1		300	—	—	µs	Figure 2.68
	LVD2		600	—	—	µs	Figure 2.69
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.66, VCC = below 1.0 V
LVD1 operation stabilization time (after LVD1 is enabled)		$T_{d\ (E-A)}$	—	—	350	µs	Figure 2.68
LVD2 operation stabilization time (after LVD2 is enabled)		$T_{d\ (E-A)}$	—	—	600	µs	Figure 2.69
Hysteresis width (POR)		V_{PORH}	—	10	—	mV	—

Table 2.64 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	60	—	mV	LVD0 selected
		—	70	—		V_{det1_0} to V_{det1_5} selected
		—	60	—		V_{det1_6} to V_{det1_7} selected
		—	50	—		V_{det1_8} to V_{det1_B} selected
		—	70	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

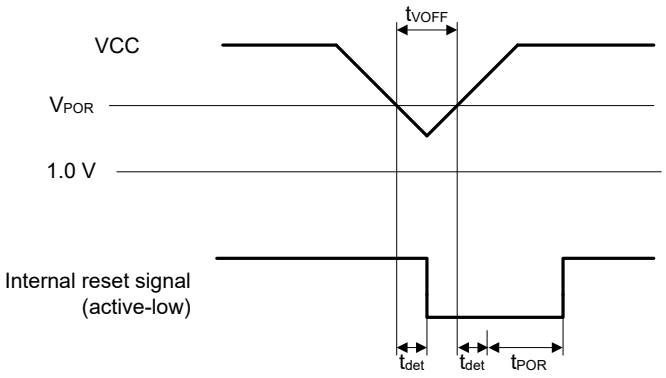
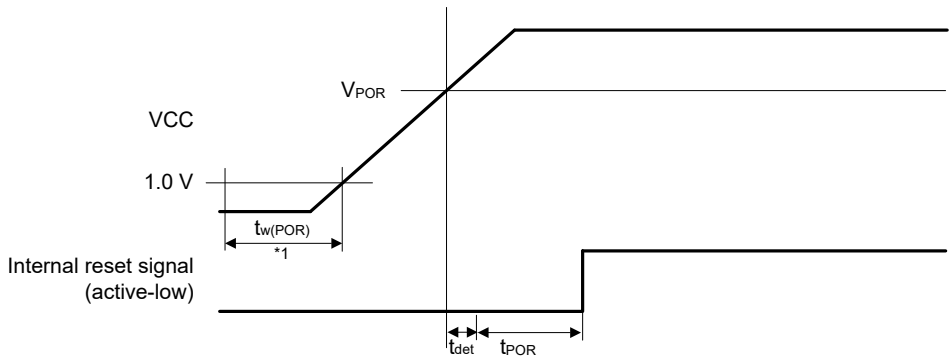


Figure 2.65 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.66 Power-on reset timing

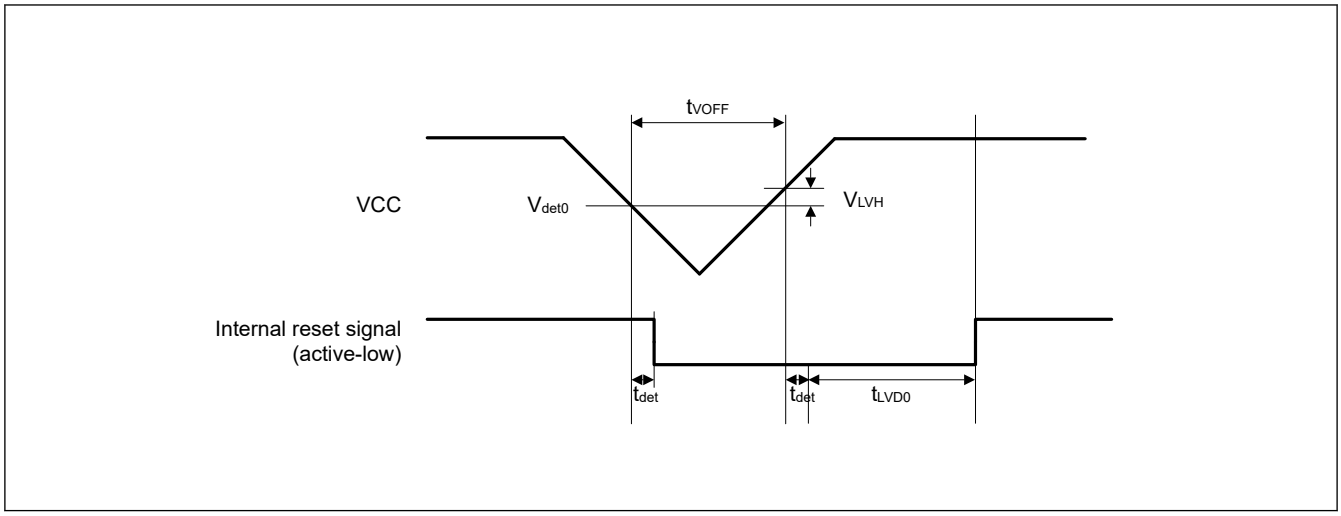


Figure 2.67 Voltage detection circuit timing (V_{det0})

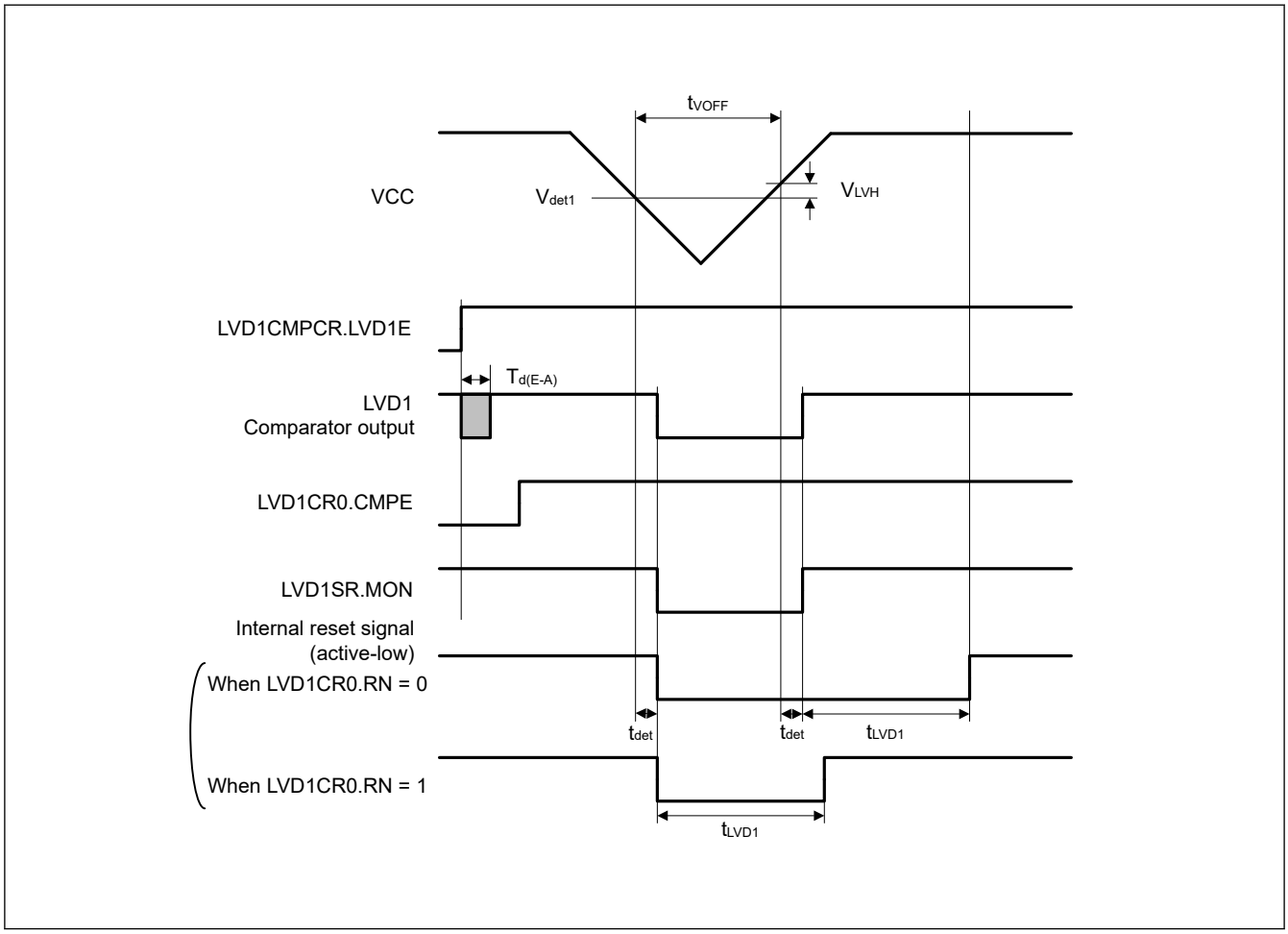


Figure 2.68 Voltage detection circuit timing (V_{det1})

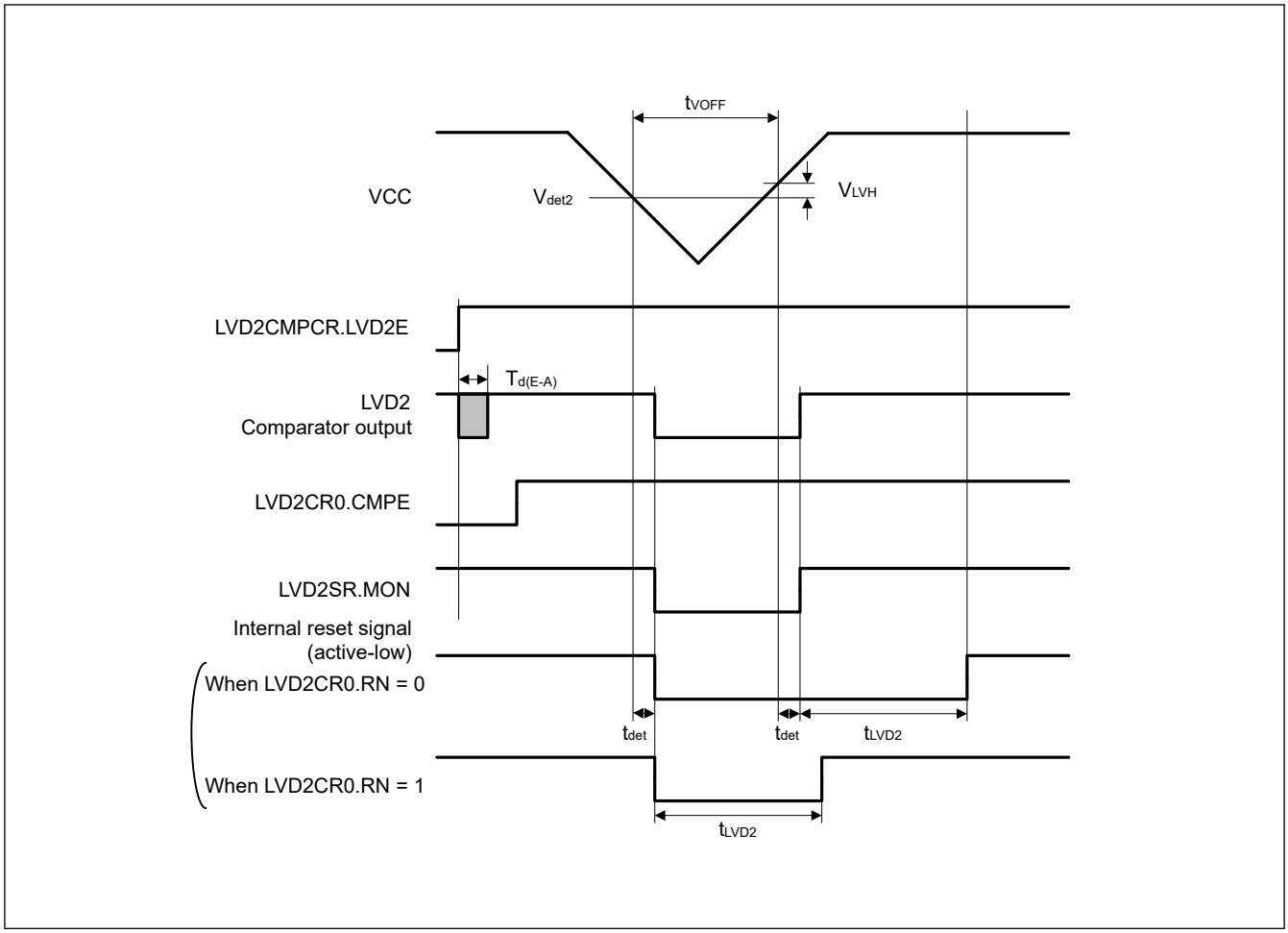


Figure 2.69 Voltage detection circuit timing (V_{det2})

2.10 CTSU Characteristics

Table 2.65 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	—

2.11 Comparator Characteristics

Table 2.66 ACMPLP characteristics (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range		V_{REF}	0	—	VCC-1.4	V	—
Input voltage range		V_I	0	—	VCC	V	—
Internal reference voltage*1		—	1.34	1.44	1.54	V	—
Output delay time	High-speed mode	T_d	—	—	1.2	µs	VCC = 3.0 V
	Low-speed mode		—	—	9	µs	
	Window mode		—	—	2	µs	
Offset voltage	High-speed mode	—	—	—	50	mV	—
	Low-speed mode	—	—	—	40	mV	—
	Window mode	—	—	—	60	mV	—

Table 2.66 ACMPLP characteristics (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Internal reference voltage for window mode		V_{RFH}	—	0.76 × VCC	—	V	—
		V_{RFL}	—	0.24 × VCC	—	V	—
Operation stabilization wait time	High-speed mode	T_{cmp}	100	—	—	μs	—
	Low-speed mode		200	—	—		

Note 1. The internal reference voltage can be selected as ACMPLP reference voltage only when 2.94 V ≤ VCC ≤ 3.6 V.

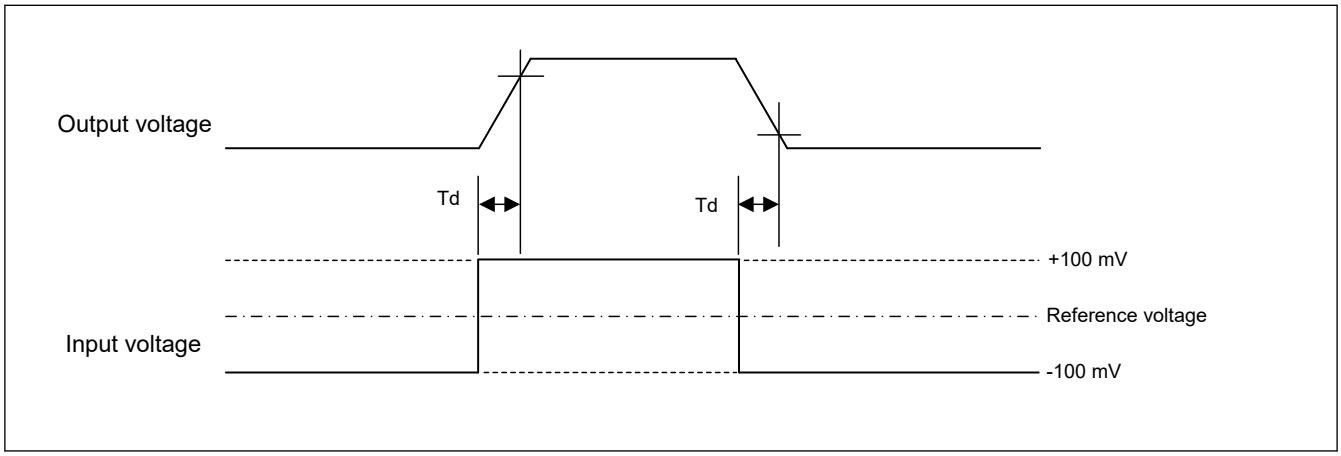


Figure 2.70 Output delay time

2.12 Segment LCD Controller Characteristics

2.12.1 External Resistance Division Method

(1) Static display mode

Table 2.67 External resistance division method LCD characteristics (1)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	—	VCC	V	—

(2) 1/2 bias method, 1/4 bias method

Table 2.68 External resistance division method LCD characteristics (2)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	—	VCC	V	—

(3) 1/3 bias method

Table 2.69 External resistance division method LCD characteristics (3)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	—	VCC	V	—

2.12.2 Internal Voltage Boosting Method (VL1 Reference)

(1) 1/3 bias method

Table 2.70 Internal voltage boosting method LCD characteristics (1)

Conditions: VCC = AVCC = 1.8 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4[*5] = 0.47 µF	VLCD[*1] = 0x04	0.97	1.01	1.04	V	—
			VLCD = 0x05	1.00	1.04	1.08	V	—
			VLCD = 0x06	1.04	1.07	1.11	V	—
			VLCD = 0x07	1.07	1.11	1.14	V	—
			VLCD = 0x08	1.10	1.14	1.18	V	—
			VLCD = 0x09	1.13	1.17	1.21	V	
			VLCD = 0x0A	1.16	1.21	1.25	V	—
			VLCD = 0x0B	1.20	1.24	1.28	V	—
			VLCD = 0x0C	1.23	1.27	1.32	V	—
			VLCD = 0x0D	1.26	1.31	1.35	V	—
			VLCD = 0x0E	1.29	1.34	1.38	V	—
			VLCD = 0x0F	1.33	1.37	1.42	V	
			VLCD = 0x10	1.36	1.40	1.45	V	—
			VLCD = 0x11	1.39	1.44	1.49	V	—
			VLCD = 0x12	1.42	1.47	1.52	V	—
			VLCD = 0x13	1.45	1.50	1.55	V	—
			VLCD = 0x14	1.49	1.54	1.59	V	—
			VLCD = 0x15	1.52	1.57	1.62	V	
			VLCD = 0x16	1.55	1.60	1.66	V	—
			VLCD = 0x17	1.58	1.64	1.69	V	—
			VLCD = 0x18	1.61	1.67	1.73	V	—
			VLCD = 0x19	1.65	1.70	1.76	V	—
			VLCD = 0x1A[*4]	1.68	1.74	1.79	V	—
Double output voltage	V_{L2}	C1 to C4[*5] = 0.47 µF		$2 \times V_{L1}$ - 5%	$2 \times V_{L1}$	$2 \times V_{L1}$ + 5%	V	—
Triple output voltage	V_{L4}	C1 to C4[*5] = 0.47 µF		$3 \times V_{L1}$ - 6%	$3 \times V_{L1}$	$3 \times V_{L1}$ + 6%	V	—
Reference voltage setup time[*2]	t_{VL1S}	—		10	—	—	ms	Figure 2.71
Voltage boost wait time[*3]	t_{VLWT}	—		500	—	—	ms	Figure 2.71

Note: 0x0E to 0x1A setting is permitted when using 5V LCD panel, 0x04 to 0x07 setting is permitted when using 3V LCD panel at 1/3 bias.

Note 1. Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL1 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 0) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. This setting is only available when VCC ≥ VL1.

Note 5. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

(2) 1/4 bias method

Table 2.71 Internal voltage boosting method LCD characteristics (2)

Conditions: VCC = AVCC = 1.8 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C5*1 = 0.47 µF	VLCD*2 = 0x04	0.97	1.01	1.04	V	—
			VLCD = 0x05	1.00	1.04	1.08	V	—
			VLCD = 0x06	1.04	1.07	1.11	V	—
			VLCD = 0x07	1.07	1.11	1.14	V	—
			VLCD = 0x08	1.10	1.14	1.18	V	—
			VLCD = 0x09	1.13	1.17	1.21	V	
			VLCD = 0x0A	1.16	1.21	1.25	V	—
			VLCD = 0x0B	1.20	1.24	1.28	V	—
			VLCD = 0x0C	1.23	1.27	1.32	V	—
			VLCD = 0x0D	1.26	1.31	1.35	V	—
Double output voltage	V_{L2}	C1 to C5*1 = 0.47 µF		2 × V_{L1} - 5%	2 × V_{L1}	2 × V_{L1} + 5%	V	—
Triple output voltage	V_{L3}	C1 to C5*1 = 0.47 µF		3 × V_{L1} - 6%	3 × V_{L1}	3 × V_{L1} + 6%	V	—
Quadruple output voltage	V_{L4}*5	C1 to C5*1 = 0.47 µF		4 × V_{L1} - 6%	4 × V_{L1}	4 × V_{L1} + 6%	V	—
Reference voltage setup time*3	t_{VL1S}	—		10	—	—	ms	Figure 2.71
Voltage boost wait time*4	t_{VLWT}	—		500	—	—	ms	Figure 2.71

Note 1. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL3 and GND

C5: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = C5 = 0.47 µF ±30%

Note 2. Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL1 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 3. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 0) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 5. V_{L4} must be 3.6 V or lower.

2.12.3 Internal Voltage Boosting Method (VL2 Reference)

(1) 1/3 bias method

Table 2.72 Internal voltage boosting method LCD characteristics (3) (1 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
Half output voltage	V_{L1}	C1 to C4*1 = 0.47 µF	1/2 × VL2 - 5%	1/2 × VL2	1/2 × VL2 + 5%	V	—

Table 2.72 Internal voltage boosting method LCD characteristics (3) (2 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L2}	C1 to C4[*1] = 0.47 µF	VLCD[*2] = 0x84	1.94	2.02	2.11	V	—
			VLCD = 0x85	2.00	2.09	2.18	V	—
			VLCD = 0x86	2.07	2.16	2.25	V	—
			VLCD = 0x87	2.13	2.22	2.32	V	—
			VLCD = 0x88	2.19	2.29	2.39	V	—
			VLCD = 0x89	2.26	2.36	2.46	V	—
			VLCD = 0x8A	2.32	2.42	2.53	V	—
			VLCD = 0x8B	2.39	2.49	2.59	V	—
			VLCD = 0x8C	2.45	2.56	2.66	V	—
			VLCD = 0x8D	2.51	2.62	2.73	V	—
			VLCD = 0x8E	2.58	2.69	2.80	V	—
			VLCD = 0x8F	2.64	2.76	2.87	V	—
			VLCD = 0x90	2.70	2.82	2.94	V	—
			VLCD = 0x91	2.77	2.89	3.01	V	—
			VLCD = 0x92	2.83	2.96	3.08	V	—
			VLCD = 0x93	2.90	3.02	3.15	V	—
			VLCD = 0x94	2.96	3.09	3.22	V	—
			VLCD = 0x95	3.02	3.15	3.29	V	—
			VLCD = 0x96	3.09	3.22	3.35	V	—
			VLCD = 0x97	3.15	3.29	3.42	V	—
			VLCD = 0x98	3.21	3.35	3.49	V	—
			VLCD = 0x99	3.28	3.42	3.56	V	—
			VLCD = 0x9A	3.34	3.49	3.63	V	—
3/2 output voltage	V_{L4}[*5]	C1 to C4[*1] = 0.47 µF		3/2 × V_{L2} - 6%	3/2 × V_{L2}	3/2 × V_{L2} + 6%	V	—
Reference voltage setup time[*3]	t_{VL2S}	—		10	—	—	ms	Figure 2.71
Voltage boost wait time[*4]	t_{VLWT}	—		500	—	—	ms	Figure 2.71

Note: 0x8E to 0x9A setting is permitted when using 5V LCD panel, 0x84 to 0x87 setting is permitted when using 3V LCD panel at 1/3 bias.

Note 1. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 2. Bit [7] (MDSET[2]) of register VLCD is set to 1 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL2 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 3. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 1) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 5. V_{L4} must be 5.5 V or lower.

2.12.4 Capacitor Split Method (VCC Reference)

(1) 1/3 bias method

Table 2.73 Capacitor split method LCD characteristics (1)

Conditions: VCC = AVCC = 2.2 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage	V_{L4}	C1 to C4*2 = 0.47 µF	—	VCC	—	V	—
VL2 voltage	V_{L2}	C1 to C4*2 = 0.47 µF	2 / 3 × V_{L4} - 3%	2 / 3 × V_{L4}	2 / 3 × V_{L4} + 3%	V	—
VL1 voltage	V_{L1}	C1 to C4*2 = 0.47 µF	1 / 3 × V_{L4} - 3%	1 / 3 × V_{L4}	1 / 3 × V_{L4} + 3%	V	—
Capacitor split wait time*1	t_{WAIT}	—	100	—	—	ms	Figure 2.71

Note: Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 10 for capacitor split method (VCC reference).
Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

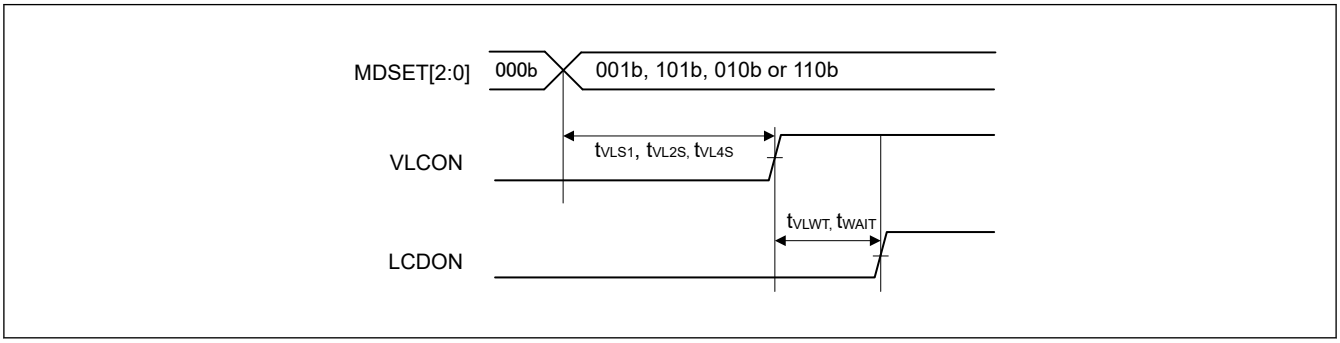


Figure 2.71 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time

2.12.5 Capacitor Split Method (VL4 Reference)

(1) 1/3 bias method

Table 2.74 Capacitor split method LCD characteristics (3)

Conditions: VCC = AVCC = 3.2 V to 3.6 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage	V_{L4}	C1 to C4*2 = 0.47 µF	2.89	3.04	3.20	V	—
VL2 voltage	V_{L2}	C1 to C4*2 = 0.47 µF	1.89	2.03	2.17	V	—
VL1 voltage	V_{L1}	C1 to C4*2 = 0.47 µF	0.94	1.01	1.08	V	—
Reference voltage setup time*3	t_{VL4S}	—	10	—	—	ms	Figure 2.71
Capacitor split wait time*1	t_{WAIT}	—	100	—	—	ms	Figure 2.71

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 3. Bit [7] (MDSET[2]) of register VLCD is set to 1 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 10 for capacitor split method (VL4 reference).

2.13 Flash Memory Characteristics

2.13.1 Code Flash Memory Characteristics

Table 2.75 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +105 °C
			10	—	—	Year	T_a = +125 °C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.76 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	—	128	1064	—	44.2	420	µs
Erasure time	2-KB	t_{E2K}	—	14.1	390	—	5.5	214	ms
Blank check time	8-byte	t_{BC8}	—	—	67.7	—	—	8.6	µs
	2-KB	t_{BC2K}	—	—	7538	—	—	272	µs
Erase suspended time		t_{SED}	—	—	33.4	—	—	10.7	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	10.7	µs
Configuration Set time		t_{CFGS}	—	27	494	—	11	255	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.

Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.77 Code flash characteristics (3) (1 of 2)

Middle-speed operating mode

Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	—	128	1064	—	50.6	468	µs
Erasure time	2-KB	t_{E2K}	—	14.1	390	—	6.32	231	ms
Blank check time	8-byte	t_{BC8}	—	—	67.7	—	—	13.3	µs
	2-KB	t_{BC2K}	—	—	7538	—	—	947	µs

Table 2.77 Code flash characteristics (3) (2 of 2)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter	Symbol	ICLK = 1 MHz			ICLK = 8 MHz*1			Unit
		Min	Typ	Max	Min	Typ	Max	
Erase suspended time	t_{SED}	—	—	33.4	—	—	13.1	µs
Forced stop time	t_{FD}	—	—	33.4	—	—	13.1	µs
Configuration Set time	t_{CFGS}	—	27	494	—	12	277	ms
Flash memory mode transition wait time 1	t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2	t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 3.6 V

Table 2.78 Code flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	8-byte	t_{P8}	—	128	1064	µs
Erasure time	2-KB	t_{E2K}	—	14.1	390	ms
Blank check time	8-byte	t_{BC8}	—	—	67.7	µs
	2-KB	t_{BC2K}	—	—	7538	µs
Erase suspended time		t_{SED}	—	—	33.4	µs
Forced stop time		t_{FD}	—	—	33.4	µs
Configuration Set time		t_{CFGS}	—	27	494	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.13.2 Data Flash Memory Characteristics

Table 2.79 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2 *3	—	—	Year	Ta = +105 °C
			10*2 *3	—	—		Ta = +125 °C
	After 100000 times of N_{DPEC}		5*2 *3	—	—		Ta = +105 °C
	After 1000000 times of N_{DPEC}		—	1*2 *3	—		Ta = +25 °C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 256 times for different addresses in 256-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.80 Data flash characteristics (2)

High-speed operating mode
Conditions: VCC = AVCC0 = 1.8 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	112	903	—	33.9	317	µs
Erasure time	256-byte	t_{DE256}	—	14.1	390	—	5.50	214	ms
Blank check time	1-byte	t_{DBC1}	—	—	67.7	—	—	8.6	µs
	256-byte	t_{DBC256}	—	—	7538	—	—	272	µs
Suspended time during erasing		t_{DSED}	—	—	33.4	—	—	10.7	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	10.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.81 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	112	903	—	39.7	359	µs
Erasure time	256-byte	t_{DE256}	—	14.1	390	—	6.32	231	ms
Blank check time	1-byte	t_{DBC1}	—	—	67.7	—	—	13.3	µs
	256-byte	t_{DBC256}	—	—	7538	—	—	947	µs
Suspended time during erasing		t_{DSED}	—	—	33.4	—	—	13.1	µs
Forced stop time		t_{FD}	—	—	33.4	—	—	13.1	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC0 ≤ 3.6 V

Table 2.82 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC0 = 1.6 to 3.6 V

Parameter		Symbol	ICLK = 1 MHz			Unit
			Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	112	903	µs
Erasure time	256-byte	t_{DE256}	—	14.1	390	ms
Blank check time	1-byte	t_{DBC1}	—	—	67.7	µs
	256-byte	t_{DBC256}	—	—	7538	µs
Suspended time during erasing		t_{DSED}	—	—	33.4	µs
Forced stop time		t_{FD}	—	—	33.4	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory.
Note: The frequency accuracy of FCLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.13.3 Serial Wire Debug (SWD)

Table 2.83 SWD characteristics (1)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.72
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	3	—	—	ns	Figure 2.73
SWDIO hold time	t_{SWDH}	13	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.84 SWD characteristics (2)

Conditions: VCC = AVCC0 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.72
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.73
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

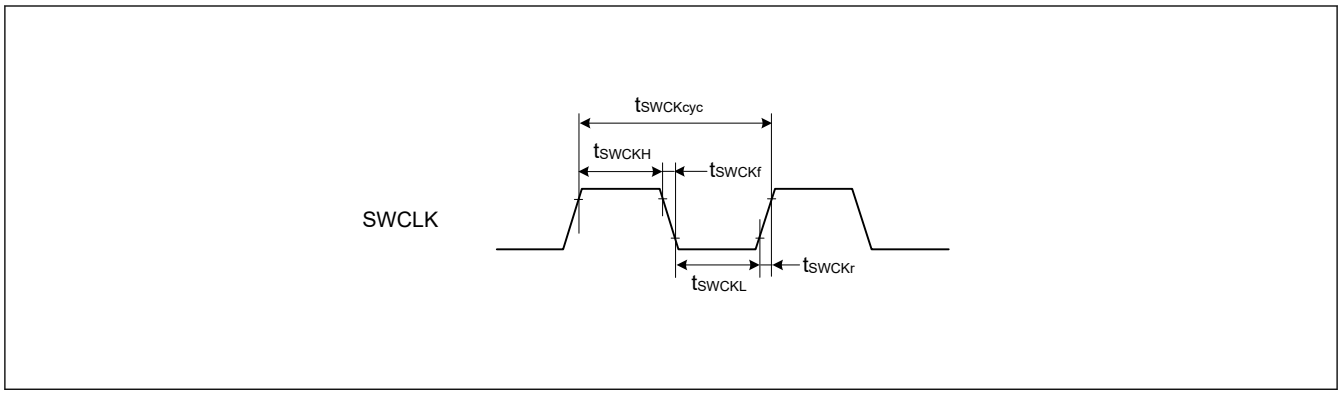


Figure 2.72 SWD SWCLK timing

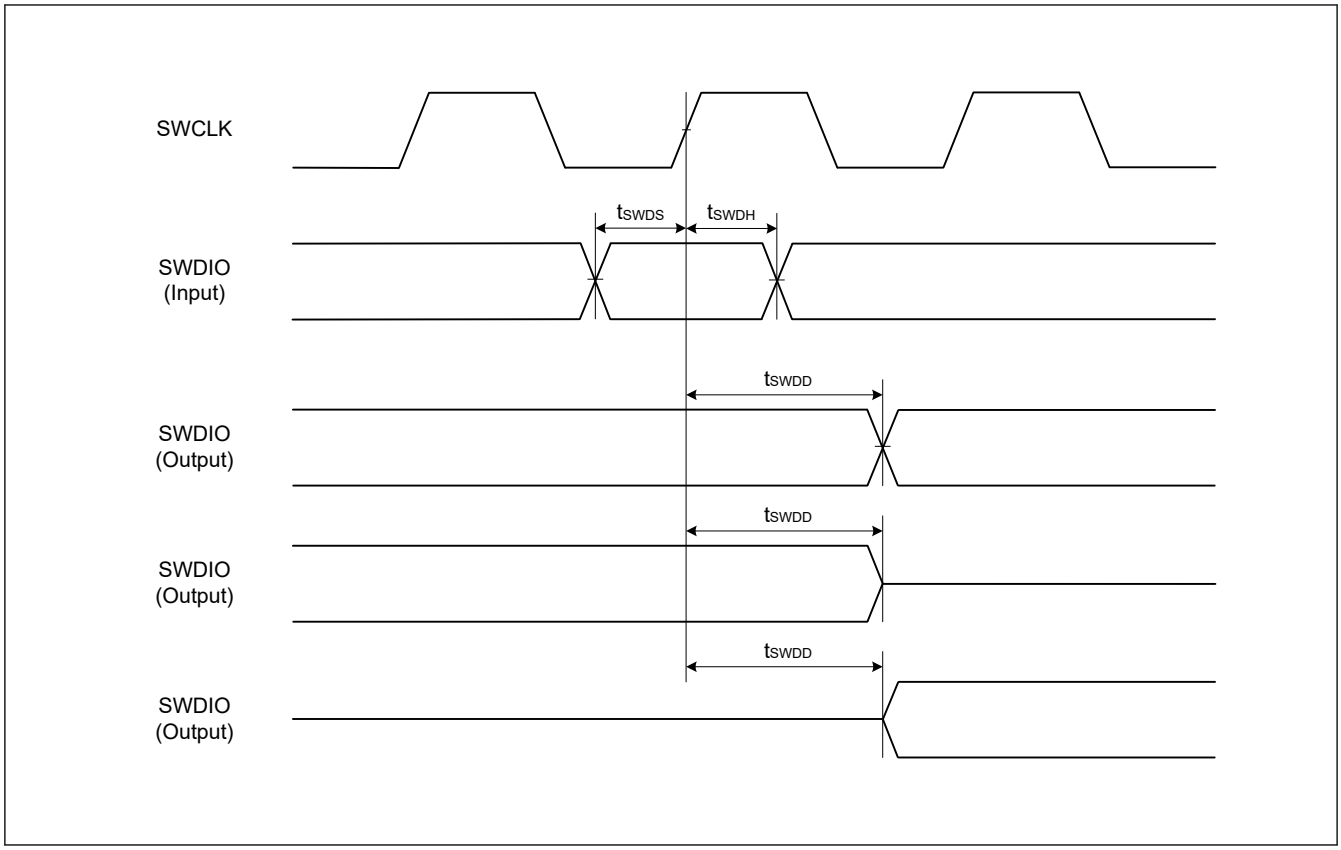


Figure 2.73 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

Table A1.1 Port states in each processing mode

Function	Pin function	Reset	Software Standby mode
Mode	MD	Pull-up	Keep-O
IRQ	IRQx	Hi-Z	Keep-O*1
AGT	AGTIOn	Hi-Z	AGTIOn input
	AGTOn/AGTOAn/AGTOBn	Hi-Z	AGTOn/AGTOAn/AGTOBn output
SCI	RXD0	Hi-Z	Keep-O*1
IIC	SCLn/SDAn	Hi-Z	Keep-O*1
I3C	I3C_SCL0/I3C_SDA0	Hi-Z	Keep-O*1
UARTA	CLKAn	Hi-Z	CLKAn output
	RxDAn	Hi-Z	RxDAn input
USBFS	USB_OVRCURx/USB_VBUS	Hi-Z	Keep-O*1
	USB_DP/USB_DM	Hi-Z	Keep-O*2
RTC	RTCICx	Hi-Z	RTCICx input
	RTCOUT	Hi-Z	RTCOUT output
ACMPLP	CMPINn/CMPREFn	Hi-Z	CMPINn/CMPREFn input
	VCOUT	Hi-Z	VCOUT output
CLKOUT	CLKOUT	Hi-Z	CLKOUT output
DAC	DA0	Hi-Z	D/A output retained
SLCDC	SEGx/COMx	Hi-Z	SEGx/COMx output
	VLx/CAPH/CAPL	Hi-Z	VLx/CAPH/CAPL input
Others	—	Hi-Z	Keep-O

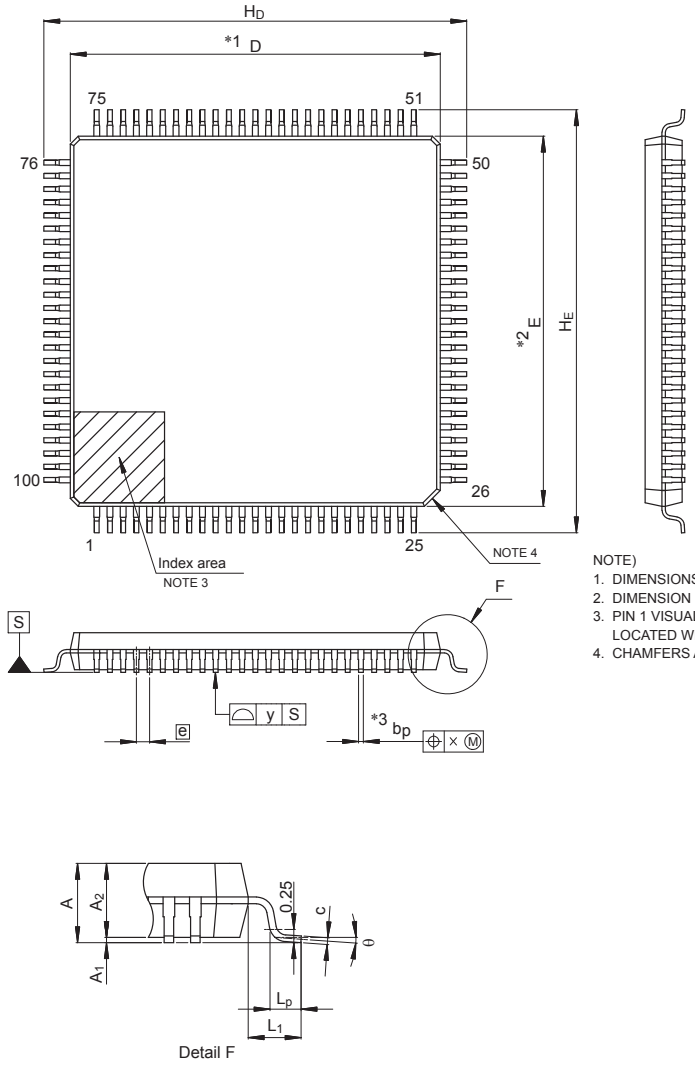
Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Note 1. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 2. Input is enabled while the pin is used as an input pin.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm

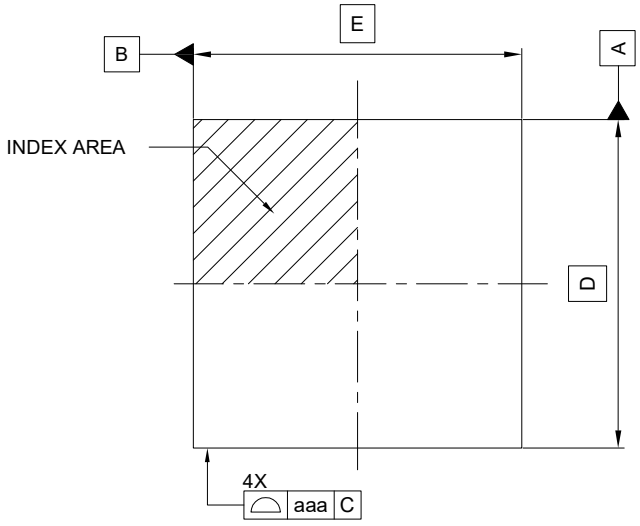


NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

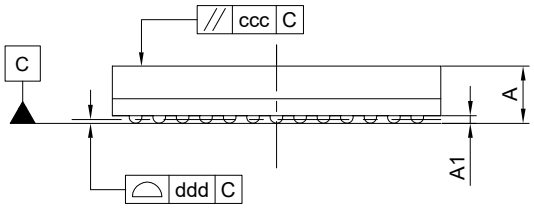
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

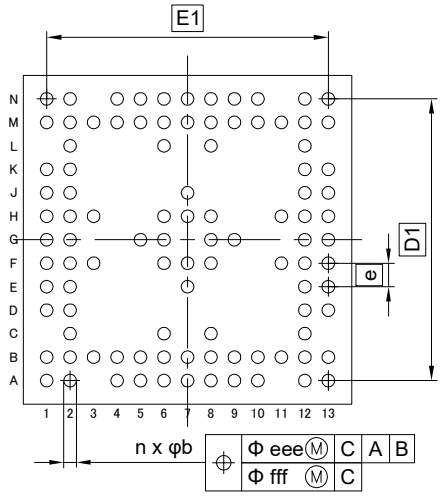
Figure A2.1 LQFP 100-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA100-7x7-0.50	PLBG0100KB-A	0.12



TOP VIEW



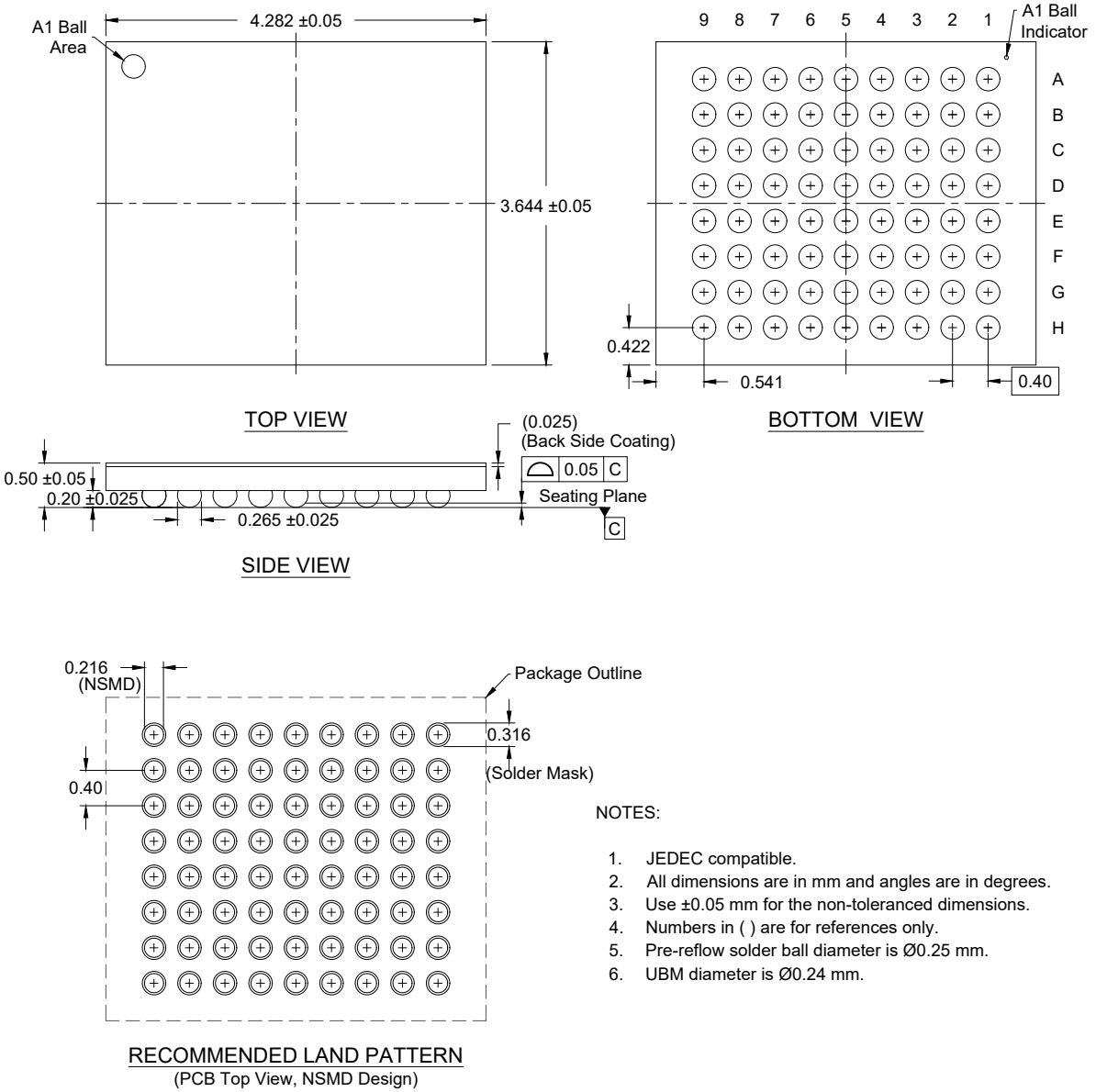


BOTTOM VIEW

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	7.00	—
E	—	7.00	—
D1	—	6.00	—
E1	—	6.00	—
A	—	—	1.30
A1	0.11	—	—
b	0.22	0.27	0.32
e	—	0.50	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.15
fff	—	—	0.05
n	—	100	—

Figure A2.2 BGA 100-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
S-UFBGA72-4.28x3.64-0.40	SUBG0072LB-A	0.02



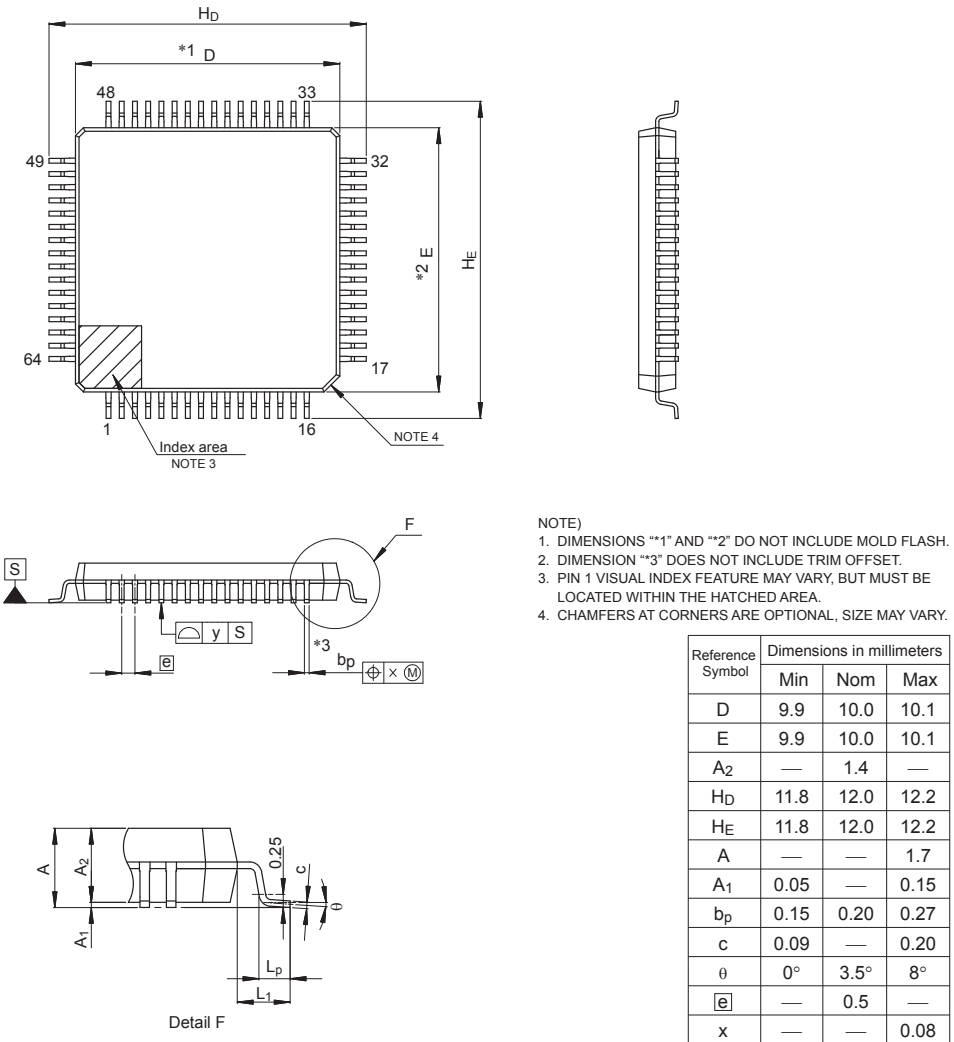
NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solder ball diameter is Ø0.25 mm.
6. UBM diameter is Ø0.24 mm.

Figure A2.3 WLCSP 72-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm

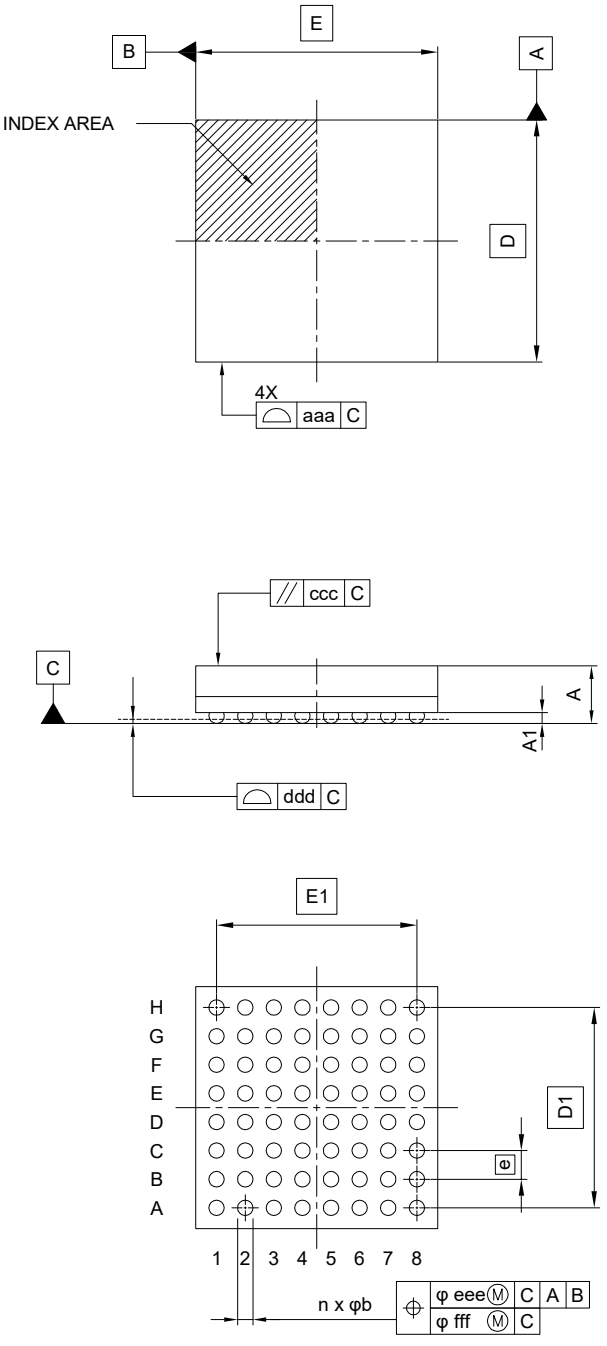


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A2.4 LQFP 64-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA64-5.5x5.5-0.65	PLBG0064JD-A	0.08

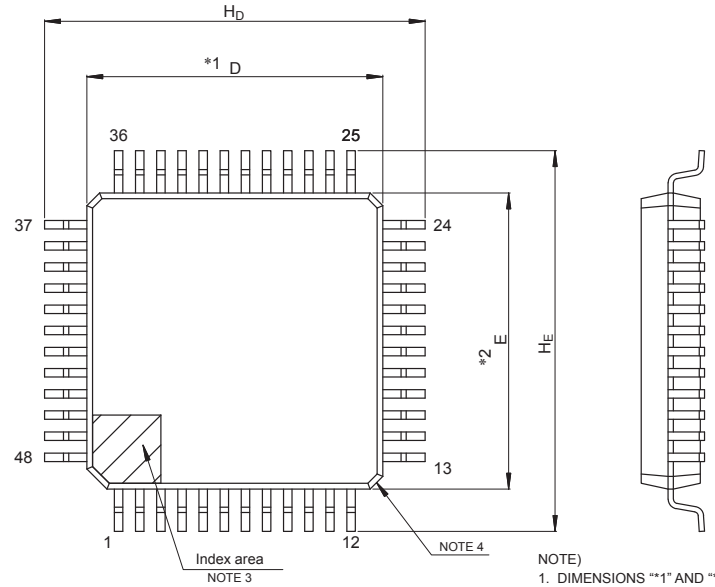


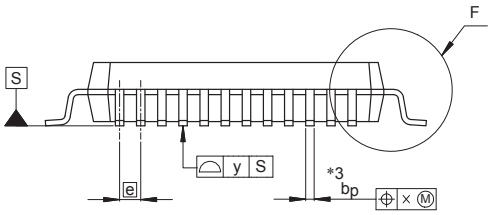
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	5.50	—
E	—	5.50	—
D1	—	4.55	—
E1	—	4.55	—
A	—	—	1.40
A1	0.20	—	—
b	0.31	0.36	0.41
e	—	0.65	—
aaa	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.15
fff	—	—	0.08
n	—	64	—

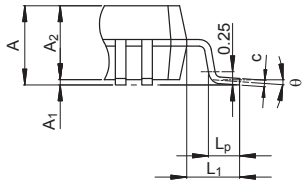
Figure A2.5 BGA 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







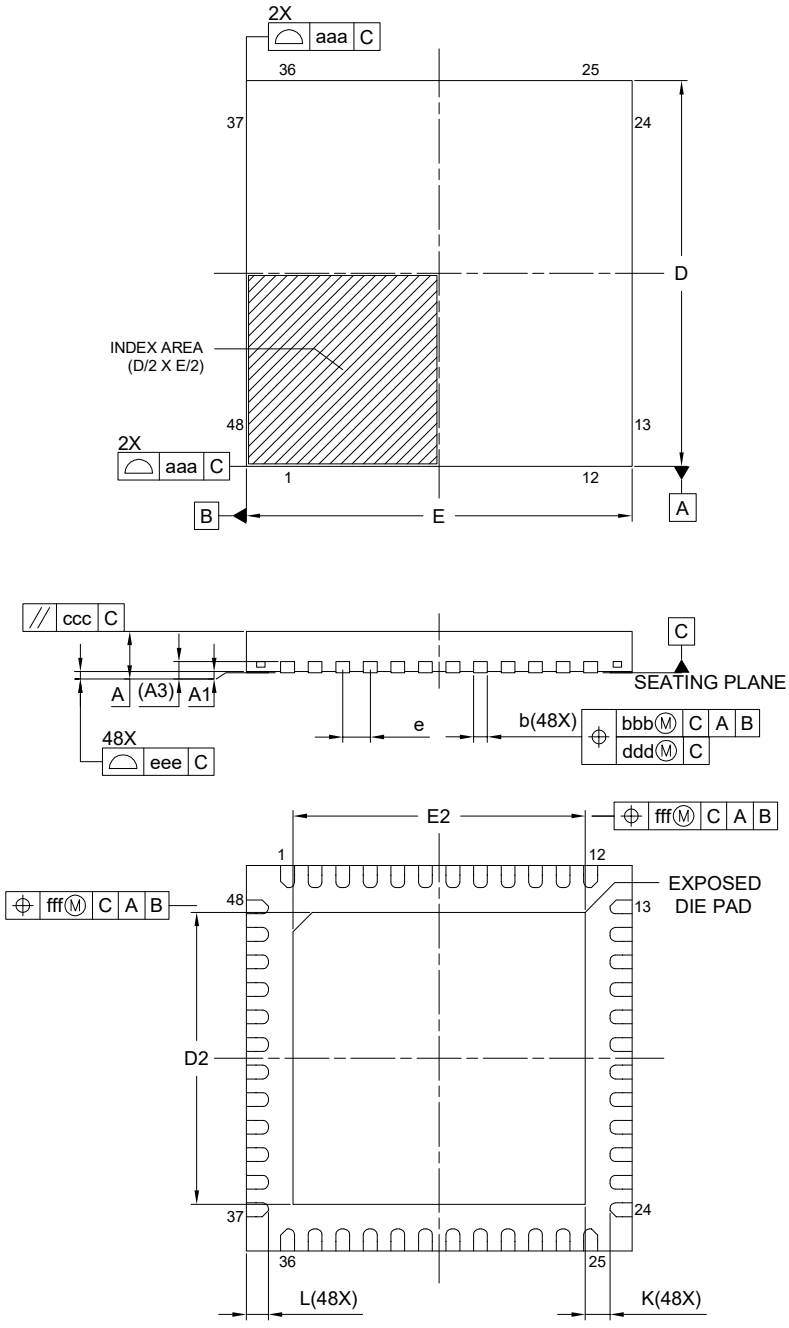
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A2.6 LQFP 48-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure A2.7 QFN 48-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Master Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	Special Function Register	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x4001_B000
FCACHE	Flash Security Attribution Control	0x4001_C100
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4001_F000
PORT1	Port 1 Control Registers	0x4001_F020
PORT2	Port 2 Control Registers	0x4001_F040
PORT3	Port 3 Control Registers	0x4001_F060
PORT4	Port 4 Control Registers	0x4001_F080
PORT5	Port 5 Control Registers	0x4001_F0A0
PORT6	Port 6 Control Registers	0x4001_F0C0
PORT7	Port 7 Control Registers	0x4001_F0E0
PORT8	Port 8 Control Registers	0x4001_F100
PFS	Pmn Pin Function Control Register	0x4001_F800
ELC	Event Link Controller	0x4008_2000
RTC	Realtime Clock	0x4008_3000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600

Table A3.1 Peripheral base address (2 of 2)

Name	Description	Base address
MSTP	Module Stop Control A, B, C, D, E	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000
USBFS	USB 2.0 FS Module	0x4009_0000
UARTA	Serial Interface UARTA	0x4009_7000
SSIE0	Serial Sound Interface Enhanced (SSIE)	0x4009_D000
IIC0	Inter-Integrated Circuit 0	0x4009_F000
CANFD	CANFD Module	0x400B_0000
CTSU	Capacitive Touch Sensing Unit	0x400D_0000
SLCDC	Segment LCD Controller/Driver	0x400D_4000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
ACMPLP	Low-Power Analog Comparator	0x400F_4000
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI1	Serial Communication Interface 1	0x4011_8100
SCI3	Serial Communication Interface 3	0x4011_8300
SCI4	Serial Communication Interface 4	0x4011_8400
SCI5	Serial Communication Interface 5	0x4011_8500
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000
I3C	I3C Bus Interface	0x4011_F000
ECCMB	Error correction circuit for MBRAM	0x4012_F000
GPT320	General PWM 32-Bit Timer 0	0x4016_9000
GPT321	General PWM 32-Bit Timer 1	0x4016_9100
GPT162	General PWM 16-Bit Timer 2	0x4016_9200
GPT163	General PWM 16-Bit Timer 3	0x4016_9300
GPT164	General PWM 16-Bit Timer 4	0x4016_9400
GPT165	General PWM 16-Bit Timer 5	0x4016_9500
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLCN	Flash I/O Registers	0x407E_C000
FACI	Flash Application Command Interface	0x407F_E000
QSPI	Quad-SPI	0x6400_0000
CPU_OCD	On-Chip Debug	0x8000_0000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table A3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	4	5	4	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Security Attribution Control
SYSC	0x4001_E000	0x4001_E5FF	6	5	6	5	ICLK	System Control
PORTn, PFS	0x4001_F000	0x4001_FFFF	5*2	4	5*2	4	ICLK	Port n Control Registers, Pmn Pin Function Control Register
ELC, RTC, IWDT, WDT, CAC, MSTP, POEG	0x4008_2000	0x4008_AFFF	5	4	2 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control, Port Output Enable Module for GPT
USBFS	0x4009_0000	0x4009_0FFF	6	5	3 to 6	3 to 5	PCLKB	USB 2.0 FS Module
UARTA	0x4009_7000	0x4009_7FFF	4	3	1 to 4	1 to 3	PCLKB	Serial Interface UARTA
SSIE0, IICn, IIC0WU, CANFD, CTSU	0x4009_D000	0x400D_0FFF	5	4	2 to 5	2 to 4	PCLKB	Serial Sound Interface Enhanced, Inter-Integrated Circuit n, Inter-Integrated Circuit 0 Wake-up Unit, CANFD Module, Capacitive Touch Sensing Unit

Table A3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
SLCDC	0x400D_4000	0x400D_4FFF	4	3	1 to 4	1 to 3	PCLKB	Segment LCD Controller/Driver
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	4 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n
ACMPLP	0x400F_4000	0x400F_4FFF	4	3	1 to 4	1 to 3	PCLKB	Low-Power Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*4	4*4	2 to 5*4	2 to 4*4	PCLKA	Serial Peripheral Interface n
I3C, ECCMB	0x4011_F000	0x4012_FFFF	5	4	2 to 5	2 to 4	PCLKA	I3C Bus Interface, Error correction circuit for MBRAM
GPT32n, GPT16n, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 32-Bit Timer n, General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC120, DAC12	0x4017_0000	0x4017_1FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter 0, 12-bit D/A converter
QSPI	0x6400_0000	0x6400_000F	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0010	0x6400_0013	25 to *5	6 to *5	25 to *5	5 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0014	0x6400_0037	5	14 to *5	2 to 5	14 to *5	PCLKA	Quad-SPI
QSPI	0x6400_0804	0x6400_0807	4	3	1 to 4	1 to 3	PCLKA	Quad-SPI

Table A3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = FCLK		ICLK > FCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
FLCN, FACI	0x407E_C000	0x407F_EFFF	5	4	3 to 5	2 to 4	FCLK	Flash I/O Registers, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.
Note 2. The access cycles of the PRCNT2 and PFS registers depend on PRWCNTR.
Note 3. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table A3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table A3.2.
Note 4. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table A3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table A3.2.
Note 5. The access cycles depend on the QSPI bus cycles.

Revision History

Revision 1.10 — January 31, 2025

First edition, issued

Revision 1.20 — October 10, 2025

Features:
- Updated product description

1. Overview:
- Updated Table 1.14 Product list

2. Electrical Characteristics:
- Updated 2. Electrical Characteristics
- Updated Table 2.5 I/O I_{OH}, I_{OL}
- Updated Table 2.20 Power consumption of each unit
- Updated Table 2.21 Outline of operation for each unit
- Updated Table 2.26 Clock timing
- Updated 2.3.12 I3C Timing
- Updated Table 2.79 Data flash characteristics

Appendix:
- Added Figure A2.2 BGA 100-pin
- Added Figure A2.3 WLCSP 72-pin
- Added Figure A2.5 BGA 64-pin
- Updated Table A3.1 Peripheral base address
- Updated Table A3.2 Access cycles

Revision 1.30 — April 28, 2026

1. Overview:
- Updated 1.3 Part Numbering

2. Electrical Characteristics:
- Updated Table 2.1 Absolute maximum ratings
- Updated Table 2.72 Internal voltage boosting method LCD characteristics (3)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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