RA4T1 Group
Renesas Microcontrollers

R01DS0415EJ0130
Rev.1.30
Sep 12, 2025

The RA4T1 Group delivers up to 100 MHz of CPU performance using an Arm® Cortex®-M33 core with a code flash memory ranging from 128 KB to 256 KB, 4 KB of data flash memory, and 40 KB of SRAM. The RA4T1 Group offers a wide set of peripherals, including CANFD, I3C, and ADC.

Features

Arm® Cortex®-M33 Core

- Armv8-M architecture with the main extension
- Maximum operating frequency: 100 MHz
- Arm Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by LOCO or system clock
- CoreSight™ ETM-M33

Memory

- Up to 256 KB code flash memory
- 4 KB data flash memory (100,000 program/erase (P/E) cycles)
- 40 KB SRAM

Connectivity

- Serial Communications Interface (SCI) × 2
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Smart card interface
  - Simple IIC
  - Simple SPI
  - Manchester coding
- I3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2
- CAN with Flexible Data-rate (CANFD)

Analog

- 12-bit A/D Converter (ADC12)
  - Sample-and-hold circuits × 3
  - Programmable Gain Amplifier × 3
- High-Speed Analog Comparator (ACMPHS) × 3
- 12-bit D/A Converter (DAC12) × 2
- Temperature Sensor (TSN)

Timers

- General PWM Timer 16-bit Enhanced (GPT16E) × 6
- Low Power Asynchronous General Purpose Timer (AGT) × 2

Security

- Arm® TrustZone®
  - Up to three regions for the code flash
  - Up to two regions for the data flash
  - Up to three regions for the SRAM
  - Individual secure or non-secure security attribution for each peripheral
- 128-bit unique ID
- True Random Number Generator (TRNG)
- Pin function
  - Secure pin multiplexing

System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- DMA Controller (DMAC) × 8
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Watchdog Timer (WDT)
- Independent Watchdog Timer (IWDT)

Data Processing Accelerator

- Trigonometric Function Unit (TFU)

Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL
- Clock out support

General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

Operating Voltage

- VCC: 2.7 to 3.6 V

Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 48-pin LQFP (7 mm × 7 mm, 0.5 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 32-pin QFN (5 mm × 5 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M33 core running up to 100 MHz with the following features:

- Up to 256 KB code flash memory
- 40 KB SRAM
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M33 core	• Maximum operating frequency: up to 100 MHz • Arm Cortex-M33 core: – Armv8-M architecture with security extension – Revision: r0p4-00rel0 • Arm Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure and Non-secure instance – Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK) • CoreSight™ ETM-M33

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 256 KB of code flash memory.
Data flash memory	4 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI/SWD boot mode
Resets	The MCU provides 14 resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The LVD module consists of three separate voltage level detectors (LVD0, LVD1, LVD2). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • PLL • Clock out support

Table 1.3 System (2 of 2)

Feature	Functional description
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), the DMA Controller (DMAC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has one Memory Protection Unit (MPU).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.
DMA Controller (DMAC)	The MCU includes an 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16E × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The low power Asynchronous General Purpose Timer (AGT) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 2 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0, 9) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I3C bus interface (I3C)	The I3C bus interface (I3C) has one channel. The I3C module conforms with and provides a subset of the NXP I2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has 2 channels. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers and 32 receive buffers.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter (ADC12) with sample-and-hold circuits and programmable gain amplifiers (PGA) are provided. Up to 12 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A converter (DAC12) is provided.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section x, High-Speed Analog Comparator.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.

Table 1.10 Data processing accelerator

Feature	Functional description
Trigonometric function unit (TFU)	Calculation of sine, cosine, arctangent, and sqrt(x2 + y2) ● A sine and cosine can be simultaneously calculated ● An arctangent and sqrt(x2 + y2) can be simultaneously calculated

Table 1.11 I/O ports

Feature	Functional description
Programmable I/O ports	• I/O ports for the 64-pin LQFP – I/O pins: 45 – Input pins: 5 – Pull-up resistors: 46 – N-ch open-drain outputs: 45 – 5-V tolerance: 11 • I/O ports for the 48-pin LQFP – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin LQFP – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4 • I/O ports for the 48-pin QFN – I/O pins: 29 – Input pins: 5 – Pull-up resistors: 30 – N-ch open-drain outputs: 29 – 5-V tolerance: 6 • I/O ports for the 32-pin QFN – I/O pins: 16 – Input pins: 5 – Pull-up resistors: 17 – N-ch open-drain outputs: 16 – 5-V tolerance: 4

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

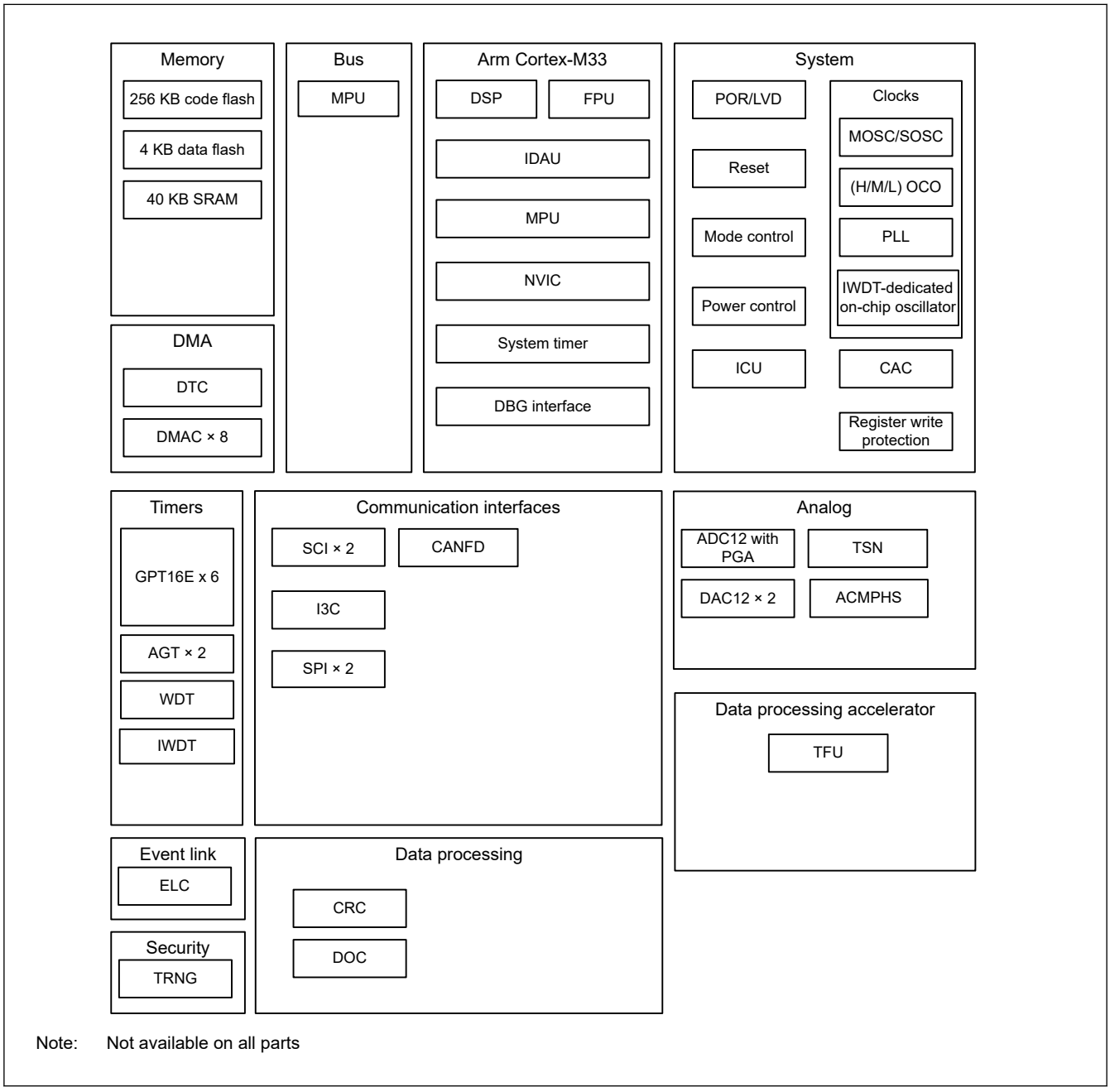
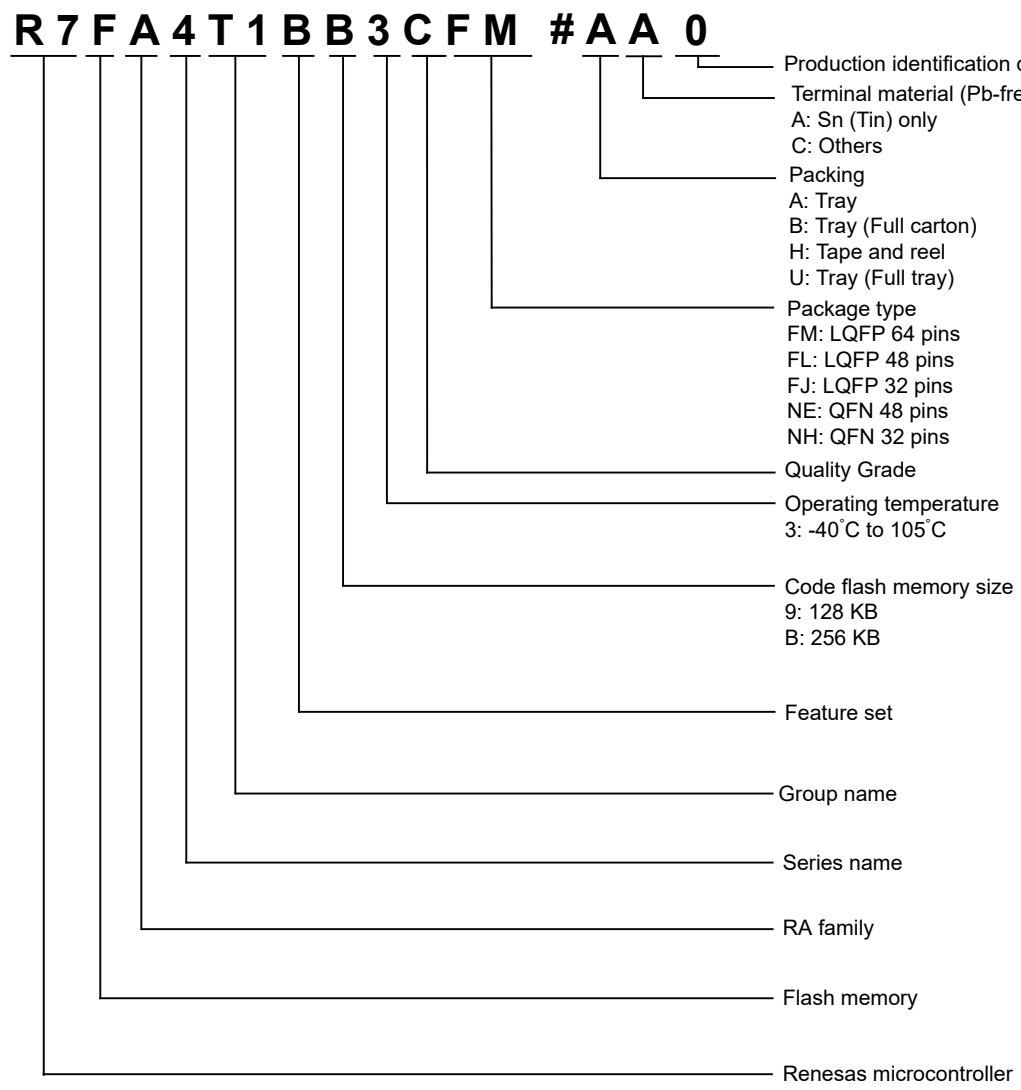


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.



Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA4T1BB3CFM	PLQP0064KB-C	256 KB	4 KB	40 KB	-40 to +105°C
R7FA4T1BB3CFL	PLQP0048KB-B				
R7FA4T1BB3CFJ	PLQP0032GB-A				
R7FA4T1BB3CNE	PWQN0048KC-A				
R7FA4T1BB3CNH	PWQN0032KE-A				
R7FA4T1B93CFM	PLQP0064KB-C	128 KB	4 KB	40 KB	-40 to +105°C
R7FA4T1B93CFL	PLQP0048KB-B				
R7FA4T1B93CFJ	PLQP0032GB-A				
R7FA4T1B93CNE	PWQN0048KC-A				
R7FA4T1B93CNH	PWQN0032KE-A				

1.4 Function Comparison

Table 1.13 Function Comparison

Parts number		R7FA4T1BB3CFM/ R7FA4T1B93CFM	R7FA4T1BB3CFL/ R7FA4T1B93CFL R7FA4T1BB3CNE/ R7FA4T1B93CNE	R7FA4T1BB3CFJ/ R7FA4T1B93CFJ R7FA4T1BB3CNH/ R7FA4T1B93CNH
Pin count		64	48	32
Package		LQFP	LQFP/QFN	LQFP/QFN
Code flash memory		256 KB, 128 KB		
Data flash memory		4 KB		
SRAM		40 KB		
	Parity	32 KB		
	ECC	8 KB		
DMA	DTC	Yes		
	DMAC	8		
System	CPU clock	100 MHz (max.)		
	CPU clock sources	MOSC, SOSC, HOCO, MOCO, LOCO, PLL		
	CAC	Yes		
	WDT/IWDT	Yes		
Communication	SCI	2		
	I3C	1		
	SPI	2		
	CANFD	1		
Timers	GPT16E*1	6		4
	AGT*1	2		
Analog	ADC12	12	8	5
	DAC12	2		1
	ACMPHS	3		
	PGA	3		
	TSN	Yes		
Data processing	CRC	Yes		
	DOC	Yes		
Event control	ELC	Yes		
Accelerator	TFU	Yes		
Security		TrustZone		
I/O ports	I/O pins	45	29	16
	Input pins	5	5	5
	Pull-up resistors	46	30	17
	N-ch open-drain outputs	45	29	16
	5-V tolerance	11	6	4

Note 1. Available pins depend on the pin count, see section 1.7. Pin Lists for details.

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
I3C	I3C_SCL	I/O	Input/output pins for the I3C clock
	I3C_SDA	I/O	Input/output pins for the I3C data
	SCL0	I/O	Input/output pins for the I2C clock
	SDA0	I/O	Input/output pins for the I2C data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CANFD	CRX0	Input	Receive data
	CTX0	Output	Transmit data
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the D/A Converter.
	VREFL	Input	Analog reference ground pin for the D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC0 when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS0 when not using the ADC12.
ADC12	AN0n	Input	Input pins for the analog signals to be processed by the A/D converter (n: pin number).
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
	PGAVSS000	Input	Pseudo-differential input pins
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
ACMPHS	VCOUT	Output	Comparator output pin
	IVREFn	Input	Reference voltage input pins for comparator
	IVCMPn	Input	Analog voltage input pins for comparator
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

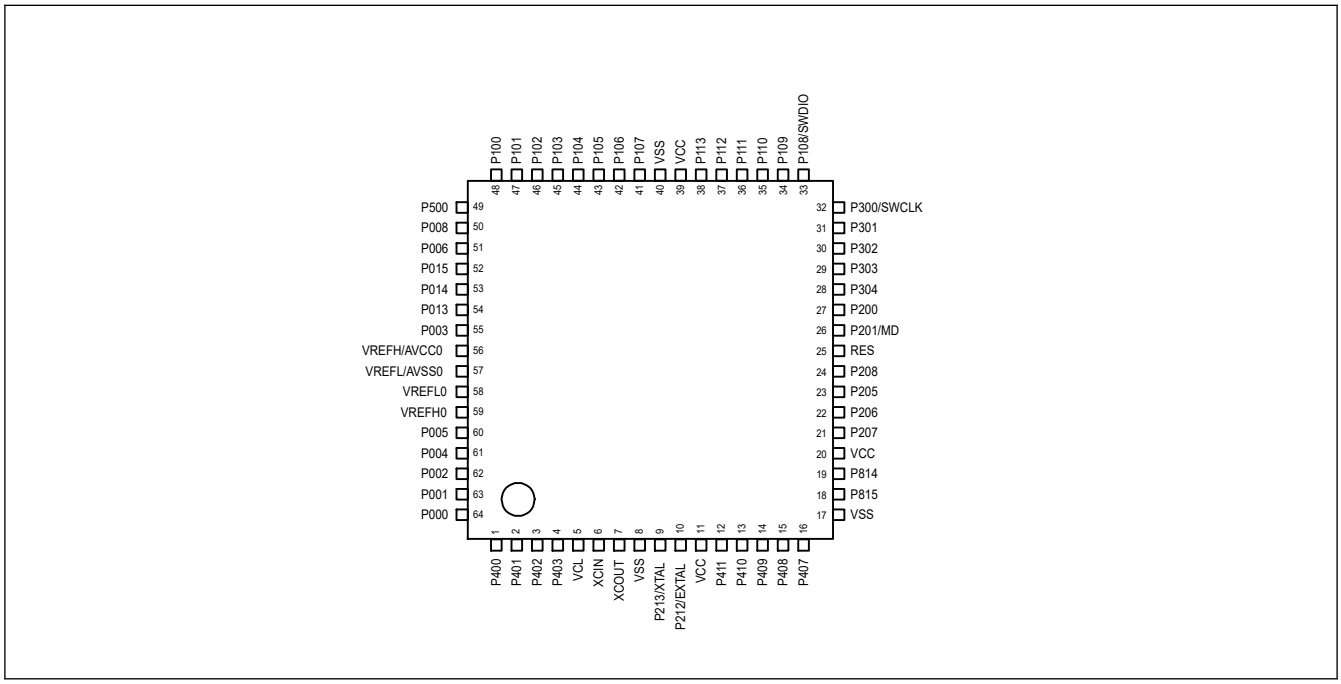


Figure 1.3 Pin assignment for LQFP 64-pin

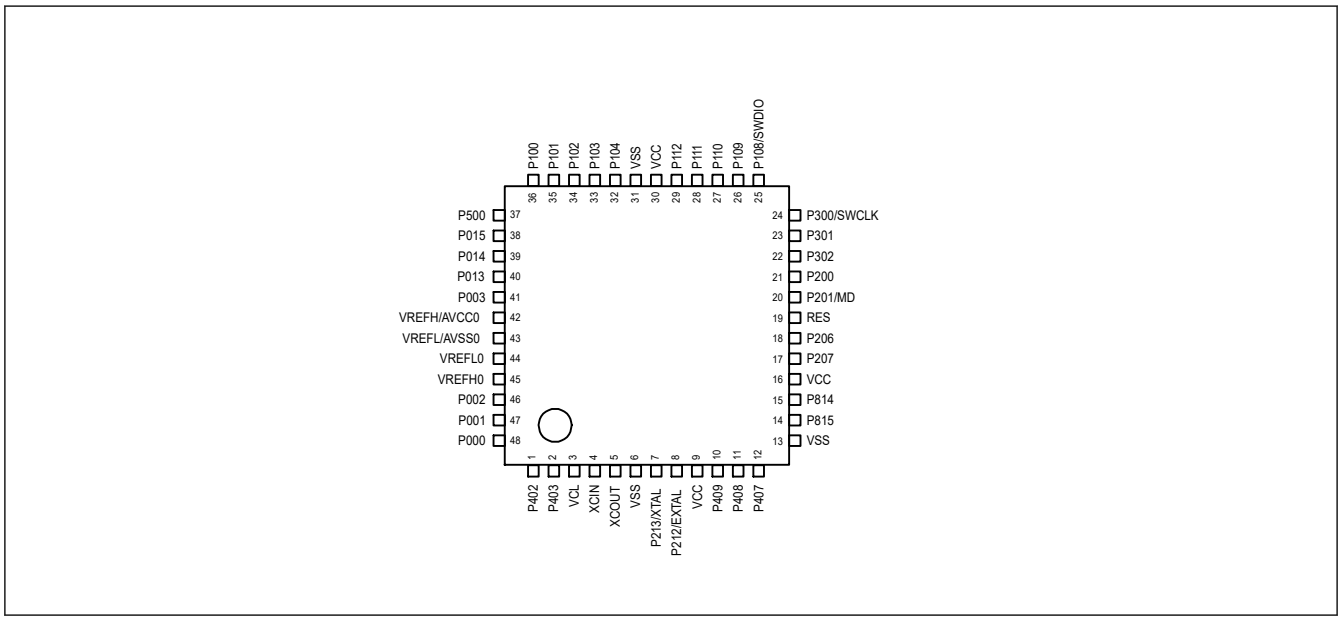
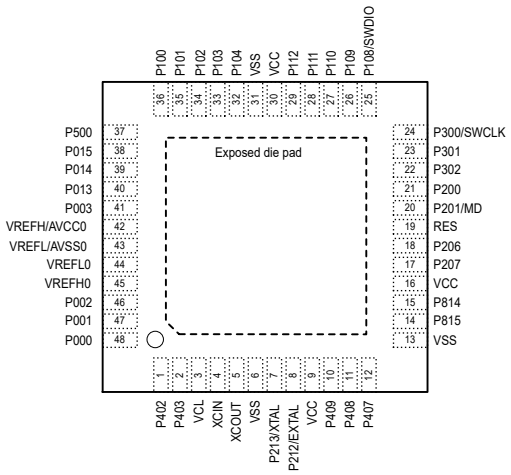
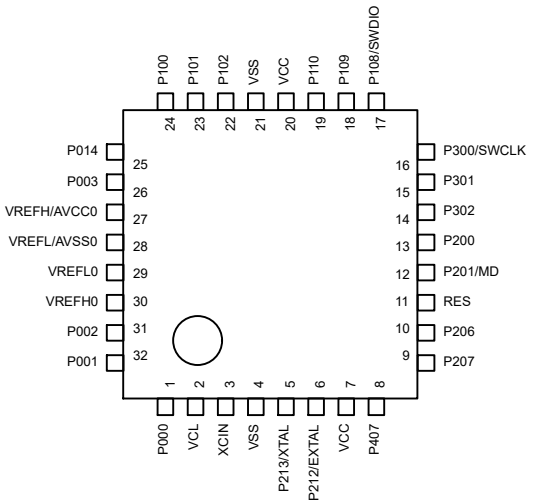


Figure 1.4 Pin assignment for LQFP 48-pin



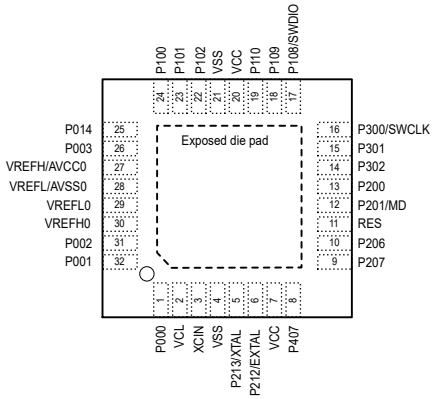
Note: Exposed die pad is recommended to connect to VSS.

Figure 1.5 Pin assignment for QFN 48-pin



Note: XCIN cannot be used in LQFP32. XCIN must be connected to VSS through a resistor (pull down).

Figure 1.6 Pin assignment for LQFP 32-pin



Note: XCIN cannot be used in QFN32. XCIN must be connected to VSS through a resistor (pull down).
Note: Exposed die pad is recommended to connect to VSS.

Figure 1.7 Pin assignment for QFN 32-pin

1.7 Pin Lists

Table 1.15 Pin list (1 of 2)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
1	—	—	—	P400	IRQ0	SCL0_A	AGTIO1	—
2	—	—	—	P401	IRQ5-DS	SDA0_A/CTX0	GTETRGA	—
3	1	—	CACREF	P402	IRQ4-DS	CRX0	AGTIO0/AGTIO1/ GTADSM1	—
4	2	—	—	P403	IRQ14-DS	—	GTIOC3A/AGTIO0/ AGTIO1	—
5	3	2	VCL	—	—	—	—	—
6	4	3	XCIN*1	—	—	—	—	—
7	5	—	XCOUT	—	—	—	—	—
8	6	4	VSS	—	—	—	—	—
9	7	5	XTAL	P213	IRQ2	TXD0/MOSI0/SDA0	GTIOC0A/GTETRGC	—
10	8	6	EXTAL	P212	IRQ3	RXD0/MISO0/SCL0	GTIOC0B/GTETRGD/ AGTEE1	—
11	9	7	VCC	—	—	—	—	—
12	—	—	—	P411	IRQ4	TXD0/MOSI0/SDA0	GTOVUP	—
13	—	—	—	P410	IRQ5	RXD0/MISO0/SCL0	GTOVLO	—
14	10	—	—	P409	IRQ6	—	GTIOC1A/GTOWUP/ AGTOA1	—
15	11	—	—	P408	IRQ7	SCL0_B	GTIOC1B/GTIW/ AGTOB1	—
16	12	8	—	P407	—	SDA0_B	GTIV/AGTIO0/ GTADSM0	ADTRG0
17	13	—	VSS	—	—	—	—	—
18	14	—	—	P815	—	—	GTIOC0A/GTETRGC	—
19	15	—	—	P814	—	—	GTIOC0B/GTETRGB	—
20	16	—	VCC	—	—	—	—	—
21	17	9	CACREF	P207	—	SCK9/MOSIA_A	GTIOC5A/GTIW/ AGTIO1	—
22	18	10	—	P206	IRQ0-DS	CTS9/SDA0_C/ MISOA_A	GTIOC5B/GTIU	—
23	—	—	CLKOUT	P205	IRQ1-DS	CTS_RTS9/SS9/ SCL0_C/SSLA3_A	GTIOC4A/GTIV/AGTO1	—
24	—	—	—	P208	—	—	GTOVLO	ADTRG0
25	19	11	RES	—	—	—	—	—
26	20	12	MD	P201	—	—	—	—
27	21	13	—	P200	NMI	—	—	—
28	—	—	—	P304	IRQ9	—	GTOWLO	—
29	—	—	—	P303	—	CTS9	—	—
30	22	14	—	P302	IRQ5	CTS0/SCK9/ RSPCKA_A	GTIOC4A/GTOUUP	—
31	23	15	—	P301	IRQ6	CTS_RTS9/SS9/ SSLA0_A	GTIOC4B/GTOULO/ AGTIO0	—
32	24	16	SWCLK	P300	—	SSLA1_B	GTIOC0A/GTOUUP	—
33	25	17	SWDIO	P108	—	CTS_RTS9/SS9/ SSLA0_B	GTIOC0B/GTOULO	—
34	26	18	CLKOUT	P109	—	TXD9/MOSI9/SDA9/ MOSIA_B/CTX0	GTIOC1A/GTOVUP/ AGTOA0	—
35	27	19	—	P110	IRQ3	RXD9/MISO9/SCL9/ MISOA_B/CRX0	GTIOC1B/GTOVLO/ AGTOB0	VCOUT
36	28	—	—	P111	IRQ4	SCK9/RSPCKA_B	GTIOC3A	—
37	29	—	—	P112	—	SSLA0_B	GTIOC3B/GTETRGD/ AGTO1	—
38	—	—	—	P113	—	—	GTIOC2A	—
39	30	20	VCC	—	—	—	—	—

Table 1.15 Pin list (2 of 2)

LQFP64	LQFP48 QFN48	LQFP32 QFN32	Power, System, Clock, Debug, CAC	I/O ports	Ex. Interrupt	SCI/I3C/SPI/CANFD	GPT/AGT	ADC12/DAC12/ ACMPHS
40	31	21	VSS	—	—	—	—	—
41	—	—	—	P107	—	SSLA2_B	AGTOA0	—
42	—	—	—	P106	—	SSLB3	AGTOB0	—
43	—	—	—	P105	IRQ0	SSLB2	GTIOC1A/GTETRGA	—
44	32	—	—	P104	IRQ1	SSLB1	GTIOC1B/GTETRGB/ AGTIO1	—
45	33	—	—	P103	—	CTS_RTS0/SS0/SSLB0/ CTX0	GTIOC2A/GTOWUP	—
46	34	22	—	P102	—	SCK0/RSPCKB/CRX0/ QIO0/SSIBCK0_B	GTIOC2B/GTOWLO/ AGTO0	ADTRG0
47	35	23	—	P101	IRQ1	TXD0/MOSI0/SDA0/ I3C_SDA/SDA0_D/ MOSIB	GTIOC5A/GTETRGB/ AGTEE0	—
48	36	24	—	P100	IRQ2	RXD0/MISO0/SCL0/ I3C_SCL/SCL0_D/ MISOB	GTIOC5B/GTETRGA/ AGTIO0	—
49	37	—	CACREF	P500	—	—	GTIU/AGTOA0	AN016/IVREF0
50	—	—	—	P008	IRQ12-DS	—	—	AN008
51	—	—	—	P006	IRQ11-DS	—	—	AN006
52	38	—	—	P015	IRQ13	—	—	AN013/DA1/IVCMP0
53	39	25	—	P014	—	—	—	AN012/DA0/IVREF1
54	40	—	—	P013	—	—	—	AN011
55	41	26	—	P003	—	—	—	AN007/PGAVSS000
56	42	27	VREFH/AVCC0	—	—	—	—	—
57	43	28	VREFL/AVSS0	—	—	—	—	—
58	44	29	VREFL0	—	—	—	—	—
59	45	30	VREFH0	—	—	—	—	—
60	—	—	—	P005	IRQ10-DS	—	—	AN005
61	—	—	—	P004	IRQ9-DS	—	—	AN004
62	46	31	—	P002	IRQ8-DS	—	—	AN002/IVCMP2
63	47	32	—	P001	IRQ7-DS	—	—	AN001/IVCMP2
64	48	1	—	P000	IRQ6-DS	—	—	AN000/IVCMP2

Note: Several pin names have the added suffix of _A, _B, _C, and _D. The suffix can be ignored when assigning functionality.
Note 1. XCIN cannot be used in QFN32 and LQFP32. XCIN must be connected to VSS through a resistor (pull down).

2. Electrical Characteristics

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = AVCC0 =2.7 to 3.6
- 2.7 ≤ VREFH0/VREFH ≤ AVCC0
- VSS = AVSS0 = VREFL0/VREFL = 0 V
- $T_a = T_{opr}$

Figure 2.1 shows the timing conditions.

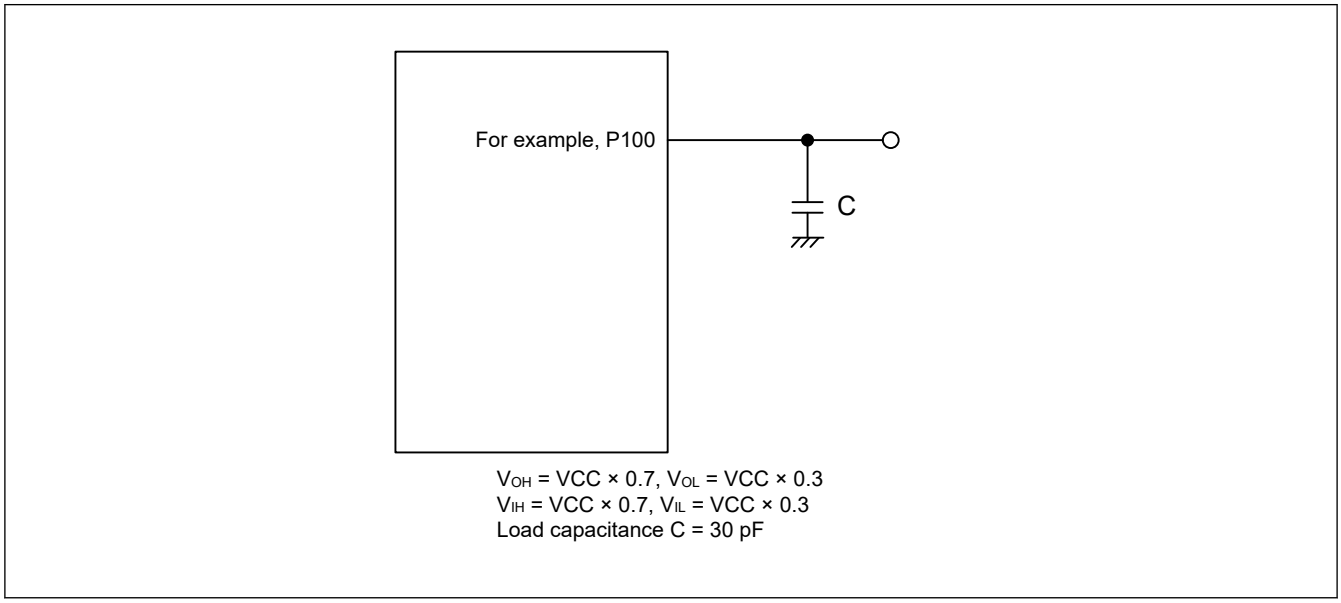


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports*1)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (5 V-tolerant ports*1)	V_{in}	–0.3 to + VCC + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	–0.3 to VCC + 0.3	V
Analog power supply voltage	AVCC0*2	–0.3 to +4.0	V
Analog input voltage (except for P000 to P003)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P003) when PGA pseudo-differential input is disabled	VAN	–0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002) when PGA pseudo-differential input is enabled	VAN	–1.3 to AVCC0 + 0.3	V
Analog input voltage (P003) when PGA pseudo-differential input is enabled	VAN	–0.8 to AVCC0 + 0.3	V
Operating temperature*3 *4	T_{opr}	–40 to +105	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note 1. Ports P100, P101, P205, P206, P400, P401 and P407 to P411 are 5 V tolerant.
Note 2. Connect AVCC0 to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltages	VCC	2.7	—	3.6	V
	VSS	—	0	—	V
Analog power supply voltages	AVCC0*1	—	VCC	—	V
	AVSS0	—	0	—	V

Note 1. Connect AVCC0 to VCC. When the A/D converter, the D/A converter and the comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	—	125	°C	High-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL (external clock input), SPI (except RSPCK)	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
		I3C (SMBus)	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	

Table 2.4 I/O V_{IH}, V_{IL} (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Schmitt trigger input voltage	Peripheral function pin	I3C (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
		5 V-tolerant ports*1 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
		Other input pins*2	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Ports	5 V-tolerant ports*3 *5	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
		Other input pins*4	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with P100, P101, P205, P206, P400, P401, P407 to P411 (total 12 pins).
Note 2. All input pins except for the peripheral function pins already described in the table.
Note 3. P100, P101, P205, P206, P400, P401, P407 to P411 (total 11 pins).
Note 4. All input pins except for the ports already described in the table.
Note 5. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break-down voltage.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–20	mA
			I_{OL}	—	—	20	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–2.0	mA
			I_{OL}	—	—	2.0	mA
		Middle drive*2	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		High drive*3	I_{OH}	—	—	–16	mA
			I_{OL}	—	—	16	mA
Permissible output current (max value per pin)	I3C pins	IIC Standard mode*4	I_{OL}	—	—	3.0	mA
		IIC Fast mode*4	I_{OL}	—	—	6.0	mA
		IIC Fast mode plus*4	I_{OL}	—	—	20	mA
		IIC High speed mode*4	I_{OL}	—	—	3.0	mA
	Ports P004 to P006, P008, P013 to P015, P201	—	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
	Ports P205, P206, P407 to P411 (total 7 pins)	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–40	mA
			I_{OL}	—	—	40	mA
	Other output pins*5	Low drive*1	I_{OH}	—	—	–4.0	mA
			I_{OL}	—	—	4.0	mA
		Middle drive*2	I_{OH}	—	—	–8.0	mA
			I_{OL}	—	—	8.0	mA
		High drive*3	I_{OH}	—	—	–32	mA
			I_{OL}	—	—	32	mA

Table 2.5 I/O I_{OH}, I_{OL} (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	$\Sigma I_{OH\ (max)}$	—	—	–80	mA
		$\Sigma I_{OL\ (max)}$	—	—	80	mA

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 4. SCL0_D, SDA0_D (total 2 pins). This is the value when IIC function is selected.
Note 5. Except for P000 to P003, P200, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	I3C*1		V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
	I3C*2		V_{OH}	VCC - 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0)
			V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1)
			V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.HSME = 1)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0)
	Ports P205, P206, P407 to P411(total 7 pins)*3		V_{OH}	VCC - 1.0	—	—		I_{OH} = –20 mA VCC = 3.3 V
			V_{OL}	—	—	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	—	—		I_{OH} = –1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\lvert I_{in} \rvert$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	Port P000 to P002, P200			—	—	1.0		V_{in} = 0 V V_{in} = VCC
	Port P003	Before initialization*5		—	—	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*6		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports (except for port P100, P101)		$\lvert I_{TSI} \rvert$	—	—	5.0	µA	V_{in} = 0 V V_{in} = 5.5 V
	5 V-tolerant ports (P100, P101)			—	—	10.0		V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P000 to P003, P200)			—	—	1.0		V_{in} = 0 V V_{in} = VCC

Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input pull-up MOS current	Ports P0 to P5, P8 (except for ports P000 to P003)	I_p	–300	—	–10	µA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Pull-up current serving as the SCL current source	I3C*4	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V Vin = 0.3 × VCC to 0.7 × VCC
Input capacitance	Ports P003, P014, P015, P814, P815	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Other input pins		—	—	8		

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, and SDA0_C (total 6 pins).
Note 2. I3C_SCL/SCL0_D, I3C_SDA/SDA0_D (total 2 pins).
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
When medium or low driving ability is selected, refer to the values of other output pins.
Note 4. I3C_SCL/SCL0_D (1 pin). This is the value when IIC high speed mode is selected.
Note 5. P0nPFS.ASEL (n = 3) = 1
Note 6. P0nPFS.ASEL (n = 3) = 0

2.2.5 Operating and Standby Current

Table 2.7 Operating and standby current

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current[*1]	High-speed mode	Maximum[*2*13]		I_{CC}[*3]	—	—	61	mA	ICLK = 100 MHz PCLKA = 100 MHz PCLKB = 50 MHz PCLKC = 50 MHz PCLKD = 100 MHz FCLK = 50 MHz
		CoreMark®[*5 *6*12]			—	8.2	—		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash[*4*12]		—	13.5	—		
			All peripheral clocks disabled, while (1) code executing from flash[*5 *6*12]		—	9.1	—		
		Sleep mode[*5]			—	5.3[*6 *12]	42[*7 *13]		
		Increase during BGO operation	Data flash P/E		—	6	—		
			Code flash P/E		—	8	—		
	Low-speed mode[*5 *10]				—	1.8	—		ICLK = 1 MHz
	Subosc-speed mode[*5 *11]				—	1.6	—		ICLK = 32.768 kHz
	Software Standby mode		SNZCR.RXDREQEN = 1		—	—	35		—
			SNZCR.RXDREQEN = 0		—	1.4	—		—
	Deep Software Standby mode	DPSBYCR.DEEPCUT[1:0] = 00b[*14]			—	16	96	μA	—
		DPSBYCR.DEEPCUT[1:0] = 01b[*14]			—	11	25.6		—
		DPSBYCR.DEEPCUT[1:0] = 11b[*14]			—	4.2	20.4		—
		Increase when the AGT is operating	When the low-speed on-chip oscillator (LOCO) is in use		—	4.2	—		—
			When a crystal oscillator for low clock loads is in use		—	0.9	—		—
			When a crystal oscillator for standard clock loads is in use		—	1.3	—		—
	Inrush current on returning from deep software standby mode		Inrush current[*8]	I_{RUSH}	—	160	—	mA	—
			Energy of inrush current[*8]	E_{RUSH}	—	1.0	—	μC	—
Analog power supply current	During 12-bit A/D conversion			AI_{CC}, AI_{REFH}	—	0.8	1.2	mA	—
	During 12-bit A/D conversion with S/H amp				—	2.3	3.3	mA	—
	PGA (1ch)				—	1	3	mA	—
	ACMPHS (1 unit)				—	100	150	μA	—
	Temperature sensor				—	0.1	0.2	mA	—
	During D/A conversion (per unit)		Without AMP output		—	0.2	0.6	mA	—
			With AMP output		—	0.7	1.5	mA	—
	Waiting for A/D, D/A conversion (all units)				—	0.5	1.0	mA	—
	ADC12, DAC12 in standby modes (all units)[*9]				—	0.4	6	μA	—
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	—	70	120	μA	—
	Waiting for 12-bit A/D conversion (unit 0)				—	0.07	0.5	μA	—
	ADC12 in standby modes (unit 0)				—	0.07	0.5	μA	—

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows.

I_{CC} Max. = 0.24 × f + 37 (max. operation in high-speed mode)
I_{CC} Typ. = 0.07 × f + 2.75 (normal operation in high-speed mode, all peripheral clocks disabled)
I_{CC} Typ. = 0.1 × f + 1.71 (low-speed mode)
I_{CC} Max. = 0.05 × f + 37 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (1.56 MHz).
Note 7. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.125 MHz).
Note 8. Reference value
Note 9. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (12-Bit A/D Converter 0 Module Stop bit) is in the module-stop state.
Note 10. FCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (15.6 kHz).
Note 11. PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (512 Hz). FCLK is the same frequency as that of ICLK.
Note 12. PLL output frequency = 100MHz.
Note 13. PLL output frequency = 200MHz.
Note 14. For more information on the DBSBYCR register, see section xx.x.xx, Deep Software Standby Control Register (DPSBYCR).

Table 2.8 Coremark and normal mode current

Parameter			Symbol	Typ	Unit	Test conditions
Supply Current*1	Coremark*2 *3		I_{CC}	82	µA/MHz	ICLK = 100 MHz PCLKA = PCLKB = PCLKC = PCLKD = FCLK = 1.563 MHz
	Normal mode	All peripheral clocks disabled, cache on, while (1) code executing from flash*2 *3		91		
		All peripheral clocks disabled, cache off, while (1) code executing from flash*2 *3		93		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. PLL output frequency = 100MHz.

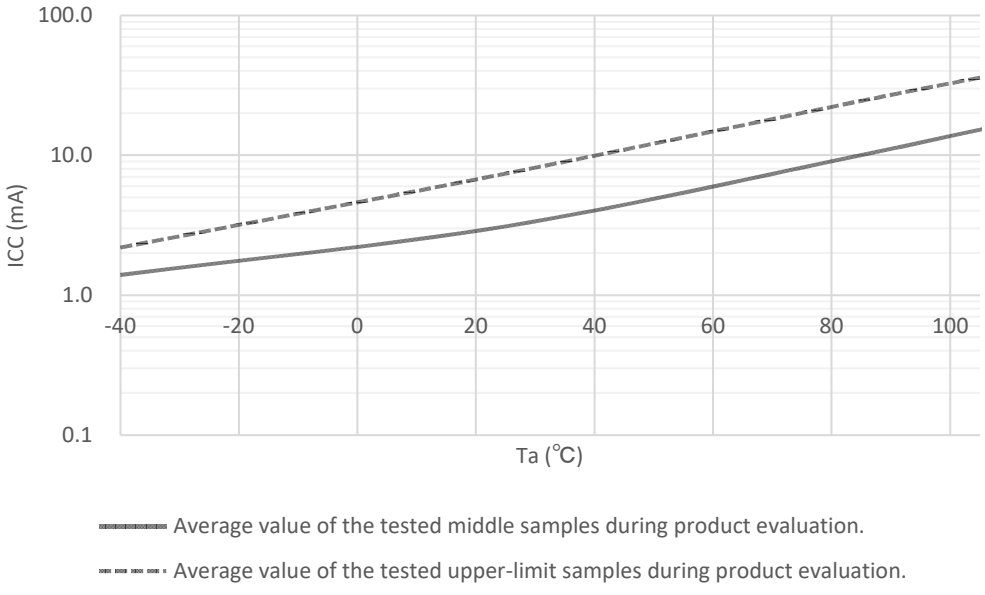


Figure 2.2 Temperature dependency in Software Standby mode (reference data)

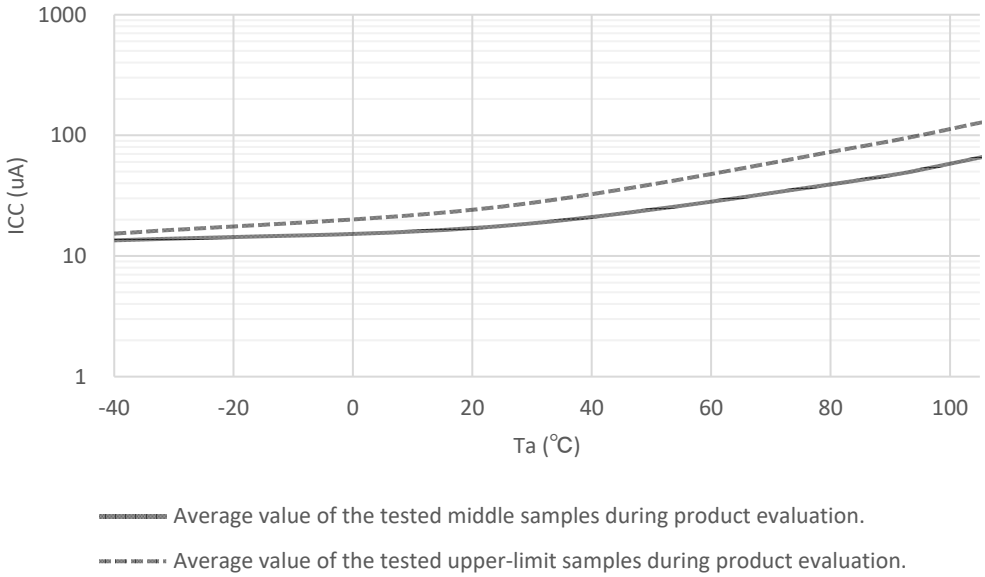


Figure 2.3 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 00b (reference data)

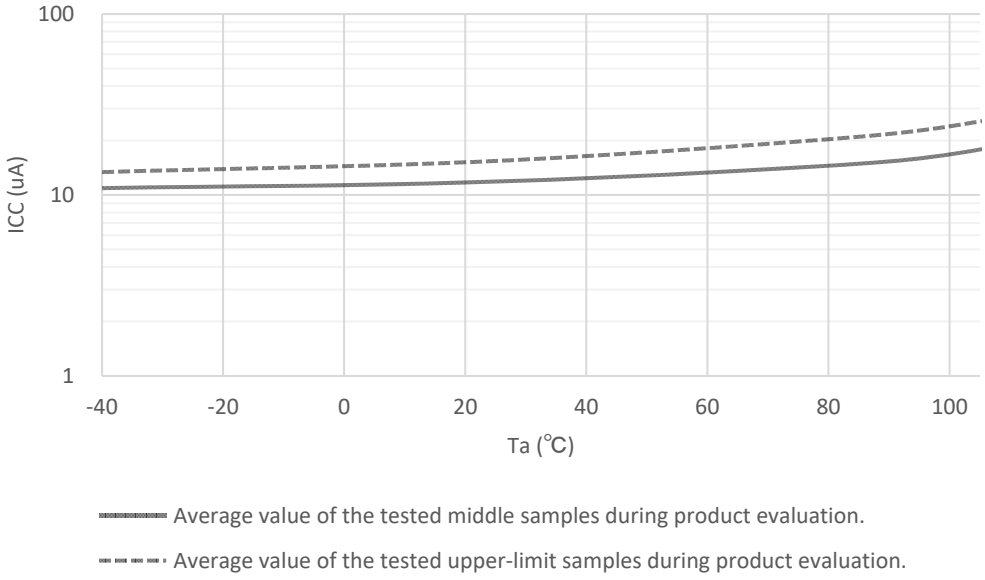


Figure 2.4 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 01b (reference data)

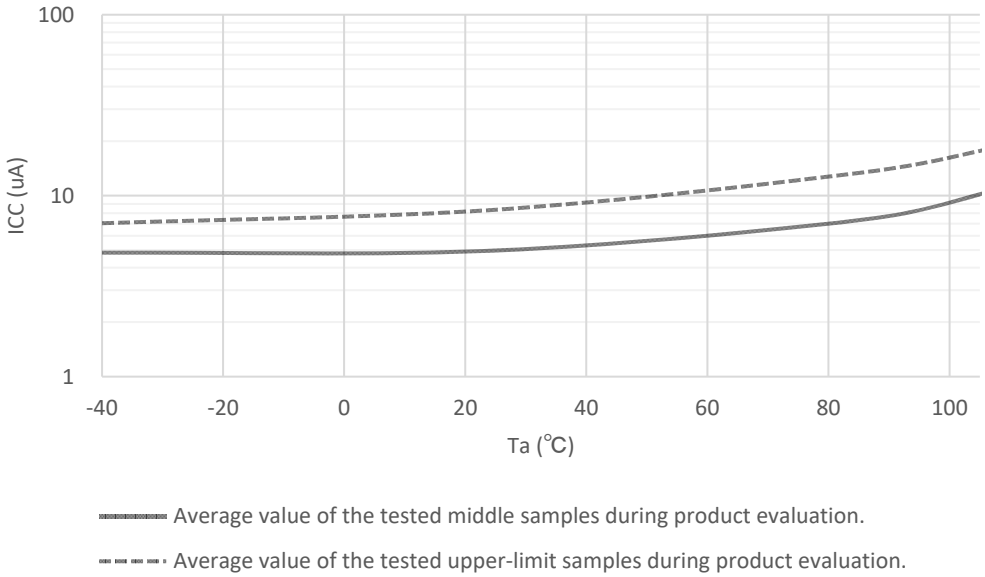


Figure 2.5 Temperature dependency in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] = 11b (reference data)

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.9 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	—	20	ms/V	—
	Voltage monitor 0 reset enabled at startup		0.0084	—	—		—
	SCI boot mode*1		0.0084	—	20		—
VCC falling gradient		SfVCC	0.0084	—	—	ms/V	—

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 2.10 Rising and falling gradient and ripple frequency characteristics

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r\ (VCC)}$	—	—	10	kHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.6 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

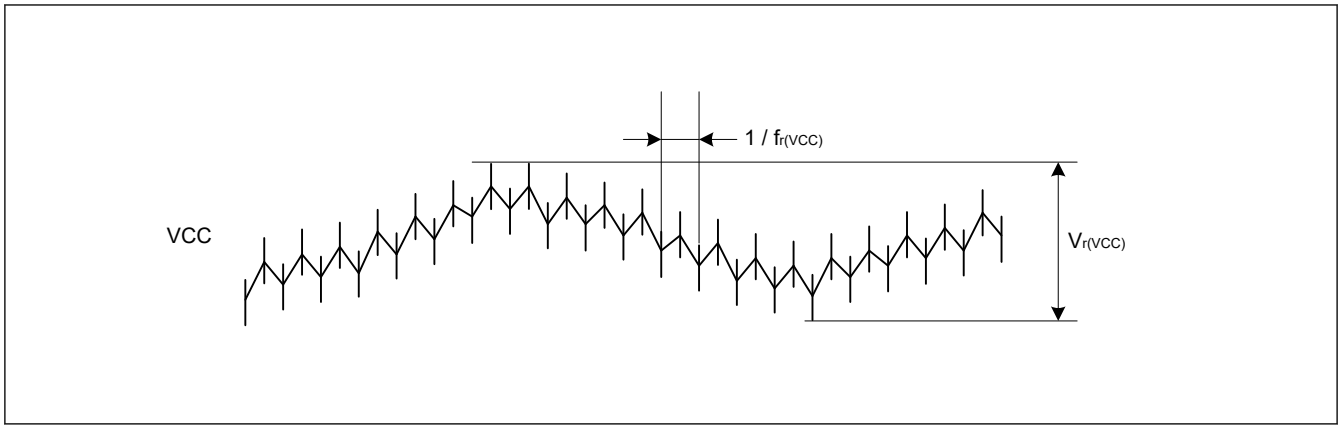


Figure 2.6 Ripple waveform

2.2.7 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of "section 2.2.1. Tj/Ta Definition".

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ ($|I_{OH}|$ × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, refer to Table 2.11.

Table 2.11 Thermal Resistance

Parameter	Package	Symbol	Value*1	Unit	Test conditions
Thermal Resistance	32-pin QFN (PWQN0032KE-A)	θja	36.8	°C/W	JESD 51-2 and 51-7 compliant
	32-pin LQFP (PLQP0032GB-A)		61.5		
	48-pin QFN (PWQN0048KC-A)		29.7		
	48-pin LQFP (PLQP0048KB-B)		62.1		
	64-pin LQFP (PLQP0064KB-C)		41.3		
	32-pin QFN (PWQN0032KE-A)	Ψjt	0.36	°C/W	JESD 51-2 and 51-7 compliant
	32-pin LQFP (PLQP0032GB-A)		2.72		
	48-pin QFN (PWQN0048KC-A)		0.27		
	48-pin LQFP (PLQP0048KB-B)		2.72		
	64-pin LQFP (PLQP0064KB-C)		1.39		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.2.7.1 Calculation Guide of I_{CC}max

Table 2.12 shows the power consumption of each unit.

Table 2.12 Power consumption of each unit

Dynamic current/ Leakage current	MCU domain	Category	Item	Frequency [MHz]	Current [uA/MHz]	Current*1 [mA]
Leakage current	Analog	LDO and Leak*2	Ta = 75 °C*3	—	—	25.10
			Ta = 85 °C*3	—	—	30.64
			Ta = 95 °C*3	—	—	35.90
			Ta = 105 °C*3	—	—	41.60
Dynamic current	CPU	Operation with Flash and SRAM	Coremark	100	57.151	5.72
	Peripheral unit	Timer	GPT16 (6ch)*4	100	8.480	0.85
			POEG (4 Groups)*4	50	1.171	0.06
			AGT (2ch)*4	50	3.967	0.20
			WDT	50	0.635	0.03
			IWDT	50	0.261	0.01
		Communication interfaces	SCI (2 ch)*4	100	5.607	0.56
			I3C	100	8.483	0.85
			CANFD	50	2.680	0.27
			SPI (2ch)*4	100	5.739	0.57
		Analog	ADC12	100	2.229	0.22
			DAC12 (2ch)*4	100	0.602	0.06
			ACMPHS (3ch)*4	50	0.135	0.01
			TSN	50	0.277	0.01
		Event link	ELC	50	0.562	0.06
		Security	TRNG	100	0.013	1.27
		Data processing accelerator	TFU	100	0.330	0.03
		Data processing	CRC	100	0.363	0.04
			DOC	100	0.133	0.01
		System	CAC	50	0.777	0.04
		DMA	DMAC	100	5.771	0.58
			DTC	100	4.843	0.48

Note 1. The values are guaranteed by design.
Note 2. LDO and Leak are current of the internal voltage regulator and leakage current of the MCU. It is selected according to the temperature of Ta.
Note 3. Δ (Tj - Ta) = 20 °C is to measure the current.
Note 4. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.13 shows the outline of operation for each unit.

Table 2.13 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
GPT	Operating mode is set to Saw-wave PWM mode. GPT is operating with PCLKD.
POEG	Only clear module stop bit.

Table 2.13 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
AGT	AGT is operating with PCLKB.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
SCI	SCI is transmitting data in Clock synchronous mode.
I3C	Communication format is set to I3C-bus format. I3C is transmitting data in Master mode.
CANFD	CANFD is transmitting and receiving data in Self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to Master mode. SPI is transmitting 8-bit width data.
ADC12	Resolution is set to 12-bit accuracy. Data register is set to A/D-converted value addition mode. ADC12 is converting the analog input in Continuous scan mode.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
ACMPHS	Compare between IVCMP2 and IVREF0 and enable compare output.
TSN	TSN is operating.
ELC	Only clear module stop bit.
TRNG	TRNG is executing built-in self test.
TFU	Performs sincos operations.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data addition mode.
CAC	Measurement target clock is set to PCLKB. Measurement reference clock is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to Block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to Block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.2.7.2 Example of T_j Calculation

Assumption :

- Package 64-pin LQFP : θja = 41.3 °C/W
- Ta = 100 °C
- I_{CC}max = 40 mA
- VCC = 3.5 V (VCC = AVCC0)
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 8 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 6 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 8 Outputs
- C_{in} = 8 pF, 8 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 8 pins, Output frequency = 10 MHz

Leakage current of IO $= \Sigma (V_{OL} \times I_{OL}) / \text{Voltage} + \Sigma ((VCC - V_{OH}) \times I_{OH}) / \text{Voltage}$

$= (20\ mA \times 1\ V) \times 6 / 3.5\ V + (1\ mA \times 0.5\ V) \times 8 / 3.5\ V + ((VCC - (VCC - 0.5\ V)) \times 1\ mA) \times 8 / 3.5\ V$

= 34.29 mA + 1.14 mA + 1.14 mA

= 36.6 mA

Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage

= ((8 pF × 8) × 10 MHz + (30 pF × 8) × 10 MHz) × 3.5 V

= 10.6 mA

Total power consumption = Voltage × (Leakage current + Dynamic current)

= (40 mA × 3.5 V) + (36.6 mA + 10.6 mA) × 3.5 V

= 305 mW (0.305 W)

Tj = Ta + θja × Total power consumption

= 100 °C + 41.3 °C/W × 0.305 W

= 112.6 °C

2.3 AC Characteristics

2.3.1 Frequency

Table 2.14 Operation frequency value in high-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	100	MHz
	Peripheral module clock (PCLKA)		—	—	100	
	Peripheral module clock (PCLKB)		—	—	50	
	Peripheral module clock (PCLKC)		—*2	—	50	
	Peripheral module clock (PCLKD)		—	—	100	
	Flash interface clock (FCLK)		—*1	—	50	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 2.15 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	—	—	1	MHz
	Peripheral module clock (PCLKA)		—	—	1	
	Peripheral module clock (PCLKB)		—	—	1	
	Peripheral module clock (PCLKC) *2		—*2	—	1	
	Peripheral module clock (PCLKD)		—	—	1	
	Flash interface clock (FCLK)*1		—	—	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 2.16 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	f	29.4	—	36.1	kHz
	Peripheral module clock (PCLKA)		—	—	36.1	
	Peripheral module clock (PCLKB)		—	—	36.1	
	Peripheral module clock (PCLKC) *2		—	—	36.1	
	Peripheral module clock (PCLKD)		—	—	36.1	
	Flash interface clock (FCLK)*1		29.4	—	36.1	

Note 1. Programming or erasing the flash memory is disabled in Subosc-speed mode.
Note 2. The ADC12 cannot be used.

2.3.2 Clock Timing

Table 2.17 Clock timing except for sub-clock oscillator (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	41.66	—	—	ns	Figure 2.7
EXTAL external clock input high pulse width		t_{EXH}	15.83	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	5.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	24	MHz	—
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.8
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	60.4	µs	Figure 2.9
ILOCO clock oscillation frequency		f_{ILOCO}	13.5	15	16.5	kHz	—
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	15.0	µs	—
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	–20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		–40 ≤ Ta ≤ –20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.960	16	16.040		–40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18	18.045		
		f_{HOCO20}	19.950	20	20.050		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	64.7	µs	—
HOCO period jitter		—	—	—	±85	ps	—
FLL stabilization wait time		t_{FLLWT}	—	—	1.8	ms	—
PLL clock frequency		f_{PLL}	100	—	240	MHz	—
PLL clock oscillation stabilization wait time		t_{PLLWT}	—	—	174.9	µs	Figure 2.10
PLL period jitter	f_{PLL} ≥ 120MHz	—	—	±100	—	ps	—
	f_{PLL} < 120MHz	—	—	±120	—	ps	—

Table 2.17 Clock timing except for sub-clock oscillator (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
PLL long term jitter	—	—	±300	—	ps	Term: 1μs, 10μs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.18 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—*1	s	Figure 2.11

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

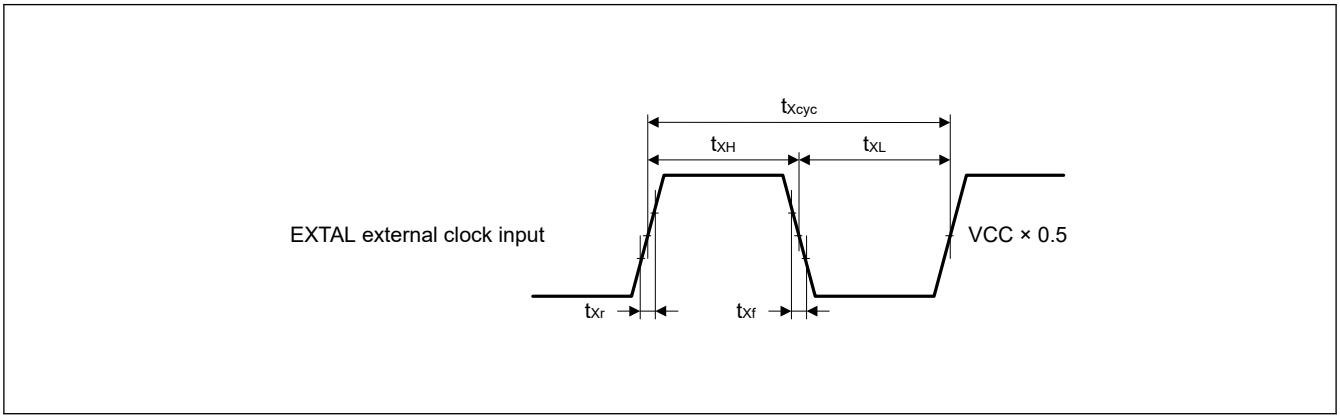


Figure 2.7 EXTAL external clock input timing

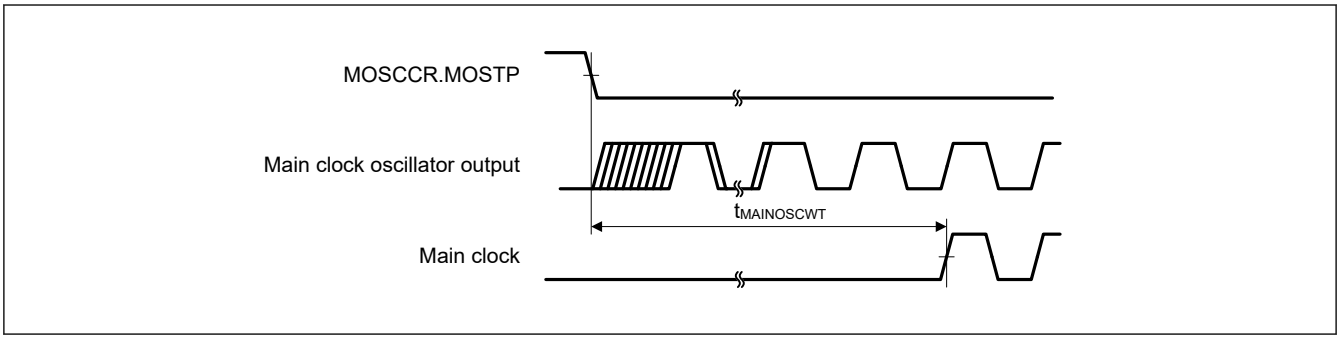


Figure 2.8 Main clock oscillation start timing

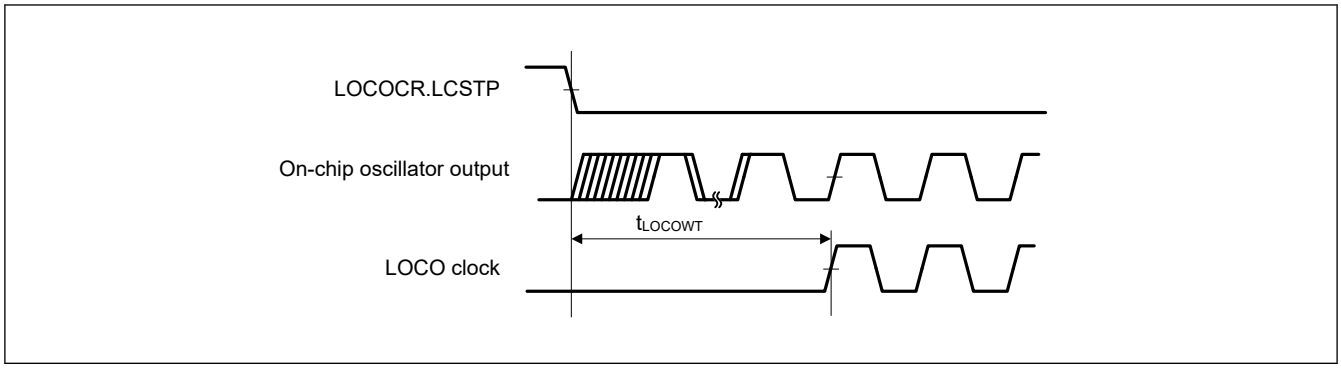


Figure 2.9 LOCO clock oscillation start timing

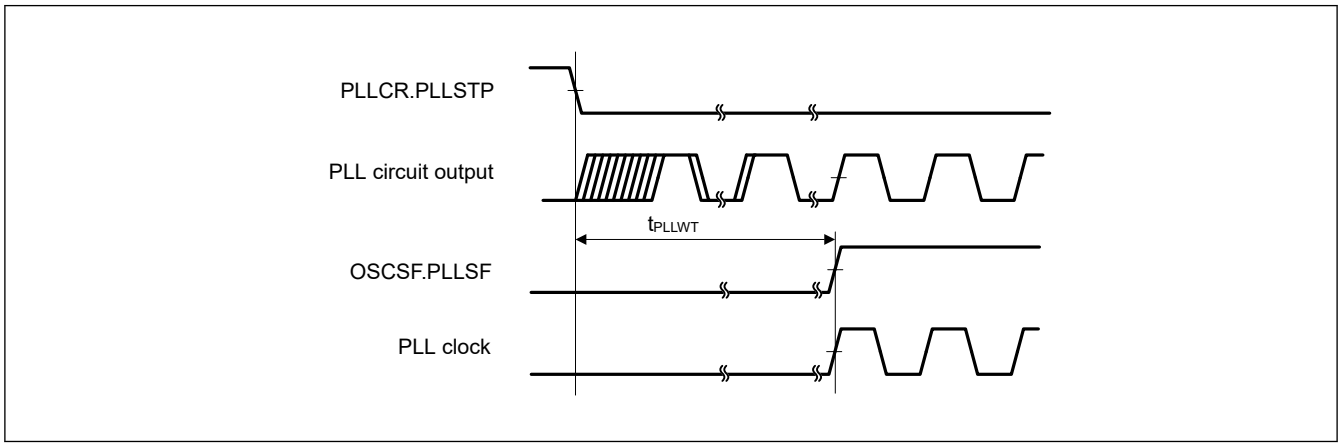


Figure 2.10 PLL clock oscillation start timing

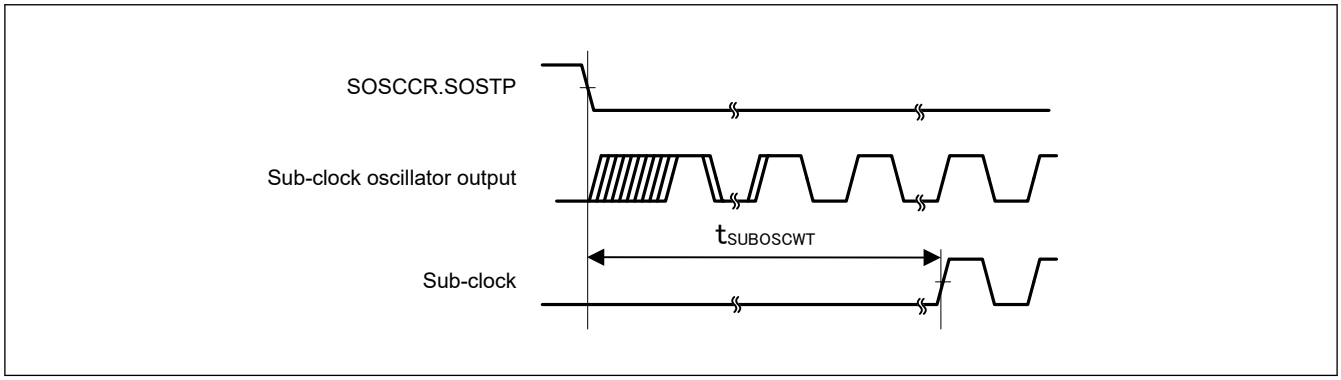


Figure 2.11 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.19 Reset timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	0.7	—	—	ms	Figure 2.12
	Deep Software Standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.13
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	—	—	ms	
	All other	t_{RESW}	200	—	—	µs	
Wait time after RES cancellation		t_{RESWT}	—	37.3	41.2	µs	Figure 2.12

Table 2.19 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, TrustZone error reset, Cache parity error reset)	t_{RESW2}	—	324	397.7	µs	—

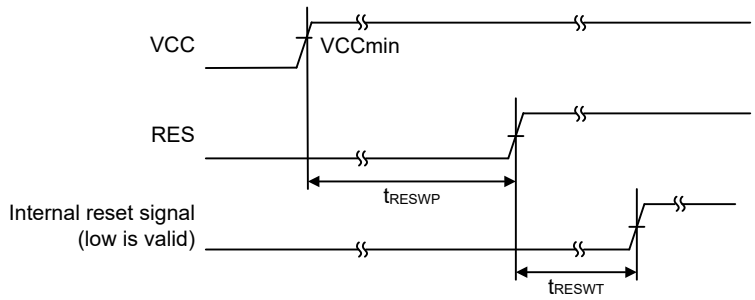


Figure 2.12 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

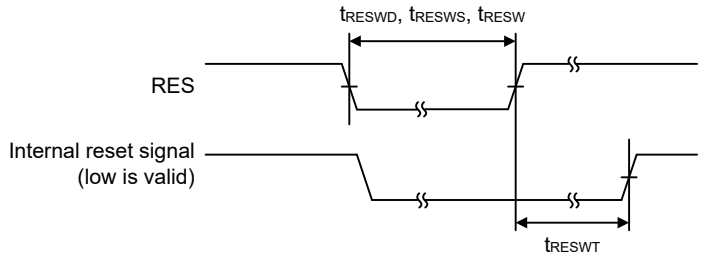


Figure 2.13 Reset input timing

2.3.4 Wakeup Timing

Table 2.20 Timing of recovery from low power modes (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}*13	—	2.1	2.4	ms	Figure 2.14 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}*13	—	2.2	2.6	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}*13	—	45	125	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}*13	—	170	255	µs	
	System clock source is sub-clock oscillator*6 *11		t_{SBYSC}*13	—	0.7	0.8	ms	
	System clock source is LOCO*7 *11		t_{SBYLO}*13	—	0.7	0.9	ms	
	System clock source is HOCO clock oscillator*8		t_{SBYHO}*13	—	55	130	µs	
	System clock source is PLL with HOCO*9		t_{SBYPH}*13	—	175	265	µs	
	System clock source is MOCO clock oscillator*10		t_{SBYMO}*13	—	35	65	µs	

Table 2.20 Timing of recovery from low power modes (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode	DPSBYCR.DEEPCUT[1] = 0 and DPSWCR.WTSTS[5:0] = 0x0E	t_{DSBY}	—	0.38	0.54	ms	Figure 2.15
	DPSBYCR.DEEPCUT[1] = 1 and DPSWCR.WTSTS[5:0] = 0x19	t_{DSBY}	—	0.55	0.73	ms	
Wait time after cancellation of Deep Software Standby mode		t_{DSBYWT}	56	—	57	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)	t_{SNZ}	—	35*12	70*12	µs	Figure 2.16
	High-speed mode when system clock source is MOCO (8 MHz)	t_{SNZ}	—	11*12	14*12	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest tSBYOSCWT in the active oscillators - tSBYOSCWT for the system clock + 2 LOCO cycles (when LOCO is operating) + Subosc is oscillating and MSTPC0 = 0 (CAC module stop).
Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 3. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 4.
Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 5. When the frequency of PLL is 200 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 4.
Note 6. The Sub-clock oscillator frequency is 32.768 KHz and the greatest value of the internal clock division setting is 1.
Note 7. The LOCO frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 8. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 9. The PLL frequency is 200 MHz and the greatest value of the internal clock division setting is 4.
Note 10. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 11. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.
Note 12. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time: 16 µs (typical), 48 µs (maximum).
Note 13. The recovery time can be calculated with the equation of tSBYOSCWT + tSBYSEQ. And they can be determined with the following value and equation. For n, the greatest value is selected from among the internal clock division settings.

Wakeup time	TYP		MAX		Unit
	tSBYOSCWT	tSBYSEQ	tSBYOSCWT	tSBYSEQ	
tSBYMC	(MSTS[7:0]*32 + 3) / 0.262	35 + 18 / fICLK + 4n / fMAIN	(MSTS[7:0]*32 + 14 / 0.236	62 + 18 / fICLK + 4n / fMAIN	µs
tSBYPC	(MSTS[7:0]*32 + 34) / 0.262	35 + 18 / fICLK + 4n / fPLL	(MSTS[7:0]*32 + 45) / 0.236	62 + 18 / fICLK + 4n / fPLL	µs
tSBYEX	10	35 + 18 / fICLK + 4n / fEXMAIN	62	62 + 18 / fICLK + 4n / fEXMAIN	µs
tSBYPE	135	35 + 18 / fICLK + 4n / fPLL	192	62 + 18 / fICLK + 4n / fPLL	µs
tSBYSC	0	35 + 18 / fICLK + 4n / fSUB	0	62 + 18 / fICLK + 4n / fSUB	µs
tSBYLO	0	35 + 18 / fICLK + 4n / fLOCO	0	62 + 18 / fICLK + 4n / fLOCO	µs
tSBYHO	20	35 + 18 / fICLK + 4n / fHOCO	67	62 + 18 / fICLK + 4n / fHOCO	µs
tSBYPH	140	35 + 18 / fICLK + 4n / fPLL	202	62 + 18 / fICLK + 4n / fPLL	µs
tSBYMO	0	35 + 18 / fICLK + 4n / fMOCO	0	62 + 18 / fICLK + 4n / fMOCO	µs

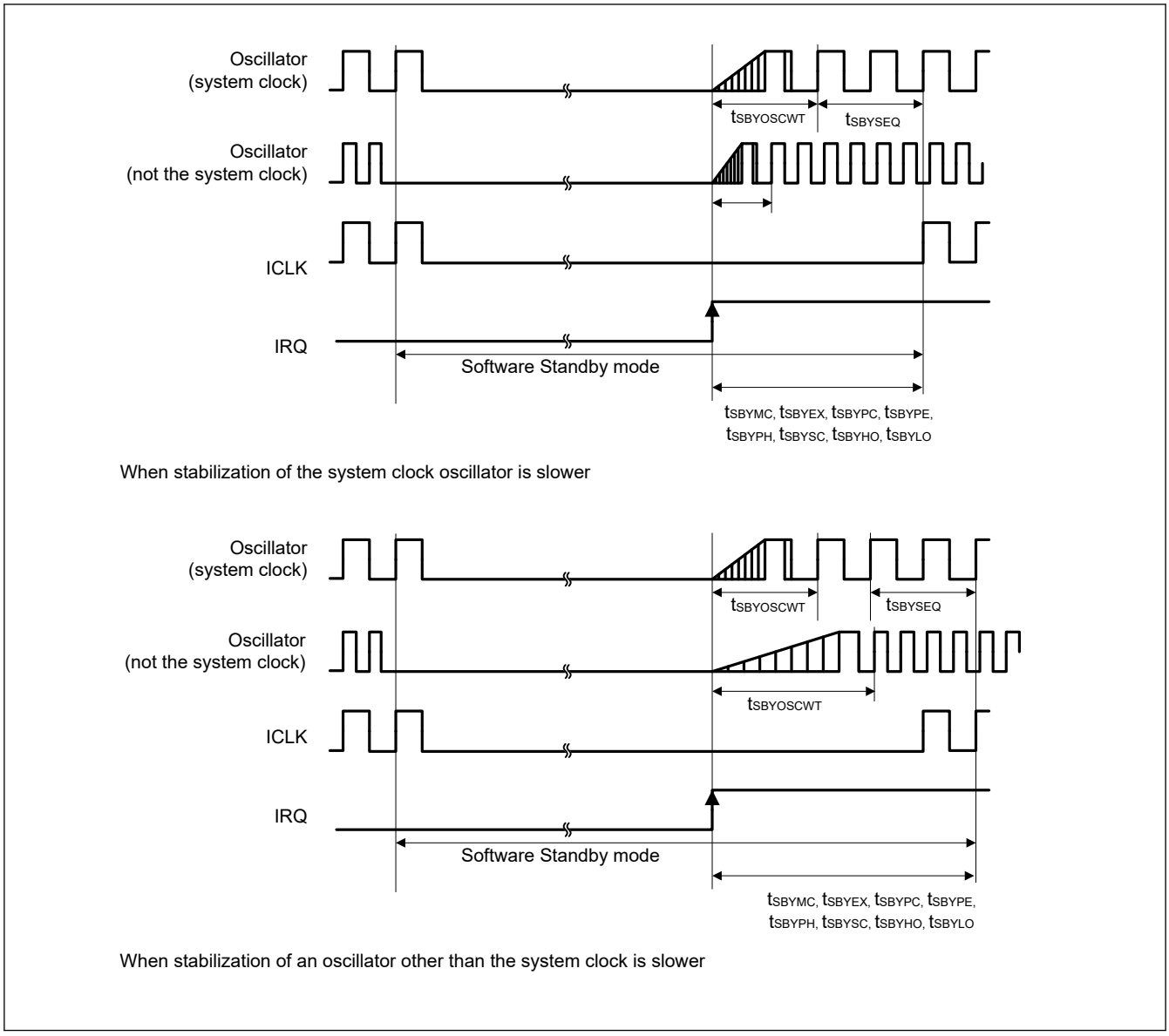


Figure 2.14 Software Standby mode cancellation timing

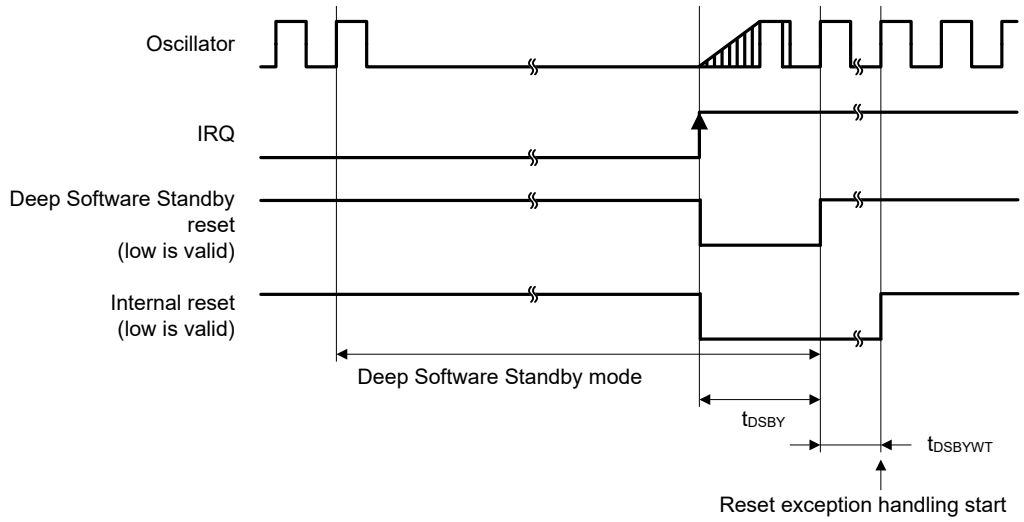
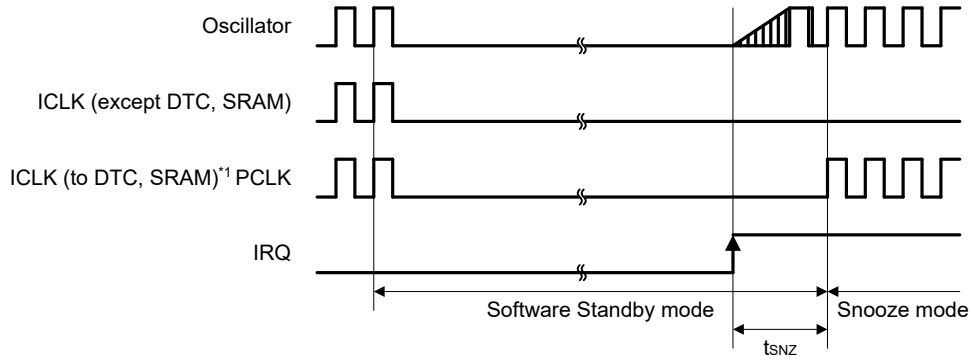


Figure 2.15 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.16 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.21 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

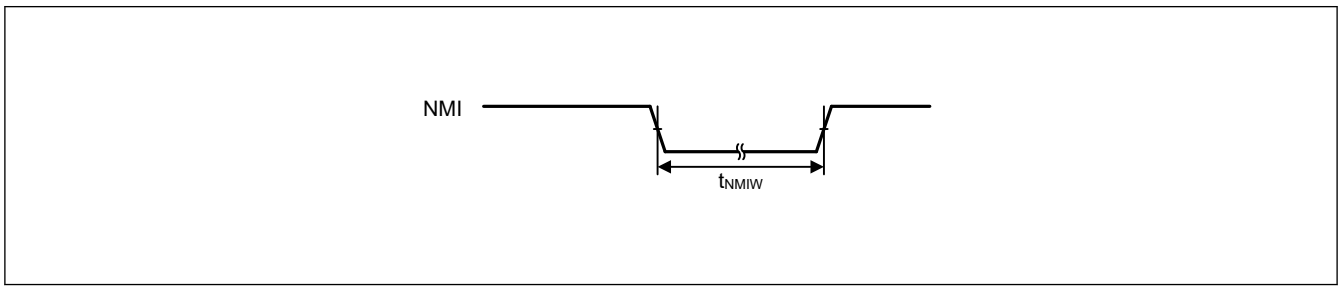


Figure 2.17 NMI interrupt input timing

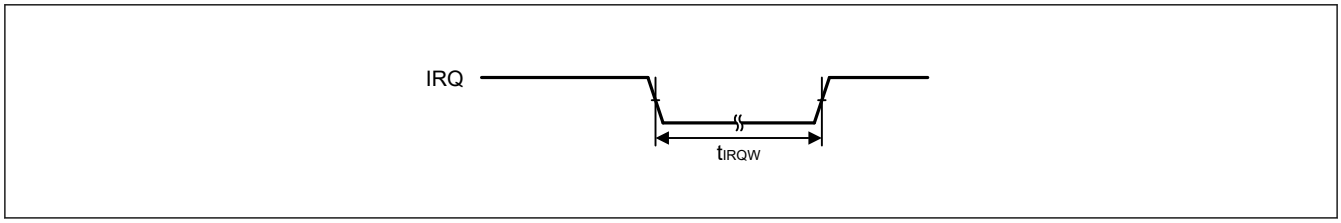


Figure 2.18 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, and ADC12 Trigger Timing

Table 2.22 I/O ports, POEG, GPT, AGT, and ADC12 trigger timing

GPT16E Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 2.19
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.20
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.21
		Dual edge		2.5	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive buffer	t_{GTISK}*1	—	4	ns	Figure 2.22
		High drive buffer		—	4		
	GTIOCxY output skew (x = 4, 5, Y = A or B)	Middle drive buffer		—	4		
		High drive buffer		—	4		
	GTIOCxY output skew (x = 0 to 5, Y = A or B)	Middle drive buffer		—	6		
		High drive buffer		—	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	—	5	ns	Figure 2.23
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*2	100	—	ns	Figure 2.24
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	—	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	—	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.25

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. Constraints on input cycle:

When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

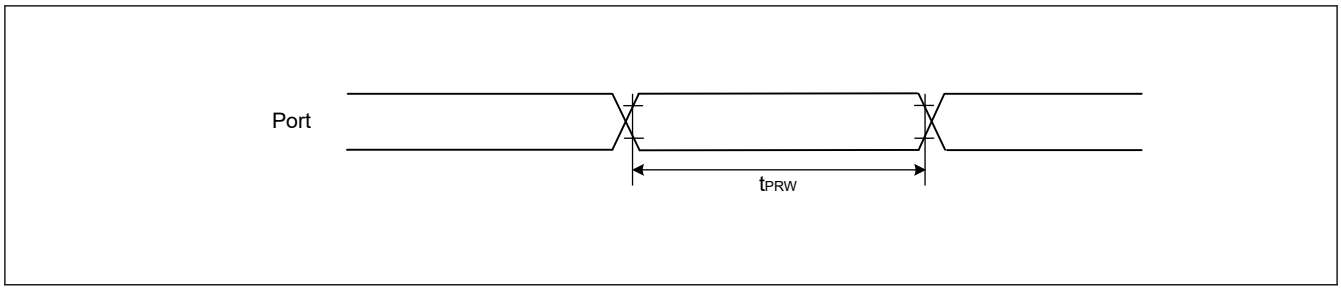


Figure 2.19 I/O ports input timing

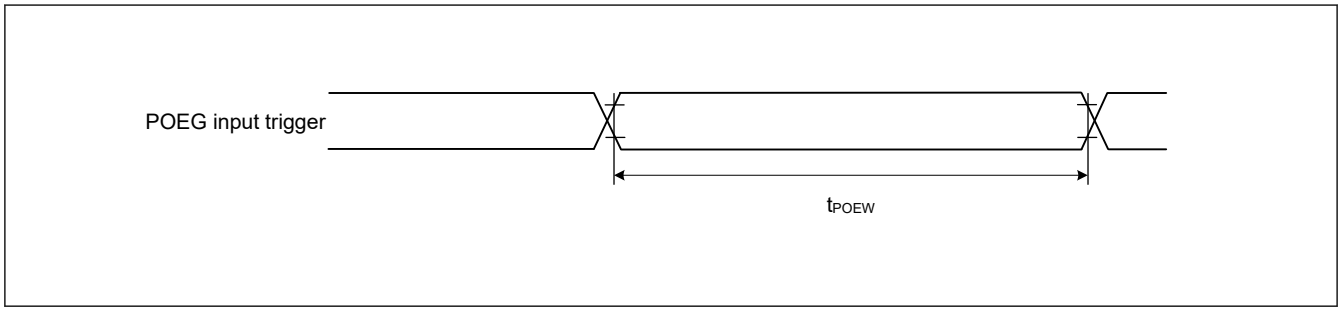


Figure 2.20 POEG input trigger timing

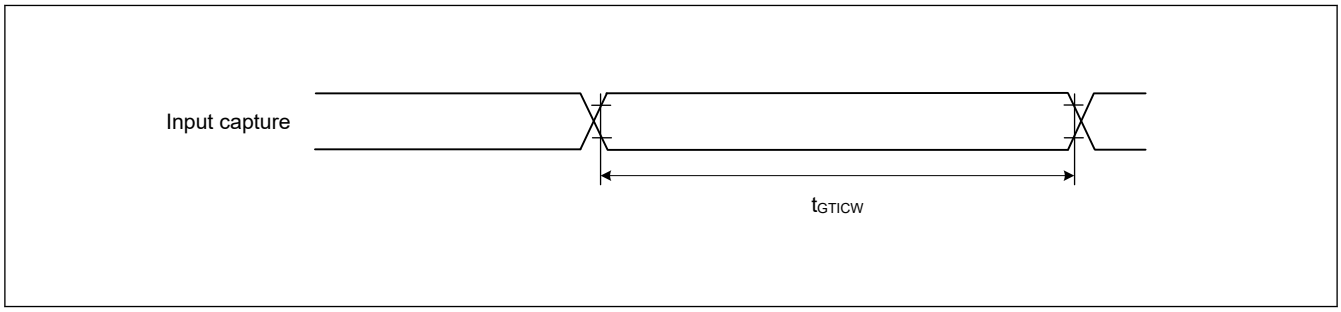


Figure 2.21 GPT input capture timing

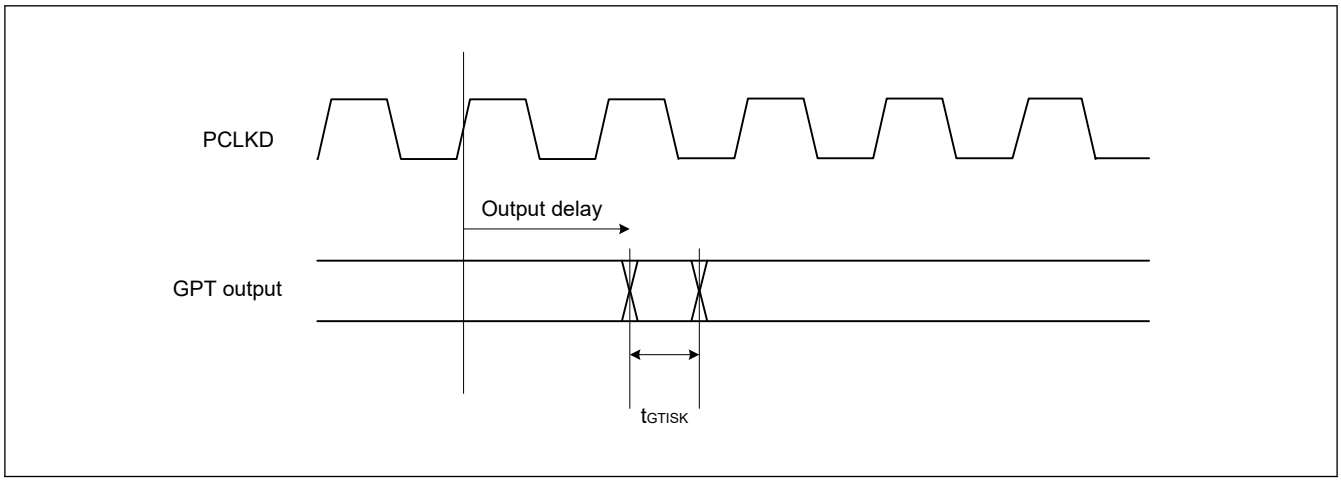


Figure 2.22 GPT output delay skew

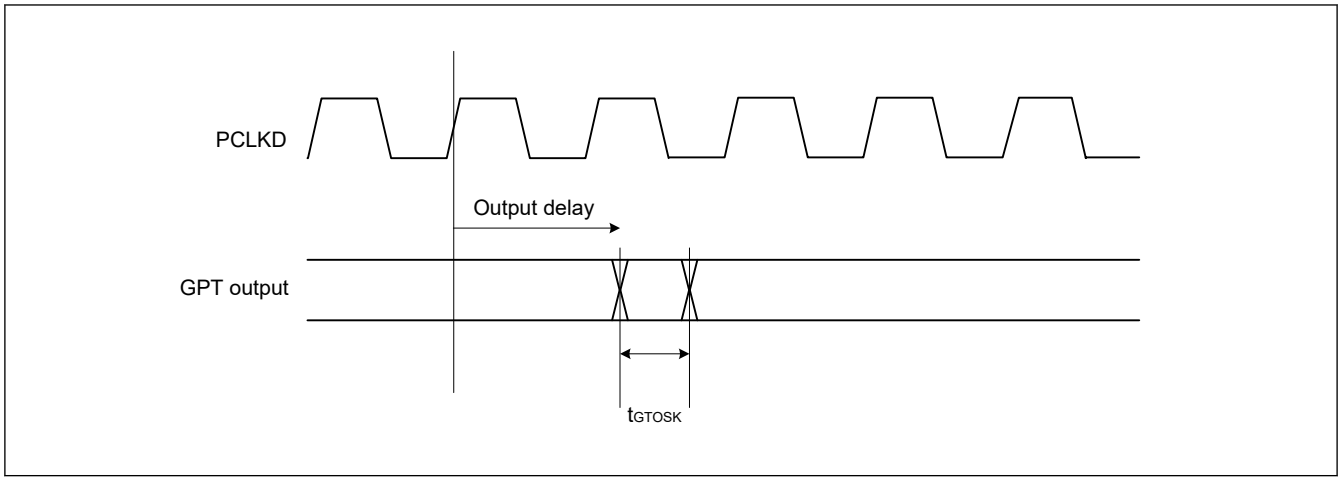


Figure 2.23 GPT output delay skew for OPS

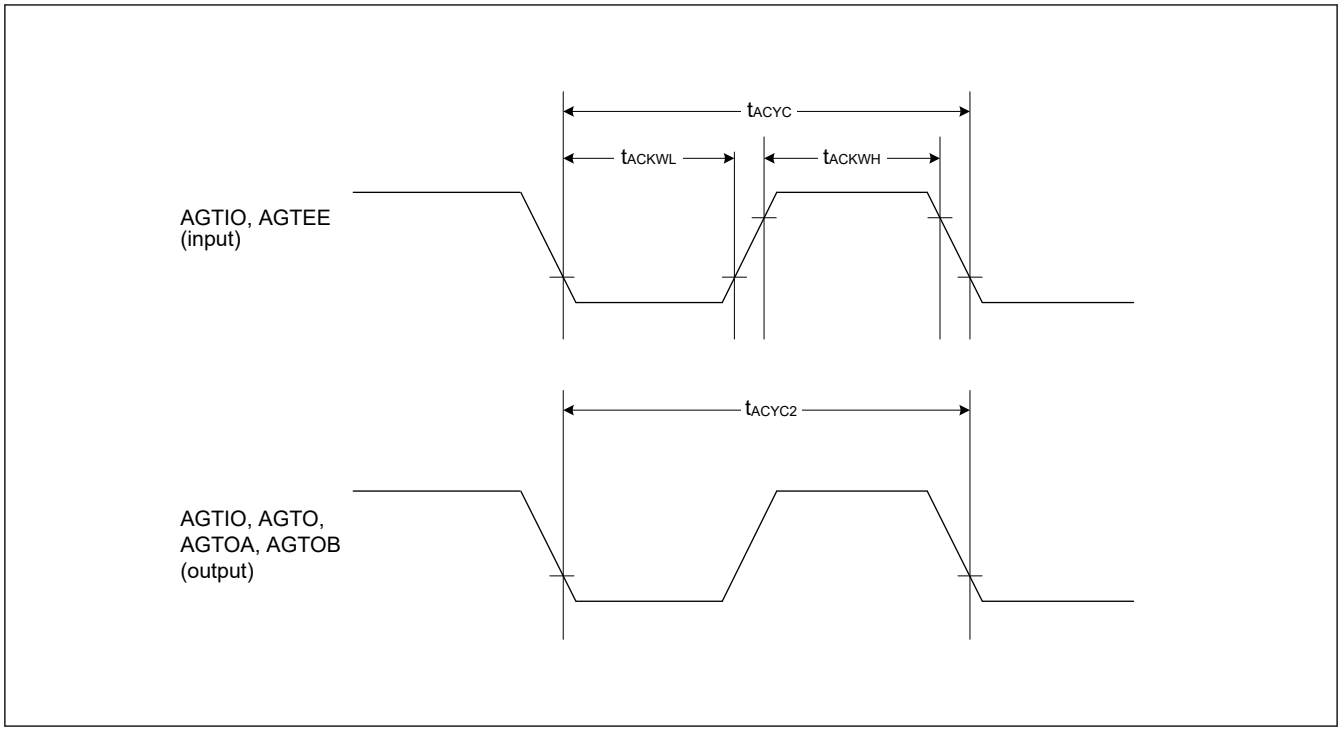


Figure 2.24 AGT input/output timing

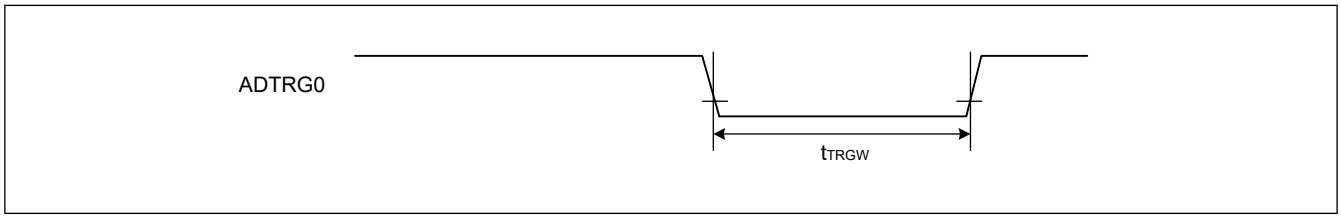


Figure 2.25 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.23 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

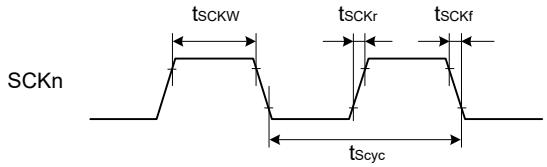
2.3.8 SCI Timing

Table 2.24 SCI timing (1)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

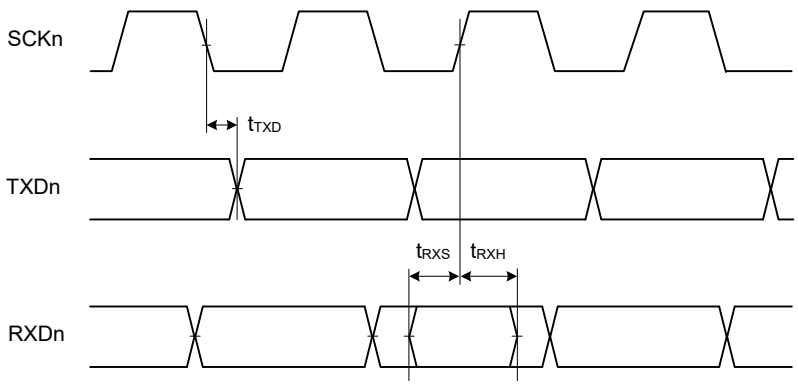
Parameter			Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 2.26
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay	Clock synchronous master mode (internal clock)	t_{TXD}	—	5	ns	Figure 2.27
		Clock synchronous slave mode (external clock)	t_{TXD}	—	25	ns	
	Receive data setup time	Clock synchronous master mode (internal clock)	t_{RXS}	15	—	ns	
		Clock synchronous slave mode (external clock)	t_{RXS}	5	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note: t_{Pcyc}: PCLKA cycle.



Note: n = 0, 9

Figure 2.26 SCK clock input/output timing



Note: n = 0, 9

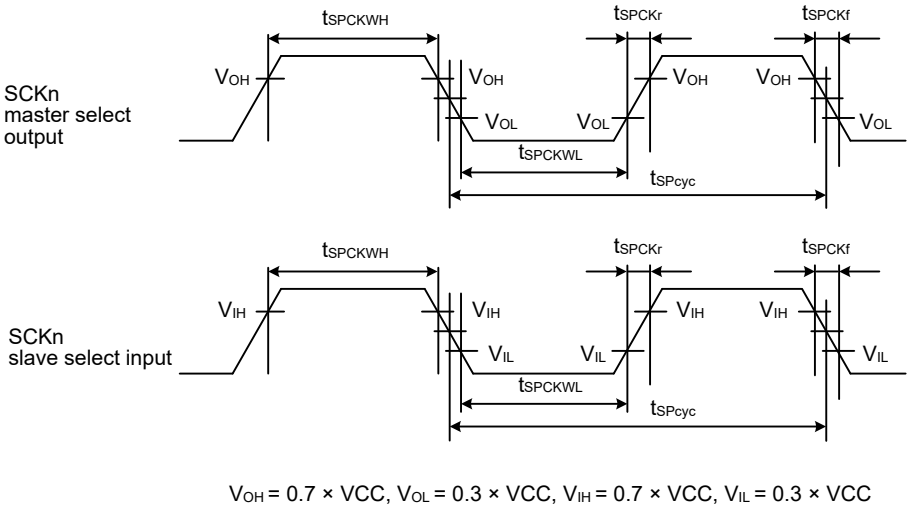
Figure 2.27 SCI input/output timing in clock synchronous mode

Table 2.25 SCI timing (2)

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.28
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr}, t_{SPCKf}	—	5	ns	
	Data input setup time	master	t_{SU}	15	—	ns	Figure 2.29 to Figure 2.32
		slave		5	—	ns	
	Data input hold time		t_{H}	5	—	ns	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	Data output delay	master	t_{OD}	—	5	ns	
		slave		—	25	ns	
	Data output hold time		t_{OH}	-5	—	ns	
	Data rise and fall time		t_{Dr}, t_{Df}	—	5	ns	
	SS input rise and fall time		t_{SSLr}, t_{SSLf}	—	5	ns	
	Slave access time		t_{SA}	—	3 × t_{Pcyc} + 25	ns	Figure 2.32
	Slave output release time		t_{REL}	—	3 × t_{Pcyc} + 25	ns	

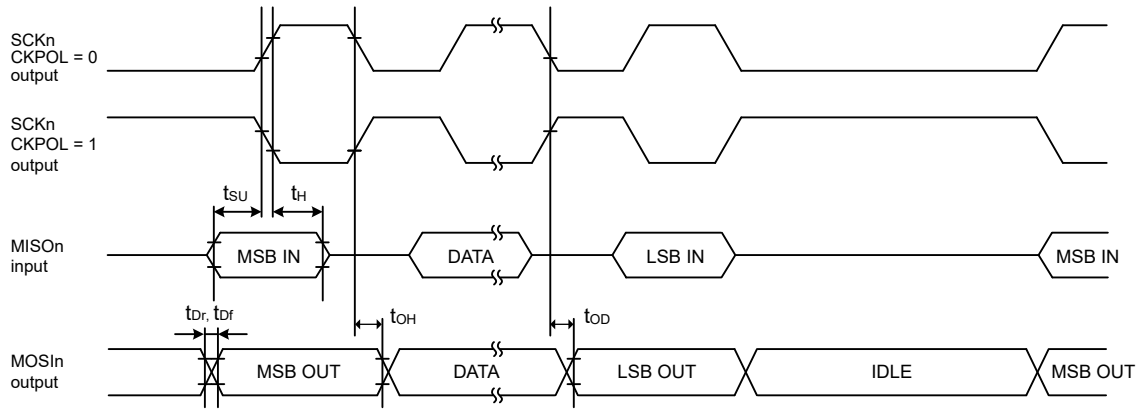
Note: t_{Pcyc}: PCLKA cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

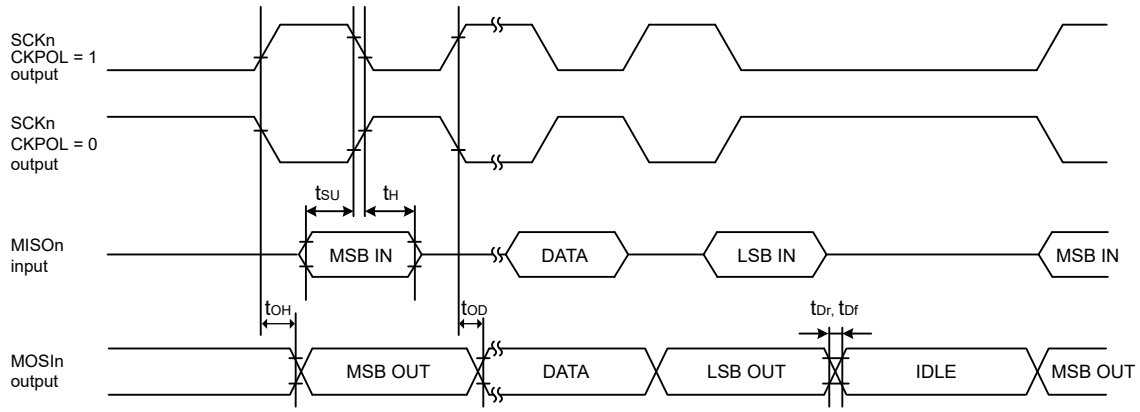
Note: n = 0, 9

Figure 2.28 SCI simple SPI mode clock timing



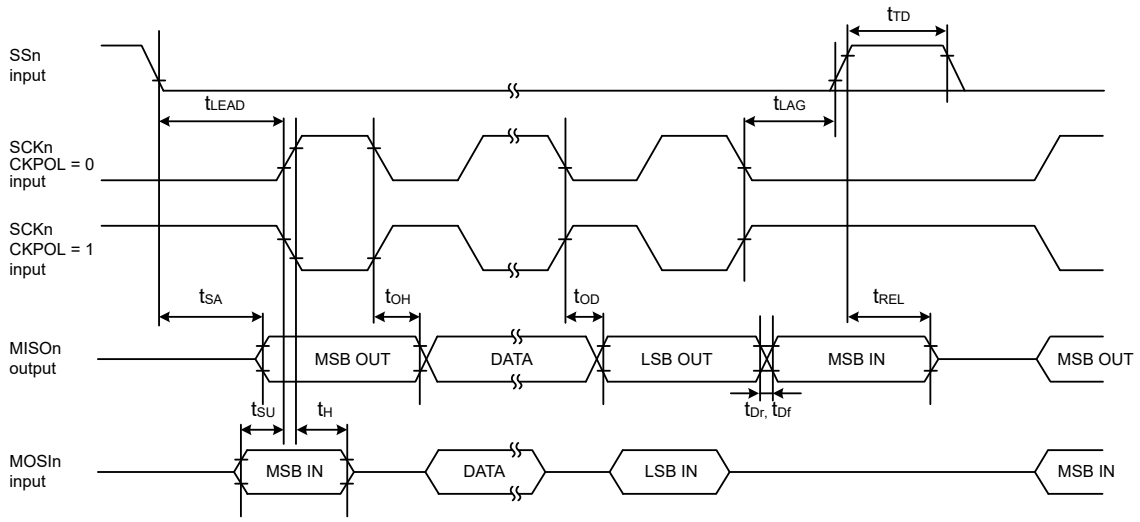
Note: n = 0, 9

Figure 2.29 SCI simple SPI mode timing for master when CKPH = 1



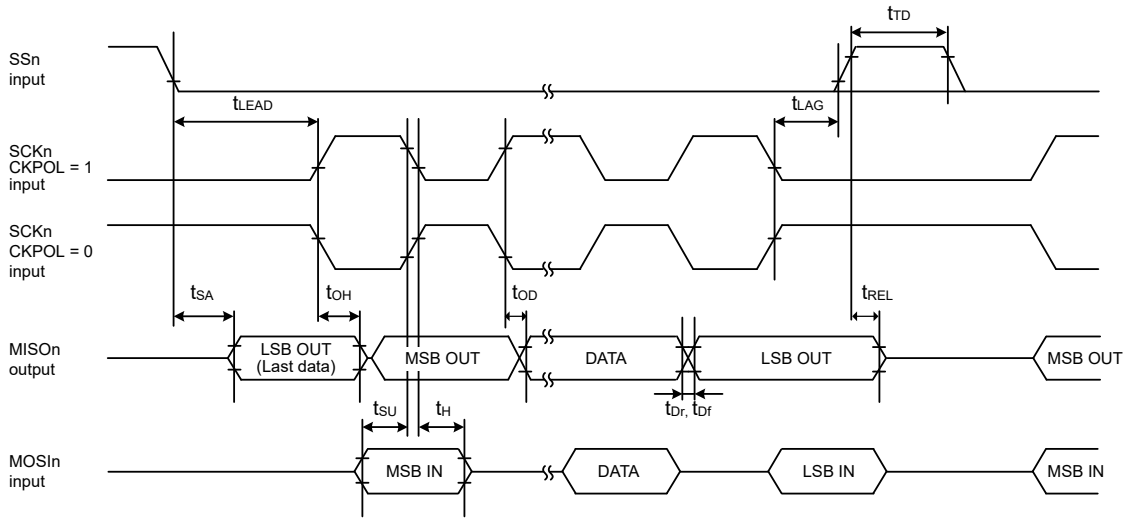
Note: n = 0, 9

Figure 2.30 SCI simple SPI mode timing for master when CKPH = 0



Note: n = 0, 9

Figure 2.31 SCI simple SPI mode timing for slave when CKPH = 1



Note: n = 0, 9

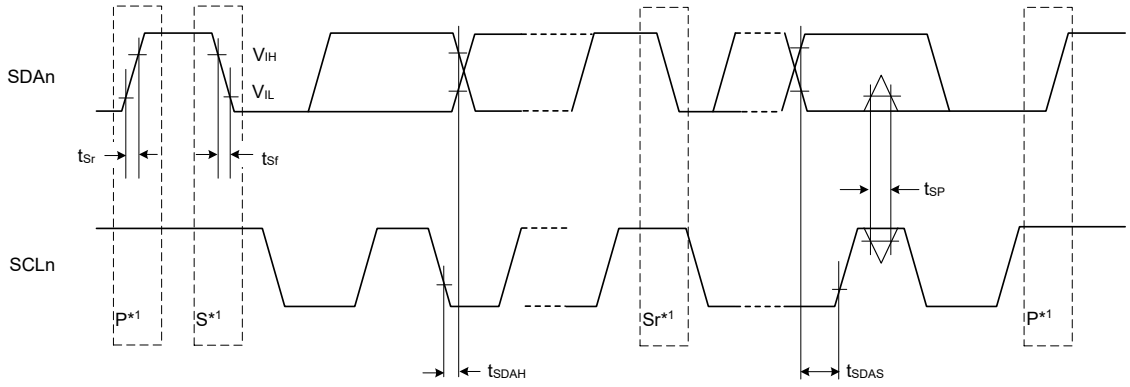
Figure 2.32 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.26 SCI timing (3)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.33
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.33 SCI simple IIC mode timing

2.3.9 SPI Timing

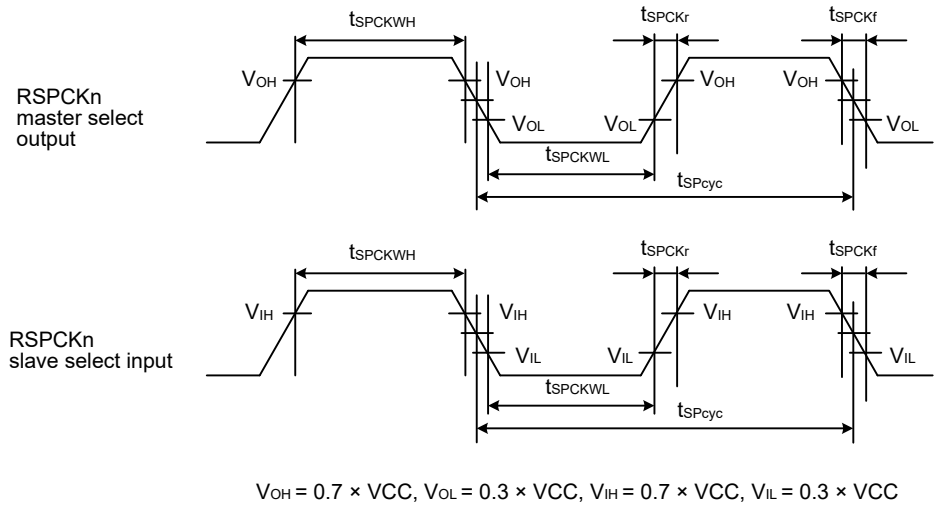
Table 2.27 SPI timing

Conditions: High drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.34
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Slave		—	1	µs	
	Data input setup time	Master	t_{SU}	4	—	ns	Figure 2.35 to Figure 2.40
		Slave		5	—		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	—	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_{H}	t_{Pcyc}	—		
		Slave	t_{H}	20	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc} - 10^{*1}$	$N \times t_{SPcyc} + 100^{*1}$	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc} - 10^{*2}$	$N \times t_{SPcyc} + 100^{*2}$	ns	
		Slave		$4 \times t_{Pcyc}$	—	ns	
	Data output delay	Master	t_{OD1}	—	6.3	ns	
			t_{OD2}		6.3		
		Slave	t_{OD}	—	20		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$4 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	25	ns	Figure 2.39 and Figure 2.40
	Slave output release time		t_{REL}	—	25		

Note: t_{Pcyc}: PCLKA cycle.

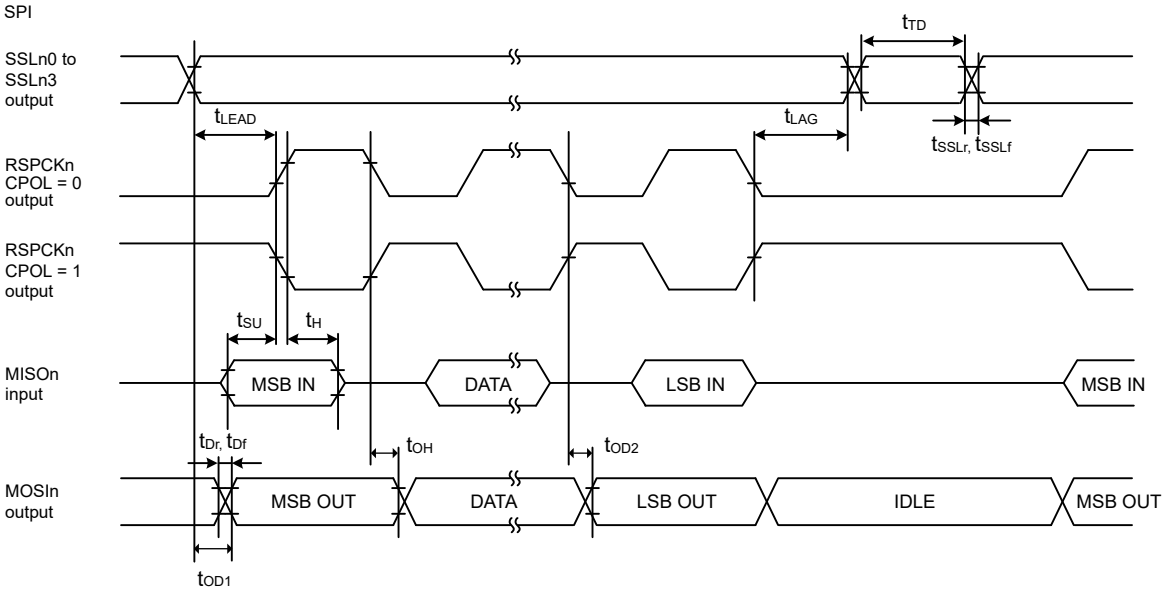
Note: Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. N is set to an integer from 1 to 8 by the SPCKD register.
Note 2. N is set to an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

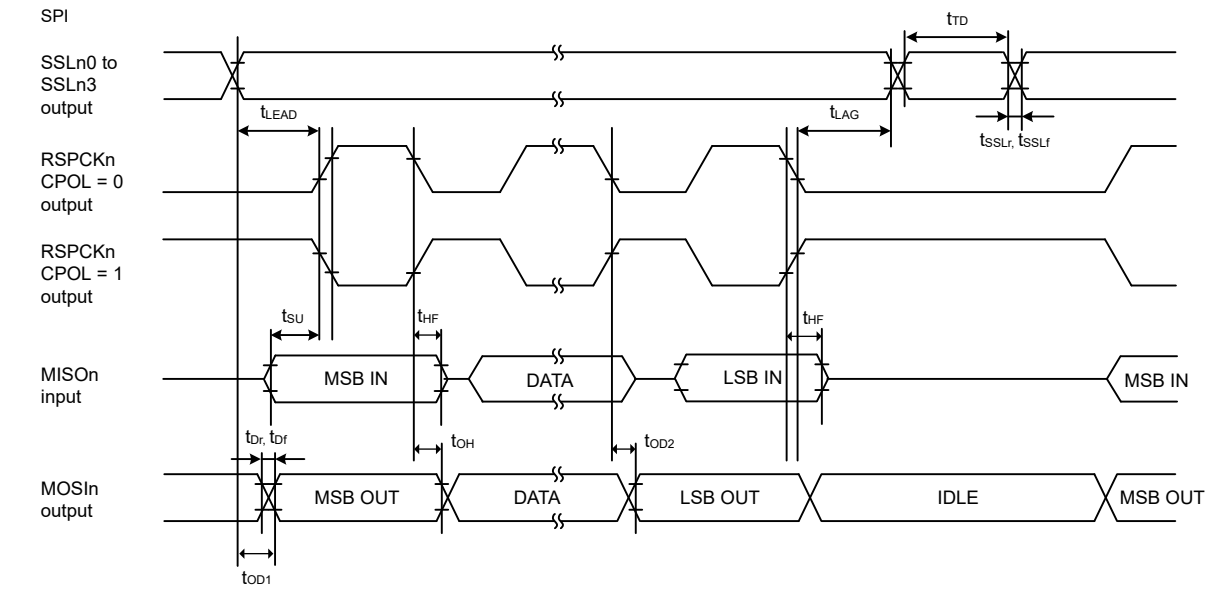
Note: n = A or B

Figure 2.34 SPI clock timing



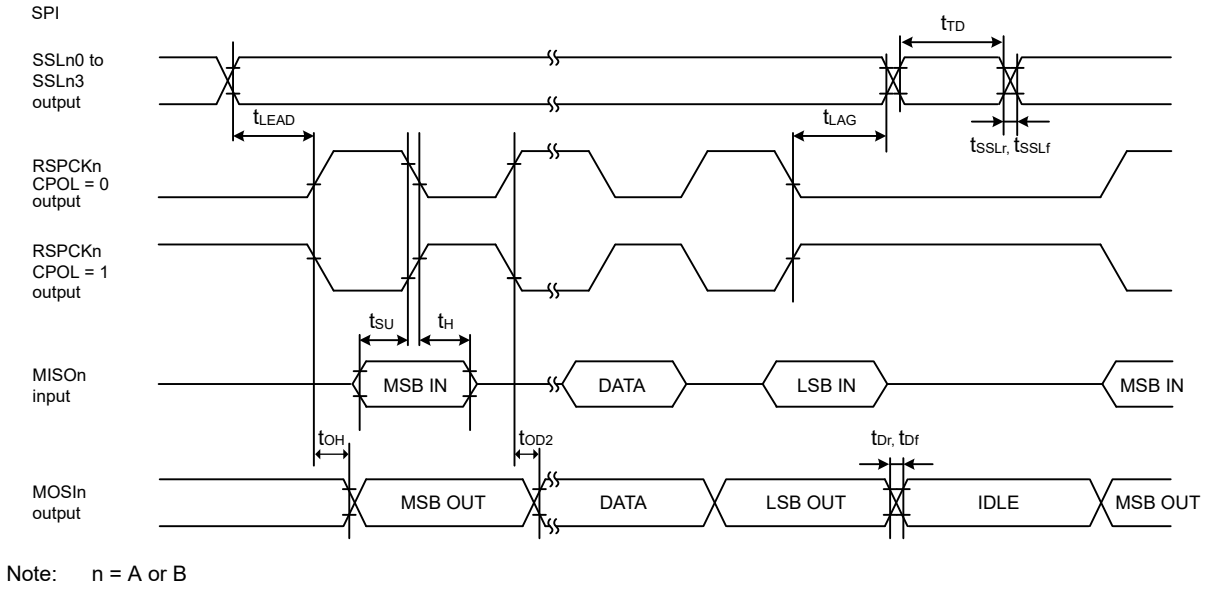
Note: n = A or B

Figure 2.35 SPI timing for master when CPHA = 0



Note: n = A or B

Figure 2.36 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2



Note: n = A or B

Figure 2.37 SPI timing for master when CPHA = 1

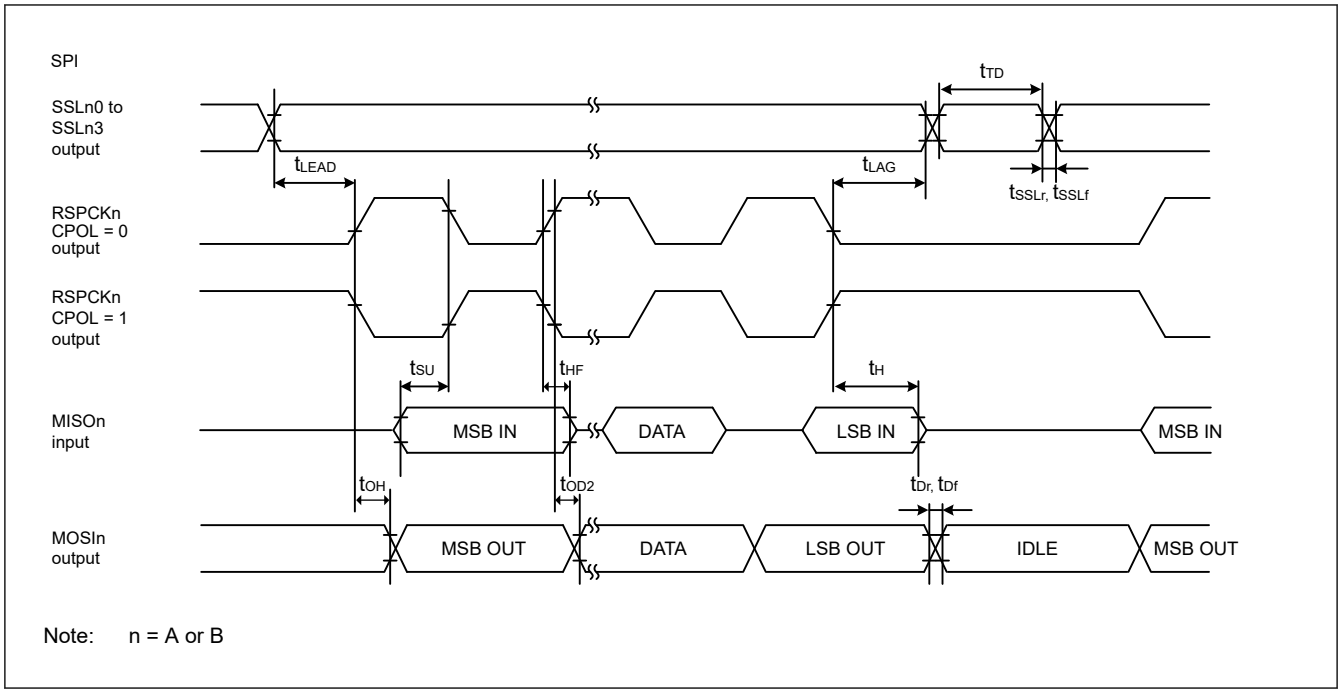


Figure 2.38 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

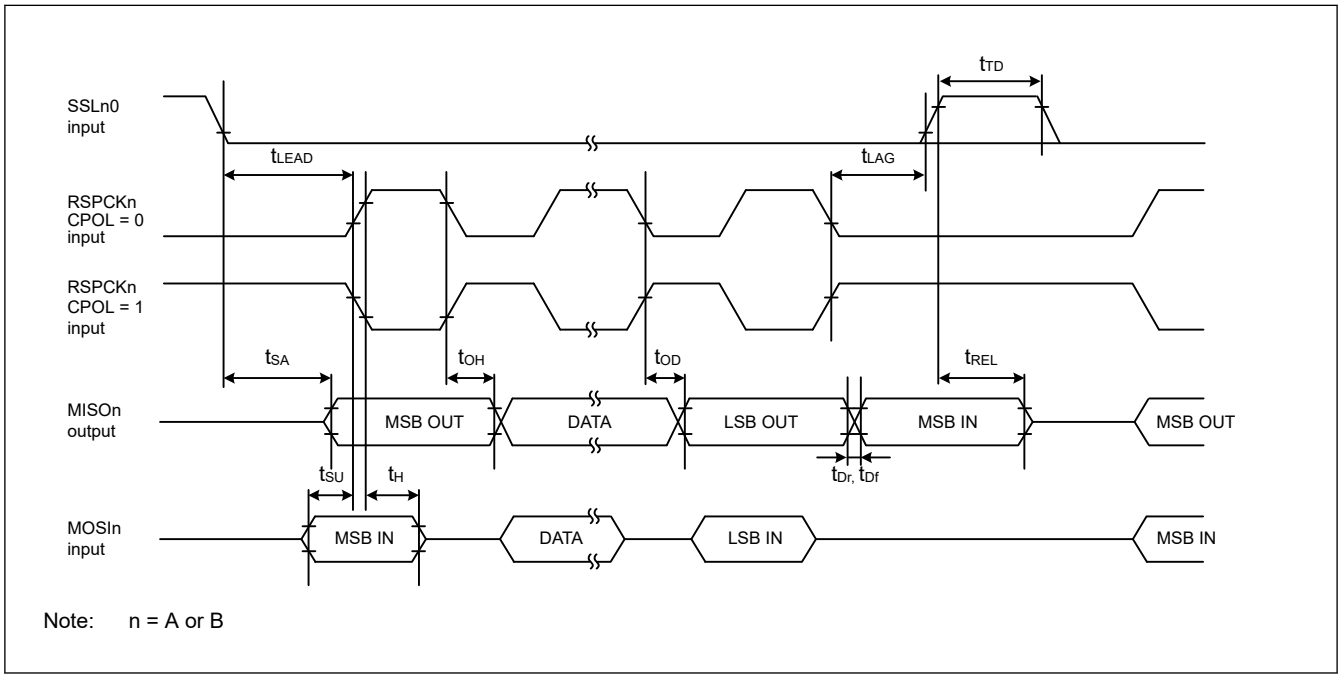
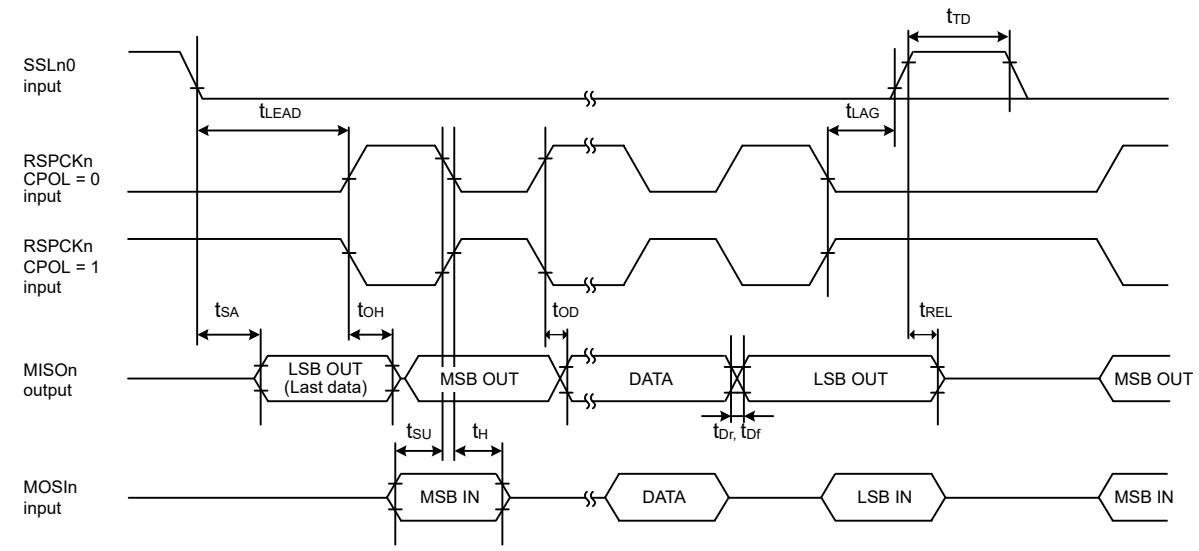


Figure 2.39 SPI timing for slave when CPHA = 0



Note: n = A or B

Figure 2.40 SPI timing for slave when CPHA = 1

2.3.10 I3C Timing

Table 2.28 IIC timing(1)-1

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	—	1000	ns
	SCL, SDA fall time	t_{Sf}	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	1000	—	ns
	STOP condition input setup time	t_{STOS}	1000	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. C_b indicates the total capacity of the bus line.

Table 2.29 IIC timing(1)-2

1. Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_A, SCL0_A, SDA0_B, SCL0_B, SDA0_C, SCL0_C.
2. The following pins do not require setting: SDA0_D, SCL0_D.
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	20 × (external pullup voltage/5.5 V)*1	300	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)*1	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	300	—	ns
	STOP condition input setup time	t_{STOS}	300	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*2	—	400	pF

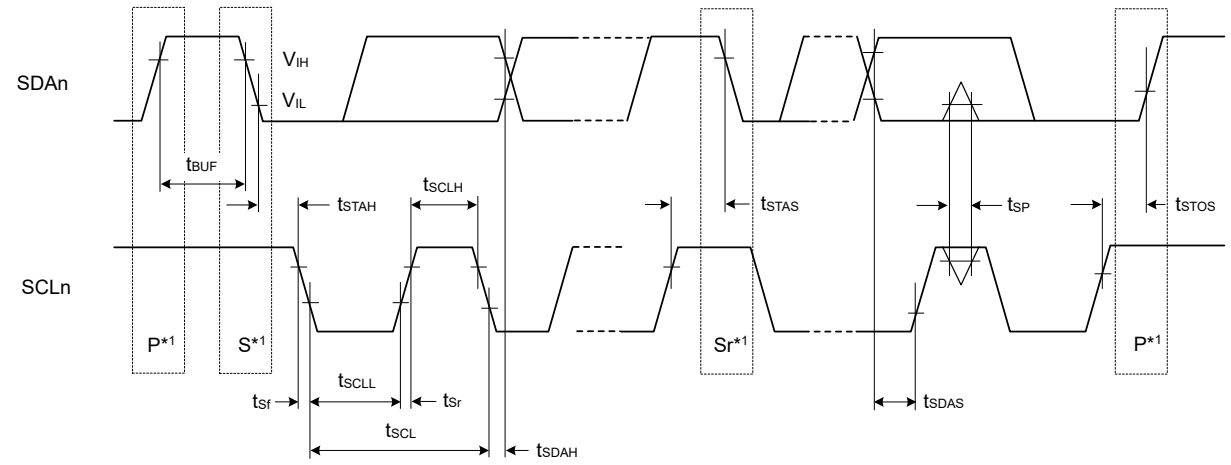
Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SDA0_D, SCL0_D.
Note 2. C_b indicates the total capacity of the bus line.

Table 2.30 IIC timing(1)-3

Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit
IIC (Fast-mode+) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	10(18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	5(9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	—	120	ns
	SCL, SDA fall time	t_{Sf}	20 × (external pullup voltage/5.5 V)	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	5(9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	1(5) × t_{I3Ccyc} + t_{Tcyc} + 120	—	ns
	Restart condition input setup time	t_{STAS}	120	—	ns
	Stop condition input setup time	t_{STOS}	120	—	ns
	Data input setup time	t_{SDAS}	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	0	—	ns
	SCL, SDA capacitive load	C_b*1	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: I3CCLK cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.41 I²C bus interface input/output timing

Table 2.31 IIC timing(2)

Conditions: VCC = 3.00 to 3.60 V
Setting of the SDA0_D, SCL0_D pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	55(57) × t_{I3Ccyc}	—	ns
	SCL input high pulse width	Cb = 400 pF	t_{SCLH}	43(44) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		23(24) × t_{I3Ccyc}	—	
	SCL input low pulse width	Cb = 400 pF	t_{SCLL}	64(65) × t_{I3Ccyc}	—	ns
		Cb = 100 pF		32(33) × t_{I3Ccyc}	—	
	SCL rise time	Cb = 400 pF	t_{SrCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA rise time	Cb = 400 pF	t_{SrDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL fall time	Cb = 400 pF	t_{SfCL}	—	80	ns
		Cb = 100 pF		—	40	
	SDA fall time	Cb = 400 pF	t_{SfDA}	—	160	ns
		Cb = 100 pF		—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	0	1(1) × t_{I3Ccyc}	ns
	Repeated START condition input setup time		t_{STAS}	40	—	ns
	STOP condition input setup time		t_{STOS}	40	—	ns
	Data input setup time		t_{SDAS}	10	—	ns
	Data input hold time	Cb = 400 pF	t_{SDAH}	0	150	ns
		Cb = 100 pF		0	70	
	SCL, SDA capacitive load		C_b*1	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0x3 while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

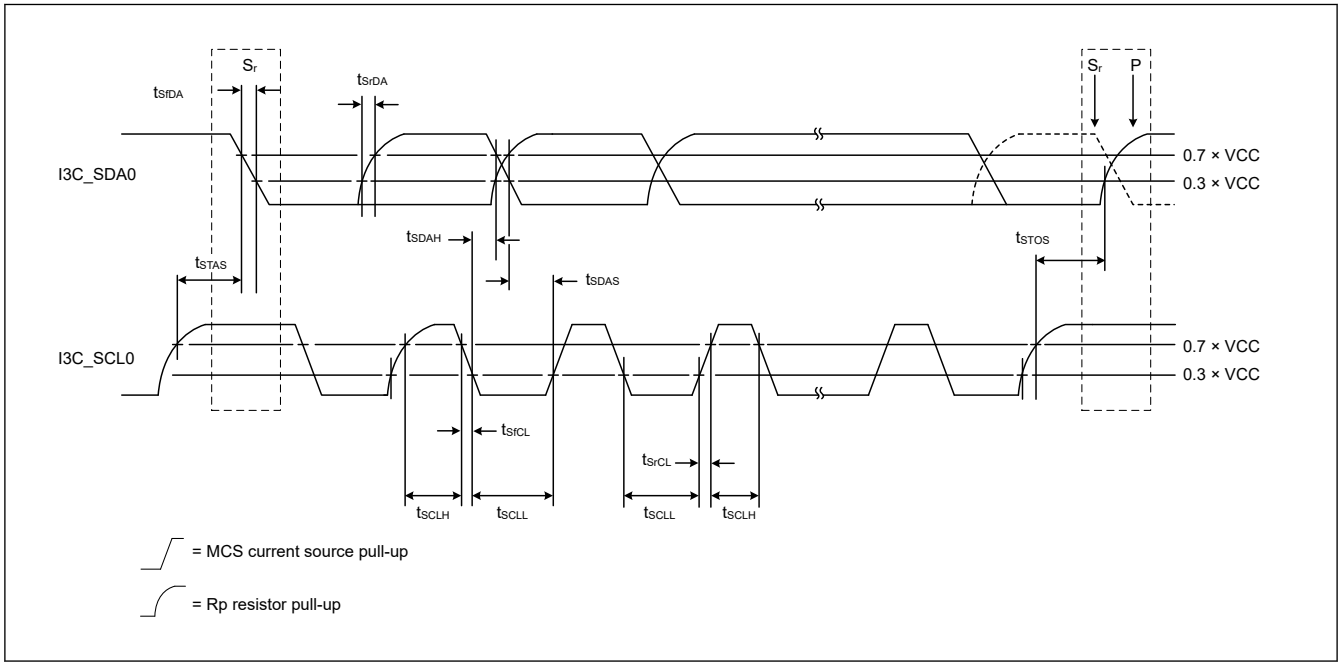


Figure 2.42 I²C bus interface input/output timing (Hs-mode)

Table 2.32 I3C timing (open drain timing parameters)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	200	—	ns	Figure 2.45
		$t_{DIG\_OD\_L}$	t_{LOW_ODmin} + t_{fDA_ODmin}	—	ns	Figure 2.45
	SCL Clock High Period	t_{HIGH} *3 *4	—	41	ns	Figure 2.43
		t_{DIG_H}	—	t_{HIGH} + t_{CF}	ns	Figure 2.43
	SDA Signal Fall Time	t_{fDA_OD}	t_{CF}	12	ns	Figure 2.45
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	17	—	ns	Figure 2.44
	Clock After START (S) Condition	t_{CAS} *5 *6	38.4 nano	For ENAS0: 1 µ	seconds	Figure 2.45
				For ENAS1: 100 µ		
				For ENAS2: 2 milli		
				For ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	t_{CASmin} / 2	—	seconds	Figure 2.46
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 2.51
	Bus Available Condition	t_{AVAL} *7	1	—	µs	—
	Bus Idle Condition	t_{IDLE}	1	—	ms	—
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	$t_{AVALmin}$	—	µs	Figure 2.51

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_Odmin}.
Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH
Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect
Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.
Note 5. On a legacy bus where I^2C devices need to see Start
Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3
Note 7. On a mixed bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.33 I3C timing (push-pull timing parameters for SDR mode)

Conditions: VCC = 3.00 to 3.60 V
Setting of the I3C_SDA, I3C_SCL pins is not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for SDR Mode	SCL Clock Frequency		f_{SCL} *1	0.01	12.5	MHz	—
	SCL Clock Low Period		t_{LOW}	24	—	ns	Figure 2.43
			t_{DIG_L} *2 *4	40	—	ns	Figure 2.43
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24	—	ns	Figure 2.43
			$t_{DIG\_H\_MIXED}$ *2 *3	40	45	ns	Figure 2.43
	SCL Clock High Period		t_{HIGH}	24	—	ns	Figure 2.43
			t_{DIG_H} *2	40	—	ns	Figure 2.43
	Clock in to Data Out for Slave		t_{SCO}	—	12	ns	Figure 2.48
	SCL Clock Rise Time		t_{CR}	—	150 × 1 /f_{SCL} (capped at 60)	ns	Figure 2.43
	SCL Clock Fall Time		t_{CF}	—	150 × 1 /f_{SCL} (capped at 60)	µs	Figure 2.43
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 2.47
		Slave	t_{HD_PP}	0	—	—	Figure 2.47
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	17	N/A	ns	Figure 2.49
	Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	N/A	ns	Figure 2.50
	Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	N/A	ns	Figure 2.50
	Capacitive Load per Bus Line (SDA/SCL)		C_b	—	50	pF	—

Note 1. f_{SCL} = 1 / (t_{DIG_L} + t_{DIG_H})
Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.
Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

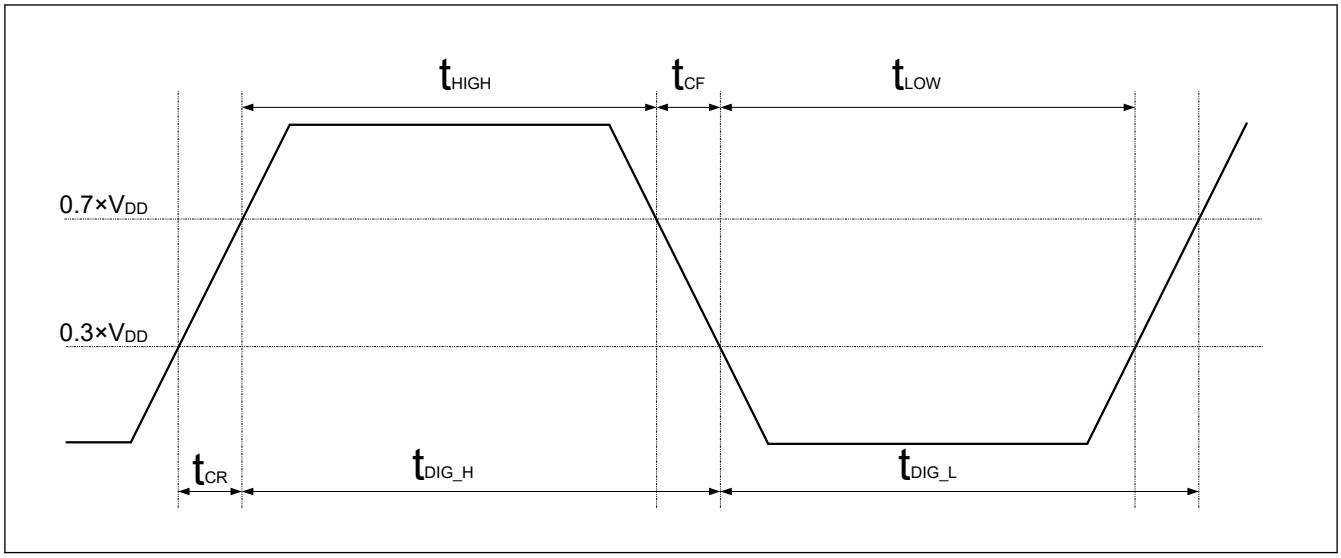


Figure 2.43 t_{DIG_H} and t_{DIG_L}

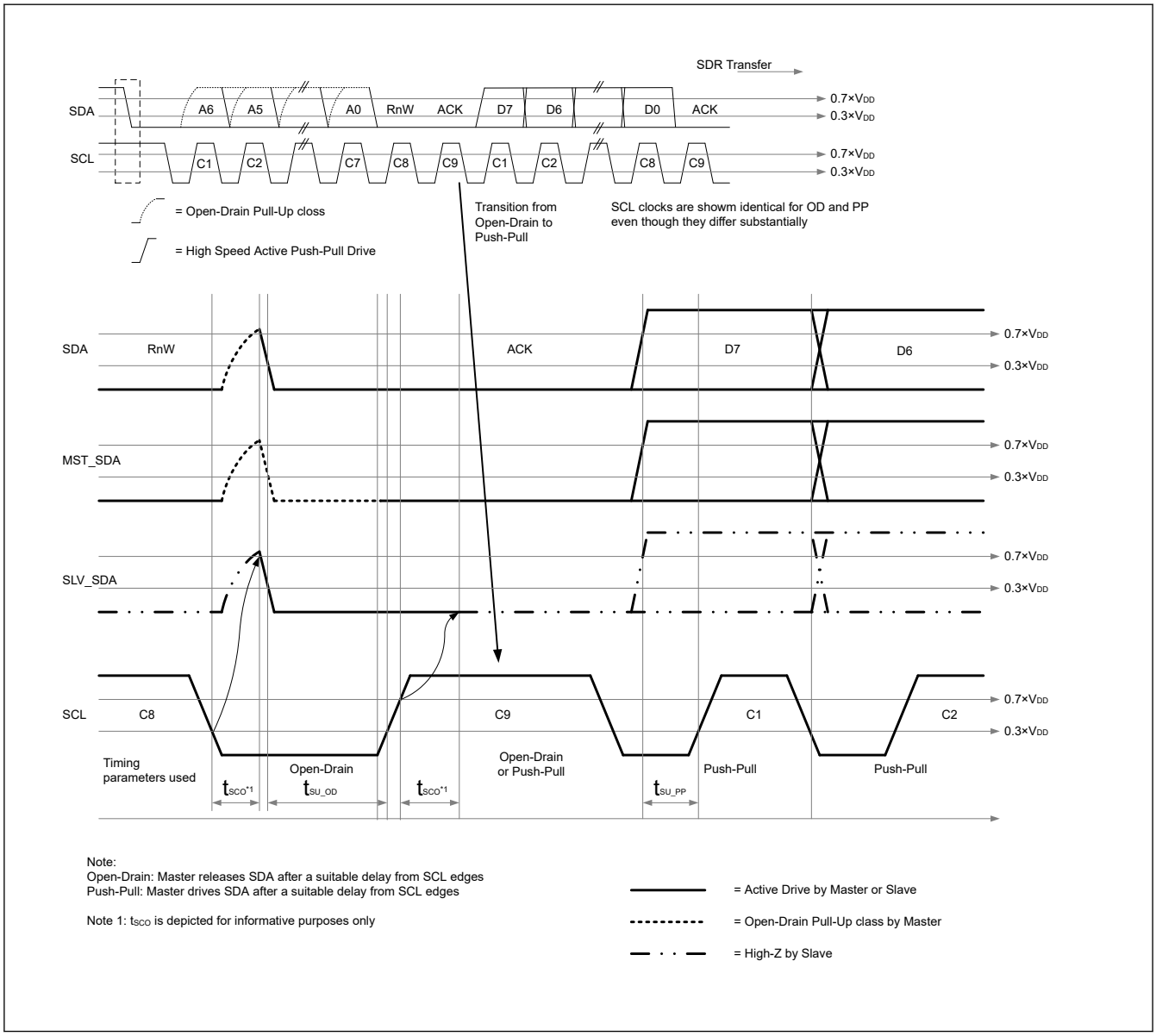


Figure 2.44 I3C data transfer – ACK by slave

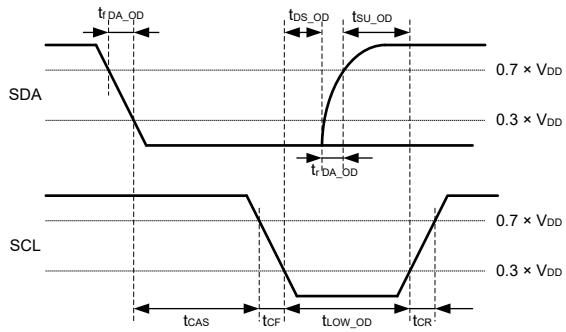


Figure 2.45 I3C START condition timing

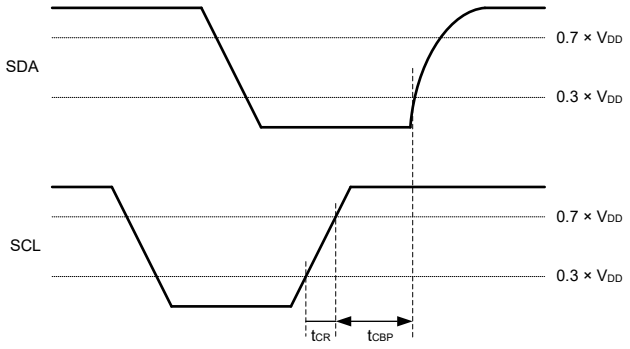


Figure 2.46 I3C STOP condition timing

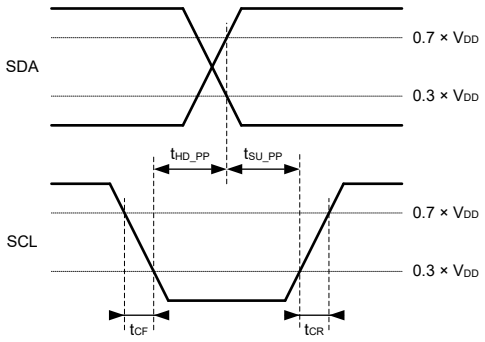


Figure 2.47 I3C master out timing

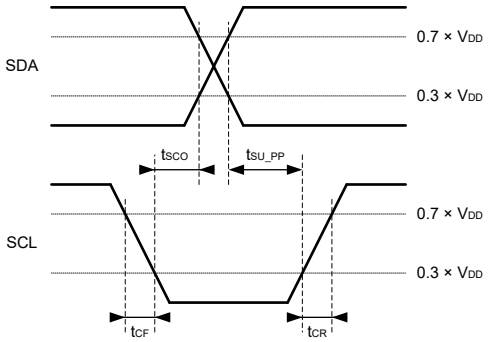


Figure 2.48 I3C slave out timing

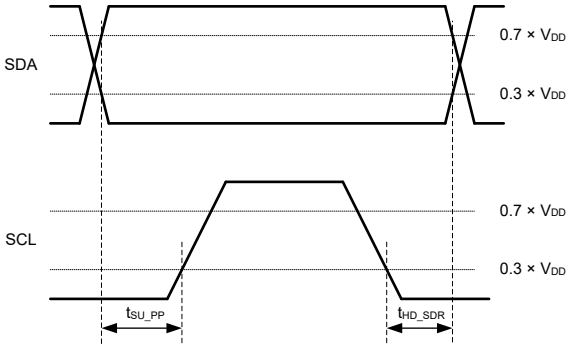


Figure 2.49 Master SDR timing

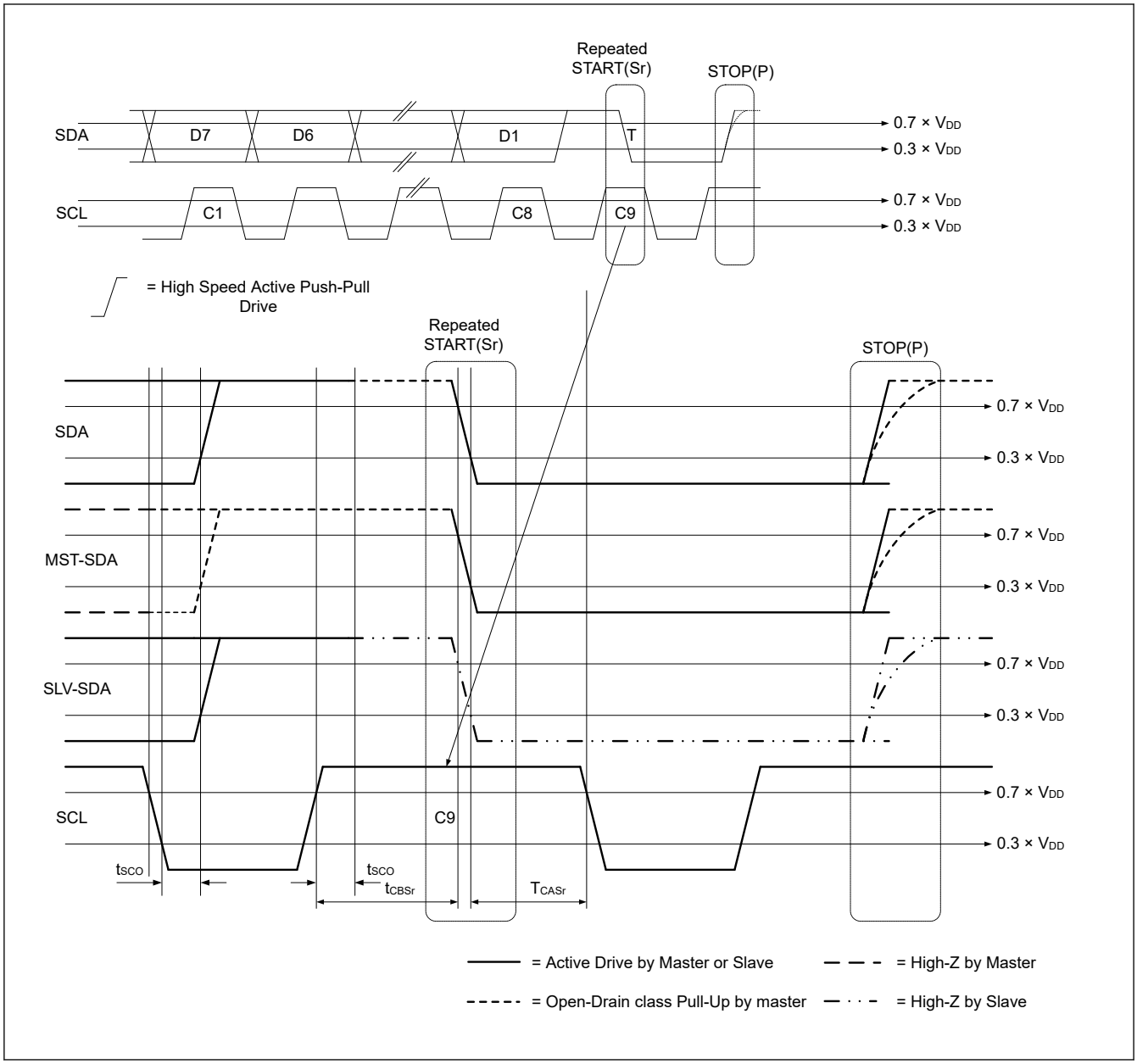


Figure 2.50 T-bit when master ends read with repeated START and STOP

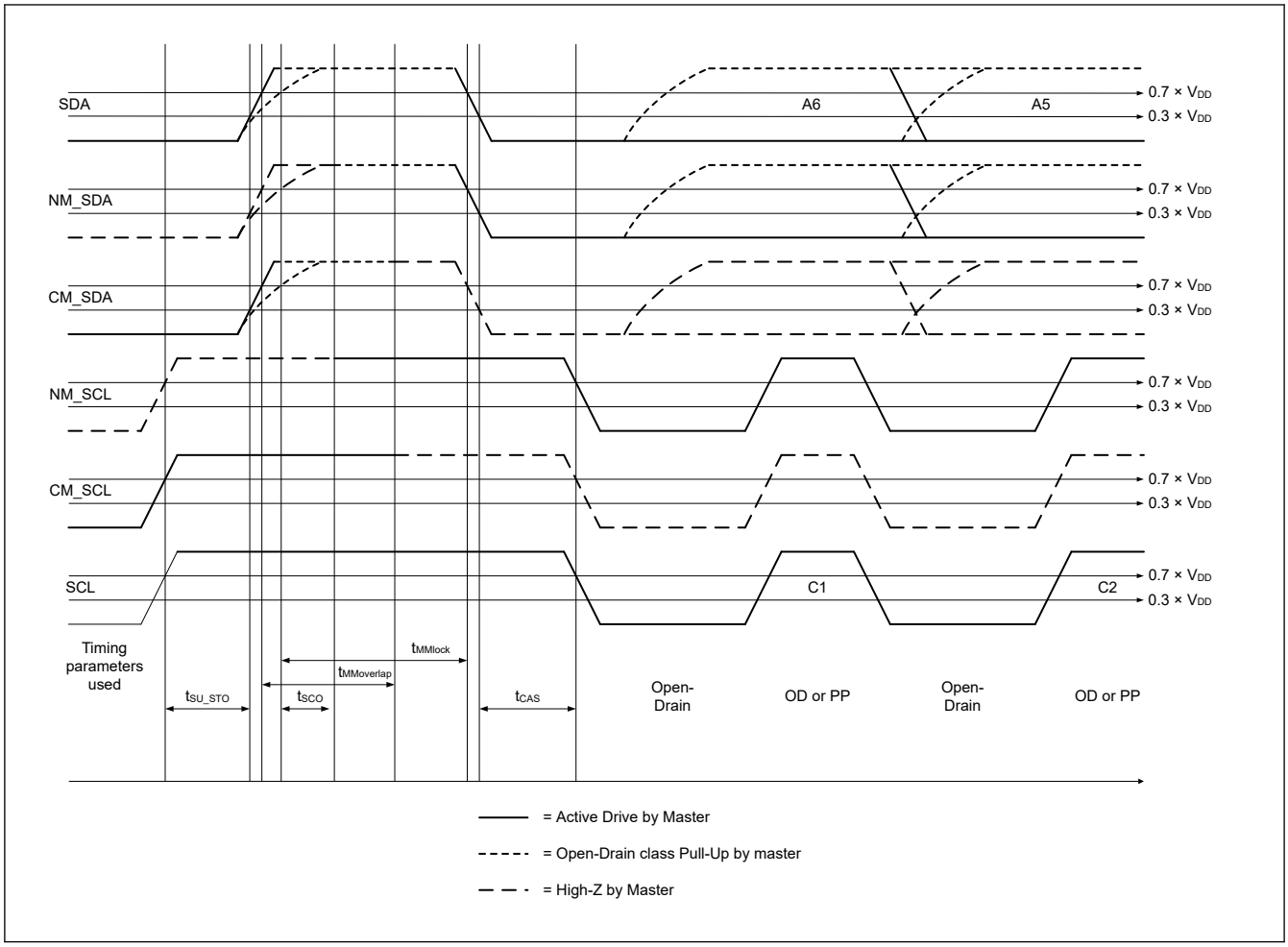


Figure 2.51 I3C timing (open drain timing parameters)

2.3.11 CANFD Timing

Table 2.34 CANFD interface timing

Parameter	Symbol	CAN-FD		Unit	Test conditions
		Min	Max		
Internal delay time	t_{node}	—	75	ns	Figure 2.52

Note: $t_{node} = t_{d(CTX)} + t_{d(CRX)}$

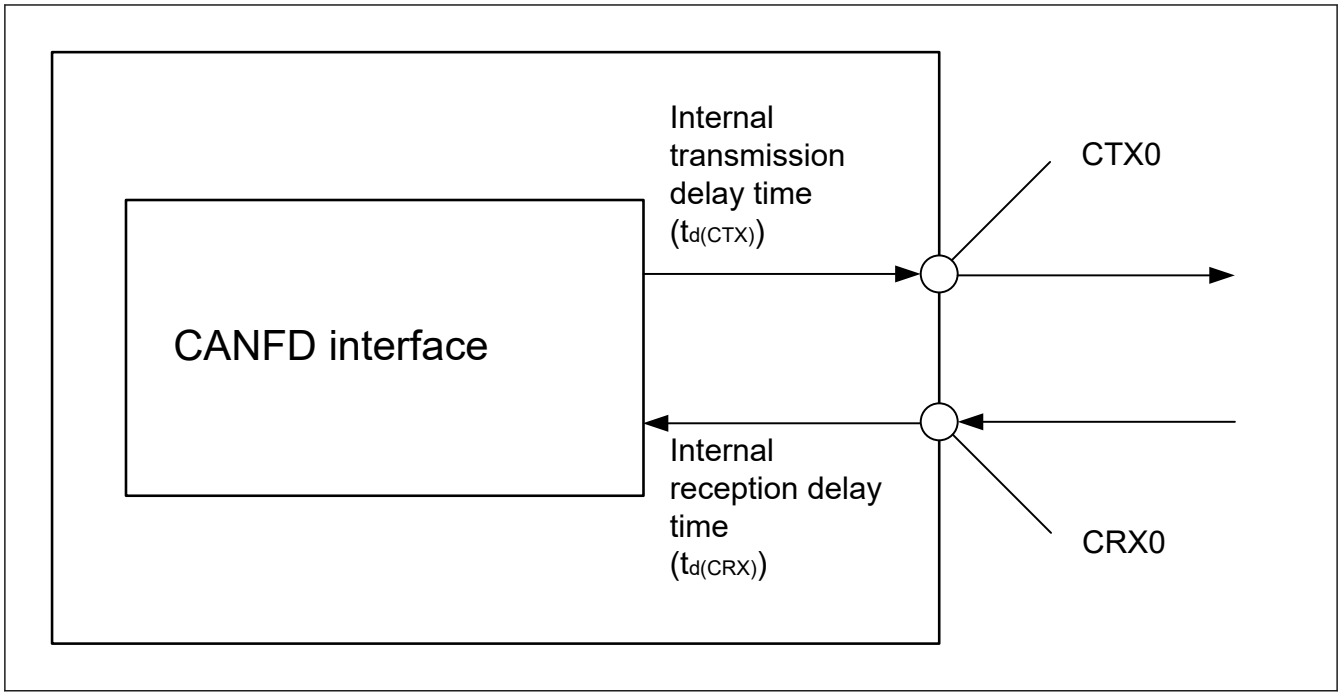


Figure 2.52 CANFD interface condition

2.4 ADC12 Characteristics

Table 2.35 A/D conversion characteristics for unit 0 (1 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	—	50	MHz	—
Analog input capacitance			—	—	30	pF	—
Quantization error			—	±0.5	—	LSB	—
Resolution			—	—	12	Bits	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.24 (0.48 + 0.26)*2	—	—	μs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states. • Sampling in 13 states
	Offset error		—	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		—	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		—	±2.5	±5.5	LSB	—
	DNL differential nonlinearity error		—	±1.0	±2.0	LSB	—
	INL integral nonlinearity error		—	±1.5	±3.0	LSB	—
	Holding characteristics of sample-and hold circuits		—	—	20	μs	—
	Dynamic range		0.25	—	VREFH0 – 0.25	V	—

Table 2.35 A/D conversion characteristics for unit 0 (2 of 2)

Conditions: PCLKC = 1 to 50 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.52 (0.26)*2	—	—	µs	Sampling in 13 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision high-speed channels (AN007)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.80 (0.54)*2	—	—	µs	Sampling in 27 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
High-precision normal-speed channels (AN004 to AN006, AN008, AN011 to AN013)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±2.5	LSB	—
	Full-scale error		—	±1.0	±2.5	LSB	—
	Absolute accuracy		—	±2.0	±4.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±1.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±2.5	LSB	—
Normal-precision normal-speed channels (AN016)	Conversion time*1 (Operation at PCLKC = 50 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.92 (0.66)*2	—	—	µs	Sampling in 33 states
	Offset error		—	±1.0	±5.5	LSB	—
	Full-scale error		—	±1.0	±5.5	LSB	—
	Absolute accuracy		—	±2.0	±7.5	LSB	—
	DNL differential nonlinearity error		—	±0.5	±4.5	LSB	—
	INL integral nonlinearity error		—	±1.0	±5.5	LSB	—

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of PORT0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFL0, and 12-bit A/D converter input voltage are stable.

Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.

Note 2. Values in parentheses indicate the sampling time.

Table 2.36 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	—
Sampling time	4.15	—	—	µs	—

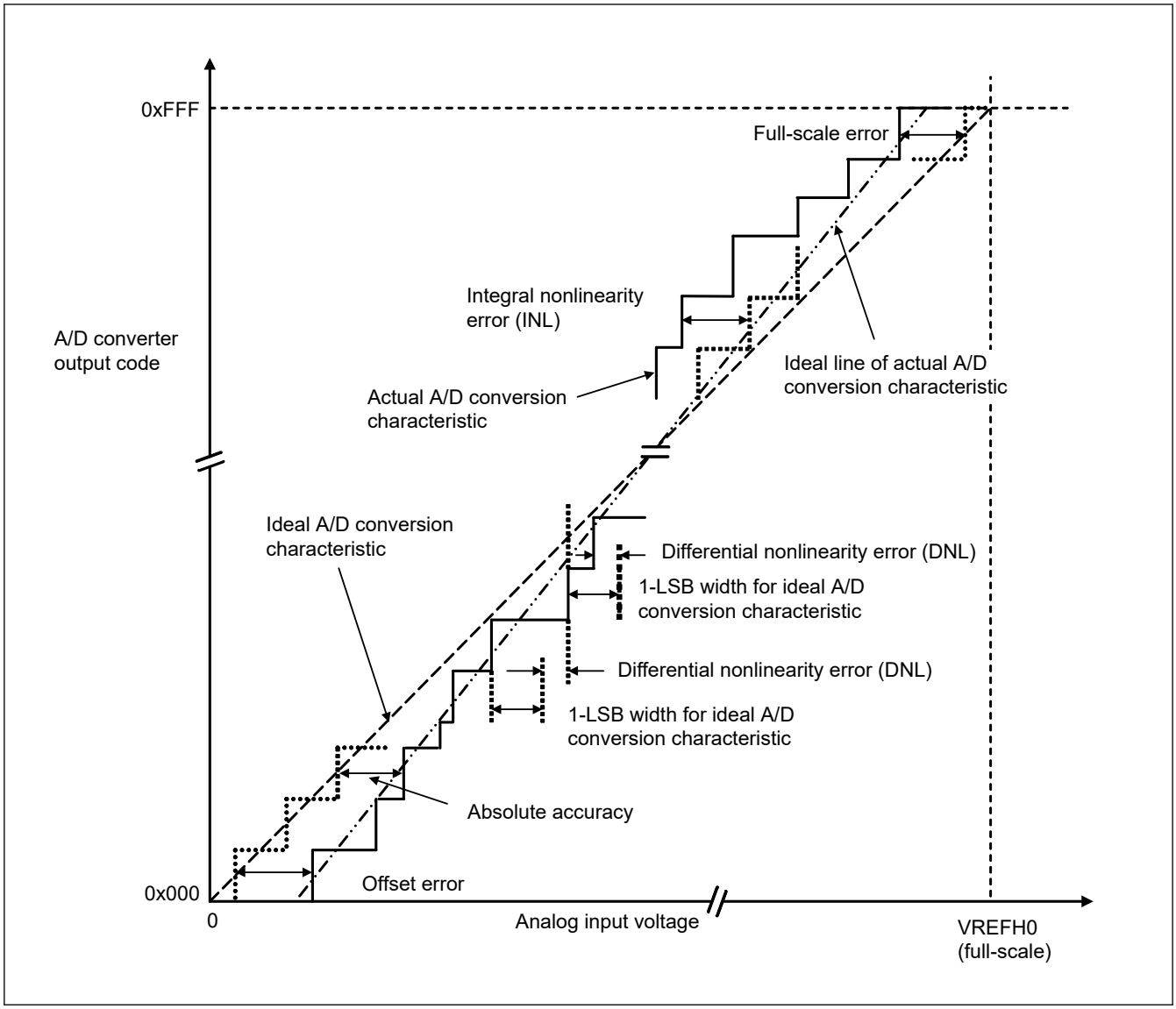


Figure 2.53 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then the 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 DAC12 Characteristics

Table 2.37 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	—	—	12	Bits	—
Without output amplifier					
Absolute accuracy	—	—	±24	LSB	Resistive load 2 MΩ
INL	—	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	—	±1.0	±2.0	LSB	—
Output impedance	—	8.5	—	kΩ	—
Conversion time	—	—	3	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	—	VREFH	V	—
With output amplifier					
INL	—	±2.0	±4.0	LSB	—
DNL	—	±1.0	±2.0	LSB	—
Conversion time	—	—	4.0	µs	—
Resistive load	5	—	—	kΩ	—
Capacitive load	—	—	50	pF	—
Output voltage range	0.2	—	VREFH – 0.2	V	—

2.6 TSN Characteristics

Table 2.38 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.0	—	°C	—
Temperature slope	—	—	4.0	—	mV/°C	—
Output voltage (at 25 °C)	—	—	1.24	—	V	—
Temperature sensor start time	t_{START}	—	—	30	µs	—
Sampling time	—	4.15	—	—	µs	—

2.7 OSC Stop Detect Characteristics

Table 2.39 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.54

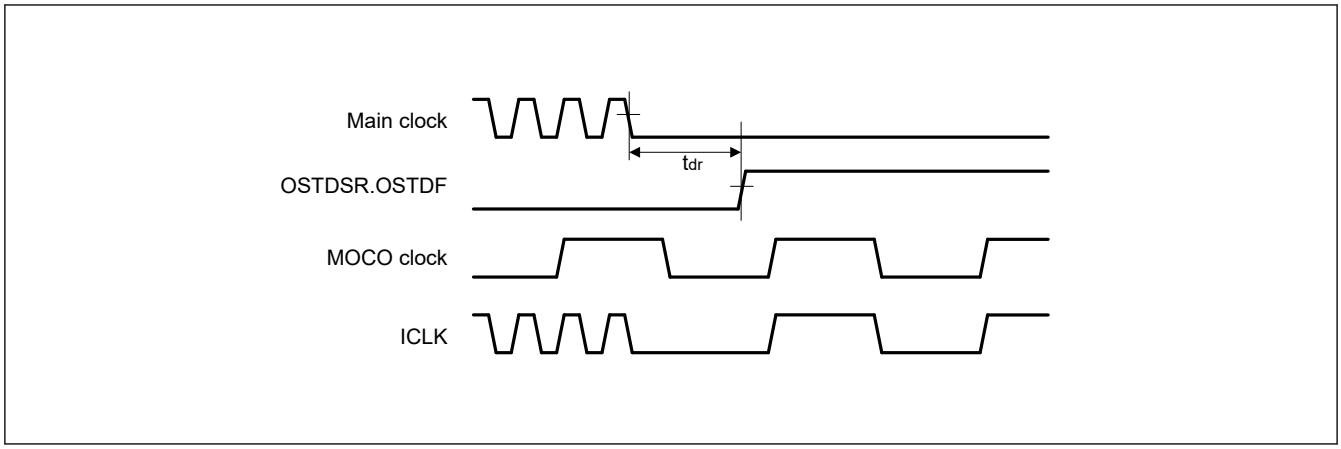


Figure 2.54 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.40 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b.	V_{POR}	2.5	2.6	2.7	V	Figure 2.55
		DPSBYCR.DEEPCUT[1:0] = 11b.		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.56
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.57
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.58
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.5	—	ms	Figure 2.55
	LVD0 reset time		t_{LVD0}	—	0.51	—		Figure 2.56
	LVD1 reset time		t_{LVD1}	—	0.38	—		Figure 2.57
	LVD2 reset time		t_{LVD2}	—	0.38	—		Figure 2.58
Minimum VCC down time*1			t_{VOFF}	200	—	—	μs	Figure 2.55, Figure 2.56
Response delay			t_{det}	—	—	200	μs	Figure 2.56 to Figure 2.58
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	μs	Figure 2.57, Figure 2.58
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for POR and LVD.

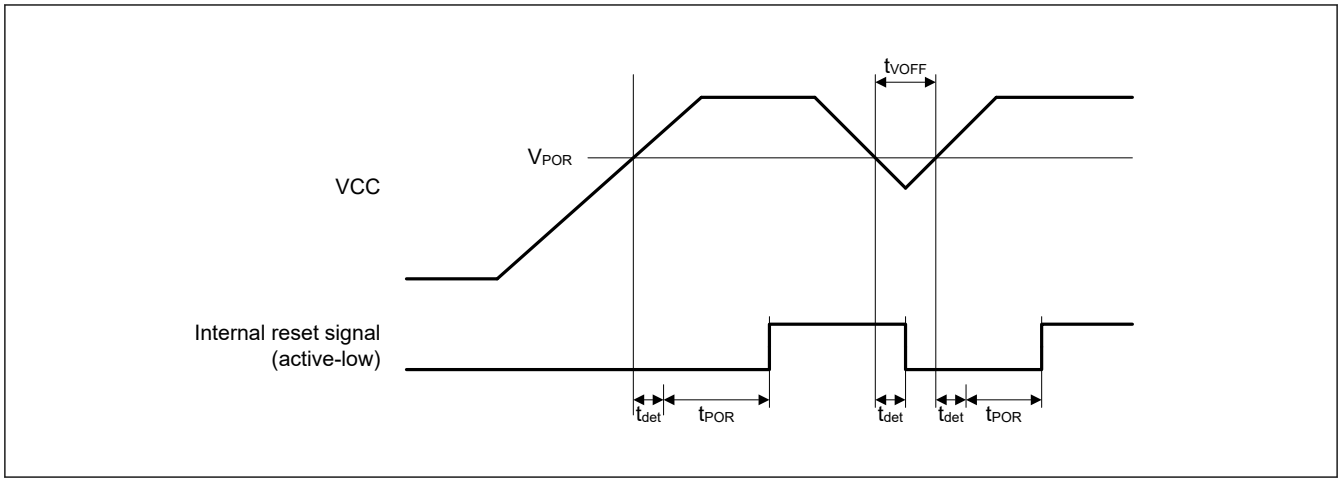


Figure 2.55 Power-on reset timing

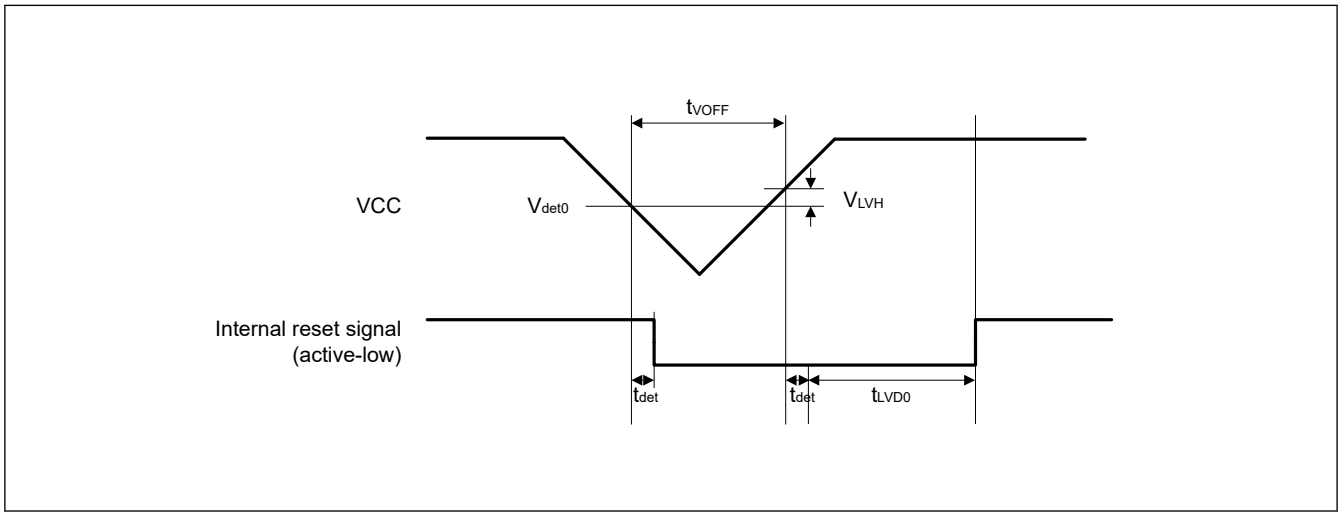


Figure 2.56 Voltage detection circuit timing (V_{det0})

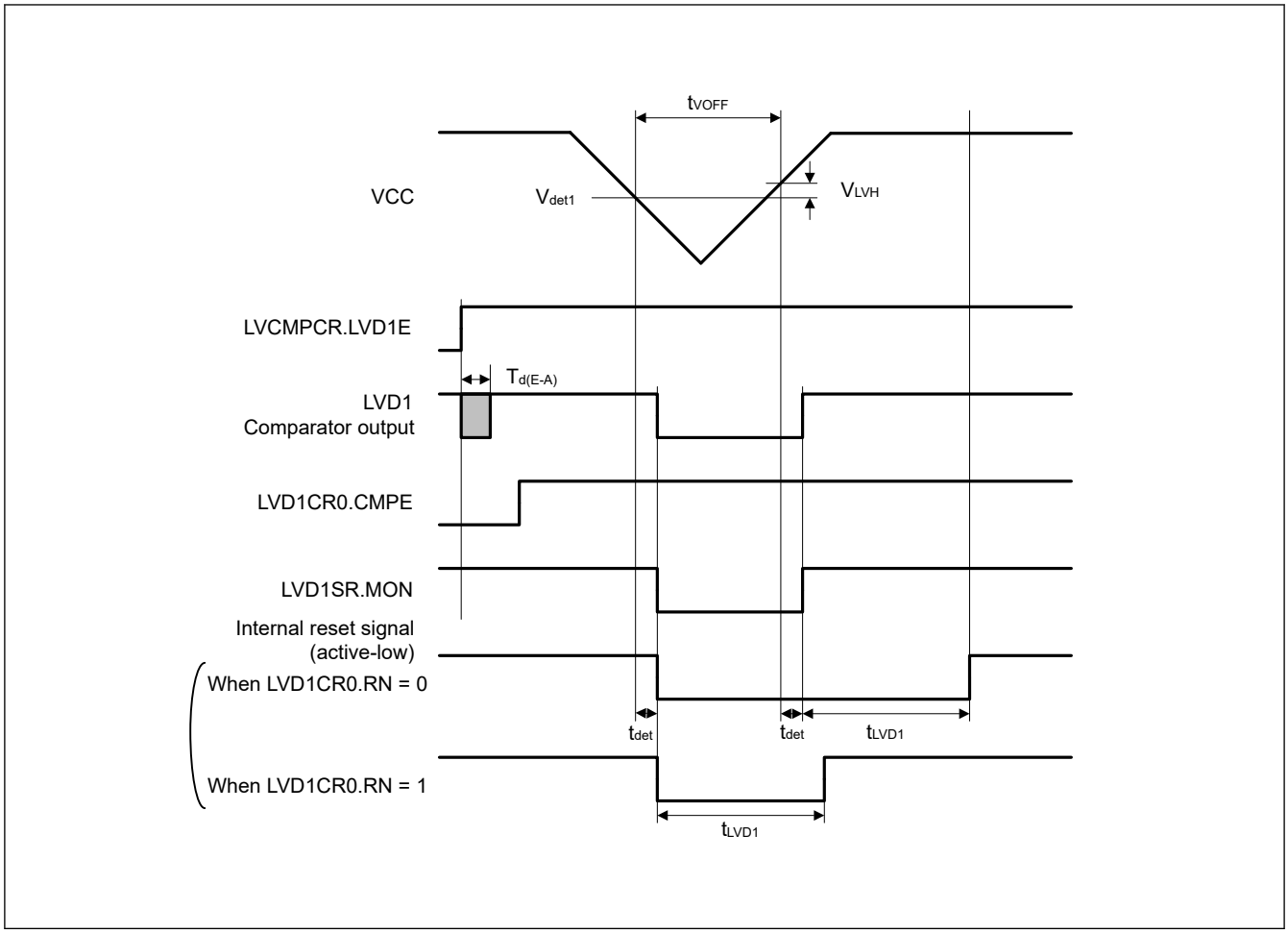


Figure 2.57 Voltage detection circuit timing (V_{det1})

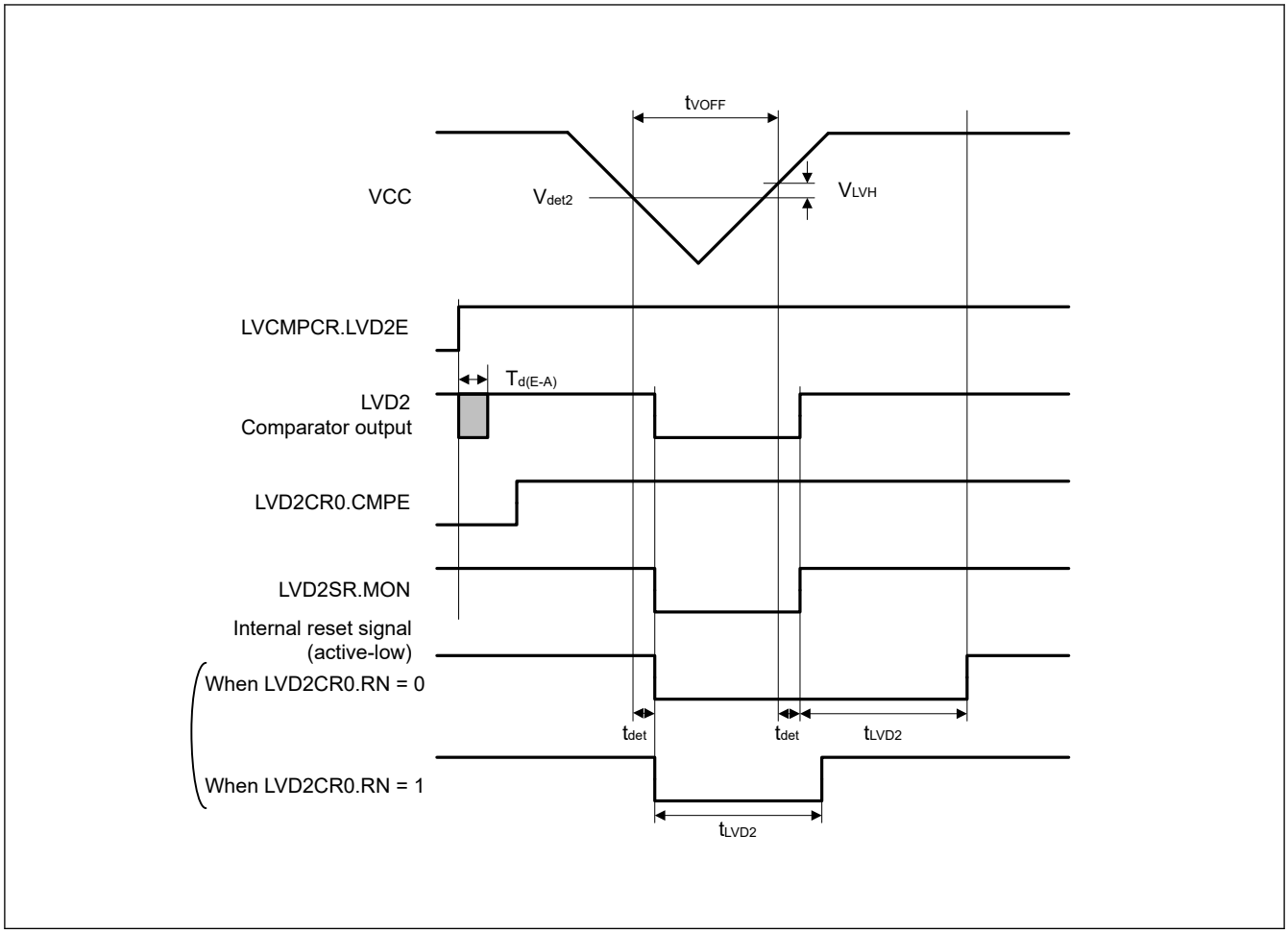


Figure 2.58 Voltage detection circuit timing (V_{det2})

2.9 ACMPHS Characteristics

Table 2.41 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	V_{REF}	0	—	AVCC0	V	
Input voltage range	V_I	0	—	AVCC0	V	
Output delay*1	t_d	—	50	100	ns	$V_I = V_{REF} \pm 100$ mV
Internal reference voltage	V_{ref}	1.13	1.18	1.23	V	

Note 1. This value is the internal propagation delay.

2.10 PGA Characteristics

Table 2.42 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	—	0	V
	AIN0 (G = 2.000)	0.05 × AVCC0	—	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	—	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	—	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	—	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	—	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	—	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	—	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.04 × AVCC0	—	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	—	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	—	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	—	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	—	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	—	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	—	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	—	0.06 × AVCC0	V
Gain error	AIN0 (G = 2.000)	-1.0	—	1.0	%
	AIN1 (G = 2.500)	-1.0	—	1.0	%
	AIN2 (G = 2.667)	-1.0	—	1.0	%
	AIN3 (G = 2.857)	-1.0	—	1.0	%
	AIN4 (G = 3.077)	-1.0	—	1.0	%
	AIN5 (G = 3.333)	-1.5	—	1.5	%
	AIN6 (G = 3.636)	-1.5	—	1.5	%
	AIN7 (G = 4.000)	-1.5	—	1.5	%
	AIN8 (G = 4.444)	-2.0	—	2.0	%
	AIN9 (G = 5.000)	-2.0	—	2.0	%
	AIN10 (G = 5.714)	-2.0	—	2.0	%
	AIN11 (G = 6.667)	-2.0	—	2.0	%
	AIN12 (G = 8.000)	-2.0	—	2.0	%
	AIN13 (G = 10.000)	-2.0	—	2.0	%
	AIN14 (G = 13.333)	-2.0	—	2.0	%
Offset error	Voff	-8	—	8	mV

Table 2.43 PGA characteristics in pseudo-differential mode (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	—	0.3	V
Pseudo-differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	—	0.5	V
	G = 2.333		-0.4	—	0.4	V
	G = 4.000		-0.2	—	0.2	V
	G = 5.667		-0.15	—	0.15	V

Table 2.43 PGA characteristics in pseudo-differential mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	-1.0	—	1.0	%
	G = 2.333		-1.0	—	1.0	%
	G = 4.000		-1.0	—	1.0	%
	G = 5.667		-1.0	—	1.0	%

2.11 Flash Memory Characteristics

2.11.1 Code Flash Memory Characteristics

Table 2.44 Code flash memory characteristics

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time N_{PEC} ≤ 100 times	128-byte	t_{P128}	—	0.75	13.2	—	0.34	6.0	ms	
	8-KB	t_{P8K}	—	49	176	—	22	80	ms	
	32-KB	t_{P32K}	—	194	704	—	88	320	ms	
Programming time N_{PEC} > 100 times	128-byte	t_{P128}	—	0.91	15.8	—	0.41	7.2	ms	
	8-KB	t_{P8K}	—	60	212	—	27	96	ms	
	32-KB	t_{P32K}	—	234	848	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8-KB	t_{E8K}	—	78	216	—	43	120	ms	
	32-KB	t_{E32K}	—	283	864	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8-KB	t_{E8K}	—	94	260	—	52	144	ms	
	32-KB	t_{E32K}	—	341	1040	—	189	576	ms	
Reprogramming/erasure cycle*4		N_{PEC}	10000*1	—	—	10000*1	—	—	Times	
Suspend delay during programming		t_{SPD}	—	—	264	—	—	120	µs	
Programming resume time		t_{PRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	—	—	216	—	—	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	—	—	1.7	—	—	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	—	—	1.7	—	—	1.7	ms	
First erasing resume time during erasure in suspend priority mode*5		t_{REST1}	—	—	1.7	—	—	1.7	ms	
Second erasing resume time during erasure in suspend priority mode		t_{REST2}	—	—	144	—	—	80	µs	
Erasing resume time during erasure in erasure priority mode		t_{REET}	—	—	144	—	—	80	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*2		t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
			30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

Note 4. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3V and room temperature.

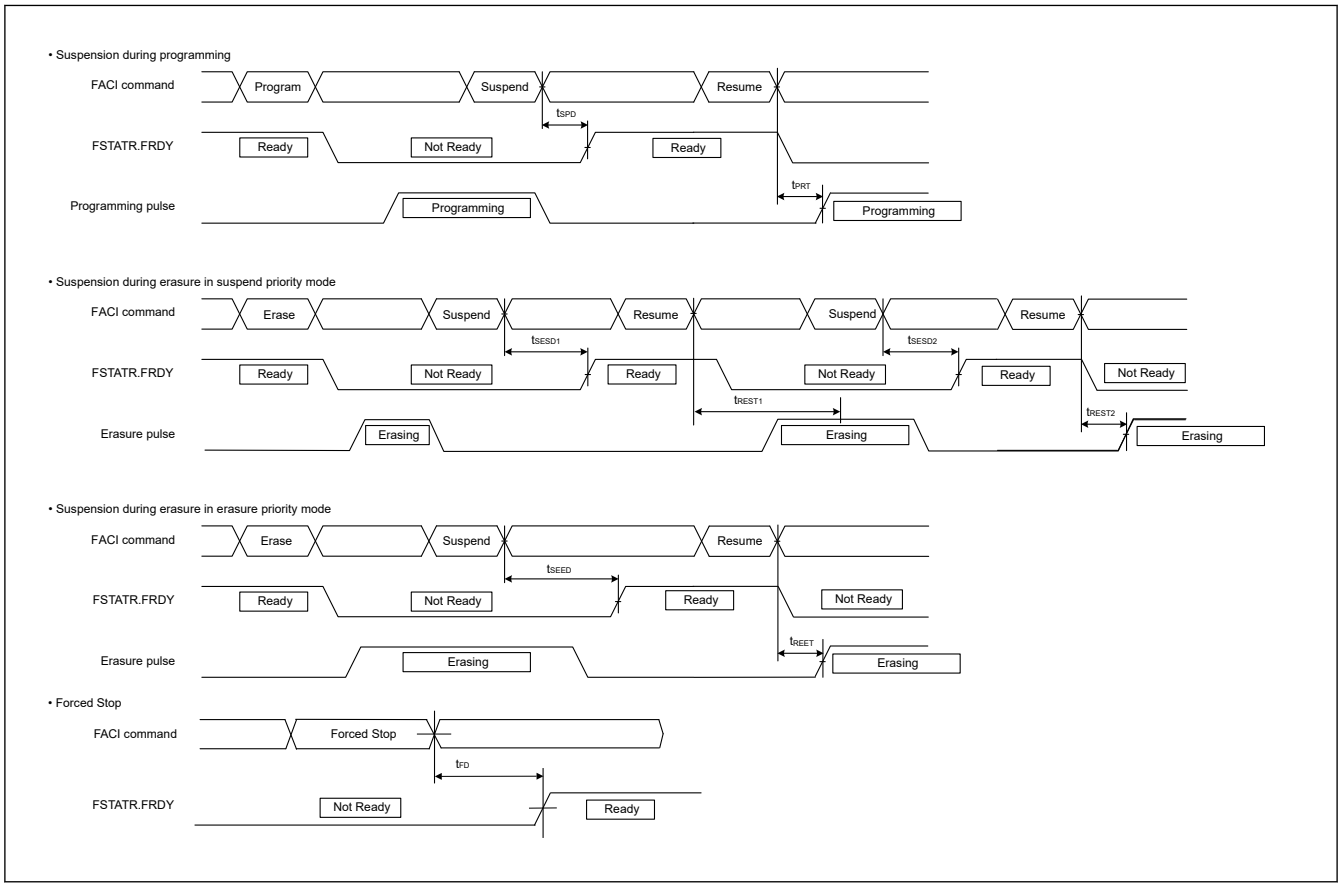


Figure 2.59 Suspension and forced stop timing for flash memory programming and erasure

2.11.2 Data Flash Memory Characteristics

Table 2.45 Data flash memory characteristics (1 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Programming time	4-byte	t_{DP4}	—	0.36	3.8	—	0.16	1.7	ms	
	8-byte	t_{DP8}	—	0.38	4.0	—	0.17	1.8		
	16-byte	t_{DP16}	—	0.42	4.5	—	0.19	2.0		
Erasure time	64-byte	t_{DE64}	—	3.1	18	—	1.7	10	ms	
	128-byte	t_{DE128}	—	4.7	27	—	2.6	15		
	256-byte	t_{DE256}	—	8.9	50	—	4.9	28		
Blank check time	4-byte	t_{DBC4}	—	—	84	—	—	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000*2	—	—	125000*2	—	—	—	

Table 2.45 Data flash memory characteristics (2 of 2)

Conditions: Program or erase: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
			Min	Typ*6	Max	Min	Typ*6	Max		
Suspend delay during programming	4-byte	t_{DSPD}	—	—	264	—	—	120	µs	
	8-byte		—	—	264	—	—	120		
	16-byte		—	—	264	—	—	120		
Programming resume time		t_{DPRT}	—	—	110	—	—	50	µs	
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	—	—	216	—	—	120	µs	
	128-byte		—	—	216	—	—	120		
	256-byte		—	—	216	—	—	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	—	—	300	—	—	300	µs	
	128-byte		—	—	390	—	—	390		
	256-byte		—	—	570	—	—	570		
First erasing resume time during erasure in suspend priority mode*5		t_{DREST1}	—	—	300	—	—	300	µs	
Second erasing resume time during erasure in suspend priority mode First erasing resume time during erasure in suspend priority mode		t_{DREST2}	—	—	126	—	—	70	µs	
Erasing resume time during erasure in erasure priority mode		t_{DREET}	—	—	126	—	—	70	µs	
Forced stop command		t_{FD}	—	—	32	—	—	20	µs	
Data hold time*3		t_{DRP}	10*3 *4	—	—	10*3 *4	—	—	Year	
			30*3 *4	—	—	30*3 *4	—	—		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. Overwriting is prohibited.
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.
Note 5. Time for resumption includes time for reapplying the erasing pulse (up to one full pulse) that was cut off at the time of suspension.
Note 6. The reference value at VCC = 3.3 V and room temperature.

2.11.3 Option Setting Memory Characteristics

Table 2.46 Option setting memory characteristics (1 of 2)

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Programming time N_{OPC} ≤ 100 times	t_{OP}	—	83	309	—	45	162	ms	
Programming time N_{OPC} > 100 times	t_{OP}	—	100	371	—	55	195	ms	
Reprogramming cycle	N_{OPC}	20000*1	—	—	20000*1	—	—	Times	

Table 2.46 Option setting memory characteristics (2 of 2)

Conditions: Program: FCLK = 4 to 50 MHz
Read: FCLK ≤ 50 MHz

Parameter	Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit	Test conditions
		Min	Typ*4	Max	Min	Typ*4	Max		
Data hold time*2	t_{DRP}	10*2 *3	—	—	10*2 *3	—	—	Years	
		30*2 *3	—	—	30*2 *3	—	—		Ta = +85°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.

2.12 Serial Wire Debug (SWD)

Table 2.47 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	—	—	ns	Figure 2.60
SWCLK clock high pulse width	t_{SWCKH}	15	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	8	—	—	ns	Figure 2.61
SWDIO hold time	t_{SWDH}	8	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	28	ns	

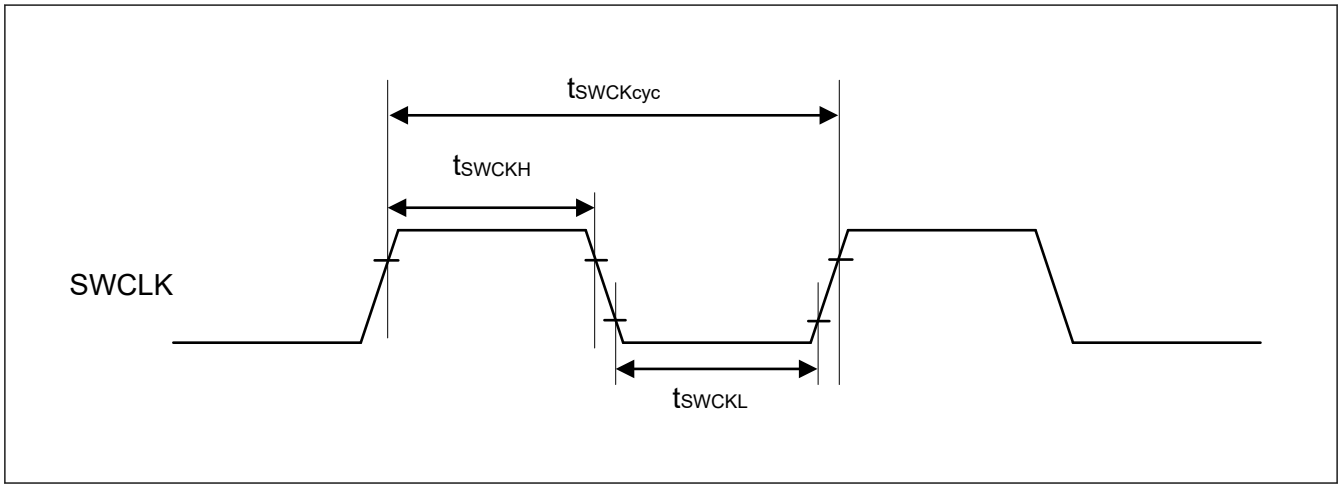


Figure 2.60 SWD SWCLK timing

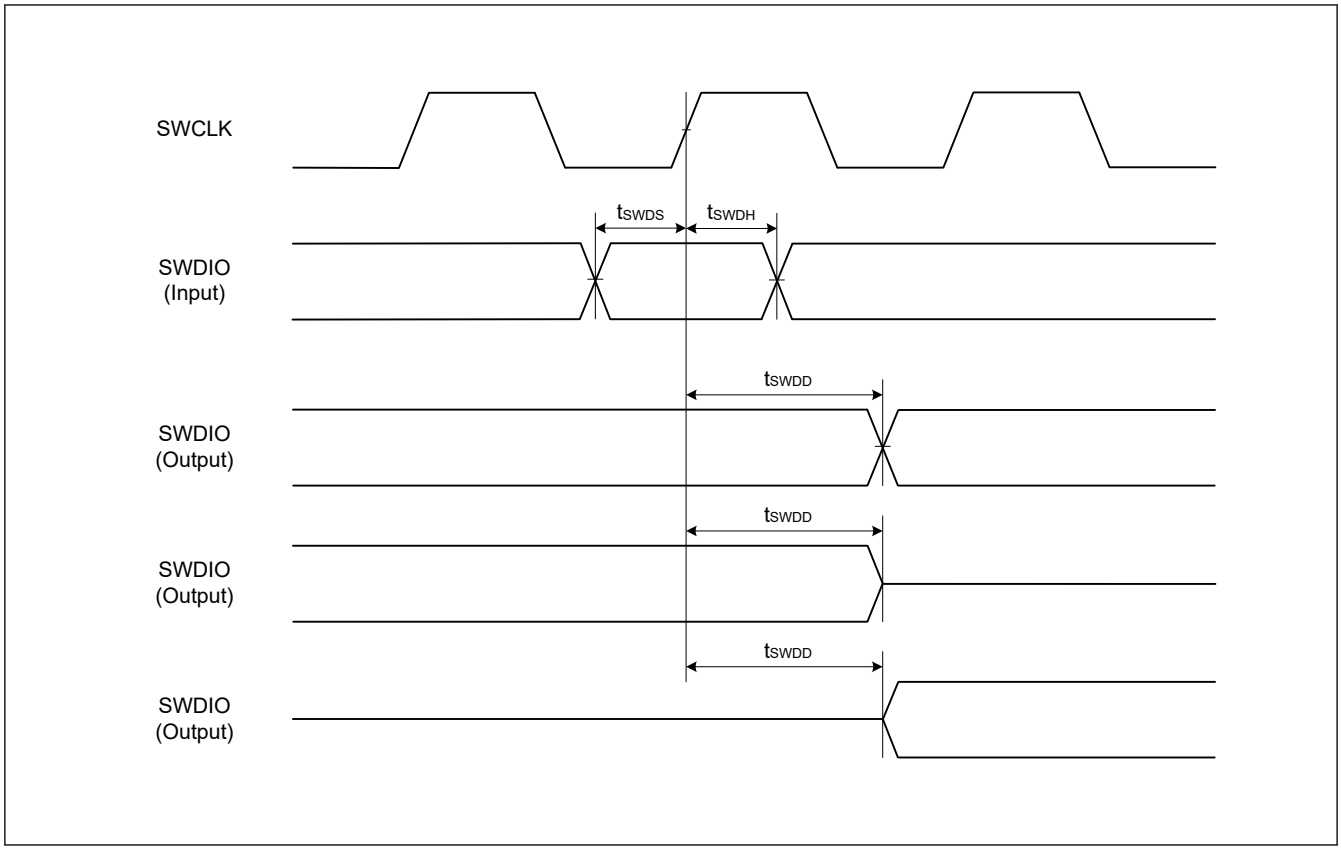


Figure 2.61 SWD input/output timing

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode	Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
					IOKEEP = 0	IOKEEP = 1*1
Mode	MD	Pull-up	Keep-O	Keep	Hi-Z	Keep
IRQ	IRQx	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	IRQx-DS	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
AGT	AGTIOn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
	AGTIOn (n = 1)	Hi-Z	Keep-O*2	Keep*3	Hi-Z	Keep
SCI	RXD0	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
I3C	I3C_SCL/I3C_SDA SCLn/SDAn	Hi-Z	Keep-O*2	Keep	Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	[CLKOUT selected] CLKOUT output	Keep	Hi-Z	Keep
DAC	DAn	Hi-Z	[DAn output (DAOE = 1)] D/A output retained	Keep	Hi-Z	Keep
ACMPHS	VCOUT	Hi-Z	VCOUT output	Keep	Hi-Z	Keep
Others	—	Hi-Z	Keep-O	Keep	Hi-Z	Keep

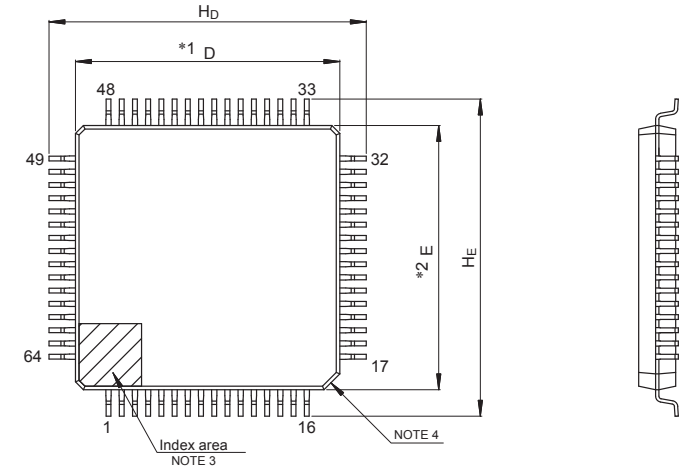
Note: H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.
Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



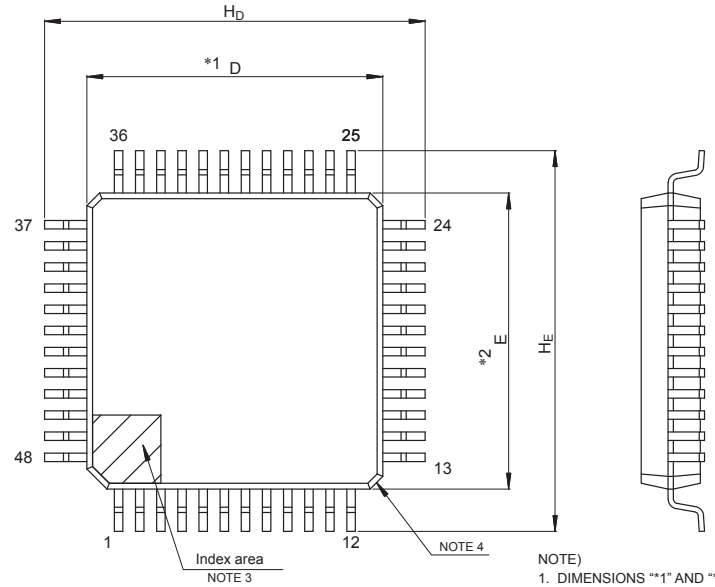
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

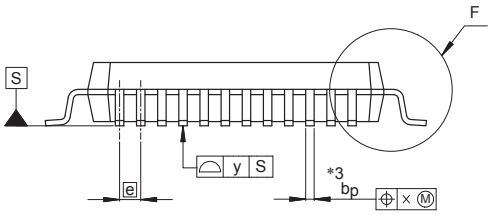
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

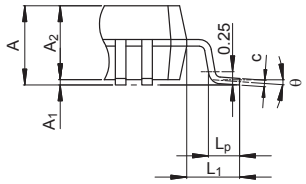
Figure A2.1 LQFP 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2

Unit: mm







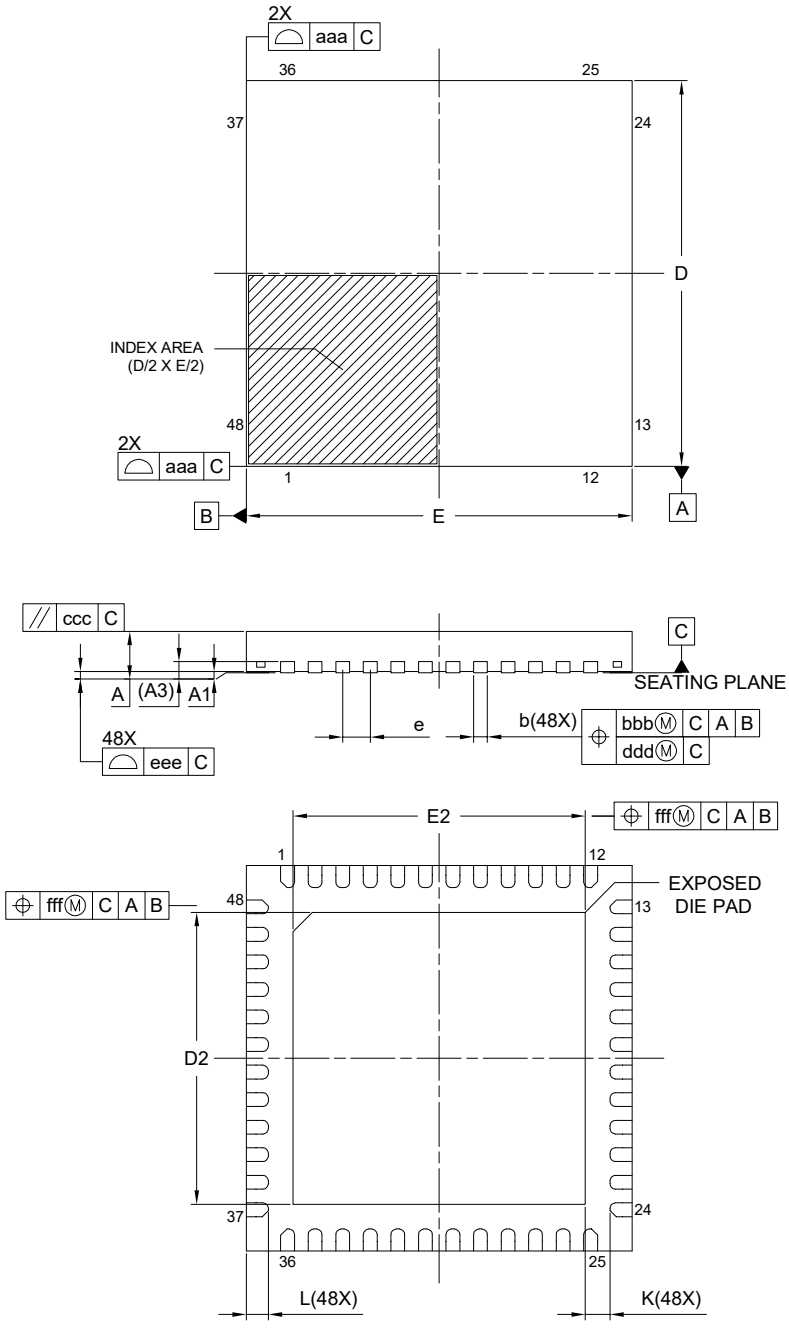
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure A2.2 LQFP 48-pin

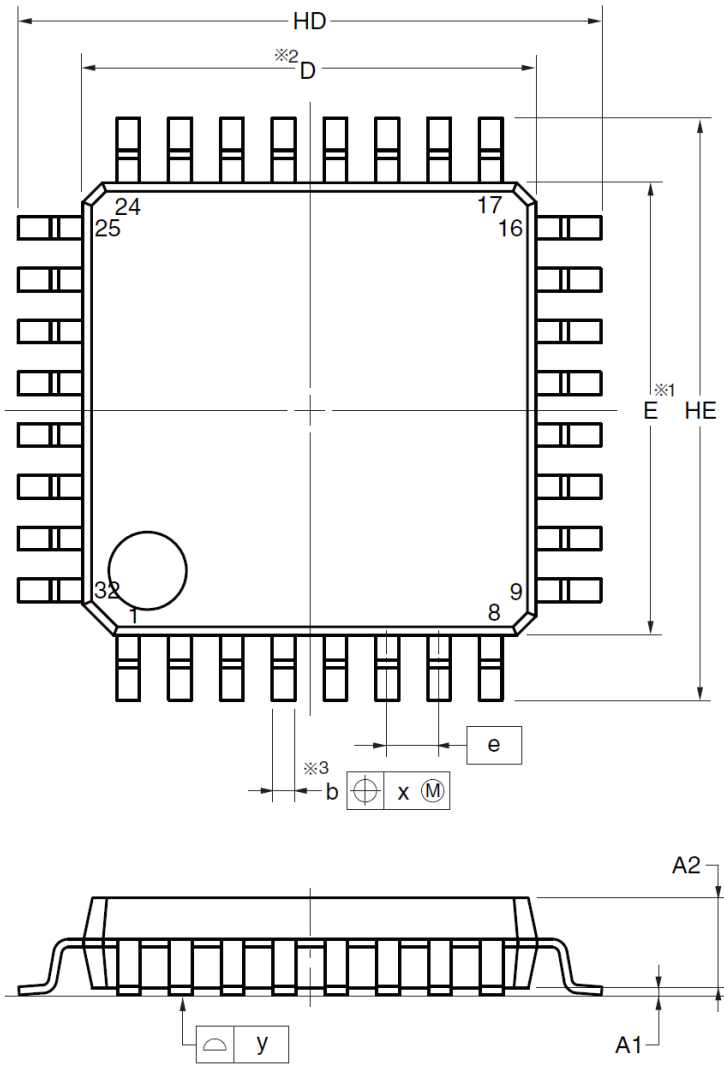
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

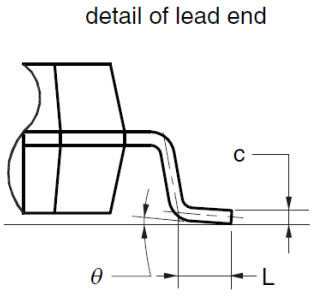


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure A2.3 QFN 48-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2





(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

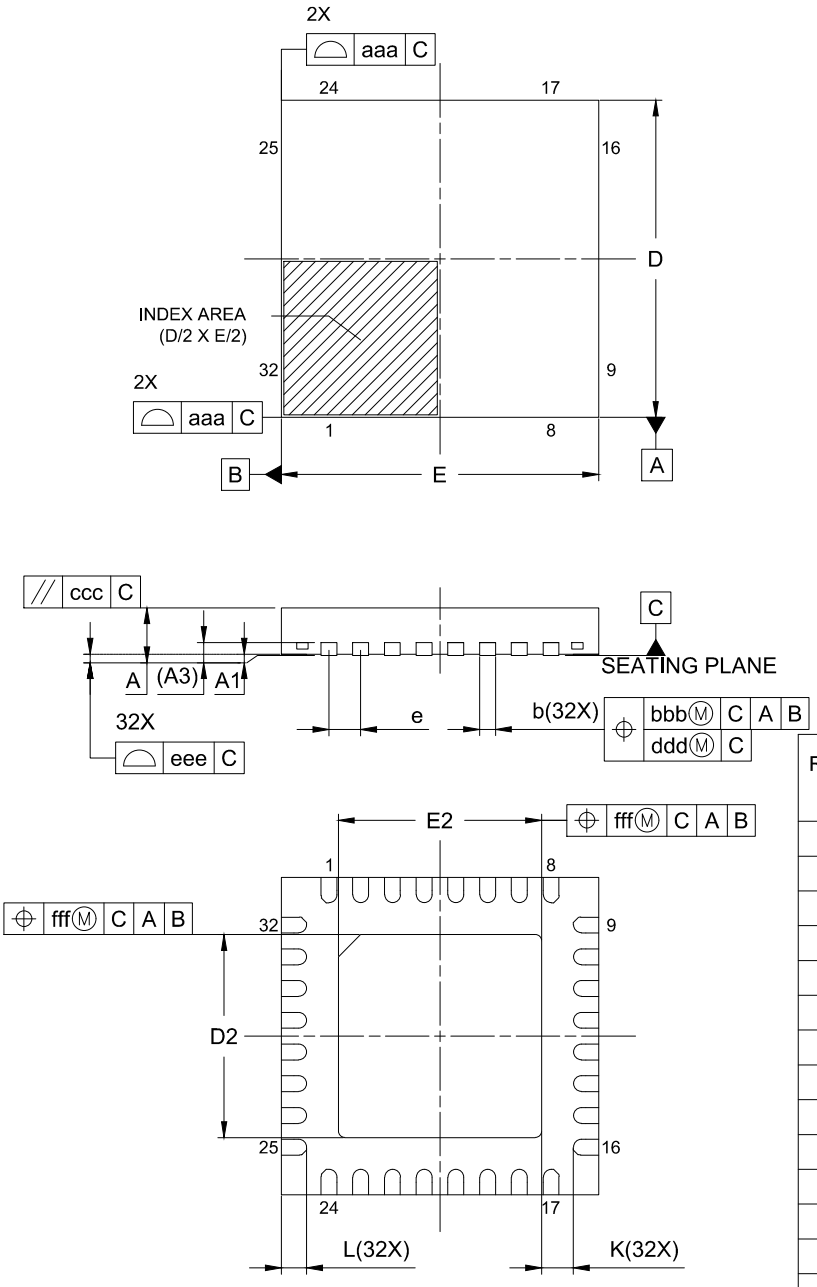
NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

Figure A2.4 LQFP 32-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure A2.5 QFN 32-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 2)

Name	Description	Base address
RMPU	Renesas Memory Protection Unit	0x4000_0000
TZF	TrustZone Filter	0x4000_0E00
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DMAC0	Direct memory access controller 0	0x4000_5000
DMAC1	Direct memory access controller 1	0x4000_5040
DMAC2	Direct memory access controller 2	0x4000_5080
DMAC3	Direct memory access controller 3	0x4000_50C0
DMAC4	Direct memory access controller 4	0x4000_5100
DMAC5	Direct memory access controller 5	0x4000_5140
DMAC6	Direct memory access controller 6	0x4000_5180
DMAC7	Direct memory access controller 7	0x4000_51C0
DMA	DMAC Module Activation	0x4000_5200
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
CACHE	CACHE	0x4000_7000
CPSCU	CPU System Security Control Unit	0x4000_8000
DBG	Debug Function	0x400_1B000
FCACHE	Flash Cache	0x400_1C100
SYSC	System Control	0x4001_E000
TFU	Trigonometric Function Unit	0x4002_1000
PORT0	Port 0 Control Registers	0x4008_0000
PORT1	Port 1 Control Registers	0x4008_0020
PORT2	Port 2 Control Registers	0x4008_0040
PORT3	Port 3 Control Registers	0x4008_0060
PORT4	Port 4 Control Registers	0x4008_0080
PORT5	Port 5 Control Registers	0x4008_00A0
PORT8	Port 8 Control Registers	0x4008_0100
PFS	Pmn Pin Function Control Register	0x4008_0800
ELC	Event Link Controller	0x4008_2000
IWDT	Independent Watchdog Timer	0x4008_3200
WDT	Watchdog Timer	0x4008_3400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4008_3600
MSTP	Module Stop Control A, B, C, D	0x4008_4000
POEG	Port Output Enable Module for GPT	0x4008_A000

Table A3.1 Peripheral base address (2 of 2)

Name	Description	Base address
CANFD	CANFD Module Control	0x400B_0000
PSCU	Peripheral Security Control Unit	0x400E_0000
AGT0	Low Power Asynchronous General purpose Timer 0	0x400E_8000
AGT1	Low Power Asynchronous General purpose Timer 1	0x400E_8100
TSN	Temperature Sensor	0x400F_3000
ACMPHS0	High-Speed Analog Comparator 0	0x400F_4000
ACMPHS1	High-Speed Analog Comparator 1	0x400F_4100
ACMPHS2	High-Speed Analog Comparator 2	0x400F_4200
CRC	CRC Calculator	0x4010_8000
DOC	Data Operation Circuit	0x4010_9000
SCI0	Serial Communication Interface 0	0x4011_8000
SCI9	Serial Communication Interface 9	0x4011_8900
SPI0	Serial Peripheral Interface 0	0x4011_A000
SPI1	Serial Peripheral Interface 1	0x4011_A100
I3C	I3C Bus Interface	0x4011_F000
CANFD ECC	CANFD ECC	0x4012_F000
GPT16E0	General PWM 16-Bit Timer 0 (16-bit Enhanced High Resolution)	0x4016_9000
GPT16E1	General PWM 16-Bit Timer 1 (16-bit Enhanced High Resolution)	0x4016_9100
GPT16E2	General PWM 16-Bit Timer 2 (16-bit Enhanced High Resolution)	0x4016_9200
GPT16E3	General PWM 16-Bit Timer 3 (16-bit Enhanced High Resolution)	0x4016_9300
GPT16E4	General PWM 16-Bit Timer 4 (16-bit Enhanced High Resolution)	0x4016_9400
GPT16E5	General PWM 16-Bit Timer 5 (16-bit Enhanced High Resolution)	0x4016_9500
GPT_OPS	Output Phase Switching Controller	0x4016_9A00
ADC120	12bit A/D Converter 0	0x4017_0000
DAC12	12-bit D/A converter	0x4017_1000
FLAD	Data Flash	0x407F_C000
FACI	Flash Application Command Interface	0x407F_E000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table A3.2 Access cycles (1 of 3)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
RMPU, TZF, SRAM, BUS, DMACn, DMA, DTC, ICU	0x4000_0000	0x4000_6FFF	4	3	4	3	ICLK	Renesas Memory Protection Unit, TrustZone Filter, SRAM Control, BUS Control, Direct memory access controller n, DMAC Module Activation, DTC Control Register, Interrupt Controller
CACHE	0x4000_7000	0x4000_7FFF	3	5	3	5	ICLK	CACHE
CPSCU, DBG, FCACHE	0x4000_8000	0x4001_CFFF	4	3	4	3	ICLK	CPU System Security Control Unit, Debug Function, Flash Cache
SYSC	0x4001_E000	0x4001_E3FF	5	4	5	4	ICLK	System Control
SYSC	0x4001_E400	0x4001_E5FF	9	8	5 to 8	5 to 8	PCLKB	System Control
TFU	0x4002_1000	0x4002_1FFF	4	3	4	3	ICLK	Trigonometric Function Unit
PORTn, PFS	0x4008_0000	0x4008_0FFF	5	4	2 to 5	2 to 4	PCLKB	Port n Control Registers, Pmn Pin Function Control Register
ELC, IWDT, WDT, CAC	0x4008_2000	0x4008_3FFF	5	4	3 to 5	2 to 4	PCLKB	Event Link Controller, Realtime Clock, Independent Watchdog Timer, Watchdog Timer, Clock Frequency Accuracy Measurement Circuit
MSTP	0x4008_4000	0x4008_4FFF	5	4	2 to 5	2 to 4	PCLKB	Module Stop Control
POEG	0x4008_A000	0x4008_AFFF	5	4	3 to 5	2 to 4	PCLKB	Port Output Enable Module for GPT
CANFD	0x400B_0000	0x400C_FFFF	5	4	2 to 5	2 to 4	PCLKB	CANFD Module
PSCU	0x400E_0000	0x400E_0FFF	5	4	2 to 5	2 to 4	PCLKB	Peripheral Security Control Unit
AGTn	0x400E_8000	0x400E_8FFF	7	4	5 to 7	2 to 4	PCLKB	Low Power Asynchronous General purpose Timer n
TSN	0x400F_3000	0x400F_3FFF	5	4	2 to 5	2 to 4	PCLKB	Temperature Sensor
ACMPHSn	0x400F_4000	0x400F_4FFF	4	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator
CRC, DOC	0x4010_8000	0x4010_9FFF	5	4	2 to 5	2 to 4	PCLKA	CRC Calculator, Data Operation Circuit
SCIn	0x4011_8000	0x4011_8FFF	5*2	4*2	2 to 5*2	2 to 4*2	PCLKA	Serial Communication Interface n
SPIn	0x4011_A000	0x4011_AFFF	5*3	4*3	2 to 5*3	2 to 4*3	PCLKA	Serial Peripheral Interface n
I3C	0x4011_F000	0x4011_FFFF	5	4	2 to 4	2 to 4	PCLKA	I3C Bus Interface
CANFD ECC	0x4012_F000	0x4012_FFFF	5	4	2 to 4	2 to 4	PCLKA	CANFD ECC Module

Table A3.2 Access cycles (2 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
GPT16En, GPT_OPS	0x4016_9000	0x4016_9FFF	7	4	4 to 7	2 to 4	PCLKA	General PWM 16-Bit Timer n, Output Phase Switching Controller
ADC12n, DAC12	0x4017_0000	0x4017_2FFF	5	4	2 to 5	2 to 4	PCLKA	12bit A/D Converter n, 12-bit D/A converter

Table A3.2 Access cycles (3 of 3)

Peripherals	Address		Number of access cycles					
			ICLK = FCLK		ICLK > FCLK*1		Cycle Unit	Related function
	From	To	Read	Write	Read	Write		
FLAD, FACI	0x407F_C000	0x407F_EFFF	5	4	2 to 5	2 to 4	FCLK	Data Flash, Flash Application Command Interface

Note 1. If the number of PCLK or FCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table A3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table A3.2.

Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table A3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table A3.2.

Revision History

Revision 1.10 — May 23, 2023

Initial release

Revision 1.20 — Oct 31, 2024

1. Overview:
- Updated Figure 1.2 Part numbering scheme.
- Updated Figure 1.5 Pin assignment for QFN 48-pin.

2. Electrical Characteristics:
- Updated Note 3 in Table 2.6 I/O V_{OH}, V_{OL}, and other characteristics.

Revision 1.30 — September 12, 2025

2. Electrical Characteristics:
- Updated Table 2.34 CANFD interface timing.
- Updated Figure 2.52 CANFD interface condition.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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