Datasheet

RA8T2 Group
Renesas Microcontrollers

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High-performance 1 GHz Arm® Cortex®-M85 core, 250 MHz Arm® Cortex®-M33 core, up to 1 MB code MRAM, and 2 MB SRAM with ECC. High-integration with Layer 3 Ethernet Switch Module, USB 2.0 Full-Speed, CANFD, SDHI, I3C, Octal SPI, Decryption on-the-fly, and advanced analog. Integrated Renesas Security IP with cryptography accelerators, key management support, tamper detection and power analysis resistance in concert with Arm® TrustZone for integrated Secure element functionality.

Features

Arm® Cortex®-M85 Core

- Armv8.1-M architecture profile
- Armv8-M Security Extension
- Maximum operating frequency: 1 GHz
- Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by CPUCLK0 or MOCO divided by 8
- CoreSight™ ETM-M85

Arm® Cortex®-M33 core

- Armv8-M architecture profile
- Armv8-M Security Extension
- Maximum operating frequency: 250 MHz
- Memory Protection Unit (Arm MPU)
  - Protected Memory System Architecture (PMSAv8)
  - Secure MPU (MPU_S): 8 regions
  - Non-secure MPU (MPU_NS): 8 regions
- SysTick timer
  - Embeds two Systick timers: Secure and Non-secure instance
  - Driven by CPUCLK1 or MOCO divided by 8
- CoreSight™ ETM-M33

Memory

- Up to 1-MB MRAM
- 2 MB SRAM including 256 KB of CM85 TCM and 128 KB of CM33 TCM
- Up to 8-MB Flash for SiP product

Connectivity

- Serial Communications Interface (SCI) × 10, up to 60 Mbps
- I^2C bus interface (IIC) × 3
- I^3C bus interface (I3C)
- Serial Peripheral Interface (SPI) × 2, up to 166 Mbps
- Octal Serial Peripheral Interface (OSPI) × 2, up to 333 MB/s
- USB 2.0 Full-Speed Module (USBFS)
- CAN with Flexible Data-rate (CANFD) × 2
- Layer 3 Ethernet Switch Module (ESWM)
  - 2 × Gigabit Ethernet
- EtherCAT slave controller × 2
- SD/MMC Host Interface (SDHI) × 2
- Delta-Sigma Modulator Interface (DSMIF) × 2

Analog

- 16-bit A/D Converter (ADC16H) × 2, up to 23 channels
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 4
- Temperature Sensor (TSN)

Timers

- General PWM Timer 32-bit (GPT32) with High Resolution × 4
  - 52 ps resolution in 300 MHz
- General PWM Timer 32-bit (GPT32) × 10
- Low Power Asynchronous General Purpose Timer (AGT) × 2
- Ultra-Low-Power Timer (ULPT) × 2

Security and Encryption

- Renesas Security IP (RSIP-E50D)
- Arm® TrustZone®
- Privileged control
- Device lifecycle management
- Secure boot
  - Immutable first stage boot loader in OTP
- Decryption on-the-fly (DOTF)
- Pin function
  - Up to three tamper-resistant pins
  - Secure pin multiplexing
- HUK zeroization

System and Power Management

- Low power modes
- Battery backup function (VBATT)
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- Data Transfer Controller (DTC) × 2
- DMA Controller (DMAC) × 16
- Power-on reset
- Programable Voltage Detection (PVD) with voltage settings
- Watchdog Timer (WDT) × 2
- Independent Watchdog Timer (IWDT)

Multiple Clock Sources

- Main clock oscillator (MOSC) (8 to 48 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20/32/48 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- PLL1/PLL2
- Clock out support

General-Purpose I/O Ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

Operating Voltage

- Standard product
  - VCC/VCC2: 1.62 to 3.63 V
- SiP product
  - VCC/VCC2: 1.62 to 3.63 V/1.70 to 2.00 V

Operating Junction Temperature and Packages

- Tj = 0 °C to +95 °C
  - 289-pin BGA (12 mm × 12 mm, 0.65 mm pitch)
  - 224-pin BGA (11 mm × 11 mm, 0.65 mm pitch)
  - 303-pin BGA (15 mm × 15 mm, 0.8 mm pitch)
- Tj = -40 °C to +105 °C
  - 289-pin BGA (12 mm × 12 mm, 0.65 mm pitch)
  - 224-pin BGA (11 mm × 11 mm, 0.65 mm pitch)
  - 303-pin BGA (15 mm × 15 mm, 0.8 mm pitch)
- Tj = -40 °C to +125 °C
  - 289-pin BGA (12 mm × 12 mm, 0.65 mm pitch)
  - 224-pin BGA (11 mm × 11 mm, 0.65 mm pitch)
  - 176-pin HLQFP (24 mm × 24 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm® Cortex®-M85 core running up to 1 GHz and Arm® Cortex®-M33 core running up to 250 MHz with the following features:

- Up to 1 MB MRAM
- 2 MB SRAM (256 KB of CM85 TCM RAM, 128 KB CM33 TCM RAM, 1664 KB of user SRAM)
- Octal Serial Peripheral Interface (OSPI)
- Layer 3 Ethernet Switch Module (ESWM), USBFS, SD/MMC Host Interface
- Analog peripherals
- Security and safety features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm® Cortex®-M85 core	• Maximum operating frequency: up to 1 GHz • Arm® Cortex®-M85 core – Revision: (r1p1-00rel0) – ARMv8.1-M architecture profile – Armv8-M Security Extension – Floating Point Unit (FPU) compliant with the ANSI/IEEE Std 754-2008 Scalar half, single, and double-precision floating-point operation – M-profile Vector Extension (MVE) Integer, half-precision, and single-precision floating-point MVE (MVE-F) • Arm® Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure instance (SysTick_S) and Non-secure instance (SysTick_NS) – Driven by CPUCLK0 or MOCO divided by 8 • CoreSight™ ETM-M85
Arm® Cortex®-M33 core	• Maximum operating frequency: up to 250 MHz • Arm® Cortex®-M33 core – Revision: (r0p4-00rel2) – ARMv8-M architecture profile – Armv8-M Security Extension – Armv8-DSP Extension – Floating Point Unit (FPU) compliant with the ANSI/IEEE Std 754-2008 single-precision floating-point operation • Arm® Memory Protection Unit (Arm MPU) – Protected Memory System Architecture (PMSAv8) – Secure MPU (MPU_S): 8 regions – Non-secure MPU (MPU_NS): 8 regions • SysTick timer – Embeds two Systick timers: Secure instance (SysTick_S) and Non-secure instance (SysTick_NS) – Driven by CPUCLK1 or MOCO divided by 8 • CoreSight™ ETM-M33

Table 1.2 Memory (1 of 2)

Feature	Functional description
Code MRAM	Maximum 1 MB of code MRAM.
Flash memory	System in package (SiP) maximum 8 MB serial flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.

Table 1.2 Memory (2 of 2)

Feature	Functional description
SRAM	On-chip high-speed SRAM with Error Correction Code (ECC).
OTP	On-chip OTP contains First Stage Bootloader (FSBL) General purpose 96-byte OTP

Table 1.3 System

Feature	Functional description
Operating modes	Three operating modes: ● Single-chip mode ● JTAG boot mode ● SCI/USB boot mode
Resets	This MCU provides the following 21 types of reset.
Programmable Voltage Detection (PVD)	The Programmable Voltage Detection (PVD) module monitors the voltage level input to the VCC pin. The detection level can be selected by register settings. The PVD module consists of five separate voltage level detectors (PVD0, PVD1, PVD2, PVD4, PVD5). These PVDs measure the voltage level input to the VCC pin. PVD registers allow your application to configure detection of VCC changes at various voltage thresholds.
Clocks	● Main clock oscillator (MOSC) ● Sub-clock oscillator (SOSC) ● High-speed on-chip oscillator (HOCO) ● Middle-speed on-chip oscillator (MOCO) ● Low-speed on-chip oscillator (LOCO) ● PLL1/PLL2 ● Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), DMA Controller (DMAC) module and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, power gating control, selecting operating power control modes in normal operation, and transitioning to low power modes and processor low power modes.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup register, tamper detection and VBATT_R voltage drop detection and switch between VCC and VBATT.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR_S and PRCR_NS).
Memory Protection Unit (MPU)	All bus masters have Memory Protection Units (MPUs).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access (1 of 2)

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.5 Direct memory access (2 of 2)

Feature	Functional description
DMA Controller (DMAC)	The 8-channel direct memory access controller (DMAC) that can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

Table 1.6 External bus interface

Feature	Functional description
External buses	● CS area (ECBI): Connected to the external devices (external memory interface) ● SDRAM area (ECBI): Connected to the SDRAM (external memory interface) ● OSPI0 area (OSPI0BI): Connected to the OSPI0 (external device interface) ● OSPI1 area (OSPI1BI): Connected to the OSPI1 (external device interface)

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with GPT32 × 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
PWM Delay Generation Circuit (PDG)	The PWM Delay Generation circuit (PDG) has 4 channels delay circuits that can connect to the GPT. The PDG can control the rise and fall edge timing with which the PWM output for the GPT320 through the GPT323.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Ultra-Low-Power Timer (ULPT)	The Ultra-Low-Power Timer (ULPT) is a 32-bit timer which can be used for outputting pulses or counting external events. This 32-bit timer consists of reload registers and a down-counter. The reload registers and the down-counter are allocated to the same address and can be accessed through the ULPTCNT register.
Realtime Clock (RTC)	The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) has a 14-bit down-counter, which resets the MCU by a reset output when the down-counter underflows. Alternatively, generation of an interrupt request when the counter underflows can be selected. This enables detection of a program runaway taking the refresh interval into account. The IWDT has two start modes: auto start mode, in which counting automatically starts after release from the reset state, and register start mode, in which counting is started by refreshing (writing to a specific register).

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 10 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface ● Manchester interface ● Simple LIN interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. All channels have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. The maximum rate supported on this MCU. Refer to the electrical characteristics for the actual rate.
I^2C Bus interface (IIC)	The I^2C Bus interface (IIC) has 3 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
I3C Bus Interface (I3C)	The I3C Bus Interface (I3C) has 1 channel. The I3C module conform with and provide a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions and a subset of the MIPI I3C.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices. The maximum rate supported on this MCU. Refer to the electrical characteristics for the actual rate.
Control Area Network with Flexible Data-Rate Module (CANFD)	The CAN with Flexible Data-Rate (CANFD) module can handle classical CAN frames and CANFD frames complied with ISO 11898-1 standard. The module supports 4 transmit buffers per channel and 16 receive buffers per channel.
USB 2.0 Full-Speed module (USBFS)	The USB 2.0 Full-Speed module (USBFS) can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system.
Octal Serial Peripheral Interface (OSPI)	The Octal Serial Peripheral Interface (OSPI) is a memory controller that supports Expanded Serial Peripheral Interface (xSPI) (JEDEC Standard JESD251, JESD251-1 and JESD252). The OSPI supports 1-bit, 2-bit, 4-bit and 8-bit protocols. JESD251 specifies two interface profiles where profile 1.0 is Octal SPI and profile 2.0 is HyperBus™ (HyperRAM™ and HyperFlash™). OSPI supports QSPI protocol.
SD/MMC Host Interface (SDHI)	The Secure Digital (SD) Card and Multi Media Card (MMC) Host Interface provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1- and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes.
Layer 3 Ethernet Switch Module (ESWM)	The Layer 3 Ethernet Switch Module (ESWM) consists of two channels of Gigabit Ethernet controller, an Ethernet switch with high level routing capability, and multi-protocol interface support. The Gigabit Ethernet controller conforms to the definition of the Ethernet MAC (Media Access Control) layer in the IEEE 802.3 standard. This can transmit and receive Ethernet (IEEE 802.3) frames by connecting with an external physical-layer LSI chip (PHY-LSI) which complies with the standard. The Ethernet switch allows autonomous frame routing within a same network interface protocol, or between different network interfaces protocols or optimized gateway applications.
EtherCAT Slave Controller (ESC)	The EtherCAT slave controller (ESC) uses an EtherCAT Slave Controller IP Core (ESC IP Core) made by Beckhoff Automation GmbH, Germany. The ESC handles the EtherCAT communication as an interface between the EtherCAT fieldbus and the slave application.

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Delta-Sigma Modulator Interface (DSMIF)	DSMIF has three channels that are connectable with external delta-sigma modulators. DSMIF can be connected with up to three external delta-sigma modulators. Each DSMIF can filter and convert 1-bit digital data streams that were delta-sigma modulated at a high sampling rate into 16-bit digital data at a lower sampling rate.

Table 1.9 Analog

Feature	Functional description
16-bit A/D Converter (ADC16H)	A 16-bit A/D Converter is provided. Up to 23 analog input channels are selectable. Temperature sensor output, and internal reference voltage and VBATT 1/6 voltage monitor are selectable for conversion.
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) is provided.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC16H for conversion and can be further used by the end application. The sensor outputs an abnormal temperature detection signal to the reset control circuit and can be used to prevent the malfunction due to abnormal temperature.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) can be used to compare an analog input voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the analog input voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output or internal reference voltage) and an external source. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 32-bits data. When a selected condition applies, 32-bit data is compared and an interrupt can be generated.

Table 1.11 Security

Feature	Functional description
Security function	• ARMv8-M TrustZone security • Privileged control • Device lifecycle management • Authentication Level (AL) • Key injection • Secure pin multiplexing • HUK zeroization • VBATT backup registers zeroization • Secure boot • Secure factory programming
Renesas Secure IP (RSIP-E50D)	• Symmetric cryptography: AES and ChaCha20-Poly1305 • Asymmetric cryptography: RSA and ECC • Message digest computation: HASH, HMAC • 128-bit true random number generation circuit • 256-bit Hardware Unique Key (HUK) • 128-bit unique ID • OEM boot loader version • Key data for the decryption on-the-fly (DOTF) • SPA/DPA Protections
Decryption on-the-fly (DOTF)	Decryption on-the-fly (DOTF) decrypts the encrypted content stored in the external memory in real-time.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

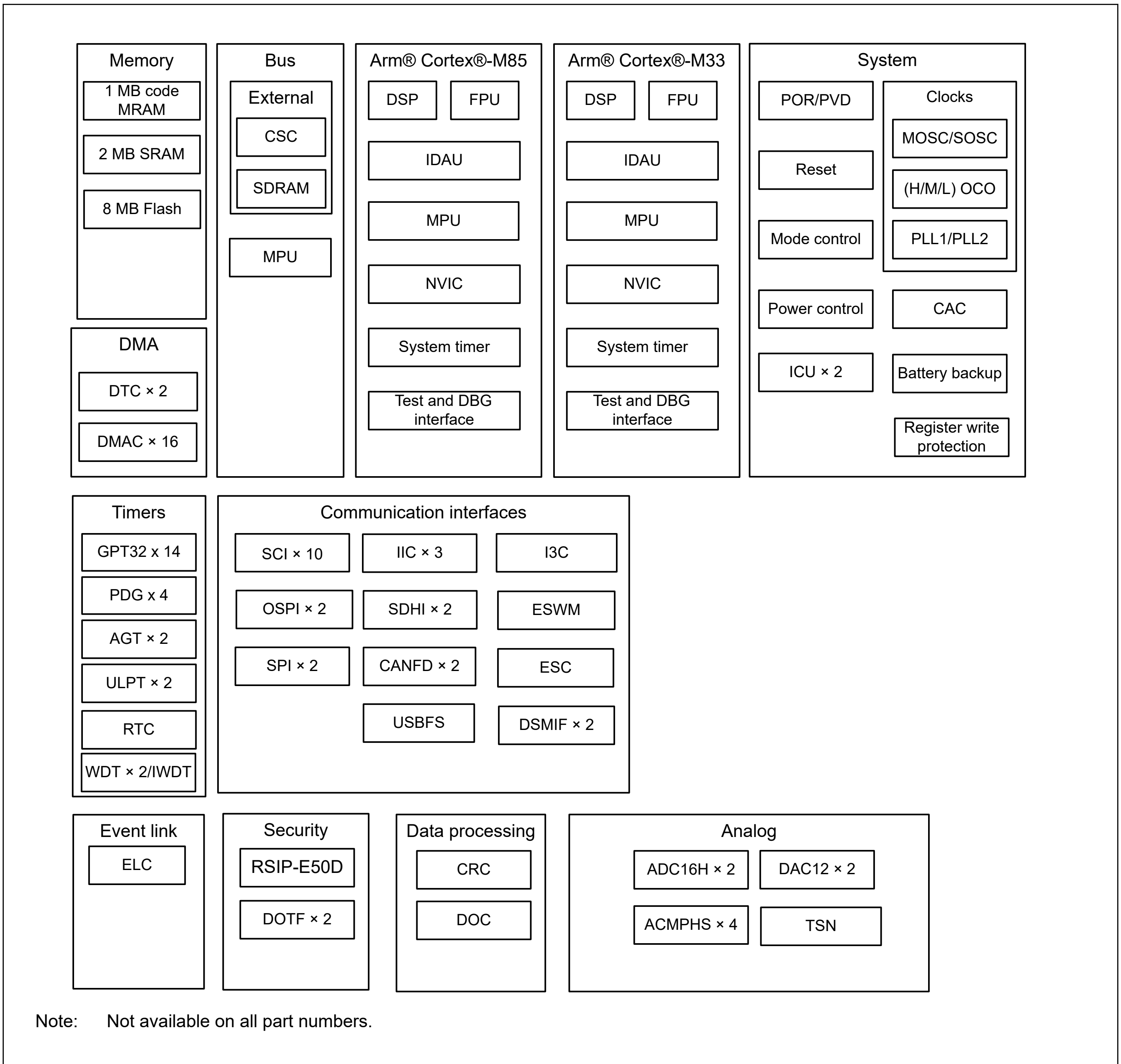


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

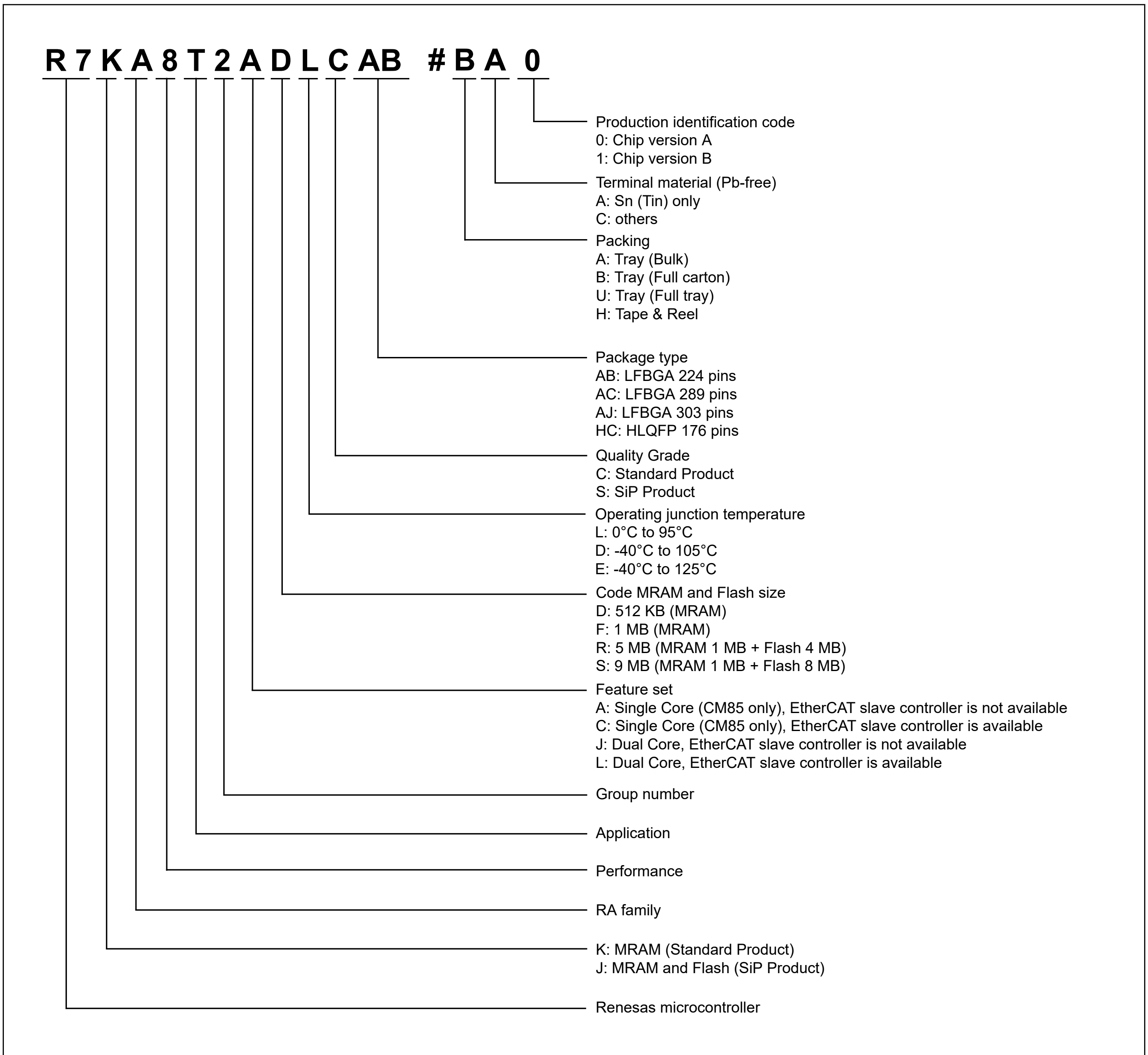


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Product group	CPU	EtherCAT	Package code	Code MRAM	SRAM	Flash	Operating junction temperature
R7KA8T2ADDCAB	B	single	—	PLBG0224JA-A	512 KB	2 MB	—	-40 to 105 °C
R7KA8T2ADECAB	C			PLBG0224JA-A				-40 to 125 °C
R7KA8T2ADECHC				PLQP0176KK-A				
R7KA8T2AFLCAB	A			PLBG0224JA-A	1 MB			0 to 95 °C
R7KA8T2AFLCAC				PLBG0289JA-A				
R7KA8T2AFDCAB	B			PLBG0224JA-A				-40 to 105 °C
R7KA8T2AFDCAC				PLBG0289JA-A				
R7KA8T2AFECAB	C			PLBG0224JA-A				-40 to 125 °C
R7KA8T2AFECAC				PLBG0289JA-A				
R7KA8T2AFECHC				PLQP0176KK-A				
R7KA8T2CDDCAB	B		✔	PLBG0224JA-A	512 KB			-40 to 105 °C
R7KA8T2CDECAB	C			PLBG0224JA-A				-40 to 125 °C
R7KA8T2CDECHC				PLQP0176KK-A				
R7KA8T2CFLCAB	A			PLBG0224JA-A	1 MB			0 to 95 °C
R7KA8T2CFLCAC				PLBG0289JA-A				
R7KA8T2CFDCAB	B			PLBG0224JA-A				-40 to 105 °C
R7KA8T2CFDCAC				PLBG0289JA-A				
R7KA8T2CFECAB	C			PLBG0224JA-A				-40 to 125 °C
R7KA8T2CFECAC				PLBG0289JA-A				
R7KA8T2CFECHC				PLQP0176KK-A				
R7KA8T2JFLCAB	A	dual	—	PLBG0224JA-A	1 MB			0 to 95 °C
R7KA8T2JFLCAC				PLBG0289JA-A				
R7KA8T2JFDCAB	B			PLBG0224JA-A				-40 to 105 °C
R7KA8T2JFDCAC				PLBG0289JA-A				
R7KA8T2JFECAB	C			PLBG0224JA-A				-40 to 125 °C
R7KA8T2JFECAC				PLBG0289JA-A				
R7KA8T2JFECHC				PLQP0176KK-A				
R7KA8T2LFLCAB	A		✔	PLBG0224JA-A				0 to 95 °C
R7KA8T2LFLCAC				PLBG0289JA-A				
R7KA8T2LFDCAB	B			PLBG0224JA-A				-40 to 105 °C
R7KA8T2LFDCAC				PLBG0289JA-A				
R7KA8T2LFECAB	C			PLBG0224JA-A				-40 to 125 °C
R7KA8T2LFECAC				PLBG0289JA-A				
R7KA8T2LFECHC				PLQP0176KK-A				
R7JA8T2JRLSAJ	A	dual	—	PLBG0303GA-A	1 MB		4 MB	0 to 95 °C
R7JA8T2JSLSAJ							8 MB	
R7JA8T2JRDSAJ	B						4 MB	-40 to 105 °C
R7JA8T2JSDSAJ							8 MB	
R7JA8T2LRLSAJ	A		✔				4 MB	0 to 95 °C
R7JA8T2LSLSAJ							8 MB	
R7JA8T2LRDSAJ	B						4 MB	-40 to 105 °C
R7JA8T2LSDSAJ							8 MB	

1.4 Function Comparison

Table 1.13 Function Comparison (1 of 2)

Parts number		R7KA 8T2Ax xCAC	R7KA 8T2Cx xCAC	R7KA 8T2Jx xCAC	R7KA 8T2Lx xCAC	R7KA 8T2Ax xCAB	R7KA 8T2Cx xCAB	R7KA 8T2Jx xCAB	R7KA 8T2Lx xCAB	R7KA 8T2Ax xCHC	R7KA 8T2Cx xCHC	R7KA 8T2Jx xCHC	R7KA 8T2Lx xCHC	R7JA 8T2Jx xSAJ	R7JA 8T2Lx xSAJ
Pin count		289				224				176				303	
Package		BGA								HLQFP				BGA	
I/O Port		215				156				137				202	
Code MRAM		1 MB, 512 KB												1 MB	
CPU0 TCM		256 KB													
CPU1 TCM		No		128 KB		No		128 KB		No		128 KB			
CPU0 I/D Caches		32 KB													
CPU1 C/S Caches		No		32 KB		No		32 KB		No		32 KB			
SRAM		1792 KB		1664 KB		1792 KB		1664 KB		1792 KB		1664 KB			
Flash		No												8 MB, 4 MB	
DMA	DTC	1		2		1		2		1		2			
	DMAC	8		16		8		16		8		16			
BUS	External bus	32-bit bus				16-bit bus									
	SDRAM	32-bit bus				16-bit bus									
System	CPU0 clock	1 GHz (max.)								600 MHz (max.)				1 GHz (max.)	
	CPU1 clock	No		250 MHz (max.)		No		250 MHz (max.)		No		200 MHz (max.)		250 MHz (max.)	
	CPUs clock sources	MOSC, SOSC, HOCO, MOCO, PLL1P													
	CAC	Yes													
	WDT	1		2		1		2		1		2			
	IWDT	Yes													
	Backup register	128 B													
Communication	SCI	10				9								10	
	IIC	3													
	I3C	Yes													
	SPI	2													
	CANFD	2													
	USBFS	Yes													
	OSPI	2				1								2[*2]	
	SDHI/ MMC	2													
	ESWM	MII, RMII, GMII, RGMII				MII, RMII, RGMII				MII, RMII				MII, RMII, GMII, RGMII	
	ESC	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
	DSMIF	2													

Table 1.13 Function Comparison (2 of 2)

<table>
<tr><th colspan="2">Parts number</th><th>R7KA 8T2Ax xCAC</th><th>R7KA 8T2Cx xCAC</th><th>R7KA 8T2Jx xCAC</th><th>R7KA 8T2Lx xCAC</th><th>R7KA 8T2Ax xCAB</th><th>R7KA 8T2Cx xCAB</th><th>R7KA 8T2Jx xCAB</th><th>R7KA 8T2Lx xCAB</th><th>R7KA 8T2Ax xCHC</th><th>R7KA 8T2Cx xCHC</th><th>R7KA 8T2Jx xCHC</th><th>R7KA 8T2Lx xCHC</th><th>R7JA 8T2Jx xSAJ</th><th>R7JA 8T2Lx xSAJ</th></tr>
<tr><td rowspan="5">Timers</td><td>GPT32 *1</td><td colspan="14">14</td></tr>
<tr><td>PDG</td><td colspan="14">4</td></tr>
<tr><td>AGT*1</td><td colspan="14">2</td></tr>
<tr><td>ULPT*1</td><td colspan="14">2</td></tr>
<tr><td>RTC</td><td colspan="14">Yes</td></tr>
<tr><td rowspan="4">Analog</td><td>ADC16H</td><td colspan="4">Unit 0: 15, Unit 1: 15</td><td colspan="8">Unit 0: 7, Unit 1: 5</td><td colspan="2">Unit 0: 15, Unit 1: 15</td></tr>
<tr><td>DAC12</td><td colspan="14">2</td></tr>
<tr><td>ACMPHS</td><td colspan="14">4</td></tr>
<tr><td>TSN</td><td colspan="14">Yes</td></tr>
<tr><td rowspan="2">Data processing</td><td>CRC</td><td colspan="14">Yes</td></tr>
<tr><td>DOC</td><td colspan="14">Yes</td></tr>
<tr><td>Event control</td><td>ELC</td><td colspan="14">Yes</td></tr>
<tr><td colspan="2">Security</td><td colspan="14">RSIP-E50D, Decryption on-the-fly, Secure Debug, OTP, TrustZone, and Lifecycle management</td></tr>
</table>

Note: The product name differs depending on the supported memory size. See section 1.3. Part Numbering.
Note: The maximum frequency varies by product group.
Note 1. Available pins depend on the Pin count, about details see section 1.7. Pin Lists.
Note 2. OSPI1 is connected to the serial Flash in the SiP product.

1.5 Pin Functions

Table 1.14 Pin functions (1 of 8)

Function	Signal	I/O	Description
Power supply	VCC_01 to VCC_10, VCC2_11 to VCC2_15	Input	Power supply pin. Connect it to the system power supply. Connect this pin to the same numbered VSS_01 to VSS_15 by a 0.1-μF capacitor. The capacitor should be placed close to the pin. In the SiP product, connect VCC2_11 to VCC2_15 to the 1.8V system power supply.
	VCC2_16 to VCC2_19	Input	Dedicated power supply pin for the SiP product. Connect it to the 1.8V system power supply. Connect this pin to the same numbered VSS_16 to VSS_19 by a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCC_DCDC	Input	Switching regulator power supply pin.
	VLO	I/O	Switching regulator pin.
	VCL0 to VCL11	Input	Connect this pin to the same numbered VSS0 to VSS11 pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VBATT	Input	Battery Backup power pin.
	VSS_01 to VSS_15, VSS0 to VSS11, VSS_DCDC	Input	Ground pin. Connect it to the system power supply (0 V).
	VSS_16 to VSS_19, VSS	Input	Dedicated ground pin for the SiP product. Connect it to the system power supply (0 V).
	Vpp	Input	Power supply pin for serial Flash programming operation. See the ISSI serial Flash IS25WX064 datasheet for the details. If not used, the Vpp pin can be floated. Note that the deep power down current varies depending on the power supply status of the Vpp pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EXCIN	Input	External sub-clock input
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
	PUP	Input	Connect to VCC2 through a resistor.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip emulator	TMS	Input	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	Output clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWO	Output	Serial wire trace output pin
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin

Table 1.14 Pin functions (2 of 8)

Function	Signal	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQn	Input	Maskable interrupt request pins
	IRQn-DS	Input	Maskable interrupt request pins that can also be used in Deep Software Standby mode
External bus interface	EBCLK	Output	Outputs the external bus clock for external devices
	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active-low
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low
	WRn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00, D15 to D08, D23 to D16 or D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode, active-low
	BCn	Output	Strobe signals indicating that either group of data bus pins (D07 to D00, D15 to D08, D23 to D16 or D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode, active-low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active-low
	CSn	Output	Select signals for CS areas, active-low
	A00 to A23	Output	Address bus
	D00 to D31	I/O	Data bus
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus
SDRAM interface	SDCLK	Output	Outputs the SDRAM-dedicated clock
	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active low
	RAS	Output	SDRAM low address strobe signal, active low
	CAS	Output	SDRAM column address strobe signal, active low
	WE	Output	SDRAM write enable signal, active low
	DQMn	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00, DQ15 to DQ08, DQ23 to DQ16 or DQ31 to DQ24
	A00 to A16	Output	Address bus
	DQ00 to DQ31	I/O	Data bus

Table 1.14 Pin functions (3 of 8)

Function	Signal	I/O	Description
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOCnA, GTIOCnB	I/O	Input capture, output compare, or PWM output pins
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
	GTCPPOn	Output	Toggle output synchronized with PWM period
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn	Input	External event input enable signals
	AGTIOn	I/O	External event input and pulse output pins
	AGTOn	Output	Pulse output pins
	AGTOAn	Output	Output compare match A output pins
	AGTOBn	Output	Output compare match B output pins
ULPT	ULPTEEn	Input	External count control input
	ULPTEVIn	Input	External event input
	ULPTEEn-DS	Input	External count control input that can also be used in Deep Software Standby mode 1
	ULPTEVIn-DS	Input	External event input that can also be used in Deep Software Standby mode 1
	ULPTOn	Output	Pulse output
	ULPTOAn	Output	Output compare match A output
	ULPTOBn	Output	Output compare match B output
	ULPTOn-DS	Output	Pulse output that can also be used in Deep Software Standby mode 1
	ULPTOAn-DS	Output	Output compare match A output that can also be used in Deep Software Standby mode 1
	ULPTOBn-DS	Output	Output compare match B output that can also be used in Deep Software Standby mode 1
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCICn	Input	Time capture event input pins

Table 1.14 Pin functions (4 of 8)

Function	Signal	I/O	Description
SCI	SCKn	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	CTSn	Input	Input for the start of transmission.
	DEn	Output	Driver enable signal for RS-485
	SCLn	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn	I/O	Input/output pins for the clock
	SDAn	I/O	Input/output pins for data
I3C	I3C_SCL0	I/O	Input/output pins for the clock
	I3C_SDA0	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
CANFD	CRXn	Input	Receive data
	CTXn	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB_DP	I/O	D+ pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus.
	USB_DM	I/O	D- pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_OVRCURA-DS, USB_OVRCURB-DS	Input	Overcurrent pins for USBFS that can also be used in Deep Software Standby mode 1. Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode

Table 1.14 Pin functions (5 of 8)

Function	Signal	I/O	Description
OSPI	OM_n_SCLK	Output	Clock output (OCTACLK divided by 2)
	OM_n_SCLKN	Output	Inverted clock output (OCTACLK divided by 2)
	OM_n_CSn	Output	Chip select signal for an OctaFlash device, active-low
	OM_n_DQS	I/O	Read data strobe/write data mask signal
	OM_n_SIOn	I/O	Data input/output
	OM_n_RESET	Output	Reset signal for both slave devices, active-low
	OM_n_ECSINT1	Input	Error Correction Status and Interrupt for slave1
	OM_n_RSTO1	Input	Slave reset status for slave1
	OM_n_WP1	Output	Write Protect for slave1, active-low
SDHI/MMC	SDnCLK	Output	SD clock output pins
	SDnCMD	I/O	Command output pin and response input signal pins
	SDnDAT0 to SDnDAT7	I/O	SD and MMC data bus pins
	SDnCD	Input	SD card detection pins
	SDnWP	Input	SD write-protect signals

Table 1.14 Pin functions (6 of 8)

Function	Signal	I/O	Description
ESWM	ETn_GTX_CLK	Output	1000 Mb/s transmit clock
	ETn_TX_CLK	Input	100 Mb/s,10 Mb/s transmit clock
	ETn_RX_CLK	Input	Receive clock
	ETn_TX_EN	Output	Transmit enable
	ETn_TXD0 to ETn_TXD7	Output	Transmit data
	ETn_TX_ER	Output	Transmit coding error
	ETn_RX_DV	Input	Receive data valid
	ETn_RXD0 to ETn_RXD7	Input	Receive data
	ETn_RX_ER	Input	Receive error
	ETn_MDC	Output	Management data clock
	ETn_MDIO	I/O	Management data input/output
	RGMIIn_TXC	Output	Transmit clock
	RGMIIn_RXC	Input	Receive clock
	RGMIIn_TX_CTL	Output	Transmit control
	RGMIIn_TXD0 to RGMIIn_TXD3	Output	Transmit data
	RGMIIn_RX_CTL	Input	Receive control
	RGMIIn_RXD0 to RGMIIn_RXD3	Input	Receive data
	RMIIn_REF50CK	Input	Synchronous clock reference
	RMIIn_TX_EN	Output	Transmit enable
	RMIIn_TXD0 to RMIIn_TXD1	Output	Transmit data
	RMIIn_CRS_DV	Input	Carrier sense/Receive data valid
	RMIIn_RXD0 to RMIIn_RXD1	Input	Receive data
	RMIIn_RX_ER	Input	Receive error
	ETn_LINKSTA	Input	PHY Link Status
	ETn_INT	Input	PHY interrupt
	ETn_WOL	Output	Wake-on-LAN. This signal indicates that a Magic Packet was received.
	GPTP_CAPTUREn	Input	Media clock capture input
	GPTP_MATCHn	Output	Media clock recovery output
	GPTP_PPSn	Output	PPS signal
	GPTP_PTPOUT0 to GPTP_PTPOUT3	Output	PTP Pulse generator signal
	ET_TAS_STA0 to ET_TAS_STA3	Output	TAS status monitor
	ETHPHYCLK	Output	Clock output for PHY (Shared with ESC)

Table 1.14 Pin functions (7 of 8)

Function	Signal	I/O	Description
ESC	CATn_LINKSTA	Input	Link status inputs from the PHY-LSI
	CATn_RX_CLK	Input	Receive clocks
	CATn_RX_DV	Input	Receive data valid
	CATn_ERXD0 to CATn_ERXD3	Input	Receive data
	CATn_RX_ER	Input	Receive error
	CATn_TX_CLK	Input	Transmit clocks
	CATn_TX_EN	Output	Transmit enable
	CATn_ETXD0 to CATn_ETXD3	Output	Transmit data
	CAT0_MDC	Output	Management data clock
	CAT0_MDIO	I/O	Management data I/O
	ETHPHYCLK	Output	Clock output for PHY (Shared with ESWM)
	CATRESETOUT	Output	PHY reset signal
	CATLEDRUN	Output	RUN LED (green) output
	CATIRQ	Output	IRQ output
	CATLEDSTER	Output	Output for RUN LED part of STATE LED (bicolor) (turned off while ERR)
	CATLEDERR	Output	ERR LED (red) output
	CATLINKACT0, CATLINKACT1	Output	Link/Activity LED outputs
	CATSYNC0, CATSYNC1	Output	SYNC signal outputs
	CATLATCH0, CATLATCH1	input	LATCH signal inputs
	CATI2CCLK	Output	EEPROM I2C clock output
	CATI2CDATA	I/O	EEPROM I2C data
DSMIF	DSMnCLK0 to DSMnCLK2	I/O	Clock input/output pin
	DSMnDAT0 to DSMnDAT2	Input	Data input pin
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH	Input	Analog reference voltage supply pin for the ADC16H (unit 1) and D/A Converter. Connect this pin to AVCC0 when not using the ADC16H (unit 1) and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC16H and D/A Converter. Connect this pin to AVSS0 when not using the ADC16H (unit 1) and D/A Converter.
	VREFH0	Input	Analog reference voltage supply pin for the ADC16H (unit 0). Connect this pin to AVCC0 when not using the ADC16H (unit 0).
	VREFL0	Input	Analog reference ground pin for the ADC16H. Connect this pin to AVSS0 when not using the ADC16H (unit 0).

Table 1.14 Pin functions (8 of 8)

Function	Signal	I/O	Description
ADC16H	ANxxx	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRGm	Input	Input pins for the external trigger signals that start the A/D conversion, active-low.
	ADSTm	Output	AD conversion start
	ADmFLAG1	Output	AD conversion end
	ADSYNC	Output	Synchronization signal between units
DAC12	DAn	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin
	IVREFn	Input	Reference voltage input pins for comparator
	IVCMPn	Input	Analog voltage input pins for comparator
I/O ports	Pmn	I/O	General-purpose input/output pins (m: port number, n: pin number)
	P200	Input	General-purpose input pin

1.6 Pin Assignments

The following figures show the pin assignments from the top view.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	P609	P113	P115	P112	P302	P915	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P309	P906	P905	P907	P904	P207	A
B	P813	PA12	P114	PA11	P300	P303	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P311	P908	P909	P206	PD01	PD02	B
C	PA06	P613	PA13	P301	P200	P210/TMS/SWDIO	P208/TDI	P110	P308	P305	P307	P911	P312	PD04	PD03	PD05	PD06	C
D	PA04	P611	P610	PA14	RES	P211/TCK/SWCLK	P109	P108	P903	P304	P306	P912	PB04	PB07	PB05	PB03	PB01	D
E	PA15	P615	P614	P612	P914	P201/MD	P209/TDO	P111	P902	P310	P910	P913	PB02	PB06	PD07	PB00	P706	E
F	PA02	PA10	PA08	PA09	PC14	VCC_08	VSS_08	VSS3	VCL3	VSS_07	VCC_07	P700	P702	P406	P701	P707	P705	F
G	PA00	PA03	PA05	PA07	PC12	VCC_09	VSS_09	VSS4	VCL4	VSS_06	VCC_06	P405	P704	P703	PB14	PB12	PB11	G
H	P504	P503	P505	PA01	PC11	VCC_10	VSS_10	VSS7	VCL5	VSS5	VCC_04	VSS_04	P403	VCC_05	PB09	PB10	PB13	H
J	P506	P507	P508	P509	PC13	VCC2_11	VSS_11	VCL7	VCL6	VSS6	VCL2	VSS2	P404	PB08	VSS_05	VSS_03	VSS_02	J
K	PC15	P608	P510	PD00	PC07	VSS_12	VSS9	VCL9	VCL8	VSS8	VCL1	VSS1	P410	VCC_03	VCC_02	P213/XTAL	P212/EXTAL	K
L	PC03	PC02	PC04	PC09	PC05	VCC2_12	VSS_14	VSS_15	VSS10	VCL10	VCL0	VSS0	P414	P402	VCC_01	P214/XCOUT	P215/XCIN/EXCIN	L
M	PC00	P607	PC01	PC08	PC10	P104	VCC2_14	VCC2_15	P810	VSS11	VCL11	P412	P710	P411	P408	VBATT	VSS_01	M
N	P605	P604	P606	PC06	P107	P106	P105	P811	P013	P011	P807	P708	P712	P714	P711	P713	P401	N
P	P603	P602	P600	P601	P102	P801	P803	P812	P012	P010	P009	P805	P512	P413	P515	P709	P400	P
R	VCC2_13	P315	P900	P103	P101	P802	P804	P501	AVCC0	AVSS0	P005	P003	P513	P514	P415	P409	P407	R
T	P205	P203	P313	P901	P809	P800	P502	P014	VREFL	VREFL0	P004	P007	P001	P806	P715	P815/USB_DM	VSS_USB	T
U	P204	P202	P314	VSS_13	P808	P100	P500	P015	VREFH	VREFH0	P008	P006	P000	P002	P511	P814/USB_DP	VCC_USB	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

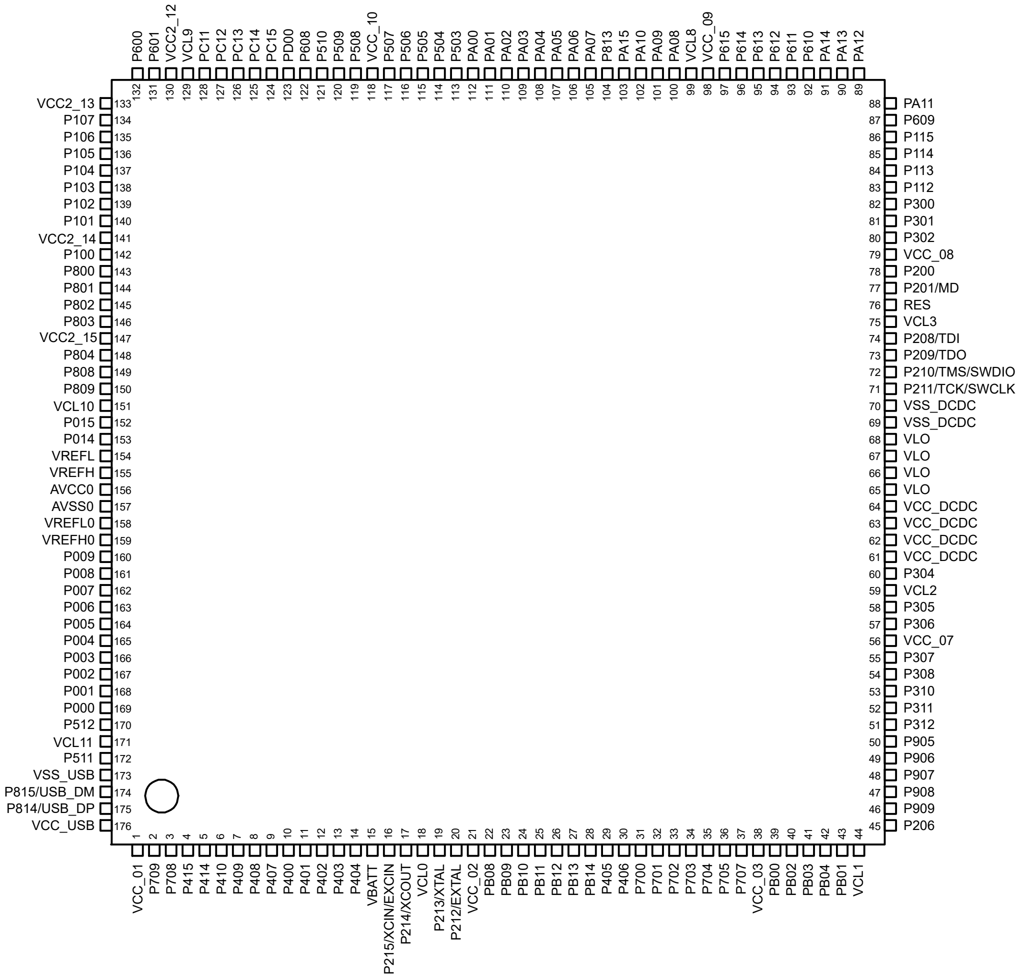
Figure 1.3 Pin assignment for BGA 289-pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	PA11	P114	P112	P300	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P309	P312	P908	P905	P206	A
B	P610	PA12	P115	P113	P302	VLO	VLO	VSS_DCDC	VCC_DCDC	VCC_DCDC	P311	P310	P906	P907	P909	B
C	P612	P611	PA13	P609	P301	RES	P210/TMS/SWDIO	P211/TCK/SWCLK	P304	P306	P305	P307	PB03	PB00	PB01	C
D	P615	P613	P614	PA14	P200	P208/TDI	P201/MD	P209/TDO	P902	P308	PB02	PB04	P705	P707	P706	D
E	PA15	PA08	P813	PA09	VCC_08	VSS_08	VSS5	VCL5	VSS_07	VCC_07	P405	P702	P704	P406	P701	E
F	PA06	PA10	PA05	PA07	VCC_09	VSS_09	VSS6	VCL6	VCL4	VSS4	P700	P703	PB14	PB12	PB11	F
G	PA04	PA02	PA01	PA03	VCC_10	VSS_10	VSS7	VCL7	VCL3	VSS3	P404	VCC_05	PB09	PB10	PB13	G
H	PA00	P504	P503	P505	PC14	VSS_15	VSS8	VCL8	VCL2	VSS2	P403	PB08	VSS_05	VSS_03	VSS_02	H
J	P506	P510	P507	P508	PC12	VCC2_15	VSS9	VCL9	VCL1	VSS1	P402	VCC_03	VCC_02	P213/XTAL	P212/EXTAL	J
K	PC15	P608	PD00	P509	VCC2_14	VSS_14	VSS10	VCL10	VCL0	VSS0	P410	P407	VCC_01	P214/XCOUT	P215/XCIN/EXCIN	K
L	PC13	P604	P603	P107	P106	P104	P105	VSS11	VCL11	P409	P414	P408	P415	VBATT	VSS_01	L
M	PC11	P602	P600	P601	P102	P801	P803	P009	P007	P708	P411	P710	P709	P711	P401	M
N	VCC2_12	P315	VSS_13	P103	P101	P802	P804	AVCC0	AVSS0	P005	P001	P712	P714	P713	P400	N
P	P205	P203	P313	VCC2_13	P809	P800	P015	VREFL	VREFL0	P006	P002	P003	P512	P815/USB_DM	VSS_USB	P
R	P204	P202	P314	VSS_12	P808	P100	P014	VREFH	VREFH0	P008	P004	P000	P511	P814/USB_DP	VCC_USB	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 1.4 Pin assignment for BGA 224-pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	VSS	P114	P609	P113	P301	P208/ TDI	P210/ TMS/ SWDIO	VLO	VLO	VSS_D CDC	VCC_D CDC	VCC_D CDC	P309	P906	P905	P907	P207	VSS	A
B	P813	PA12	P115	PA11	P112	P209/ TDO	P211/ TCK/ SWCLK	VLO	VLO	VSS_D CDC	VCC_D CDC	VCC_D CDC	P311	P908	P909	P904	PD01	PD02	B
C	PA06	P613	PA13	P300	P302	P200	RES	P110	P903	P308	P305	P307	P911	P206	PD04	PD03	PD05	PD06	C
D	PA04	P611	P610	PA14	P303	P915	P108	P111	P109	P310	P304	P306	P912	PB04	PB07	PB05	PB03	PB01	D
E	PA15	P615	P614	P612	P914	P201/ MD				P902	P312	P910	P913	PB02	PB06	PD07	PB00	P706	E
F	PA02	PA10	PA08	PA09	PC14		VCC_ 08	VSS_ 08	VSS3	VCL3	VSS_ 07	VCC_ 07	P700	P702	P406	P701	P707	P705	F
G	PA00	PA03	PA05	PA07	PC12		VCC_ 09	VSS_ 09	VSS4	VCL4	VSS_ 06	VCC_ 06	P405	P704	P703	PB14	PB12	PB11	G
H	P504	P503	P505	PA01	PC11		VCC_ 10	VSS_ 10	VSS7	VCL5	VSS5	VCC_ 04	VSS_ 04		VCC_ 05	PB09	PB10	PB13	H
J	P506	P507	P508	P509	PC13		VCC2_ 11	VSS_ 11	VCL7	VCL6	VSS6	VCL2	VSS2		PB08	VSS_ 05	VSS_ 03	VSS_ 02	J
K	PC15	P608	P510	PD00	VSS	VSS	VSS_ 12	VSS9	VCL9	VCL8	VSS8	VCL1	VSS1		VCC_ 03	VCC_ 02	P213/ XTAL	P212/ EXTAL	K
L	PC10	VSS	PUP	VCC2_ 16	VSS_ 16		VCC2_ 12	VSS_ 14	VSS_ 15	VSS10	VCL10	VCL0	VSS0	P403	P404	VCC_ 01	P214/ XCOUT	P215/ XCIN/ EXCIN	L
M	PC09	VSS	VSS	VCC2_ 17	VSS_ 17			VCC2 _14	VCC2 _15		VSS11	VCL11		P414	P402	P410	VBATT	VSS_ 01	M
N	PC08	VSS	VSS	VCC2_ 18	VSS_ 18		P105			P810				P710	P411	P408	P412	P401	N
P	VSS	VSS	VSS	VCC2_ 19	VSS_ 19	P104	P107	P106	P811	P013	P011	P807	P708	P712	P714	P711	P713	P400	P
R	P602	VSS	VSS	P600	P601	P102	P801	P803	P812	P012	P010	P009	P805	P512	P413	P515	P709	P407	R
T	Vpp	VSS	P315	P900	P103	P101	P802	P804	P501	AVCC0	AVSS0	P005	P003	P513	P514	P415	P409	VCC_U SB	T
U	VCC2_ 13	P205	P203	P313	P901	P809	P800	P502	P014	VREFL	VREFL 0	P004	P007	P001	P806	P715	P815/ USB_D M	VSS_U SB	U
V	VSS	P204	P202	P314	VSS_ 13	P808	P100	P500	P015	VREFH	VREFH 0	P008	P006	P000	P002	P511	P814/ USB_D P	VSS	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 1.5 Pin assignment for BGA 303-pin



Note: VSS_01 to VSS_15 and VSS0 to VSS11 are assigned to Exposed PAD on the QFP package bottom. The PAD must be connected to the ground (0V).

Figure 1.6 Pin assignment for 176-pin

1.7 Pin Lists

Table 1.15 Pin list for the Standard product (1 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
A1	C4	87	—	P609	D7/DQ7	IRQ29	TXD0_C/SDA0_C/MOSI0_C/ MISOA_B/CTX1	GTIU/GTIOC5B/ULPTOA1-DS	AD1FLAG1
A2	B4	84	—	P113	D4/DQ4	IRQ28	RXD0_A/SCL0_A/MISO0_A/ SSLA1_B/SD0DAT5_B	GTETRGB/GTIOC2A/ ULPTOA0-DS	ADST1
A3	B3	86	—	P115	D6/DQ6	IRQ31-DS	CTS0_A/MOSIA_B/SD0DAT7_B	GTETRGD/GTIOC5A	AD0FLAG1
A4	A4	83	—	P112	D3/DQ3	IRQ27	TXD0_A/SDA0_A/MOSI0_A/ SSLA2_B/SD0DAT4_B	GTETRGA/GTIOC3B/ ULPTOB0-DS	ADST0
A5	B5	80	—	P302	D0/DQ0	IRQ5	RXD6_B/SCL6_B/MISO6_B/ SD0DAT1_B	GTOUUP/GTIOC4A/ ULPTO0-DS	—
A6	—	—	—	P915	—	IRQ8	CTS6_B	GTIOC5A	—
A7	A6	68	VLO	—	—	—	—	—	—
A8	A7	66	VLO	—	—	—	—	—	—
A9	A8	70	VSS_DCDC	—	—	—	—	—	—
A10	A9	64	VCC_DCDC	—	—	—	—	—	—
A11	A10	62	VCC_DCDC	—	—	—	—	—	—
A12	A11	—	—	P309	—	IRQ25-DS	CTS9_B/ET1_GTX_CLK/ RGMII1_TXC	GTCPPO8	VCOUT
A13	B13	49	—	P906	—	IRQ9	CTS6_A/USB_ID/ET1_RXD0/ RGMII1_RXD0/RMII1_RXD0/ CAT1_ERXD0	GTIOC13B/ULPTO1	AD0FLAG1
A14	A14	50	—	P905	—	IRQ8	RXD3_B/SCL3_B/MISO3_B/ ET1_RX_CLK/RGMII1_RXC/ RMII1_REF50CK/CAT1_RX_CLK	GTCPPO13	AD1FLAG1
A15	B14	48	—	P907	—	IRQ10	SCK6_A/DE6/USB_EXICEN/ ET1_RXD1/RGMII1_RXD1/ RMII1_RXD1/CAT1_ERXD1	GTIOC13A/ULPTEE1	ADSYNC
A16	—	—	—	P904	—	IRQ2	ET1_RXD4	GTIOC11B	—
A17	—	—	—	P207	—	IRQ25	ET1_RXD5	GTCPPO3	—
B1	E3	104	—	P813	SDCS	IRQ15	SCK7_A/DE7	GTETRGA/GTIOC7B	—
B2	B2	89	—	PA12	D9/DQ9	IRQ11	RXD9_C/SCL9_C/MISO9_C	GTIW/GTIOC6B	—
B3	A3	85	—	P114	D5/DQ5	IRQ30-DS	CTS_RTS0_A/SS0_A/DE0/ SSLA0_B/SD0DAT6_B	GTETRGC/GTIOC2B	ADSYNC
B4	A2	88	—	PA11	D8/DQ8	IRQ10	SCK9_C/DE9	GTIV/GTIOC6A	—
B5	A5	82	—	P300	D2/DQ2	IRQ4	SCK0_A/DE0/SSLA3_B/ SD0DAT3_B	GTIOC3A/ULPTEVI0-DS	—
B6	—	—	—	P303	—	IRQ29-DS	SCK6_B/DE6	GTIOC7B	—
B7	B6	67	VLO	—	—	—	—	—	—
B8	B7	65	VLO	—	—	—	—	—	—
B9	B8	69	VSS_DCDC	—	—	—	—	—	—
B10	B9	63	VCC_DCDC	—	—	—	—	—	—
B11	B10	61	VCC_DCDC	—	—	—	—	—	—
B12	B11	52	—	P311	—	IRQ23-DS	SCK3_B/DE3/CRX0/ET1_TX_CLK/ CAT1_TX_CLK	GTADSM1/GTCPPO6/ AGTOB1	—
B13	A13	47	—	P908	—	IRQ11	TXD6_A/SDA6_A/MOSI6_A/CRX1/ USB_OVRCURB/ET1_RXD2/ RGMII1_RXD2/CAT1_ERXD2	GTIOC12B/ULPTEVI1	ADST1
B14	B15	46	—	P909	—	IRQ21-DS	RXD6_A/SCL6_A/MISO6_A/CTX1/ USB_OVRCURA/ET1_RXD3/ RGMII1_RXD3/CAT1_ERXD3	GTIOC12A/ULPTOA1	ADST0
B15	A15	45	CLKOUT	P206	CS7	IRQ0-DS	USB_VBUSEN/SD0DAT7_C/ ET1_RX_DV/RGMII1_RX_CTL/ RMII1_CRS_DV/CAT1_RX_DV	GTIU/GTCPPO0/ULPTOB1	—
B16	—	—	—	PD01	—	IRQ22	SCK8_C/DE8/SD0DAT2_C/ ET1_RXD6	GTCPPO2	—
B17	—	—	—	PD02	—	IRQ21	TXD8_C/SDA8_C/MOSI8_C/ SD0DAT1_C/ET1_RXD7	GTCPPO1	—
C1	F1	106	—	PA06	CS1/CKE	IRQ17	CTS2_C/SD0DAT1_A	GTETRGC/GTIOC7B	—
C2	D2	95	—	P613	D15/ DQ15	IRQ19	CTS0_C	GTETRGA/GTIOC9B/ AGTO1	—

Table 1.15 Pin list for the Standard product (2 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
C3	C3	90	—	PA13	D10/ DQ10	IRQ12	CTS_RTS9_C/SS9_C/DE9	GTOVUP/GTIOC10A	—
C4	C5	81	—	P301	D1/DQ1	IRQ6	TXD6_B/SDA6_B/MOSI6_B/ SD0DAT2_B	GTOULO/GTIOC4B/ AGTIO0/ULPTEE0-DS	—
C5	D5	78	—	P200	—	NMI	—	—	—
C6	C7	72	TMS/SWDIO	P210	—	IRQ24	CTS_RTS9_B/SS9_B/DE9	GTOULO/GTIOC0B	—
C7	D6	74	TDI	P208	—	IRQ3	RXD9_B/SCL9_B/MISO9_B/CRX1	GTOVLO/GTIOC1B	VCOUT
C8	—	—	—	P110	—	IRQ20	SD0DAT4_C	GTIOC9B	—
C9	D10	54	TCLK	P308	—	IRQ26-DS	CTS3_B/SD0CLK_B/ET1_TX_ER/ ETHPHYCLK	GTIU/GTCPPO9/ULPTOB1	—
C10	C11	58	TDATA2	P305	—	IRQ8	SD0WP/ET1_TXD2/RGMII1_TXD2/ CAT1_ETXD2	GTOVUP/GTCPPO12/ ULPTEE1	—
C11	C12	55	TDATA0	P307	—	IRQ27-DS	CTS_RTS6_A/SS6_A/DE6/ SD0CMD_B/ET1_TXD0/ RGMII1_TXD0/RMII1_TXD0/ CAT1_ETXD0	GTIV/GTCPPO10/ULPTOA1	—
C12	—	—	—	P911	—	IRQ6	ET1_TXD5	GTIOC3B	—
C13	A12	51	—	P312	—	IRQ22-DS	CTS_RTS3_B/SS3_B/DE3/CTX0/ ET1_RX_ER/RMII1_RX_ER/ CAT1_RX_ER	GTADSM0/GTCPPO5/ AGTOA1	—
C14	—	—	—	PD04	—	IRQ20	CTS_RTS8_C/SS8_C/DE8/ SD0CMD_C/ET0_RXD5	GTIOC3A	—
C15	—	—	—	PD03	—	IRQ21	RXD8_C/SCL8_C/MISO8_C/ SD0DAT0_C/ET0_RXD4	GTIOC3B	—
C16	—	—	—	PD05	—	IRQ19	CTS8_C/SD0CLK_C/ET0_RXD6	GTIOC2B	—
C17	—	—	—	PD06	—	IRQ18	SD0WP/ET0_RXD7	GTIOC2A	—
D1	G1	108	—	PA04	A1/DQM3	IRQ19	SCK2_C/DE2/SD0DAT3_A	GTIU/GTIOC4B	ADST0
D2	C2	93	CACREF/CLKOUT	P611	D13/ DQ13	IRQ17	SCK0_C/DE0/MOSIA_B	GTOULO/GTIOC4B	—
D3	B1	92	—	P610	D12/ DQ12	IRQ16	RXD0_C/SCL0_C/MISO0_C/ RSPCKA_B/CRX1	GTOUUP/GTIOC4A/ ULPTOB1-DS	—
D4	D4	91	—	PA14	D11/ DQ11	IRQ13	TXD9_C/SDA9_C/MOSI9_C	GTOVLO/GTIOC10B	—
D5	C6	76	RES	—	—	—	—	—	—
D6	C8	71	TCK/SWCLK	P211	—	IRQ23	SCK9_B/DE9	GTOUUP/GTIOC0A	—
D7	—	—	—	P109	—	IRQ23	SD0DAT5_C	GTIOC10A	—
D8	—	—	—	P108	—	IRQ24	SD0DAT6_C	GTIOC10B	—
D9	—	—	—	P903	—	IRQ1	—	GTIOC11A	—
D10	C9	60	TDATA3	P304	—	IRQ9	SD0DAT0_B/ET1_TXD3/ RGMII1_TXD3/CAT1_ETXD3	GTOVLO/GTIOC7A/ ULPTO1	—
D11	C10	57	TDATA1	P306	—	IRQ28-DS	SD0CD/ET1_TXD1/RGMII1_TXD1/ RMII1_TXD1/CAT1_ETXD1	GTIW/GTCPPO11/ ULPTEVI1	—
D12	—	—	—	P912	—	IRQ5	ET1_TXD6	GTIOC3A	—
D13	D12	42	—	PB04	—	IRQ9	SCK5_C/DE5/ET0_TXD3/ RGMII0_TXD3/CAT0_ETXD3	GTCPPO3	AD0FLAG1
D14	—	—	—	PB07	—	IRQ1	ET0_TXD5	GTIOC9B	—
D15	—	—	—	PB05	—	IRQ15	CTS5_C/ET0_TXD7	GTCPPO4	—
D16	C13	41	—	PB03	—	IRQ13	TXD5_C/SDA5_C/MOSI5_C/ ET0_TXD2/RGMII0_TXD2/ CAT0_ETXD2	GTCPPO1	ADSYNC
D17	C15	43	—	PB01	ALE	IRQ12	CTS_RTS1_B/SS1_B/DE1/ ET0_TX_CLK/CAT0_TX_CLK	GTCPPO2	AD1FLAG1
E1	E1	103	—	PA15	EBCLK/ SDCLK	IRQ14	CTS9_C	GTIOC7A	—
E2	D1	97	—	P615	WR2/BC 2/DQM2	IRQ7	TXD7_A/SDA7_A/MOSI7_A	GTETRGC/GTCPPO10	—
E3	D3	96	—	P614	WR/WR0 /DQM0	IRQ20	RXD7_A/SCL7_A/MISO7_A	GTETRGB/GTCPPO9/ AGTO0	—
E4	C1	94	—	P612	D14/ DQ14	IRQ18	CTS_RTS0_C/SS0_C/DE0/ SSLA0_B	GTIOC9A	—
E5	—	—	—	P914	—	IRQ9	CTS_RTS6_B/SS6_B/DE6	GTIOC5B	—
E6	D7	77	MD	P201	—	IRQ4	—	—	—

Table 1.15 Pin list for the Standard product (3 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
E7	D8	73	TDO/SWO/CLKOUT	P209	—	IRQ25	TXD9_B/SDA9_B/MOSI9_B/CTX1	GTOVUP/GTIOC1A	—
E8	—	—	—	P111	—	IRQ19	SD0DAT3_C	GTIOC9A	—
E9	D9	—	—	P902	ALE	IRQ0	ETHPHYCLK	GTCPPO13	—
E10	B12	53	—	P310	—	IRQ24-DS	TXD3_B/SDA3_B/MOSI3_B/ ET1_TX_EN/RGMII1_TX_CTL/ RMII1_TX_EN/CAT1_TX_EN	GTCPPO7/AGTEE1	—
E11	—	—	—	P910	—	IRQ7	ET1_TXD4	GTCPPO12	—
E12	—	—	CLKOUT	P913	—	IRQ3	ET1_TXD7	GTCPPO11	—
E13	D11	40	—	PB02	—	IRQ11	RXD5_C/SCL5_C/MISO5_C/ ET0_TXD1/RGMII0_TXD1/ RMII0_TXD1/CAT0_ETXD1	GTCPPO0	ADST1
E14	—	—	—	PB06	—	IRQ0	CTS_RTS5_C/SS5_C/DE5/ ET0_TXD6	GTIOC9A	—
E15	—	—	—	PD07	—	IRQ17	SD0CD/ET0_TXD4	GTCPPO0	—
E16	C14	39	—	PB00	—	IRQ10	SCK1_B/DE1/ET0_TXD0/ RGMII0_TXD0/RMII0_TXD0/ CAT0_ETXD0/DSM1CLK2	GTCPPO4	ADST0
E17	D15	—	—	P706	—	IRQ7	RXD1_B/SCL1_B/MISO1_B/ ET0_GTX_CLK/RGMII0_TXC/ ETHPHYCLK/DSM1CLK0	GTCPPO2/AGTIO0	—
F1	G2	110	—	PA02	A3	IRQ31	RXD2_C/SCL2_C/MISO2_C/ SD0DAT5_A	GTIW/GTCPPO9	ADSYNC
F2	F2	102	—	PA10	CS2/RAS	IRQ4	SCK5_B/DE5	GTCPPO13	—
F3	E2	100	—	PA08	CS0/WE	IRQ6	RXD5_B/SCL5_B/MISO5_B	GTETRGD/GTCPPO11	—
F4	E4	101	—	PA09	CS3/CAS	IRQ5	TXD5_B/SDA5_B/MOSI5_B	GTCPPO12	—
F5	H5	125	—	PC14	D16/ DQ16	IRQ0	TXD6_C/SDA6_C/MOSI6_C/ ET0_WOL/DSM1DAT1	GTADSM1/GTCPPO9	—
F6	E5	79	VCC_08	—	—	—	—	—	—
F7	E6	—	VSS_08	—	—	—	—	—	—
F8	G10	—	VSS3	—	—	—	—	—	—
F9	G9	75	VCL3	—	—	—	—	—	—
F10	E9	—	VSS_07	—	—	—	—	—	—
F11	E10	56	VCC_07	—	—	—	—	—	—
F12	F11	31	—	P700	—	IRQ16-DS	RXD2_B/SCL2_B/MISO2_B/ MISOA_C/SD1WP/ET0_RXD2/ RGMII0_RXD2/CAT0_ERXD2/ DSM0CLK0	GTIOC5A	—
F13	E12	33	—	P702	—	IRQ18-DS	CTS2_B/RSPCKA_C/SD1DAT5_B/ ET0_RXD0/RGMII0_RXD0/ RMII0_RXD0/CAT0_ERXD0/ DSM0CLK2	GTIOC6A/ULPTO0	—
F14	E14	30	—	P406	—	IRQ31	TXD2_B/SDA2_B/MOSI2_B/ SSLA3_C/SD1CD/ET0_RXD3/ RGMII0_RXD3/CAT0_ERXD3/ DSM0DAT2	GTIOC1B	—
F15	E15	32	—	P701	—	IRQ17-DS	CTS_RTS2_B/SS2_B/DE2/ MOSIA_C/SD1DAT4_B/ET0_RXD1/ RGMII0_RXD1/RMII0_RXD1/ CAT0_ERXD1/DSM0CLK1	GTIOC5B/ULPTO1	—
F16	D14	37	—	P707	—	IRQ8	TXD1_B/SDA1_B/MOSI1_B/ ET0_TX_ER/ETHPHYCLK/ DSM1CLK1	GTCPPO3	—
F17	D13	36	—	P705	—	IRQ19	CTS1_B/SSLA2_C/CRX0/ ET0_TX_EN/RGMII0_TX_CTL/ RMII0_TX_EN/CAT0_TX_EN/ DSM1DAT2	GTADSM1/GTCPPO1/ AGTIO0	—
G1	H1	112	—	PA00	A5	IRQ22	CTS_RTS5_B/SS5_B/DE5/ SD0DAT7_A	GTOVLO/GTCPPO7	AD1FLAG1
G2	G4	109	—	PA03	A2	IRQ20	TXD2_C/SDA2_C/MOSI2_C/ SD0DAT4_A	GTIV/GTCPPO10	ADST1
G3	F3	107	—	PA05	A0/BC0/ DQM1	IRQ18	CTS_RTS2_C/SS2_C/DE2/ SD0DAT2_A	GTETRGD/GTIOC4A	—
G4	F4	105	—	PA07	RD	IRQ16	CTS7_A/SD0DAT0_A	GTETRGB/GTIOC7A	VCOUT
G5	J5	127	—	PC12	D18/ DQ18	IRQ2	SCK6_C/DE6/ET0_MDIO/ CAT0_MDIO/DSM1CLK0	GTCPPO11	—
G6	F5	98	VCC_09	—	—	—	—	—	—

Table 1.15 Pin list for the Standard product (4 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
G7	F6	—	VSS_09	—	—	—	—	—	—
G8	F10	—	VSS4	—	—	—	—	—	—
G9	F9	—	VCL4	—	—	—	—	—	—
G10	—	—	VSS_06	—	—	—	—	—	—
G11	—	—	VCC_06	—	—	—	—	—	—
G12	E11	29	—	P405	—	IRQ30	SCK2_B/DE2/SD1DAT3_B/ ET0_RX_DV/RGMII0_RX_CTL/ RMII0_CRS_DV/CAT0_RX_DV/ DSM0DAT1	GTIOC1A/AGTIO1	—
G13	E13	35	—	P704	—	IRQ26	SSLA1_C/CTX0/SD1DAT7_B/ ET0_RX_ER/RMII0_RX_ER/ CAT0_RX_ER/DSM1DAT1	GTADSM0/GTCPPO0/ AGTO0	—
G14	F12	34	—	P703	—	IRQ19-DS	SSLA0_C/SD1DAT6_B/ ET0_RX_CLK/RGMII0_RXC/ RMII0_REF50CK/CAT0_RX_CLK/ DSM1DAT0	GTIOC6B/AGTO1	VCOUT
G15	F13	28	—	PB14	—	IRQ10	CATSYNC0	—	—
G16	F14	26	—	PB12	—	IRQ6	CATLINKACT0	—	—
G17	F15	25	—	PB11	—	IRQ5	CATLEDERR	—	—
H1	H2	114	—	P504	A7	IRQ7	SD0WP	GTOULO/GTCPPO1	—
H2	H3	113	—	P503	A6	IRQ6	SD0CD	GTOUUP/GTCPPO6	—
H3	H4	115	—	P505	A8	IRQ8	SD0CLK_A	GTOWUP/GTCPPO2	—
H4	G3	111	—	PA01	A4	IRQ21	CTS5_B/SD0DAT6_A	GTOVUP/GTCPPO8	AD0FLAG1
H5	M1	128	—	PC11	D19/ DQ19	IRQ3	CTS_RTS6_C/SS6_C/DE6/ ET0_MDC/CAT0_MDC/DSM1CLK1	GTCPPO12	—
H6	G5	118	VCC_10	—	—	—	—	—	—
H7	G6	—	VSS_10	—	—	—	—	—	—
H8	G7	—	VSS7	—	—	—	—	—	—
H9	E8	—	VCL5	—	—	—	—	—	—
H10	E7	—	VSS5	—	—	—	—	—	—
H11	—	—	VCC_04	—	—	—	—	—	—
H12	—	—	VSS_04	—	—	—	—	—	—
H13	H11	13	—	P403	—	IRQ14-DS	CTS_RTS1_A/SS1_A/DE1/ SD1DAT1_B/ET1_WOL/ CATI2CCLK	GTIOC3A/RTCIC1	AD0FLAG1
H14	G12	—	VCC_05	—	—	—	—	—	—
H15	G13	23	—	PB09	—	IRQ13	CATIRQ	—	—
H16	G14	24	—	PB10	—	IRQ4	CATLEDSTER	—	—
H17	G15	27	—	PB13	—	IRQ7	CATLINKACT1	—	—
J1	J1	116	—	P506	A9	IRQ9	SD0CMD_A	GTOWLO/GTCPPO3	—
J2	J3	117	—	P507	A10	IRQ10	CTS_RTS7_A/SS7_A/DE7/ ET_TAS_STA0	GTADSM0/GTIOC0A	—
J3	J4	119	—	P508	A11	IRQ1	CTS5_A/ET_TAS_STA1	GTADSM1/GTIOC0B	—
J4	K4	120	—	P509	A12	IRQ2	CTS_RTS5_A/SS5_A/DE5/ ET_TAS_STA2	GTIOC1A/ULPTEVI1	—
J5	L1	126	—	PC13	D17/ DQ17	IRQ1	RXD6_C/SCL6_C/MISO6_C/ ET0_INT/DSM1DAT2	GTCPPO10	—
J6	—	—	VCC2_11	—	—	—	—	—	—
J7	—	—	VSS_11	—	—	—	—	—	—
J8	G8	—	VCL7	—	—	—	—	—	—
J9	F8	—	VCL6	—	—	—	—	—	—
J10	F7	—	VSS6	—	—	—	—	—	—
J11	H9	59	VCL2	—	—	—	—	—	—
J12	H10	—	VSS2	—	—	—	—	—	—
J13	G11	14	—	P404	—	IRQ15-DS	CTS1_A/SD1DAT2_B/ET0_WOL/ CATI2CDATA/DSM0DAT0	GTIOC3B/RTCIC2	AD1FLAG1
J14	H12	22	—	PB08	—	IRQ12	CATLEDRUN	—	—
J15	H13	—	VSS_05	—	—	—	—	—	—

Table 1.15 Pin list for the Standard product (5 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
J16	H14	—	VSS_03	—	—	—	—	—	—
J17	H15	—	VSS_02	—	—	—	—	—	—
K1	K1	124	—	PC15	A16	IRQ30	CTS6_C/CRX1	GTADSM0	—
K2	K2	122	CACREF	P608	A14	IRQ22	TXD5_A/SDA5_A/MOSI5_A	GTOWUP/GTCPPO4	—
K3	J2	121	—	P510	A13	IRQ3	RXD5_A/SCL5_A/MISO5_A/ ET_TAS_STA3	GTIOC1B/ULPTEVI0	—
K4	K3	123	—	PD00	A15	IRQ23	SCK5_A/DE5/CTX1	GTOWLO/GTCPPO5	—
K5	—	—	—	PC07	D23/ DQ23	IRQ21	OM_1_RESET/DSM0DAT0	GTCPPO0	—
K6	R4	—	VSS_12	—	—	—	—	—	—
K7	J7	—	VSS9	—	—	—	—	—	—
K8	J8	129	VCL9	—	—	—	—	—	—
K9	H8	99	VCL8	—	—	—	—	—	—
K10	H7	—	VSS8	—	—	—	—	—	—
K11	J9	44	VCL1	—	—	—	—	—	—
K12	J10	—	VSS1	—	—	—	—	—	—
K13	K11	6	—	P410	A19	IRQ5	SCK3_A/DE3/SCL0_A[*1]/ USB_OVRCURB-DS/ GPTP_MATCH0/CATI2CCLK	GTOVLO/GTIOC9B/ AGTOB1	ADST0
K14	J12	38	VCC_03	—	—	—	—	—	—
K15	J13	21	VCC_02	—	—	—	—	—	—
K16	J14	19	XTAL	P213	—	IRQ2	TXD1_C/SDA1_C/MOSI1_C	GTETRGC/GTIOC0A/ ULPTEE0	ADTRG1
K17	J15	20	EXTAL	P212	—	IRQ3	RXD1_C/SCL1_C/MISO1_C	GTETRGD/GTIOC0B/ AGTEE1	—
L1	—	—	—	PC03	D27/ DQ27	IRQ25	TXD7_C/SDA7_C/MOSI7_C/ OM_1_SIO4/DSM0CLK1	GTCPPO4	—
L2	—	—	—	PC02	D28/ DQ28	IRQ26	SCK7_C/DE7/OM_1_SIO3/ DSM0CLK2	GTCPPO5	—
L3	—	—	—	PC04	D26/ DQ26	IRQ24	RXD7_C/SCL7_C/MISO7_C/ OM_1_SIO2/DSM0CLK0	GTCPPO3	—
L4	—	—	—	PC09	D21/ DQ21	IRQ5	OM_1_RSTO1	—	—
L5	—	—	—	PC05	D25/ DQ25	IRQ23	OM_1_CS1/DSM0DAT2	GTCPPO2	—
L6	N1	130	VCC2_12	—	—	—	—	—	—
L7	K6	—	VSS_14	—	—	—	—	—	—
L8	H6	—	VSS_15	—	—	—	—	—	—
L9	K7	—	VSS10	—	—	—	—	—	—
L10	K8	151	VCL10	—	—	—	—	—	—
L11	K9	18	VCL0	—	—	—	—	—	—
L12	K10	—	VSS0	—	—	—	—	—	—
L13	L11	5	—	P414	A23	IRQ9	RXD4_B/SCL4_B/MISO4_B/ SSLB0_B/CRX1/ET1_MDIO/ CATLATCH1	GTIOC0B	—
L14	J11	12	CACREF	P402	—	IRQ4-DS	SCK1_A/DE1/CRX0/SD1DAT0_B/ ET0_LINKSTA/CAT0_LINKSTA	RTCIC0	—
L15	K13	1	VCC_01	—	—	—	—	—	—
L16	K14	17	XCOUT	P214	—	IRQ21	—	—	—
L17	K15	16	XCIN/EXCIN	P215	—	IRQ20	—	—	—
M1	—	—	—	PC00	D30/ DQ30	IRQ28	CTS_RTS7_C/SS7_C/DE7/ OM_1_SIO5	GTCPPO7	—
M2	—	—	—	P607	D31/ DQ31	IRQ23	OM_1_DQS	—	—
M3	—	—	—	PC01	D29/ DQ29	IRQ27	CTS7_C/OM_1_SIO0	GTCPPO6	—
M4	—	—	—	PC08	D22/ DQ22	IRQ29	OM_1_CS0/DSM1DAT0	GTCPPO8	—
M5	—	—	—	PC10	D20/ DQ20	IRQ4	OM_1_WP1/DSM1CLK2	GTCPPO13	—

Table 1.15 Pin list for the Standard product (6 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
M6	L6	137	—	P104	—	IRQ1	CTS9_A/SSLB1_A/OM_0_CS1/ GPTP_MATCH0/CATLATCH0/ DSM0DAT1	GTETRGB/GTIOC1B	AD0FLAG1
M7	K5	141	VCC2_14	—	—	—	—	—	—
M8	J6	147	VCC2_15	—	—	—	—	—	—
M9	—	—	—	P810	—	IRQ21	SCK7_B/DE7/SD1DAT2_A	GTIOC10A/ULPTOA0	—
M10	L8	—	VSS11	—	—	—	—	—	—
M11	L9	171	VCL11	—	—	—	—	—	—
M12	—	—	—	P412	A21	IRQ20-DS	CTS3_A/USB_EXICEN/ GPTP_PTPOUT0	GTOULO/GTCPPO8/ AGTEE1	—
M13	M12	—	—	P710	CS5	IRQ17	CTS4_B/SSLB3_B/ET0_LINKSTA/ CAT0_LINKSTA	GTIOC11B	—
M14	M11	—	CACREF	P411	A20	IRQ4	CTS_RTS3_A/SS3_A/DE3/USB_ID/ GPTP_PTPOUT1	GTOVUP/GTIOC9A/ AGTOA1	—
M15	L12	8	—	P408	A17	IRQ7	RXD3_A/SCL3_A/MISO3_A/ SCL0_B*1/USB_VBUSEN/ GPTP_PTPOUT2/CATRESETOUT	GTOWLO/GTIOC10A/ ULPTOB0	ADSYNC
M16	L14	15	VBATT	—	—	—	—	—	—
M17	L15	—	VSS_01	—	—	—	—	—	—
N1	—	—	—	P605	—	IRQ25	CTS0_B/OM_1_SIO1	GTIOC8A	—
N2	L2	—	—	P604	—	IRQ26	CTS_RTS0_B/SS0_B/DE0/ OM_1_SIO7	GTIOC8B	—
N3	—	—	—	P606	WR3/BC 3	IRQ24	OM_1_SIO6	—	—
N4	—	—	—	PC06	D24/ DQ24	IRQ22	OM_1_ECSINT1/DSM0DAT1	GTCPPO1	—
N5	L4	134	—	P107	—	IRQ31	CTS4_A/OM_0_CS0/ET1_INT	GTOWUP/GTIOC8A/ AGTOA0	ADST0
N6	L5	135	—	P106	—	IRQ16	CTS8_B/SSLB3_A/OM_0_RESET/ ET1_LINKSTA/CAT1_LINKSTA	GTOWLO/GTIOC8B/ AGTOB0/ULPTEE1-DS	ADST1
N7	L7	136	—	P105	—	IRQ0	CTS_RTS8_B/SS8_B/DE8/ SSLB2_A/OM_0_ECSINT1/ GPTP_CAPTURE0/CATSYNC1/ DSM0DAT0	GTIOC1A/ULPTO1-DS	ADSYNC
N8	—	—	—	P811	—	IRQ22	CTS7_B/USB_ID/SD1DAT3_A	GTIOC10B/ULPTOB0	—
N9	—	—	—	P013	—	IRQ14	—	—	AN013
N10	—	—	—	P011	—	IRQ16	—	—	AN011
N11	—	—	—	P807	—	IRQ11	—	GTIOC13A	—
N12	M10	3	CACREF	P708	WR1/BC 1	IRQ11	SCK4_B/DE4/SDA2_A*1/MOSIB_B/ ET0_MDC/CAT0_MDC	GTCPPO6	—
N13	N12	—	—	P712	—	IRQ2	CTS1_C/SSLB1_B/ GPTP_CAPTURE1/CATLATCH1	GTIOC2B/AGTOB0	—
N14	N13	—	—	P714	—	IRQ13	TXD4_C/SDA4_C/MOSI4_C/ GPTP_PPS1/CATSYNC1	GTIOC12B	—
N15	M14	—	—	P711	—	IRQ3	CTS_RTS1_C/SS1_C/DE1/ SSLB2_B/GPTP_PPS0/ CATRESETOUT	GTIOC11A/AGTEE0	—
N16	N14	—	—	P713	—	IRQ14	CTS4_C/GPTP_MATCH1/ CATLATCH0	GTIOC2A/AGTOA0	—
N17	M15	11	—	P401	—	IRQ5-DS	RXD1_A/SCL1_A/MISO1_A/ I3C_SDA0/CTX0/SD1CMD_B	GTETRGA/GTIOC6B	—
P1	L3	—	—	P603	—	IRQ27	TXD0_B/SDA0_B/MOSI0_B/ OM_1_SCLK	GTIOC7A/ULPTO0	—
P2	M2	—	—	P602	—	IRQ28	RXD0_B/SCL0_B/MISO0_B/ OM_1_SCLKN	GTIOC7B/ULPTEE0	—
P3	M3	132	CACREF	P600	—	IRQ30	OM_0_RSTO1/ET1_WOL	GTIOC6B/ULPTEVI1-DS	—
P4	M4	131	—	P601	—	IRQ29	SCK0_B/DE0/OM_0_WP1	GTIOC6A/ULPTEVI0/ RTCOUT	—
P5	M5	139	—	P102	—	IRQ17	TXD9_A/SDA9_A/MOSI9_A/ RSPCKB_A/CRX0/OM_0_SIO4/ DSM0CLK0	GTOWLO/GTIOC2B/AGTO0	ADTRG0
P6	M6	144	—	P801	—	IRQ12	TXD2_A/SDA2_A/MOSI2_A/ OM_0_DQS/GPTP_PPS1/ CATRESETOUT/DSM1DAT1	GTIV/GTIOC11B/AGTOB0	—

Table 1.15 Pin list for the Standard product (7 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
P7	M7	146	—	P803	—	IRQ19	SCK2_A/DE2/OM_0_SIO1/ DSM1CLK0	GTETRGC/GTIOC12B	—
P8	—	—	—	P812	—	IRQ23	CTS_RTS7_B/SS7_B/DE7/ USB_EXICEN/SD1DAT4_A	GTIOC11A	AN022
P9	—	—	—	P012	—	IRQ15	—	—	AN012
P10	—	—	—	P010	—	IRQ14	—	—	AN010
P11	M8	160	—	P009	—	IRQ13-DS	—	—	AN009/IVREF1
P12	—	—	—	P805	—	IRQ30	TXD8_A/SDA8_A/MOSI8_A/ ET1_MDIO	—	AN017/IVCMP0
P13	P13	170	—	P512	—	IRQ14	CTS8_A/SCL1_A[*1]/CTX1/ET1_INT	GTIOC0A	—
P14	—	—	—	P413	A22	IRQ18	ET_TAS_STA3	GTOUUP/GTCPPO7/ ULPTEE1	—
P15	—	—	—	P515	—	IRQ12	CTS_RTS4_C/SS4_C/DE4/ SCL2_B[*1]/ET_TAS_STA0	GTIOC13A	—
P16	M13	2	—	P709	CS4	IRQ10	CTS_RTS4_B/SS4_B/DE4/ SCL2_A[*1]/MISOB_B/ET0_MDIO/ CAT0_MDIO	GTCPPO5	—
P17	N15	10	—	P400	—	IRQ0	TXD1_A/SDA1_A/MOSI1_A/ I3C_SCL0/SD1CLK_B	GTIOC6A/AGTIO1	ADTRG1
R1	P4	133	VCC2_13	—	—	—	—	—	—
R2	N2	—	—	P315	—	IRQ29	SCK3_C/DE3/SSLA3_A	—	—
R3	—	—	—	P900	—	IRQ30	CTS3_C	GTADSM0	—
R4	N4	138	—	P103	—	IRQ16	CTS_RTS9_A/SS9_A/DE9/ SSLB0_A/CTX0/OM_0_SIO2/ GPTP_PPS0/CATLATCH1/ DSM0DAT2	GTOWUP/GTIOC2A	AD1FLAG1
R5	N5	140	—	P101	—	IRQ1	RXD9_A/SCL9_A/MISO9_A/ MOSIB_A/OM_0_SIO3/ GPTP_CAPTURE1/CATI2CCLK/ DSM0CLK1	GTETRGB/GTIOC8A/ AGTEE0	—
R6	N6	145	—	P802	—	IRQ18	RXD2_A/SCL2_A/MISO2_A/ OM_0_SIO6/DSM1DAT2	GTIW/GTIOC12A	—
R7	N7	148	—	P804	—	IRQ14	CTS_RTS2_A/SS2_A/DE2/ OM_0_SIO7/DSM1CLK1	GTETRGD/GTIOC13A	—
R8	—	—	—	P501	—	IRQ25	TXD8_B/SDA8_B/MOSI8_B/ USB_OVRCURA/SD1DAT6_A	GTIOC12A	AN020
R9	N8	156	AVCC0	—	—	—	—	—	—
R10	N9	157	AVSS0	—	—	—	—	—	—
R11	N10	164	—	P005	—	IRQ10-DS	—	—	AN005/IVCMP3
R12	P12	166	—	P003	—	IRQ29	—	—	AN003/IVCMP3
R13	—	—	—	P513	—	IRQ31	SCK8_A/DE8/ET0_INT	GTIOC13B	AN016/IVCMP0
R14	—	—	—	P514	—	IRQ13	SCK4_C/DE4/SDA2_B[*1]/ ET_TAS_STA1	GTIOC13B	—
R15	L13	4	—	P415	WAIT	IRQ8	TXD4_B/SDA4_B/MOSI4_B/ RSPCKB_B/CTX1/ET1_MDC/ CATLATCH0	GTIOC0A	—
R16	L10	7	—	P409	A18	IRQ6	TXD3_A/SDA3_A/MOSI3_A/ SDA0_A[*1]/USB_OVRCURA-DS/ GPTP_CAPTURE0/CATI2CDATA	GTOWUP/ULPTOA0	ADST1
R17	K12	9	—	P407	CS6	IRQ22	SCK1_C/DE1/SDA0_B[*1]/ USB_VBUS/GPTP_PTPOUT3/ CATSYNC1	GTIOC10B/AGTIO0/ RTCOUT	ADTRG0
T1	P1	—	CLKOUT	P205	—	IRQ1-DS	TXD4_A/SDA4_A/MOSI4_A/ SCL1_B[*1]/SSLA1_A/ USB_OVRCURA/SD1CD	GTIV/GTIOC4A/AGTO1	—
T2	P2	—	—	P203	—	IRQ2-DS	RXD4_A/SCL4_A/MISO4_A/ RSPCKA_A/CTX0/USB_VBUSEN/ SD1CLK_A	GTIOC5A/ULPTOA1	—
T3	P3	—	—	P313	—	IRQ27	TXD3_C/SDA3_C/MOSI3_C/ MISOA_A/USB_ID/SD1DAT0_A	—	—
T4	—	—	—	P901	—	IRQ31	CTS_RTS3_C/SS3_C/DE3	GTADSM1/AGTIO1	—
T5	P5	150	—	P809	—	IRQ20	TXD7_B/SDA7_B/MOSI7_B/ OM_0_SCLKN	—	—
T6	P6	143	—	P800	—	IRQ11	CTS2_A/OM_0_SIO5/DSM1DAT0	GTIU/GTIOC11A/AGTOA0	—

Table 1.15 Pin list for the Standard product (8 of 8)

BGA289	BGA224	HLQFP176	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/ OSPI/SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/DAC12/ ACMPHS
T7	—	—	—	P502	—	IRQ26	SCK8_B/DE8/USB_OVRCURB/ SD1DAT7_A	GTIOC12B	AN019
T8	R7	153	—	P014	—	IRQ27	—	—	AN014/DA0/ IVCMP0
T9	P8	154	VREFL	—	—	—	—	—	—
T10	P9	158	VREFL0	—	—	—	—	—	—
T11	R11	165	—	P004	—	IRQ9-DS	—	—	AN004/IVCMP2
T12	M9	162	—	P007	—	IRQ28	—	—	AN007/IVCMP3
T13	N11	168	—	P001	—	IRQ7-DS	—	—	AN001/IVCMP3
T14	—	—	—	P806	—	IRQ0	RXD8_A/SCL8_A/MISO8_A/ ET1_MDC	—	AN018
T15	—	—	—	P715	—	IRQ12	RXD4_C/SCL4_C/MISO4_C/ ET_TAS_STA2	GTIOC12A	—
T16	P14	174	—	P815	—	IRQ15	CTX0/USB_DM	GTIOC8A	—
T17	P15	173	VSS_USB	—	—	—	—	—	—
U1	R1	—	CACREF	P204	—	IRQ26	SCK4_A/DE4/SDA1_B[*1]/SSLA0_A/ USB_OVRCURB/SD1WP	GTIW/GTIOC4B/AGTIO1	—
U2	R2	—	—	P202	—	IRQ3-DS	CTS_RTS4_A/SS4_A/DE4/ MOSIA_A/CRX0/USB_EXICEN/ SD1CMD_A	GTIOC5B/ULPTOB1	—
U3	R3	—	—	P314	—	IRQ28	RXD3_C/SCL3_C/MISO3_C/ SSLA2_A/SD1DAT1_A	—	ADTRG0
U4	N3	—	VSS_13	—	—	—	—	—	—
U5	R5	149	—	P808	—	IRQ15	RXD7_B/SCL7_B/MISO7_B/ OM_0_SCLK/DSM1CLK2	GTIOC13B	—
U6	R6	142	—	P100	—	IRQ2	SCK9_A/DE9/MISOB_A/ OM_0_SIO0/GPTP_MATCH1/ CATI2CDATA/DSM0CLK2	GTETRGA/GTIOC8B/ AGTIO0	—
U7	—	—	CACREF	P500	—	IRQ24	RXD8_B/SCL8_B/MISO8_B/ USB_VBUSEN/SD1DAT5_A	GTIOC11B	AN021
U8	P7	152	—	P015	—	IRQ13	—	—	AN015/DA1/ IVCMP0
U9	R8	155	VREFH	—	—	—	—	—	—
U10	R9	159	VREFH0	—	—	—	—	—	—
U11	R10	161	—	P008	—	IRQ12-DS	—	—	AN008/IVREF0
U12	P10	163	—	P006	—	IRQ11-DS	—	—	AN006/IVCMP2
U13	R12	169	—	P000	—	IRQ6-DS	—	—	AN000/IVCMP2
U14	P11	167	—	P002	—	IRQ8-DS	—	—	AN002/IVCMP2
U15	R13	172	—	P511	—	IRQ15	CTS_RTS8_A/SS8_A/DE8/ SDA1_A[*1]/CRX1/ET1_LINKSTA/ CAT1_LINKSTA	GTIOC0B	—
U16	R14	175	—	P814	—	IRQ16	CRX0/USB_DP	GTIOC8B	—
U17	R15	176	VCC_USB	—	—	—	—	—	—

Note: Several pin names have the added suffix of _A, _B, and _C. These suffixes have special conditions for electrical characteristics.
Note 1. There are two types for IIC function, one is a simple IIC by SCI and another is a dedicated IIC. This terminal is for a dedicated IIC.

Table 1.16 Pin list for the SiP product (1 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
A1	VSS	—	—	—	—	—	—
A2	—	P114	D5/DQ5	IRQ30-DS	CTS_RTS0_A/SS0_A/DE0/SSLA0_B/ SD0DAT6_B	GTETRGC/GTIOC2B	ADSYNC
A3	—	P609	D7/DQ7	IRQ29	TXD0_C/SDA0_C/MOSI0_C/MISOA_B/CTX1	GTIU/GTIOC5B/ULPTOA1-DS	AD1FLAG1
A4	—	P113	D4/DQ4	IRQ28	RXD0_A/SCL0_A/MISO0_A/SSLA1_B/ SD0DAT5_B	GTETRGB/GTIOC2A/ULPTOA0-DS	ADST1
A5	—	P301	D1/DQ1	IRQ6	TXD6_B/SDA6_B/MOSI6_B/SD0DAT2_B	GTOULO/GTIOC4B/AGTIO0/ ULPTEE0-DS	—
A6	TDI	P208	—	IRQ3	RXD9_B/SCL9_B/MISO9_B/CRX1	GTOVLO/GTIOC1B	VCOUT
A7	TMS/SWDIO	P210	—	IRQ24	CTS_RTS9_B/SS9_B/DE9	GTOULO/GTIOC0B	—
A8	VLO	—	—	—	—	—	—

Table 1.16 Pin list for the SiP product (2 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
A9	VLO	—	—	—	—	—	—
A10	VSS_DCDC	—	—	—	—	—	—
A11	VCC_DCDC	—	—	—	—	—	—
A12	VCC_DCDC	—	—	—	—	—	—
A13	—	P309	—	IRQ25-DS	CTS9_B/ET1_GTX_CLK/RGMII1_TXC	GTCPPO8	VCOUT
A14	—	P906	—	IRQ9	CTS6_A/USB_ID/ET1_RXD0/RGMII1_RXD0/ RMII1_RXD0/CAT1_ERXD0	GTIOC13B/ULPTO1	AD0FLAG1
A15	—	P905	—	IRQ8	RXD3_B/SCL3_B/MISO3_B/ET1_RX_CLK/ RGMII1_RXC/RMII1_REF50CK/ CAT1_RX_CLK	GTCPPO13	AD1FLAG1
A16	—	P907	—	IRQ10	SCK6_A/DE6/USB_EXICEN/ET1_RXD1/ RGMII1_RXD1/RMII1_RXD1/CAT1_ERXD1	GTIOC13A/ULPTEE1	ADSYNC
A17	—	P207	—	IRQ25	ET1_RXD5	GTCPPO3	—
A18	VSS	—	—	—	—	—	—
B1	—	P813	SDCS	IRQ15	SCK7_A/DE7	GTETRGA/GTIOC7B	—
B2	—	PA12	D9/DQ9	IRQ11	RXD9_C/SCL9_C/MISO9_C	GTIW/GTIOC6B	—
B3	—	P115	D6/DQ6	IRQ31-DS	CTS0_A/MOSIA_B/SD0DAT7_B	GTETRGD/GTIOC5A	AD0FLAG1
B4	—	PA11	D8/DQ8	IRQ10	SCK9_C/DE9	GTIV/GTIOC6A	—
B5	—	P112	D3/DQ3	IRQ27	TXD0_A/SDA0_A/MOSI0_A/SSLA2_B/ SD0DAT4_B	GTETRGA/GTIOC3B/ULPTOB0-DS	ADST0
B6	TDO/SWO/CLKOUT	P209	—	IRQ25	TXD9_B/SDA9_B/MOSI9_B/CTX1	GTOVUP/GTIOC1A	—
B7	TCK/SWCLK	P211	—	IRQ23	SCK9_B/DE9	GTOUUP/GTIOC0A	—
B8	VLO	—	—	—	—	—	—
B9	VLO	—	—	—	—	—	—
B10	VSS_DCDC	—	—	—	—	—	—
B11	VCC_DCDC	—	—	—	—	—	—
B12	VCC_DCDC	—	—	—	—	—	—
B13	—	P311	—	IRQ23-DS	SCK3_B/DE3/CRX0/ET1_TX_CLK/ CAT1_TX_CLK	GTADSM1/GTCPPO6/AGTOB1	—
B14	—	P908	—	IRQ11	TXD6_A/SDA6_A/MOSI6_A/CRX1/ USB_OVRCURB/ET1_RXD2/RGMII1_RXD2/ CAT1_ERXD2	GTIOC12B/ULPTEVI1	ADST1
B15	—	P909	—	IRQ21-DS	RXD6_A/SCL6_A/MISO6_A/CTX1/ USB_OVRCURA/ET1_RXD3/RGMII1_RXD3/ CAT1_ERXD3	GTIOC12A/ULPTOA1	ADST0
B16	—	P904	—	IRQ2	ET1_RXD4	GTIOC11B	—
B17	—	PD01	—	IRQ22	SCK8_C/DE8/SD0DAT2_C/ET1_RXD6	GTCPPO2	—
B18	—	PD02	—	IRQ21	TXD8_C/SDA8_C/MOSI8_C/SD0DAT1_C/ ET1_RXD7	GTCPPO1	—
C1	—	PA06	CS1/CKE	IRQ17	CTS2_C/SD0DAT1_A	GTETRGC/GTIOC7B	—
C2	—	P613	D15/DQ15	IRQ19	CTS0_C	GTETRGA/GTIOC9B/AGTO1	—
C3	—	PA13	D10/DQ10	IRQ12	CTS_RTS9_C/SS9_C/DE9	GTOVUP/GTIOC10A	—
C4	—	P300	D2/DQ2	IRQ4	SCK0_A/DE0/SSLA3_B/SD0DAT3_B	GTIOC3A/ULPTEVI0-DS	—
C5	—	P302	D0/DQ0	IRQ5	RXD6_B/SCL6_B/MISO6_B/SD0DAT1_B	GTOUUP/GTIOC4A/ULPTO0-DS	—
C6	—	P200	—	NMI	—	—	—
C7	RES	—	—	—	—	—	—
C8	—	P110	—	IRQ20	SD0DAT4_C	GTIOC9B	—
C9	—	P903	—	IRQ1	—	GTIOC11A	—
C10	TCLK	P308	—	IRQ26-DS	CTS3_B/SD0CLK_B/ET1_TX_ER/ ETHPHYCLK	GTIU/GTCPPO9/ULPTOB1	—
C11	TDATA2	P305	—	IRQ8	SD0WP/ET1_TXD2/RGMII1_TXD2/ CAT1_ETXD2	GTOVUP/GTCPPO12/ULPTEE1	—
C12	TDATA0	P307	—	IRQ27-DS	CTS_RTS6_A/SS6_A/DE6/SD0CMD_B/ ET1_TXD0/RGMII1_TXD0/RMII1_TXD0/ CAT1_ETXD0	GTIV/GTCPPO10/ULPTOA1	—
C13	—	P911	—	IRQ6	ET1_TXD5	GTIOC3B	—
C14	CLKOUT	P206	CS7	IRQ0-DS	USB_VBUSEN/SD0DAT7_C/ET1_RX_DV/ RGMII1_RX_CTL/RMII1_CRS_DV/ CAT1_RX_DV	GTIU/GTCPPO0/ULPTOB1	—

Table 1.16 Pin list for the SiP product (3 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
C15	—	PD04	—	IRQ20	CTS_RTS8_C/SS8_C/DE8/SD0CMD_C/ ET0_RXD5	GTIOC3A	—
C16	—	PD03	—	IRQ21	RXD8_C/SCL8_C/MISO8_C/SD0DAT0_C/ ET0_RXD4	GTIOC3B	—
C17	—	PD05	—	IRQ19	CTS8_C/SD0CLK_C/ET0_RXD6	GTIOC2B	—
C18	—	PD06	—	IRQ18	SD0WP/ET0_RXD7	GTIOC2A	—
D1	—	PA04	A1	IRQ19	SCK2_C/DE2/SD0DAT3_A	GTIU/GTIOC4B	ADST0
D2	CACREF/CLKOUT	P611	D13/DQ13	IRQ17	SCK0_C/DE0/MOSIA_B	GTOULO/GTIOC4B	—
D3	—	P610	D12/DQ12	IRQ16	RXD0_C/SCL0_C/MISO0_C/RSPCKA_B/ CRX1	GTOUUP/GTIOC4A/ULPTOB1-DS	—
D4	—	PA14	D11/DQ11	IRQ13	TXD9_C/SDA9_C/MOSI9_C	GTOVLO/GTIOC10B	—
D5	—	P303	—	IRQ29-DS	SCK6_B/DE6	GTIOC7B	—
D6	—	P915	—	IRQ8	CTS6_B	GTIOC5A	—
D7	—	P108	—	IRQ24	SD0DAT6_C	GTIOC10B	—
D8	—	P111	—	IRQ19	SD0DAT3_C	GTIOC9A	—
D9	—	P109	—	IRQ23	SD0DAT5_C	GTIOC10A	—
D10	—	P310	—	IRQ24-DS	TXD3_B/SDA3_B/MOSI3_B/ET1_TX_EN/ RGMII1_TX_CTL/RMII1_TX_EN/ CAT1_TX_EN	GTCPPO7/AGTEE1	—
D11	TDATA3	P304	—	IRQ9	SD0DAT0_B/ET1_TXD3/RGMII1_TXD3/ CAT1_ETXD3	GTOVLO/GTIOC7A/ULPTO1	—
D12	TDATA1	P306	—	IRQ28-DS	SD0CD/ET1_TXD1/RGMII1_TXD1/ RMII1_TXD1/CAT1_ETXD1	GTIW/GTCPPO11/ULPTEVI1	—
D13	—	P912	—	IRQ5	ET1_TXD6	GTIOC3A	—
D14	—	PB04	—	IRQ9	SCK5_C/DE5/ET0_TXD3/RGMII0_TXD3/ CAT0_ETXD3	GTCPPO3	AD0FLAG1
D15	—	PB07	—	IRQ1	ET0_TXD5	GTIOC9B	—
D16	—	PB05	—	IRQ15	CTS5_C/ET0_TXD7	GTCPPO4	—
D17	—	PB03	—	IRQ13	TXD5_C/SDA5_C/MOSI5_C/ET0_TXD2/ RGMII0_TXD2/CAT0_ETXD2	GTCPPO1	ADSYNC
D18	—	PB01	ALE	IRQ12	CTS_RTS1_B/SS1_B/DE1/ET0_TX_CLK/ CAT0_TX_CLK	GTCPPO2	AD1FLAG1
E1	—	PA15	EBCLK/ SDCLK	IRQ14	CTS9_C	GTIOC7A	—
E2	—	P615	—	IRQ7	TXD7_A/SDA7_A/MOSI7_A	GTETRGC/GTCPPO10	—
E3	—	P614	WR/WR0/ DQM0	IRQ20	RXD7_A/SCL7_A/MISO7_A	GTETRGB/GTCPPO9/AGTO0	—
E4	—	P612	D14/DQ14	IRQ18	CTS_RTS0_C/SS0_C/DE0/SSLA0_B	GTIOC9A	—
E5	—	P914	—	IRQ9	CTS_RTS6_B/SS6_B/DE6	GTIOC5B	—
E6	MD	P201	—	IRQ4	—	—	—
E10	—	P902	ALE	IRQ0	ETHPHYCLK	GTCPPO13	—
E11	—	P312	—	IRQ22-DS	CTS_RTS3_B/SS3_B/DE3/CTX0/ ET1_RX_ER/RMII1_RX_ER/CAT1_RX_ER	GTADSM0/GTCPPO5/AGTOA1	—
E12	—	P910	—	IRQ7	ET1_TXD4	GTCPPO12	—
E13	CLKOUT	P913	—	IRQ3	ET1_TXD7	GTCPPO11	—
E14	—	PB02	—	IRQ11	RXD5_C/SCL5_C/MISO5_C/ET0_TXD1/ RGMII0_TXD1/RMII0_TXD1/CAT0_ETXD1	GTCPPO0	ADST1
E15	—	PB06	—	IRQ0	CTS_RTS5_C/SS5_C/DE5/ET0_TXD6	GTIOC9A	—
E16	—	PD07	—	IRQ17	SD0CD/ET0_TXD4	GTCPPO0	—
E17	—	PB00	—	IRQ10	SCK1_B/DE1/ET0_TXD0/RGMII0_TXD0/ RMII0_TXD0/CAT0_ETXD0/DSM1CLK2	GTCPPO4	ADST0
E18	—	P706	—	IRQ7	RXD1_B/SCL1_B/MISO1_B/ET0_GTX_CLK/ RGMII0_TXC/ETHPHYCLK/DSM1CLK0	GTCPPO2/AGTIO0	—
F1	—	PA02	A3	IRQ31	RXD2_C/SCL2_C/MISO2_C/SD0DAT5_A	GTIW/GTCPPO9	ADSYNC
F2	—	PA10	CS2/RAS	IRQ4	SCK5_B/DE5	GTCPPO13	—
F3	—	PA08	CS0/WE	IRQ6	RXD5_B/SCL5_B/MISO5_B	GTETRGD/GTCPPO11	—
F4	—	PA09	CS3/CAS	IRQ5	TXD5_B/SDA5_B/MOSI5_B	GTCPPO12	—
F5	—	PC14	—	IRQ0	TXD6_C/SDA6_C/MOSI6_C/ET0_WOL/ DSM1DAT1	GTADSM1/GTCPPO9	—

Table 1.16 Pin list for the SiP product (4 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
F7	VCC_08	—	—	—	—	—	—
F8	VSS_08	—	—	—	—	—	—
F9	VSS3	—	—	—	—	—	—
F10	VCL3	—	—	—	—	—	—
F11	VSS_07	—	—	—	—	—	—
F12	VCC_07	—	—	—	—	—	—
F13	—	P700	—	IRQ16-DS	RXD2_B/SCL2_B/MISO2_B/MISOA_C/ SD1WP/ET0_RXD2/RGMII0_RXD2/ CAT0_ERXD2/DSM0CLK0	GTIOC5A	—
F14	—	P702	—	IRQ18-DS	CTS2_B/RSPCKA_C/SD1DAT5_B/ ET0_RXD0/RGMII0_RXD0/RMII0_RXD0/ CAT0_ERXD0/DSM0CLK2	GTIOC6A/ULPTO0	—
F15	—	P406	—	IRQ31	TXD2_B/SDA2_B/MOSI2_B/SSLA3_C/ SD1CD/ET0_RXD3/RGMII0_RXD3/ CAT0_ERXD3/DSM0DAT2	GTIOC1B	—
F16	—	P701	—	IRQ17-DS	CTS_RTS2_B/SS2_B/DE2/MOSIA_C/ SD1DAT4_B/ET0_RXD1/RGMII0_RXD1/ RMII0_RXD1/CAT0_ERXD1/DSM0CLK1	GTIOC5B/ULPTO1	—
F17	—	P707	—	IRQ8	TXD1_B/SDA1_B/MOSI1_B/ET0_TX_ER/ ETHPHYCLK/DSM1CLK1	GTCPPO3	—
F18	—	P705	—	IRQ19	CTS1_B/SSLA2_C/CRX0/ET0_TX_EN/ RGMII0_TX_CTL/RMII0_TX_EN/ CAT0_TX_EN/DSM1DAT2	GTADSM1/GTCPPO1/AGTIO0	—
G1	—	PA00	A5	IRQ22	CTS_RTS5_B/SS5_B/DE5/SD0DAT7_A	GTOVLO/GTCPPO7	AD1FLAG1
G2	—	PA03	A2	IRQ20	TXD2_C/SDA2_C/MOSI2_C/SD0DAT4_A	GTIV/GTCPPO10	ADST1
G3	—	PA05	A0/BC0/ DQM1	IRQ18	CTS_RTS2_C/SS2_C/DE2/SD0DAT2_A	GTETRGD/GTIOC4A	—
G4	—	PA07	RD	IRQ16	CTS7_A/SD0DAT0_A	GTETRGB/GTIOC7A	VCOUT
G5	—	PC12	—	IRQ2	SCK6_C/DE6/ET0_MDIO/CAT0_MDIO/ DSM1CLK0	GTCPPO11	—
G7	VCC_09	—	—	—	—	—	—
G8	VSS_09	—	—	—	—	—	—
G9	VSS4	—	—	—	—	—	—
G10	VCL4	—	—	—	—	—	—
G11	VSS_06	—	—	—	—	—	—
G12	VCC_06	—	—	—	—	—	—
G13	—	P405	—	IRQ30	SCK2_B/DE2/SD1DAT3_B/ET0_RX_DV/ RGMII0_RX_CTL/RMII0_CRS_DV/ CAT0_RX_DV/DSM0DAT1	GTIOC1A/AGTIO1	—
G14	—	P704	—	IRQ26	SSLA1_C/CTX0/SD1DAT7_B/ET0_RX_ER/ RMII0_RX_ER/CAT0_RX_ER/DSM1DAT1	GTADSM0/GTCPPO0/AGTO0	—
G15	—	P703	—	IRQ19-DS	SSLA0_C/SD1DAT6_B/ET0_RX_CLK/ RGMII0_RXC/RMII0_REF50CK/ CAT0_RX_CLK/DSM1DAT0	GTIOC6B/AGTO1	VCOUT
G16	—	PB14	—	IRQ10	CATSYNC0	—	—
G17	—	PB12	—	IRQ6	CATLINKACT0	—	—
G18	—	PB11	—	IRQ5	CATLEDERR	—	—
H1	—	P504	A7	IRQ7	SD0WP	GTOULO/GTCPPO1	—
H2	—	P503	A6	IRQ6	SD0CD	GTOUUP/GTCPPO6	—
H3	—	P505	A8	IRQ8	SD0CLK_A	GTOWUP/GTCPPO2	—
H4	—	PA01	A4	IRQ21	CTS5_B/SD0DAT6_A	GTOVUP/GTCPPO8	AD0FLAG1
H5	—	PC11	—	IRQ3	CTS_RTS6_C/SS6_C/DE6/ET0_MDC/ CAT0_MDC/DSM1CLK1	GTCPPO12	—
H7	VCC_10	—	—	—	—	—	—
H8	VSS_10	—	—	—	—	—	—
H9	VSS7	—	—	—	—	—	—
H10	VCL5	—	—	—	—	—	—
H11	VSS5	—	—	—	—	—	—
H12	VCC_04	—	—	—	—	—	—
H13	VSS_04	—	—	—	—	—	—

Table 1.16 Pin list for the SiP product (5 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
H15	VCC_05	—	—	—	—	—	—
H16	—	PB09	—	IRQ13	CATIRQ	—	—
H17	—	PB10	—	IRQ4	CATLEDSTER	—	—
H18	—	PB13	—	IRQ7	CATLINKACT1	—	—
J1	—	P506	A9	IRQ9	SD0CMD_A	GTOWLO/GTCPPO3	—
J2	—	P507	A10	IRQ10	CTS_RTS7_A/SS7_A/DE7/ET_TAS_STA0	GTADSM0/GTIOC0A	—
J3	—	P508	A11	IRQ1	CTS5_A/ET_TAS_STA1	GTADSM1/GTIOC0B	—
J4	—	P509	A12	IRQ2	CTS_RTS5_A/SS5_A/DE5/ET_TAS_STA2	GTIOC1A/ULPTEVI1	—
J5	—	PC13	—	IRQ1	RXD6_C/SCL6_C/MISO6_C/ET0_INT/ DSM1DAT2	GTCPPO10	—
J7	VCC2_11	—	—	—	—	—	—
J8	VSS_11	—	—	—	—	—	—
J9	VCL7	—	—	—	—	—	—
J10	VCL6	—	—	—	—	—	—
J11	VSS6	—	—	—	—	—	—
J12	VCL2	—	—	—	—	—	—
J13	VSS2	—	—	—	—	—	—
J15	—	PB08	—	IRQ12	CATLEDRUN	—	—
J16	VSS_05	—	—	—	—	—	—
J17	VSS_03	—	—	—	—	—	—
J18	VSS_02	—	—	—	—	—	—
K1	—	PC15	A16	IRQ30	CTS6_C/CRX1	GTADSM0	—
K2	CACREF	P608	A14	IRQ22	TXD5_A/SDA5_A/MOSI5_A	GTOWUP/GTCPPO4	—
K3	—	P510	A13	IRQ3	RXD5_A/SCL5_A/MISO5_A/ET_TAS_STA3	GTIOC1B/ULPTEVI0	—
K4	—	PD00	A15	IRQ23	SCK5_A/DE5/CTX1	GTOWLO/GTCPPO5	—
K5	VSS	—	—	—	—	—	—
K6	VSS	—	—	—	—	—	—
K7	VSS_12	—	—	—	—	—	—
K8	VSS9	—	—	—	—	—	—
K9	VCL9	—	—	—	—	—	—
K10	VCL8	—	—	—	—	—	—
K11	VSS8	—	—	—	—	—	—
K12	VCL1	—	—	—	—	—	—
K13	VSS1	—	—	—	—	—	—
K15	VCC_03	—	—	—	—	—	—
K16	VCC_02	—	—	—	—	—	—
K17	XTAL	P213	—	IRQ2	TXD1_C/SDA1_C/MOSI1_C	GTETRGC/GTIOC0A/ULPTEE0	ADTRG1
K18	EXTAL	P212	—	IRQ3	RXD1_C/SCL1_C/MISO1_C	GTETRGD/GTIOC0B/AGTEE1	—
L1	—	PC10	—	IRQ4	DSM1CLK2	GTCPPO13	—
L2	VSS	—	—	—	—	—	—
L3	PUP	—	—	—	—	—	—
L4	VCC2_16	—	—	—	—	—	—
L5	VSS_16	—	—	—	—	—	—
L7	VCC2_12	—	—	—	—	—	—
L8	VSS_14	—	—	—	—	—	—
L9	VSS_15	—	—	—	—	—	—
L10	VSS10	—	—	—	—	—	—
L11	VCL10	—	—	—	—	—	—
L12	VCL0	—	—	—	—	—	—
L13	VSS0	—	—	—	—	—	—
L14	—	P403	—	IRQ14-DS	CTS_RTS1_A/SS1_A/DE1/SD1DAT1_B/ ET1_WOL/CATI2CCLK	GTIOC3A/RTCIC1	AD0FLAG1

Table 1.16 Pin list for the SiP product (6 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
L15	—	P404	—	IRQ15-DS	CTS1_A/SD1DAT2_B/ET0_WOL/ CATI2CDATA/DSM0DAT0	GTIOC3B/RTCIC2	AD1FLAG1
L16	VCC_01	—	—	—	—	—	—
L17	XCOUT	P214	—	IRQ21	—	—	—
L18	XCIN/EXCIN	P215	—	IRQ20	—	—	—
M1	—	PC09	—	IRQ5	—	—	—
M2	VSS	—	—	—	—	—	—
M3	VSS	—	—	—	—	—	—
M4	VCC2_17	—	—	—	—	—	—
M5	VSS_17	—	—	—	—	—	—
M8	VCC2_14	—	—	—	—	—	—
M9	VCC2_15	—	—	—	—	—	—
M11	VSS11	—	—	—	—	—	—
M12	VCL11	—	—	—	—	—	—
M14	—	P414	A23	IRQ9	RXD4_B/SCL4_B/MISO4_B/SSLB0_B/CRX1/ ET1_MDIO/CATLATCH1	GTIOC0B	—
M15	CACREF	P402	—	IRQ4-DS	SCK1_A/DE1/CRX0/SD1DAT0_B/ ET0_LINKSTA/CAT0_LINKSTA	RTCIC0	—
M16	—	P410	A19	IRQ5	SCK3_A/DE3/SCL0_A[*1]/USB_OVRCURB-DS/GPTP_MATCH0/CATI2CCLK	GTOVLO/GTIOC9B/AGTOB1	ADST0
M17	VBATT	—	—	—	—	—	—
M18	VSS_01	—	—	—	—	—	—
N1	—	PC08	—	IRQ29	DSM1DAT0	GTCPPO8	—
N2	VSS	—	—	—	—	—	—
N3	VSS	—	—	—	—	—	—
N4	VCC2_18	—	—	—	—	—	—
N5	VSS_18	—	—	—	—	—	—
N7	—	P105	—	IRQ0	CTS_RTS8_B/SS8_B/DE8/SSLB2_A/ OM_0_ECSINT1/DSM0DAT0	GTIOC1A/ULPTO1-DS	ADSYNC
N10	—	P810	—	IRQ21	SCK7_B/DE7/SD1DAT2_A	GTIOC10A/ULPTOA0	—
N14	—	P710	CS5	IRQ17	CTS4_B/SSLB3_B/ET0_LINKSTA/ CAT0_LINKSTA	GTIOC11B	—
N15	CACREF	P411	A20	IRQ4	CTS_RTS3_A/SS3_A/DE3/USB_ID/ GPTP_PTPOUT1	GTOVUP/GTIOC9A/AGTOA1	—
N16	—	P408	A17	IRQ7	RXD3_A/SCL3_A/MISO3_A/SCL0_B[*1]/ USB_VBUSEN/GPTP_PTPOUT2/ CATRESETOUT	GTOWLO/GTIOC10A/ULPTOB0	ADSYNC
N17	—	P412	A21	IRQ20-DS	CTS3_A/USB_EXICEN/GPTP_PTPOUT0	GTOULO/GTCPPO8/AGTEE1	—
N18	—	P401	—	IRQ5-DS	RXD1_A/SCL1_A/MISO1_A/I3C_SDA0/ CTX0/SD1CMD_B	GTETRGA/GTIOC6B	—
P1	VSS	—	—	—	—	—	—
P2	VSS	—	—	—	—	—	—
P3	VSS	—	—	—	—	—	—
P4	VCC2_19	—	—	—	—	—	—
P5	VSS_19	—	—	—	—	—	—
P6	—	P104	—	IRQ1	CTS9_A/SSLB1_A/OM_0_CS1/DSM0DAT1	GTETRGB/GTIOC1B	AD0FLAG1
P7	—	P107	—	IRQ31	CTS4_A/OM_0_CS0	GTOWUP/GTIOC8A/AGTOA0	ADST0
P8	—	P106	—	IRQ16	CTS8_B/SSLB3_A/OM_0_RESET	GTOWLO/GTIOC8B/AGTOB0/ ULPTEE1-DS	ADST1
P9	—	P811	—	IRQ22	CTS7_B/USB_ID/SD1DAT3_A	GTIOC10B/ULPTOB0	—
P10	—	P013	—	IRQ14	—	—	AN013
P11	—	P011	—	IRQ16	—	—	AN011
P12	—	P807	—	IRQ11	—	GTIOC13A	—
P13	CACREF	P708	WR1/BC1	IRQ11	SCK4_B/DE4/SDA2_A[*1]/MOSIB_B/ ET0_MDC/CAT0_MDC	GTCPPO6	—
P14	—	P712	—	IRQ2	CTS1_C/SSLB1_B/GPTP_CAPTURE1/ CATLATCH1	GTIOC2B/AGTOB0	—

Table 1.16 Pin list for the SiP product (7 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
P15	—	P714	—	IRQ13	TXD4_C/SDA4_C/MOSI4_C/GPTP_PPS1/ CATSYNC1	GTIOC12B	—
P16	—	P711	—	IRQ3	CTS_RTS1_C/SS1_C/DE1/SSLB2_B/ GPTP_PPS0/CATRESETOUT	GTIOC11A/AGTEE0	—
P17	—	P713	—	IRQ14	CTS4_C/GPTP_MATCH1/CATLATCH0	GTIOC2A/AGTOA0	—
P18	—	P400	—	IRQ0	TXD1_A/SDA1_A/MOSI1_A/I3C_SCL0/ SD1CLK_B	GTIOC6A/AGTIO1	ADTRG1
R1	—	P602	—	IRQ28	RXD0_B/SCL0_B/MISO0_B	GTIOC7B/ULPTEE0	—
R2	VSS	—	—	—	—	—	—
R3	VSS	—	—	—	—	—	—
R4	CACREF	P600	—	IRQ30	OM_0_RSTO1	GTIOC6B/ULPTEVI1-DS	—
R5	—	P601	—	IRQ29	SCK0_B/DE0/OM_0_WP1	GTIOC6A/ULPTEVI0/RTCOUT	—
R6	—	P102	—	IRQ17	TXD9_A/SDA9_A/MOSI9_A/RSPCKB_A/ CRX0/OM_0_SIO4/DSM0CLK0	GTOWLO/GTIOC2B/AGTO0	ADTRG0
R7	—	P801	—	IRQ12	TXD2_A/SDA2_A/MOSI2_A/OM_0_DQS/ DSM1DAT1	GTIV/GTIOC11B/AGTOB0	—
R8	—	P803	—	IRQ19	SCK2_A/DE2/OM_0_SIO1/DSM1CLK0	GTETRGC/GTIOC12B	—
R9	—	P812	—	IRQ23	CTS_RTS7_B/SS7_B/DE7/USB_EXICEN/ SD1DAT4_A	GTIOC11A	AN022
R10	—	P012	—	IRQ15	—	—	AN012
R11	—	P010	—	IRQ14	—	—	AN010
R12	—	P009	—	IRQ13-DS	—	—	AN009/ IVREF1
R13	—	P805	—	IRQ30	TXD8_A/SDA8_A/MOSI8_A/ET1_MDIO	—	AN017/ IVCMP0
R14	—	P512	—	IRQ14	CTS8_A/SCL1_A[*1]/CTX1/ET1_INT	GTIOC0A	—
R15	—	P413	A22	IRQ18	ET_TAS_STA3	GTOUUP/GTCPPO7/ULPTEE1	—
R16	—	P515	—	IRQ12	CTS_RTS4_C/SS4_C/DE4/SCL2_B[*1]/ ET_TAS_STA0	GTIOC13A	—
R17	—	P709	CS4	IRQ10	CTS_RTS4_B/SS4_B/DE4/SCL2_A[*1]/ MISOB_B/ET0_MDIO/CAT0_MDIO	GTCPPO5	—
R18	—	P407	CS6	IRQ22	SCK1_C/DE1/SDA0_B[*1]/USB_VBUS/ GPTP_PTPOUT3/CATSYNC1	GTIOC10B/AGTIO0/RTCOUT	ADTRG0
T1	Vpp	—	—	—	—	—	—
T2	VSS	—	—	—	—	—	—
T3	—	P315	—	IRQ29	SCK3_C/DE3/SSLA3_A	—	—
T4	—	P900	—	IRQ30	CTS3_C	GTADSM0	—
T5	—	P103	—	IRQ16	CTS_RTS9_A/SS9_A/DE9/SSLB0_A/CTX0/ OM_0_SIO2/DSM0DAT2	GTOWUP/GTIOC2A	AD1FLAG1
T6	—	P101	—	IRQ1	RXD9_A/SCL9_A/MISO9_A/MOSIB_A/ OM_0_SIO3/DSM0CLK1	GTETRGB/GTIOC8A/AGTEE0	—
T7	—	P802	—	IRQ18	RXD2_A/SCL2_A/MISO2_A/OM_0_SIO6/ DSM1DAT2	GTIW/GTIOC12A	—
T8	—	P804	—	IRQ14	CTS_RTS2_A/SS2_A/DE2/OM_0_SIO7/ DSM1CLK1	GTETRGD/GTIOC13A	—
T9	—	P501	—	IRQ25	TXD8_B/SDA8_B/MOSI8_B/ USB_OVRCURA/SD1DAT6_A	GTIOC12A	AN020
T10	AVCC0	—	—	—	—	—	—
T11	AVSS0	—	—	—	—	—	—
T12	—	P005	—	IRQ10-DS	—	—	AN005/ IVCMP3
T13	—	P003	—	IRQ29	—	—	AN003/ IVCMP3
T14	—	P513	—	IRQ31	SCK8_A/DE8/ET0_INT	GTIOC13B	AN016/ IVCMP0
T15	—	P514	—	IRQ13	SCK4_C/DE4/SDA2_B[*1]/ET_TAS_STA1	GTIOC13B	—
T16	—	P415	WAIT	IRQ8	TXD4_B/SDA4_B/MOSI4_B/RSPCKB_B/ CTX1/ET1_MDC/CATLATCH0	GTIOC0A	—
T17	—	P409	A18	IRQ6	TXD3_A/SDA3_A/MOSI3_A/SDA0_A[*1]/ USB_OVRCURA-DS/GPTP_CAPTURE0/ CATI2CDATA	GTOWUP/ULPTOA0	ADST1

Table 1.16 Pin list for the SiP product (8 of 8)

BGA303	Power, System, Clock, Debug, CAC	I/O ports	ExBus/ SDRAM	Ex.Interrupt	SCI/IIC/I3C/SPI/CANFD/USBFS/OSPI/ SDHI/MMC/ESWM(GMII, RGMII, MII, RMII)/ EtherCAT/DSMIF	GPT/AGT/ULPT/RTC	ADC16H/ DAC12/ ACMPHS
T18	VCC_USB	—	—	—	—	—	—
U1	VCC2_13	—	—	—	—	—	—
U2	CLKOUT	P205	—	IRQ1-DS	TXD4_A/SDA4_A/MOSI4_A/SCL1_B*1/ SSLA1_A/USB_OVRCURA/SD1CD	GTIV/GTIOC4A/AGTO1	—
U3	—	P203	—	IRQ2-DS	RXD4_A/SCL4_A/MISO4_A/RSPCKA_A/ CTX0/USB_VBUSEN/SD1CLK_A	GTIOC5A/ULPTOA1	—
U4	—	P313	—	IRQ27	TXD3_C/SDA3_C/MOSI3_C/MISOA_A/ USB_ID/SD1DAT0_A	—	—
U5	—	P901	—	IRQ31	CTS_RTS3_C/SS3_C/DE3	GTADSM1/AGTIO1	—
U6	—	P809	—	IRQ20	TXD7_B/SDA7_B/MOSI7_B/OM_0_SCLKN	—	—
U7	—	P800	—	IRQ11	CTS2_A/OM_0_SIO5/DSM1DAT0	GTIU/GTIOC11A/AGTOA0	—
U8	—	P502	—	IRQ26	SCK8_B/DE8/USB_OVRCURB/SD1DAT7_A	GTIOC12B	AN019
U9	—	P014	—	IRQ27	—	—	AN014/DA0/ IVCMP0
U10	VREFL	—	—	—	—	—	—
U11	VREFL0	—	—	—	—	—	—
U12	—	P004	—	IRQ9-DS	—	—	AN004/ IVCMP2
U13	—	P007	—	IRQ28	—	—	AN007/ IVCMP3
U14	—	P001	—	IRQ7-DS	—	—	AN001/ IVCMP3
U15	—	P806	—	IRQ0	RXD8_A/SCL8_A/MISO8_A/ET1_MDC	—	AN018
U16	—	P715	—	IRQ12	RXD4_C/SCL4_C/MISO4_C/ET_TAS_STA2	GTIOC12A	—
U17	—	P815	—	IRQ15	CTX0/USB_DM	GTIOC8A	—
U18	VSS_USB	—	—	—	—	—	—
V1	VSS	—	—	—	—	—	—
V2	CACREF	P204	—	IRQ26	SCK4_A/DE4/SDA1_B*1/SSLA0_A/ USB_OVRCURB/SD1WP	GTIW/GTIOC4B/AGTIO1	—
V3	—	P202	—	IRQ3-DS	CTS_RTS4_A/SS4_A/DE4/MOSIA_A/CRX0/ USB_EXICEN/SD1CMD_A	GTIOC5B/ULPTOB1	—
V4	—	P314	—	IRQ28	RXD3_C/SCL3_C/MISO3_C/SSLA2_A/ SD1DAT1_A	—	ADTRG0
V5	VSS_13	—	—	—	—	—	—
V6	—	P808	—	IRQ15	RXD7_B/SCL7_B/MISO7_B/OM_0_SCLK/ DSM1CLK2	GTIOC13B	—
V7	—	P100	—	IRQ2	SCK9_A/DE9/MISOB_A/OM_0_SIO0/ DSM0CLK2	GTETRGA/GTIOC8B/AGTIO0	—
V8	CACREF	P500	—	IRQ24	RXD8_B/SCL8_B/MISO8_B/USB_VBUSEN/ SD1DAT5_A	GTIOC11B	AN021
V9	—	P015	—	IRQ13	—	—	AN015/DA1/ IVCMP0
V10	VREFH	—	—	—	—	—	—
V11	VREFH0	—	—	—	—	—	—
V12	—	P008	—	IRQ12-DS	—	—	AN008/ IVREF0
V13	—	P006	—	IRQ11-DS	—	—	AN006/ IVCMP2
V14	—	P000	—	IRQ6-DS	—	—	AN000/ IVCMP2
V15	—	P002	—	IRQ8-DS	—	—	AN002/ IVCMP2
V16	—	P511	—	IRQ15	CTS_RTS8_A/SS8_A/DE8/SDA1_A*1/CRX1/ ET1_LINKSTA/CAT1_LINKSTA	GTIOC0B	—
V17	—	P814	—	IRQ16	CRX0/USB_DP	GTIOC8B	—
V18	VSS	—	—	—	—	—	—

Note: Several pin names have the added suffix of _A, _B, and _C. These suffixes have special conditions for electrical characteristics.
Note 1. There are two types for IIC function, one is a simple IIC by SCI and another is a dedicated IIC. This terminal is for a dedicated IIC.

2. Electrical Characteristics

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

Supported peripheral functions and pins differ from one product name to another.

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = VCC_DCDC = VBATT = 1.62 to 3.63 V
- VCC2 = 1.62 to 3.63 V for Standard Product
- VCC2 = 1.70 to 2.00 V for SiP Product
- AVCC0 = 1.62 to 3.63 V
- VCC_USB = 3.0 to 3.6 V
- VREFH0/VREFH = 1.62 V to AVCC0
- VSS = VSS_DCDC = AVSS0 = VREFL0/VREFL = VSS_USB = 0 V
- VCC voltage is lower than 2.7 V : LVOCR.LVO0E = 1, otherwise LVOCR.LVO0E = 0
- VCC2 voltage is lower than 2.7 V : LVOCR.LVO1E = 1, otherwise LVOCR.LVO1E = 0
- $T_j = T_{opj}$
  When not specified otherwise, typical values are measured at room temperature of 25 °C and VCC = VCC_DCDC = VCC_USB = VBATT = AVCC0 = VREFH0 = VREFH = 3.3V

Figure 2.1 shows the timing conditions.

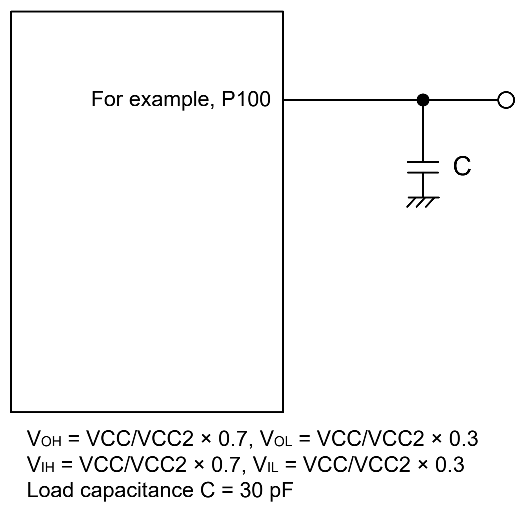


Figure 2.1 Input or output timing measurement conditions

The recommended measurement conditions for the timing specification of each peripheral provided are for the best peripheral operation. Make sure to adjust the driving abilities of each pin to meet your conditions.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter	Symbol		Value	Unit
Power supply voltage	VCC, VCC_DCDC*2		−0.3 to +4.0	V
	VCC2	Standard Product	−0.3 to +4.0	V
		SiP Product	−0.3 to +2.5	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
External power supply voltage *6	VCL	−0.3 to +1.2	V
VBATT power supply voltage	VBATT	−0.3 to +4.0	V
Input voltage (except for 5 V-tolerant ports *1)	V_{in}	−0.3 to VCC + 0.3, −0.3 to VCC2 + 0.3, −0.3 to VCC_USB + 0.3 or −0.3 to VBATT_R + 0.3	V
Input voltage (5 V-tolerant ports *1)	V_{in}	−0.3 to + VCC + 4.0 (max. 5.8) or −0.3 to + VCC2 + 4.0 (max. 5.8)	V
Reference power supply voltage	VREFH/VREFH0	−0.3 to AVCC0 + 0.3	V
USBFS power supply voltage	VCC_USB	−0.3 to +4.0	V
Analog power supply voltage	AVCC0	−0.3 to +4.0	V
Analog input voltage	V_{AN}	−0.3 to AVCC0 + 0.3	V
Operating junction temperature *3 *4 *5	T_{opj}	0 to 95 or −40 to +105 or −40 to +125	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note 1. Ports P204, P205, P303, P407 to P413, P511, P512, P514, P515 and P708 to P715 are 5 V tolerant.
Note 2. Connect VCC_DCDC to VCC.
Note 3. See section 2.2.1. Tj/Ta Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when Tj = +95 °C to +125 °C. Derating is the systematic reduction of load for improved reliability.
Note 5. The lower and upper limit of operating junction temperature depend on the product.
Note 6. External VDD mode does not support in HLQFP package.

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Table 2.2 Recommended operating conditions

Parameter	Symbol			Min	Typ	Max	Unit
Power supply voltages	VCC, VCC_DCDC	Other than the following		1.62	—	3.63	V
		When ESC is used		2.70	—	3.60	V
		When ESWM is used		2.30	—	3.63	V
		When SDRAM is used		3.00	—	3.63	V
	VCC2	Standard Product	Other than the following	1.62	—	3.63	V
			When 32bit SDRAM is used	3.00	—	3.63	V
		SiP Product		1.70	—	2.00	V
	VCL	When external VDD is used*2*3	voltage range 1	0.92	—	0.99	V
			voltage range 2	0.87	—	0.99	V
		When DCDC is used (High-speed mode)	VSCR_1	—	0.95	—	V
			VSCR_2	—	0.925	—	V
		When DCDC is used (Software Standby mode)	SVSCR_1	—	0.95	—	V
			SVSCR_2	—	0.925	—	V
			SVSCR_3	—	0.825	—	V
			SVSCR_4	—	0.765	—	V
			SVSCR_5	—	0.715	—	V
	VSS, VSS_DCDC			—	0	—	V
USB power supply voltages	VCC_USB	When USB is not used		1.62	—	3.63	V
		When USB is used		3.00	—	3.60	V
	VSS_USB			—	0	—	V
VBATT power supply voltage	VBATT			1.62	—	3.63	V
Analog power supply voltages	AVCC0*1		Other than the following	1.62	—	3.63	V
			When Channel dedicated sample-and-hold circuit is used	2.70	—	3.63	V
	AVSS0			—	0	—	V

Note 1. When the A/D converter, the D/A converter and the High-Speed Analog Comparator are not in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.
Note 2. VCL voltage must never be higher than VCC voltage.
Note 3. External VDD mode does not support in HLQFP package.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible operating junction temperature	T_j	—	125*1	°C	High-speed mode

Note: Make sure that $T_j = T_a + θ_{ja}$ × total power consumption (W), where total power consumption = (VCC - V_{OH}) × $ΣI_{OH}$ + V_{OL} × $ΣI_{OL}$ + (I_{CC}max + I_{CC_DCDC}max) × VCC.
Note: Minimum Ambient Temperature (Ta) is -40℃ or 0℃, depending on the product.
Note 1. The upper limit of operating junction temperature is 95°C, 105°C or 125°C, depending on the product.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} except for Schmitt trigger input pins (1 of 2)

Parameter		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Peripheral function pin	EXTAL (external clock input), WAIT, SPI*1 (except RSPCK)	1.62 V or above	V_{IH}	VCC × 0.8	—	—	V
			V_{IL}	—	—	VCC × 0.2	
	SPI*2 (except RSPCK)	1.62 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
	OSPI (except OM_0_RSTO1, OM_0_ECSINT 1, OM_1_RSTO1 and OM_1_ECSINT 1)	2.70 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
		1.62 to 2.00V	V_{IH}	VCC2 × 0.7	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.3	
	SD*3	2.70 V or above	V_{IH}	VCC × 0.625	—	VCC + 0.3	
			V_{IL}	VSS − 0.3	—	VCC × 0.25	
		1.70 to 1.95 V	V_{IH}	1.27	—	2	
			V_{IL}	VSS − 0.3	—	0.58	
	SD*4	2.70 V or above	V_{IH}	VCC2 × 0.625	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.25	
		1.70 to 1.95 V	V_{IH}	1.27	—	2	
			V_{IL}	VSS − 0.3	—	0.58	
	MMC*5	2.70 V or above	V_{IH}	VCC × 0.625	—	VCC + 0.3	
			V_{IL}	VSS − 0.3	—	VCC × 0.25	
		1.70 to 1.95 V	V_{IH}	VCC × 0.65	—	VCC + 0.3	
			V_{IL}	VSS − 0.3	—	VCC × 0.35	
	MMC*6	2.70 V or above	V_{IH}	VCC2 × 0.625	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.25	
		1.70 to 1.95 V	V_{IH}	VCC2 × 0.65	—	VCC2 + 0.3	
			V_{IL}	VSS − 0.3	—	VCC2 × 0.35	
	D00 to D19, TMS, TDI, SWDIO	1.62 V or above	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
	D20 to D31	1.62 V or above	V_{IH}	VCC2 × 0.7	—	—	
			V_{IL}	—	—	VCC2 × 0.3	
	DQ00 to DQ19	3.00 V or above	V_{IH}	VCC × 0.7	—	—	
			V_{IL}	—	—	VCC × 0.3	
	DQ20 to DQ31	3.00 V or above	V_{IH}	VCC2 × 0.7	—	—	
			V_{IL}	—	—	VCC2 × 0.3	

Table 2.4 I/O V_{IH}, V_{IL} except for Schmitt trigger input pins (2 of 2)

Parameter		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Peripheral function pin	ESWM*9, ESC*13	2.30 V to 3.60 V	V_{IH}	VCC × 0.7	—	—	V
			V_{IL}	—	—	VCC × 0.3	
			V_{IH}	VCC2 × 0.7	—	—	
			V_{IL}	—	—	VCC2 × 0.3	
	ESWM (MII)*10, ESWM (RMII)*11, ESC*14	2.70 V to 3.60 V	V_{IH}	2.3	—	—	
			V_{IL}	—	—	VCC × 0.2	
	ESWM (GMII)*10, ESWM (RGMII)*12	3.00 to 3.60 V	V_{IH}	2	—	—	
			V_{IL}	—	—	0.8	
		2.30 to 2.70 V	V_{IH}	1.7	—	—	
			V_{IL}	—	—	0.7	
	IIC (SMBus)*7	2.70 V or above	V_{IH}	2.1	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
	IIC (SMBus)*8	2.70 V or above	V_{IH}	2.1	—	VCC2 + 3.6 (max 5.8)	
			V_{IL}	—	—	0.8	
	I3C (SMBus)	2.70 V or above	V_{IH}	2.1	—	VCC + 0.3	
			V_{IL}	—	—	0.8	
	RTCIC0, RTCIC1, RTCIC2, when VCC power supply is selected	1.62 V or above	V_{IH}	0.9	—	3.9	
			V_{IL}	—	—	0.3	
	RTCIC0, RTCIC1, RTCIC2 when VBATT power supply is selected		V_{IH}	0.9	—	3.9	
			V_{IL}	—	—	0.3	
	EXCIN when VCC power supply is selected	1.62 V or above	V_{IH}	0.9	—	VCC	
			V_{IL}	—	—	0.3	
	EXCIN when VBATT power supply is selected		V_{IH}	0.9	—	VBATT	
			V_{IL}	—	—	0.3	

Note 1. SPI0_B, SPI0_C and SPI1_B
Note 2. SPI0_A, SPI1_A
Note 3. SD_A ch0, SD_B ch0, SD_C ch0 and SD_B ch1
Note 4. SD_A ch1
Note 5. MMC_A ch0, MMC_B ch0, MM_C ch0 and MMC_B ch1
Note 6. MMC_A ch1
Note 7. IIC0_A, IIC0_B, IIC1_A, IIC2_A and IIC2_B
Note 8. IIC1_B
Note 9. GPTP_CAPTUREn, ETn_LINKSTA, ETn_MDIO and ETn_INT (n = 0, 1)
Note 10. ETn_RX_CLK, ETn_RX_DV, ETn_RXD7 to ETn_RXD0, ETn_RX_ER and ETn_TX_CLK (n = 0, 1)
Note 11. RMIIn_REF50CK, RMIIn_CRS_DV, RMIIn_RXD1 to RMIIn_RXD0 and RMIIn_RX_ER (n = 0, 1)
Note 12. RGMIIn_RXC, RGMIIn_RX_CTL and RGMIIn_RXD3 to RGMIIn_RXD0 (n = 0, 1)
Note 13. CATn_LINKSTA, CAT0_MDIO, CATI2CDATA and CATLATCHn (n = 0, 1)
Note 14. CATn_RX_CLK, CATn_RX_DV, CATn_ERXD3 to CATn_ERXD0, CATn_RX_ER and CATn_TX_CLK (n = 0, 1)

Table 2.5 I/O V_{IH}, V_{IL} of Schmitt trigger input pins (1 of 2)

Parameter		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Peripheral function pin	IIC (except for SMBus)*7	1.62 V or above	V_{IH}	VCC × 0.7	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.05	—	—	
	IIC (except for SMBus)*8	1.62 V or above	V_{IH}	VCC2 × 0.7	—	VCC2 + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC2 × 0.3	
			ΔV_T	VCC2 × 0.05	—	—	
	I3C (except for SMBus)	1.65 V or above	V_{IH}	VCC × 0.7	—	VCC + 0.3	
			V_{IL}	—	—	VCC × 0.3	
			ΔV_T	VCC × 0.1	—	—	
	5 V-tolerant ports*1*6	1.62 V or above	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	5 V-tolerant ports*2*6	1.62 V or above	V_{IH}	VCC2 × 0.8	—	VCC2 + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC2 × 0.2	
			ΔV_T	VCC2 × 0.05	—	—	
	Other VCC input pins*3	1.62 V or above	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	
	Other VCC2 input pins*3	1.62 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
			ΔV_T	VCC2 × 0.05	—	—	
	Other AVCC0 input pins*3	1.62 V or above	V_{IH}	AVCC0 × 0.8	—	—	
			V_{IL}	—	—	AVCC0 × 0.2	
			ΔV_T	AVCC0 × 0.05	—	—	
	Other VCC_USB input pins*3	1.62 V or above	V_{IH}	VCC_USB × 0.8	—	—	
			V_{IL}	—	—	VCC_USB × 0.2	
			ΔV_T	VCC_USB × 0.05	—	—	
	Other VBATT_R input pins when VCC power supply is selected*3	1.62 V or above	V_{IH}	VCC × 0.8	—	VCC	
			V_{IL}	—	—	VCC × 0.2	
			ΔV_T	VCC × 0.05	—	—	

Table 2.5 I/O V_{IH}, V_{IL} of Schmitt trigger input pins (2 of 2)

Parameter		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Ports	5 V-tolerant port*4*6	1.62 V or above	V_{IH}	VCC × 0.8	—	VCC + 3.6 (max 5.8)	V
			V_{IL}	—	—	VCC × 0.2	
	5 V-tolerant port*2*6	1.62 V or above	V_{IH}	VCC2 × 0.8	—	VCC2 + 3.6 (max 5.8)	
			V_{IL}	—	—	VCC2 × 0.2	
	Other VCC input pins*5	1.62 V or above	V_{IH}	VCC × 0.8	—	—	
			V_{IL}	—	—	VCC × 0.2	
	Other VCC2 input pins*5	1.62 V or above	V_{IH}	VCC2 × 0.8	—	—	
			V_{IL}	—	—	VCC2 × 0.2	
	Other AVCC0 input pins*5	1.62 V or above	V_{IH}	AVCC0 × 0.8	—	—	
			V_{IL}	—	—	AVCC0 × 0.2	
	Other VCC_USB input pins*5	1.62 V or above	V_{IH}	VCC_USB × 0.8	—	—	
			V_{IL}	—	—	VCC_USB × 0.2	
	Other VBATT_R input pins when VCC power supply is selected*5	1.62 V or above	V_{IH}	VCC × 0.8	—	VCC	
			V_{IL}	—	—	VCC × 0.2	

Note 1. RES and peripheral function pins associated with P303, P407 to P413, P511, P512, P514, P515, P708 to P715 (total 21 pins).
Note 2. P204 and P205 (total 2 pins)
Note 3. All input pins except for the peripheral function pins already described in the table. There is an item for each power supply voltage for each port. Refer to the IO chapter for the power supply of the port.
Note 4. P303, P407 to P413, P511, P512, P514, P515, P708 to P715 (total 20 pins).
Note 5. All input pins except for the ports already described in the table. There is an item for each power supply voltage for each port. Refer to the IO chapter for the power supply of the port.
Note 6. When VCC or VCC2 is less than 1.62 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown may occur because 5 V-tolerant ports are electrically controlled so as not to violate the break down voltage.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.6 I/O I_{OH}, I_{OL} (1 of 5)

Parameter			VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P000 to P015, P201	—	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
	Ports P204, P205, P303, P407 to P413, P511, P512, P514, P515, P708 to P715, PA15 (total 23 pins)	Low drive*1	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
		Middle drive*2	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		High drive*3	—	I_{OH}	—	—	−16	mA
				I_{OL}	—	—	20.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−20	mA
				I_{OL}	—	—	20.0	mA
	Other output pins*5	Low drive*1	—	I_{OH}	—	—	−2.0	mA
				I_{OL}	—	—	2.0	mA
		Middle drive*2	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		High drive*3	—	I_{OH}	—	—	−16	mA
				I_{OL}	—	—	16.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−20	mA
				I_{OL}	—	—	20.0	mA
Permissible output current (max value per pin)	Ports P000 to P015, P201	—	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
	Ports P204, P205, P303, P407 to P413, P511, P512, P514, P515, P708 to P715, PA15 (total 23 pins)	Low drive*1	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		Middle drive*2	—	I_{OH}	—	—	−8.0	mA
				I_{OL}	—	—	8.0	mA
		High drive*3	—	I_{OH}	—	—	−32	mA
				I_{OL}	—	—	40.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−40	mA
				I_{OL}	—	—	40.0	mA
	Other output pins*5	Low drive*1	—	I_{OH}	—	—	−4.0	mA
				I_{OL}	—	—	4.0	mA
		Middle drive*2	—	I_{OH}	—	—	−8.0	mA
				I_{OL}	—	—	8.0	mA
		High drive*3	—	I_{OH}	—	—	−32	mA
				I_{OL}	—	—	32.0	mA
		High-speed high drive*4	—	I_{OH}	—	—	−40	mA
				I_{OL}	—	—	40.0	mA

Table 2.6 I/O I_{OH}, I_{OL} (2 of 5)

Parameter				VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	VCC I/O	Ports P411 to P415, P511 to P515, P708 to P715, P805 to P807 (total 21 pins)	1.62 V or above	$\Sigma I_{OH\ (max)}$	—	—	−40	mA
			Ports P212, P213, P400 to P410, PB08 to PB14 (total 20 pins)	1.62 V or above		—	—	−40	
			Ports P700 to P707, PB00 to PB04 (total 13 pins)	1.62 V or above		—	—	−40	
			Ports PB05 to PB07, PD06, PD07 (total 5 pins)	1.62 V or above		—	—	−40	
			Ports P207, PD01 to PD05 (total 6 pins)	1.62 V or above		—	—	−40	
			Ports P904, P910 to P913 (total 5 pins)	1.62 V or above		—	—	−40	
			Ports P206, P304 to P312, P902, P903, P905 to P909 (total 17 pins)	1.62 V or above		—	—	−40	
			Ports P108 to P115, P201, P208 to P211, P300 to P303, P609, P914, P915, PA11 (total 21 pins)	1.62 V or above		—	—	−40	
			Ports P610 to P615, P813, PA04 to PA10, PA12 to PA15 (total 18 pins)	1.62 V or above		—	—	−40	
			Ports P503 to P510, P608, PA00 to PA03, PC11 to PC15, PD00 (total 19 pins)	1.62 V or above		—	—	−40	

Table 2.6 I/O I_{OH}, I_{OL} (3 of 5)

Parameter				VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	VCC2 I/O	Ports PC00 to PC10 (total 11 pins)	1.62 V or above	$\Sigma I_{OH\ (max)}$	—	—	−40	mA
			Ports P204, P205, P600 to P607 (total 10 pins)	1.62 V or above		—	—	−40	
			Ports P202, P203, P313 to P315, P900, P901 (total 7 pins)	1.62 V or above		—	—	−40	
			Ports P100 to P107, P800, P801 (total 10 pins)	1.62 V or above		—	—	−40	
			Ports P500 to P502, P802 to P804, P808 to P812 (total 11 pins)	1.62 V or above		—	—	−40	
		AVCC0 I/O		1.62 V or above		—	—	-33	
		VCC_USB I/O		1.62 V or above		—	—	-33	

Table 2.6 I/O I_{OH}, I_{OL} (4 of 5)

Parameter				VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	VCC and VCC2 I/O	Ports P411 to P415, P511 to P515, P708 to P715, P805 to P807 (total 21 pins)	1.62 V or above	$\Sigma I_{OL\ (max)}$	—	—	40	mA
			Ports P212, P213, P400 to P410, PB08 to PB14 (total 20 pins)	1.62 V or above		—	—	40	
			Ports P700 to P707, PB00 to PB04 (total 13 pins)	1.62 V or above		—	—	40	
			Ports PB05 to PB07, PD06, PD07 (total 5 pins)	1.62 V or above		—	—	40	
			Ports P207, PD01 to PD05 (total 6 pins)	1.62 V or above		—	—	40	
			Ports P904, P910 to P913 (total 5 pins)	1.62 V or above		—	—	40	
			Ports P206, P304 to P312, P902, P903, P905 to P909 (total 17 pins)	1.62 V or above		—	—	40	
			Ports P108 to P115, P201, P208 to P211, P300 to P303, P609, P914, P915, PA11 (total 21 pins)	1.62 V or above		—	—	40	
			Ports P610 to P615, P813, PA04 to PA10, PA12 to PA15 (total 18 pins)	1.62 V or above		—	—	40	
			Ports P503 to P510, P608, PA00 to PA03, PC11 to PC15, PD00 (total 19 pins)	1.62 V or above		—	—	40	
			Ports PC00 to PC10 (total 11 pins)	1.62 V or above		—	—	40	
			Ports P204, P205, P600 to P607 (total 10 pins)	1.62 V or above		—	—	40	

Table 2.6 I/O I_{OH}, I_{OL} (5 of 5)

Parameter				VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit
Permissible output current (maxvalue of total of all pins)	Maximum of all output pins	VCC and VCC2 I/O	Ports P202, P203, P313 to P315, P900, P901 (total 7 pins)	1.62 V or above	$\Sigma I_{OL\ (max)}$	—	—	40	mA
			Ports P100 to P107, P800, P801 (total 10 pins)	1.62 V or above		—	—	40	
			Ports P500 to P502, P802 to P804, P808 to P812 (total 11 pins)	1.62 V or above		—	—	40	
		AVCC0 I/O		1.62 V or above		—	—	33	
		VCC_USB I/O		1.62 V or above		—	—	33	

Note 1. This is the value when low driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability except for P400 and P401 is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability except for P400 and P401 is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability except for P400 and P401 is retained in Deep Software Standby mode.
Note 4. This is the value when high-speed high driving ability is selected in the Port Drive Capability in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 5. Except for P200, P214 and P215, which is an input port.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.7 I/O V_{OH}, V_{OL}, and other characteristics (1 of 3)

Parameter		VCC/ VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC	2.70 V or above	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA
		1.62 V to 1.95 V	V_{OL}	—	—	VCC × 0.2		I_{OL} = 2.0 mA
			V_{OL}	—	—	0.4		I_{OL} = 3.0 mA
			V_{OL}	—	—	0.6[*4]		I_{OL} = 6.0 mA
			V_{OL}	—	—	VCC2 × 0.2		I_{OL} = 2.0 mA
	IIC[*1]	2.70 V or above	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
		1.62 V to 1.95 V	V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	I3C	2.70 V or above	V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
		3.00 V or above	V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 1)
			V_{OH}	VCC − 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
		1.65 V to 1.95 V	V_{OL}	—	—	VCC × 0.2		I_{OL} = 2.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.4		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.6		I_{OL} = 6.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	VCC × 0.2		I_{OL} = 2.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
			V_{OL}	—	—	0.4		I_{OL} = 15.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
			V_{OL}	—	0.4	—		I_{OL} = 20.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 1, BFCTL.HSME = 0)
			V_{OL}	—	—	VCC × 0.2		I_{OL} = 3.0 mA (PRTS.PRTMD = 1, BFCTL.FMPE = 0, BFCTL.HSME = 1)
			V_{OH}	VCC − 0.27	—	—		I_{OH} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
			V_{OL}	—	—	0.27		I_{OL} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)

Table 2.7 I/O V_{OH}, V_{OL}, and other characteristics (2 of 3)

Parameter		VCC/ VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	ESWM, ESC	2.70 V to 3.60 V	V_{OH}	VCC − 0.5	—	—	V	I_{OH} = −1.0 mA
			V_{OL}	—	—	0.4		I_{OL} = 1.0 mA
			V_{OH}	VCC2 − 0.5	—	—		I_{OH} = −1.0 mA
		2.30 V to 2.70 V	V_{OH}	2	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.4		I_{OL} = 1.0 mA
	SD	2.70 V or above	V_{OH}	VCC × 0.75	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	VCC × 0.125		I_{OL} = 3.0 mA
			V_{OH}	VCC2 × 0.75	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	VCC2 × 0.125		I_{OL} = 3.0 mA
		1.70 to 1.95 V	V_{OH}	1.4	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	0.45		I_{OL} = 2.0 mA
	MMC	2.70 V or above	V_{OH}	VCC × 0.75	—	—		I_{OH} = −0.1 mA (VCC = 2.7 V)
			V_{OL}	—	—	VCC × 0.125		I_{OL} = 0.1 mA (VCC = 2.7 V)
			V_{OH}	VCC2 × 0.75	—	—		I_{OH} = −0.1mA (VCC2 = 2.7 V)
			V_{OL}	—	—	VCC2 × 0.125		I_{OL} = 0.1 mA (VCC2 = 2.7 V)
		1.70 to 1.95 V	V_{OH}	VCC − 0.45	—	—		I_{OH} = −2.0 mA
			V_{OL}	—	—	0.45		I_{OL} = 2.0 mA
			V_{OH}	VCC2 − 0.45	—	—		I_{OH} = −2.0 mA
	Ports P204, P205, P303, P407 to P413, P511, P512, P514, P515, P708 to P715, PA15 (total of 23 pins)*2	—	V_{OH}	VCC − 1.0	—	—		I_{OH} = −16 mA (VCC = 3.3 V)
			V_{OL}	—	—	1		I_{OL} = 20 mA (VCC = 3.3 V)
			V_{OH}	VCC2 − 1.0	—	—		I_{OH} = −16 mA (VCC2 = 3.3 V)
			V_{OL}	—	—	1		I_{OL} = 20 mA (VCC2 = 3.3 V)
	Other output pins	1.62 V or above	V_{OH}	VCC − 0.5	—	—	V	I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
			V_{OH}	VCC2 − 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
			V_{OH}	AVCC0 − 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA
			V_{OH}	VCC_USB – 0.5	—	—		I_{OH} = −1.0 mA
			V_{OL}	—	—	0.5		I_{OL} = 1.0 mA

Table 2.7 I/O V_{OH}, V_{OL}, and other characteristics (3 of 3)

Parameter		VCC/ VCC2/ AVCC0/ VCC_USB	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES	1.62 V or above	$\|I_{in}\|$	—	—	5	μA	V_{in} = 0 V V_{in} = 5.5 V
	Port P200, P214, P215	1.62 V or above		—	—	1		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	1.62 V or above	$\|I_{TSI}\|$	—	—	5	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for port P200, P214, P215)	1.62 V or above		—	—	1		V_{in} = 0 V V_{in} = VCC, VCC2, AVCC0, VCC_USB
Input pull-up MOS current	Ports P0 to PD	2.70 V or above	I_p	−300	—	−10	μA	VCC, VCC2, AVCC0, VCC_USB = 2.7 to 3.63 V V_{in} = 0 V
		1.62 V or above		−300	—	−5		VCC, VCC2, AVCC0, VCC_USB = 1.62 to 3.63 V V_{in} = 0 V
Pull-up current serving as the SCL current source	I3C*3	3.00 to 3.63 V	I_{cs}	3	—	12	mA	VCC = 3.0 to 3.63 V V_{in} = 0.3 × VCC to 0.7 × VCC
		1.65 to 1.95 V						VCC = 1.65 to 1.95 V V_{in} = 0.3 × VCC to 0.7 × VCC
Input capacitance	Ports P014, P015	—	C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz Ta = 25°C
	Ports P814/ USB_DP, P815/ USB_DM	—		—	—	12		
	Ports P400, P401, P409, P410, P511, P512, P708, P709	—		—	—	10		
	Other input pins	—		—	—	8		

Note 1. SCL0_A, SDA0_A, SCL1_A, SDA1_A, SCL2_A, SDA2_A (total 6 pins).
Note 2. This is the value when high speed high driving ability is selected in the Port Drive Capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. I3C_SCL0 (1 pin). This is the value when IIC high speed mode is selected.
Note 4. This is the value when high speed high driving ability is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SDA2_B, SCL2_B.

2.2.5 Operating and Standby Current

Current value of SiP Flash memory is not included in this section, refer to the datasheet of IS25WX064.

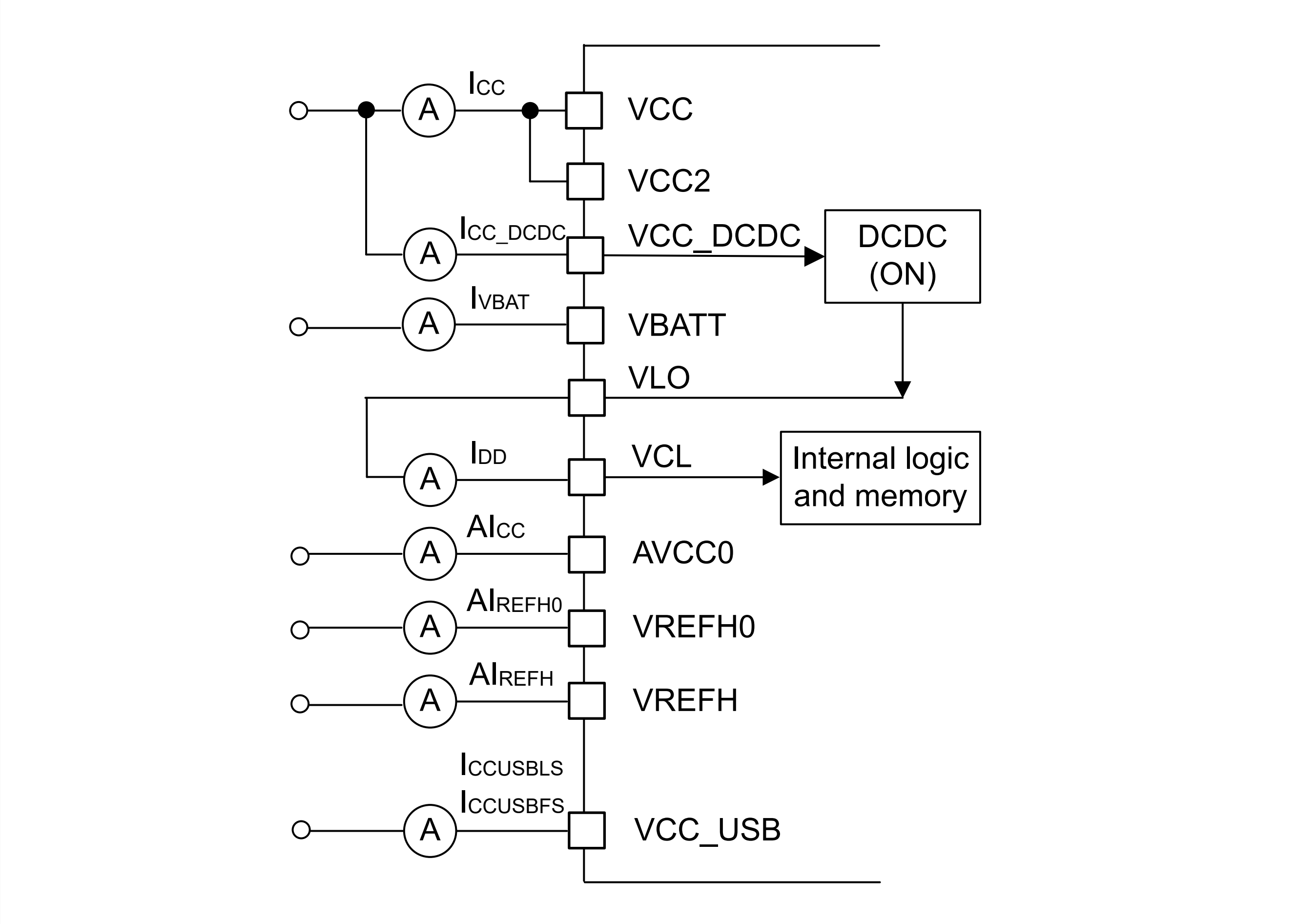


Figure 2.2 Consumption current measurement diagram (DCDC mode)

Table 2.8 Current of high-speed mode, maximum condition (MVE and peripheral operation) (DCDC mode)

Parameter			Symbol	Typ	Max 95 °C	Max 105 °C	Max 125 °C	Unit	Test conditions
Supply current *1 *2*6	—		I_{CC}	3.85	6.27	6.69	8.01	mA	—
	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	VCC_DCDC ≥ 2.5 V	I_{CC_DCDC} *4	176	340	—	—	mA	VCC_DCDC = 3.3 V MRICLK = 250 MHz, MRPCLK = 125 MHz, ICLK = 250 MHz, BCLK = 125 MHz, PCLKA = 125 MHz, PCLKB = 62.5 MHz, PCLKC = 125 MHz, PCLKD = 250 MHz, PCLKE = 250 MHz
			I_{DD} *3	452	873	—	—		
		VCC_DCDC < 2.5 V	I_{CC_DCDC} *4	343	664	—	—		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	452	873	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	VCC_DCDC ≥ 2.5 V	I_{CC_DCDC} *4	148	—	356	—	mA	VCC_DCDC = 3.3 V MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz
			I_{DD} *3	380	—	915	—		
		VCC_DCDC < 2.5 V	I_{CC_DCDC} *4	289	—	696	—		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	380	—	915	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	VCC_DCDC ≥ 2.5 V	I_{CC_DCDC} *4	129	—	—	390	mA	VCC_DCDC = 3.3 V MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz
			I_{DD} *3	330	—	—	1000 *5		
		VCC_DCDC < 2.5 V	I_{CC_DCDC} *4	251	—	—	760		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	330	—	—	1000 *5		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	VCC_DCDC ≥ 2.5 V	I_{CC_DCDC} *4	115	282	309	366	mA	VCC_DCDC = 3.3 V MRICLK = 150 MHz, MRPCLK = 75 MHz, ICLK = 150 MHz, BCLK = 75 MHz, PCLKA = 75 MHz, PCLKB = 37.5 MHz, PCLKC = 75 MHz, PCLKD = 150 MHz, PCLKE = 150 MHz
			I_{DD} *3	301	738	810	959		
		VCC_DCDC < 2.5 V	I_{CC_DCDC} *4	224	550	604	715		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	301	738	810	959		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows. The ICLK items in the formula include CPU1 current.
I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.77 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95℃) = 0.22 × fCPUCLK0 + 0.80 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105℃) = 0.22 × fCPUCLK0 + 0.80 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125℃) = 0.22 × fCPUCLK0 + 0.80 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95℃) = 0.22 × fCPUCLK0 + 0.93 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105℃) = 0.22 × fCPUCLK0 + 0.93 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.22 × fCPUCLK0 + 0.93 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.
Note 5. Do not let actual consumption current during operation exceed the current value described here.
Note 6. The power consumption is calculated as Power = VCC × I_{cc} + VCC_DCDC × I_{cc_DCDC}.

Table 2.9 Current of high-speed mode, maximum condition (MVE and peripheral operation) (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1 *2*5	—	I_{CC}	3.85	6.27	6.69	8.01	mA	—
	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD} *3	452	873	—	—	mA	MRICLK = 250 MHz, MRPCLK = 125 MHz, ICLK = 250 MHz, BCLK = 125 MHz, PCLKA = 125 MHz, PCLKB = 62.5 MHz, PCLKC = 125MHz, PCLKD = 250 MHz, PCLKE = 250 MHz
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *3	380	—	915	—	mA	MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *3	330	—	—	1000 *4	mA	MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD} *3	301	738	810	959	mA	MRICLK = 150 MHz, MRPCLK = 75 MHz, ICLK = 150 MHz, BCLK = 75 MHz, PCLKA = 75 MHz, PCLKB = 37.5 MHz, PCLKC = 75 MHz, PCLKD = 150 MHz, PCLKE = 150 MHz

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.

Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows. The ICLK items in the formula include CPU1 current.

I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.77 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.22 × fCPUCLK0 + 0.80 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.22 × fCPUCLK0 + 0.80 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.22 × fCPUCLK0 + 0.80 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.22 × fCPUCLK0 + 0.93 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.22 × fCPUCLK0 + 0.93 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.22 × fCPUCLK0 + 0.93 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)

Note 4. Do not let actual consumption current during operation exceed the current value described here.

Note 5. The power consumption is calculated as Power = VCC × I_{cc} + VCL × I_{DD}.

Table 2.10 Current of high-speed mode, maximum condition (MVE and peripheral operation), CPU0 active, CPU1 Deep Sleep (DCDC mode)

Parameter			Symbol	Typ	Max 95 °C	Max 105 °C	Max 125 °C	Unit	Test conditions
Supply current *1*2*5	—		I_{CC}	3.85	6.27	6.69	8.01	mA	—
	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	VCC_DCDC ≥ 2.5V	I_{CC_DCDC} *4	168	329	—	—	mA	VCC_DCDC = 3.3 V MRICLK = 250 MHz, MRPCLK = 125 MHz, ICLK = 250 MHz, BCLK = 125 MHz, PCLKA = 125 MHz, PCLKB = 62.5 MHz, PCLKC = 125 MHz, PCLKD = 250 MHz, PCLKE = 250 MHz CPU1 = Deep Sleep
			I_{DD} *3	430	844	—	—		
		VCC_DCDC < 2.5V	I_{CC_DCDC} *4	327	642	—	—		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	430	844	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	VCC_DCDC ≥ 2.5V	I_{CC_DCDC} *4	141	—	347	—	mA	VCC_DCDC = 3.3 V MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz CPU1 = Deep Sleep
			I_{DD} *3	362	—	891	—		
		VCC_DCDC < 2.5V	I_{CC_DCDC} *4	275	—	678	—		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	362	—	891	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	VCC_DCDC ≥ 2.5V	I_{CC_DCDC} *4	122	—	—	380	mA	VCC_DCDC = 3.3 V MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz CPU1 = Deep Sleep
			I_{DD} *3	312	—	—	976		
		VCC_DCDC < 2.5V	I_{CC_DCDC} *4	237	—	—	742		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	312	—	—	976		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	VCC_DCDC ≥ 2.5V	I_{CC_DCDC} *4	110	274	301	359	mA	VCC_DCDC = 3.3 V MRICLK = 150 MHz, MRPCLK = 75 MHz, ICLK = 150 MHz, BCLK = 75 MHz, PCLKA = 75 MHz, PCLKB = 37.5 MHz, PCLKC = 75 MHz, PCLKD = 150 MHz, PCLKE = 150 MHz CPU1 = Deep Sleep
			I_{DD} *3	289	718	788	940		
		VCC_DCDC < 2.5V	I_{CC_DCDC} *4	216	536	588	701		VCC_DCDC = 1.8 V Clock settings are the same as above
			I_{DD}	289	718	788	940		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows.
I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.71 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95℃) = 0.22 × fCPUCLK0 + 0.70 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105℃) = 0.22 × fCPUCLK0 + 0.70 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125℃) = 0.22 × fCPUCLK0 + 0.70 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95℃) = 0.22 × fCPUCLK0 + 0.83 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105℃) = 0.22 × fCPUCLK0 + 0.83 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.22 × fCPUCLK0 + 0.83 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.
Note 5. The power consumption is calculated as Power = VCC × I_{cc} + VCC_DCDC × I_{cc_DCDC}.

Table 2.11 Current of high-speed mode, maximum condition (MVE and peripheral operation), CPU0 active, CPU1 Deep Sleep (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2*4	—	I_{CC}	3.85	6.27	6.69	8.01	mA	—
	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD} *3	430	844	—	—	mA	MRICLK = 250 MHz, MRPCLK = 125 MHz, ICLK = 250 MHz, BCLK = 125 MHz, PCLKA = 125 MHz, PCLKB = 62.5 MHz, PCLKC = 125 MHz, PCLKD = 250 MHz, PCLKE = 250 MHz CPU1 = Deep Sleep
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *3	362	—	891	—	mA	MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz CPU1 = Deep Sleep
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *3	312	—	—	976	mA	MRICLK = 200 MHz, MRPCLK = 100 MHz, ICLK = 200 MHz, BCLK = 100 MHz, PCLKA = 100 MHz, PCLKB = 50 MHz, PCLKC = 100 MHz, PCLKD = 200 MHz, PCLKE = 200 MHz CPU1 = Deep Sleep
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD} *3	289	718	788	940	mA	MRICLK = 150 MHz, MRPCLK = 75 MHz, ICLK = 150 MHz, BCLK = 75 MHz, PCLKA = 75 MHz, PCLKB = 37.5 MHz, PCLKC = 75 MHz, PCLKD = 150 MHz, PCLKE = 150 MHz CPU1 = Deep Sleep

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows.
I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.71 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.22 × fCPUCLK0 + 0.70 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.22 × fCPUCLK0 + 0.70 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.22 × fCPUCLK0 + 0.70 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.22 × fCPUCLK0 + 0.83 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.22 × fCPUCLK0 + 0.83 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.22 × fCPUCLK0 + 0.83 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. The power consumption is calculated as Power = VCC × I_{cc} + VCL x I_{DD}.

Table 2.12 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock ON (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current [*1*2]	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC}[*4]	136	322	—	—	mA	VCC_DCDC = 3.3 V[*5]
		I_{DD}[*3]	350	827	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}[*4]	113	—	340	—		
		I_{DD}[*3]	290	—	874	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}[*4]	94	—	—	356		
		I_{DD}[*3]	241	—	—	915		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC}[*4]	86	264	305	336		
		I_{DD}[*3]	226	692	798	879		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows. The ICLK items in the formula include CPU1 current.
I_{DD} Typ. = 0.24 × fCPUCLK0 + 0.37 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95℃) = 0.27 × fCPUCLK0 + 0.20 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105℃) = 0.27 × fCPUCLK0 + 0.20 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125℃) = 0.27 × fCPUCLK0 + 0.20 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95℃) = 0.27 × fCPUCLK0 + 0.18 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105℃) = 0.27 × fCPUCLK0 + 0.18 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.27 × fCPUCLK0 + 0.18 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.
Note 5. Same frequency condition is applied as in the maximum condition.

Table 2.13 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock ON (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}*3	350	827	—	—	mA	*4
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*3	290	—	874	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*3	241	—	—	915		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}*3	226	692	798	879		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows. The ICLK items in the formula include CPU1 current.
I_{DD} Typ. = 0.24 × fCPUCLK0 + 0.37 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.27 × fCPUCLK0 + 0.20 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.27 × fCPUCLK0 + 0.20 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.27 × fCPUCLK0 + 0.20 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.27 × fCPUCLK0 + 0.18 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.27 × fCPUCLK0 + 0.18 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.27 × fCPUCLK0 + 0.18 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Same frequency condition is applied as in the maximum condition.

Table 2.14 Current of high-speed mode, maximum data processing (MVE operation), CPU0 active, CPU1 Deep Sleep, peripheral clock ON (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC} *4	131	313	—	—	mA	VCC_DCDC = 3.3 V CPU1 = Deep Sleep *5
		I_{DD} *3	335	804	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	109	—	332	—		
		I_{DD} *3	279	—	853	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	89	—	—	342		
		I_{DD} *3	229	—	—	879		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC} *4	83	258	298	328		
		I_{DD} *3	216	676	780	858		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.

Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows.

I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.30 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VSCR_1, 95℃) = 0.27 × fCPUCLK0 + 0.05 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VSCR_1, 105℃) = 0.27 × fCPUCLK0 + 0.05 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VSCR_1, 125℃) = 0.27 × fCPUCLK0 + 0.05 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VSCR_2, 95℃) = 0.27 × fCPUCLK0 + 0.07 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VSCR_2, 105℃) = 0.27 × fCPUCLK0 + 0.07 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)

I_{DD} Max.(VSCR_2, 125℃) = 0.27 × fCPUCLK0 + 0.07 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)

Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.

Note 5. Same frequency condition is applied as in the maximum condition.

Table 2.15 Current of high-speed mode, maximum data processing (MVE operation), CPU0 active, CPU1 Deep Sleep, peripheral clock ON (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}*3	335	804	—	—	mA	CPU1 = Deep Sleep *4
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*3	279	—	853	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*3	229	—	—	879		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}*3	216	676	780	858		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows.
I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.30 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.27 × fCPUCLK0 + 0.05 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.27 × fCPUCLK0 + 0.05 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.27 × fCPUCLK0 + 0.05 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.27 × fCPUCLK0 + 0.07 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.27 × fCPUCLK0 + 0.07 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.27 × fCPUCLK0 + 0.07 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Same frequency condition is applied as in the maximum condition.

Table 2.16 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock ON (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC} *4	44	175	—	—	mA	VCC_DCDC = 3.3 V CPU0 = Deep Sleep *3
		I_{DD}	112	450	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	38	—	190	—		
		I_{DD}	99	—	488	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	38	—	—	224		
		I_{DD}	96	—	—	545		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC} *4	31	155	179	208		
		I_{DD}	82	406	470	545		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. Same frequency condition is applied as in the maximum condition.
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.

Table 2.17 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock ON (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}	112	450	—	—	mA	CPU0 = Deep Sleep *3
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	99	—	488	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	96	—	—	545		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}	82	406	470	545		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions and peripherals being operated. This does not include the BGO operation.
Note 3. Same frequency condition is applied as in the maximum condition.

Table 2.18 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock OFF (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC}*4	121	317	—	—	mA	VCC_DCDC = 3.3 V*5
		I_{DD}*3	310	814	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*4	99	—	325	—		
		I_{DD}*3	255	—	833	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*4	80	—	—	358		
		I_{DD}*3	207	—	—	919		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC}*4	75	258	292	340		
		I_{DD}*3	197	675	764	889		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows. The ICLK items in the formula include CPU1 current.
I_{DD} Typ. = 0.24 × fCPUCLK0 + 0.20 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95℃) = 0.27 × fCPUCLK0 + 0.23 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105℃) = 0.27 × fCPUCLK0 + 0.23 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125℃) = 0.27 × fCPUCLK0 + 0.23 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95℃) = 0.27 × fCPUCLK0 + 0.25 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105℃) = 0.27 × fCPUCLK0 + 0.25 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.27 × fCPUCLK0 + 0.25 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.
Note 5. Same frequency condition is applied as in the maximum condition.

Table 2.19 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock OFF (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}*3	310	814	—	—	mA	*4
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*3	255	—	833	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*3	207	—	—	919		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}*3	197	675	764	889		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows. The ICLK items in the formula include CPU1 current.
I_{DD} Typ. = 0.24 × fCPUCLK0 + 0.20 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.27 × fCPUCLK0 + 0.23 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.27 × fCPUCLK0 + 0.23 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.27 × fCPUCLK0 + 0.23 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.27 × fCPUCLK0 + 0.25 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.27 × fCPUCLK0 + 0.25 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.27 × fCPUCLK0 + 0.25 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Same frequency condition is applied as in the maximum condition.

Table 2.20 Current of high-speed mode, maximum data processing (MVE operation), CPU0 active, CPU1 Deep Sleep, peripheral clock OFF (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC} *4	115	308	—	—	mA	VCC_DCDC = 3.3 V CPU1 = Deep Sleep *5
		I_{DD} *3	295	792	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	95	—	317	—		
		I_{DD} *3	244	—	813	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	76	—	—	348		
		I_{DD} *3	194	—	—	895		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC} *4	71	251	285	331		
		I_{DD} *3	187	658	746	868		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows.
I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.13 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95°C) = 0.27 × fCPUCLK0 + 0.13 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105°C) = 0.27 × fCPUCLK0 + 0.13 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125°C) = 0.27 × fCPUCLK0 + 0.13 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95°C) = 0.27 × fCPUCLK0 + 0.14 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105°C) = 0.27 × fCPUCLK0 + 0.14 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125°C) = 0.27 × fCPUCLK0 + 0.14 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.
Note 5. Same frequency condition is applied as in the maximum condition.

Table 2.21 Current of high-speed mode, maximum data processing (MVE operation), CPU0 active, CPU1 Deep Sleep, peripheral clock OFF (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD} *3	295	792	—	—	mA	CPU1 = Deep Sleep *4
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *3	244	—	813	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *3	194	—	—	895		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD} *3	187	658	746	868		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. I_{DD} depends on f (CPUCLK0 and ICLK) as follows.
I_{DD} Typ. = 0.25 × fCPUCLK0 + 0.13 × fICLK + 21 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.27 × fCPUCLK0 + 0.13 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.27 × fCPUCLK0 + 0.13 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.27 × fCPUCLK0 + 0.13 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.27 × fCPUCLK0 + 0.14 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.27 × fCPUCLK0 + 0.14 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.27 × fCPUCLK0 + 0.14 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 4. Same frequency condition is applied as in the maximum condition.

Table 2.22 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock OFF (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC}*4	28	157	—	—	mA	VCC_DCDC = 3.3 V CPU0 = Deep Sleep *3
		I_{DD}	72	404	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*4	25	—	174	—		
		I_{DD}	64	—	447	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*4	24	—	—	208		
		I_{DD}	61	—	—	533		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC}*4	20	142	166	195		
		I_{DD}	53	372	435	511		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. Same frequency condition is applied as in the maximum condition.
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.

Table 2.23 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock OFF (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}	72	404	—	—	mA	CPU0 = Deep Sleep *3
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	64	—	447	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	61	—	—	533		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}	53	372	435	511		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. Same frequency condition is applied as in the maximum condition.

Table 2.24 Current of high-speed mode, CPU Sleep mode (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*3*4	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC}*5	22	200	—	—	mA	VCC_DCDC = 3.3 V
		I_{DD}*2	56	513	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*5	20	—	228	—		
		I_{DD}*2	50	—	586	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*5	18	—	—	279		
		I_{DD}*2	46	—	—	716		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC}*5	16	185	219	264		
		I_{DD}*2	42	484	573	690		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. I_{DD} depends on f (ICLK) as follows.
I_{DD} Typ. = 0.02 × fCPUCLK0 + 0.06 × fICLK + 57 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 3. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 4. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.
Note 5. Typical DCDC efficiency and the voltage of the test conditions are applied.

Table 2.25 Current of high-speed mode, CPU Sleep mode (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*3*4	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD} *2	56	513	—	—	mA	—
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *2	50	—	586	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD} *2	46	—	—	716		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD} *2	42	484	573	690		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. I_{DD} depends on f (ICLK) as follows.
I_{DD} Typ. = 0.02 × fCPUCLK0 + 0.06 × fICLK + 57 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 477 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 553 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 709 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 464 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 537 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.02 × fCPUCLK0 + 0.01 × fICLK + 691 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 3. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 4. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.

Table 2.26 Current of high-speed mode, CPU0 Sleep, CPU1 Deep Sleep (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*3*4	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC} *5	21	197	—	—	mA	VCC_DCDC = 3.3 V CPU1 = Deep Sleep
		I_{DD} *2	54	505	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *5	19	—	229	—		
		I_{DD} *2	48	—	576	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *5	17	—	—	274		
		I_{DD} *2	44	—	—	703		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC} *5	15	182	216	259		
		I_{DD} *2	40	477	565	678		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. I_{DD} depends on f (ICLK) as follows.
I_{DD} Typ. = 0.02 × fCPUCLK0 + 0.05 × fICLK + 55 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 95℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 105℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_1, 125℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 95℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 105℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VSCR_2, 125℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 3. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 4. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.
Note 5. Typical DCDC efficiency and the voltage of the test conditions are applied.

Table 2.27 Current of high-speed mode, CPU0 Sleep, CPU1 Deep Sleep (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*3*4	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}*2	54	505	—	—	mA	CPU1 = Deep Sleep
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*2	48	—	576	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}*2	44	—	—	703		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}*2	40	477	565	678		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. I_{DD} depends on f (ICLK) as follows.
I_{DD} Typ. = 0.02 × fCPUCLK0 + 0.05 × fICLK + 55 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 95℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 474 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 105℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 549 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 1, 125℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 704 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 95℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 461 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 105℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 533 (unit : mA, fCPUCLK0 and fICLK are MHz)
I_{DD} Max.(VCL = voltage range 2, 125℃) = 0.004 × fCPUCLK0 + 0.01 × fICLK + 686 (unit : mA, fCPUCLK0 and fICLK are MHz)
Note 3. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 4. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.

Table 2.28 Current of high-speed mode, CPU0 Deep Sleep, CPU1 Sleep (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2*3	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC}*4	12	141	—	—	mA	VCC_DCDC = 3.3 V CPU0 = Deep Sleep
		I_{DD}	32	363	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*4	12	—	161	—		
		I_{DD}	30	—	414	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC}*4	11	—	—	196		
		I_{DD}	29	—	—	504		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC}*4	10	132	157	184		
		I_{DD}	26	347	411	481		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.

Table 2.29 Current of high-speed mode, CPU0 Deep Sleep, CPU1 Sleep (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2*3	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}	32	363	—	—	mA	CPU0 = Deep Sleep
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	30	—	414	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	29	—	—	504		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}	26	347	411	481		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.

Table 2.30 Current of high-speed mode, CPU Deep Sleep mode (DCDC mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2*3	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VSCR_1	I_{CC_DCDC} *4	13	138	—	—	mA	VCC_DCDC = 3.3 V
		I_{DD}	32	355	—	—		
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	12	—	158	—		
		I_{DD}	30	—	405	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1	I_{CC_DCDC} *4	11	—	—	192		
		I_{DD}	29	—	—	492		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VSCR_2	I_{CC_DCDC} *4	11	130	154	182		
		I_{DD}	28	340	402	476		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.
Note 4. Typical DCDC efficiency and the voltage of the test conditions are applied.

Table 2.31 Current of high-speed mode, CPU Deep Sleep mode (External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current *1*2*3	CPUCLK0 = 1 GHz CPUCLK1 = 250 MHz VCL = voltage range 1	I_{DD}	32	355	—	—	mA	—
	CPUCLK0 = 800 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	30	—	405	—		
	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VCL = voltage range 1	I_{DD}	29	—	—	492		
	CPUCLK0 = 600 MHz CPUCLK1 = 150 MHz VCL = voltage range 2	I_{DD}	28	340	402	476		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 3. MRICLK, MRPCLK, ICLK, PCLKA, PCLKB, PCLKC, PCLKD, PCLKE and BCLK are set to divided by 64.

Table 2.32 Current increase during BGO operation (Programing of MRAM OTP) (DCDC mode and External VDD mode)

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current*1	normal speed write mode	I_{CC}	—	—	—	20	mA	VCC ≥ 1.62V
		I_{DD}	—	—	—	0.50		
	high speed write mode 0	I_{CC}	—	—	—	25		VCC ≥ 2.5V
		I_{DD}	—	—	—	0.5		
	high speed write mode 1	I_{CC}	—	—	—	80		VCC ≥ 3.0V
		I_{DD}	—	—	—	0.5		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Table 2.33 Standby current (DCDC mode) (1 of 4)

Parameter					Symbol	Typ	Max			Unit	Test conditions
							95 °C	105 °C	125 °C		
Supply current*1	Software Standby mode				I_{CC}	0.10	1.11	1.12	1.14	mA	—
		SS2LP_0	SVSCR_1	Data of SRAM and TCM is retained	I_{CC_DCDC}	2.67	54.24	62.23	78.41		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	2.44	52.53	59.86	74.47		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_2	Data of SRAM and TCM is retained	I_{CC_DCDC}	2.52	51.58	59.19	74.81		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	2.33	50.03	57.09	71.10		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_3	Data of SRAM and TCM is retained	I_{CC_DCDC}	1.68	37.85	43.60	56.69		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.60	36.87	42.22	54.07		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_4	Data of SRAM and TCM is retained	I_{CC_DCDC}	1.47	32.41	38.22	49.79		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.42	31.61	37.07	47.62		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_5	Data of SRAM and TCM is retained	I_{CC_DCDC}	1.28	29.69	34.28	44.67		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.24	29.03	33.32	42.82		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)

Table 2.33 Standby current (DCDC mode) (2 of 4)

Parameter					Symbol	Typ	Max			Unit	Test conditions
							95 °C	105 °C	125 °C		
Supply current*1	Software Standby mode	SS2LP_1	SVSCR_2	Data of SRAM and TCM is retained	I_{CC_DCDC}	2.12	43.32	49.71	62.83	mA	VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.95	42.01	47.94	59.71		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_3	Data of SRAM and TCM is retained	I_{CC_DCDC}	1.40	31.70	36.52	47.48		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.34	30.88	35.36	45.29		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_4	Data of SRAM and TCM is retained	I_{CC_DCDC}	1.22	26.41	31.14	40.57		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.18	25.76	30.20	38.80		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)
			SVSCR_5	Data of SRAM and TCM is retained	I_{CC_DCDC}	1.06	24.15	27.89	36.35		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 1 (n = 0 to 12) PDRAMSCR1.RKEEPn = 1 (n = 0, 1)
				Data of SRAM and TCM is not retained	I_{CC_DCDC}	1.03	23.62	27.11	34.84		VCC_DCDC = 3.3 V PDRAMSCR0.RKEEPn = 0 (n = 0 to 12) PDRAMSCR1.RKEEPn = 0 (n = 0, 1)

Table 2.33 Standby current (DCDC mode) (3 of 4)

Parameter				Symbol	Typ	Max 95 °C	Max 105 °C	Max 125 °C	Unit	Test conditions
Supply current*1	Deep Software Standby mode 1			I_{CC}	10.04	207	297	498	μA	—
				I_{CC_DCDC}	0.16	0.85	1.24	2.45		—
		Increase when the function is activated	PVDn (n = 0 to 2, 4, 5) or Battery power supply switch	I_{CC}	See Table 2.36					—
			When the LOCO is in use		2.46	—	—	—		—
			Crystal oscillator and RTC		See Table 2.37					—
			IWDT and ULPT (all units) are operating		1.58	—	—	—		—
Supply current*1	Deep Software Standby mode 2			I_{CC}	3.04	98	122	175	μA	—
				I_{CC_DCDC}	0.16	0.85	1.24	2.45		—
		Increase when the function is activated	PVDn (n = 0 to 2, 4, 5) or Battery power supply switch	I_{CC}	See Table 2.36					—
			Crystal oscillator and RTC		See Table 2.37					—
	Deep Software Standby mode 3			I_{CC}	2.78	97	121	173		—
				I_{CC_DCDC}	0.16	0.85	1.24	2.45		—
		Increase when the function is activated	Crystal oscillator and RTC	I_{CC}	See Table 2.37					—

Table 2.33 Standby current (DCDC mode) (4 of 4)

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current*1	RTC operating while VCC is off (with the battery backup function, only the RTC operate)	When a crystal oscillator with low power mode 3 is in use		I_{VBAT}	0.53	—	—	—	μA	VBATT = 1.8 V, VCC = 0 V
					0.82	—	—	—		VBATT = 3.3 V, VCC = 0 V
		When a crystal oscillator with low power mode 2 is in use			0.63	—	—	—		VBATT = 1.8 V, VCC = 0 V
					0.94	—	—	—		VBATT = 3.3 V, VCC = 0 V
		When a crystal oscillator with low power mode 1 is in use			0.73	—	—	—		VBATT = 1.8 V, VCC = 0 V
					1.03	—	—	—		VBATT = 3.3 V, VCC = 0 V
		When a crystal oscillator with standard mode is in use			0.99	—	—	—		VBATT = 1.8 V, VCC = 0 V
					1.29	—	—	—		VBATT = 3.3 V, VCC = 0 V
		When EXCIN is in use			0.30	—	—	—		VBATT = 1.8 V, VCC = 0 V
					0.52	—	—	—		VBATT = 3.3 V, VCC = 0 V
		Increase when the function is activated	RTCICn (n = 0 to 2) input is in use per channel		0.01	—	—	—		VBATT = 1.8 V, VCC = 0 V
					0.01	—	—	—		VBATT = 3.3 V, VCC = 0 V

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.

Table 2.34 Coremark and normal mode current, CPU0 active, CPU1 Deep Sleep. (DCDC mode and External VDD mode) (1 of 2)

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current[*1*2]	CPUCLK0 = 1 GHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I_{DD}	151	—	—	—	μA/MHz	CPU1 = Deep Sleep ESWM power domain off CPUCLK1 = 250 MHz, MRICLK = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz
			Cache off, executing from ITCM		143	—	—	—		
			Cache off, executing from SRAM		92	—	—	—		
			Cache off, executing from MRAM		104	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		118	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		121	—	—	—		
	CPUCLK0 = 800 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on		157	—	—	—	μA/MHz	CPU1 = Deep Sleep ESWM power domain off CPUCLK1 = 200 MHz, MRICLK = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
			Cache off, executing from ITCM		149	—	—	—		
			Cache off, executing from SRAM		98	—	—	—		
			Cache off, executing from MRAM		111	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		124	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		127	—	—	—		

Table 2.34 Coremark and normal mode current, CPU0 active, CPU1 Deep Sleep. (DCDC mode and External VDD mode) (2 of 2)

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current*1*2	CPUCLK0 = 600 MHz CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I_{DD}	172	—	—	—	µA/MHz	CPU1 = Deep Sleep ESWM power domain off CPUCLK1 = 200 MHz, MRICLK = 200 MHz, MRPCLK = 25 MHz, ICLK = 200 MHz, PCLKA = 25 MHz, PCLKB = 25 MHz, PCLKC = 25 MHz, PCLKD = 25 MHz, PCLKE = 25 MHz, BCLK = 25 MHz
			Cache off, executing from ITCM		164	—	—	—		
			Cache off, executing from SRAM		118	—	—	—		
			Cache off, executing from MRAM		133	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		139	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		142	—	—	—		
	CPUCLK0 = 600 MHz VSCR_2 VCL = voltage range 2	Coremark	Cache on		164	—	—	—	µA/MHz	CPU1 = Deep Sleep ESWM power domain off CPUCLK1 = 150 MHz, MRICLK = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz
			Cache off, executing from ITCM		156	—	—	—		
			Cache off, executing from SRAM		106	—	—	—		
			Cache off, executing from MRAM		119	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		131	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		135	—	—	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Table 2.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (1 of 2)

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current[*1] [*2]	CPUCLK1 = 250 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I_{DD}	215	—	—	—	μA/MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 1 GHz, MRICLK = 250 MHz, MRPCLK = 15.6 MHz, ICLK = 250 MHz, PCLKA = 15.6 MHz, PCLKB = 15.6 MHz, PCLKC = 15.6 MHz, PCLKD = 15.6 MHz, PCLKE = 15.6 MHz, BCLK = 15.6 MHz
			Cache off, executing from ITCM		197	—	—	—		
			Cache off, executing from SRAM		194	—	—	—		
			Cache off, executing from MRAM		268	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		201	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		264	—	—	—		
	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on		236	—	—	—	μA/MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 800 MHz, MRICLK = 200 MHz, MRPCLK = 12.5 MHz, ICLK = 200 MHz, PCLKA = 12.5 MHz, PCLKB = 12.5 MHz, PCLKC = 12.5 MHz, PCLKD = 12.5 MHz, PCLKE = 12.5 MHz, BCLK = 12.5 MHz
			Cache off, executing from ITCM		218	—	—	—		
			Cache off, executing from SRAM		215	—	—	—		
			Cache off, executing from MRAM		299	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		222	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		297	—	—	—		

Table 2.35 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode) (2 of 2)

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current[*1] [*2]	CPUCLK1 = 200 MHz VSCR_1 VCL = voltage range 1	Coremark	Cache on	I_{DD}	226	—	—	—	μA/MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICLK = 200 MHz, MRPCLK = 25 MHz, ICLK = 200 MHz, PCLKA = 25 MHz, PCLKB = 25 MHz, PCLKC = 25 MHz, PCLKD = 25 MHz, PCLKE = 25 MHz, BCLK = 25MHz
			Cache off, executing from ITCM		208	—	—	—		
			Cache off, executing from SRAM		205	—	—	—		
			Cache off, executing from MRAM		289	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		213	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		287	—	—	—		
	CPUCLK1 = 150 MHz VSCR_2 VCL = voltage range 2	Coremark	Cache on		265	—	—	—	μA/MHz	CPU0 = Deep Sleep ESWM power domain off CPUCLK0 = 600 MHz, MRICLK = 150 MHz, MRPCLK = 9.4 MHz, ICLK = 150 MHz, PCLKA = 9.4 MHz, PCLKB = 9.4 MHz, PCLKC = 9.4 MHz, PCLKD = 9.4 MHz, PCLKE = 9.4 MHz, BCLK = 9.4 MHz
			Cache off, executing from ITCM		247	—	—	—		
			Cache off, executing from SRAM		244	—	—	—		
			Cache off, executing from MRAM		326	—	—	—		
		Normal mode	All peripheral disabled, Cache on, while (1) code		252	—	—	—		
			All peripheral disabled, Cache off, while (1) code executing from MRAM		324	—	—	—		

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.

Table 2.36 Increase when the PVD1, PVD2, PVD4, PVD5 or Battery power supply switch is enabled in Deep Software Standby mode 1 and 2.

Parameter		Symbol	Typ	Max			Unit	Test conditions
				95 °C	105 °C	125 °C		
Supply current	Common circuit when enabling PVDn (n=1, 2, 4, 5) or disabling low power consumption function of PVD0 for the battery power supply switch control (OFS1(_SEC).PVDLPSEL=1) in Deep Software Standby mode 1	I_{CC}	4.00	—	—	—	μA	—
	Common circuit when enabling PVDn (n=1, 2, 4, 5) or disabling low power consumption function of PVD0 for the battery power supply switch control (OFS1(_SEC).PVDLPSEL=1) in Deep Software Standby mode 2		4.00	—	—	—		—
	PVD1 enabled		2.00	—	—	—		—
	PVD2 enabled		2.00	—	—	—		—
	PVD4 enabled		2.00		—	—		
	PVD5 enabled		2.00	—	—	—		—
	Battery power supply switch enabled with following conditions.[*1] ● Battery power supply switch enable (VBTBPCR1.BPWSWSTP=0), and low power consumption function of PVD0 select at Deep Software Standby mode disable (OFS1(_SEC).PVDLPSEL=1).		2.00	—	—	—		—

Note 1. Consumption current is not increased in other condition.

Table 2.37 Increase when the sub-clock oscillator and RTC are enabled in Deep Software Standby mode 1, 2 and 3.

Parameter			Symbol	Typ	Max			Unit	Test conditions
					95 °C	105 °C	125 °C		
Supply current	When a crystal oscillator is in use	Low Power mode 3	I_{CC}	0.31	—	—	—	μA	—
		Low Power mode 2		0.43	—	—	—		—
		Low Power mode 1		0.52	—	—	—		—
		Standard mode		0.78	—	—	—		—
	RTC is operating			0.30	—	—	—		—

Table 2.38 Inrush current

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current	Inrush current on Cold Start		Inrush current of VCC_DCDC[*1]	I_{RUSH}	—	1330	1330	1330	mA	—
	Inrush current on returning from deep software standby mode	DPSBYCR.DCSSMODE=1			—	1270	1270	1270		—
		DPSBYCR.DCSSMODE=2			—	1170	1170	1170		—
		DPSBYCR.DCSSMODE=3			—	1160	1160	1160		—

Note 1. Reference value

Table 2.39 Operating current (Analog)

Parameter				Symbol	Typ	Max			Unit	Test conditions
						95 °C	105 °C	125 °C		
Supply current[*1]	Oscillator	Main clock oscillator		I_{CC}	0.65	—	—	—	mA	MOMCR.MODRV0 [2:0] = 000b
					0.76	—	—	—	mA	MOMCR.MODRV0 [2:0] = 011b
					0.88	—	—	—	mA	MOMCR.MODRV0 [2:0] = 101b
	Analog power supply current	During 16-bit A/D conversion	SAR mode, Oversampling mode and Hybrid mode	AI_{CC}	2.4	3.2	3.2	3.2	mA	—
		During 16-bit A/D conversion with S/H amp	SAR mode and Hybrid mode		3.9	5.1	5.1	5.1	mA	—
		ACMPHS(1unit)			99	192	192	192	µA	—
		Temperature sensor			0.1	0.2	0.2	0.2	mA	—
		During D/A conversion (per unit)			1.2	1.6	1.6	1.6	mA	—
		Waiting for A/D, D/A conversion (all units)			3.4	4.1	4.1	4.1	mA	—
		ADC16H, DAC12 in standby modes (all units)[*2]			1	16.0	22.4	42	µA	—
	Reference power supply current (VREFH0)	During 16-bit A/D conversion (unit 0)	SAR mode	AI_{REFH0}	70	120	120	120	µA	—
			Oversampling mode and Hybrid mode		200	310	310	310	µA	
		Waiting for 12-bit A/D conversion (unit 0)			14.00	14.00	14.00	14.00	µA	—
		ADC16H in standby modes (unit 0)			0.01	0.12	0.1	0.2	µA	—
	Reference power supply current (VREFH)	During 16-bit A/D conversion (unit 1)	SAR mode	AI_{REFH}	70	120	120	120	µA	—
			Oversampling mode and Hybrid mode		200	310	310	310	µA	—
		During D/A conversion (per unit)			29	41.0	41.0	41.0	µA	—
		Waiting for 16-bit A/D (unit 1), D/A (all units) conversion			14	14	14	14	µA	—
		ADC16H in standby modes (unit 1)			0.1	0.1	0.2	0.3	µA	—
	USB operating current	Low speed	USBFS	$I_{CCUSBLS}$	2.9	4.0	4.0	4.0	mA	VCC_USB
		Full speed	USBFS	$I_{CCUSBFS}$	4.0	4.7	4.7	4.7	mA	VCC_USB

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD21 (16-Bit A/D Converter Module Stop bit) is in the module-stop state.

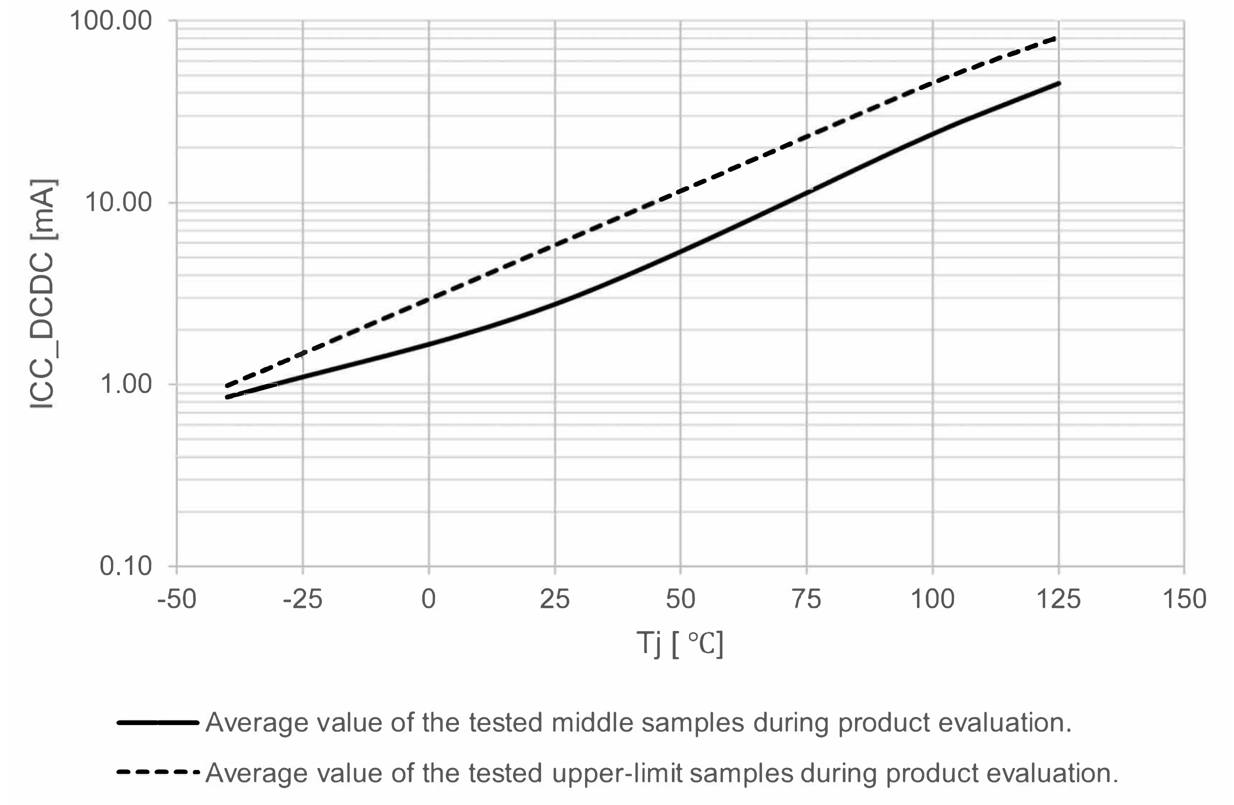


Figure 2.3 Temperature dependency in Software Standby mode (ICC_DCDC, SS2LP_0, SVSCR_1) (reference data)

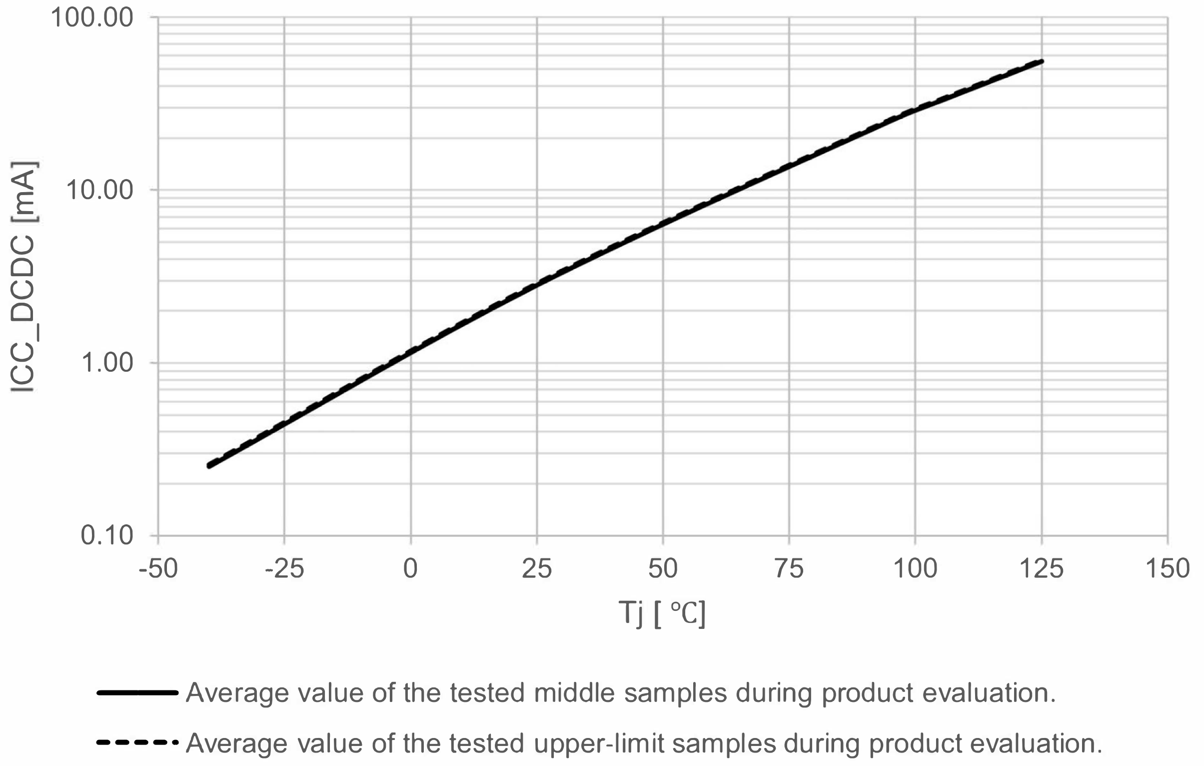


Figure 2.4 Temperature dependency in Software Standby mode (ICC_DCDC, SS2LP_0, SVSCR_5) (reference data)

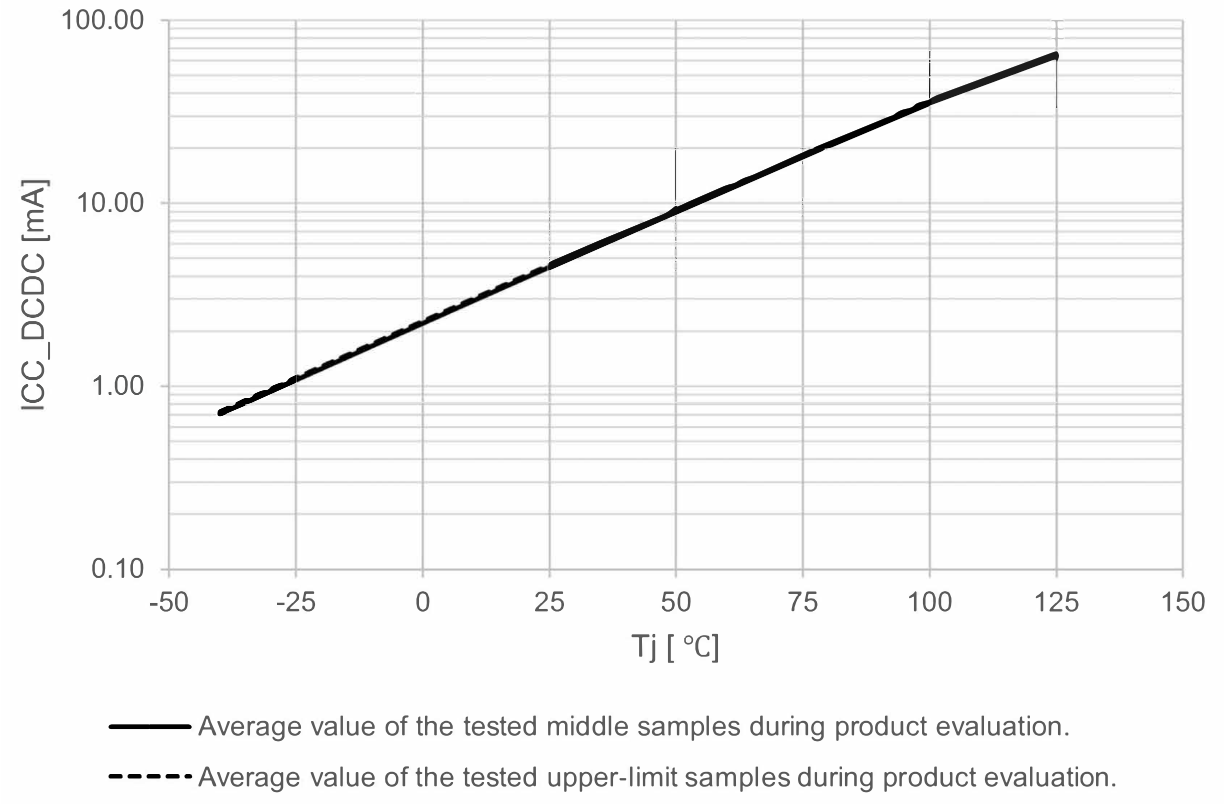


Figure 2.5 Temperature dependency in Software Standby mode (ICC_DCDC, SS2LP_1, SVSCR_2) (reference data)

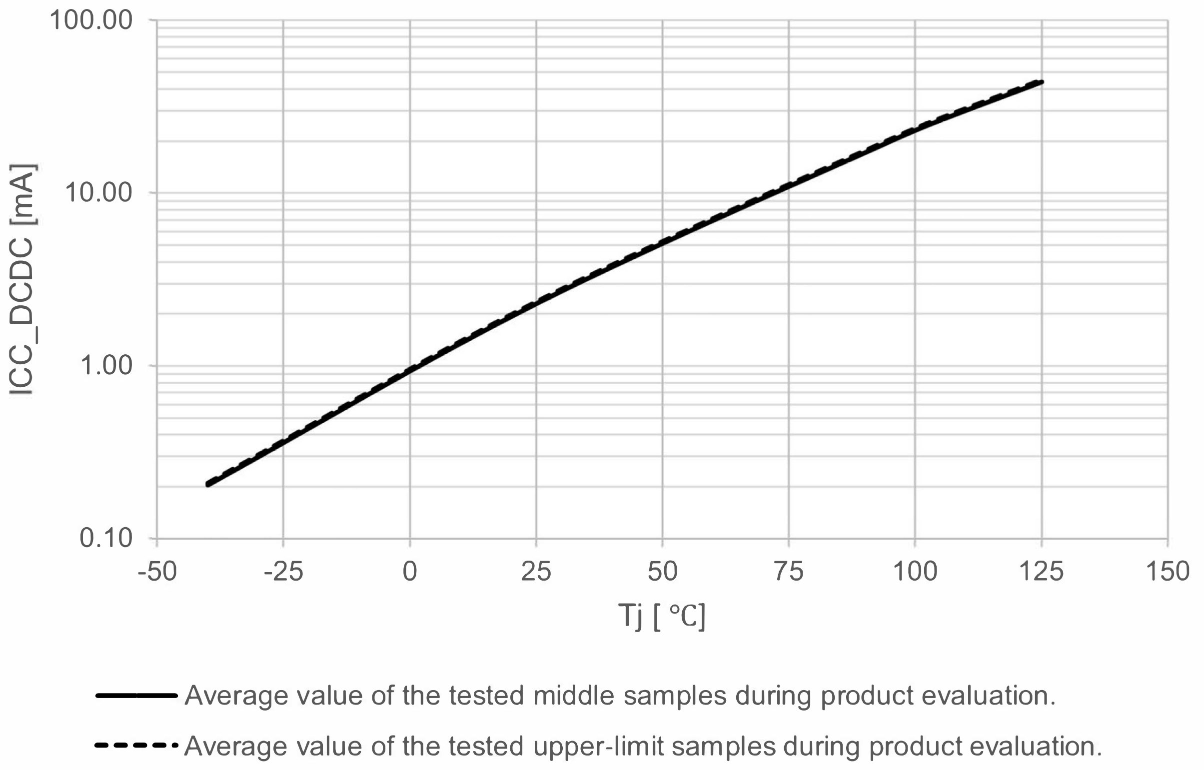


Figure 2.6 Temperature dependency in Software Standby mode (ICC_DCDC, SS2LP_1, SVSCR_5) (reference data)

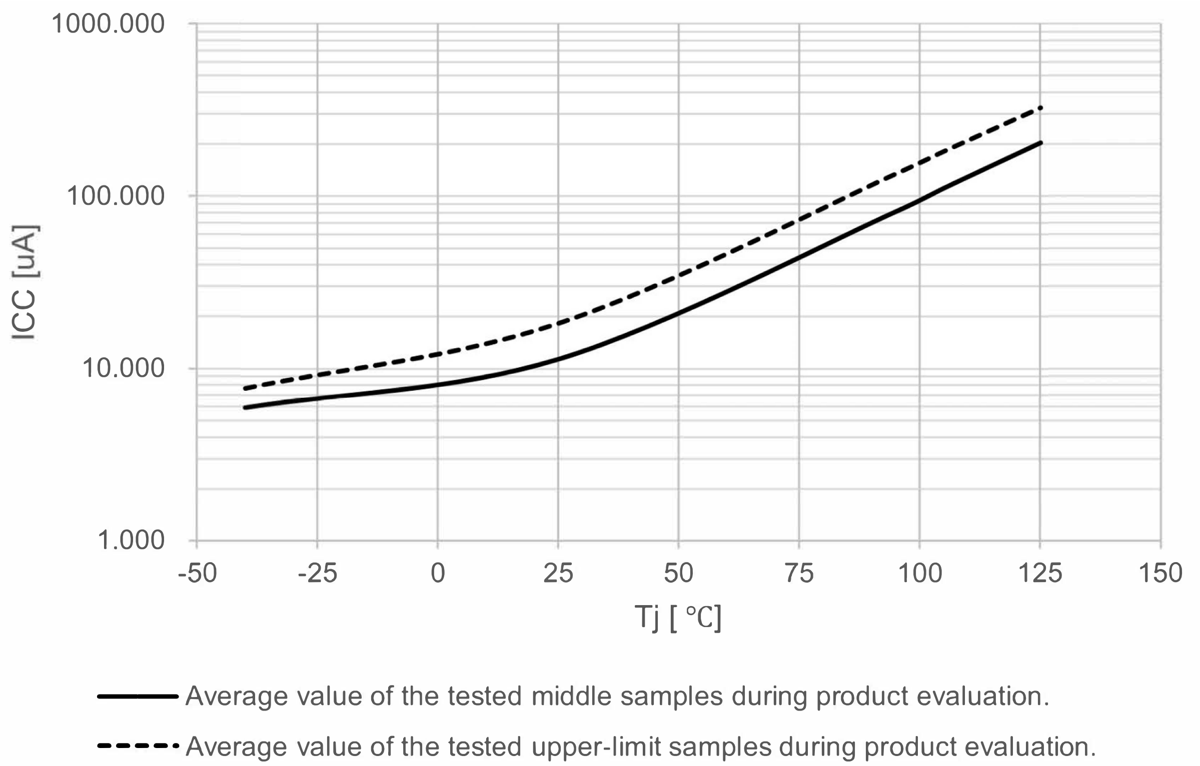


Figure 2.7 Temperature dependency in Deep Software Standby mode 1 (reference data)

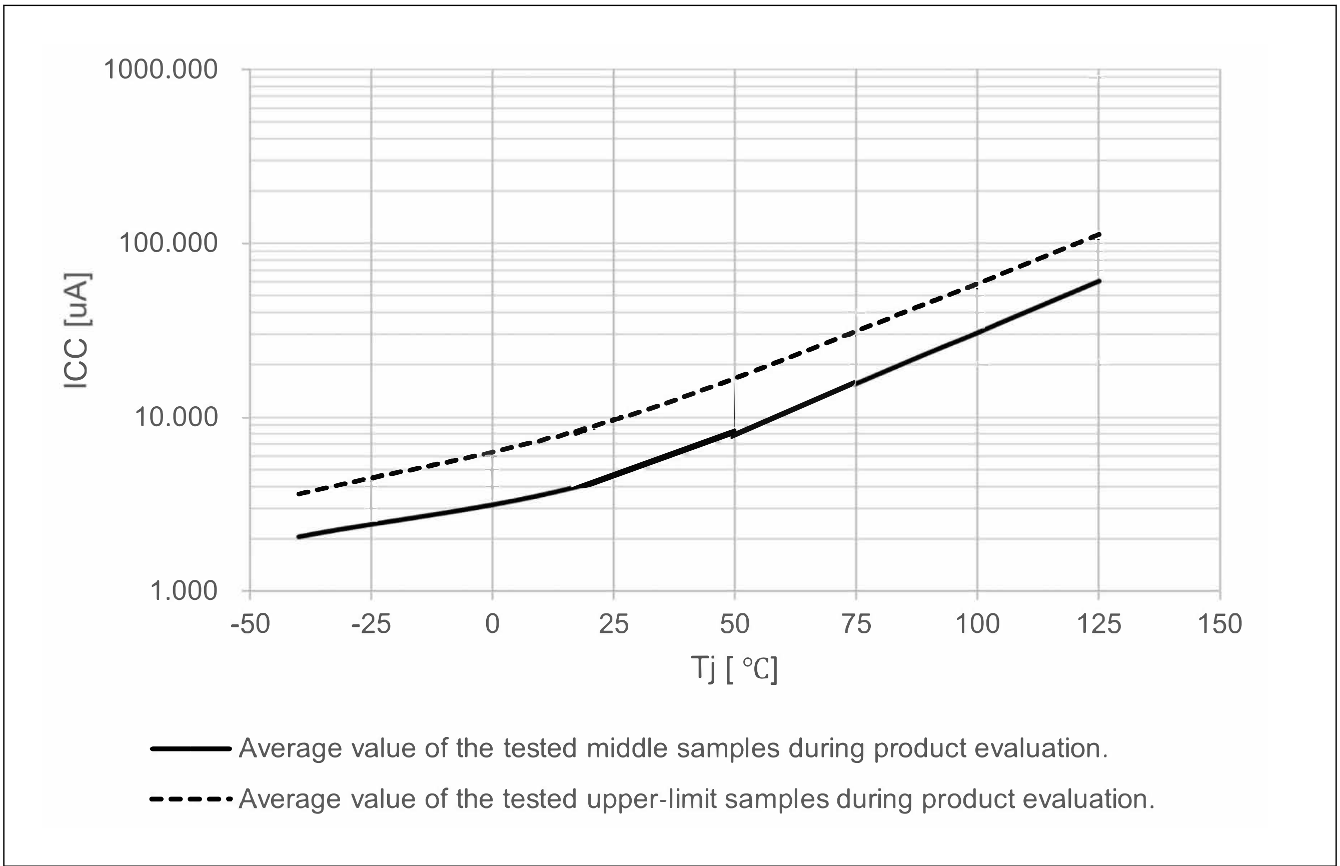


Figure 2.8 Temperature dependency in Deep Software Standby mode 2 (reference data)

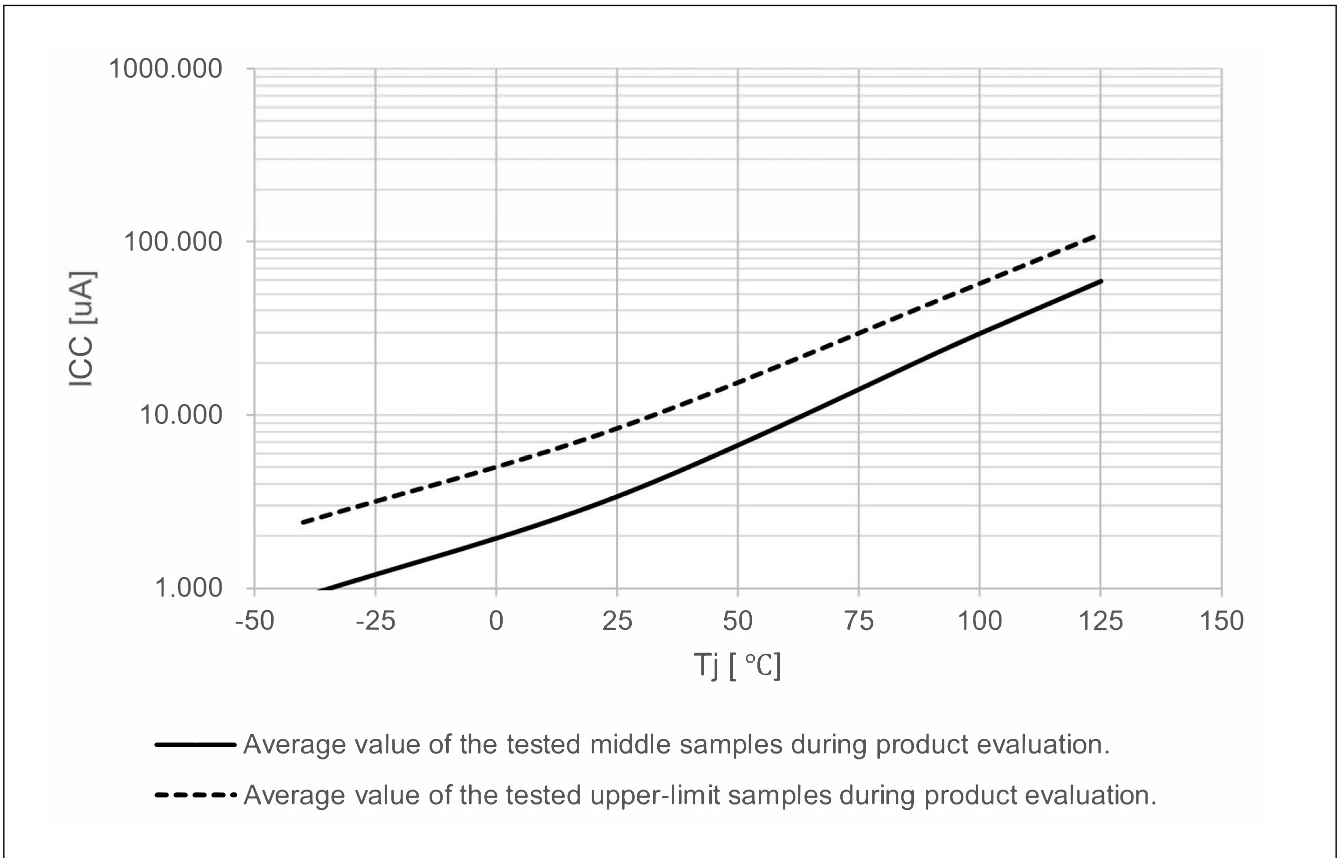


Figure 2.9 Temperature dependency in Deep Software Standby mode 3 (reference data)

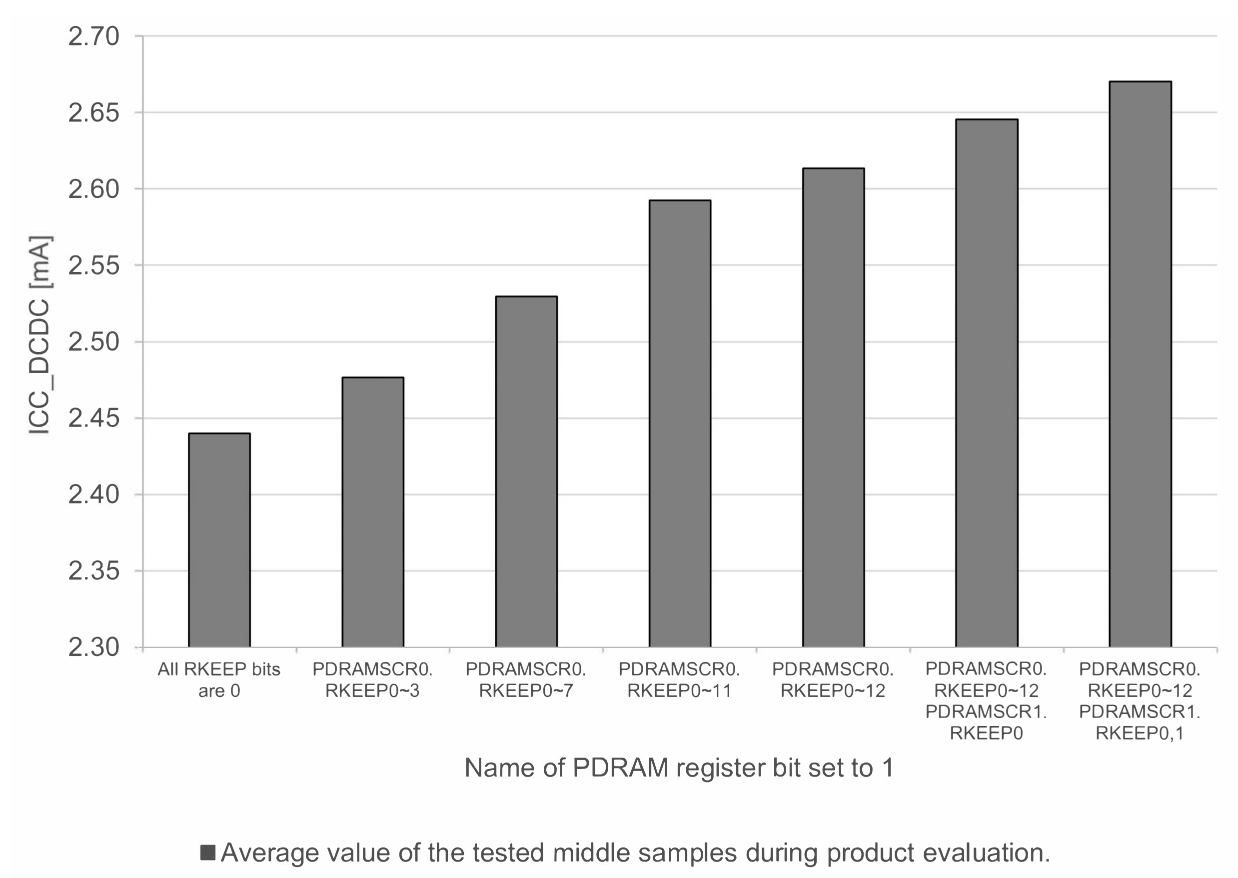


Figure 2.10 Software Standby current per SRAM state (ICC_DCDC, SS2LP_0, SVSCR_1) (reference data)

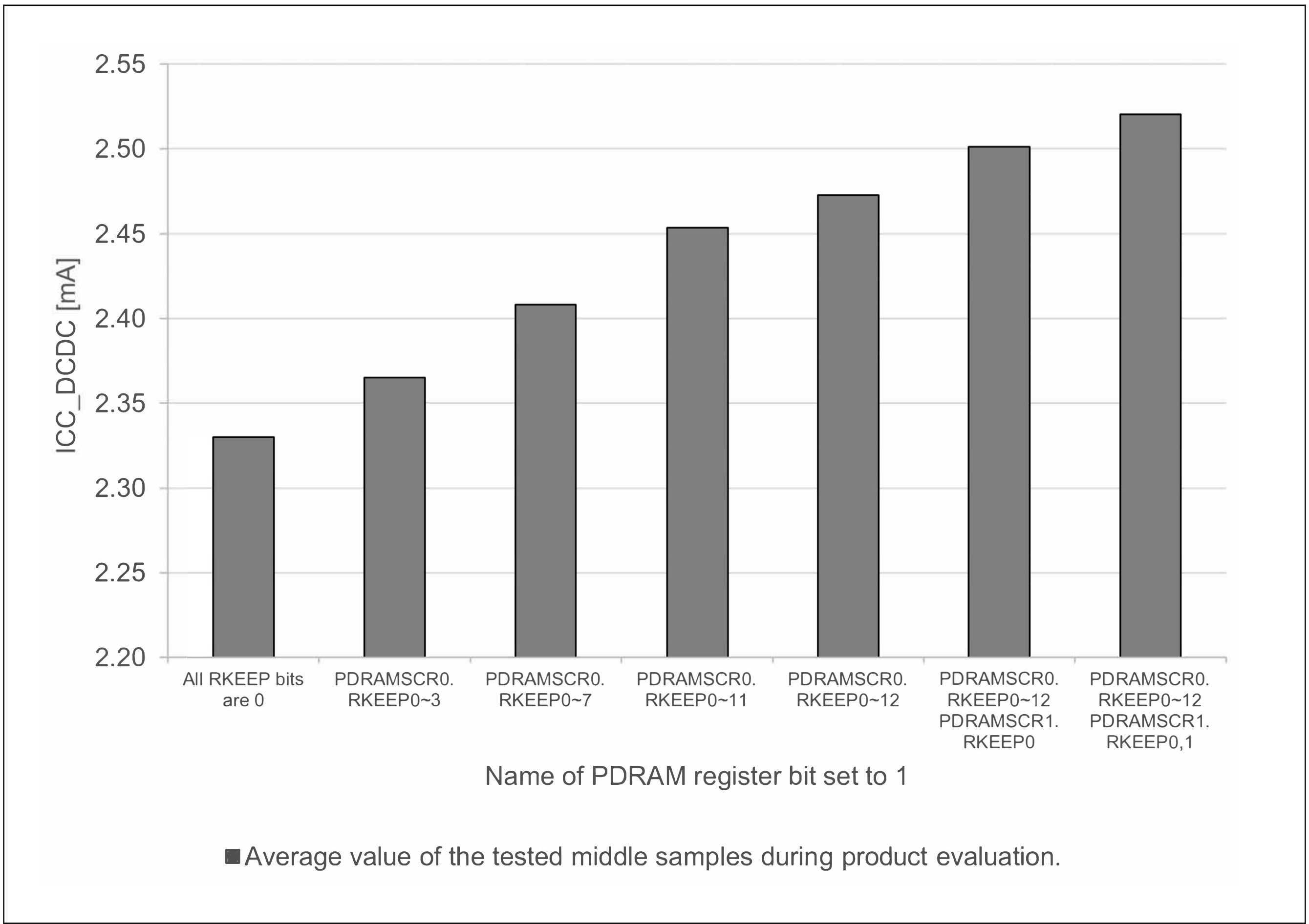


Figure 2.11 Software Standby current per SRAM state (ICC_DCDC, SS2LP_0, SVSCR_2) (reference data)

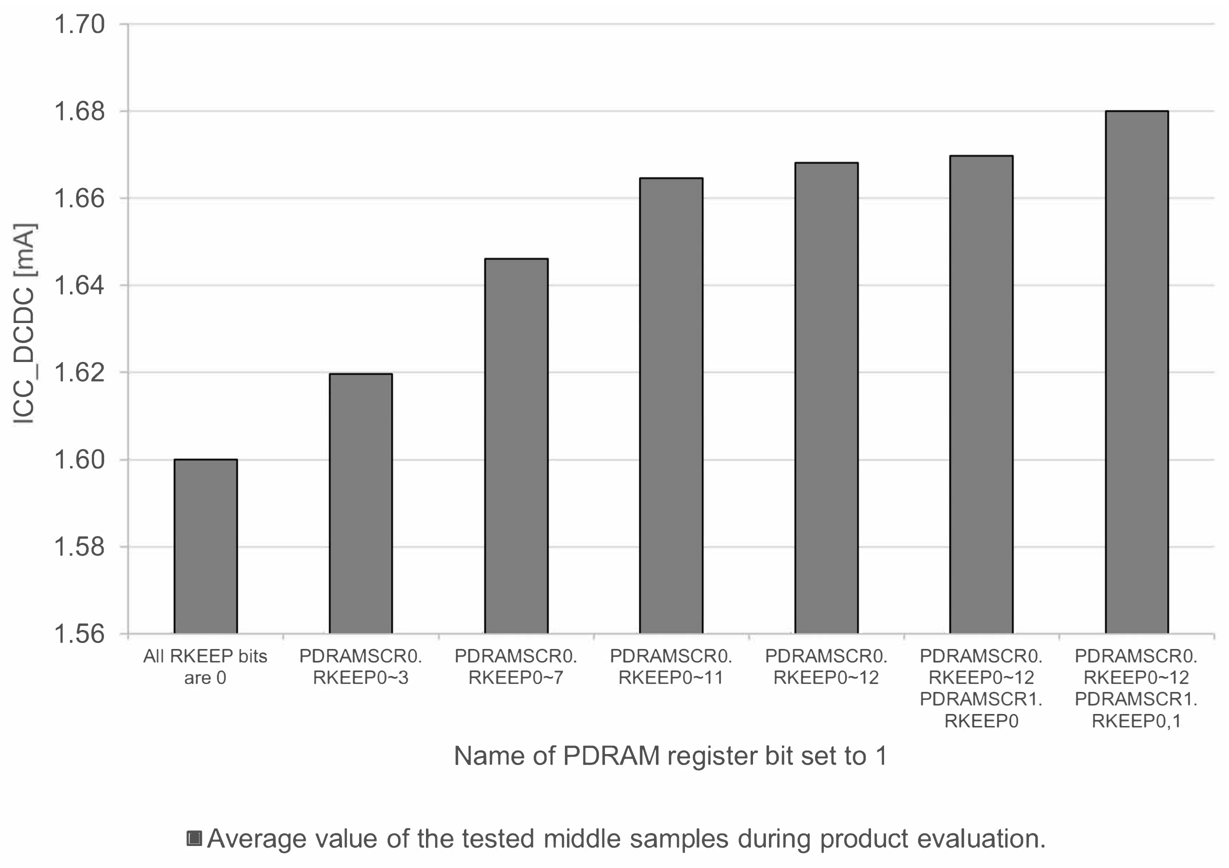


Figure 2.12 Software Standby current per SRAM state (ICC_DCDC, SS2LP_0, SVSCR_3) (reference data)

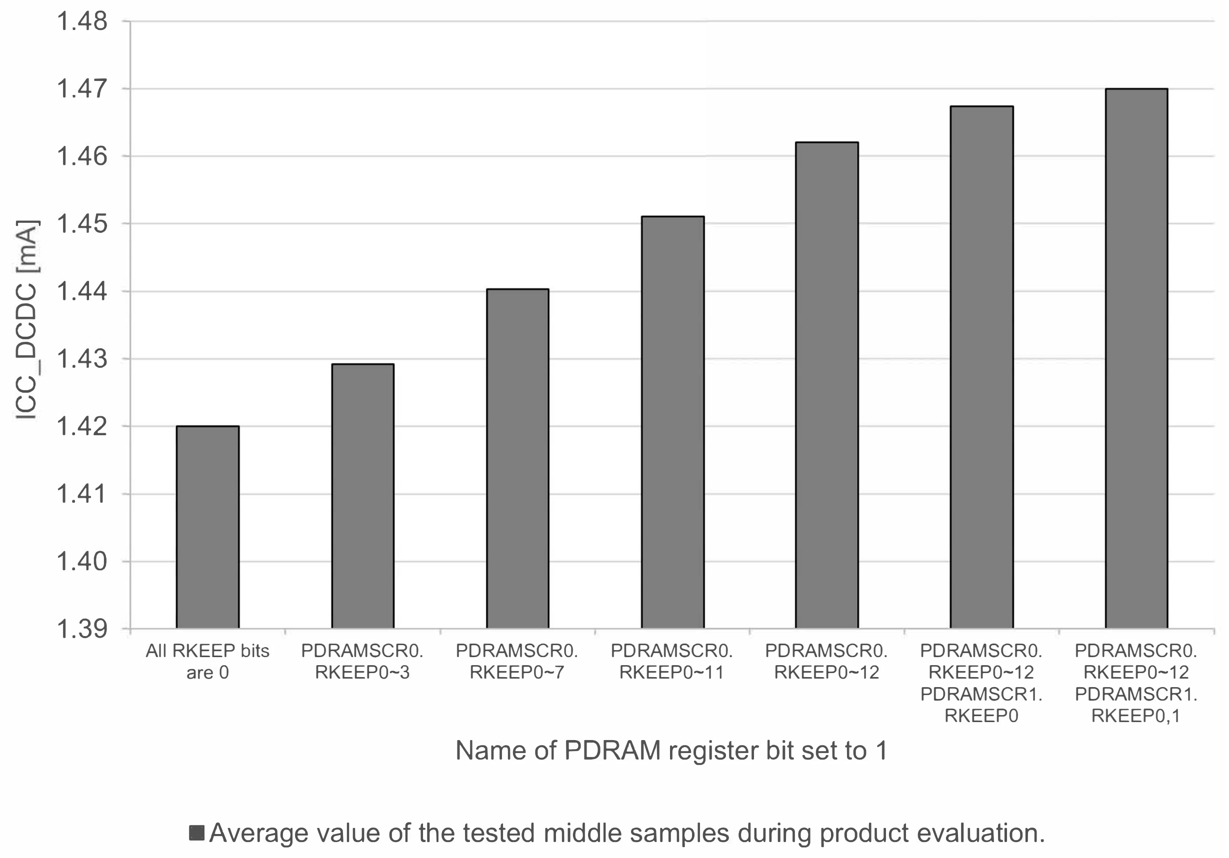


Figure 2.13 Software Standby current per SRAM state (ICC_DCDC, SS2LP_0, SVSCR_4) (reference data)

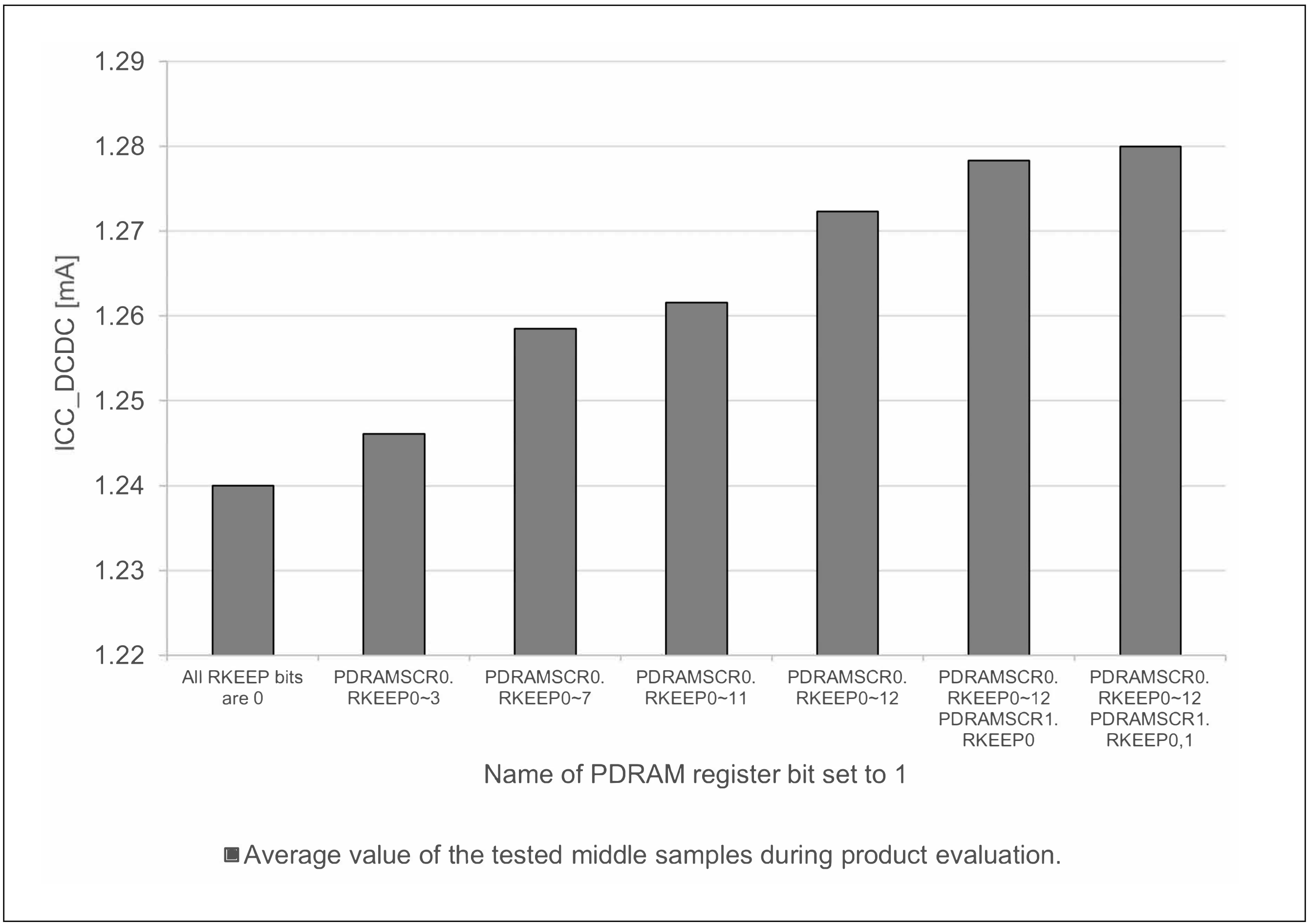


Figure 2.14 Software Standby current per SRAM state (ICC_DCDC, SS2LP_0, SVSCR_5) (reference data)

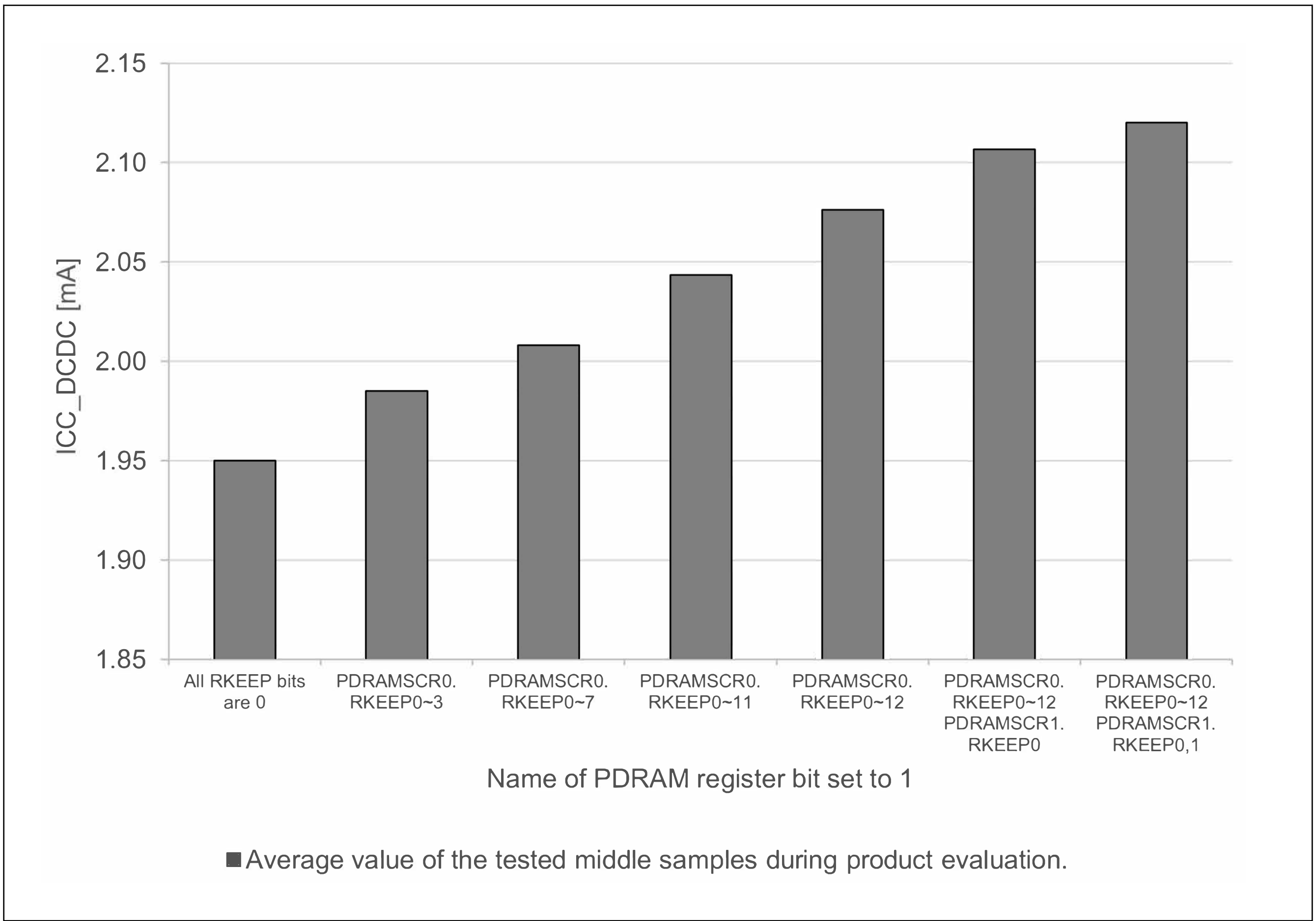


Figure 2.15 Software Standby current per SRAM state (ICC_DCDC, SS2LP_1, SVSCR_2) (reference data)

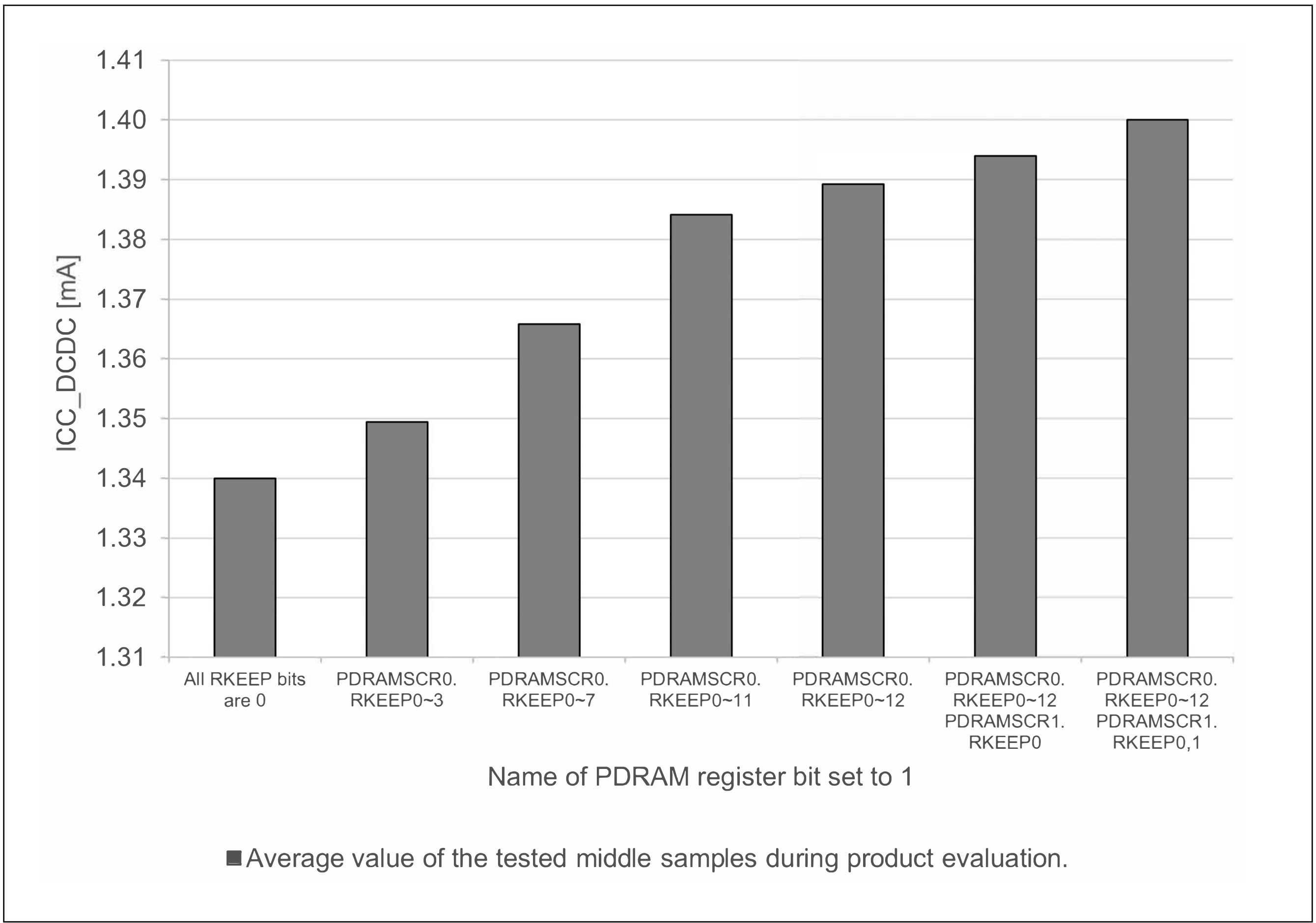


Figure 2.16 Software Standby current per SRAM state (ICC_DCDC, SS2LP_1, SVSCR_3) (reference data)

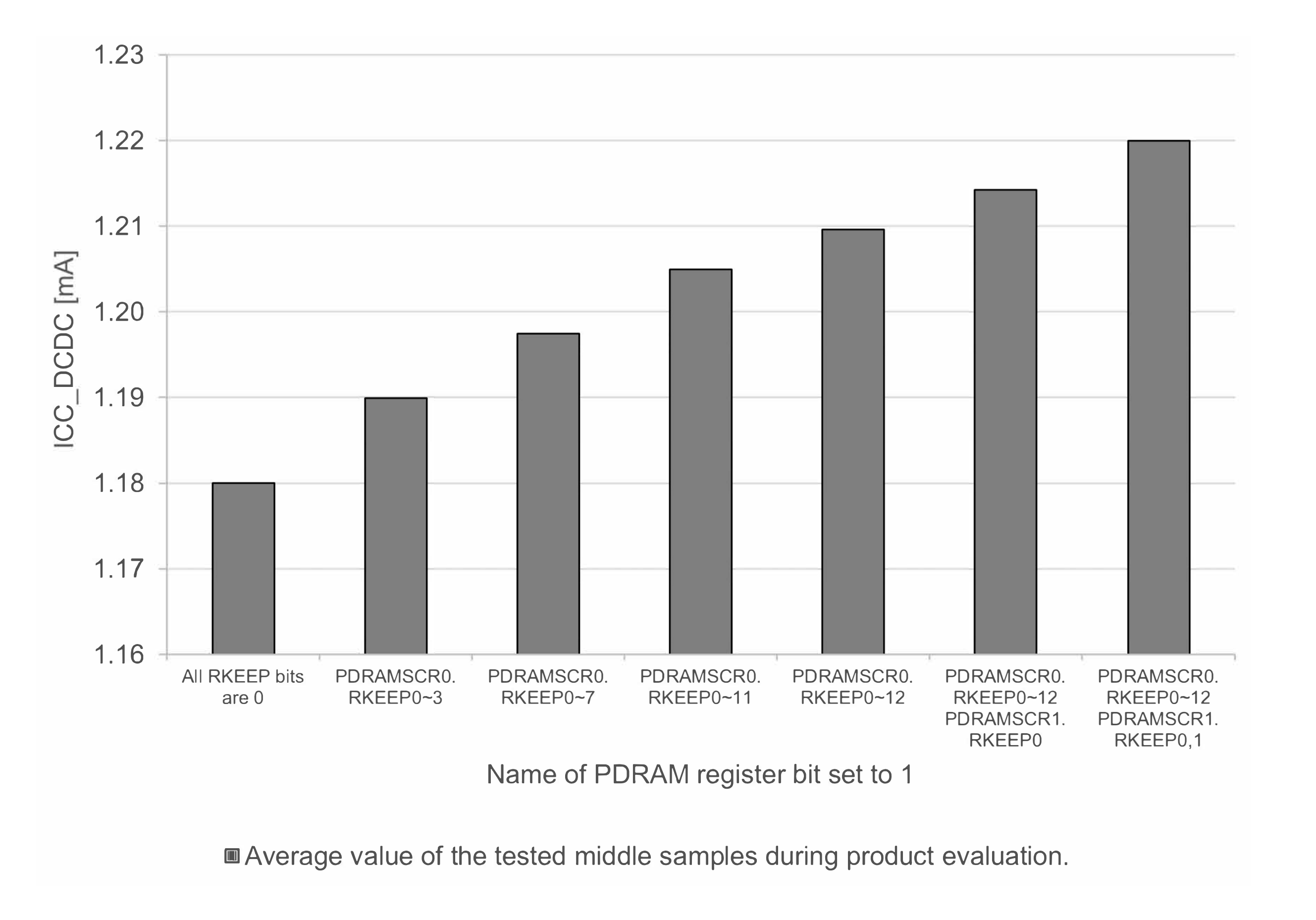


Figure 2.17 Software Standby current per SRAM state (ICC_DCDC, SS2LP_1, SVSCR_4) (reference data)

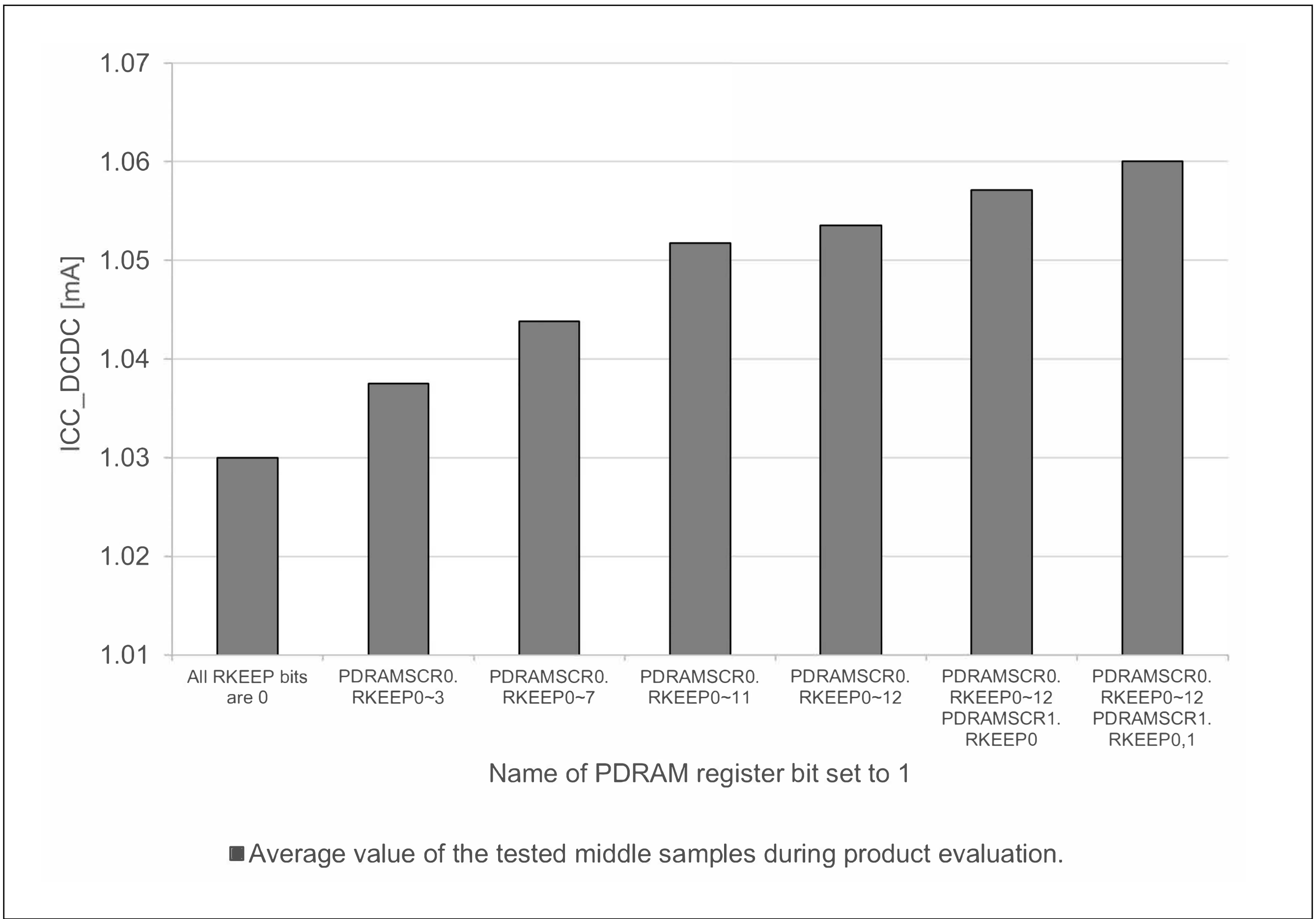


Figure 2.18 Software Standby current per SRAM state (ICC_DCDC, SS2LP_1, SVSCR_5) (reference data)

The more practical I_{CC_DCDC} value can be obtained with the following formula.

$I_{CC\_DCDC} = (I_{DD} \times VCL) / (VCC\_DCDC \times efficiency)$

Where: VCL and VCC are the voltage of VCL pin and VCC pin respectively, and efficiency is shown in the following figures.

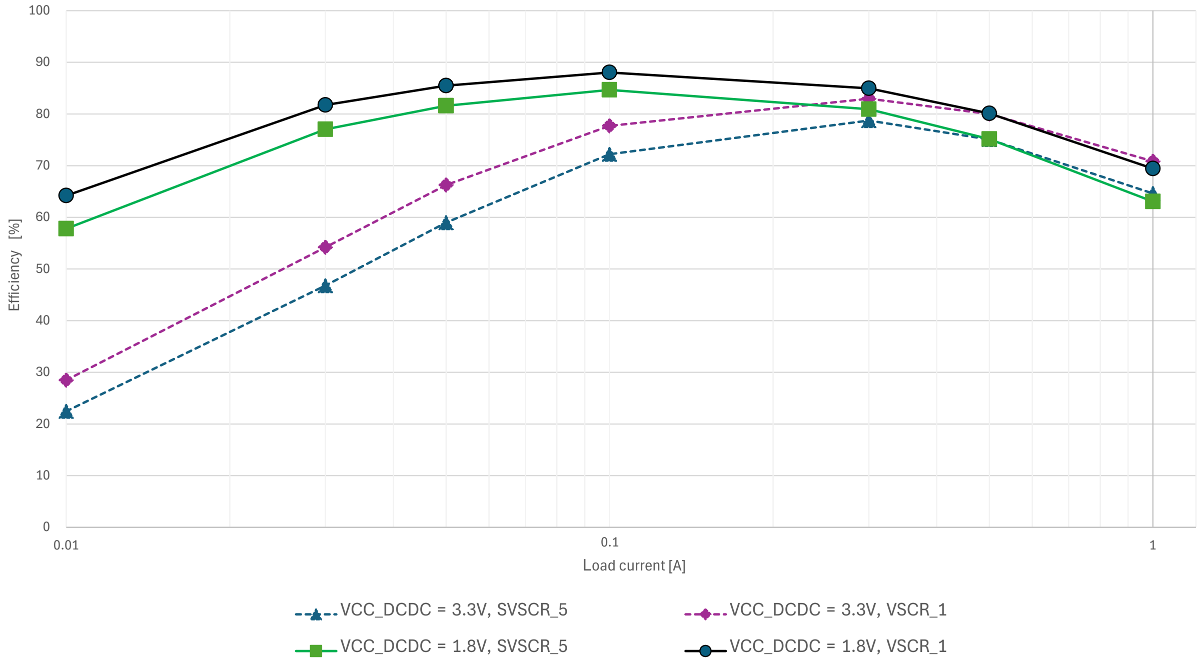


Figure 2.19 Typical DCDC efficiency (%) vs load current (A) in High-speed mode and Software Standby mode (SSCR1.SS2LP = SS2LP_1), Tj = 25 °C

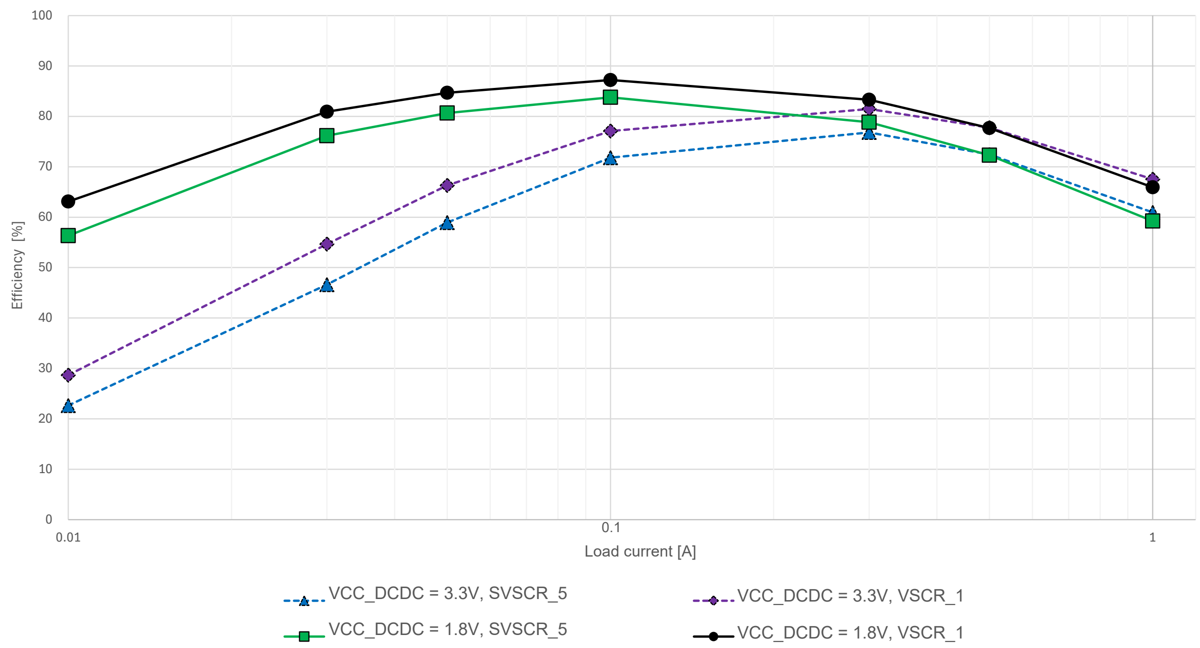


Figure 2.20 Typical DCDC efficiency (%) vs load current (A) in High-speed mode and Software Standby mode (SSCR1.SS2LP = SS2LP_0), Tj = 125 °C

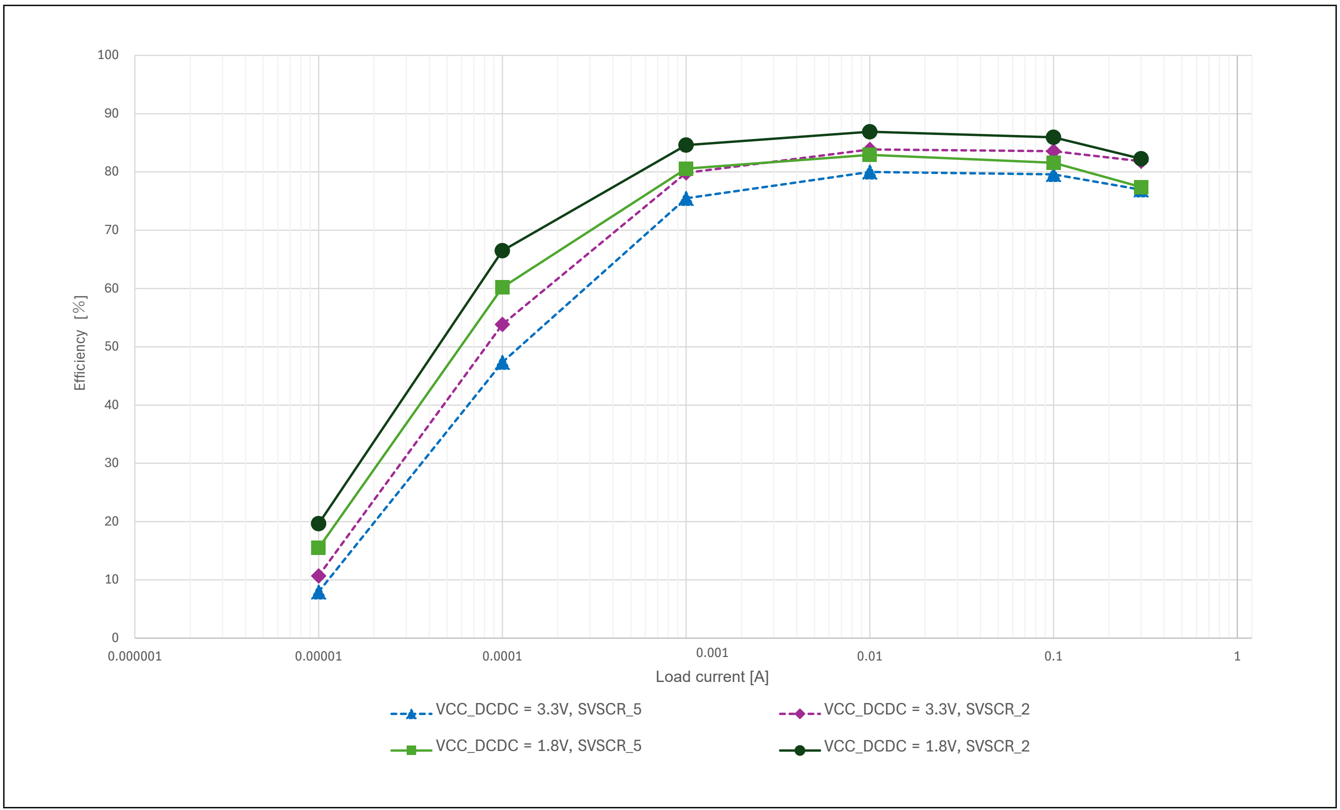


Figure 2.21 Typical DCDC efficiency (%) vs load current (A) in Software Standby mode (SSCR1.SS2LP = SS2LP_1), Tj = 25 °C

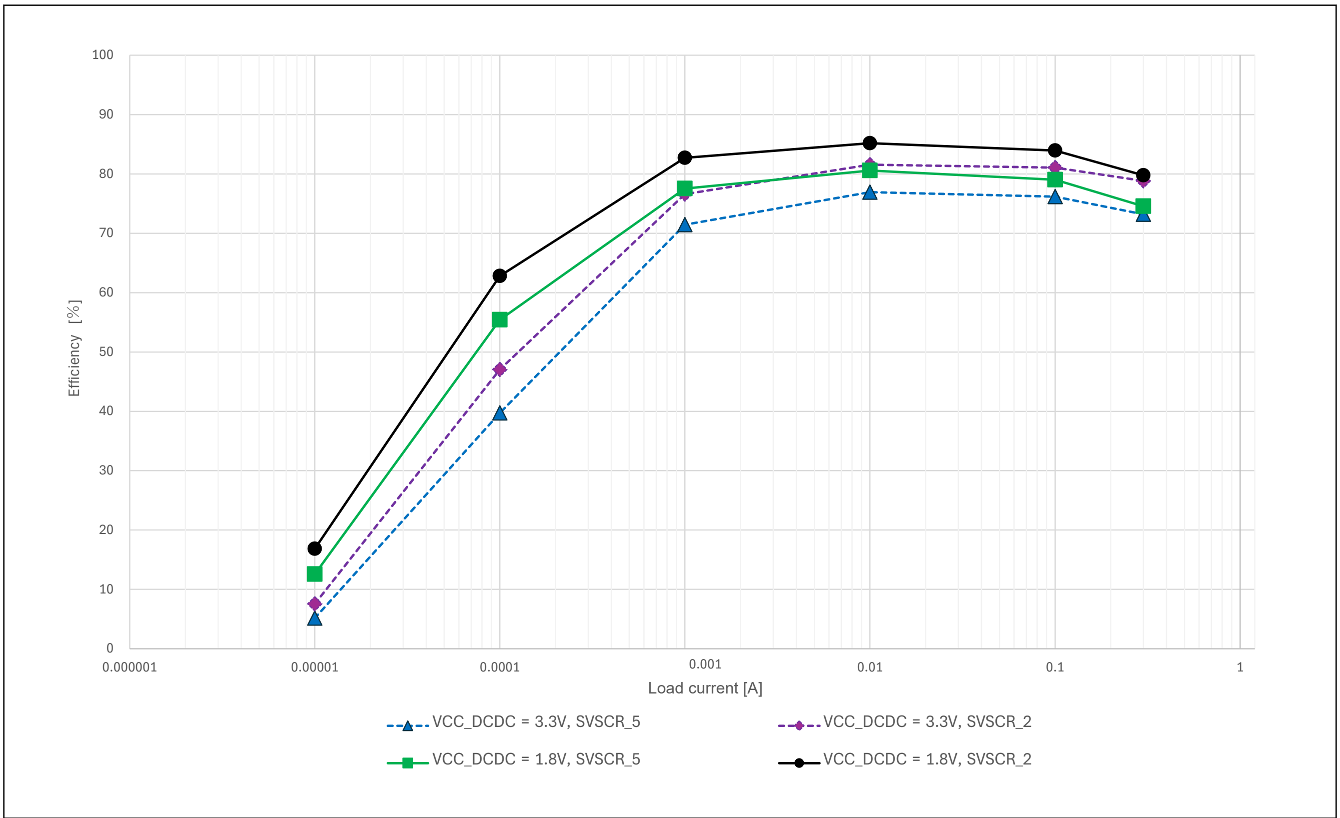


Figure 2.22 Typical DCDC efficiency (%) vs load current (A) in Software Standby mode (SSCR1.SS2LP = SS2LP_1), Tj = 125 °C

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.40 VCC rise and fall gradient characteristics at power on/off

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient at power on[*1]		SrVCC	0.0084	—	20	ms/V	—
VCC falling gradient at power off	VBATT function is disabled[*1]	SfVCC1	0.0084	—	—	ms/V	—
	VBATT function is enabled.	SfVCC2	1.0000	—	—		—

Note 1. In case the VCC voltage crosses V_{POR1}

Table 2.41 VCC ripple frequency and gradient characteristics during operation

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.63 V) and lower limit (1.62 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.23 $V_{r(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.23 $V_{r(VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.23 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC[*1]	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

Note 1. In case the VCC voltage does not cross V_{POR1}.

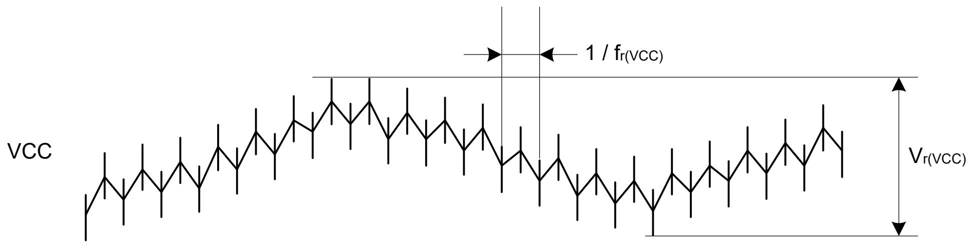


Figure 2.23 Ripple waveform

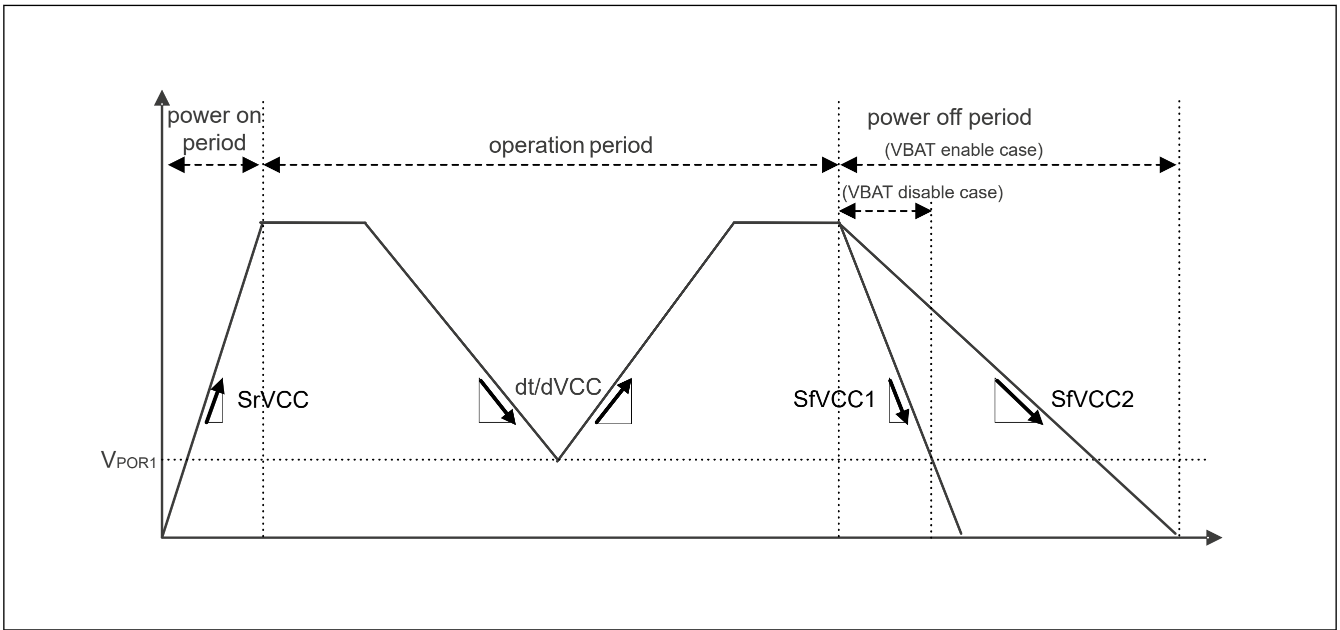


Figure 2.24 VCC rising and falling waveform

2.2.7 Power Supply Rise Gradient

Table 2.42 VCC_USB rise gradient characteristics at power on

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
VCC_USB rising gradient at power on	SrVCC_USB	8.4	—	—	μs/V	—

2.2.8 Thermal Characteristics

Maximum value of junction temperature (Tj) must not exceed the value of section 2.2.1. Tj/Ta Definition.

Tj is calculated by either of the following equations.

- Tj = Ta + θja × Total power consumption
- Tj = Tt + Ψjt × Total power consumption
  - Tj : Junction Temperature (°C)
  - Ta : Ambient Temperature (°C)
  - Tt : Top Center Case Temperature (°C)
  - θja : Thermal Resistance of "Junction"-to-"Ambient" (°C/W)
  - Ψjt : Thermal Resistance of "Junction"-to-"Top Center Case" (°C/W)
- Total power consumption = Voltage × (Leakage current + Dynamic current)
- Leakage current of IO = Σ (I_{OL} × V_{OL}) /Voltage + Σ (|I_{OH}| × |VCC – V_{OH}|) /Voltage
- Dynamic current of IO = Σ IO (C_{in} + C_{load}) × IO switching frequency × Voltage
  - C_{in}: Input capacitance
  - C_{load}: Output capacitance

Regarding θja and Ψjt, see Table 2.43.

Table 2.43 Thermal Resistance

Parameter	Package	Symbol	Value[*1]	Unit	Test conditions
Thermal Resistance	176-pin HLQFP (PLQP0176K?-A)	θja	15	°C/W	JESD 51-2 and 51-7 compliant
	224-pin BGA (PLBG0224J?-A)		21		JESD 51-2 and 51-9 compliant
	289-pin BGA (PLBG0289J?-A)		20		
	303-pin BGA (PLBG0303G?-A)		17		
	176-pin HLQFP (PLQP0176K?-A)	Ψjt	0.3	°C/W	JESD 51-2 and 51-7 compliant
	224-pin BGA (PLBG0224J?-A)		0.3		JESD 51-2 and 51-9 compliant
	289-pin BGA (PLBG0289J?-A)		0.3		
	303-pin BGA (PLBG0303G?-A)		0.5		

Note 1. The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, see the JEDEC standards.

2.2.8.1 Calculation Guide of Maximum Current

Table 2.44 Power consumption of each unit (DCDC mode) (1 of 3)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [μA/MHz]	Current [mA]	Condition
Leakage current	Analog	Regulator and Leak[*1]	Tj = 95°C	I_{CC}	—	—	2.51	—
			Tj = 105°C		—	—	2.91	
			Tj = 115°C		—	—	3.45	
			Tj = 125°C		—	—	4.15	
			Tj = 95°C	I_{CC_DCDC}	—	—	186	VCC_DCDC = 3.3 V, VSCR_1, PDCTRESWM .PDDE = 0
			Tj = 105°C		—	—	216	
			Tj = 115°C		—	—	243	
			Tj = 125°C		—	—	277	
			Tj = 95°C		—	—	363	VCC_DCDC = 1.8 V, VSCR_1, PDCTRESWM .PDDE = 0
			Tj = 105°C		—	—	421	
			Tj = 115°C		—	—	474	
			Tj = 125°C		—	—	540	
			Tj = 95°C	I_{DD}	—	—	477	VSCR_1 PDCTRESWM .PDDE = 0
			Tj = 105°C		—	—	553	
			Tj = 115°C		—	—	622	
			Tj = 125°C		—	—	709	

Table 2.44 Power consumption of each unit (DCDC mode) (2 of 3)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [μA/MHz]	Current [mA]	Condition
Dynamic current	CPU0	Operation with Cache	CoreMark	I_{DD}	1000	145	144	CPUCLK0 = 1000 MHz VSCR_1
	CPU1	Operation with Cache	CoreMark		250	166	41	CPUCLK1 = 250 MHz VSCR_1
	Peripheral Unit	Timer	RTC		62.5	1.229	0.077	VSCR_1
			GPT32 (14ch)*2		125	65.123	8.140	
			POEG (4 Groups)*2		62.5	1.539	0.096	
			PDG (4ch)*2		125	47.465	5.933	
			AGT (2ch)*2		62.5	1.518	0.095	
			ULPT (2ch)*2		62.5	2.373	0.148	
			WDT0		62.5	0.437	0.027	
			WDT1		62.5	0.446	0.028	
			IWDT		62.5	0.014	0.001	
Dynamic current	Peripheral Unit	Communication interfaces	ESWM	I_{DD}	125	294.026	36.753	VSCR_1
			ESC		125	14.095	1.762	
			USBFS		62.5	7.495	0.468	
			SCI (10ch)*2		125	32.336	4.042	
			IIC (3ch)*2		62.5	3.722	0.233	
			I3C		125	9.883	1.235	
			CANFD (2ch)*2		125	6.025	0.753	
			SPI (2ch)*2		125	11.36	1.420	
			OSPI (2ch)*2		62.5	100.8	6.300	
			SDHI (2ch)*2		62.5	9.858	0.616	
			DSMIF (2ch)*2		125	31.614	3.952	
		Analog	ADC16H (2 units)*2		125	66.267	8.283	VSCR_1
			DAC12 (2ch)*2		62.5	0.325	0.020	
			TSN		62.5	0.115	0.007	
			ACMPHS (4ch)*2		62.5	0.173	0.011	
		Event link	ELC		62.5	5.075	0.317	VSCR_1
		Security	RSIP-E50D		125	302.444	37.806	VSCR_1
			DOTF (2ch)*2		62.5	131.817	8.239	
		Data processing	CRC		125	1.455	0.182	
			DOC		125	0.241	0.030	VSCR_1
		System	CAC		62.5	0.946	0.059	
		DMA	DMAC0 (per 1ch)		250	7.278	1.819	VSCR_1
			DMAC1 (per 1ch)		250	6.858	1.715	VSCR_1
			DTC0		250	9.077	2.269	
			DTC1		250	8.716	2.179	

Table 2.44 Power consumption of each unit (DCDC mode) (3 of 3)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [μA/MHz]	Current [mA]	Condition
Dynamic current	FSBL operation			I_{DD}	250	—	81.1	FSBLCLK[2:0] = 111
					200	—	67.0	FSBLCLK[2:0] = 110
					150	—	51.7	FSBLCLK[2:0] = 101
					133	—	47.2	FSBLCLK[2:0] = 100

Note 1. Regulator and Leak are Internal voltage regulator's current and MCU's leakage current.
It is selected according to the temperature of Tj.

Note 2. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.45 Power consumption of each unit (External VDD mode) (1 of 3)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [μA/MHz]	Current [mA]	Condition
Leakage Current	Analog	Regulator and Leak*1	T_j = 95℃	I_{CC}	—	—	2.51	—
			T_j = 105℃		—	—	2.91	
			T_j = 115℃		—	—	3.45	
			T_j = 125℃		—	—	4.15	
			Tj = 95℃	I_{DD}	—	—	477	VCL = voltage range 1, PDCTRESWM. PDDE = 0
			Tj = 105℃		—	—	553	
			Tj = 115℃		—	—	622	
			Tj = 125℃		—	—	709	
Dynamic Current	CPU0	Operation with Cache	CoreMark	I_{DD}	1000	145	144	CPUCLK0 = 1000 MHz, VCL = voltage range 1
	CPU1	Operation with Cache	CoreMark		250	166	41	CPUCLK1 = 250 MHz, VCL = voltage range 1

Table 2.45 Power consumption of each unit (External VDD mode) (2 of 3)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [μA/MHz]	Current [mA]	Condition
Dynamic Current	Peripheral Unit	Timer	RTC	I_{DD}	62.5	1.229	0.077	VCL = voltage range 1
			GPT32 (14ch)*2		125	65.123	8.140	
			POEG (4 Groups)*2		62.5	1.539	0.096	
			PDG (4ch)*2		125	47.465	5.933	
			AGT (2ch)*2		62.5	1.518	0.095	
			ULPT (2ch)*2		62.5	2.373	0.148	
			WDT0		62.5	0.437	0.027	
			WDT1		62.5	0.446	0.028	
			IWDT		62.5	0.014	0.001	
		Communication interfaces	ESWM	I_{DD}	125	294.026	36.753	VCL = voltage range 1
			ESC		125	14.095	1.762	
			USBFS		62.5	7.495	0.468	
			SCI (10ch)*2		125	32.336	4.042	
			IIC (3ch)*2		62.5	3.722	0.233	
			I3C		125	9.883	1.235	
			CANFD (2ch)*2		125	6.025	0.753	
			SPI (2ch)*2		125	11.36	1.420	
			OSPI (2ch) *2		62.5	100.8	6.300	
			SDHI (2ch)*2		62.5	9.858	0.616	
			DSMIF (2ch) *2		125	31.614	3.952	
Dynamic Current	Peripheral Unit	Analog	ADC16H (2 units)*2	I_{DD}	125	66.267	8.283	VCL = voltage range 1
			DAC12 (2ch)*2		62.5	0.325	0.020	
			TSN		62.5	0.115	0.007	
			ACMPHS (4ch)*2		62.5	0.173	0.011	
		Event link	ELC	I_{DD}	62.5	5.075	0.317	VCL = voltage range 1
		Security	RSIP-E50D	I_{DD}	125	302.444	37.806	VCL = voltage range 1
			DOTF (2ch)*2		62.5	131.817	8.239	
		Data processing	CRC	I_{DD}	125	1.455	0.182	VCL = voltage range 1
			DOC		125	0.241	0.030	
		System	CAC	I_{DD}	62.5	0.946	0.059	VCL = voltage range 1
		DMA	DMAC0 (per 1ch)	I_{DD}	250	7.278	1.819	VCL = voltage range 1
			DMAC1 (per 1ch)		250	6.858	1.715	
			DTC0		250	9.077	2.269	
			DTC1		250	8.716	2.179	

Table 2.45 Power consumption of each unit (External VDD mode) (3 of 3)

Dynamic current/ Leakage current	MCU Domain	Category	Item	Symbol	Frequency [MHz]	Current [μA/MHz]	Current [mA]	Condition
Dynamic Current	FSBL operation			I_{DD}	250	—	79.9	FSBLCLK[2:0] = 111
					200	—	66.1	FSBLCLK[2:0] = 110
					150	—	51.0	FSBLCLK[2:0] = 101
					133	—	46.6	FSBLCLK[2:0] = 100

Note 1. Regulator and Leak are Internal voltage regulator’s current and MCU’s leakage current.
It is selected according to the temperature of Tj.
Note 2. To determine the current consumption per channel or unit, divide Current [mA] by the number of channels, groups or units.

Table 2.46 Outline of operation for each unit (1 of 2)

Peripheral	Outline of operation
RTC	RTC is operating with LOCO.
GPT	Operating modes is set to saw-wave PWM mode. GPT is operating with PCLKD
POEG	Only clear module stop bit.
PDG	PDG is applying delay of 1/128 times GTCLK period.
AGT	AGT is operating with PCLKB.
ULPT	ULPT is operating with LOCO.
WDT	WDT is operating with PCLKB.
IWDT	IWDT is operating with IWDTCLK.
ESWM	Communication mode is set to 1 Gbps, MAC Loop back. gPTP timer is enabled. ESWM is operating continuous transmission and reception on two ports simultaneously.
ESC	ESC is operating to access USERRAM from EtherCAT network.
USBFS	Transfer types are set to bulk transfer. USBFS is operating using Full-speed transfer (12 Mbps).
SCI	SCI is transmitting data in clock synchronous mode.
IIC	Communication format is set to I2C-bus format. IIC is transmitting data in master mode.
I3C	Communication format is set to I3C SDR format. I3C is transmitting data in master mode (12.5MHz).
CANFD	CANFD is transmitting and receiving data in self-test mode 1.
SPI	SPI mode is set to SPI operation (4-wire method). SPI master/slave mode is set to master mode. SPI is transmitting 32-bit width data.
OSPI	OSPI is issuing memory write command to HyperRAM.
SDHI	Transfer bus mode is set to 8-bit wide bus mode. SDHI is issuing CMD24 (single-block write).
DSMIF	DSMIF is capturing current data of 3 channels by capture trigger A.
ADC16H	Resolution is set to 16-bit accuracy. Conversion Data Operation Control B Register is set to 16 times average mode. ADC is converting the analog input in continuous scan mode. ADC is operating with ADCCLK.
DAC12	DAC12 is outputting the conversion result while updating the value of data register.
TSN	TSN is operating.
ACMPHS	ACMPHS is operating.
ELC	Only clear module stop bit.

Table 2.46 Outline of operation for each unit (2 of 2)

Peripheral	Outline of operation
RSIP-E50D	RSIP is doing self-test operation.
DOTF	DOTF is doing decryption with AES.
CRC	CRC is generating CRC code using 32-bit CRC32-C polynomial.
DOC	DOC is operating in data comparison mode.
CAC	Measurement target clocks is set to PCLKB. Measurement reference clocks is set to PCLKB. CAC is measuring the clock frequency accuracy.
DMAC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DMAC is transferring data from SRAM0 to SRAM0.
DTC	Bit length of transfer data is set to 32 bits. Transfer mode is set to block transfer mode. DTC is transferring data from SRAM0 to SRAM0.

2.2.8.2 Example of Tj Calculation

Assumption :

- Package 289-pin BGA : θja = 20 °C/W
- Ta = 65 °C
- I_{CC} + I_{CC_DCDC} = 320 mA
- VCC = 3.5 V (VCC = VCC2 = AVCC0 = VCC_USB
- I_{OH} = 1 mA, V_{OH} = VCC – 0.5 V, 12 Outputs
- I_{OL} = 20 mA, V_{OL} = 1.0 V, 8 Outputs
- I_{OL} = 1 mA, V_{OL} = 0.5 V, 12 Outputs
- C_{in} = 8 pF, 32 pins, Input frequency = 10 MHz
- C_{load} = 30 pF, 32 pins, Output frequency = 10 MHz

Static current of IO = Σ (VOL × IOL) / Voltage + Σ ((VCC - VOH) × IOH) / Voltage

= (20 mA × 1 V) × 8 / 3.5 V + (1 mA × 0.5 V) × 12 / 3.5 V + ((VCC - (VCC - 0.5 V)) × 1 mA) × 12 / 3.5 V

= 45.7 mA + 1.71 mA + 1.71 mA

= 49.1 mA

Dynamic current of IO = Σ IO (Cin + Cload) × IO switching frequency × Voltage

= ((8 pF × 32) × 10 MHz + (30 pF × 32) × 10 MHz) × 3.5 V

= 42.6 mA

Total power consumption = Voltage × (Static current + Dynamic current)

= (320 mA × 3.5 V) + (49.1 mA + 42.6 mA) × 3.5 V

= 1441 mW (1.441 W)

Tj = Ta + θja × Total power consumption

= 65 °C + 20 °C/W × 1.441W

= 93.82 °C

2.3 AC Characteristics

2.3.1 Frequency

Table 2.47 Operation frequency value in high-speed mode (1 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	PLL1 output clock P (PLL1P)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	1000	MHz
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	800	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	600	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	600	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	600	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	600	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	600	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	600	
	Other PLL output clock (PLL1Q, PLL1R, PLL2P, PLL2Q, PLL2R)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	1200	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	1200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	1200	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	1200	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	1200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	1200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	1200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	1200	

Table 2.47 Operation frequency value in high-speed mode (2 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	CPU0 clock (CPUCLK0)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	1000	MHz
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	800	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	600	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	600	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	600	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	600	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	600	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	600	
	CPU1 clock (CPUCLK1)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	250	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	150	

Table 2.47 Operation frequency value in high-speed mode (3 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	250	MHz
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	150	

Table 2.47 Operation frequency value in high-speed mode (4 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	MRAM bus clock (MRICLK)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	250	MHz
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	150	
	MRAM clock (MRPCLK)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	125	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	100	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	100	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	100	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	75	

Table 2.47 Operation frequency value in high-speed mode (5 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	Peripheral module clock (PCLKA)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	125	MHz
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	100	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	100	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	100	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	75	
	Peripheral module clock (PCLKB)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	62.5	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	50	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	50	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	37.5	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	37.5	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	37.5	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	50	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	37.5	

Table 2.47 Operation frequency value in high-speed mode (6 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	Peripheral module clock (PCLKD)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	250	MHz
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	150	
	Peripheral module clock (PCLKE)	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	250	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	200	
		BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	150	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	200	
		HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	150	

Table 2.47 Operation frequency value in high-speed mode (7 of 8)

Parameter				Symbol	Min	Typ	Max	Unit
Operation frequency	External bus clock (BCLK)	VCC ≥ 2.7 V	BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)	f	—	—	125	MHz
			BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	100	
			BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode), voltage range 1 (External VDD mode)		—	—	100	
			BGA package, 0 °C ≤ Tj ≤ 95 °C (Product group A), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
			BGA package, –40 °C ≤ Tj ≤ 105 °C (Product group B), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
			BGA package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode), voltage range 2 (External VDD mode)		—	—	75	
			HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_1 (DCDC mode)		—	—	100	
			HLQFP package, –40 °C ≤ Tj ≤ 125 °C (Product group C), VSCR_2 (DCDC mode)		—	—	75	
		VCC ≥ 1.62 V			—	—	60	
	EBCLK pin output	VCC ≥ 2.7 V			—	—	60	
		VCC ≥ 1.62 V			—	—	30	
	SDCLK pin output	VCC ≥ 3.0 V			—	—	133	

Table 2.47 Operation frequency value in high-speed mode (8 of 8)

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	SCI clock (SCICLK)		f	—	—	120	MHz
	SPI clock (SPICLK)			—	—	333	
	Octal SPI clock (OCTACLK)			—	—	333	
	CANFD core clock (CANFDCLK)			—	—	80	
	ADC clock (ADCCLK)			25	—	120	
	GPT clock (GPTCLK)			—*1	—	300	
	USB clock (USBCLK)			—	—	48	
	I3C clock (I3CCLK)			—	—	200	
	Asynchronous external bus clock (BCLKA)			—	—	133	
	EtherSW clock (ESWCLK)	BGA package		—	—	250	
		HLQFP package		—	—	125	
	EtherSW-PHY clock (ESWPHYCLK)			—	—	500	
	EtherCAT clock (ESCCLK)			—	—	100	
	EtherCAT-PHY clock (ESCPHYCLK)			—	—	50	
	DSMIF clock (DSMIFCLK)			—	—	300	

Note 1. When the GPTCLK is used for A/D conversion clock, the GPTCLK frequency must be at least 25 MHz.

2.3.2 Clock Timing

Table 2.48 Clock timing except for sub-clock oscillator (1 of 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	VCC = 2.70 V or above	t_{Bcyc}	16.6	—	—	ns	Figure 2.25
	VCC = 1.62 V or above		33.3	—	—		
EBCLK pin output high pulse width	VCC = 2.70 V or above	t_{CH}	3.3	—	—	ns	
	VCC = 1.62 V or above		9.6	—	—		
EBCLK pin output low pulse width	VCC = 2.70 V or above	t_{CL}	3.3	—	—	ns	
	VCC = 1.62 V or above		9.6	—	—		
EBCLK pin output rise time	VCC = 2.70 V or above	t_{Cr}	—	—	5.0	ns	
	VCC = 1.62 V or above		—	—	7.0		
EBCLK pin output fall time	VCC = 2.70 V or above	t_{Cf}	—	—	5.0	ns	
	VCC = 1.62 V or above		—	—	7.0		
SDCLK pin output cycle time		t_{SDcyc}	7.52	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	1.0	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	1.0	—	—	ns	
SDCLK pin output rise time		t_{Cr}	—	—	2.7	ns	
SDCLK pin output fall time		t_{Cf}	—	—	2.7	ns	
EXTAL external clock input cycle time		t_{EXcyc}	20.80	—	—	ns	Figure 2.26
EXTAL external clock input high pulse width		t_{EXH}	5.30	—	—	ns	
EXTAL external clock input low pulse width		t_{EXL}	5.30	—	—	ns	
EXTAL external clock rise time		t_{EXr}	—	—	3.0	ns	
EXTAL external clock fall time		t_{EXf}	—	—	3.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	—	48	MHz	—

Table 2.48 Clock timing except for sub-clock oscillator (2 of 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Main clock oscillation stabilization wait time (crystal)*1		$t_{MAINOSCWT}$	—	—	—*1	ms	Figure 2.27
LOCO clock oscillation frequency		f_{LOCO}	29.4912	32.768	36.0448	kHz	—
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	—	—	26.0	μs	Figure 2.28
MOCO clock oscillation frequency		F_{MOCO}	7.2	8.0	8.8	MHz	—
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	—	—	3.5	μs	—
HOCO clock oscillator oscillation frequency	Without FLL (Standard Product)	f_{HOCO16}	15.776	16.000	16.224	MHz	–20 ≤ Tj ≤ 105 °C
		f_{HOCO18}	17.748	18.000	18.252		
		f_{HOCO20}	19.720	20.000	20.280		
		f_{HOCO32}	31.552	32.000	32.448		
		f_{HOCO48}	47.328	48.000	48.672		
		f_{HOCO16}	15.712	16.000	16.288		–40 ≤ Tj ≤ 125 °C
		f_{HOCO18}	17.676	18.000	18.324		
		f_{HOCO20}	19.640	20.000	20.360		
		f_{HOCO32}	31.424	32.000	32.576		
		f_{HOCO48}	47.136	48.000	48.864		
	Without FLL (SiP Product)	f_{HOCO16}	15.744	16.000	16.256		–20 ≤ Tj ≤ 105 °C
		f_{HOCO18}	17.712	18.000	18.288		
		f_{HOCO20}	19.680	20.000	20.320		
		f_{HOCO32}	31.488	32.000	32.512		
		f_{HOCO48}	47.232	48.000	48.768		
		f_{HOCO16}	15.680	16.000	16.320		–40 ≤ Tj ≤ 125 °C
		f_{HOCO18}	17.640	18.000	18.360		
		f_{HOCO20}	19.600	20.000	20.400		
		f_{HOCO32}	31.360	32.000	32.640		
		f_{HOCO48}	47.040	48.000	48.960		
	With FLL	f_{HOCO16}	15.960	16.000	16.040		–40 ≤ Tj ≤ 125 °C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18.000	18.045		
		f_{HOCO20}	19.950	20.000	20.050		
		f_{HOCO32}	31.920	32.000	32.080		
		f_{HOCO48}	47.880	48.000	48.120		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	—	—	15.0	μs	—
HOCO stop width time		$t_{HOCOSTP}$	1	—	—	μs	Figure 2.31
HOCO period jitter		—	-3	—	3	ps	—
FLL stabilization wait time (Standard Product)		t_{FLLWT}	—	—	1.92	ms	—
FLL stabilization wait time (SiP Product)		t_{FLLWT}	—	—	2.15	ms	—
PLL1/PLL2 clock frequency		f_{PLL}	60	—	1200	MHz	—
PLL1/PLL2 clock oscillation stabilization wait time		t_{PLLWT}	—	—	50	μs	Figure 2.29
PLL1/PLL2 period jitter		—	—	±52	—	ps	—

Table 2.48 Clock timing except for sub-clock oscillator (3 of 3)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
PLL1/PLL2 long term jitter	—	—	±300	—	ps	Term: 1 µs, 10 µs

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation, and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (f_{HOCO}) reaches the range for guaranteed operation.

Table 2.49 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	—[*1]	s	Figure 2.30

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. A value that is two times the value shown is recommended.

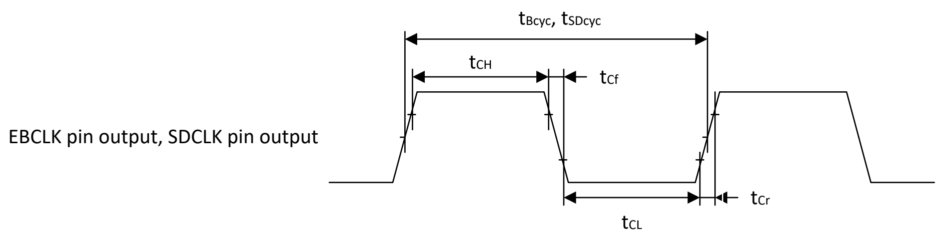


Figure 2.25 EBCLK and SDCLK output timing

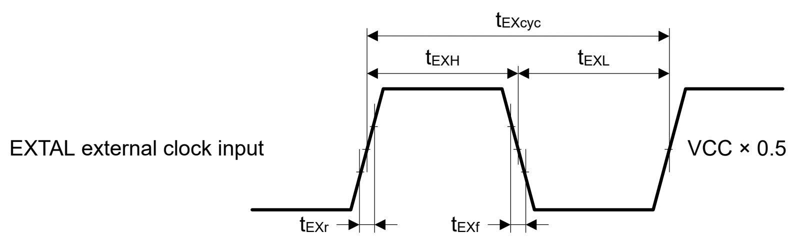


Figure 2.26 EXTAL external clock input timing

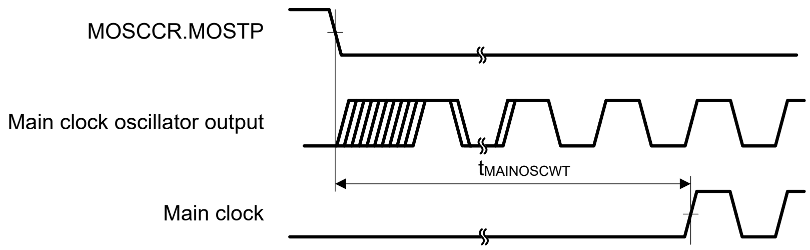


Figure 2.27 Main clock oscillation start timing

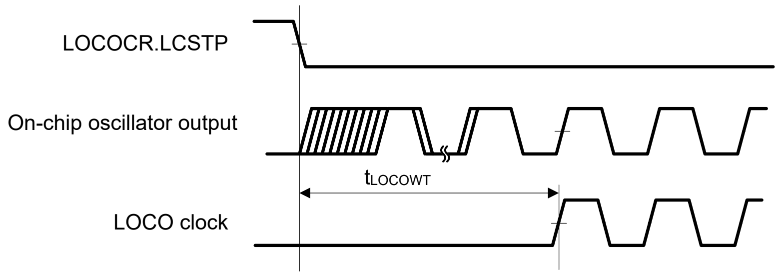
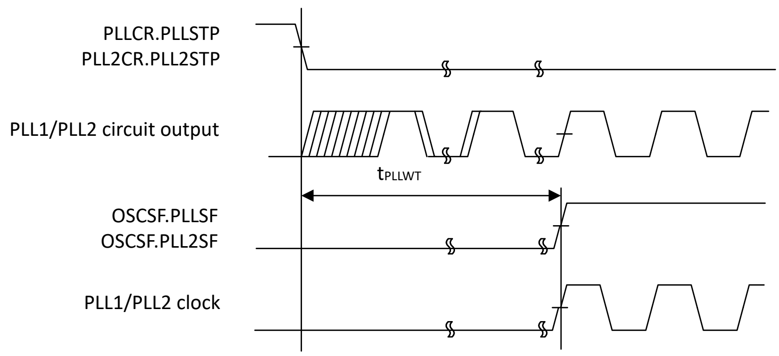


Figure 2.28 LOCO clock oscillation start timing



Note: Only operate the PLL is operated after main clock oscillation has stabilized.

Figure 2.29 PLL1/PLL2 clock oscillation start timing

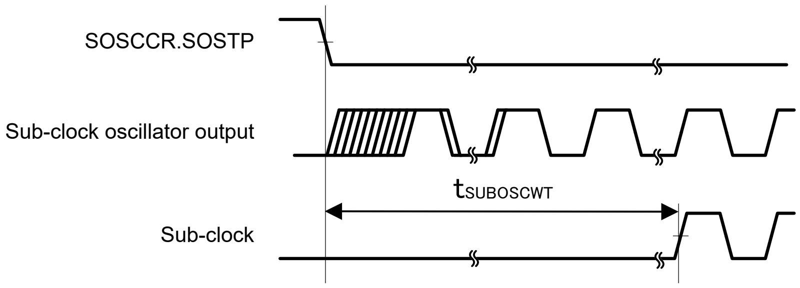


Figure 2.30 Sub-clock oscillation start timing

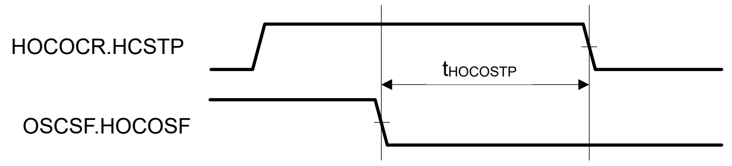


Figure 2.31 HOCO stop width time

2.3.3 Reset Timing

Table 2.50 Reset timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	—	t_{RESWP}	2.4	—	—	ms	Figure 2.32
	Deep Software Standby Mode 1	DPSBYCR.DCSSMODE = 01	t_{RESWD}	0.51	—	—	ms	Figure 2.33
		DPSBYCR.DCSSMODE = 10		0.67	—	—		
		DPSBYCR.DCSSMODE = 11		1.00	—	—		
	Deep Software Standby Mode 2	DPSBYCR.DCSSMODE = 01		0.51	—	—		
		DPSBYCR.DCSSMODE = 10		0.67	—	—		
		DPSBYCR.DCSSMODE = 11		1.00	—	—		
	Deep Software Standby Mode 3	DPSBYCR.DCSSMODE = 01		0.68	—	—		
		DPSBYCR.DCSSMODE = 10		0.84	—	—		
		DPSBYCR.DCSSMODE = 11		1.20	—	—		
	Software Standby Mode		t_{RESWS}	0.55	—	—	ms	
	CPU Deep Sleep mode (Subosc operation)		$t_{RESWSODS}$	0.16	—	—	ms	
	CPU Deep Sleep mode (Other than SOSC operation)		t_{RESWDS}	0.04	—	—	ms	
	SOSC operation	PGSCR.PGS = 1	t_{RESWSO}	0.27	—	—	ms	
		PGSCR.PGS = 0		0.30	—	—		
	Other than above	PGSCR.PGS = 1	t_{RESW}	0.15	—	—	ms	
		PGSCR.PGS = 0		0.18	—	—		
Wait time after RES cancellation			t_{RESWT}	—	78.7	79.1	μs	Figure 2.32
Wait time after internal reset cancellation (IWDT reset, WDT0/1 reset, CPU0/1 Lockup reset, Bus Error reset, Common Memory Error reset, Software reset, Local Memory 0/1 error reset, Temperature monitor reset)			t_{RESW2}	—	78.7	79.1	μs	—

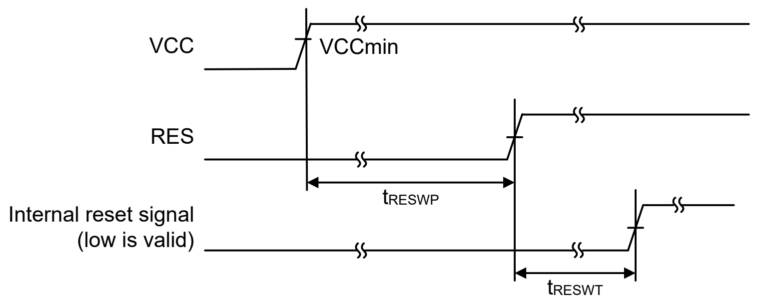


Figure 2.32 RES pin input timing under the condition that VCC exceeds V_{POR} voltage threshold

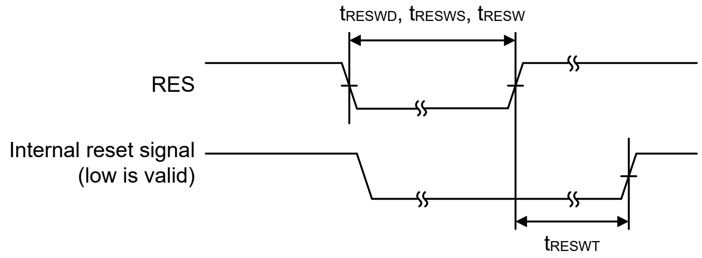


Figure 2.33 Reset input timing

2.3.4 Wakeup Timing

Table 2.51 Timing of recovery from low power modes (1 of 3)

Parameter		Fast return function*9	Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from CPU Deep Sleep mode	CPU0 Deep Sleep mode	—	t_{DSLP}*11	—	6.14	9.45	µs	—
	CPU1 Deep Sleep mode	—		—	7.71	15.66	µs	

Table 2.51 Timing of recovery from low power modes (2 of 3)

Parameter			Fast return function[*9]	Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode[*12]	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator[*1] MOSCSCR.MOSCSOKP = 0	Enabled	t_{SBYMC}[*10]	—	2.09	2.14	ms	Figure 2.34 The division ratio of all oscillators is 1.
		System clock source is main clock oscillator[*1] MOSCSCR.MOSCSOKP = 1	Enabled		—	44.9	94.6	µs	
		System clock source is PLL1P with main clock oscillator[*2] MOSCSCR.MOSCSOKP = 0	Enabled	t_{SBYPC}[*10]	—	2.21	2.27	ms	
		System clock source is PLL1P with main clock oscillator[*2] MOSCSCR.MOSCSOKP = 1	Enabled		—	135	197	µs	
	External clock input to main clock oscillator	System clock source is main clock oscillator[*3]	Enabled	t_{SBYEX}[*10]	—	44.9	94.6	µs	
		System clock source is PLL1P with main clock oscillator[*4]	Enabled	t_{SBYPE}[*10]	—	135	197		
	System clock source is sub-clock oscillator[*5]		Enabled	t_{SBYSC}[*10]	—	480	481	µs	
	System clock source is HOCO clock oscillator[*6]		Enabled	t_{SBYHO}[*10]	—	46.3	96.0	µs	
	System clock source is PLL1P with HOCO[*7]		Enabled	t_{SBYPH}[*10]	—	146	208	µs	
	System clock source is MOCO clock oscillator[*8]		Enabled	t_{SBYMO}[*10]	—	44.6	87.5	µs	

Table 2.51 Timing of recovery from low power modes (3 of 3)

Parameter			Fast return function*9	Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Deep Software Standby mode	Deep Software Standby mode 1	DPSBYCR.DCSSMODE[1:0] = 01	—	t_{DSBY}	—	296	346	µs	Figure 2.35
		DPSBYCR.DCSSMODE[1:0] = 10	—		—	456	506	µs	
		DPSBYCR.DCSSMODE[1:0] = 11	—		—	776	826	µs	
	Deep Software Standby mode 2	DPSBYCR.DCSSMODE[1:0] = 01	—		—	296	346	µs	
		DPSBYCR.DCSSMODE[1:0] = 10	—		—	456	506	µs	
		DPSBYCR.DCSSMODE[1:0] = 11	—		—	776	826	µs	
	Deep Software Standby mode 3	DPSBYCR.DCSSMODE[1:0] = 01	—		—	483	604	µs	
		DPSBYCR.DCSSMODE[1:0] = 10	—		—	643	764	µs	
		DPSBYCR.DCSSMODE[1:0] = 11	—		—	963	1084	µs	
Wait time after cancellation of Deep Software Standby mode			—	t_{DSBYWT}	22.2	—	33.6	µs	

Note 1. When the frequency of the crystal is 48 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 1.
Note 2. When the frequency of PLL1P is 1 GHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05) and the greatest value of the internal clock division setting is 16.
Note 3. When the frequency of the external clock is 48 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 1.
Note 4. When the frequency of PLL1P is 1 GHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00) and the greatest value of the internal clock division setting is 16.
Note 5. The Sub-clock oscillator frequency is 32.768 kHz and the greatest value of the internal clock division setting is 1.
Note 6. The HOCO frequency is 20 MHz and the greatest value of the internal clock division setting is 1.
Note 7. The PLL frequency is 1 GHz and the greatest value of the internal clock division setting is 16.
Note 8. The MOCO frequency is 8 MHz and the greatest value of the internal clock division setting is 1.
Note 9. For details, see SSCR1.SS2FR bit.
Note 10. The recovery time can be calculated with the equation of t_{Common} + max(t_{OSCSTB}, t_{PG1}, t_{PGCK}) + max(t_{PG2}, t_{LPW}). And they can be determined with the following values and equations. For n, the greatest value is selected from among the internal clock(CPUCLK0, CPUCLK1, NPUCLK, ICLK, MRICLK, MRPCLK, PCLKm, FCLK, BCLK and EBCLK) division settings (m = A to E).
t_{OSCSTB} in the table below means the time when each oscillator is active. When multiple oscillators are active, t_{OSCSTB} is determined by the longest t_{OSCSTB} among the active oscillators.
Note 11. The ICLK frequency is 250 MHz. This recovery time corresponds to t_{PG2}.
Note 12. When Ccyc is 27. See Table 2.53.

Table 2.52 Each element of recovery time

Mode	Wakeup time	Oscillation keep	Fast return function	Typ t_{Common}	Typ t_{OSCSTB} *1	Typ t_{PG1}	Typ t_{PGCK}	Typ t_{PG2}	Typ t_{LPW}	Max t_{Common}	Max t_{OSCSTB} *1	Max t_{PG1}	Max t_{PGCK}	Max t_{PG2}	Max t_{LPW}	Unit
Software Standby mode	t_{SBYMC}	MOSC disabled	Enabled	Ccyc*2/ f_{MOCO} + 2/f_{ICLK}	$t_{MAINOSCWT}$	t_{OSCSTB}/ f_{MOCO} + 208/ f_{MOCO} + 11.6	(10.5 + 2.5n)/ f_{MOCO} + 2.5/ f_{SRCCLK} + 2/ f_{ICLK}	18/ f_{MOCO} + 9/ f_{ICLK}	2/f_{ICLK} + 2n/ f_{MOSC} + 2/ f_{ICLK}	Ccyc*2/ f_{MOCO} + 2/f_{ICLK}	$t_{MAINOSCWT}$ + 11/0.236	t_{OSCSTB}/ f_{MOCO} + 208/ f_{MOCO} + 51.0	(10.5 + 2.5n)/ f_{MOCO} + 2.5/ f_{SRCCLK} + 2/ f_{ICLK}	18/ f_{MOCO} + 9/ f_{ICLK}	2/f_{ICLK} + 2n/ f_{MOSC} + 2/ f_{ICLK}	μs
		MOSC enabled	Enabled		3/0.262						14/0.236					μs
	t_{SBYPC}	MOSC disabled	Enabled		$t_{MAINOSCWT}$ +31/0.262				2/f_{ICLK} + 2n/ f_{PLL} + 2/f_{ICLK}		$t_{MAINOSCWT}$ + 42/0.236				2/f_{ICLK} + 2n/ f_{PLL} + 2/f_{ICLK}	μs
		MOSC enabled	Enabled		34/0.262						(14 + 31)/ 0.236					μs
	t_{SBYEX}	—	Enabled		3/0.262				2/f_{ICLK} + 2n/ f_{MOSC} + 2/ f_{ICLK}		14/0.236				2/f_{ICLK} + 2n/ f_{MOSC} + 2/ f_{ICLK}	μs
	t_{SBYPE}	—	Enabled		34/0.262				2/f_{ICLK} + 2n/ f_{PLL} + 2/f_{ICLK}		45/0.236				2/f_{ICLK} + 2n/ f_{PLL} + 2/f_{ICLK}	μs
	t_{SBYSC}	—	Enabled		0				2/f_{ICLK} + 2n/ f_{SOSC} + 2/ f_{ICLK}		0				2/f_{ICLK} + 2n/ f_{SOSC} + 2/ f_{ICLK}	μs
	t_{SBYHO}	—	Enabled		20				2/f_{ICLK} + 2n/ f_{HOCO} + 2/ f_{ICLK}		67				2/f_{ICLK} + 2n/ f_{HOCO} + 2/ f_{ICLK}	μs
	t_{SBYPH}	—	Enabled		140				2/f_{ICLK} + 2n/ f_{PLL} + 2/f_{ICLK}		202				2/f_{ICLK} + 2n/ f_{PLL} + 2/f_{ICLK}	μs
	t_{SBYMO}	—	Enabled		0				2/f_{ICLK} + 2n/ f_{MOCO} + 2/ f_{ICLK}		0				2/f_{ICLK} + 2n/ f_{MOCO} + 2/ f_{ICLK}	μs

Note: The unit of frequency is MHz.
Note 1. If more than one oscillator is operating, the largest value of the operating oscillator in this column is applied.
Note 2. For Ccyc, see Table 2.53.

Table 2.53 Ccyc value

SSCR1.SS2LP [1:0]	VSCR.VSCM[2:0]	SVSCR.SVSCM [2:0]	{PLL1LDOCR.LDOSTP, PLL2LDOCR.LDOSTP, PLL1LDOCR.SKEEP, PLL2LDOCR.SKEEP}	{HOCOLDOCR.LDOSTP, HOCOLDOCR.SKEEP}	Ccyc	Unit
00: SS2LP_0	001 : VSCR_1	001 : SVSCR_1	{1, 1, x, x} or {x, x, 1, 1}	{0, 0}	56	cycle
				Other than above	27	cycle
			Other than above	Don't care	237	cycle
		010 : SVSCR_2	Don't care	Don't care	379	cycle
		011 : SVSCR_3	Don't care	Don't care	591	cycle
		100 : SVSCR_4	Don't care	Don't care	696	cycle
		101 : SVSCR_5	Don't care	Don't care	802	cycle
	010 : VSCR_2	001 : SVSCR_1	Don't care	Don't care	379	cycle
		010 : SVSCR_2	{1, 1, x, x} or {x, x, 1, 1}	{0, 0}	56	cycle
				Other than above	27	cycle
			Other than above	Don't care	237	cycle
		011 : SVSCR_3	Don't care	Don't care	538	cycle
		100 : SVSCR_4	Don't care	Don't care	643	cycle
		101 : SVSCR_5	Don't care	Don't care	749	cycle
01: SS2LP_1	001 : VSCR_1	010 : SVSCR_2	Don't care	Don't care	514	cycle
		011 : SVSCR_3	Don't care	Don't care	726	cycle
		100 : SVSCR_4	Don't care	Don't care	831	cycle
		101 : SVSCR_5	Don't care	Don't care	937	cycle
	010 : VSCR_2	010 : SVSCR_2	{1, 1, x, x} or {x, x, 1, 1}	Don't care	162	cycle
			Other than above	Don't care	327	cycle
		011 : SVSCR_3	Don't care	Don't care	673	cycle
		100 : SVSCR_4	Don't care	Don't care	778	cycle
		101 : SVSCR_5	Don't care	Don't care	884	cycle

Note: x: Don't care

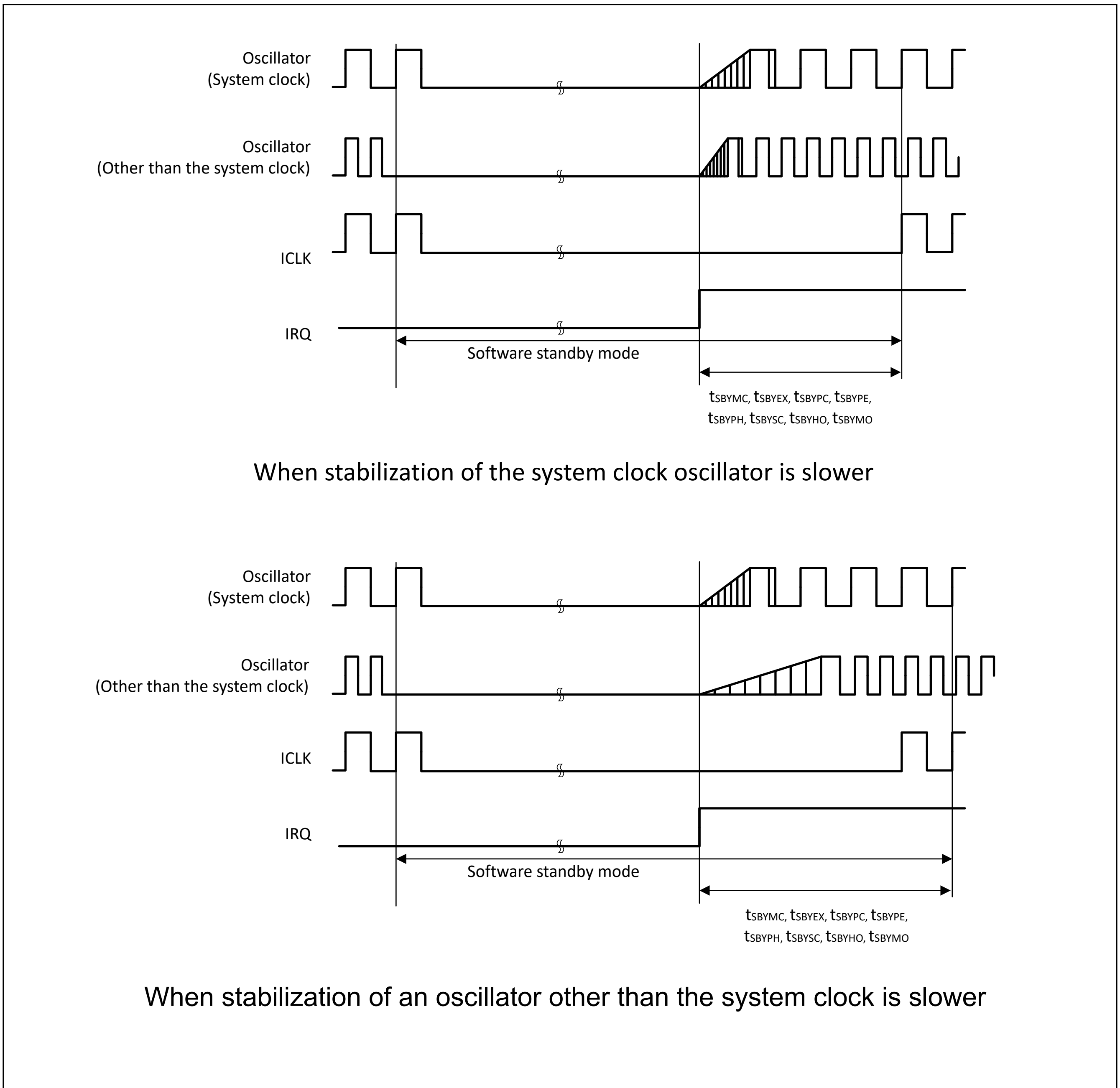


Figure 2.34 Software Standby mode cancellation timing

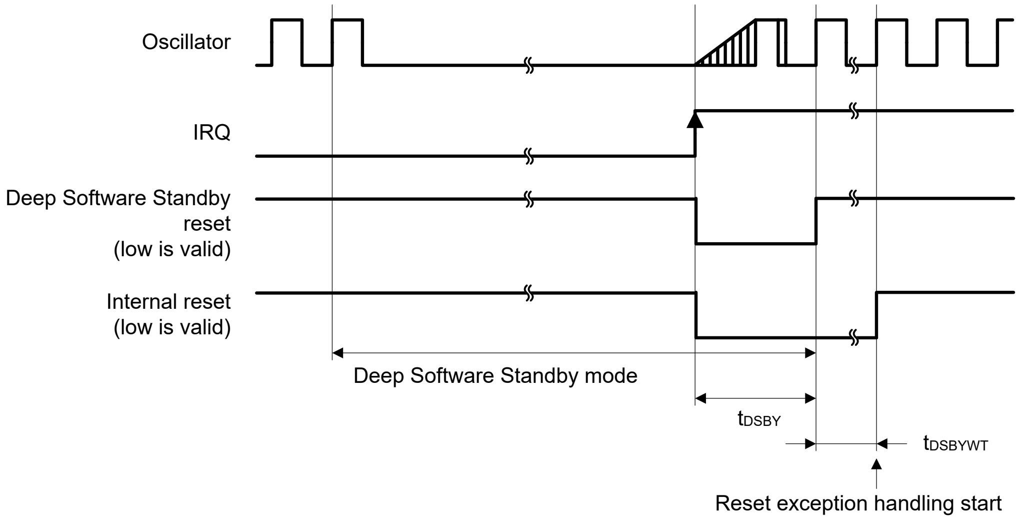


Figure 2.35 Deep Software Standby mode cancellation timing

2.3.5 NMI and IRQ Noise Filter

Table 2.54 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the system clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

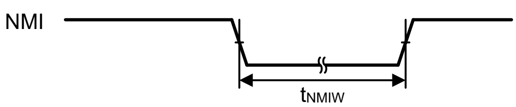


Figure 2.36 NMI interrupt input timing

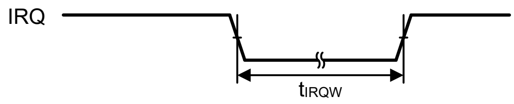


Figure 2.37 IRQ interrupt input timing

2.3.6 Bus Timing

Table 2.55 Bus timing (1 of 3)

Condition 1: When using the CS area controller (CSC).
VCC = VCC_DCDC = VBATT = 1.62 V to 3.6 V, VCC2 = 1.62 V to 3.63 V
BCLK = 8 to 120 MHz, BCLKA = 8 to 120 MHz, EBCLK = 8 to 60 MHz (When VCC = VCC_USB = VBATT = 2.70 to 3.63 V)
BCLK = BCLKA = 8 to 60 MHz, EBCLK = 8 to 30 MHz (When VCC = VCC_USB = VBATT = 1.62 to 3.63 V)
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 125 MHz, BCLKA = SDCLK = 8 to 133 MHz
VCC = VCC_DCDC = VBATT = 3.0 to 3.63 V, VCC2 = 1.62 V to 3.63V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
SDCLK: High-speed high drive output is selected in the port drive capability bit in the PmnPFS register.
Others: High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 66 MHz, BCLKA = SDCLK = 8 to 66 MHz
VCC = VCC_DCDC = VBATT = 3.0 to 3.63 V, VCC2 = 1.62 V to 3.63V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
EBCLK/SDCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Condition	VCC/VCC2	Symbol	Min	Max	Unit	Test conditions
Address delay	Condition1	2.70 V or above	t_{AD}	1.0	12.5	ns	Figure 2.38 to Figure 2.44
		1.62 V or above		1.0	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
Byte control delay	Condition1	2.70 V or above	t_{BCD}	1.0	12.5	ns	
		1.62 V or above		1.0	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
CS delay	Condition1	2.70 V or above	t_{CSD}	1.0	12.5	ns	
		1.62 V or above		1.0	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
ALE delay time	Condition1	2.70 V or above	t_{ALED}	1.0	12.5	ns	
		1.62 V or above		1.0	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
RD delay	Condition1	2.70 V or above	t_{RSD}	1.0	12.5	ns	
		1.62 V or above		1.0	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
Read data setup time	Condition1	2.70 V or above	t_{RDS}	12.5	—	ns	
		1.62 V or above		20.5	—	ns	
	Condition3	3.0 V or above		10.8	—	ns	
Read data hold time	Condition1	2.70 V or above	t_{RDH}	0	—	ns	
		1.62 V or above		0	—	ns	
	Condition3	3.0 V or above		0	—	ns	
WR/WRn delay	Condition1	2.70 V or above	t_{WRD}	1.0	12.5	ns	
		1.62 V or above		1.0	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
Write data delay	Condition1	2.70 V or above	t_{WDD}	—	12.5	ns	
		1.62 V or above		—	12.5	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	

Table 2.55 Bus timing (2 of 3)

Condition 1: When using the CS area controller (CSC).
VCC = VCC_DCDC = VBATT = 1.62 V to 3.6 V, VCC2 = 1.62 V to 3.63 V
BCLK = 8 to 120 MHz, BCLKA = 8 to 120 MHz, EBCLK = 8 to 60 MHz (When VCC = VCC_USB = VBATT = 2.70 to 3.63 V)
BCLK = BCLKA = 8 to 60 MHz, EBCLK = 8 to 30 MHz (When VCC = VCC_USB = VBATT = 1.62 to 3.63 V)
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 125 MHz, BCLKA = SDCLK = 8 to 133 MHz
VCC = VCC_DCDC = VBATT = 3.0 to 3.63 V, VCC2 = 1.62 V to 3.63V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
SDCLK: High-speed high drive output is selected in the port drive capability bit in the PmnPFS register.
Others: High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 66 MHz, BCLKA = SDCLK = 8 to 66 MHz
VCC = VCC_DCDC = VBATT = 3.0 to 3.63 V, VCC2 = 1.62 V to 3.63V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
EBCLK/SDCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Condition	VCC/VCC2	Symbol	Min	Max	Unit	Test conditions
Write data hold time	Condition1	2.70 V or above	t_{WDH}	1.0	—	ns	Figure 2.38 to Figure 2.44
		1.62 V or above		1.0	—	ns	
	Condition3	3.0 V or above		1.0	10.8	ns	
WAIT setup time	Condition1	2.70 V or above	t_{WTS}	12.5	—	ns	
		1.62 V or above		20.5	—	ns	
	Condition3	3.0 V or above		10.8	—	ns	
WAIT hold time	Condition1	2.70 V or above	t_{WTH}	0	—	ns	
		1.62 V or above		0	—	ns	
	Condition3	3.0 V or above		0	—	ns	

Table 2.55 Bus timing (3 of 3)

Condition 1: When using the CS area controller (CSC).
VCC = VCC_DCDC = VBATT = 1.62 V to 3.6 V, VCC2 = 1.62 V to 3.63 V
BCLK = 8 to 120 MHz, BCLKA = 8 to 120 MHz, EBCLK = 8 to 60 MHz (When VCC = VCC_USB = VBATT = 2.70 to 3.63 V)
BCLK = BCLKA = 8 to 60 MHz, EBCLK = 8 to 30 MHz (When VCC = VCC_USB = VBATT = 1.62 to 3.63 V)
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 125 MHz, BCLKA = SDCLK = 8 to 133 MHz
VCC = VCC_DCDC = VBATT = 3.0 to 3.63 V, VCC2 = 1.62 V to 3.63V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
SDCLK: High-speed high drive output is selected in the port drive capability bit in the PmnPFS register.
Others: High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 66 MHz, BCLKA = SDCLK = 8 to 66 MHz
VCC = VCC_DCDC = VBATT = 3.0 to 3.63 V, VCC2 = 1.62 V to 3.63V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
EBCLK/SDCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Condition	VCC/VCC2	Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	Condition 2	3.0 V or above	t_{AD2}	0.8	6.0	ns	Figure 2.45 to Figure 2.51
	Condition 3	3.0 V or above		0.8	10		
CS delay 2 (SDRAM)	Condition 2	3.0 V or above	t_{CSD2}	0.8	6.0	ns	
	Condition 3	3.0 V or above		0.8	10		
DQM delay (SDRAM)	Condition 2	3.0 V or above	t_{DQMD}	0.8	6.0	ns	
	Condition 3	3.0 V or above		0.8	10		
CKE delay (SDRAM)	Condition 2	3.0 V or above	t_{CKED}	0.8	6.0	ns	
	Condition 3	3.0 V or above		0.8	10		
Read data setup time 2 (SDRAM)	Condition 2	3.0 V or above	t_{RDS2}	2.1	—	ns	
	Condition 3	3.0 V or above		6.1	—		
Read data hold time 2 (SDRAM)	Condition 2	3.0 V or above	t_{RDH2}	1.5	—	ns	
	Condition 3	3.0 V or above		1.5	—		
Write data delay 2 (SDRAM)	Condition 2	3.0 V or above	t_{WDD2}	—	6.0	ns	
	Condition 3	3.0 V or above		—	10		
Write data hold time 2 (SDRAM)	Condition 2	3.0 V or above	t_{WDH2}	0.8	—	ns	
	Condition 3	3.0 V or above		0.8	—		
WE delay (SDRAM)	Condition 2	3.0 V or above	t_{WED}	0.8	6.0	ns	
	Condition 3	3.0 V or above		0.8	10		
RAS delay (SDRAM)	Condition 2	3.0 V or above	t_{RASD}	0.8	6.0	ns	
	Condition 3	3.0 V or above		0.8	10		
CAS delay (SDRAM)	Condition 2	3.0 V or above	t_{CASD}	0.8	6.0	ns	
	Condition 3	3.0 V or above		0.8	10		

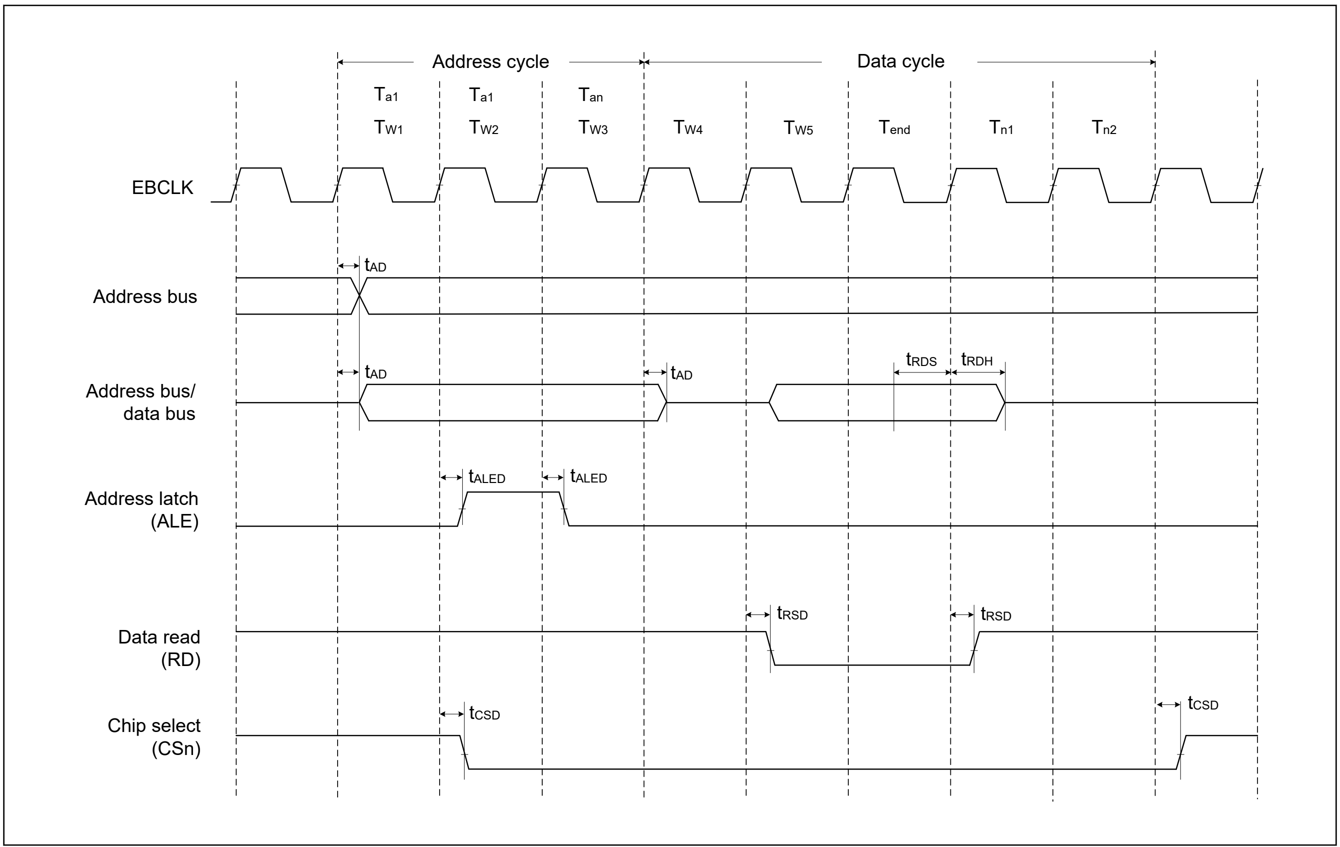


Figure 2.38 Address/data multiplexed bus read access timing

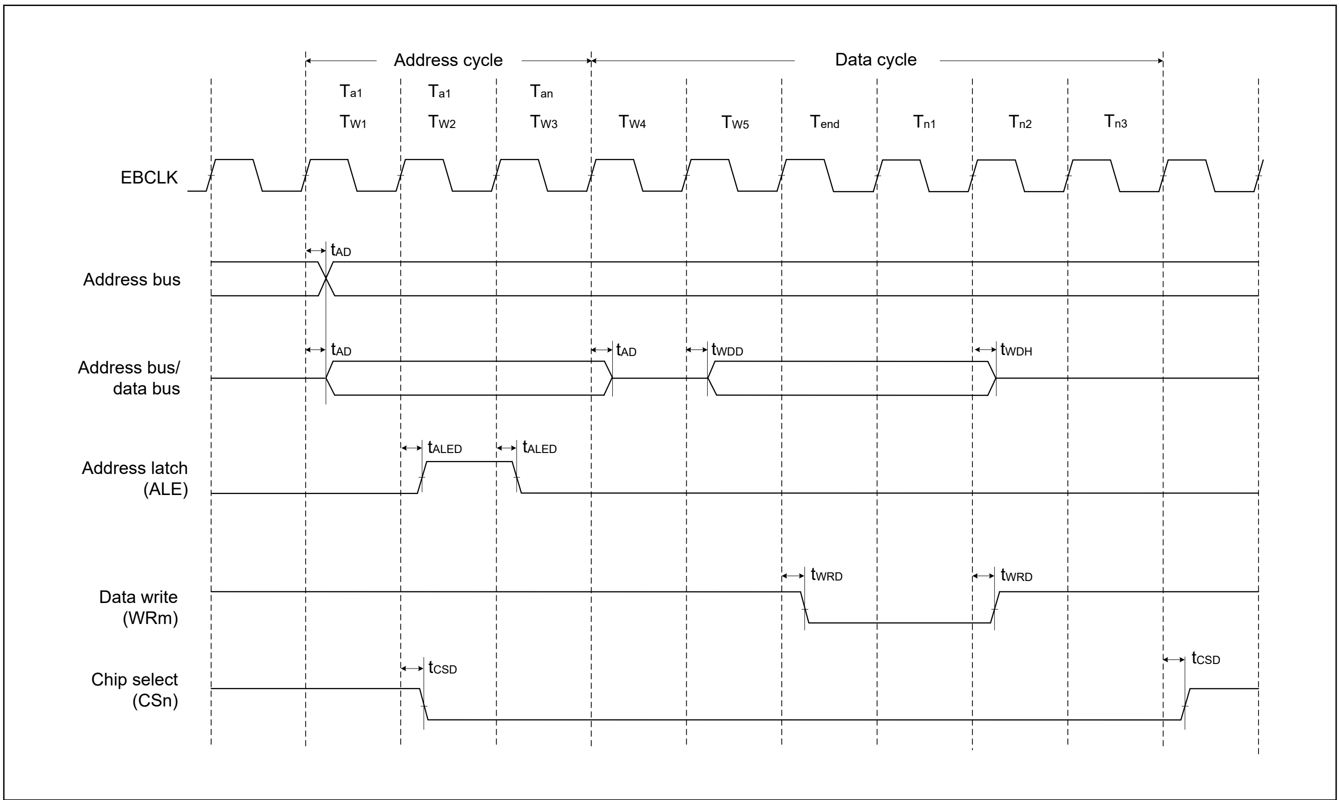


Figure 2.39 Address/data multiplexed bus write access timing

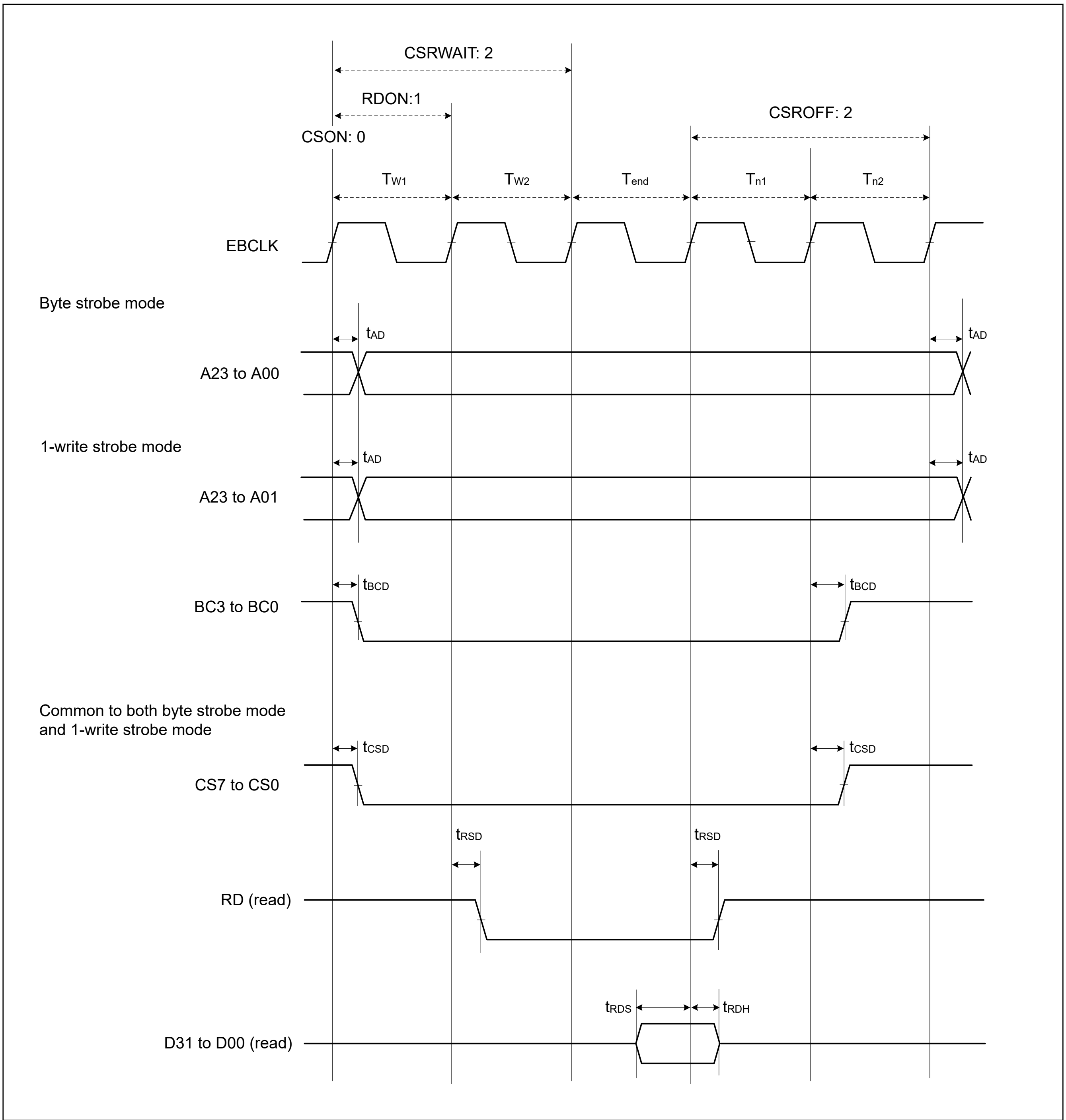
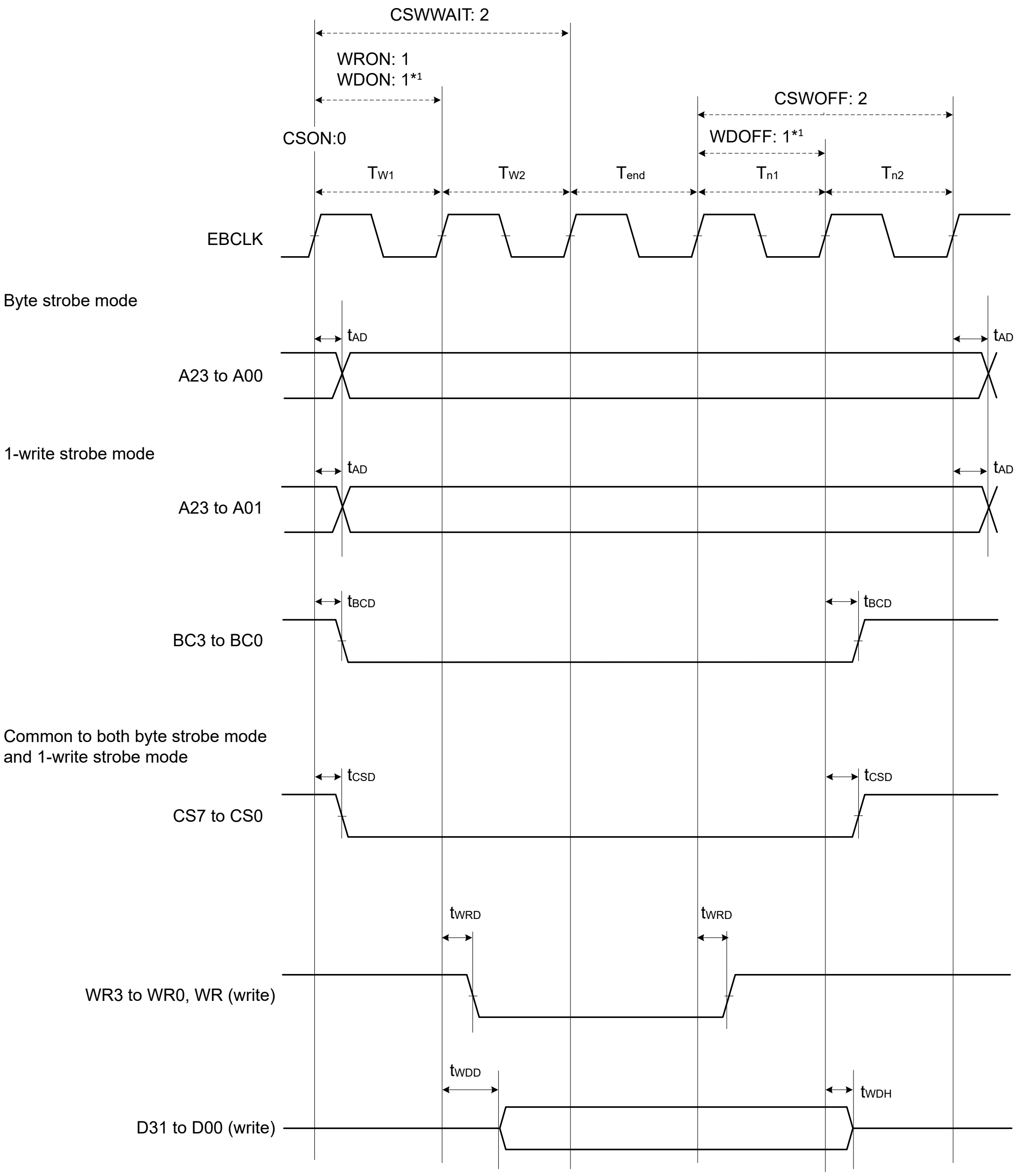


Figure 2.40 External bus timing for normal read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.41 External bus timing for normal write cycle with bus clock synchronized

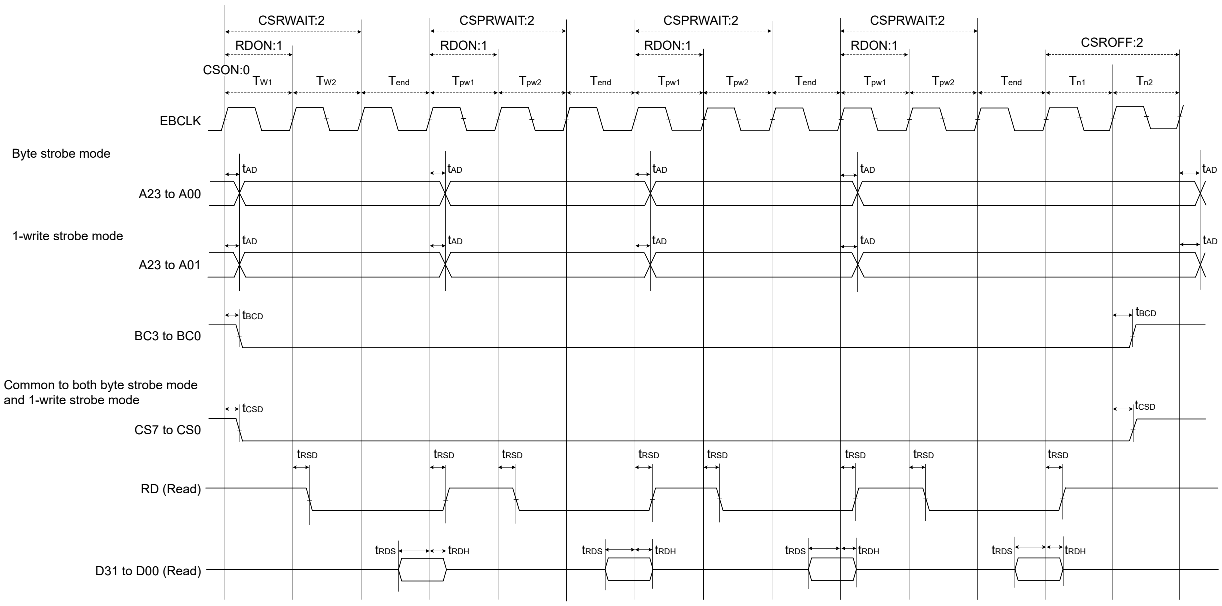
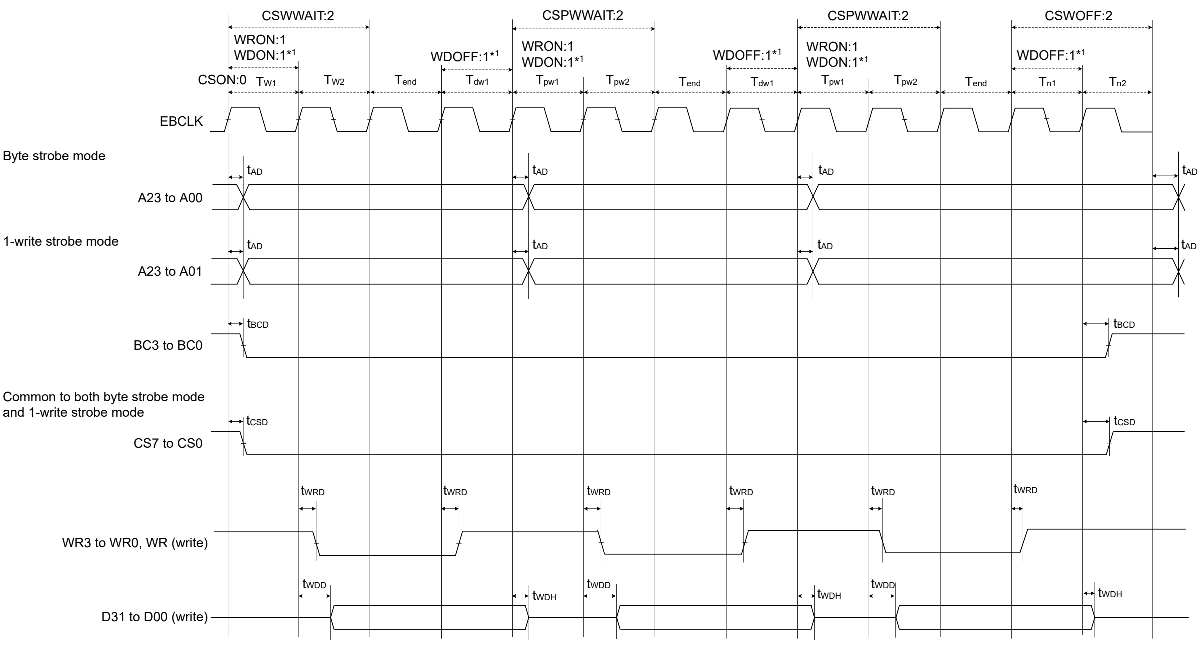


Figure 2.42 External bus timing for page read cycle with bus clock synchronized



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 2.43 External bus timing for page write cycle with bus clock synchronized

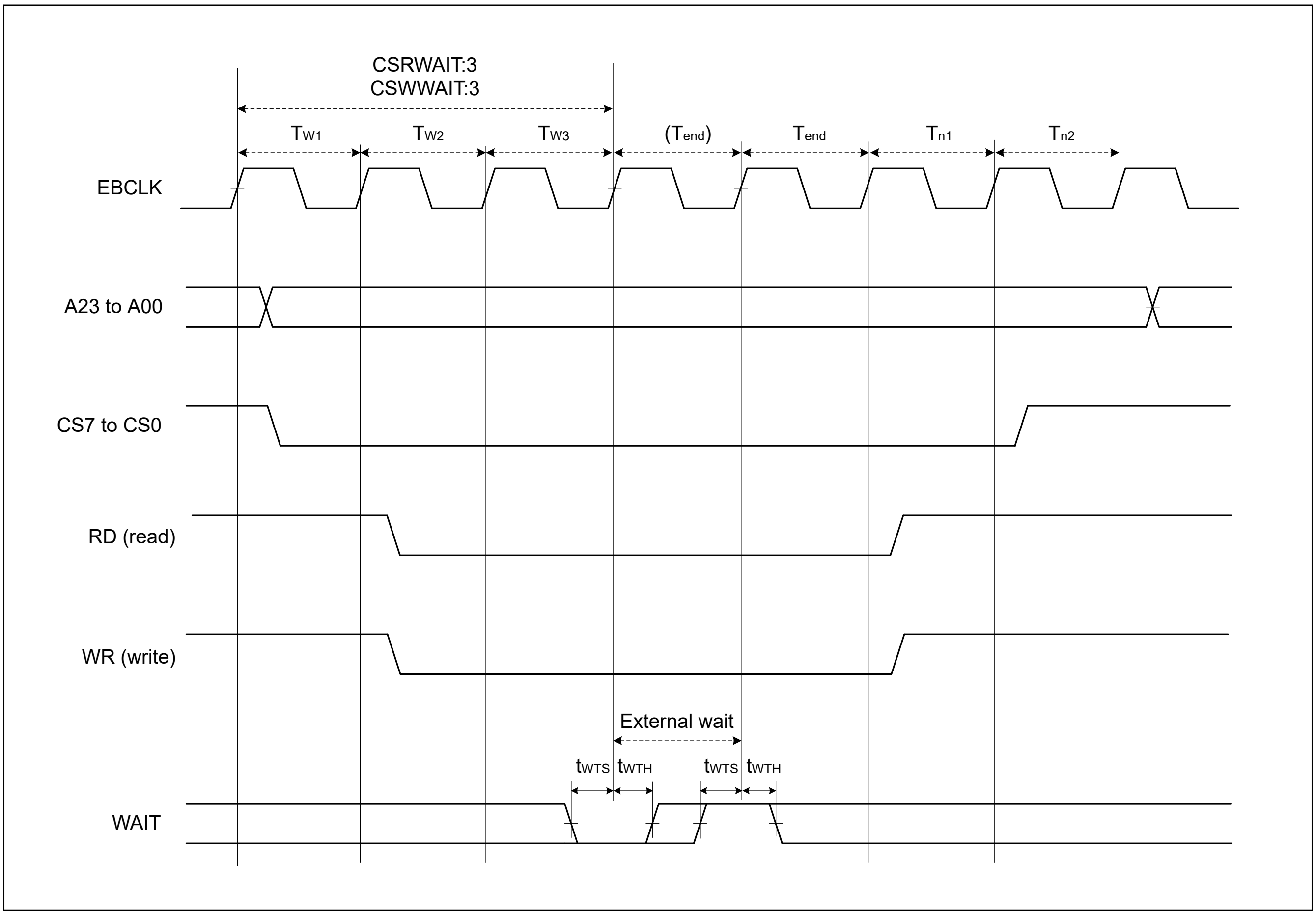


Figure 2.44 External bus timing for external wait control

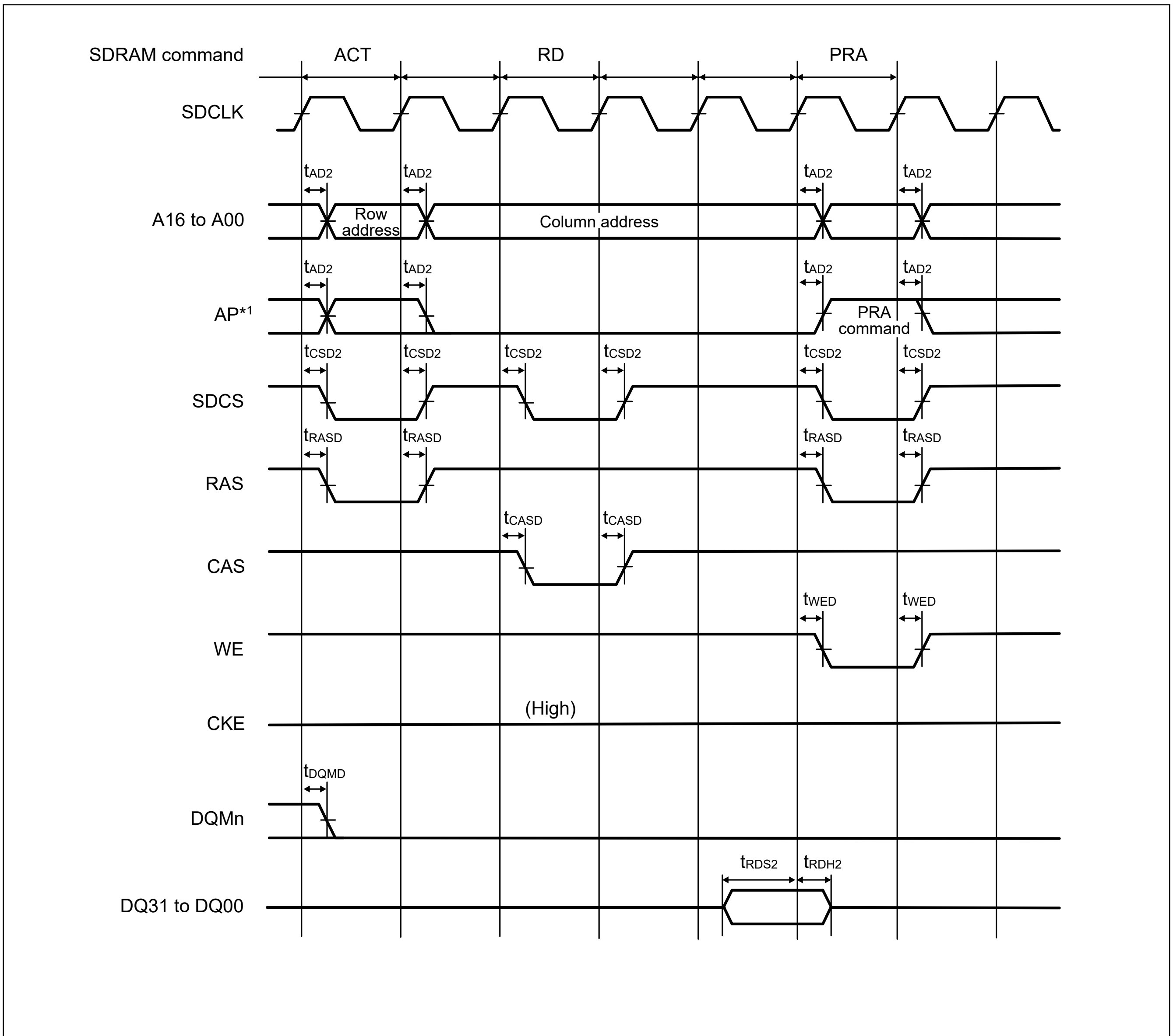


Figure 2.45 SDRAM single read timing

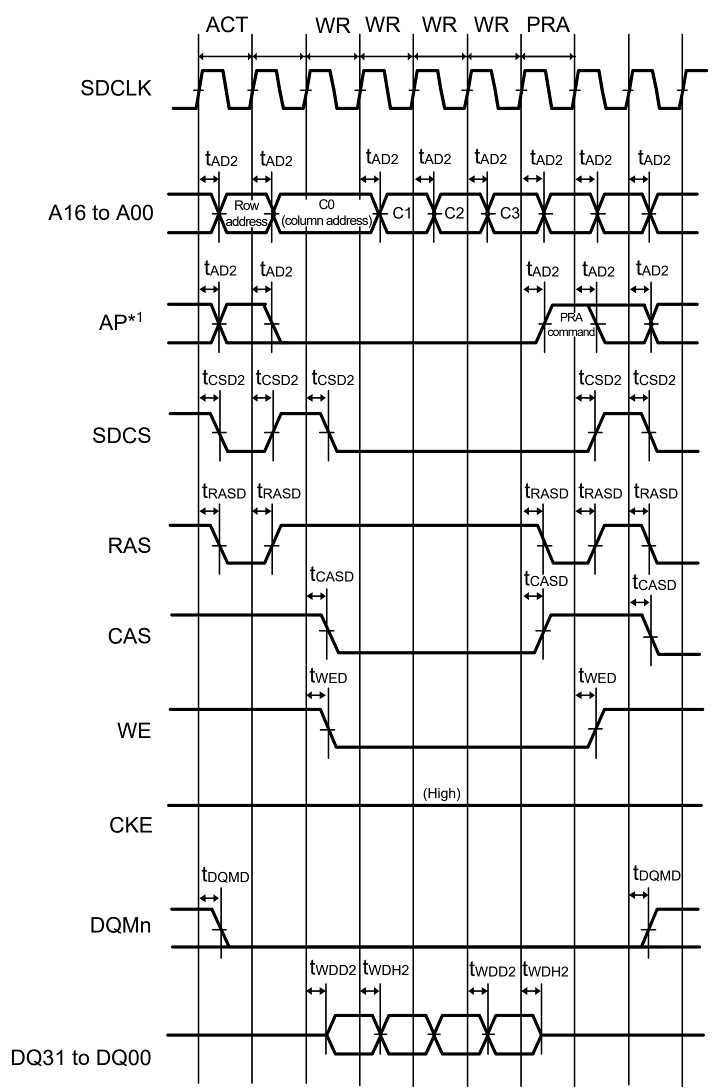


Figure 2.46 SDRAM single write timing

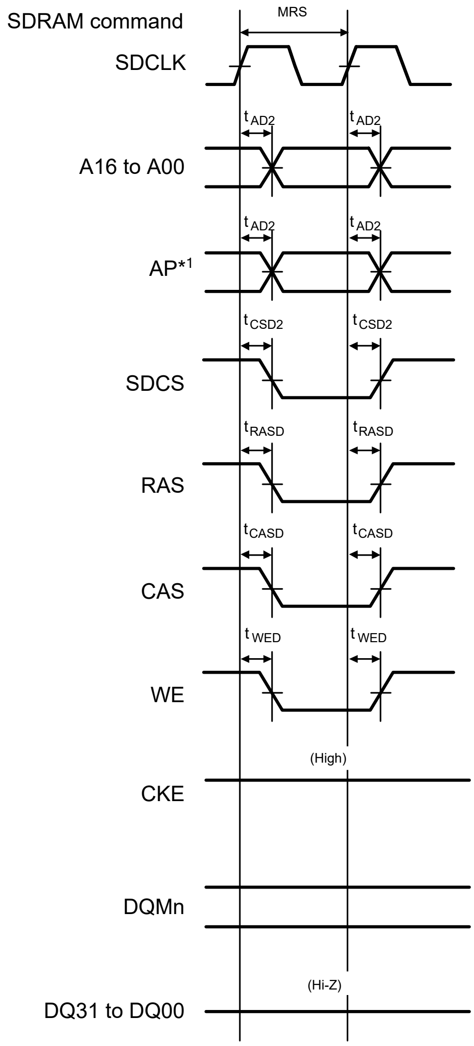


Figure 2.47 SDRAM multiple read timing

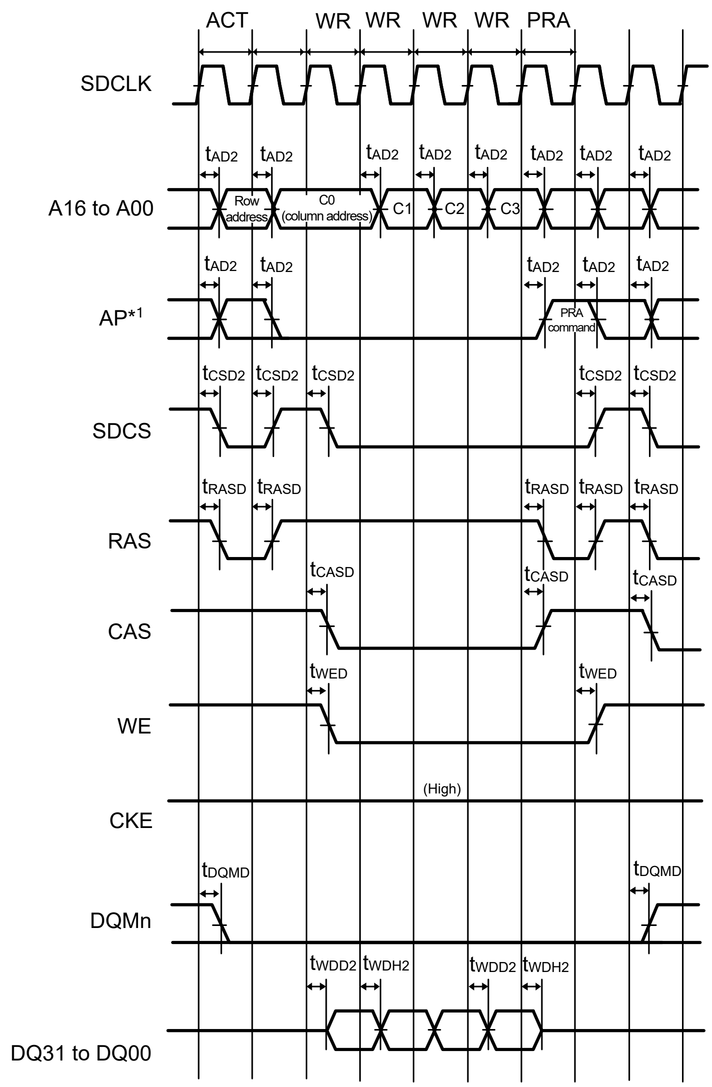


Figure 2.48 SDRAM multiple write timing

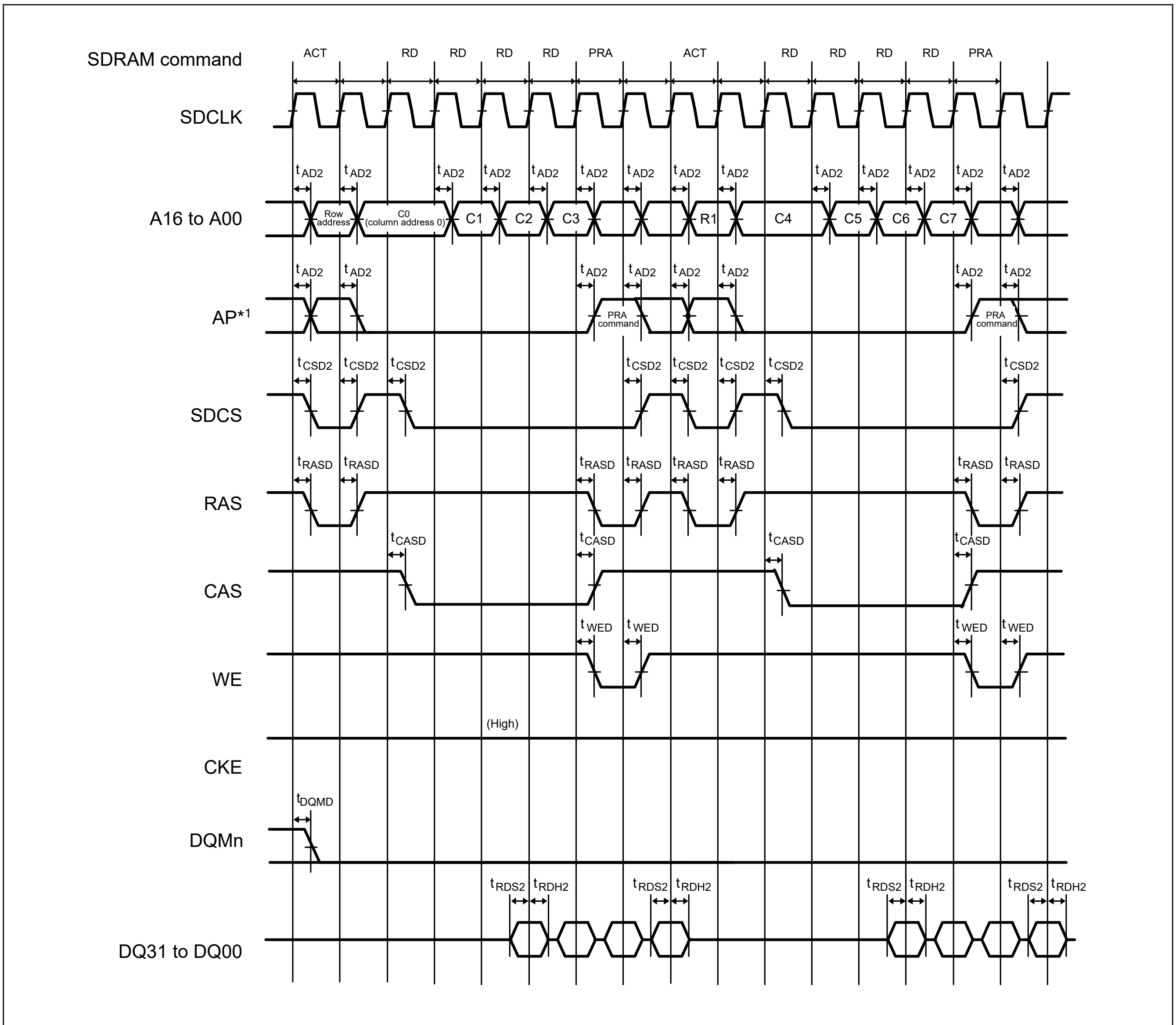


Figure 2.49 SDRAM multiple read line stride timing

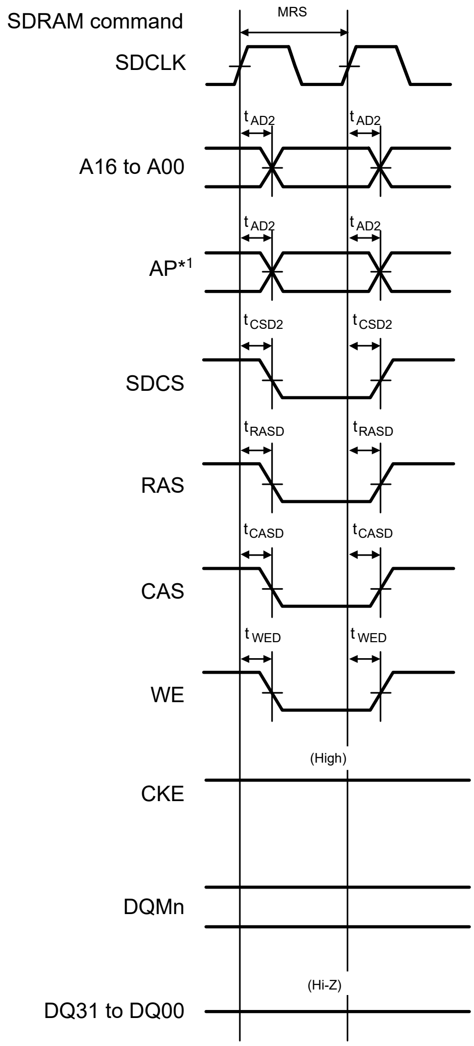


Figure 2.50 SDRAM mode register set timing

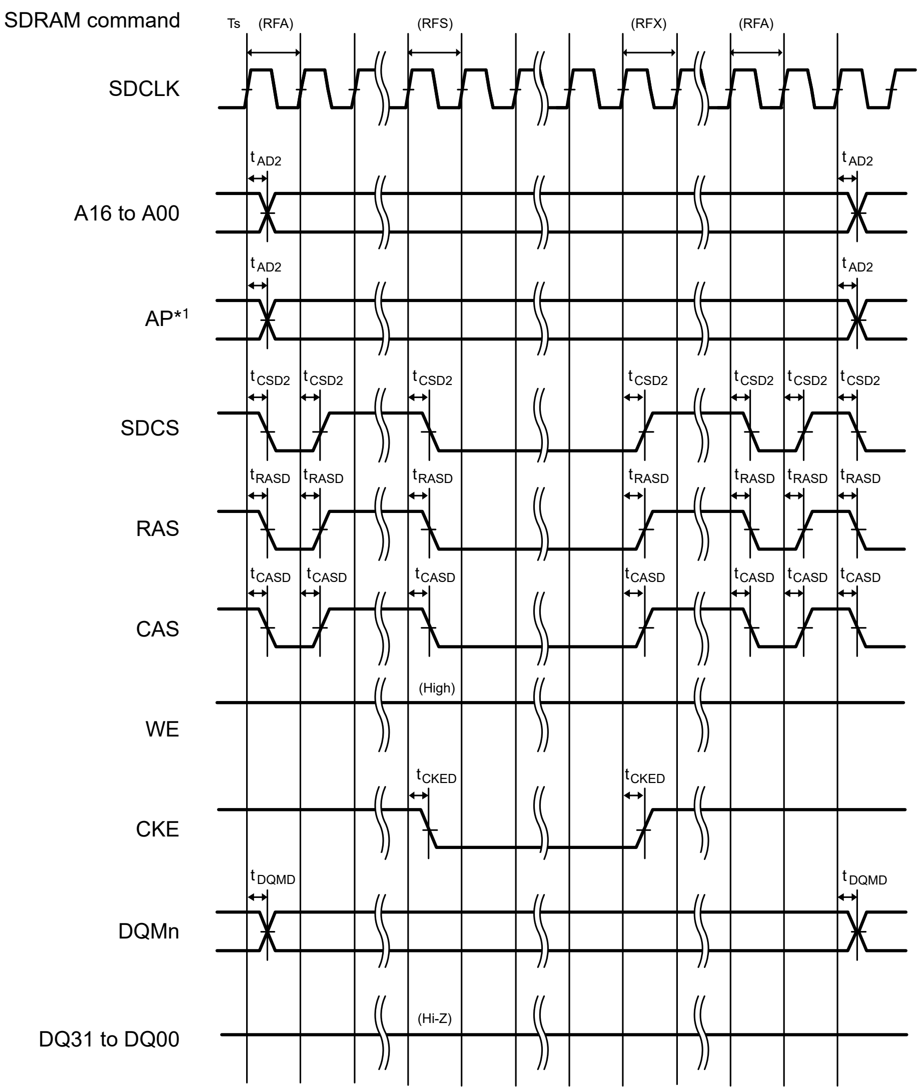


Figure 2.51 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT, AGT, ULPT and ADC Trigger Timing

Table 2.56 I/O ports, POEG, GPT, AGT, ULPT and ADC trigger timing (1 of 4)

GPT32 Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	5.5	—	t_{Icyc}	Figure 2.52
	EXCIN input frequency	t_{EXCIN}	—	36	kHz	
	RTCICn (n = 0 to 2) input pulse width	t_{RTCICW}	13.89	—	μs	Figure 2.53

Table 2.56 I/O ports, POEG, GPT, AGT, ULPT and ADC trigger timing (2 of 4)

GPT32 Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.54
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	2 PCLKB + 0.34	µs	Figure 2.55 When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Detection of the output stopping signal from GPT (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	0.5	µs	Figure 2.56
		Edge detection signal from a comparator	t_{POEGDC}	—	3 PCLKB + 0.5	µs	Figure 2.57 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS [1:0] = 00b) and excludes the time for detection by ACMPHS.
		Register setting	t_{POEGDS}	—	0.3	µs	Figure 2.58 Time for access to the register is not included.
		Oscillation stop detection	$t_{POEGDOS}$	—	1.3	µs	Figure 2.59
		Level detection signal from a comparator	$t_{POEGDDC}$	—	0.5	µs	Figure 2.60 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS [1:0] = 00b) and excludes the time for detection by ACMPHS.
		Overcurrent Detection Window Notification detection from DSMIF	$t_{POEGDERR}$	—	0.5	µs	Figure 2.61 The time is that when the noise filter for ACMPHS is not in use (CMPCTL.CDFS [1:0] = 00b) and excludes the time for detection by ACMPHS.

Table 2.56 I/O ports, POEG, GPT, AGT, ULPT and ADC trigger timing (3 of 4)

GPT32 Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit	Test conditions
GPT	Input capture pulse width (Cycle)		Single edge	t_{GTICW} *1	1.5	—	t_{PDcyc}	Figure 2.62
			Dual edge		2.5	—		
	Input capture pulse width (Times)		2.70 V or above	t_{GTICW} *1	8.3	—	ns	
			1.62 V or above		10.0	—		
	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive output	2.70 V or above	t_{GTISK}	—	4	ns	Figure 2.63
			1.62 V or above		—	6		
		High drive output	2.70 V or above			3.5		
			1.62 V or above			4.5		
	GTIOCxY output skew (x = 4 to 13, Y = A or B)	Middle drive output	2.70 V or above		—	4		
			1.62 V or above		—	6		
		High drive output	2.70 V or above		—	3.5		
			1.62 V or above		—	4.5		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive output	2.70 V or above		—	6		
			1.62 V or above		—	7		
		High drive output	2.70 V or above		—	3.5		
			1.62 V or above		—	5		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO	Middle drive output	2.70 V or above	t_{GTOSK}	—	5	ns	Figure 2.64
			1.62 V or above		—	6		
GPT (PWM Delay Generation Circuit)	GTIOCxY output skew (x = 0 to 3, Y = A or B)	Middle drive output	2.70 V or above	t_{HRSK}	—	4	ns	Figure 2.65
			1.62 V or above		—	6		
		High drive output	2.70 V or above		—	3.5		
			1.62 V or above		—	5		

Table 2.56 I/O ports, POEG, GPT, AGT, ULPT and ADC trigger timing (4 of 4)

GPT32 Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If GPT pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
AGT Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
AGT	AGTIO, AGTEE input cycle	2.70 V or above	t_{ACYC}*2	100	—	ns	Figure 2.66
		1.62 V or above		100	—		
	AGTIO, AGTEE input high width, low width	2.70 V or above	t_{ACKWH}, t_{ACKWL}	40	—	ns	
		1.62 V or above		40	—		
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.70 V or above	t_{ACYC2}	62.5	—	ns	
		1.62 V or above		62.5	—		
ULPT	ULPTEE, ULPTEVI input cycle	2.70 V or above	t_{ULCYC}*3	32	—	μs	Figure 2.67
		1.62 V or above		32	—		
	ULPTEE, ULPTVI input high width, low width	2.70 V or above	t_{ULCKWH}, t_{ULCKWL}	12	—	μs	
		1.62 V or above		12	—		
	ULPTO, ULPTOA, ULPTOB output cycle	2.70 V or above	t_{ULCYC2}	64	—	μs	
		1.62 V or above		64	—		
ADC	ADC trigger input pulse width	2.70 V or above	t_{TRGW}	1.5	—	t_{ADcyc}	Figure 2.68
		1.62 V or above		3.0	—		

Note: t_{Icyc}: ICLK cycle, t_{Pcyc}: PCLKB cycle, t_{PDcyc}: GTCLK cycle, $t_{ULPTLCLK}$: ULPTLCLK cycle, t_{ADcyc}: ADCLK cycle.
Note 1. For Cycle and Time, the longer time characteristics are applied.
Note 2. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.
Note 3. Constraints on input cycle:
ULPTEVI: $t_{Pcyc} \times 2 < t_{ULCYC}$ should be satisfied.
ULPTEE: $t_{ULPTLCLK} \times 2 < t_{ULCYC}$ should be satisfied.

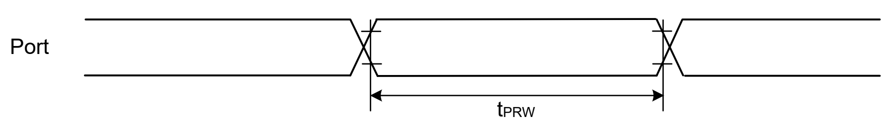


Figure 2.52 I/O ports input timing

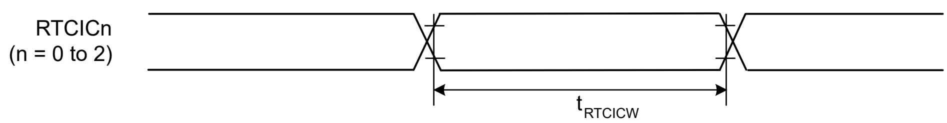


Figure 2.53 RTCICn input timing

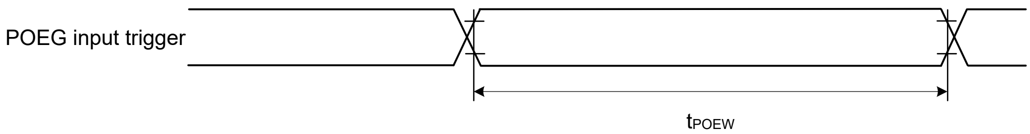


Figure 2.54 POEG input trigger timing

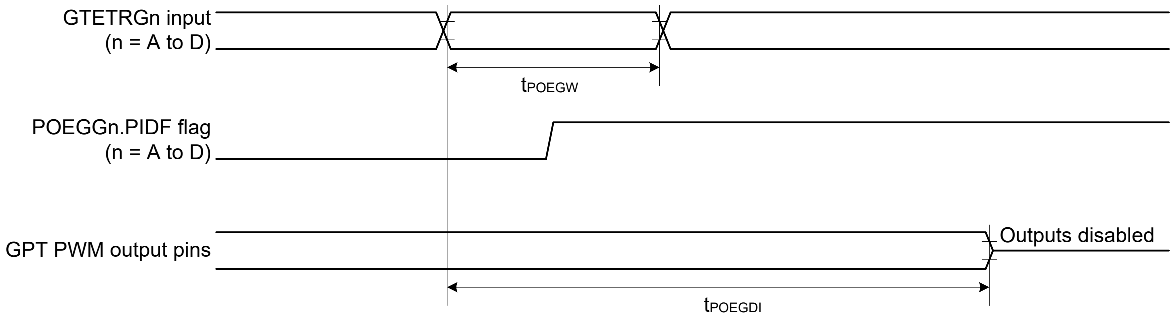
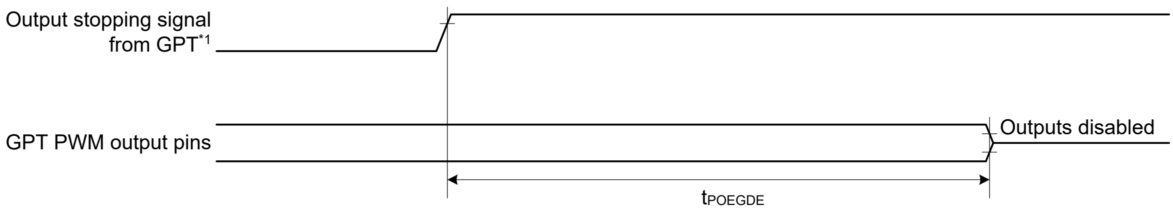


Figure 2.55 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRGn pin



Note 1. GPT32n.GTST.DTEF (dead time error flag), GPT32n.GTST.OABLF (simultaneous low output flag), or GPT32n.GTST.OABHF (simultaneous high output flag)

Figure 2.56 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPT

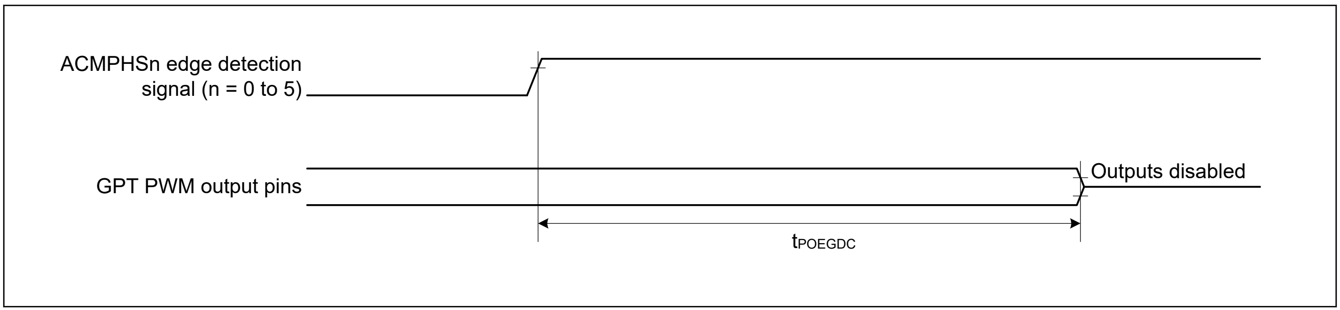


Figure 2.57 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

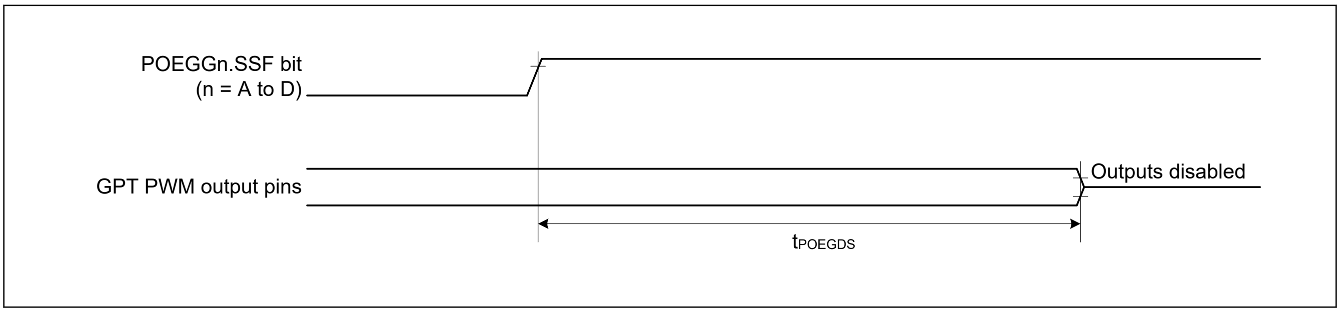


Figure 2.58 Output Disable Time for POEG in Response to the Register Setting

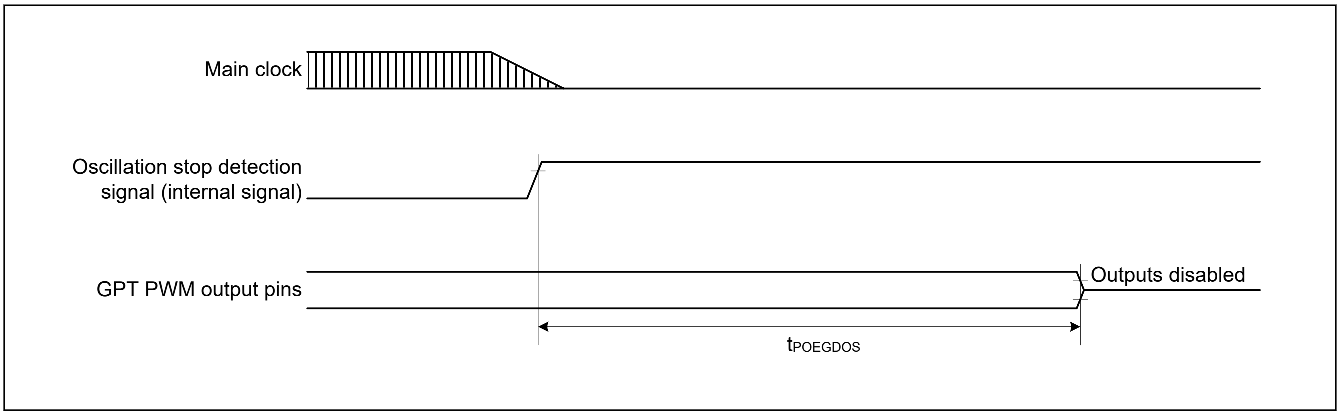


Figure 2.59 Output Disable Time of POEG in Response to the Oscillation Stop Detection

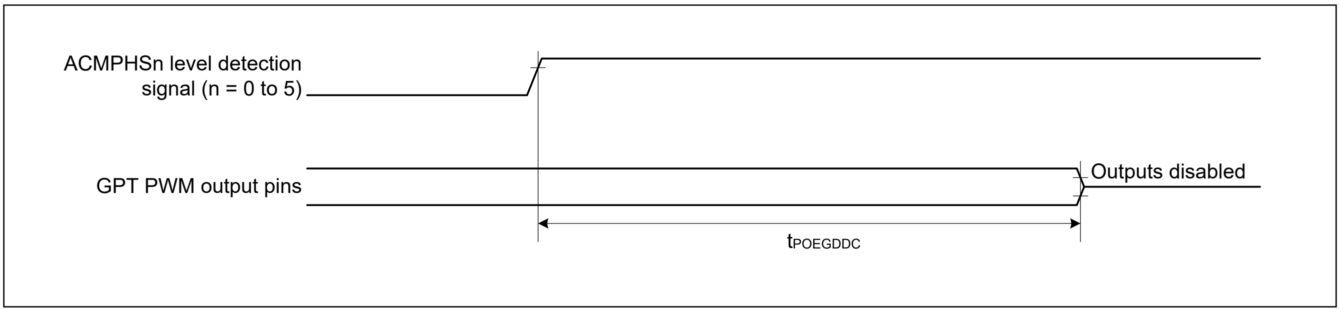


Figure 2.60 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator

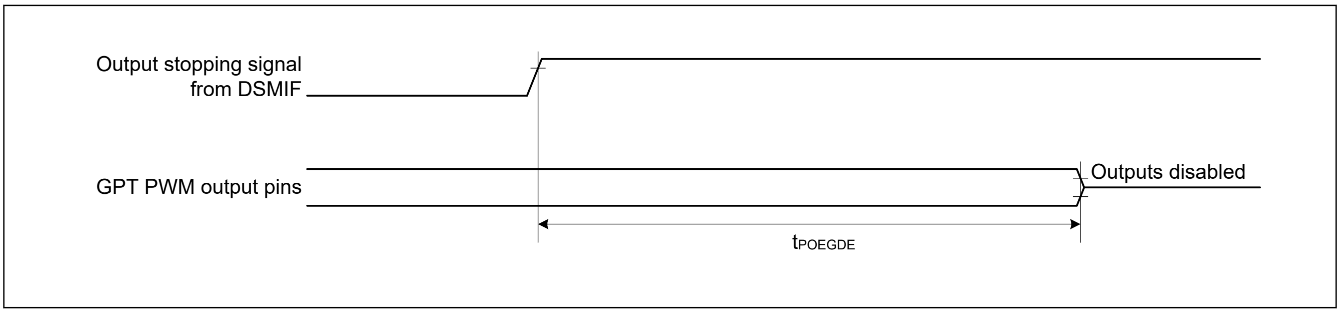


Figure 2.61 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from DSMIF

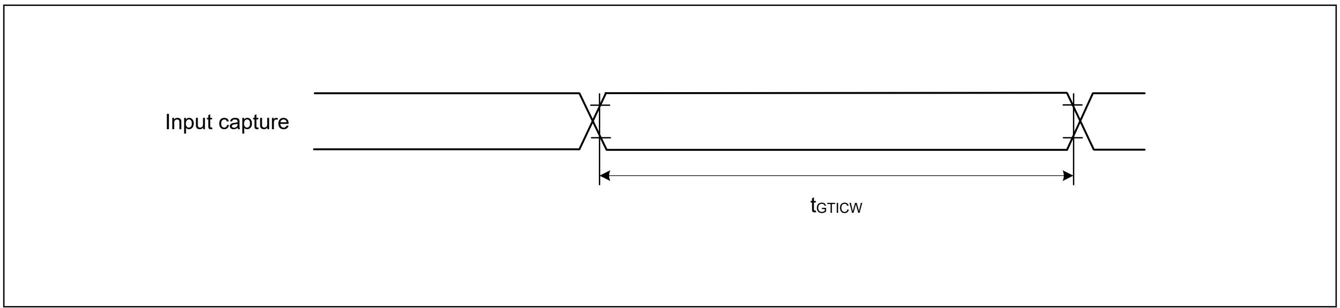


Figure 2.62 GPT input capture timing

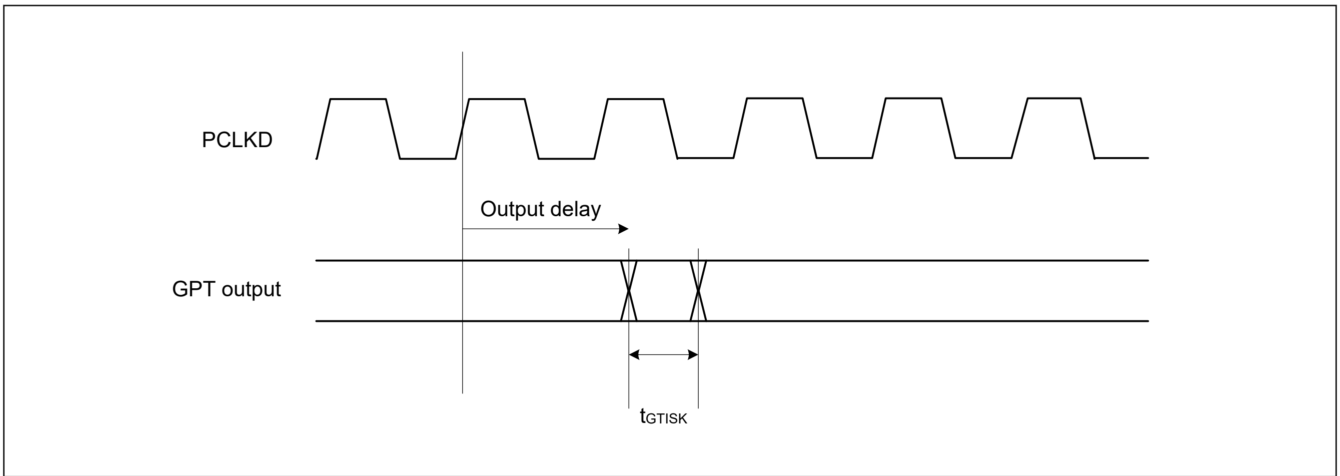


Figure 2.63 GPT output delay skew

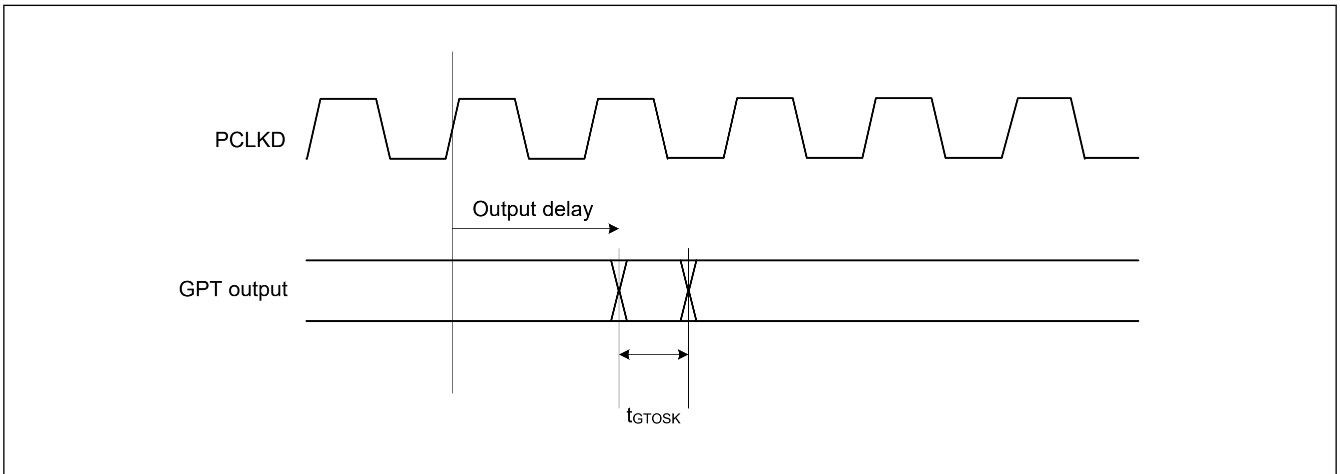


Figure 2.64 GPT output delay skew for OPS

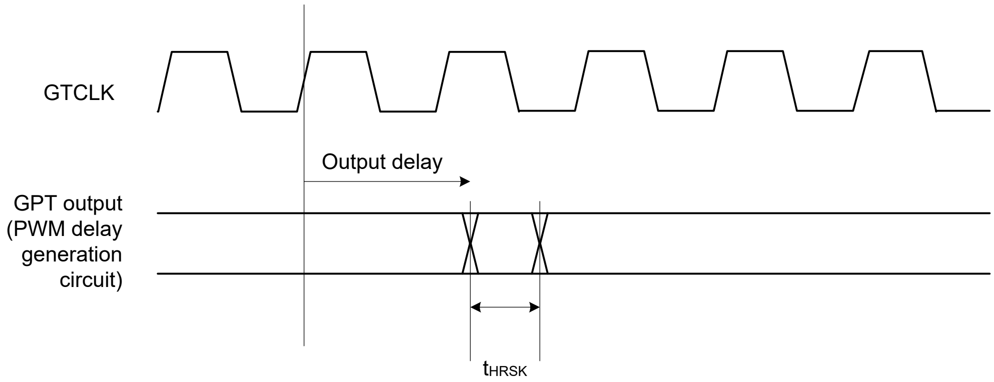


Figure 2.65 GPT (PDG) output delay skew

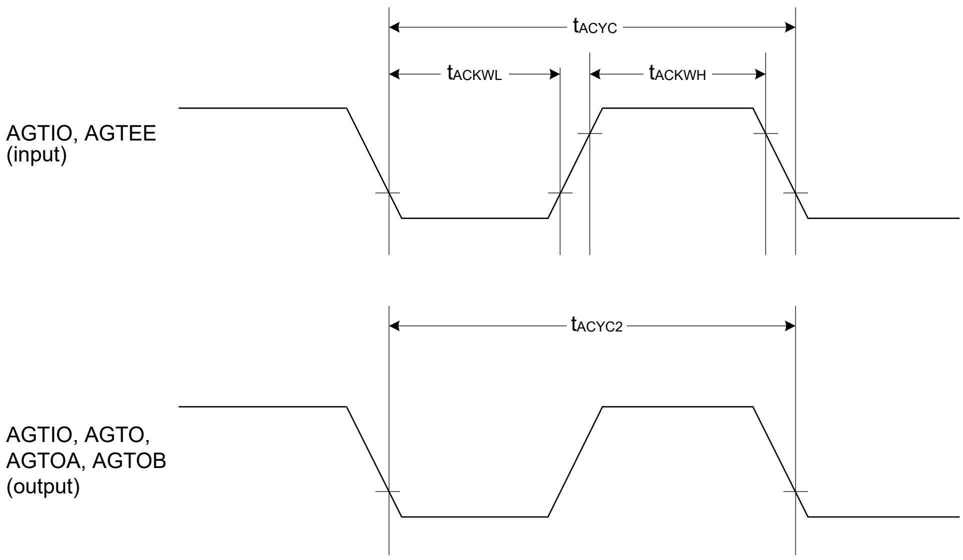


Figure 2.66 AGT input/output timing

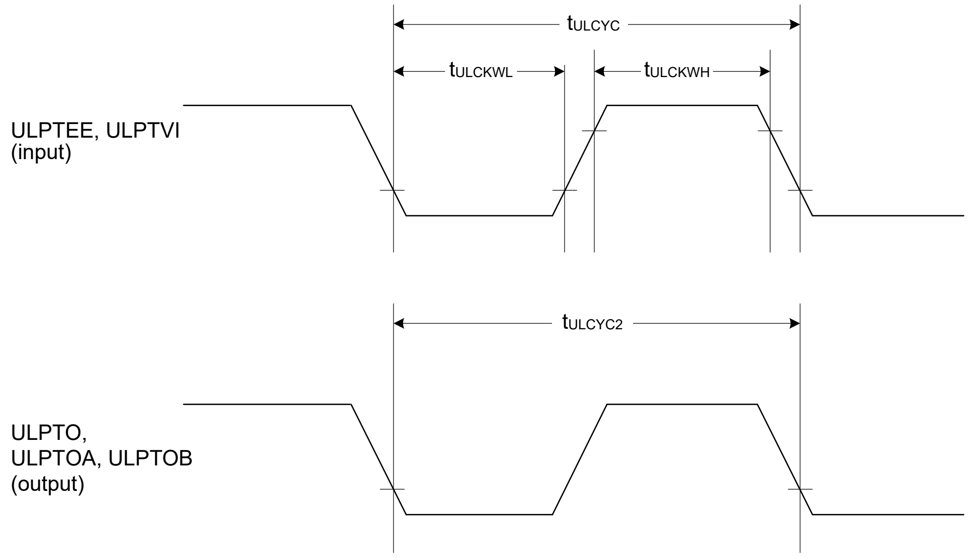


Figure 2.67 ULPT input/output timing

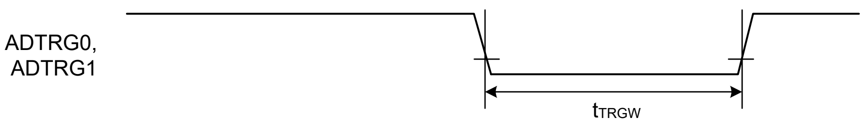


Figure 2.68 ADC trigger input timing

2.3.8 CAC Timing

Table 2.57 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \leq t_{cac}$ *1	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	—	—	ns	—
		$t_{PBcyc} > t_{cac}$ *1		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	—	—	ns	

Note: t_{PBcyc}: PCLKB cycle.
Note 1. t_{cac}: CAC count clock source cycle.

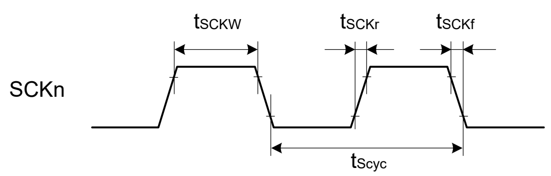
2.3.9 SCI Timing

Table 2.58 SCI timing (Asynchronous mode)

Conditions:
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter	VCC/VCC2	Symbol	Min	Max	Unit	Note
Input clock cycle	1.62 V or above	t_{Scyc}	4.0	—	t_{Tcyc}	Figure 2.69
Input clock pulse width	1.62 V or above	t_{SCKW}	0.4	0.6	t_{Scyc}	
Input clock rise time	1.62 V or above	t_{SCKr}	—	0.1[*1]	t_{Scyc}	
Input clock fall time	1.62 V or above	t_{SCKf}	—	0.1[*1]	t_{Scyc}	
Output clock cycle	1.62 V or above	t_{Scyc}	6.0	—	t_{Tcyc}	
Output clock pulse width	1.62 V or above	t_{SCKW}	0.4	0.6	t_{Scyc}	
Output clock rise time	2.70 V or above	t_{SCKr}	—	3.3	ns	
	1.62 V or above		—	6.6		
Output clock fall time	2.70 V or above	t_{SCKf}	—	3.3	ns	
	1.62 V or above		—	6.6		

Note: tT_{cyc}: TCLK cycle.
Note 1. 1 μs at the longest



Note: n = 0 to 4, 9

Figure 2.69 SCK clock input/output timing

Table 2.59 SCI timing (Simple SPI) (1 of 3)

Condition 1: VCC/VCC2 = 2.70 V or above
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
Condition 2: VCC/VCC2 = 1.62 V or above
Following pins have high-speed high-drive output selected in the Port Drive Capability bit in the PmnPFS register: SCK1_A, SCK1_C, SCK3_A, SCK4_A, SCK4_B, SCK4_C and SCK6_B
Other pins have high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC=VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master	—	2.70 V or above	t_{SPcyc}	2 (TCLK ≤ 120MHz) 4 (TCLK > 120MHz)	65536	t_{Tcyc}	Figure 2.70
			1.62 V or above		2 (TCLK ≤ 60MHz) 4 (TCLK ≤ 120MHz) 8 (TCLK > 120MHz)	65536		
SCK clock cycle input	Slave	—	2.70 V or above		2	—		
			1.62 V or above		2 (TCLK ≤ 100MHz) 4 (TCLK > 100MHz)	—		
SCK clock high pulse width	Master	—	1.62 V or above	t_{SPCKWH}	0.4	—	t_{SPcyc}	
	Slave	—						
SCK clock low pulse width	Master	—	1.62 V or above	t_{SPCKWL}	0.4	—	t_{SPcyc}	
	Slave	—						
SCK clock rise and fall time	Output	—	2.70 V or above	t_{SPCKr}, t_{SPCKf}	—	3.3	ns	
			1.62 V or above		—	6.6		
	Input	—	2.70 V or above		—	0.1*3	t_{SPcyc}	
			1.62 V or above		—	0.1*3		

Table 2.59 SCI timing (Simple SPI) (2 of 3)

Condition 1: VCC/VCC2 = 2.70 V or above
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
Condition 2: VCC/VCC2 = 1.62 V or above
Following pins have high-speed high-drive output selected in the Port Drive Capability bit in the PmnPFS register: SCK1_A, SCK1_C, SCK3_A, SCK4_A, SCK4_B, SCK4_C and SCK6_B
Other pins have high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC=VCC2.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Data input setup time	Master	High Speed*1	2.70 V or above	t_{SU}	-1.5	—	ns	Figure 2.71, Figure 2.72
			1.62 V or above		-1.5	—		
		Default*2	2.70 V or above		2.0	—		
			1.62 V or above		2.0	—		
	Slave	Default*2	2.70 V or above		2.5	—		
			1.62 V or above		4.5	—		
Data input hold time	Master	High Speed*1	2.70 V or above	t_H	7.5	—	ns	
			1.62 V or above		9.5	—		
		Default*2	2.70 V or above		7.5	—		
			1.62 V or above		9.5	—		
	Slave	Default*2	2.70 V or above		2.5	—		
			1.62 V or above		4.5	—		
Data output delay	Master	High Speed*1	2.70 V or above	t_{OD}	—	3.0	ns	
			1.62 V or above		—	4.5		
		Default*2	2.70 V or above		—	3.5		
			1.62V or above		—	5.5		
	Slave	High Speed*1	2.70 V or above		—	12.5		
			1.62 V or above		—	20.5		
		Default*2	2.70 V or above		—	18.5		
			1.62 V or above		—	26.5		
Data output hold time	Master	High Speed*1	2.70 V or above	t_{OH}	−3.0	—	ns	
			1.62 V or above		−4.5	—		
		Default*2	2.70 V or above		−3.5	—		
			1.62 V or above		−5.5	—		
	Slave	Default*2	2.70 V or above		0.0	—		
			1.62 V or above		0.0	—		
Data rise and fall time	Output	—	2.70 V or above	t_{Dr}, t_{Df}	—	3.3	ns	
			1.62 V or above		—	6.6		
	Input	—	2.70 V or above		—	1		
			1.62 V or above		—	1		
SS input setup time		—	1.62 V or above	t_{LEAD}	1.0	—	t_{SPcyc}	Figure 2.73, Figure 2.74
SS input hold time		—	1.62 V or above	t_{LAG}	1.0	—	t_{SPcyc}	
SS input rise and fall time		—	1.62 V or above	t_{SSLr}, t_{SSLf}	—	1	μs	—

Table 2.59 SCI timing (Simple SPI) (3 of 3)

Condition 1: VCC/VCC2 = 2.70 V or above
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
Condition 2: VCC/VCC2 = 1.62 V or above
Following pins have high-speed high-drive output selected in the Port Drive Capability bit in the PmnPFS register: SCK1_A, SCK1_C, SCK3_A, SCK4_A, SCK4_B, SCK4_C and SCK6_B
Other pins have high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC=VCC2.

Parameter	High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Slave access time	—	2.70 V or above	t_{SA}	—	3 × t_{Tcyc} + 25	ns	Figure 2.73, Figure 2.74
		1.62 V or above		—	3 × t_{Tcyc} + 32		
Slave output release time	—	2.70 V or above	t_{REL}	—	3 × t_{Tcyc} + 25	ns	
		1.62 V or above		—	3 × t_{Tcyc} + 32		

Note: t_{Tcyc}: TCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0, SCI1, SCI2, SCI3 and SCI9 are instance _A, SCI4 and SCI5 are instance _B, SCI6, SCI7 and SCI8 are instance _C.
Note 2. All pins of group membership can be used.
Note 3. 1 µs at the longest

Table 2.60 SCI timing (Clock synchronous mode) (1 of 2)

Condition 1: VCC/VCC2 = 2.70 V or above
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
Condition 2: VCC/VCC2 = 1.62 V or above
Following pins have high-speed high-drive output selected in the Port Drive Capability bit in the PmnPFS register: SCK1_A, SCK1_C, SCK3_A, SCK4_A, SCK4_B, SCK4_C and SCK6_B
Other pins have high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC=VCC2.

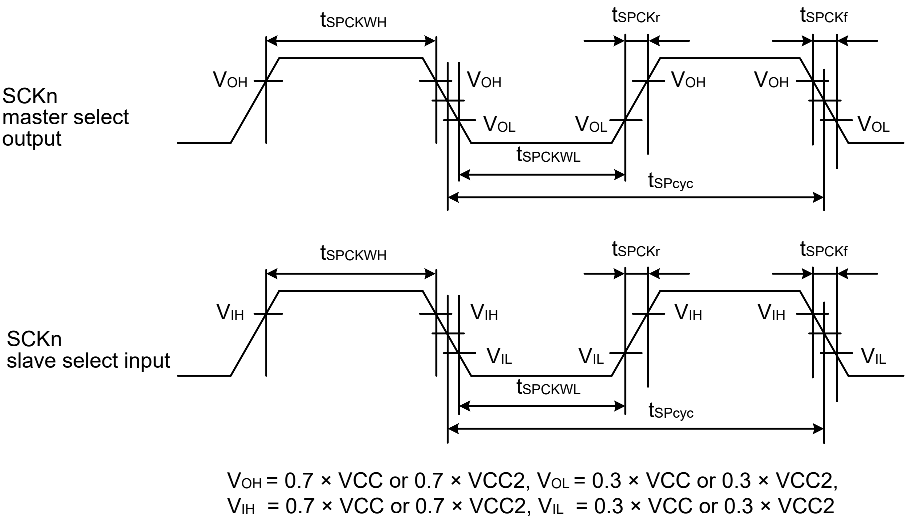
Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
SCK clock cycle output	Master	—	2.70 V or above	t_{Scyc}	2 (TCLK ≤ 120MHz) 4 (TCLK > 120MHz)	—	t_{Tcyc}	
			1.62 V or above		2 (TCLK ≤ 60MHz) 4 (TCLK ≤ 120MHz) 8 (TCLK > 120MHz)	—		
SCK clock cycle input	Slave	—	2.70 V or above		2	—		
			1.62 V or above		2 (TCLK ≤ 100MHz) 4 (TCLK > 100MHz)	—		
SCK clock high pulse width	Master	—	1.62 V or above	t_{SCKWH}	0.4	0.6	t_{Scyc}	
	Slave		1.62 V or above					
SCK clock low pulse width	Master	—	1.62 V or above	t_{SCKWL}	0.4	0.6	t_{Scyc}	
	Slave		1.62 V or above					

Table 2.60 SCI timing (Clock synchronous mode) (2 of 2)

Condition 1: VCC/VCC2 = 2.70 V or above
High drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.
Condition 2: VCC/VCC2 = 1.62 V or above
Following pins have high-speed high-drive output selected in the Port Drive Capability bit in the PmnPFS register: SCK1_A, SCK1_C, SCK3_A, SCK4_A, SCK4_B, SCK4_C and SCK6_B
Other pins have high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC=VCC2.

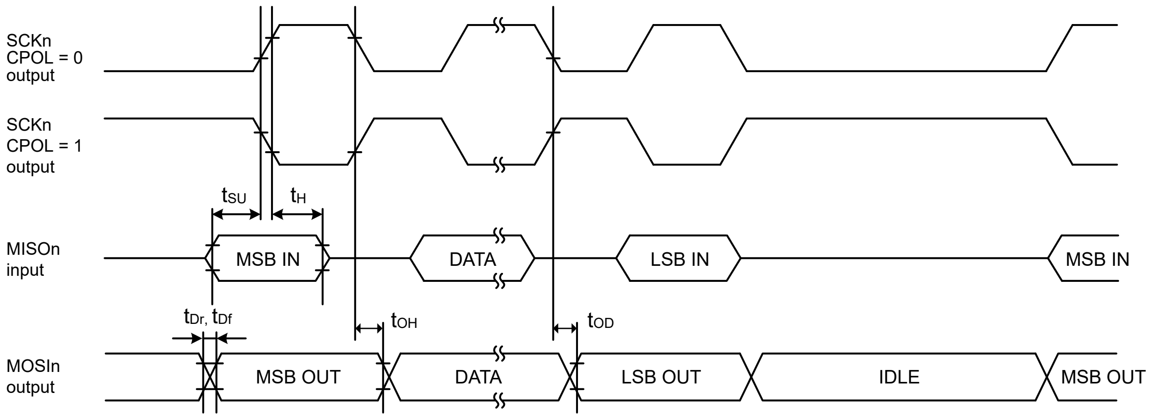
Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
SCK clock rise and fall time	Output	—	2.70 V or above	t_{SCKr}, t_{SCKf}	—	3.3	ns	
			1.62 V or above		—	6.6		
	Input	—	1.62 V or above		—	0.1[*3]	t_{Scyc}	
Data input setup time	Master	High Speed[*1]	2.70 V or above	t_{SU}	2.6	—	ns	
			1.62 V or above		2.6	—		
		Default[*2]	2.70 V or above		2.8	—		
			1.62 V or above		2.8	—		
	Slave	Default[*2]	2.70 V or above		3.3	—		
			1.62 V or above		5.3	—		
Data input hold time	Master	High Speed[*1]	2.70 V or above	t_H	7.5	—	ns	
			1.62 V or above		9.5	—		
		Default[*2]	2.70 V or above		7.5	—		
			1.62 V or above		9.5	—		
	Slave	Default[*2]	2.70 V or above		3.0	—		
			1.62 V or above		5.0	—		
Data output delay	Master	High Speed[*1]	2.70 V or above	t_{OD}	—	5	ns	
			1.62 V or above		—	5		
		Default[*2]	2.70 V or above		—	7.3		
			1.62 V or above		—	7.3		
	Slave	High Speed[*1]	2.70 V or above		—	12.5		
			1.62 V or above		—	20.5		
		Default[*2]	2.70 V or above		—	18.5		
			1.62 V or above		—	26.5		
Data rise and fall time	Output	—	2.70 V or above	t_{Dr}, t_{Df}	—	3.3	ns	
			1.62 V or above		—	6.6		
	Input	—	1.62 V or above		—	1	μs	

Note: t_{Tcyc}: TCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, _C, to indicate group membership. SCI0, SCI1, SCI2, SCI3 and SCI9 are instance _A, SCI4 and SCI5 are instance _B, SCI6, SCI7 and SCI8 are instance _C.
Note 2. All pins of group membership can be used.
Note 3. 1 μs at the longest



Note: n = 0 to 4, 9

Figure 2.70 SCI simple SPI mode clock timing



Note: n = 0 to 4, 9

Figure 2.71 SCI simple SPI mode timing for master when CPHA = 0

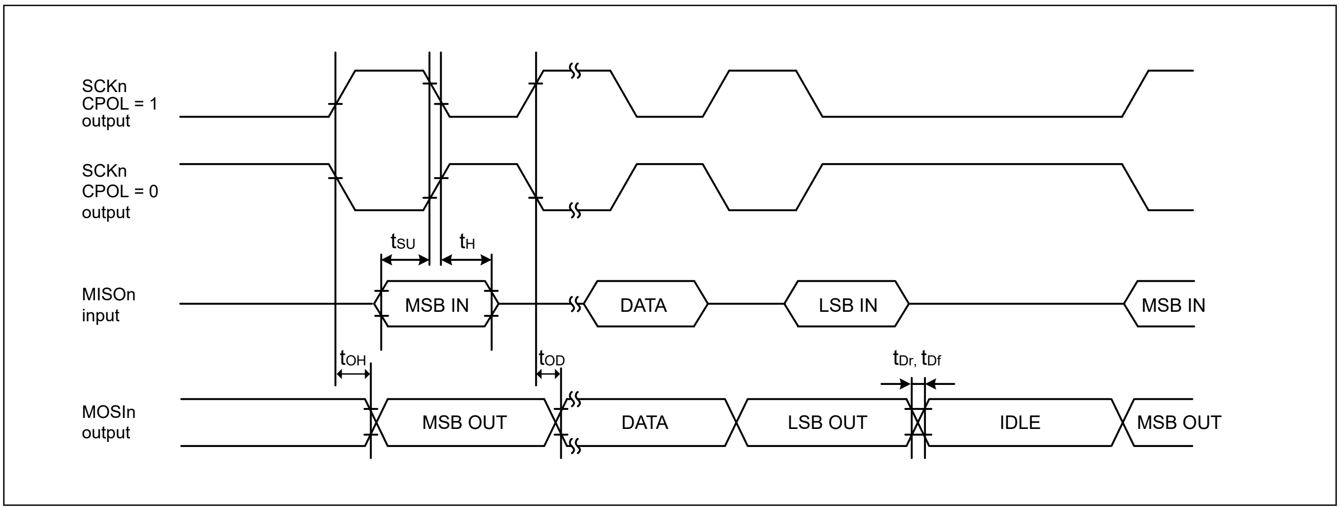


Figure 2.72 SCI simple SPI mode timing for master when CPHA = 1

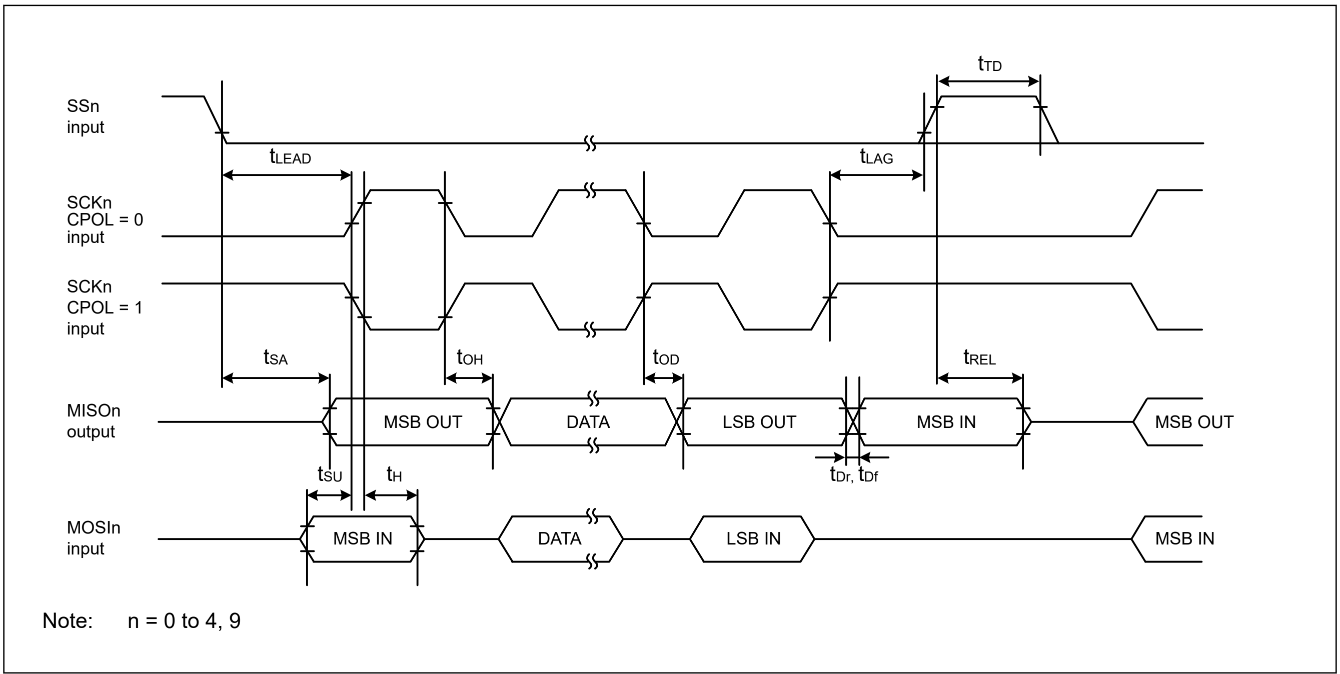


Figure 2.73 SCI simple SPI mode timing for slave when CPHA = 0

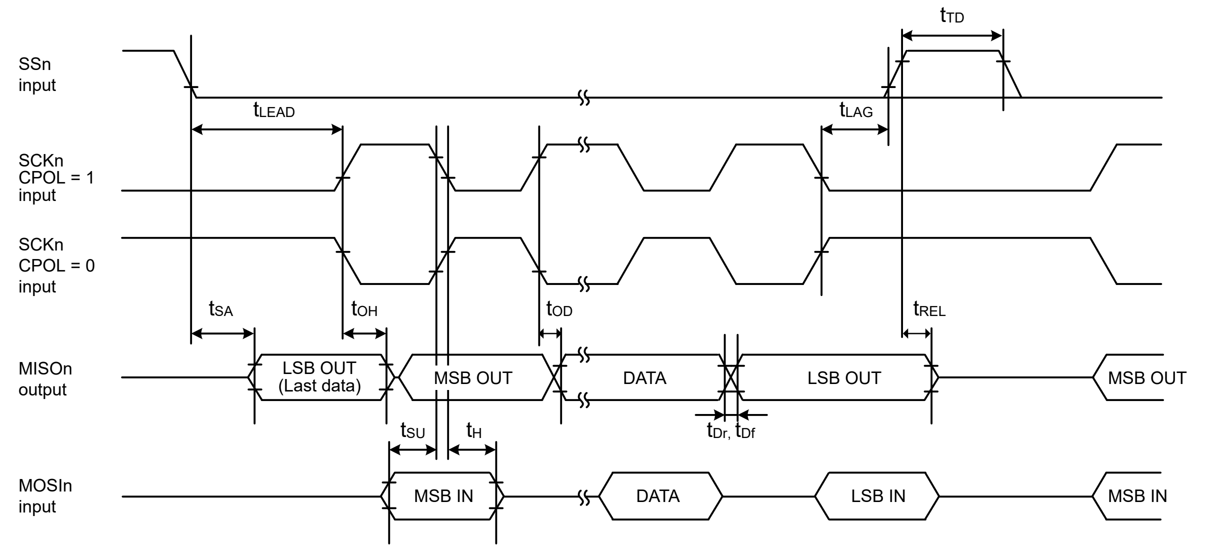


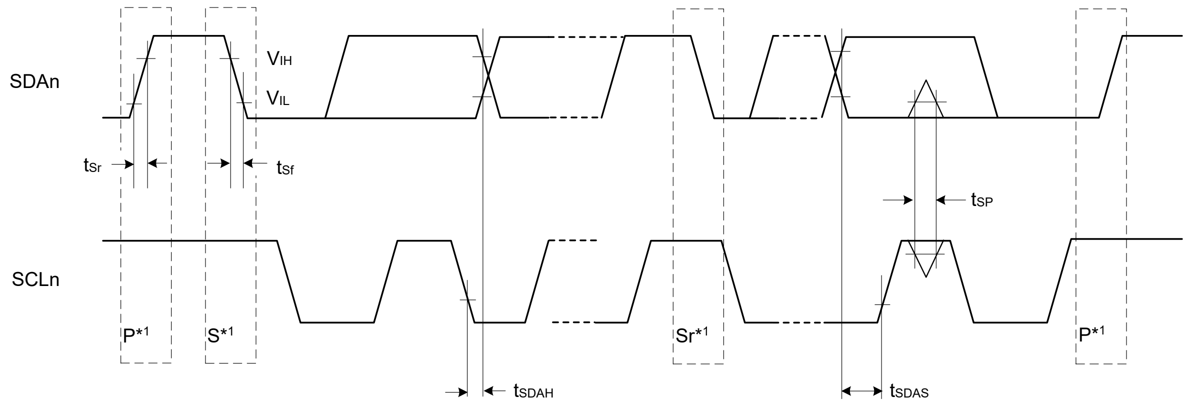
Figure 2.74 SCI simple SPI mode timing for slave when CPHA = 1

Table 2.61 SCI timing (Simple IIC mode)

Conditions:
Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.
VCC/VCC2 : 1.62 V or above
If SCI pins are specified across the VCC I/O and VCC2 I/O, characteristics below is guaranteed only when VCC = VCC2.

Parameter		Symbol	Min	Max	Unit	Note
Simple IIC (Standard mode)	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast mode)	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	4 × t_{Tcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*1	—	400	pF	

Note: t_{Tcyc}: TCLK cycle.
Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7 or VCC2 × 0.7
V_{IL} = VCC × 0.3 or VCC2 × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 4, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.75 SCI simple IIC mode timing

2.3.10 SPI Timing

Table 2.62 SPI timing (1 of 5)

Conditions:

1. High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: RSPCLKA_B, RSPCLKB_B.
   For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
RSPCK clock cycle	Master	High Speed*1	3.00 V or above	t_{SPcyc}	2	4096	t_{Tcyc}	Figure 2.76
		High Speed*1	2.70 V or above		2 (TCLK ≤ 166.6MHz) 4 (TCLK > 166.6 MHz)	4096		
		High Speed*1	1.62 V or above		2 (TCLK ≤ 83.3MHz) 4 (TCLK ≤ 166.6 MHz) 8 (TCLK > 166.6 MHz)	4096		
		Default*2	3.00 V or above		2 (TCLK ≤ 166.6 MHz) 4 (TCLK > 166.6 MHz)	4096		
		Default*2	2.70 V or above		2 (TCLK ≤ 120MHz) 4 (TCLK ≤ 240 MHz) 8 (TCLK > 240 MHz)	4096		
		Default*2	1.62 V or above		2 (TCLK ≤ 60 MHz) 4 (TCLK ≤ 120 MHz) 8 (TCLK ≤ 240 MHz) 16 (TCLK > 240 MHz)	4096		
	Slave	High Speed*1	3.00 V or above		2 (TCLK ≤ 266 MHz) 4 (TCLK > 266 MHz)	—		
		High Speed*1	2.70 V or above		2 (TCLK ≤ 166.6 MHz) 4 (TCLK > 166.6 MHz)	—		
		High Speed*1	1.62 V or above		2 (TCLK ≤ 83.3MHz) 4 (TCLK ≤ 166.6 MHz) 8 (TCLK > 166.6 MHz)	—		
		Default*2	3.00 V or above		2 (TCLK ≤ 166.6 MHz) 4 (TCLK > 166.6 MHz)	—		
		Default*2	2.70 V or above		2 (TCLK ≤ 120 MHz) 4 (TCLK ≤ 240 MHz) 8 (TCLK > 240 MHz)	—		
		Default*2	1.62 V or above		2 (TCLK ≤ 60 MHz) 4 (TCLK ≤ 120 MHz) 8 (TCLK ≤ 240 MHz) 16 (TCLK > 240 MHz)	—		

Table 2.62 SPI timing (2 of 5)

Conditions:

1. High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: RSPCLKA_B, RSPCLKB_B.
   For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
RSPCK clock high pulse width	Master	—	3.00 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 1$	—	ns	Figure 2.76
		—	2.70 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 2$	—		
		—	1.62 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—		
	Slave	—	1.62 V or above		0.4	—	t_{SPcyc}	
RSPCK clock low pulse width	Master	—	3.00 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 1$	—	ns	
		—	2.70 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 2$	—		
		—	1.62 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—		
	Slave	—	1.62 V or above		0.4	—	t_{SPcyc}	
RSPCK clock rise and fall time	Output	High Speed*1	3.00 V or above	t_{SPCKr}, t_{SPCKf}	—	0.80	ns	
		High Speed*1	2.70 V or above		—	1.40		
		High Speed*1	1.62 V or above		—	2.50		
		Default*2	3.00 V or above		—	1.66		
		Default*2	2.70 V or above		—	3.30		
		Default*2	1.62 V or above		—	6.60		
	Input	—	3.00 V or above		—	0.1*3	μs	
		—	2.70 V or above		—	0.1*3		
		—	1.62 V or above		—	0.1*3		

Table 2.62 SPI timing (3 of 5)

Conditions:

1. High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: RSPCLKA_B, RSPCLKB_B.
   For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Data input setup time	Master	—	3.00 V or above	t_{SU}	−2.5	—	ns	Figure 2.77, Figure 2.78
		—	2.70 V or above		0.0	—		
		—	1.62 V or above		0.0	—		
	Slave	High Speed*1	3.00 V or above		1.5	—		
		High Speed*1	2.70 V or above		1.5	—		
		High Speed*1	1.62 V or above		1.5	—		
		Default*2	3.00 V or above		2.5	—		
		Default*2	2.70 V or above		2.5	—		
		Default*2	1.62 V or above		2.5	—		
Data input hold time	Master	—	3.00 V or above	t_H	7.5	—	ns	
		—	2.70 V or above		7.5	—		
		—	1.62 V or above		9.5	—		
	Slave	High Speed*1	3.00 V or above		1.5	—		
		High Speed*1	2.70 V or above		1.5	—		
		High Speed*1	1.62 V or above		1.5	—		
		Default*2	3.00 V or above		2.5	—		
		Default*2	2.70 V or above		2.5	—		
		Default*2	1.62 V or above		5.5	—		
SSL setup time	Master	—	3.00 V or above	t_{LEAD}	$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$	ns	Figure 2.77, Figure 2.78
		—	2.70 V or above		$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$		
		—	1.62 V or above		$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$		
	Slave	—	3.00 V or above		5.0	—	t_{Tcyc}	
		—	2.70 V or above		5.0	—		
		—	1.62 V or above		5.0	—		
SSL hold time	Master	—	3.00 V or above	t_{LAG}	$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$	ns	
		—	2.70 V or above		$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$		
		—	1.62 V or above		$1 \times t_{SPcyc}$–- 10	$8 \times t_{SPcyc} + 10$		
	Slave	—	3.00 V or above		5.0	—	t_{Tcyc}	
		—	2.70 V or above		5.0	—		
		—	1.62 V or above		5.0	—		

Table 2.62 SPI timing (4 of 5)

Conditions:

1. High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: RSPCLKA_B, RSPCLKB_B.
   For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance “_A” or “_B” to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition “3.00 V or above”.

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
TI SSP SS input setup time	Slave	—	3.00 V or above	t_{TISS}	2.5	—	ns	Figure 2.82
		—	2.70 V or above		2.5	—		
		—	1.62 V or above		2.5	—		
TI SSP SS input hold time	Slave	—	3.00 V or above	t_{TISH}	2.5	—	ns	
		—	2.70 V or above		2.5	—		
		—	1.62 V or above		5.5	—		
TI SSP next-access time	Slave	—	3.00 V or above	t_{TIND}	2 × t_{Tcyc} + SLNDL × t_{Tcyc}	—	ns	
		—	2.70 V or above		2 × t_{Tcyc} + SLNDL × t_{Tcyc}	—		
		—	1.62 V or above		2 × t_{Tcyc} + SLNDL × t_{Tcyc}	—		
TI SSP master SS output delay	Master	—	3.00 V or above	t_{TISSOD}	—	4.0	ns	Figure 2.79
		—	2.70 V or above		—	8.0		
		—	1.62 V or above		—	8.0		
Data output delay time	Master	—	3.00 V or above	t_{OD1}	—	2.0	ns	Figure 2.77, Figure 2.78
		—	2.70 V or above		—	3.0		
		—	1.62 V or above		—	6.0		
		High Speed*1	3.00 V or above	t_{OD2}	—	1.5		
		High Speed*1	2.70 V or above		—	2.5		
		High Speed*1	1.62 V or above		—	4.5		
		Default*2	3.00 V or above		—	2.5		
		Default*2	2.70 V or above		—	2.5		
		Default*2	1.62 V or above		—	4.5		
	Slave	—	3.00 V or above	t_{OD}	—	10.0		
		—	2.70 V or above		—	13.5		
		—	1.62 V or above		—	21.5		
Data output hold time	Master	High Speed*1	3.00 V or above	t_{OH}	−1.5	—	ns	
		High Speed*1	2.70 V or above		−2.5	—		
		High Speed*1	1.62 V or above		−4.5	—		
		Default*2	3.00 V or above		−2.5	—		
		Default*2	2.70 V or above		−2.5	—		
		Default*2	1.62 V or above		−4.5	—		
	Slave	—	3.00 V or above		0.0	—		
		—	2.70 V or above		0.0	—		
		—	1.62 V or above		0.0	—		

Table 2.62 SPI timing (5 of 5)

Conditions:

1. High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: RSPCLKA_B, RSPCLKB_B.
   For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
2. Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership.
3. Load capacitance C = 15pF is applied to the VCC/VCC2 condition "3.00 V or above".

Parameter		High Speed/ Default	VCC/VCC2	Symbol	Min	Max	Unit	Note
Successive transmission delay time	Master	—	3.00 V or above	t_{TD}	t_{SPcyc} + 2 × t_{Tcyc}	8 × t_{SPcyc} + 2 × t_{Tcyc}	ns	Figure 2.77, Figure 2.78
		—	2.70 V or above		t_{SPcyc} + 2 × t_{Tcyc}	8 × t_{SPcyc} + 2 × t_{Tcyc}		
		—	1.62 V or above		t_{SPcyc} + 2 × t_{Tcyc}	8 × t_{SPcyc} + 2 × t_{Tcyc}		
	Slave	—	3.00 V or above		t_{Tcyc}	—	ns	
		—	2.70 V or above		t_{Tcyc}	—		
		—	1.62 V or above		t_{Tcyc}	—		
MOSI and MISO rise and fall time	Output	—	3.00 V or above	t_{Dr}, t_{Df}	—	1.66	ns	
		—	2.70 V or above		—	3.30		
		—	1.62V or above		—	6.60		
	Input	—	3.00 V or above		—	1.0	μs	
		—	2.70 V or above		—	1.0		
		—	1.62 V or above		—	1.0		
SSL rise and fall time	Output	—	3.00- V or above	t_{SSLr}, t_{SSLf}	—	1.66	ns	
		—	2.70 V or above		—	3.30		
		—	1.62 V or above		—	6.60		
	Input	—	3.00 V or above		—	1.0	μs	
		—	2.70 V or above		—	1.0		
		—	1.62 V or above		—	1.0		
Slave access time	Slave	—	3.00 V or above	t_{SA}	—	20.0	ns	Figure 2.80, Figure 2.81
		—	2.70 V or above		—	20.0		
		—	1.62 V or above		—	25.0		
Slave output release time	Slave	—	3.00 V or above	t_{REL}	—	20.0	ns	
		—	2.70 V or above		—	20.0		
		—	1.62 V or above		—	25.0		

Note: t_{Tcyc}: TCLK cycle.
Note 1. Must use pins that have a letter appended to their name, for instance _A, _B, to indicate group membership. SPI0 and SPI1 are instance _B.
Note 2. All pins of group membership can be used.
Note 3. 1 μs at the longest

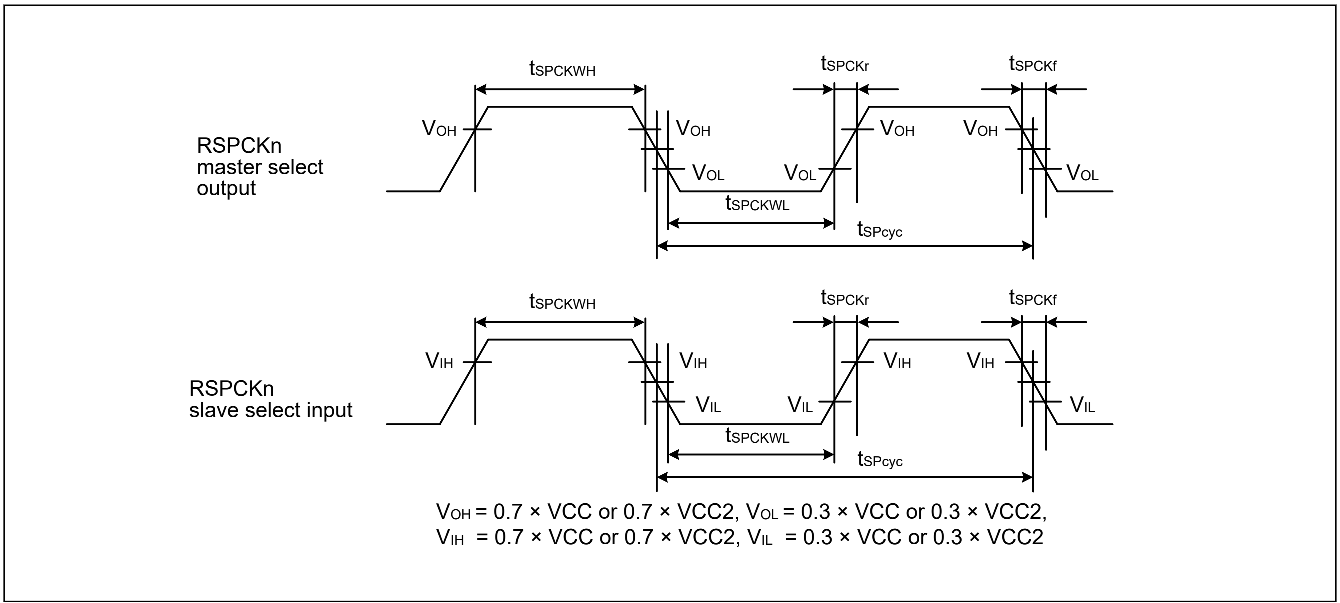


Figure 2.76 SPI clock timing

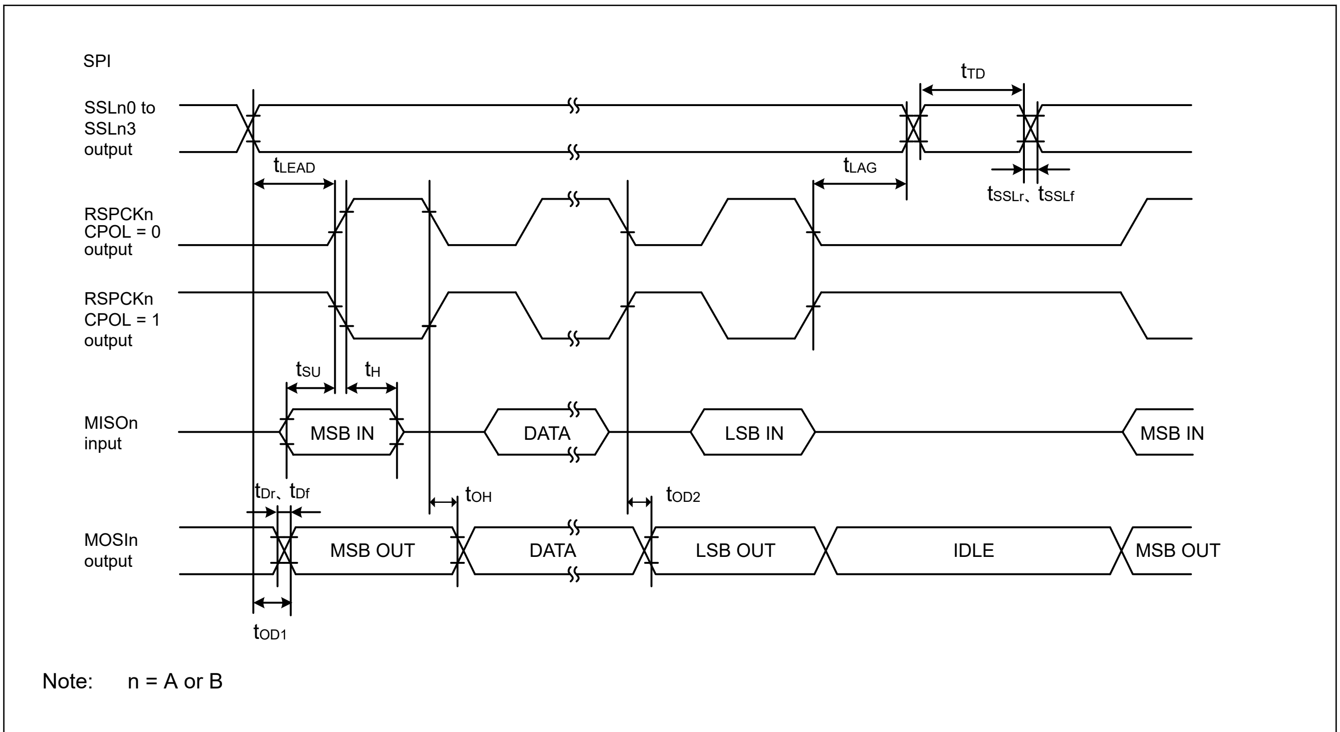


Figure 2.77 SPI timing for Motorola SPI master when CPHA = 0

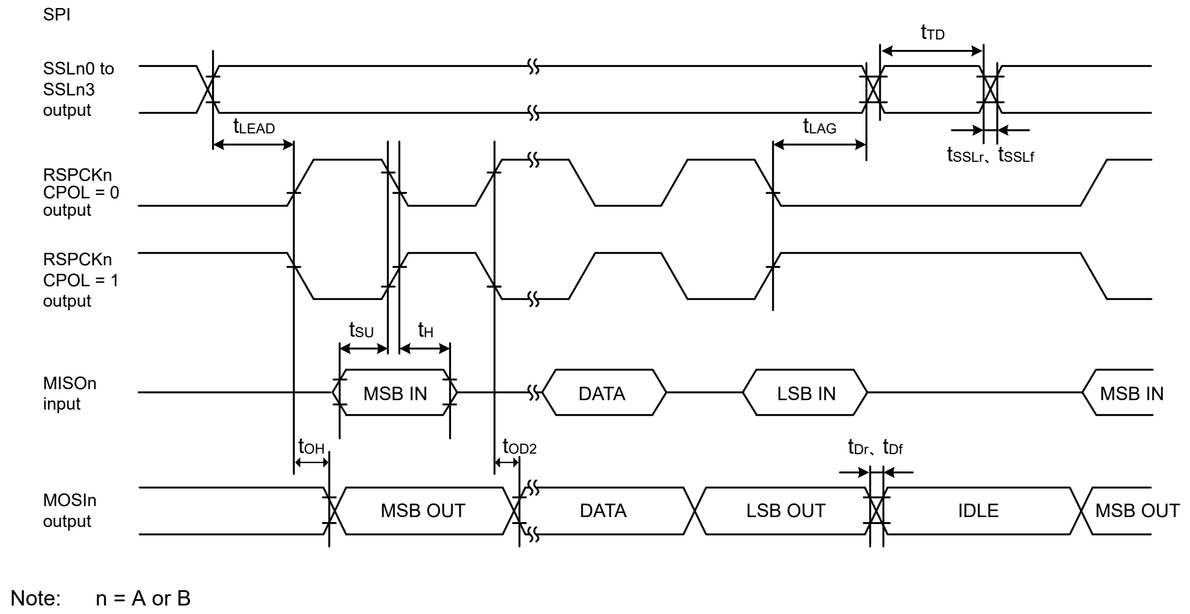


Figure 2.78 SPI timing for Motorola SPI master when CPHA = 1

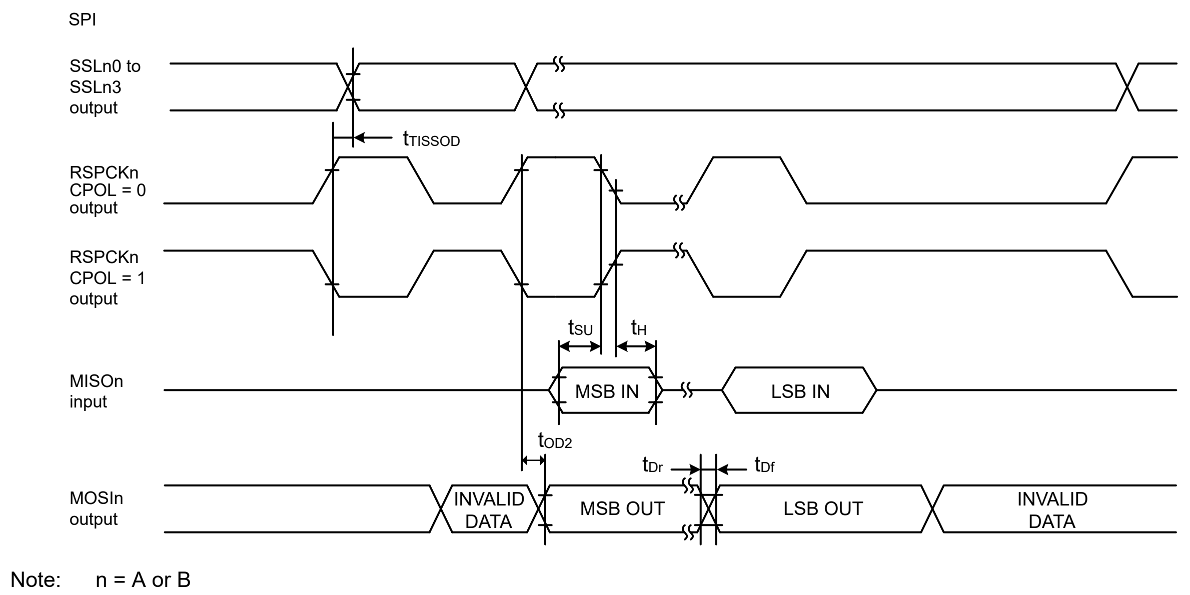


Figure 2.79 SPI timing for TI SSP master

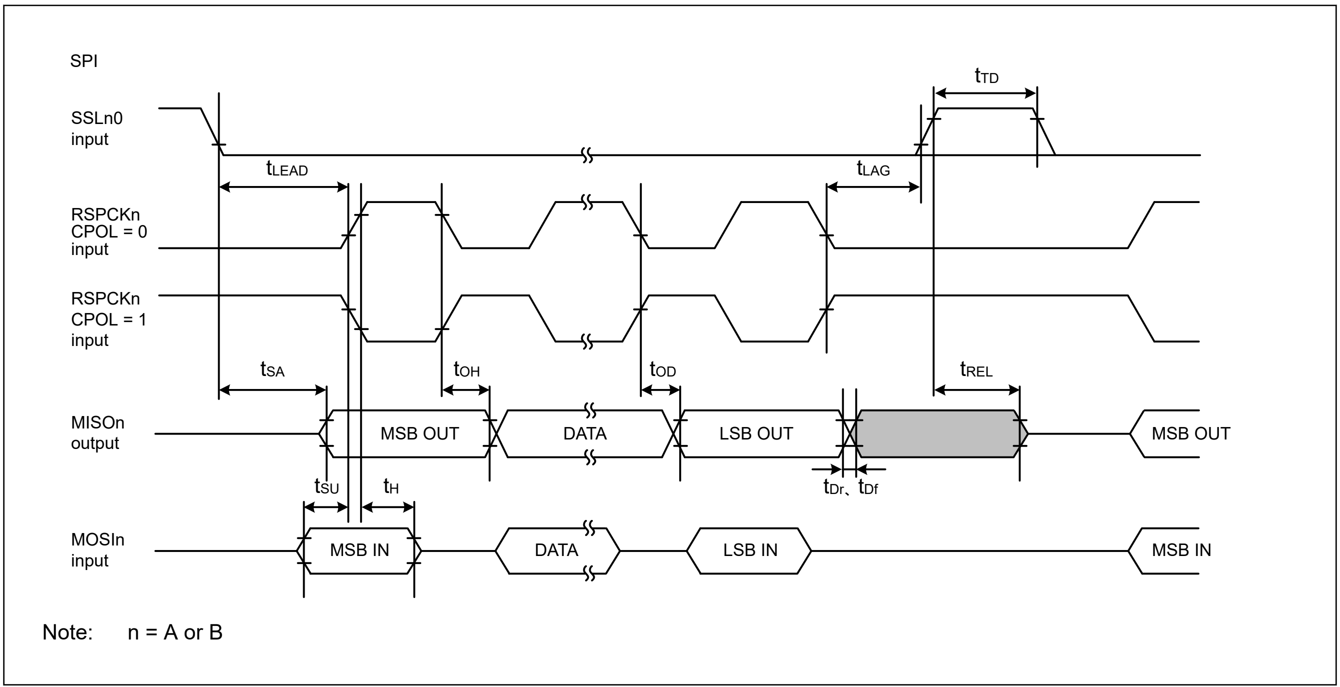


Figure 2.80 SPI timing for Motorola SPI slave when CPHA = 0

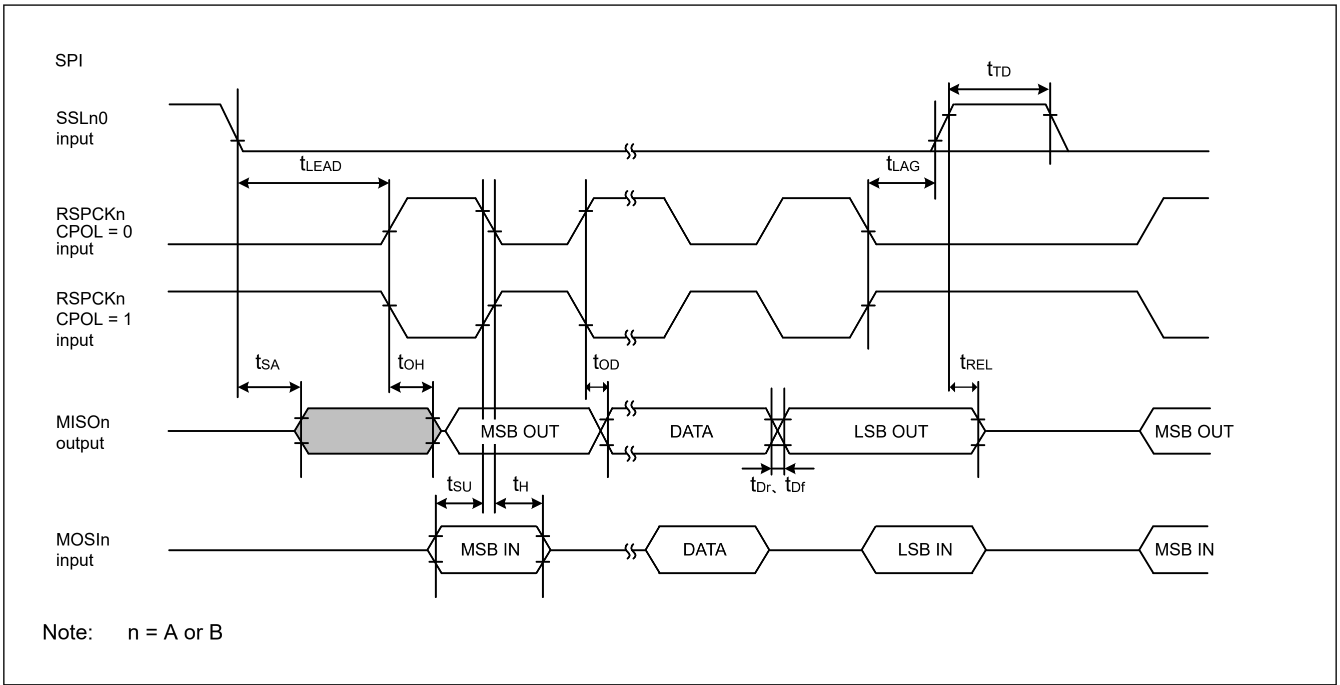


Figure 2.81 SPI timing for Motorola SPI slave when CPHA = 1

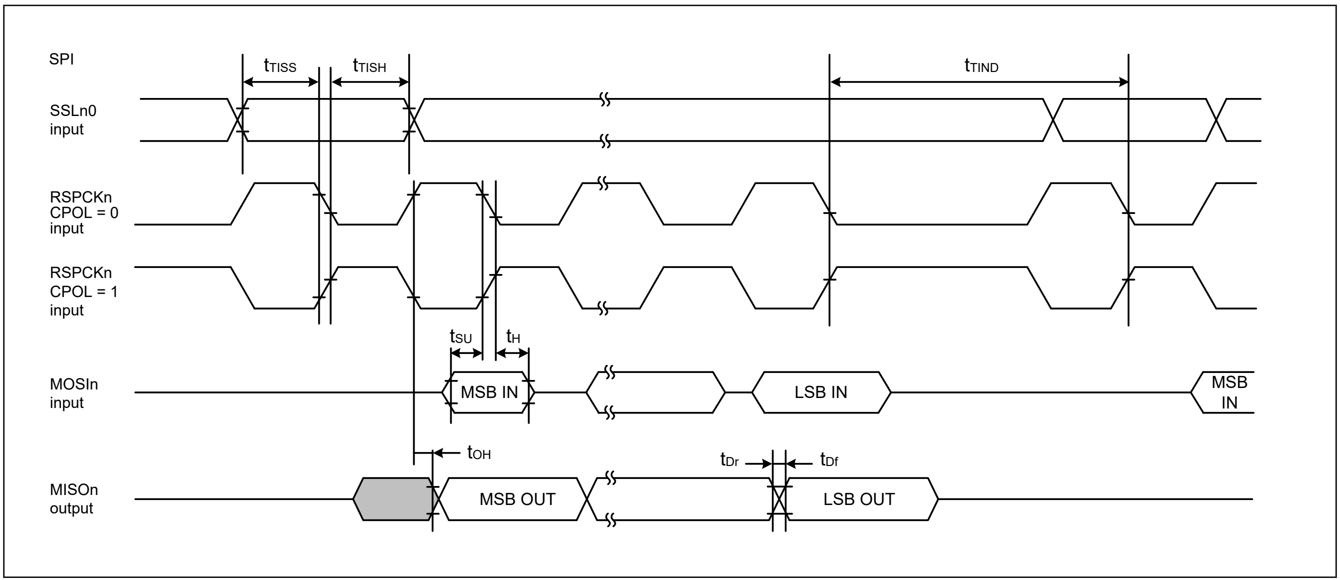


Figure 2.82 SPI timing for TI SSP slave when transmit with delay between frames

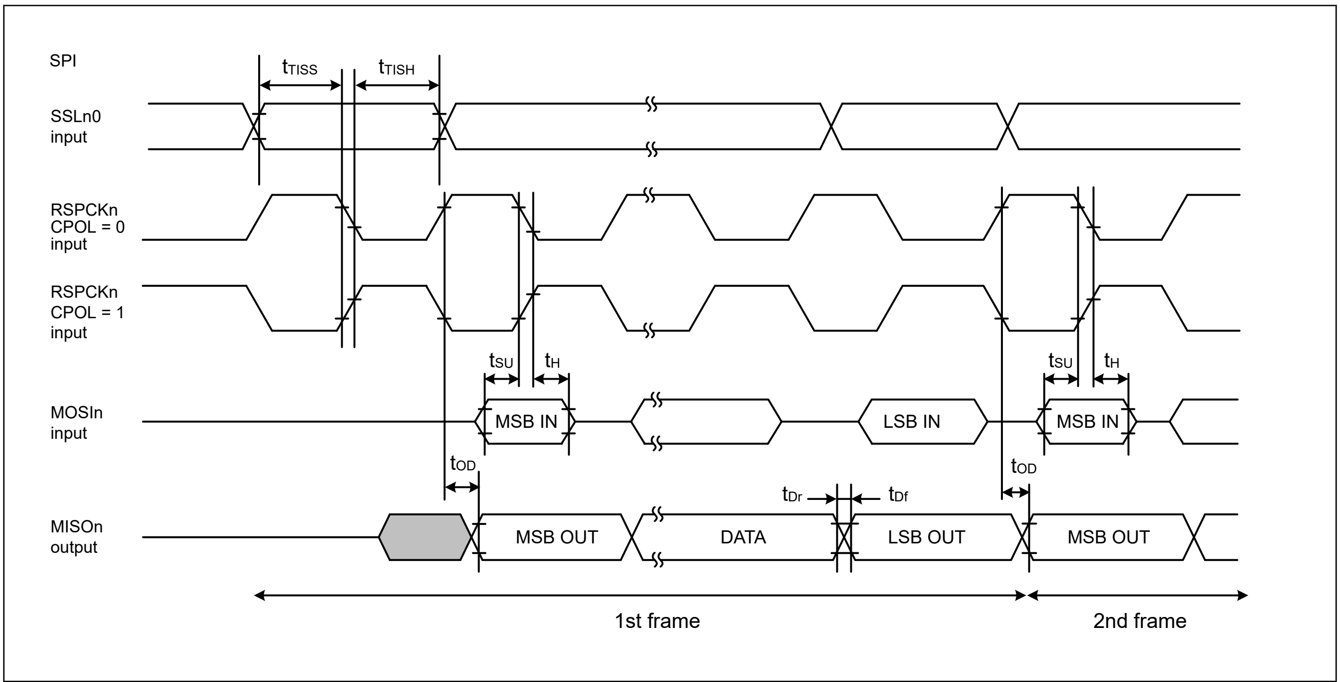


Figure 2.83 SPI timing for TI SSP slave when transmit with no delay between frames

2.3.11 OSPI Timing

Table 2.63 OSPI timing (1 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item		Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Cycle time	SDR without OM_DQS	t_{PERIOD}	2.70 V or above	VSCR_1, voltage range 1	16.67	—	ns	Figure 2.84
				VSCR_2, voltage range 2				
			1.62 V to 2.00 V	VSCR_1, voltage range 1	20.00	—		
				VSCR_2, voltage range 2				
	SDR with OM_DQS/DDR	t_{PERIOD}	2.70 V or above	VSCR_1, voltage range 1	6.00	—	ns	
				VSCR_2, voltage range 2	7.50	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				
Clock output slew rate		t_{SRck}	2.70 V or above	VSCR_1, voltage range 1	0.94	—	V/ns	Figure 2.84
				VSCR_2, voltage range 2	0.75	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				
Clock Duty cycle-distortion		t_{CKDCD}	2.70 V or above	VSCR_1, voltage range 1	0	0.3	ns	Figure 2.84
				VSCR_2, voltage range 2	0	0.375		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				

Table 2.63 OSPI timing (2 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item	Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Clock Minimum Pulse width	t_{CKMPW}	2.70 V or above	VSCR_1, voltage range 1	2.7	—	ns	Figure 2.84
			VSCR_2, voltage range 2	3.375	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
Differential clock crossing voltage	$V_{ox}(AC)$	2.70 V or above	VSCR_1, voltage range 1	0.2 × VCC2	0.6 × VCC2	V	Figure 2.84
			VSCR_2, voltage range 2				
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
DS Duty cycle distortion	t_{DSDCD}	2.70 V or above	VSCR_1, voltage range 1	0	0.24	ns	Figure 2.84
			VSCR_2, voltage range 2	0	0.3		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
DS Minimum Pulse width	t_{DSMPW}	2.70 V or above	VSCR_1, voltage range 1	2.46	—	ns	Figure 2.84
			VSCR_2, voltage range 2	3.075	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				

Table 2.63 OSPI timing (3 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item		Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Data input/output slew rate		t_{SR}	2.70 V or above	VSCR_1, voltage range 1	1.72	—	ns	Figure 2.84
				VSCR_2, voltage range 2	1.37	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1	0.75	—		
				VSCR_2, voltage range 2				
Data input setup time (to OM_SCLK/ OM_SCLKN)	SDR without OM_DQS	t_{SU}	2.70 V or above	VSCR_1, voltage range 1	8.17	—	ns	Figure 2.85
				VSCR_2, voltage range 2				
			1.62 V to 2.00 V	VSCR_1, voltage range 1	13.0	—		
				VSCR_2, voltage range 2				
Data input hold time (to OM_SCLK/ OM_SCLKN)		t_H	2.70 V or above	VSCR_1, voltage range 1	0.5	—	ns	
				VSCR_2, voltage range 2				
			1.62 V to 2.00 V	VSCR_1, voltage range 1	0.5	—		
				VSCR_2, voltage range 2				

Table 2.63 OSPI timing (4 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item		Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Data output valid time	SDR without OM_DQS	t_{OV}*2	2.70 V or above	VSCR_1, voltage range 1	—	5.4	ns	Figure 2.85
				VSCR_2, voltage range 2				
			1.62 V to 2.00 V	VSCR_1, voltage range 1	—	6.9		
				VSCR_2, voltage range 2				
Data output hold time		t_{OH}	2.70 V or above	VSCR_1, voltage range 1	−5.4	—	ns	
				VSCR_2, voltage range 2				
			1.62 V to 2.00 V	VSCR_1, voltage range 1	−6.9	—		
				VSCR_2, voltage range 2				
Data output buffer off time		t_{BOFF}	2.70 V or above	VSCR_1, voltage range 1	−5.4	—	ns	
				VSCR_2, voltage range 2				
			1.62 V to 2.00 V	VSCR_1, voltage range 1	−6.9	—		
				VSCR_2, voltage range 2				

Table 2.63 OSPI timing (5 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item		Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Data input setup time (to OM_DQS)	SDR with OM_DQS/DDR	t_{SU}	2.70 V or above	VSCR_1, voltage range 1	−0.58	—	ns	Figure 2.86, Figure 2.87
				VSCR_2, voltage range 2	−0.7	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				
Data input hold time (to OM_DQS)		t_H	2.70 V or above	VSCR_1, voltage range 1	1.88	—	ns	
				VSCR_2, voltage range 2	2.375	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				

Table 2.63 OSPI timing (6 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item		Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Data output valid time	SDR with OM_DQS/DDR	t_{OV}*2	2.70 V or above	VSCR_1, voltage range 1	—	$t_{PERIOD}/4 + 0.5$	ns	Figure 2.86, Figure 2.87
				VSCR_2, voltage range 2	—	$t_{PERIOD}/4 + 0.6$		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				
Data output hold time		t_{OH}	2.70 V or above	VSCR_1, voltage range 1	0.7	—	ns	
				VSCR_2, voltage range 2	0.9	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				
Data output buffer off time		t_{BOFF}	2.70 V or above	VSCR_1, voltage range 1	0.7	—	ns	
				VSCR_2, voltage range 2	0.9	—		
			1.62 V to 2.00 V	VSCR_1, voltage range 1				
				VSCR_2, voltage range 2				

Table 2.63 OSPI timing (7 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item	Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Clock Low to CS Low	t_{CKLCSL}	2.70 V or above	VSCR_1, voltage range 1	4.8	—	ns	Figure 2.85, Figure 2.86, Figure 2.87
			VSCR_2, voltage range 2	6	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
CS Low to Clock High	t_{CSLCKH}*3	2.70 V or above	VSCR_1, voltage range 1	4.8	—	ns	
			VSCR_2, voltage range 2	6	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
Clock Low to CS High	t_{CKLCSH}	2.70 V or above	VSCR_1, voltage range 1	4.8	—	ns	
			VSCR_2, voltage range 2	6	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
CS High to Clock High	t_{CSHCKH}	2.70 V or above	VSCR_1, voltage range 1	4.8	—	ns	
			VSCR_2, voltage range 2	6	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				

Table 2.63 OSPI timing (8 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item	Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
DS Low output to CS High	t_{CSHCKH}	2.70 V or above	VSCR_1, voltage range 1	0.8 × t_{PERIOD}	—	ns	Figure 2.88
			VSCR_2, voltage range 2	0.8 × t_{PERIOD}	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
CS High to DS Tri-State	t_{CSHDST}	2.70 V or above	VSCR_1, voltage range 1	—	t_{PERIOD}	ns	
			VSCR_2, voltage range 2	—	t_{PERIOD}		
		1.62 V to 2.00V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				
CS Low to DS Low input*1 *3	t_{CSLDSL}	2.70 V or above	VSCR_1, voltage range 1	0	12.5	ns	
			VSCR_2, voltage range 2	0	20		
		1.62 V to 2.00 V	VSCR_1, voltage range 1	0	12.5		
			VSCR_2, voltage range 2				
DS Tri-State to CS Low	t_{DSTCSL}	2.70 V or above	VSCR_1, voltage range 1	0	—	ns	
			VSCR_2, voltage range 2	0	—		
		1.62 V to 2.00 V	VSCR_1, voltage range 1				
			VSCR_2, voltage range 2				

Table 2.63 OSPI timing (9 of 9)

Conditions:
High-speed high drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_SCLK, OM_n_SCLKN, OM_n_SIO7-0, OM_n_DQS.
Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: OM_n_CS0, OM_n_CS1.
Load capacitance C = 15pF

Item	Symbol	VCC/VCC2	VDD	Min	Max	Unit	Note
Clock High to DQS input*4	t_{CKHDSH}	2.70 V or above	VSCR_1, voltage range 1	—	t_{PERIOD} × (1 + DDRSMPEX [3:0]) − 8.5	ns	Figure 2.86
			VSCR_2, voltage range 2				
		1.62 V to 2.00 V	VSCR_1, voltage range 1	—	t_{PERIOD} × (1 + DDRSMPEX [3:0]) − 12.5		
			VSCR_2, voltage range 2				

Note: n = 0, 1
Note 1. This restriction does not need to be met when using the JESD251 Profile 1.0 memory with an external pull-down attached to the OM_DQS pin.
Note 2. Condition: COMCFG.OEASTEX = 1
Note 3. Condition: LIOCFGCSx.CSASTEX = 1
Note 4. See the datasheet of memory and set DDRSMPEX[3:0] bits to satisfy this value.

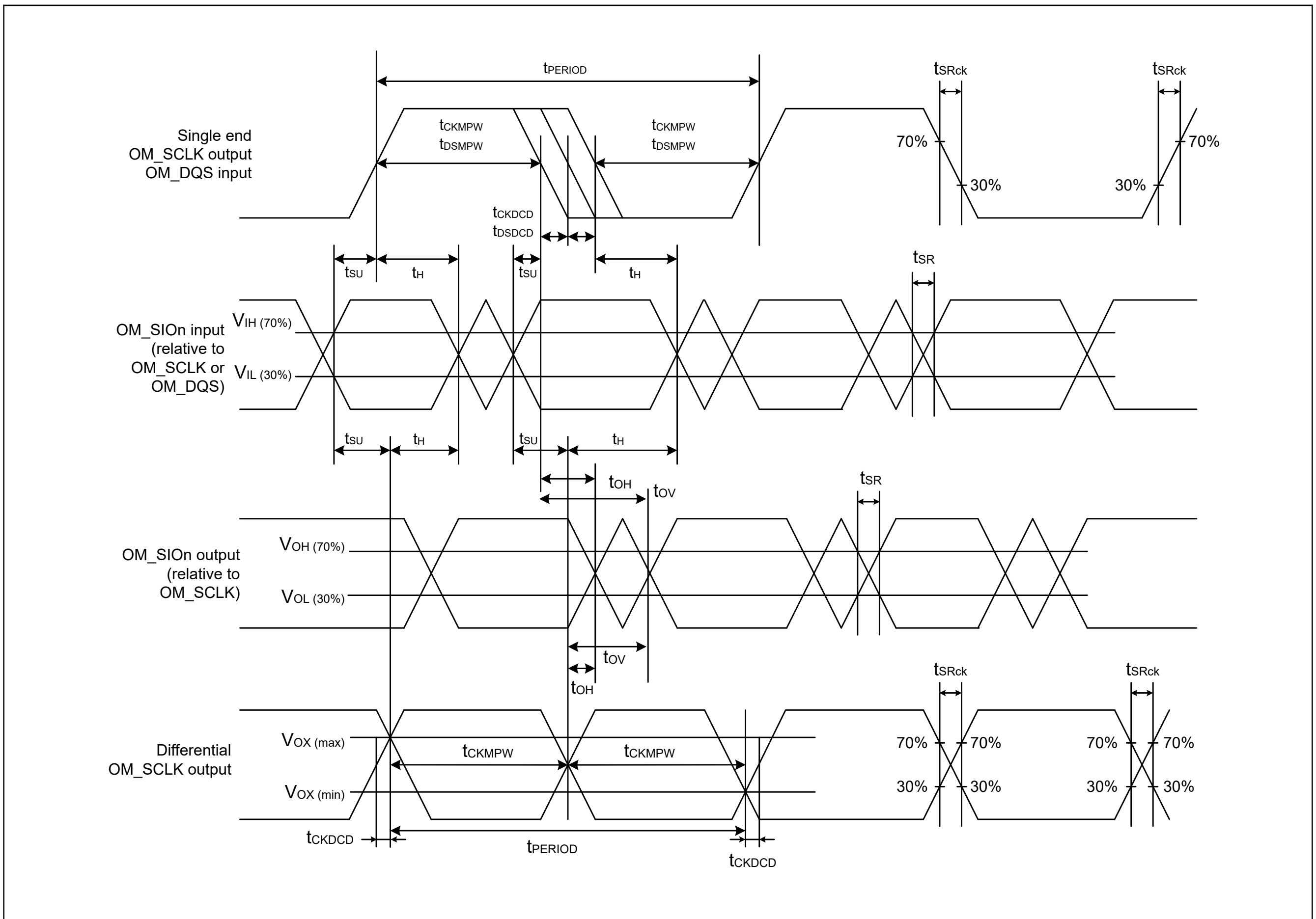


Figure 2.84 OSPI clock / DS timing

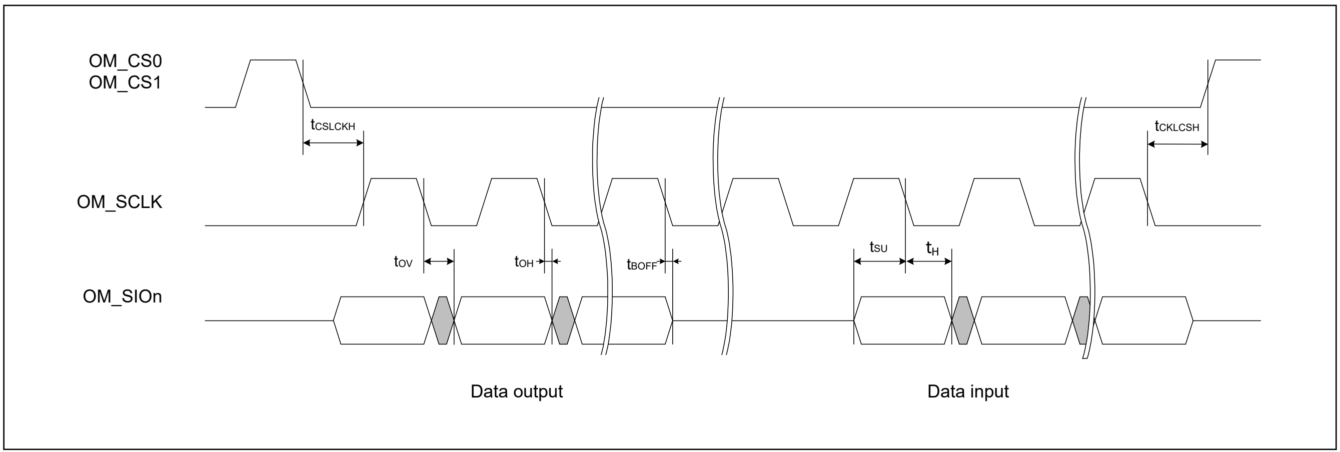


Figure 2.85 SDR transmit/receive timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

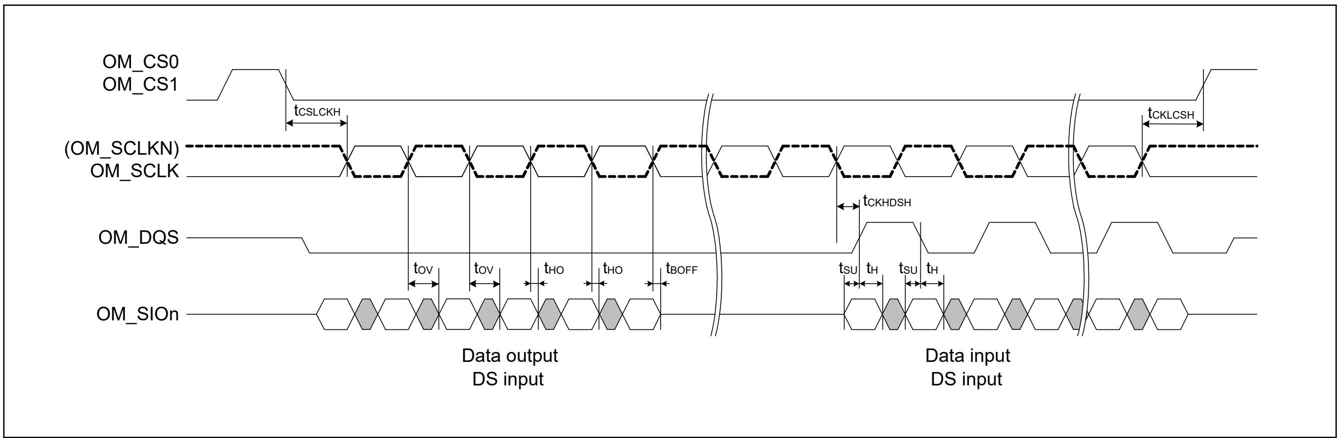


Figure 2.86 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

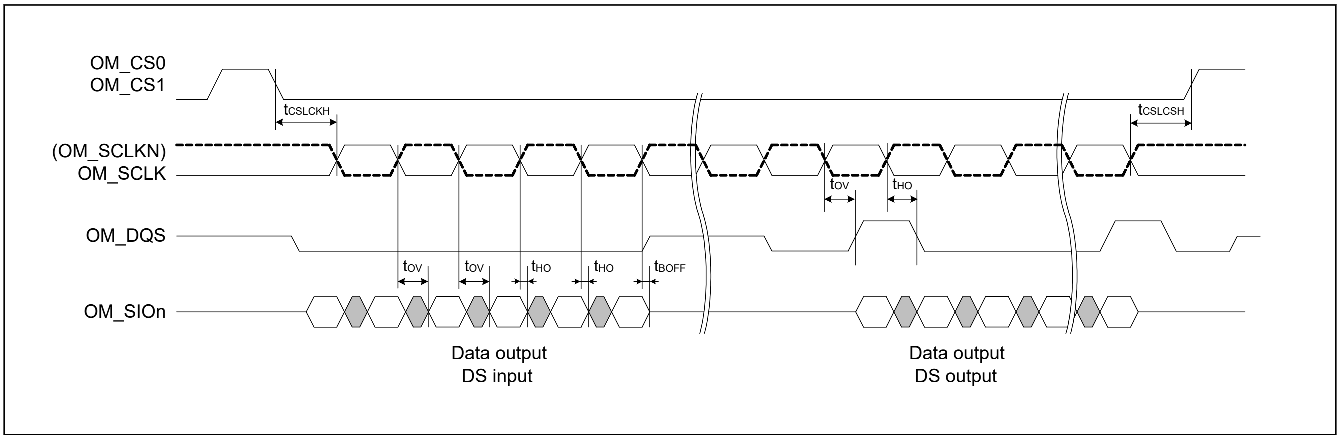


Figure 2.87 DDR transmit/receive timing (HyperRAM write)

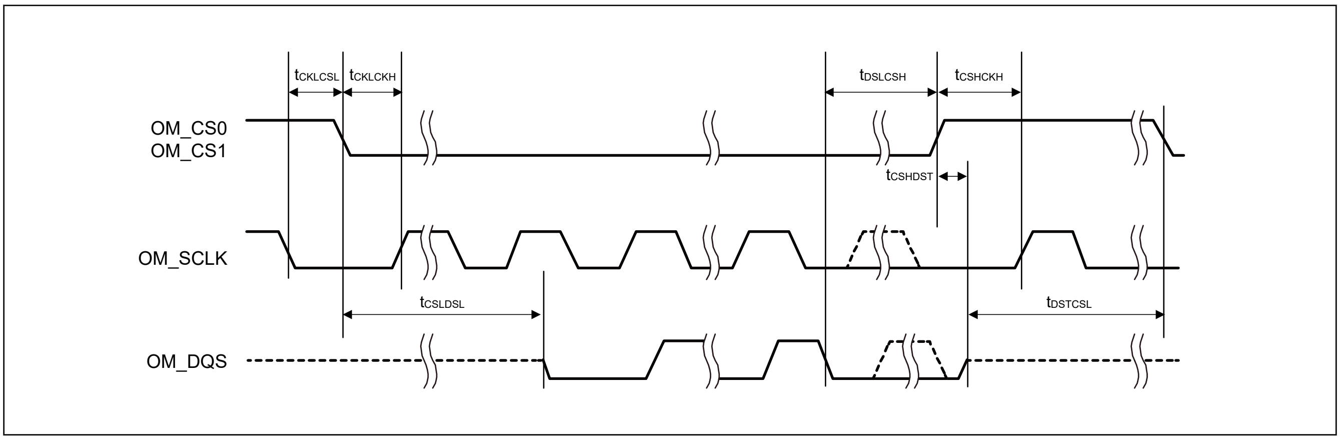


Figure 2.88 DS to CS signal timing

2.3.12 IIC Timing

Table 2.64 IIC timing (1) (1 of 2)

Conditions:

1. Middle drive output is selected when VCC is 2.70 V or above, High drive output is selected when VCC is 1.62 to 1.95 V in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SDA2_B, SCL2_B
2. The following pins do not require setting: SCL0_A, SDA0_A. SCL1_A, SDA1_A. SCL2_A, SDA2_A
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership.

For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	2.70 V or above	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.89
			1.62 to 1.95 V				
	SCL input high pulse width	t_{SCLH}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	SCL input low pulse width	t_{SCLL}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	SCL, SDA rise time	t_{Sr}	2.70 V or above	—	1000	ns	
			1.62 to 1.95 V				
	SCL, SDA fall time	t_{Sf}	2.70 V or above	—	300	ns	
			1.62 to 1.95 V				
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{IICcyc}	ns	
			1.62 to 1.95 V				
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
			1.62 to 1.95 V				
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
			1.62 to 1.95 V				
	Repeated START condition input setup time	t_{STAS}	2.70 V or above	1000	—	ns	
			1.62 to 1.95 V				
	STOP condition input setup time	t_{STOS}	2.70 V or above	1000	—	ns	
			1.62 to 1.95 V				
	Data input setup time	t_{SDAS}	2.70 V or above	t_{IICcyc} + 50	—	ns	
			1.62 to 1.95 V				
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns	
			1.62 to 1.95 V				
	SCL, SDA capacitive load	C_b	2.70 V or above	—	400	pF	
			1.62 to 1.95 V				

Table 2.64 IIC timing (1) (2 of 2)

Conditions:

1. Middle drive output is selected when VCC is 2.70 V or above, High drive output is selected when VCC is 1.62 to 1.95 V in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_B, SCL1_B, SDA2_B, SCL2_B
2. The following pins do not require setting: SCL0_A, SDA0_A. SCL1_A, SDA1_A. SCL2_A, SDA2_A
3. Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership.

For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
IIC (Fast mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	2.70 V or above	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.89
			1.62 to 1.95 V				
	SCL input high pulse width	t_{SCLH}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	SCL input low pulse width	t_{SCLL}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	SCL, SDA rise time	t_{Sr}	2.70 V or above	20	300	ns	
			1.62 to 1.95 V				
	SCL, SDA fall time	t_{Sf}	2.70 V or above	20 × (external pullup voltage/5.5 V)*1	300	ns	
			1.62 to 1.95 V				
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{IICcyc}	ns	
			1.62 to 1.95 V				
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
			1.62 to 1.95 V				
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{IICcyc} + 300	—	ns	
			1.62 to 1.95 V				
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
			1.62 to 1.95 V				
	Repeated START condition input setup time	t_{STAS}	2.70 V or above	300	—	ns	
			1.62 to 1.95 V				
	STOP condition input setup time	t_{STOS}	2.70 V or above	300	—	ns	
			1.62 to 1.95 V				
	Data input setup time	t_{SDAS}	2.70 V or above	t_{IICcyc} + 50	—	ns	
			1.62 to 1.95 V				
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns	
			1.62 to 1.95 V				
	SCL, SDA capacitive load	C_b	2.70 V or above	—	400	pF	
			1.62 to 1.95 V				

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note: Must use pins that have a letter appended to their name, for instance "_A", "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.
Note 1. Only supported for SCL0_A, SDA0_A, SCL1_A, SDA1_A, SCL2_A, and SDA2_A.

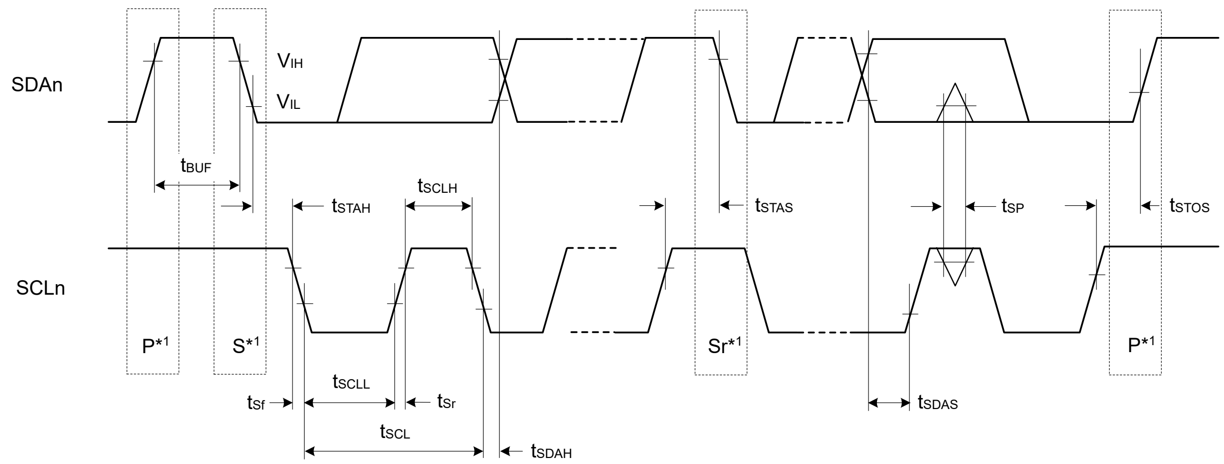
Table 2.65 IIC timing (2)

Setting of the SCL0_A, SDA0_A, SCL1_A, SDA1_A. SCL2_A, SDA2_A pins are not required with the port drive capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	2.70 V or above	6 (12) × t_{IICcyc} + 240	—	ns	Figure 2.89
			1.62 to 1.95V				
	SCL input high pulse width	t_{SCLH}	2.70 V or above	3 (6) × t_{IICcyc} + 120	—	ns	
			1.62 to 1.95V				
	SCL input low pulse width	t_{SCLL}	2.70 V or above	3 (6) × t_{IICcyc} + 120	—	ns	
			1.62 to 1.95V				
	SCL, SDA rise time	t_{Sr}	2.70 V or above	—	120	ns	
			1.62 to 1.95V				
	SCL, SDA fall time	t_{Sf}	2.70 V or above	20 × (external pullup voltage/ 5.5V)	120	ns	
			1.62 to 1.95V				
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above	0	1 (4) × t_{IICcyc}	ns	
			1.62 to 1.95V				
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 120	—	ns	
			1.62 to 1.95V				
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	—	ns	
			1.62 to 1.95V				
	Start condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above	t_{IICcyc} + 120	—	ns	
			1.62 to 1.95V				
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	—	ns	
			1.62 to 1.95V				
	Restart condition input setup time	t_{STAS}	2.70 V or above	120	—	ns	
			1.62 to 1.95V				
	Stop condition input setup time	t_{STOS}	2.70 V or above	120	—	ns	
			1.62 to 1.95V				
	Data input setup time	t_{SDAS}	2.70 V or above	t_{IICcyc} + 30	—	ns	
			1.62 to 1.95V				
	Data input hold time	t_{SDAH}	2.70 V or above	0	—	ns	
			1.62 to 1.95V				
	SCL, SDA capacitive load	C_b*1	2.70 V or above	—	550	pF	
			1.62 to 1.95V				

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, tPcyc: PCLKB cycle.

Note: Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 1. Cb indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.89 I²C bus interface input/output timing

2.3.13 I3C Timing

Table 2.66 IIC timing (1)-1

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit
IIC (Standard mode, SMBus) BFCTL.FMPE = 0	SCL input cycle time	t_{SCL}	2.70 V or above, 1.65 to 1.95 V	10 (18) × t_{I3Ccyc} + 1300	—	ns
	SCL input high pulse width	t_{SCLH}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	2.70 V or above, 1.65 to 1.95 V	—	1000	ns
	SCL, SDA fall time	t_{Sf}	2.70 V or above, 1.65 to 1.95 V	—	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above, 1.65 to 1.95 V	0	1 (4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above, 1.65 to 1.95 V	5(9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled	t_{BUF}	2.70 V or above, 1.65 to 1.95 V	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above, 1.65 to 1.95 V	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled	t_{STAH}	2.70 V or above, 1.65 to 1.95 V	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	2.70 V or above, 1.65 to 1.95 V	1000	—	ns
	STOP condition input setup time	t_{STOS}	2.70 V or above, 1.65 to 1.95 V	1000	—	ns
	Data input setup time	t_{SDAS}	2.70 V or above, 1.65 to 1.95 V	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	2.70 V or above, 1.65 to 1.95 V	0	—	ns
	SCL, SDA capacitive load	C_b[*1]	2.70 V or above, 1.65 to 1.95 V	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: TCLK cycle.

Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.

Table 2.67 IIC timing (1)-2

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	2.70 V or above, 1.65 to 1.95 V	10 (18) × t_{I3Ccyc} + 600	—	ns
	SCL input high pulse width	t_{SCLH}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL input low pulse width	t_{SCLL}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SCL, SDA rise time	t_{Sr}	2.70 V or above, 1.65 to 1.95 V	20	300	ns
	SCL, SDA fall time	t_{Sf}	2.70 V or above, 1.65 to 1.95 V	20 × (external pull-up voltage/3.6 V)	300	ns
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above, 1.65 to 1.95 V	0	1 (4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 300	—	ns
	SDA input bus free time when wakeup function is enabled		2.70 V or above, 1.65 to 1.95 V	5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 300	—	ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above, 1.65 to 1.95 V	t_{I3Ccyc} + 300	—	ns
	START condition input hold time when wakeup function is enabled		2.70 V or above, 1.65 to 1.95 V	1(5) × t_{I3Ccyc} + t_{Tcyc} + 300	—	ns
	Repeated START condition input setup time	t_{STAS}	2.70 V or above, 1.65 to 1.95 V	300	—	ns
	STOP condition input setup time	t_{STOS}	2.70 V or above, 1.65 to 1.95 V	300	—	ns
	Data input setup time	t_{SDAS}	2.70 V or above, 1.65 to 1.95 V	t_{I3Ccyc} + 50	—	ns
	Data input hold time	t_{SDAH}	2.70 V or above, 1.65 to 1.95 V	0	—	ns
	SCL, SDA capacitive load	C_b*1	2.70 V or above, 1.65 to 1.95 V	—	400	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: TCLK cycle.

Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.

Table 2.68 IIC timing (1)-3

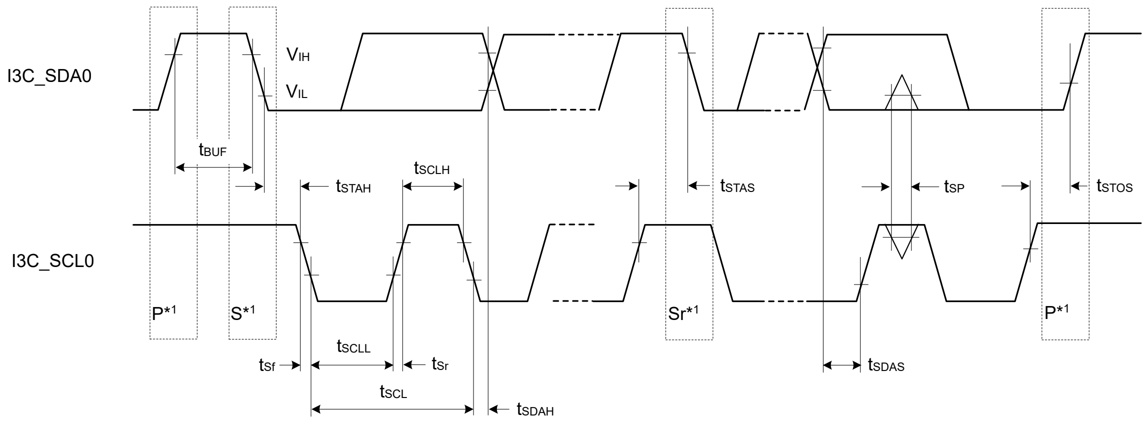
Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit
IIC (Fast-mode +) BFCTL.FMPE = 1	SCL input cycle time	t_{SCL}	2.70 V or above, 1.65 to 1.95 V	10 (18) × t_{I3Ccyc} + 240	—	ns
	SCL input high pulse width	t_{SCLH}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 120	—	ns
	SCL input low pulse width	t_{SCLL}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 120	—	ns
	SCL, SDA rise time	t_{Sr}	2.70 V or above, 1.65 to 1.95 V	—	120	ns
	SCL, SDA fall time	t_{Sf}	2.70 V or above, 1.65 to 1.95 V	20 × (external pull-up voltage/3.3V)	120	ns
	SCL, SDA input spike pulse removal time	t_{SP}	2.70 V or above, 1.65 to 1.95 V	0	1 (4) × t_{I3Ccyc}	ns
	SDA input bus free time when wakeup function is disabled	t_{BUF}	2.70 V or above, 1.65 to 1.95 V	5 (9) × t_{I3Ccyc} + 120	—	ns
	SDA input bus free time when wakeup function is enabled			5(9) × t_{I3Ccyc} + 4 × t_{Tcyc} + 120		ns
	START condition input hold time when wakeup function is disabled	t_{STAH}	2.70 V or above, 1.65 to 1.95 V	t_{I3Ccyc} + 120	—	ns
	START condition input hold time when wakeup function is enabled			1(5) × t_{I3Ccyc} + t_{Tcyc} + 120		ns
	Restart condition input setup time	t_{STAS}	2.70 V or above, 1.65 to 1.95 V	120	—	ns
	Stop condition input setup time	t_{STOS}	2.70 V or above, 1.65 to 1.95 V	120	—	ns
	Data input setup time	t_{SDAS}	2.70 V or above, 1.65 to 1.95 V	t_{I3Ccyc} + 30	—	ns
	Data input hold time	t_{SDAH}	2.70 V or above, 1.65 to 1.95 V	0	—	ns
	SCL, SDA capacitive load	C_b*1	2.70 V or above, 1.65 to 1.95 V	—	550	pF

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle, t_{Tcyc}: TCLK cycle.

Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.

Note 1. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA (BFCTL.FMPE = 0)
V_{OL} = 0.4 V, I_{OL} = 15 mA (BFCTL.FMPE = 1)

Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.90 I²C bus interface input/output timing

Table 2.69 IIC timing (2)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	VCC	Min	Max	Unit
IIC (Hs-mode) BFCTL.HSME = 1	SCL input cycle time		t_{SCL}	3.00 V or above	46 (48) × t_{I3Ccyc}	—	ns
				1.65 to 1.95 V	46 (48) × t_{I3Ccyc}	—	
	SCL input high pulse width	Cb = 400 pF	t_{SCLH}	3.00 V or above	29 (30) × t_{I3Ccyc}	—	ns
				1.65 to 1.95 V	29 (30) × t_{I3Ccyc}	—	
		Cb = 100 pF		3.00 V or above	13 (14) × t_{I3Ccyc}	—	
				1.65 to 1.95 V	13 (14) × t_{I3Ccyc}	—	
	SCL input low pulse width	Cb = 400 pF	t_{SCLL}	3.00 V or above	69 (70) × t_{I3Ccyc}	—	ns
				1.65 to 1.95 V	69 (70) × t_{I3Ccyc}	—	
		Cb = 100 pF		3.00 V or above	33 (34) × t_{I3Ccyc}	—	
				1.65 to 1.95 V	33 (34) × t_{I3Ccyc}	—	
	SCL rise time	Cb = 400 pF	t_{SrCL}	3.00 V or above	—	80	ns
				1.65 to 1.95 V	—	80	
		Cb = 100 pF		3.00 V or above	—	40	
				1.65 to 1.95 V	—	40	
	SDA rise time	Cb = 400 pF	t_{SrDA}	3.00 V or above	—	160	ns
				1.65 to 1.95 V	—	160	
		Cb = 100 pF		3.00 V or above	—	80	
				1.65 to 1.95 V	—	80	
	SCL fall time	Cb = 400 pF	t_{SfCL}	3.00 V or above	—	80	ns
				1.65 to 1.95 V	—	80	
		Cb = 100 pF		3.00 V or above	—	40	
				1.65 to 1.95 V	—	40	
	SDA fall time	Cb = 400 pF	t_{SfDA}	3.00 V or above	—	160	ns
				1.65 to 1.95 V	—	160	
		Cb = 100 pF		3.00 V or above	—	80	
				1.65 to 1.95 V	—	80	
	SCL, SDA input spike pulse removal time		t_{SP}	3.00 V or above	0	1 (1) × t_{I3Ccyc}	ns
				1.65 to 1.95 V	0	1 (1) × t_{I3Ccyc}	
	Repeated START condition input setup time		t_{STAS}	3.00 V or above	40	—	ns
				1.65 to 1.95 V	40	—	
	STOP condition input setup time		t_{STOS}	3.00 V or above	40	—	ns
				1.65 to 1.95 V	40	—	
	Data input setup time		t_{SDAS}	3.00 V or above	10	—	ns
				1.65 to 1.95 V	10	—	
	Data input hold time	Cb = 400 pF	t_{SDAH}	3.00 V or above	0	150	ns
				1.65 to 1.95 V	0	150	
		Cb = 100 pF		3.00 V or above	0	70	
				1.65 to 1.95 V	0	70	
	SCL, SDA capacitive load		C_b*1	3.00 V or above	—	400	pF
				1.65 to 1.95 V	—	400	

Note: t_{I3Ccyc}: I3C internal reference clock (I3Cφ) cycle.
Note: Values in parentheses apply when INCTL.DNFS[3:0] is set to 0011b while the digital filter is enabled with INCTL.DNFE set to 1.
Note 1. C_b indicates the total capacity of the bus line.

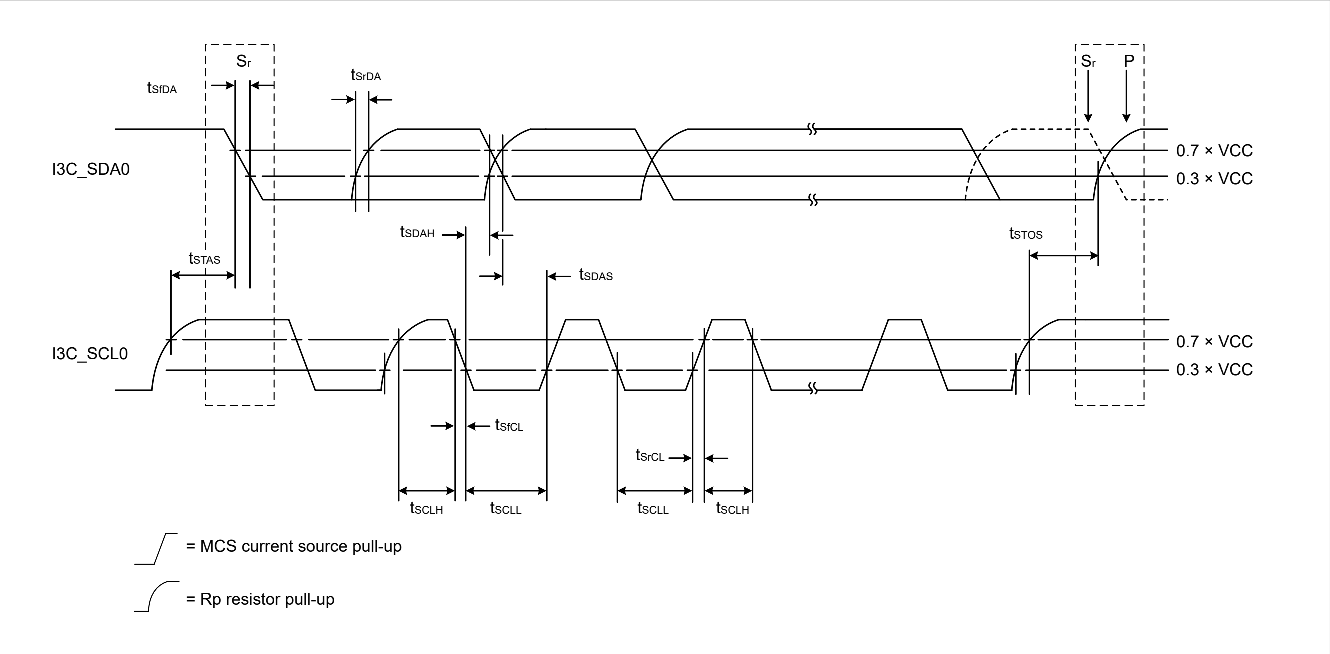


Figure 2.91 **I^2C bus interface input/output timing (Hs-mode)**

Table 2.70 I3C timing (Open Drain Timing Parameters)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
I3C Open Drain Timing Parameters	SCL Clock Low Period	t_{LOW_OD} *1 *2	3.00 V or above	200	—	ns	Figure 2.94
			1.65 to 1.95 V	200	—		
		$t_{DIG\_OD\_L}$	3.00 V or above	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—	ns	Figure 2.94
			1.65 to 1.95 V	$t_{LOW\_ODmin} + t_{fDA\_ODmin}$	—		
	SCL Clock High Period	t_{HIGH} *3 *4	3.00 V or above	—	41	ns	Figure 2.92
			1.65 to 1.95 V	—	41		
		t_{DIG_H}	3.00 V or above	—	$t_{HIGH} + t_{CF}$	ns	Figure 2.92
			1.65 to 1.95 V	—	$t_{HIGH} + t_{CF}$		
	SDA Signal Fall Time	t_{fDA_OD}	3.00 V or above	t_{CF}	12	ns	Figure 2.94
			1.65 to 1.95 V	t_{CF}	12		
	SDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	3.00 V or above	12	—	ns	Figure 2.93
			1.65 to 1.95 V	18	—		
	Clock After START (S) Condition	t_{CAS} *5 *6	3.00 V or above	38.4 nano	For ENAS0: 1 µ	seconds	Figure 2.94
					For ENAS1: 100 µ		
					For ENAS2: 2 milli		
					For ENAS3: 50 milli		
			1.65 to 1.95 V	38.4 nano	For ENAS0: 1 µ		
					For ENAS1: 100 µ		
					For ENAS2: 2 milli		
					For ENAS3: 50 milli		
	Clock Before STOP (P) Condition	t_{CBP}	3.00 V or above	t_{CASmin} / 2	—	seconds	Figure 2.95
			1.65 to 1.95 V	t_{CASmin} / 2	—		
	Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	3.00 V or above	$t_{DIG\_OD\_Lmin}$	—	ns	Figure 2.101
			1.65 to 1.95 V	$t_{DIG\_OD\_Lmin}$	—		
	Bus Available Condition	t_{AVAL} *7	3.00 V or above	1	—	µs	—
			1.65 to 1.95 V	1	—		
	Bus Idle Condition	t_{IDLE}	3.00 V or above	1	—	ms	—
			1.65 to 1.95 V	1	—		
	Time Internal Where New Master Not Driving SDA Low	t_{MMLock}	3.00 V or above	$t_{AVALmin}$	—	µs	Figure 2.101
			1.65 to 1.95 V	$t_{AVALmin}$	—		

Note 1. This is approximately equal to $t_{LOWmin} + t_{DS\_ODmin} + t_{rDA\_ODtyp} + t_{SU\_Odmin}$.

Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that SDA is already above VIH

Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I^2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).
As a product specification, if this Max value cannot be guaranteed, change this Max value and specify that it cannot be used in the Mixed Bus.

Note 5. On a Legacy Bus where I^2C Devices need to see Start

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3

Note 7. On a Mixed Bus with Fm Legacy I^2C Devices, t_{AVAL} is 300 ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 2.71 I3C timing (Push-Pull Timing Parameters for SDR and HDR-DDR Modes)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter			Symbol	VCC	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes	SCL Clock Frequency		f_{SCL} *1	3.00 V or above	0.01	12.5	MHz	—
				1.65 to 1.95 V	0.01	12.5		
	SCL Clock Low Period		t_{LOW}	3.00 V or above	27	—	ns	Figure 2.92
				1.65 to 1.95 V	32	—		
			t_{DIG_L} *2 *4	3.00 V or above	35	—	ns	Figure 2.92
				1.65 to 1.95 V	40	—		
	SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	3.00 V or above	24	—	ns	Figure 2.92
				1.65 to 1.95 V	27	—		
			$t_{DIG\_H\_MIXED}$ *2 *3	3.00 V or above	32	45	ns	Figure 2.92
				1.65 to 1.95 V	35	45		
	SCL Clock High Period		t_{HIGH}	3.00 V or above	24	—	ns	Figure 2.92
				1.65 to 1.95 V	27	—		
			t_{DIG_H} *2	3.00 V or above	32	—	ns	Figure 2.92
				1.65 to 1.95 V	35	—		
	Clock in to Data Out for Slave		t_{SCO}	3.00 V or above	—	12	ns	Figure 2.97
				1.65 to 1.95 V	—	12		
	SCL Clock Rise Time		t_{CR}	3.00 V or above	—	150 × 1 / f_{SCL} (capped at 60)	ns	Figure 2.92
				1.65 to 1.95 V	—	150 × 1 / f_{SCL} (capped at 60)		
	SCL Clock Fall Time		t_{CF}	3.00 V or above	—	150 × 1 / f_{SCL} (capped at 60)	ns	Figure 2.92
				1.65 to 1.95 V	—	150 × 1 / f_{SCL} (capped at 60)		
	SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4*5	3.00 V or above	t_{CR} + 3 and t_{CF} + 3	—	—	Figure 2.96
				1.65 to 1.95 V	t_{CR} + 3 and t_{CF} + 3	—		
		Slave	t_{HD_PP} *5	3.00 V or above	0	—	—	Figure 2.96
				1.65 to 1.95 V	0	—		
	SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	3.00 V or above	12	N/A	ns	Figure 2.98
				1.65 to 1.95 V	18	N/A		
	Clock After Repeated START (Sr)		t_{CASr}	3.00 V or above	t_{CASmin}	N/A	ns	Figure 2.100
				1.65 to 1.95 V	t_{CASmin}	N/A		
	Clock Before Repeated START (Sr)		t_{CBSr}	3.00 V or above	t_{CASmin} / 2	N/A	ns	Figure 2.100
				1.65 to 1.95 V	t_{CASmin} / 2	N/A		
	Capacitive Load per Bus Line (SDA/SCL)		C_b	3.00 V or above	—	50	pF	—
				1.65 to 1.95 V	—	50		

Note 1. $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH}.
Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I^2C Devices do not interpret I3C signaling as valid I^2C signaling.
Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.
Note 5. In SDR Mode the Hold time parameter is referred to as t_{HD_SDR}, and in DDR Mode it is referred to as t_{HD_DDR}.

Table 2.72 I3C timing (Push-Pull Timing Parameters for HDR-TSP and HDR-TSL Modes)

Setting of the I3C_SCL0, I3C_SDA0 pins are not required with the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
I3C Push-Pull Timing Parameters for HDR-TSP and HDR-TSL Modes	Edge-to-Edge Period	t_{EDGE} *1 *2	3.00 V or above	t_{DIG_H}	—	ns	Figure 2.102
			1.65 to 1.95 V	t_{DIG_H}	—		
	Allowed Difference Between Signals for 'Simultaneous' Change	t_{SKEW}	3.00 V or above	—	11	ns	
			1.65 to 1.95 V	—	11		
	Stable Condition Between Symbols	t_{EYE}	3.00 V or above	12	—	ns	
			1.65 to 1.95 V	12	—		
	Time Between Successive Symbols	t_{SYMBOL}	3.00 V or above	$t_{EDGE\ Min}$	—	ns	
			1.65 to 1.95 V	$t_{EDGE\ Min}$	—		
	Symbol Clock	t_{CLOCK}	3.00 V or above	$1 / f_{SCL}$ (Max)	—	—	
			1.65 to 1.95 V	$1 / f_{SCL}$ (Max)	—		

Note 1. Edges occur at the rate of $1 / (t_{EDGE} \times 2)$
Note 2. In a Mixed Bus, HDR-TSL shall respect the maximum $t_{DIG\_H\_MIXED}$ shown in Figure 2.95.

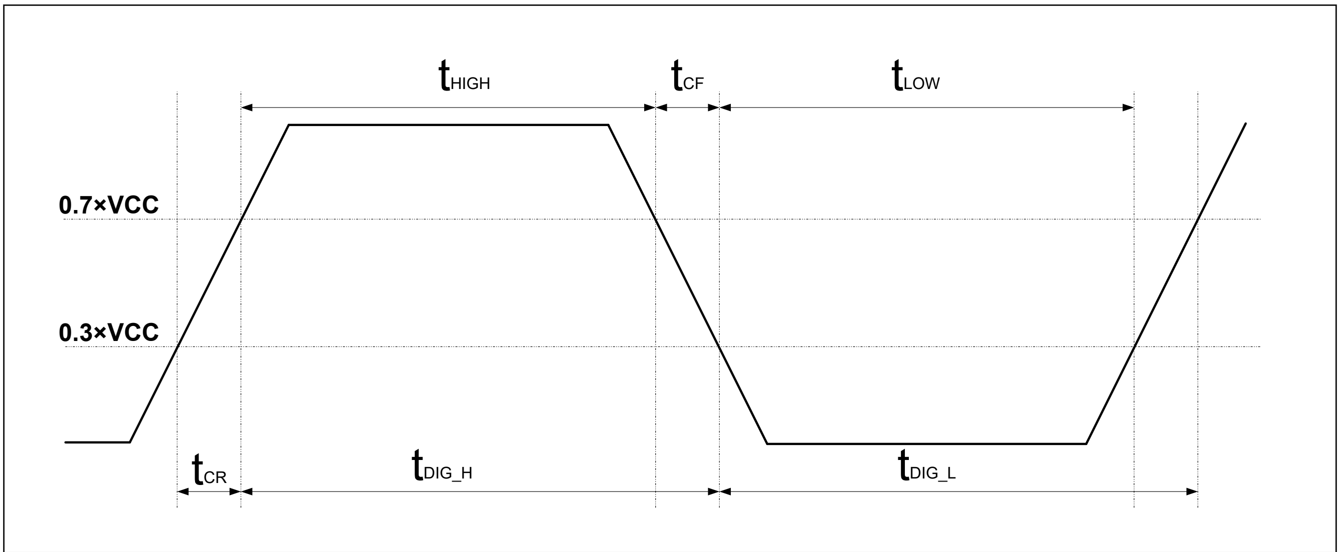
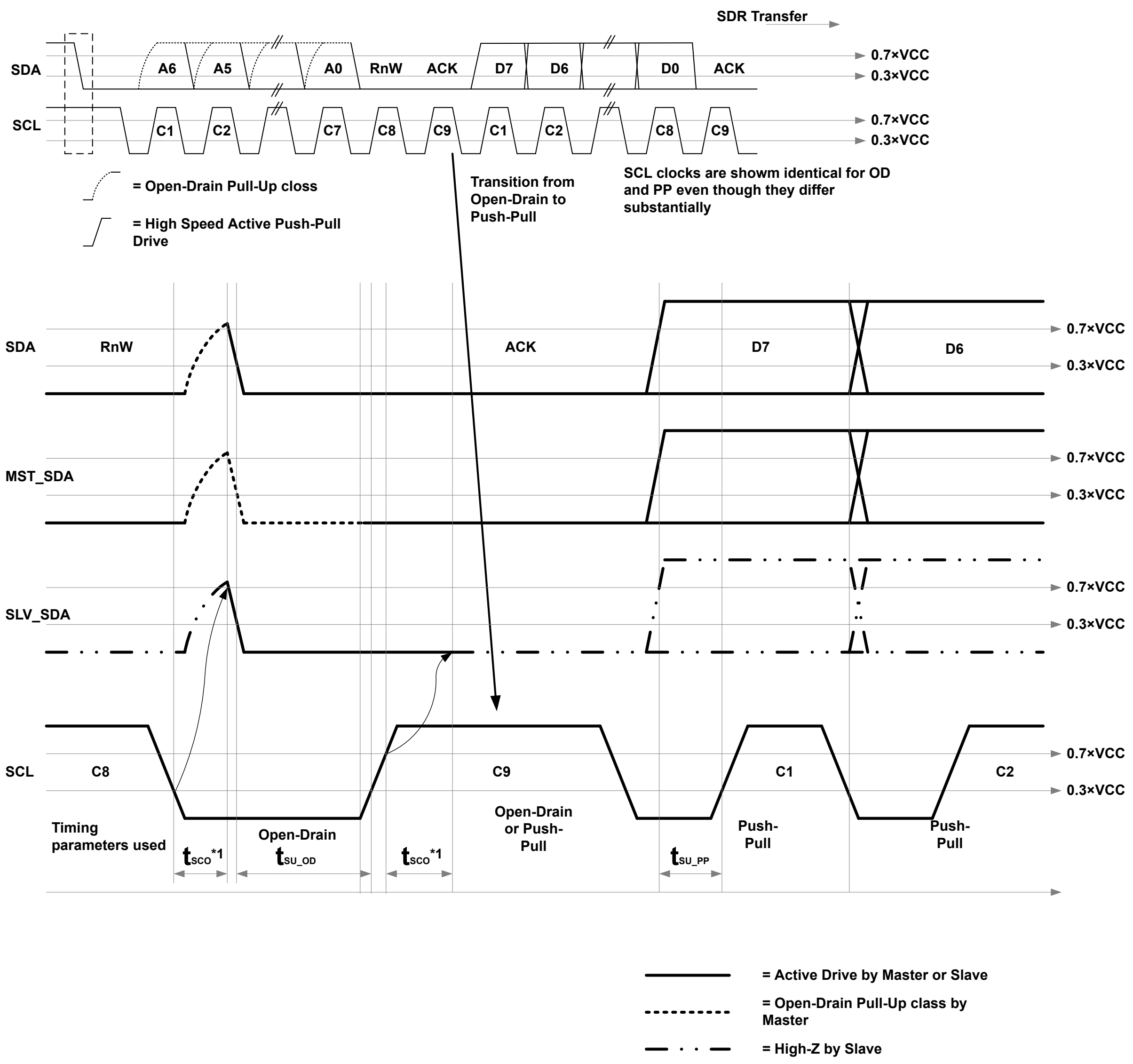


Figure 2.92 t_{DIG_H} and t_{DIG_L}



Note: Open-Drain: Master releases SDA after a suitable delay from SCL edges
Push-Pull: Master drives SDA after a suitable delay from SCL edges

Note 1. t_{SCO} is depicted for informative purposes only

Figure 2.93 I3C Data Transfer – ACK by Slave

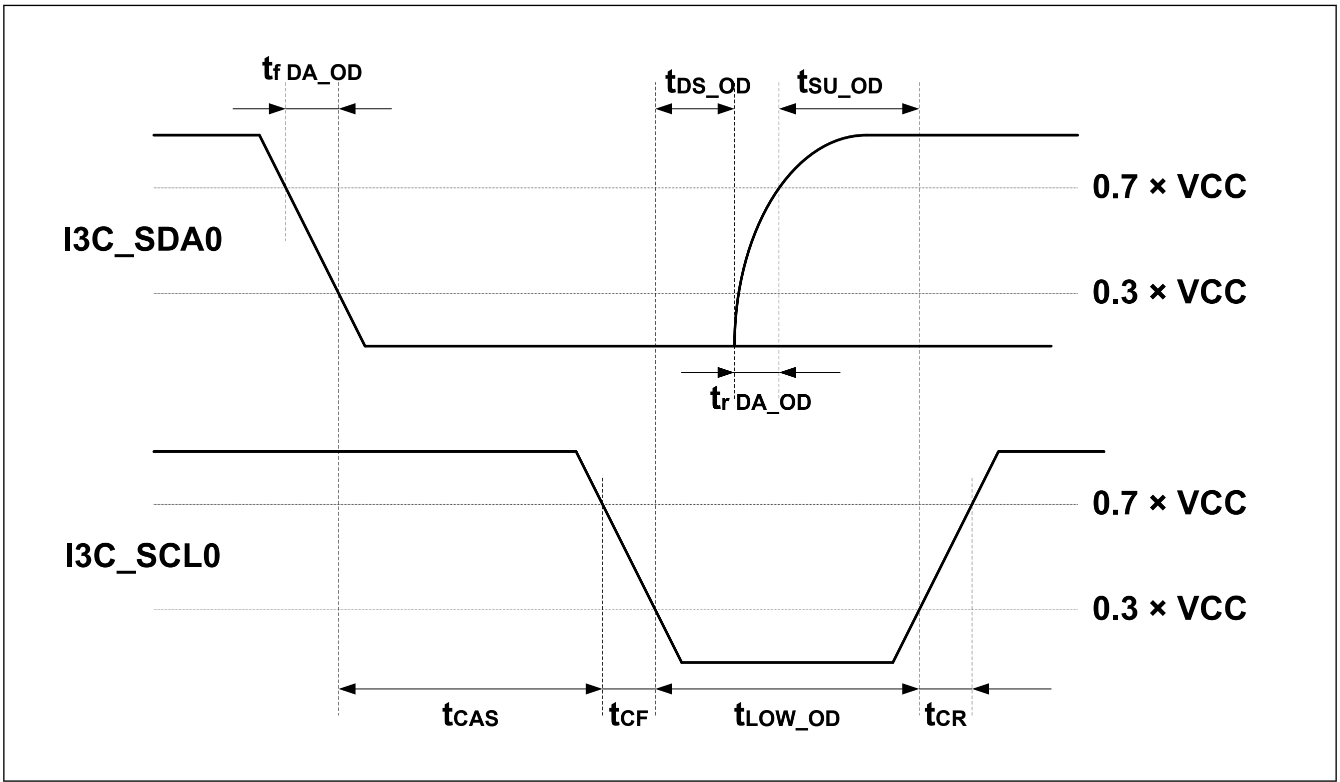


Figure 2.94 I3C START condition Timing

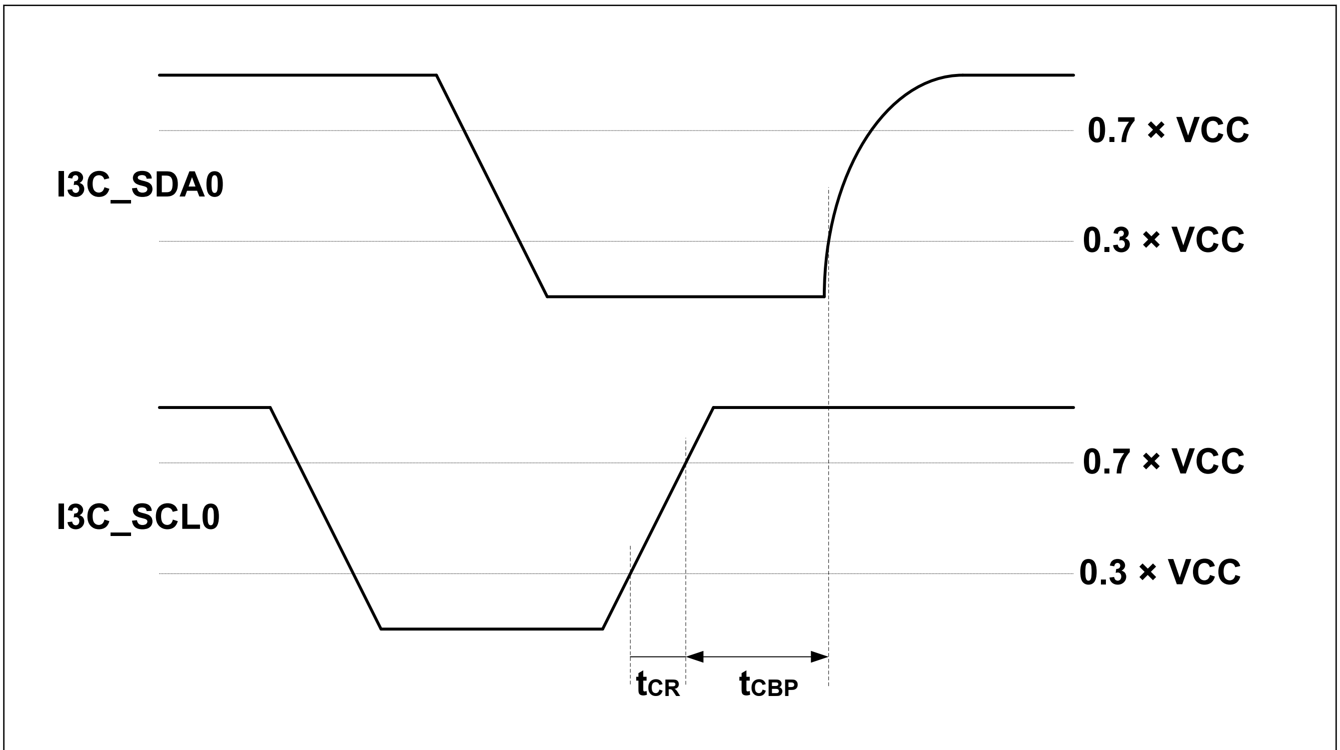


Figure 2.95 I3C STOP condition Timing

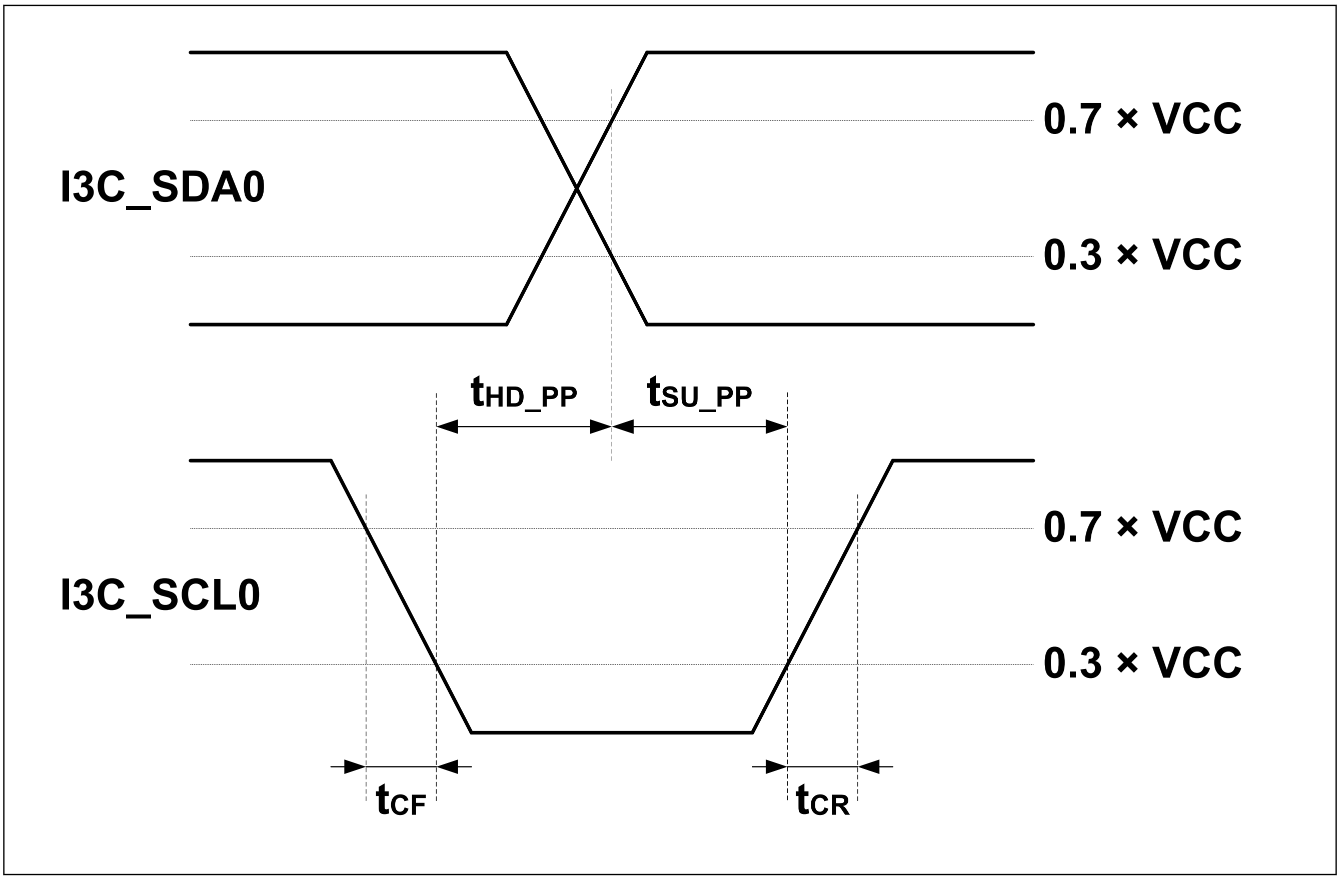


Figure 2.96 I3C Master Out Timing

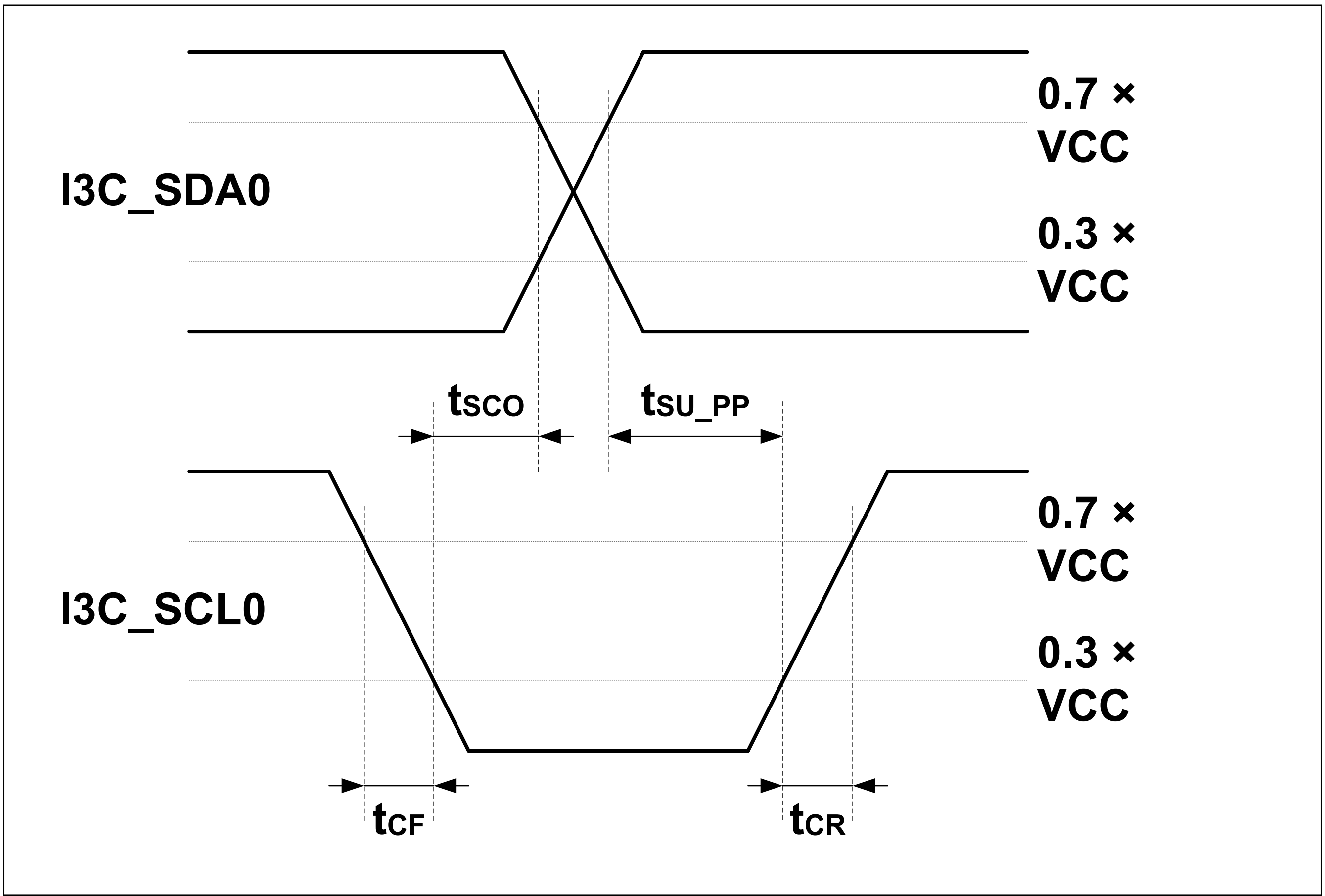


Figure 2.97 I3C Slave Out Timing

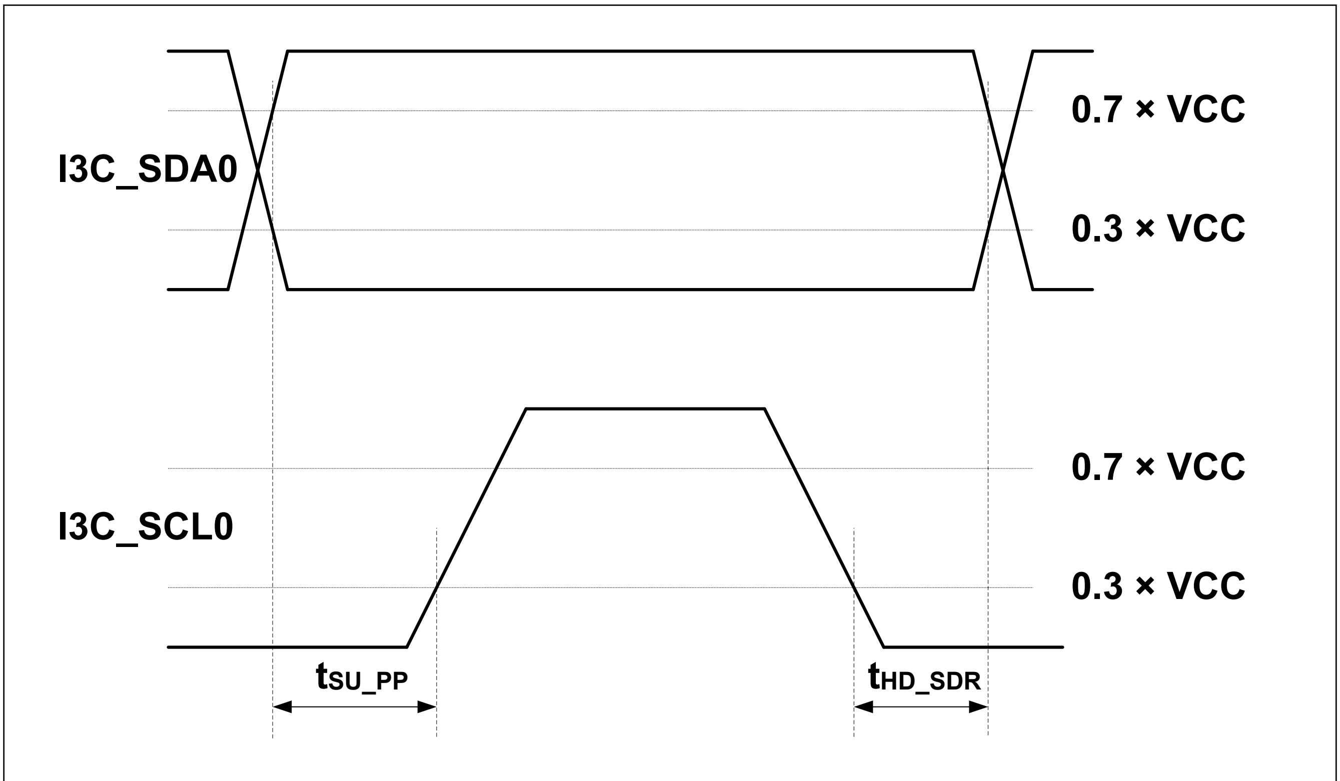


Figure 2.98 Master SDR Timing

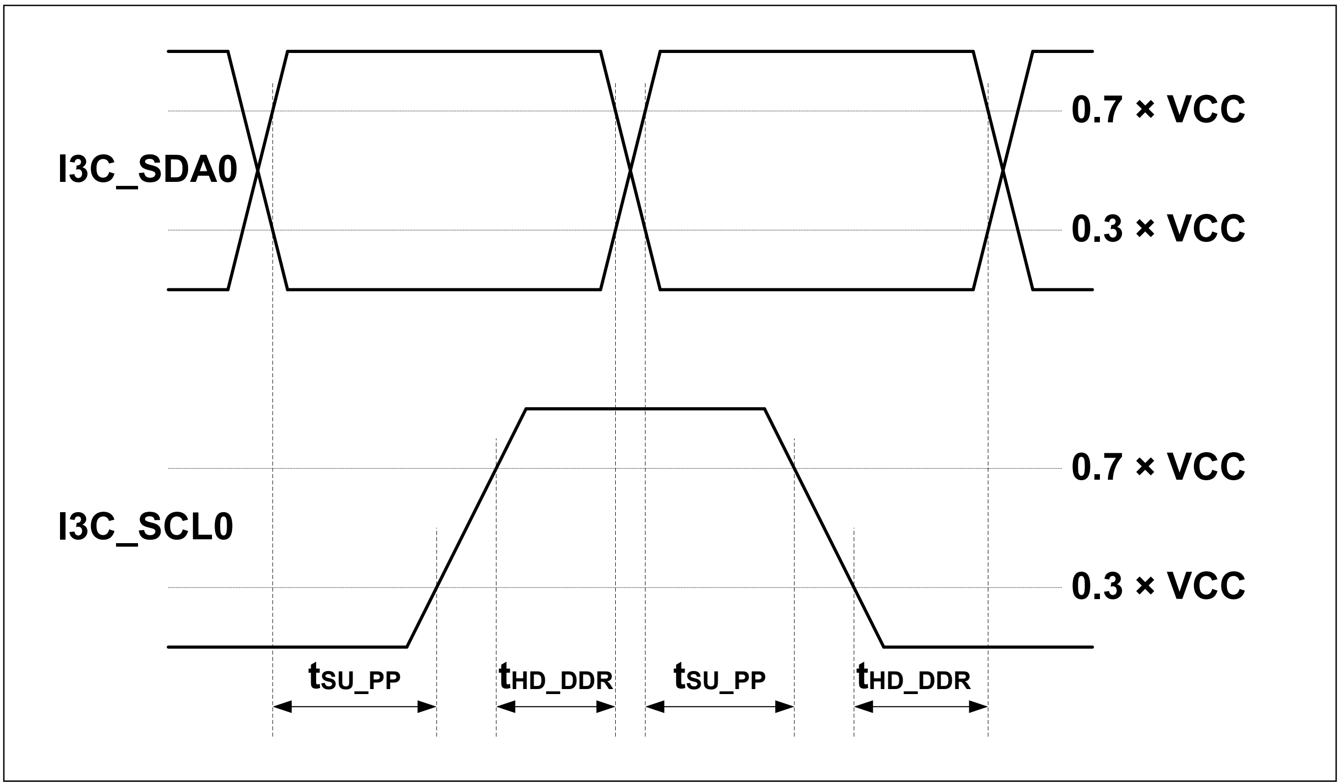
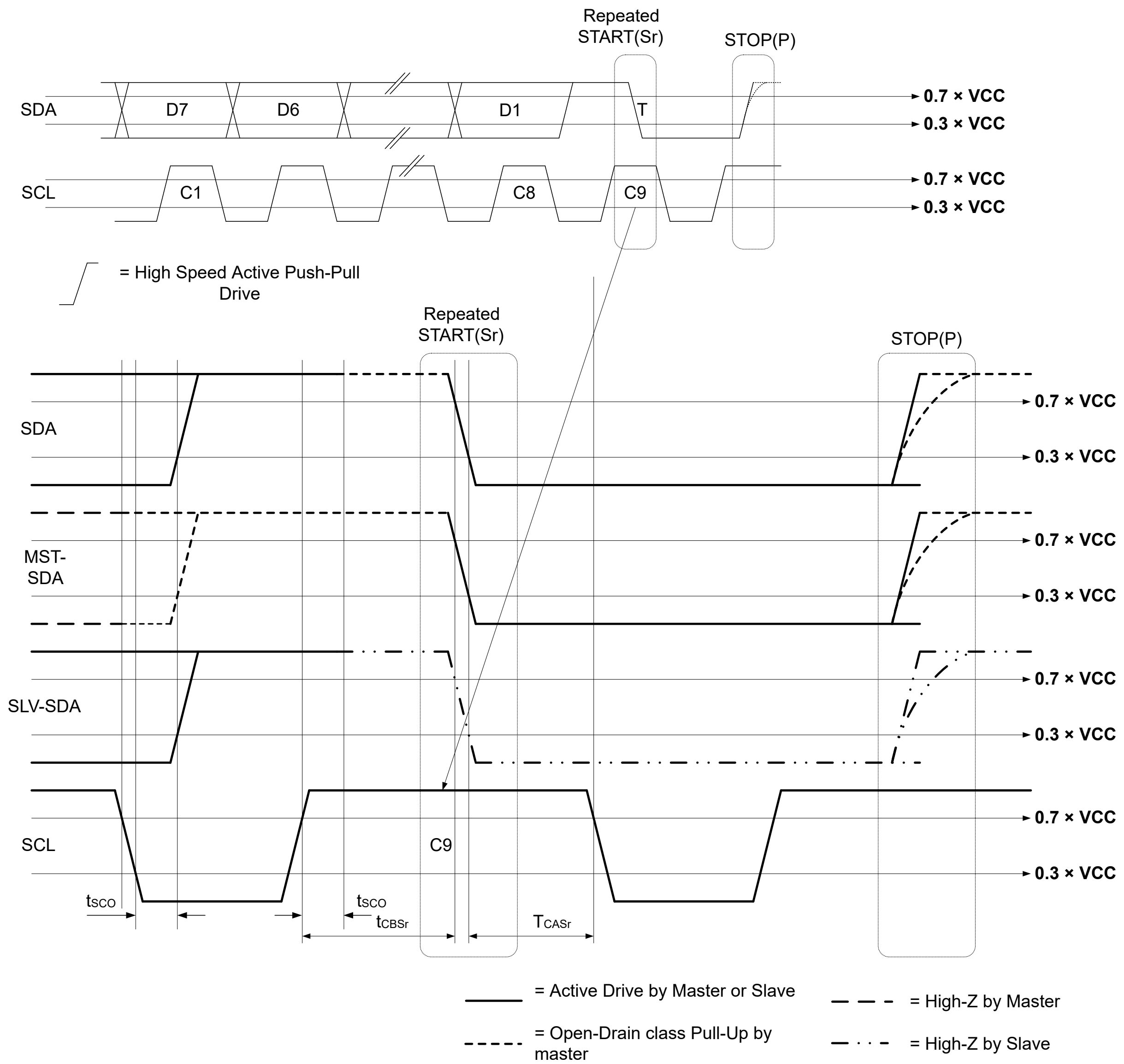


Figure 2.99 Master DDR Timing



Note: Sr immediately followed by P is illegal for I2C devices, however many devices are not adversely affected by it. The condition is not illegal for I3C devices.

Figure 2.100 T-Bit When Master Ends Read with Repeated START and STOP

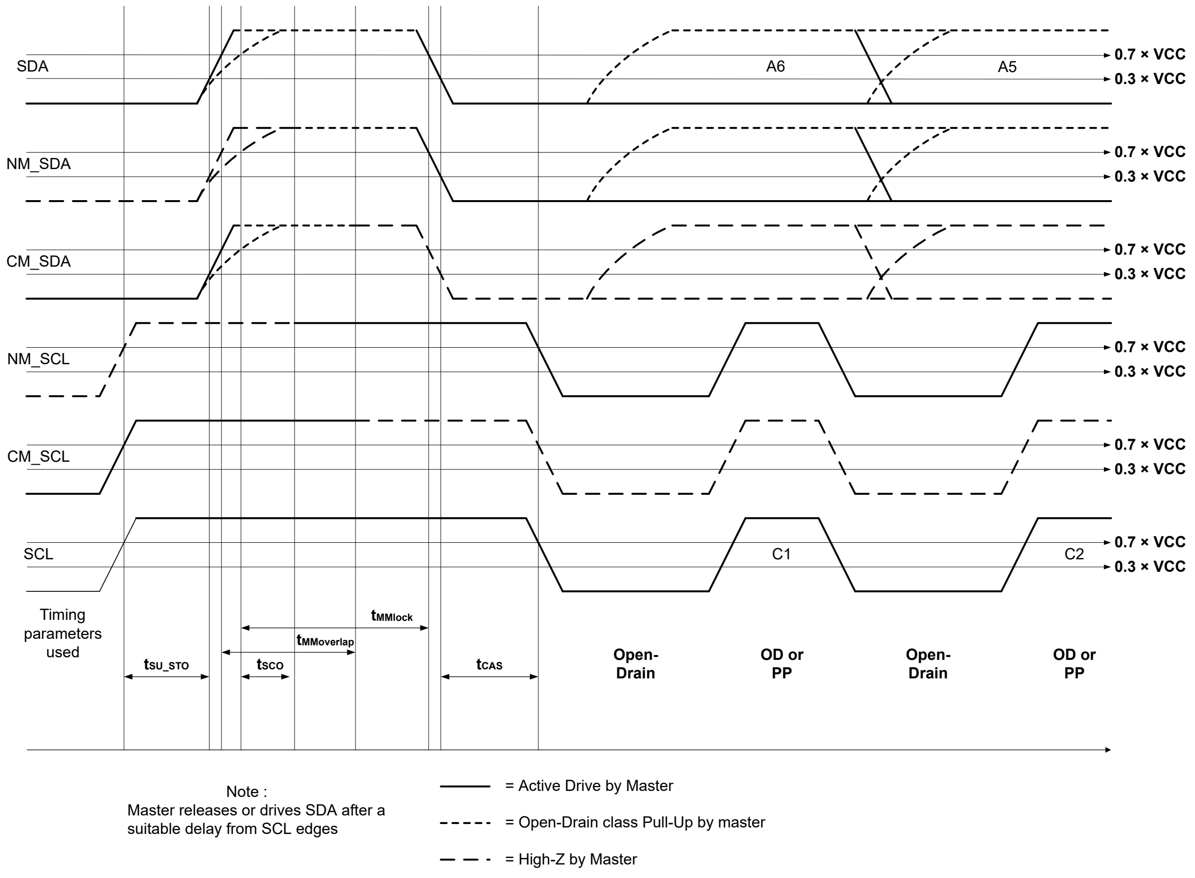
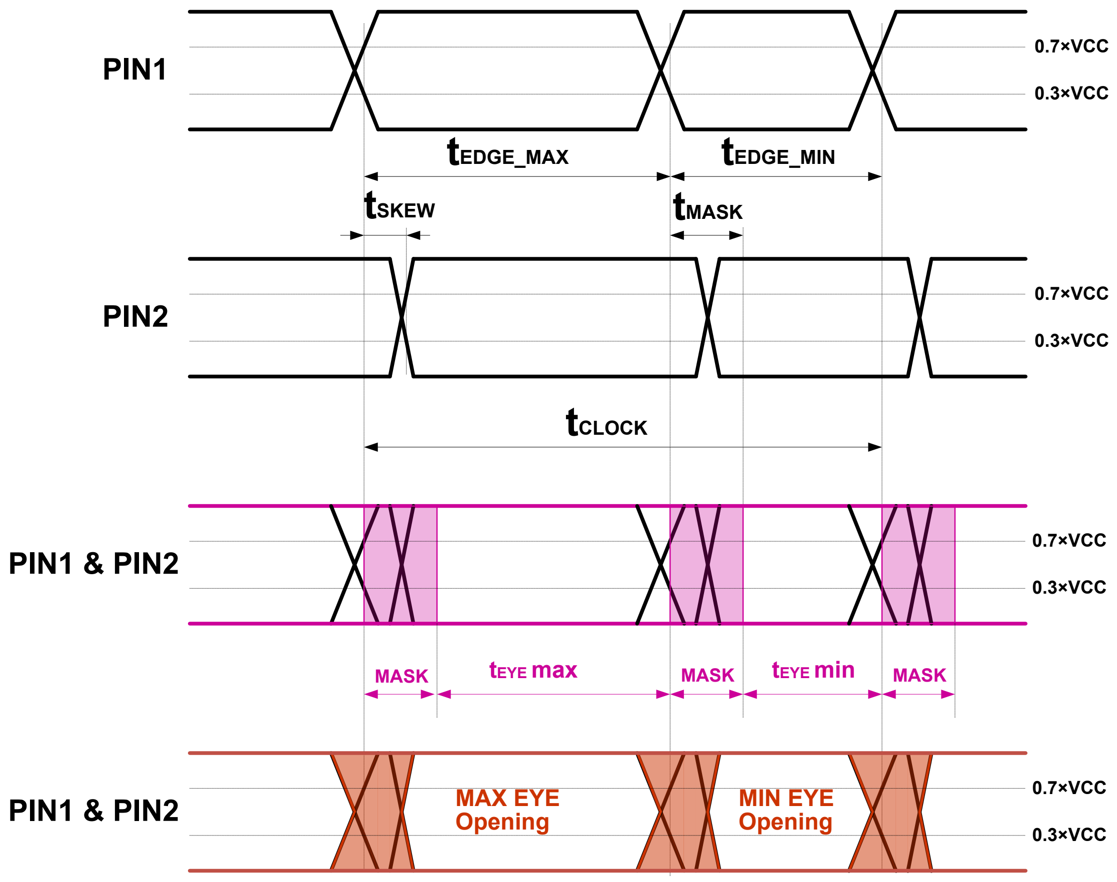


Figure 2.101 Master to Master Bus Handoff



Design Conditions

1. The The differences of load magnitude and drive strength between the SDA and SCL lines result in different slopes, as shown
2. MASK period ≧ MAX t_{SKEW} + MAX rise/fall time between 0.3 × V_{DD} and 0.7 × V_{DD}, respectively, decreased by the time crossing the hysteresis window.

Simplifying Assumptions

1. t_{SKEW} is the same for both edges
2. Base CLOCK (e.g. 12.5MHz) is asymmetrical
3. Falling edges are equal rising edges
4. The MASK is shown as starting, from the last possible moment, whereas in reality it could be shifted left (towards the start point) delayed by the hysteresis window

Figure 2.102 Ternary Protocol Timing

2.3.14 SD/MMC Host Interface Timing

Table 2.73 SD/MMC Host Interface signal timing

Conditions:
High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins:
SD0CLK_A, SD0CLK_B, SD0CLK_C, SD1CLK_A, SD1CLK_B
For other pins, high drive output is selected in the Port Drive Capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Parameter	Symbol	VCC/VCC2	Min	Max	Unit	Test conditions
SDCLK clock cycle	t_{SDCYC}	2.70 V or above	20	—	ns	Figure 2.103
		1.70 to1.95 V*1	20	—		
		1.70 to1.95 V	40	—		
SDCLK clock high pulse width	t_{SDWH}	2.70 V or above	6.5	—	ns	
		1.70 to1.95 V*1	6.5	—		
		1.70 to1.95 V	13.0	—		
SDCLK clock low pulse width	t_{SDWL}	2.70 V or above	6.5	—	ns	
		1.70 to1.95 V*1	6.5	—		
		1.70 to1.95 V	13.0	—		
SDCLK clock rise time	t_{SDLH}	2.70 V or above	—	3	ns	
		1.70 to1.95 V*1	—	4		
		1.70 to1.95 V	—	8		
SDCLK clock fall time	t_{SDHL}	2.70 V or above	—	3	ns	
		1.70 to1.95 V*1	—	4		
		1.70 to1.95 V	—	8		
SDCMD/SDDAT output data delay	t_{SDODLY}	2.70 V or above	–7.0	4.0	ns	
		1.70 to1.95 V*1	–7.0	7.0		
		1.70 to1.95 V	–15.0	15.0		
SDCMD/SDDAT input data setup	t_{SDIS}	2.70 V or above	4.5	—	ns	
		1.70 to1.95 V*1	4.5	—		
		1.70 to1.95 V	20.0	—		
SDCMD/SDDAT input data hold	t_{SDIH}	2.70 V or above	1.5	—	ns	
		1.70 to1.95 V	1.5	—		

Note: Must use pins that have a letter appended to their name, for instance “_A”, “_B”, to indicate group membership. For the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.
Note: If SD1DAT4_A to SD1DAT7_A are used, characteristics above is guaranteed only when VCC = VCC2.
Note 1. Only supported for Ch0 group B ("SD0*_B") and Ch1 group A ("SD1*_A")

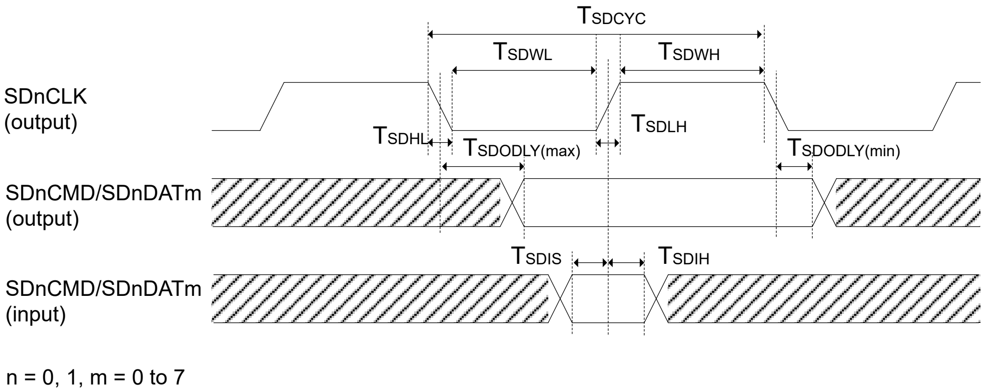


Figure 2.103 SD/MMC Host Interface signal timing

2.3.15 CANFD Timing

Table 2.74 CANFD interface timing

Conditions: Low drive output is selected when VCC is 2.70V or above. Middle drive output is selected when VCC is 1.62V or above.

Parameter	Symbol	VCC/VCC2	Min	Max	Unit	Test conditions
Internal delay time	t_{node}	2.70 V or above	—	50	ns	Figure 2.104
		1.62 V or above	—	50		
Transmission rate		2.70 V or above	—	8	Mbps	
		1.62 V or above	—	8		

Note: Internal delay time (t_{node}) = Internal transfer delay time (t_{output}) + Internal receive delay time (t_{input})

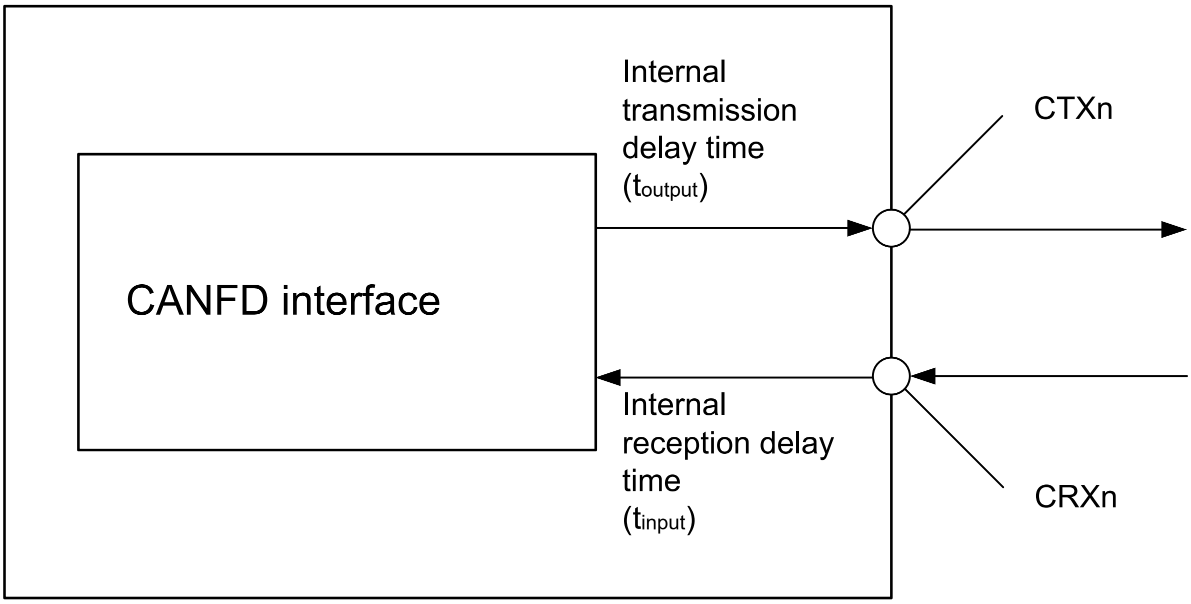


Figure 2.104 CANFD interface condition

2.3.16 PDG Timing

Table 2.75 PDG Timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	—	300	MHz	—
Resolution	—	48.8	—	ps	GTDLYCR.FRANGE [1:0] = 00 and GPTCLK = 160 MHz
	—	52.1	—	ps	GTDLYCR.FRANGE [1:0] = 01 and GPTCLK = 300 MHz
DNL*1	—	±2.0	—	LSB	—

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

2.3.17 ESWM Timing

Table 2.76 ESWM timing (RMII)

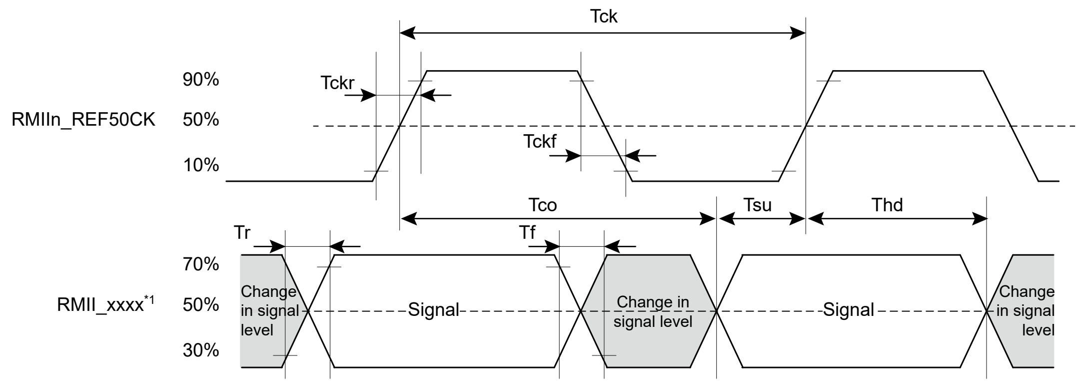
Conditions:

1. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ETn_MDC, ETn_MDIO.
2. The drive capacity selection and voltage range for pins other than ETn_MDC, ETn_MDIO.

- RMII use: High drive select, VCC = 2.7 to 3.6

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ESWM (RMII)	RMIIn_REF50CK cycle time	Tck	2.70V or above	20	—	ns	Figure 2.106
	RMIIn_REF50CK frequency, typical 50 MHz	—		—	50 + 100 ppm	MHz	
	RMIIn_REF50CK duty	—		35	65	%	
	RMIIn_REF50CK rise/fall time	Tckr/ckf		0.5	3.5	ns	
	RMIIn_xxxx*1 output delay	Tco		2.5	12	ns	
	RMIIn_xxxx*2 setup time	Tsu		3	—	ns	
	RMIIn_xxxx*2 hold time	Thd		1	—	ns	
	RMIIn_xxxx*1 *2 rise/fall time	Tr/Tf		0.5	4	ns	

Note 1. RMIIn_TX_EN, RMIIn_TXD1, RMIIn_TXD0.
Note 2. RMIIn_CRS_DV, RMIIn_RXD1, RMIIn_RXD0, RMIIn_RX_ER.



Note 1. RMIIn_TX_EN, RMIIn_TXD1, RMIIn_TXD0, RMIIn_CRS_DV, RMIIn_RXD1, RMIIn_RXD0, RMIIn_RX_ER

Figure 2.106 RMIIn_REF50CK and RMII signal timing

Table 2.77 ESWM timing (MII)

Conditions:

1. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ETn_MDC, ETn_MDIO.
2. The drive capacity selection and voltage range for pins other than ETn_MDC, ETn_MDIO.

- MII use only: Middle drive select, VCC = 2.7 to 3.6
- GMII and MII use: RGMII 2.50 V drive select, VCC = 2.3 to 2.7
- GMII and MII use: RGMII 3.30 V drive select, VCC = 3.0 to 3.6

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ESWM (MII)	ETn_TX_CLK cycle time	t_{Tcyc}	2.30 V or above	40	—	ns	—
	ETn_TX_EN output delay	t_{TENd}		1	20	ns	Figure 2.107
	ETn_ETXD0 to ETn_ETXD3 output delay	t_{MTDd}		1	20	ns	
	ETn_RX_CLK cycle time	t_{TRcyc}		40	—	ns	—
	ETn_RX_DV setup time	t_{RDVs}		10	—	ns	Figure 2.108
	ETn_RX_DV hold time	t_{RDVh}		10	—	ns	
	ETn_ERXD0 to ETn_ERXD3 setup time	t_{MRDs}		10	—	ns	
	ETn_ERXD0 to ETn_ERXD3 hold time	t_{MRDh}		10	—	ns	
	ETn_RX_ER setup time	t_{RERs}		10	—	ns	
	ETn_RX_ER hold time	t_{RESh}		10	—	ns	

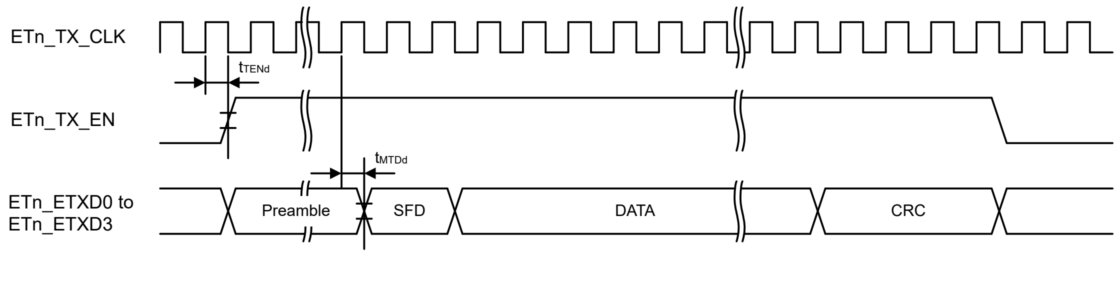


Figure 2.107 MII transmission timing in normal operation

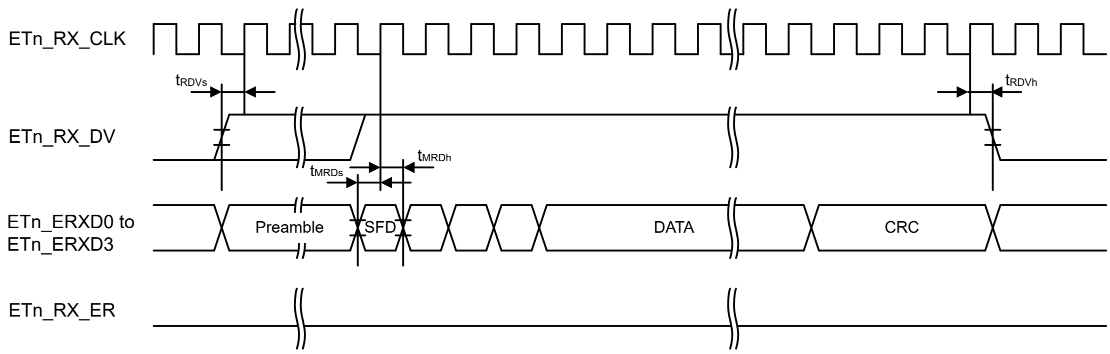


Figure 2.108 MII reception timing in normal operation

Table 2.78 ESWM timing (GMII)

Conditions:

1. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ETn_MDC, ETn_MDIO.
2. The drive capacity selection and voltage range for pins other than ETn_MDC, ETn_MDIO.

- GMII use at 2.5 V: RGMII 2.50V drive select, VCC = 2.3 to 2.7
- GMII use at 3.3 V: RGMII 3.30V drive select, VCC = 3.0 to 3.6

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ESWM (GMII)	ETn_GTX_CLK Frequency	t_{FREQ}	2.30 V to 3.60 V	125 - 100 ppm	125 + 100 ppm	MHz	Figure 2.109 Figure 2.110
	ETn_GTX_CLK Period	t_{PERIOD}		7.5	8.5	ns	
	ETn_RX_CLK Period	t_{PERIOD}		7.5	—	ns	
	ETn_GTX_CLK, ETn_RX_CLK Time High	t_{HIGH}		2.5	—	ns	
	ETn_GTX_CLK, ETn_RX_CLK Time Low	t_{LOW}		2.5	—	ns	
	ETn_GTX_CLK, ETn_RX_CLK Rise Time	t_R		—	1	ns	
	ETn_GTX_CLK, ETn_RX_CLK Fall Time	t_F		—	1	ns	
	Magnitude of ETn_GTX_CLK, ETn_RX_CLK Slew Rate (rising)*1	—		0.6	—	V/ns	
	Magnitude of ETn_GTX_CLK, ETn_RX_CLK Slew Rate (falling)*1	—		0.6	—	V/ns	
	ETn_TXD, ETn_TX_EN, ETn_TX_ER Setup to ↑ETn_GTX_CLK and ETn_RXD, ETn_RX_DV, ETn_RX_ER Setup to ↑ ETn_RX_CLK	t_{SETUP}		2.5	—	ns	
	ETn_TXD, ETn_TX_EN, ETn_TX_ER Hold from ↑ ETn_GTX_CLK and ETn_RXD, ETn_RX_DV, ETn_RX_ER Hold from ↑ ETn_RX_CLK	t_{HOLD}		0.5	—	ns	
	ETn_TXD, ETn_TX_EN, ETn_TX_ER Setup to ↑ ETn_GTX_CLK and ETn_RXD, ETn_RX_DV, ETn_RX_ER Setup to ↑ ETn_RX_CLK	t_{SETUP}(RCVR)		2	—	ns	
	TXD, TX_EN, TX_ER, ETn_TX_ER Hold from ↑ GTX_CLK and RXD, RX_DV, RX_ER Hold from ↑ RX_CLK	t_{HOLD}(RCVR)		0	—	ns	

Note 1. Clock Skew rate is the instantaneous rate of change of the clock potential with respect to time (dV/dt), not an average value over the entire rise or fall time interval. Conformance with this specification guarantees that the clock signals will rise and fall monotonically through the switching region.

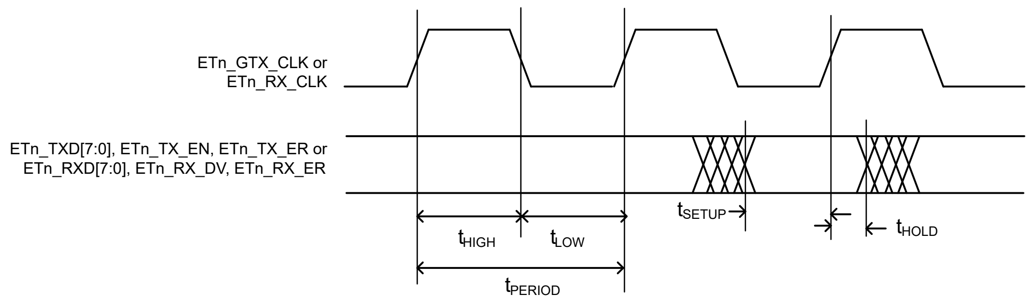


Figure 2.109 GMII timing

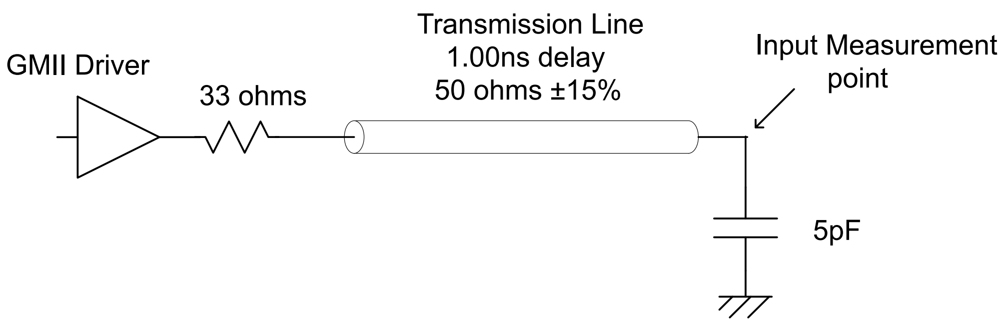


Figure 2.110 GMII output timing measurement conditions

Table 2.79 ESWM timing (RGMII)

Conditions:

1. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: ETn_MDC, ETn_MDIO.
2. The drive capacity selection and voltage range for pins other than ETn_MDC, ETn_MDIO.

- RGMII use at 2.5 V: RGMII 2.50V drive select, VCC = 2.3 to 2.7
- RGMII use at 3.3 V: RGMII 3.30V drive select, VCC = 3.0 to 3.6

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ESWM (RGMII)	Data to Clock output Skew (at Transmitter)*1	T_{skewT}	2.30 V to 3.60 V	−500	500	ps	Figure 2.111 Figure 2.112 Figure 2.113
	Data to Clock input Skew (at Receiver)*1	T_{skewR}		1	2.6	ns	
	Data to Clock output Setup (at Transmitter-integrated delay)	T_{setupT}		1.2	—	ns	
	Clock to Data output Hold (at Transmitter–integrated delay)	T_{holdT}		1.2	—	ns	
	Data to Clock input Setup (at Receiver–integrated delay)	T_{setupR}		1	—	ns	
	Data to Clock input Hold (at Receiver–integrated delay)	T_{holdR}		1	—	ns	
	Clock Cycle Duration*2	T_{cyc}		7.2	8.8	ns	
	Duty Cycle for Gigabit*3	Duty_G		45	55	%	
	Duty Cycle for 10/100T*3	Duty_T		40	60	%	
	Rise / Fall Time (20-80%)	T_r / T_f		—	0.75	ns	

Note 1. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal.
Note 2. For 10Mbps and 100Mbps, Tcyc will scale to 400ns+-40ns and 40ns+-4ns respectively.
Note 3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

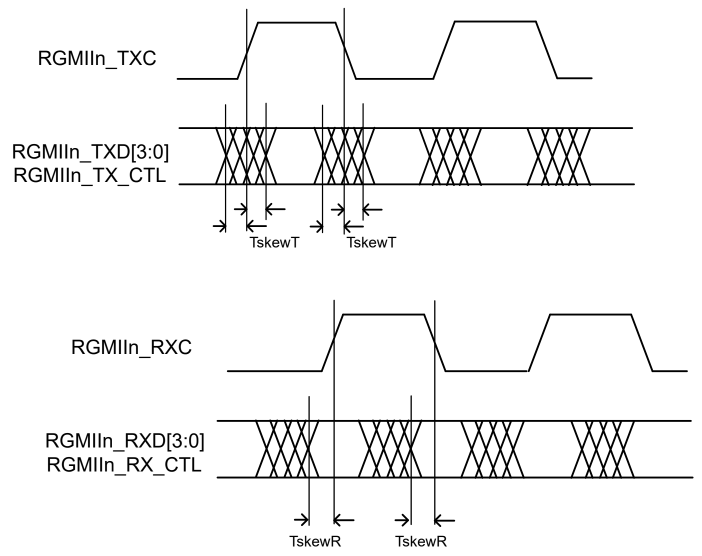


Figure 2.111 RGMII timing

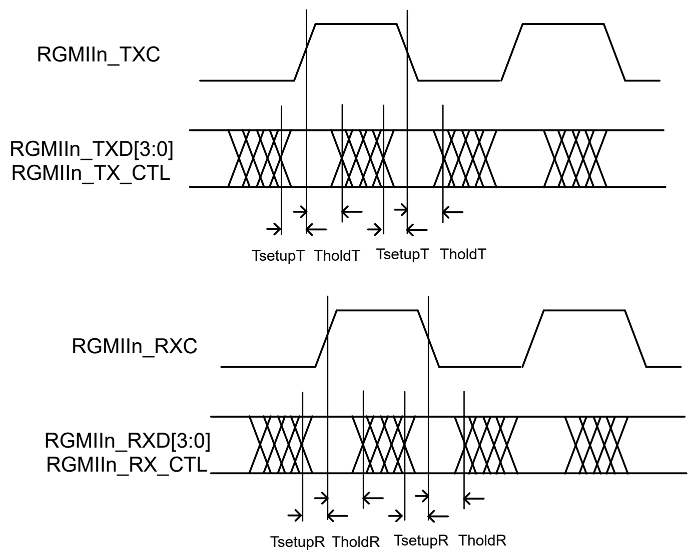


Figure 2.112 RGMII timing (RGMII-ID)

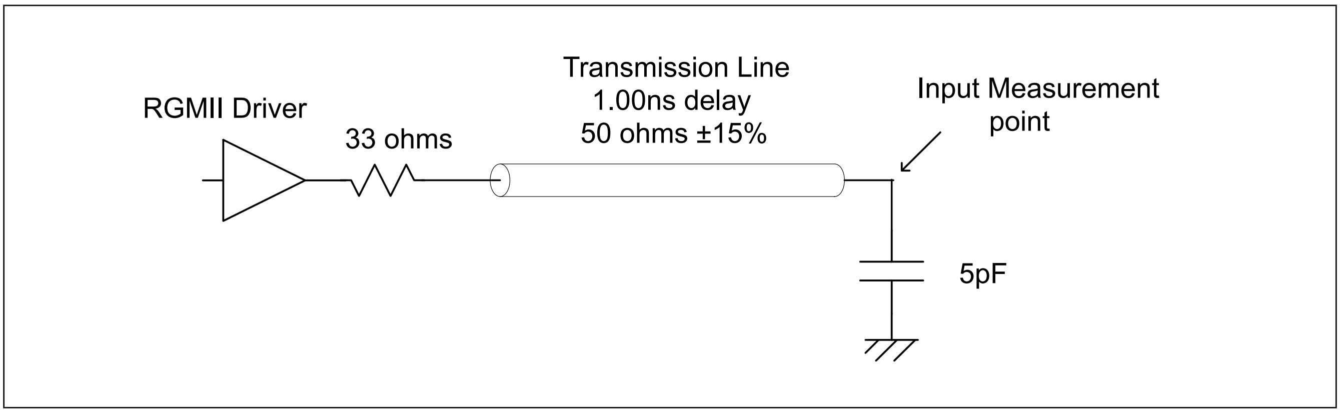


Figure 2.113 RGMII output timing measurement conditions

Table 2.80 ESWM timing (ETn_MDIO, ETn_MDC)

Conditions:

1. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ESWM (ETn_MDIO, ETn_MDC)	ETHn_MDC output cycle	t_{MDC}	2.70 V or above	80	—	ns	Figure 2.114
			2.30 V or above	160	—	ns	
	ETHn_MDIO setup time (relative to ETHn_MDC↑)	t_{SMDIO}	2.70 V or above	20	—	ns	
			2.30 V or above	40	—	ns	
	ETHn_MDIO hold time (relative to ETHn_MDC↑)	t_{HMDIO}	2.70 V or above	0	—	ns	
			2.30 V or above	0	—	ns	
	ETHn_MDIO output delay time (relative to ETHn_MDC↑)	t_{DMDIO}	2.70 V or above	0	20	ns	
			2.30 V or above	0	40	ns	

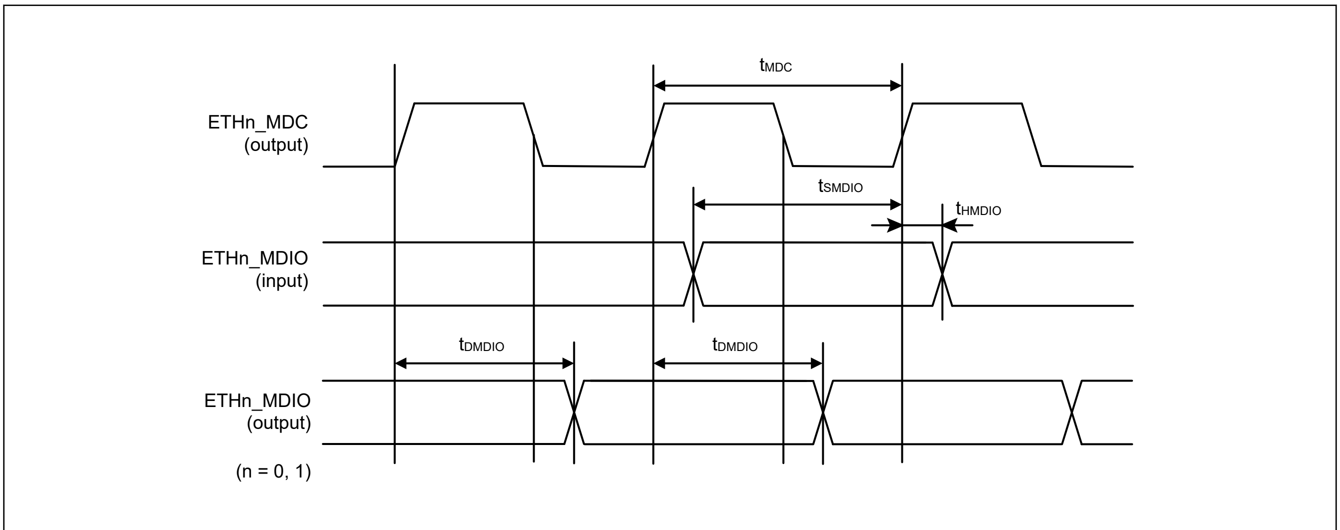


Figure 2.114 ETn_MDIO, ETn_MDC timing

2.3.18 ESC Timing

Table 2.81 ESC timing

Conditions:

1. Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register for the following pins: CAT0_MDC, CAT0_MDIO.
2. High drive output is selected in the Port Drive Capability bit in the PmnPFS register for pins other than CAT0_MDC, CAT0_MDIO.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
ESC (MII)	CATn_TX_CLK cycle time	t_{Tcyc}	2.70V or above	40	—	ns	
	CATn_TX_EN output delay time	t_{TENd}		1	25	ns	Figure 2.114
	CATn_ETXD0 to CATn_ETXD3 output delay time	t_{MTDd}		1	25	ns	
	CATn_RX_CLK cycle time	t_{TRcyc}		40	—	ns	
	CATn_RX_DV setup time	t_{RDVs}		10	—	ns	Figure 2.115
	CATn_RX_DV hold time	t_{RDVh}		10	—	ns	
	CATn_ERXD0 to CATn_ERXD3 setup time	t_{MRDs}		10	—	ns	
	CATn_ERXD0 to CATn_ERXD3 hold time	t_{MRDh}		10	—	ns	
	CATn_RX_ER setup time	t_{RERs}		10	—	ns	Figure 2.116
	CATn_RX_ER hold time	t_{RERh}		10	—	ns	
ESC (MDIO)	CAT0_MDIO setup time (CAT0_MDC↑)	t_{SMDIO}		60	—	ns	Figure 2.117
	CAT0_MDIO hold time (CAT0_MDC↑)	t_{HMDIO}		0	—	ns	
	CAT0_MDIO output delay time (CAT0_MDC↓)	t_{DMDIO}		0	30	ns	

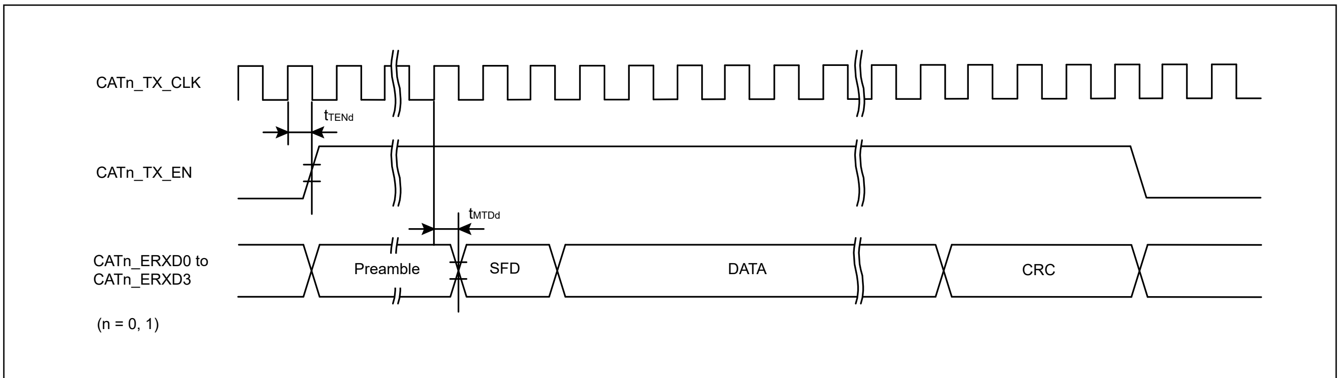


Figure 2.114 MII Transmission Timing (Normal Operation)

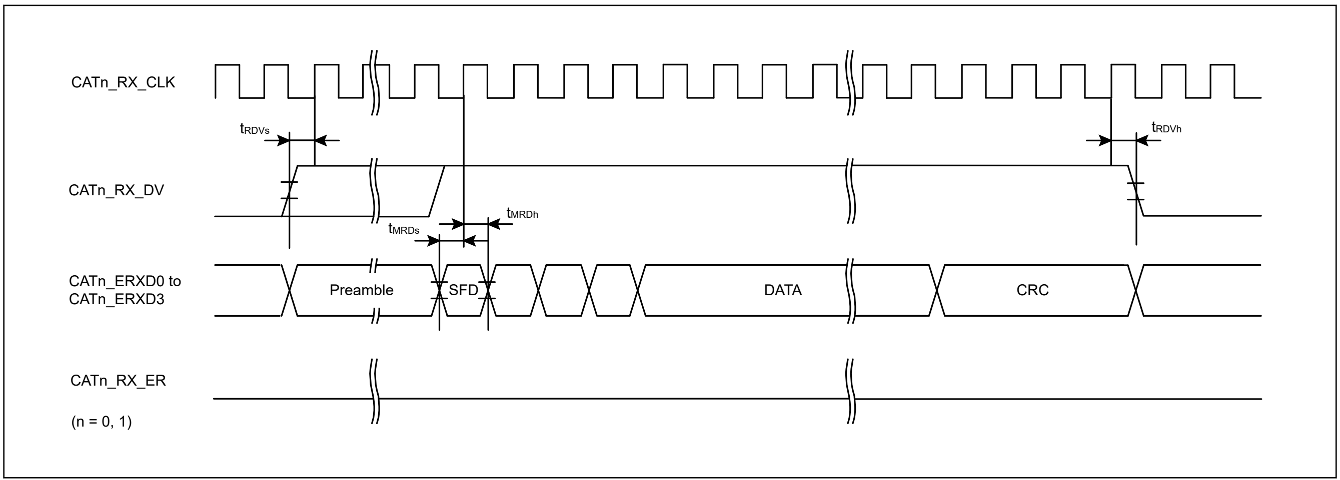


Figure 2.115 MII Reception Timing (Normal Operation)

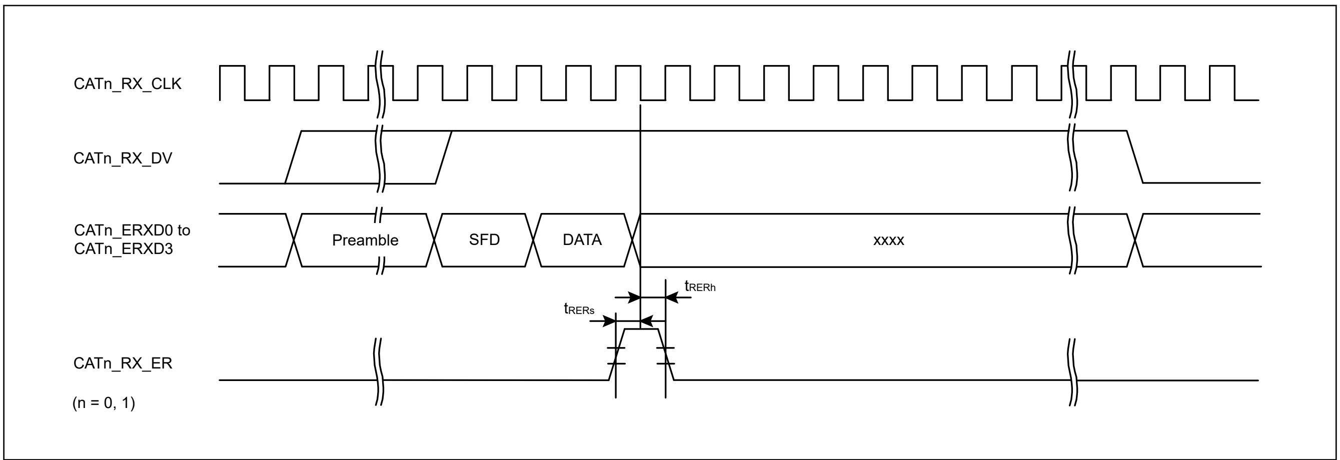


Figure 2.116 MII Reception Timing (Error Occurrence)

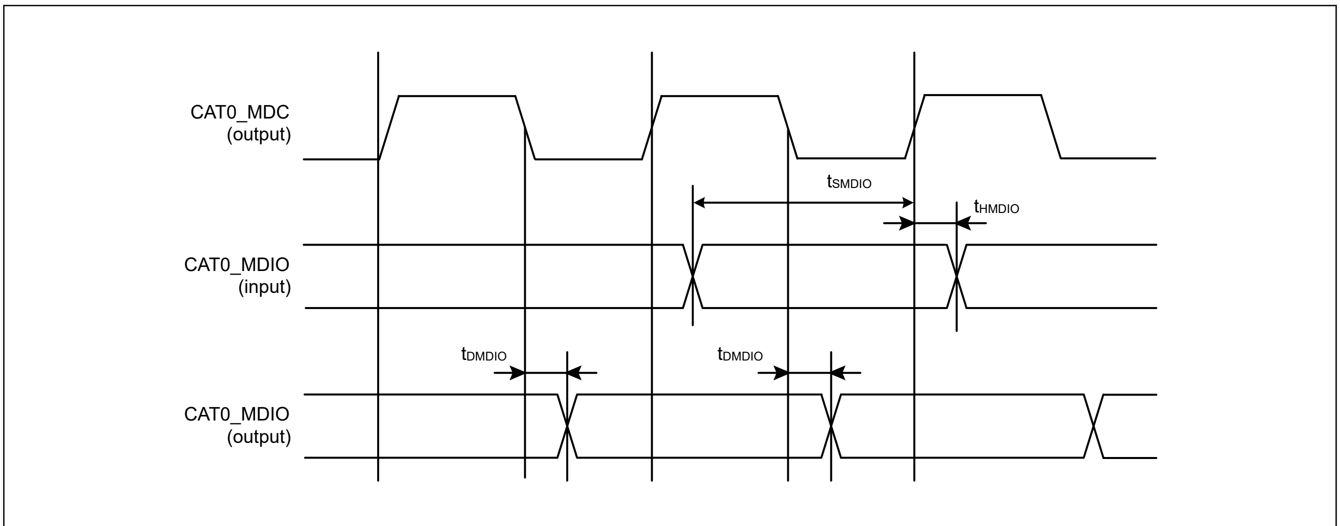


Figure 2.117 Timing of Serial Management Access

2.3.19 DSMIF Timing

Table 2.82 DSMIF timing

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter		Symbol	VCC	Min	Max	Unit	Test conditions
Clock period	Master	t_{DScyc}	2.70 V or above	40	200	ns	Figure 2.118
			1.62 V or above	80	200		
	Slave		2.70 V or above	40	200		
			1.62 V or above	40	200		
Clock high level pulse width	Master	t_{DSCKWH}	2.70 V or above	16	—	ns	
			1.62 V or above	32	—		
	Slave		2.70 V or above	16	—		
			1.62 V or above	16	—		
Clock low level pulse width	Master	t_{DSCKWL}	2.70 V or above	16	—	ns	
			1.62 V or above	32	—		
	Slave		2.70 V or above	16	—		
			1.62 V or above	16	—		
Setup time	Master	t_{SU}	2.70 V or above	15	—	ns	Figure 2.119 Figure 2.120
			1.62 V or above	30	—		
	Slave		2.70 V or above	10	—		
			1.62 V or above	10	—		
Hold time	Master	t_H	2.70 V or above	0	—	ns	
			1.62 V or above	0	—		
	Slave		2.70 V or above	10	—		
			1.62 V or above	10	—		

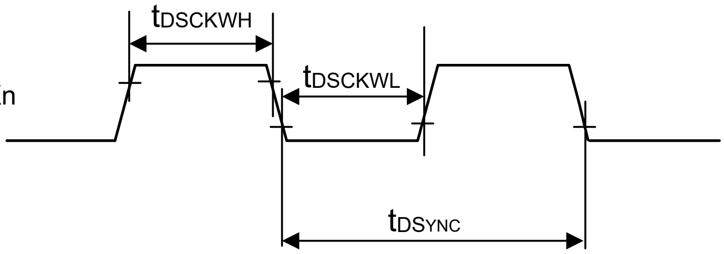


Figure 2.118 Timing of clock input / output

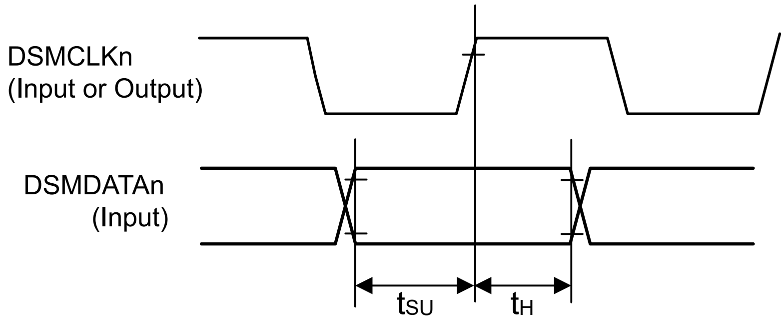


Figure 2.119 Receive Timing (Synchronized with the rise of DSMCLKn)

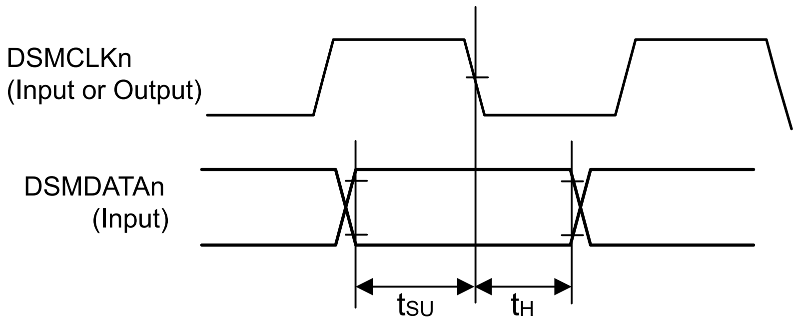


Figure 2.120 Receive Timing (Synchronized with the fall of DSMCLKn)

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.83 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—

Table 2.83 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (2 of 2)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.121
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

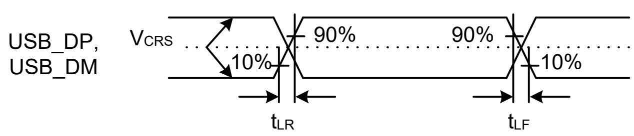


Figure 2.121 USB_DP and USB_DM output timing in low-speed mode

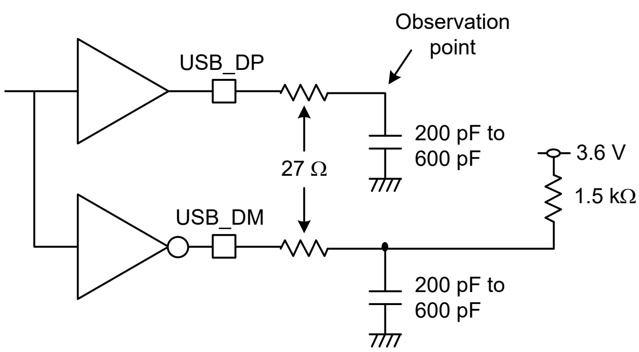


Figure 2.122 Test circuit in low-speed mode

Table 2.84 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (1 of 2)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	—	—	V	—
	Input low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	—	2.5	V	—

Table 2.84 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics) (2 of 2)

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, USBCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output characteristics	Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.123
	Rise time	t_{LR}	4	—	20	ns	
	Fall time	t_{LF}	4	—	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	—	1.575	kΩ	During idle state
			1.425	—	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	—	24.80	kΩ	—

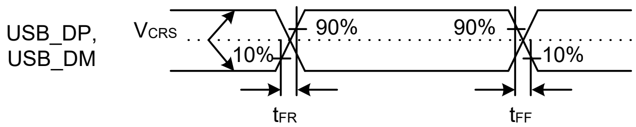


Figure 2.123 USB_DP and USB_DM output timing in full-speed mode

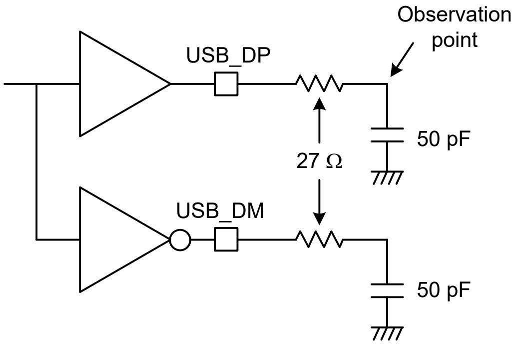


Figure 2.124 Test circuit in full-speed mode

2.5 ADC Characteristics

Table 2.85 A/D conversion characteristics (common) (1 of 3)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter	Min	Typ	Max	Unit	Test conditions
A/D conversion clock frequency (ADCLK)	25	50	60	MHz	AVCC: 2.7 to 3.63 V VCC: 2.7 to 3.63 V VREFH0/VREFH: 2.7 V to AVCC
Successive approximation time	100	—	200	ns	

Table 2.85 A/D conversion characteristics (common) (2 of 3)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
A/D sampling time (Normal mode)	Self-calibration				SAR mode	$1 \times t_{ADcyc} + 40$	—	—	ns	AVCC: 2.7 to 3.63 V VCC: 2.7 to 3.63 V VREFH0/VREFH: 2.7 V to AVCC tCmp=100ns
					Oversampling mode	$1 \times t_{ADcyc} + 40$	—	—	ns	
	Self-diagnosis				SAR mode	$1 \times t_{ADcyc} + 40$	—	—	ns	
					Oversampling mode	$1 \times t_{ADcyc} + 40$	—	—	ns	
	A/D conversion	High-speed channels	Without channel dedicated sample and hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	$1 \times t_{ADcyc} + 40$	—	—	ns	
					Oversampling mode (One-channel continuous scan mode)	40	—	—	ns	
					Oversampling mode (Single/ Continuous scan mode)	$1 \times t_{ADcyc} + 40$	—	—	ns	
			With channel-dedicated sample-and-hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	$1 \times t_{ADcyc} + 160$	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc} + 160$	—	—	ns	
		Middle-speed channels		(AN012 to AN015)	SAR mode	180	—	—	ns	
					Oversampling mode	200	—	—	ns	
		Low-speed channels		(AN016 to AN022)	SAR mode	400	—	—	ns	
					Oversampling mode	400	—	—	ns	
A/D sampling time (High accuracy mode)	Self-calibration				SAR mode	$1 \times t_{ADcyc} + 140^{*1}$	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc} + 140^{*1}$	—	—	ns	
	Self-diagnosis				SAR mode	$1 \times t_{ADcyc} + 140^{*1}$	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc} + 140^{*1}$	—	—	ns	
	A/D conversion	High-speed channels	Without channel dedicated sample and hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	$1 \times t_{ADcyc} + 140^{*1}$	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc} + 140^{*1}$	—	—	ns	
			With channel-dedicated sample-and-hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	$1 \times t_{ADcyc} + 320$	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc} + 320$	—	—	ns	
		Middle-speed channels		(AN012 to AN015)	SAR mode	400	—	—	ns	
					Hybrid mode	440	—	—	ns	
		Low-speed channels		(AN016 to AN022)	SAR mode	840	—	—	ns	
					Hybrid mode	840	—	—	ns	

Table 2.85 A/D conversion characteristics (common) (3 of 3)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter				Min	Typ	Max	Unit	Test conditions
Channel dedicated sample and hold circuits	Sampling time	Self-calibration		400	—	—	ns	AVCC: 2.7 to 3.63 V VCC: 2.7 to 3.63 V VREFH0/VREFH: 2.7 V to AVCC
		A/D conversion		400	—	—	ns	
	Hold mode switching time			40	—	—	ns	
	Hold time			—	—	5	μs	
Operation stabilization time	A/D start-up time			2	—	—	μs	
	Channel-dedicated sample-and-hold circuits start-up time			2	—	—	μs	
	A/D shut-down time			1	—	—	μs	
Analog input voltage range	Single-ended input voltage	Unit 0	AN000 to AN005, AN012, AN014	VREFL0	—	VREFH0	V	—
			AN016 to AN018	VREFL0	—	VREFH0	V	VCC ≥ VREFH0
				VREFL0	—	VCC	V	VCC < VREFH0
			AN019 to AN022	VREFL0	—	VREFH0	V	VCC2 ≥ VREFH0
				VREFL0	—	VCC2	V	VCC2 < VREFH0
		Unit 1	AN006 to AN011, AN013, AN015	VREFL	—	VREFH	V	—
			AN016 to AN018	VREFL	—	VREFH	V	VCC ≥ VREFH
				VREFL	—	VCC	V	VCC < VREFH
			AN019 to AN022	VREFL	—	VREFH	V	VCC2 ≥ VREFH
				VREFL	—	VCC2	V	VCC2 < VREFH
	Differential input voltage[*2]	Unit 0	AN000 to AN005	-VREFH0	—	+VREFH0	V	—
		Unit 1	AN006 to AN011	-VREFH	—	+VREFH	V	—

Note: t_{ADcyc}: ADCLK cycle

Note: t_{Cmp}: Successive approximation time

Note 1. If t_{Cmp} is greater than 100ns, the A/D sampling time should be greater than the following equation.
$1 \times t_{ADcyc} + 1.6 \times t_{Cmp}$

Note 2. Differential input voltage is (A_{INP} - A_{INN}).

A/D Converter Unit 0:

- A_{INP} is input voltage of A_{Nx}, and VREFL0 ≤ A_{INP} ≤ VREFH0.
- A_{INN} is input voltage of A_{Ny}, and VREFL0 ≤ A_{INN} ≤ VREFH0.

A/D Converter Unit 1:

- A_{INP} is input voltage of A_{Nx}, and VREFL ≤ A_{INP} ≤ VREFH.
- A_{INN} is input voltage of A_{Ny}, and VREFL ≤ A_{INN} ≤ VREFH.

(x = 2i, y = 2i +1, i = 0, 1, 2… (any integer))

Table 2.86 A/D conversion characteristics (common) (1 of 2)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
A/D conversion clock frequency (ADCLK)						25	50	60	MHz	AVCC: 1.62 to 2.7 V VCC: 1.62 to 2.7 V VREFH0/VREFH: 1.62 V to AVCC
Successive approximation time						200	—	200	ns	
A/D sampling time (Normal mode)	Self-calibration				SAR mode	$1 \times t_{ADcyc}$ + 420	—	—	ns	AVCC: 1.62 to 2.7 V VCC: 1.62 to 2.7 V VREFH0/VREFH: 1.62 V to AVCC tCmp=200ns
					Oversampling mode	$1 \times t_{ADcyc}$ + 420	—	—	ns	
	Self-diagnosis				SAR mode	$1 \times t_{ADcyc}$ + 420	—	—	ns	
					Oversampling mode	$1 \times t_{ADcyc}$ + 420	—	—	ns	
	A/D conversion	High-speed channels	Without channel dedicated sample and hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	$1 \times t_{ADcyc}$ + 420	—	—	ns	
					Oversampling mode (One-channel continuous scan mode)	440	—	—	ns	
					Oversampling mode (Single/ Continuous scan mode)	$1 \times t_{ADcyc}$ + 420	—	—	ns	
		Middle-speed channels		(AN012 to AN015)	SAR mode	560	—	—	ns	
					Oversampling mode	560	—	—	ns	
		Low-speed channels		(AN016 to AN022)	SAR mode	800	—	—	ns	
					Oversampling mode	800	—	—	ns	
A/D sampling time (High accuracy mode)	Self-calibration				SAR mode	$1 \times t_{ADcyc}$ + 780	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc}$ + 780	—	—	ns	
	Self-diagnosis				SAR mode	$1 \times t_{ADcyc}$ + 780	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc}$ + 780	—	—	ns	
	A/D conversion	High-speed channels	Without channel dedicated sample and hold circuits	(AN000 to AN005) (AN006 to AN011)	SAR mode	$1 \times t_{ADcyc}$ + 780	—	—	ns	
					Hybrid mode	$1 \times t_{ADcyc}$ + 780	—	—	ns	
		Middle-speed channels		(AN012 to AN015)	SAR mode	1200	—	—	ns	
					Hybrid mode	1200	—	—	ns	
		Low-speed channels		(AN016 to AN022)	SAR mode	1680	—	—	ns	
					Hybrid mode	1680	—	—	ns	
Operation	A/D start-up time					2	—	—	ns	AVCC: 1.62 to 2.7 V VCC: 1.62 to 2.7 V VREFH0/VREFH: 1.62 V to AVCC
	A/D shut-down time					1	—	—	ns	

Table 2.86 A/D conversion characteristics (common) (2 of 2)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter				Min	Typ	Max	Unit	Test conditions
Analog input voltage range	Single-ended input voltage	Unit 0	AN000 to AN005, AN012, AN014	VREFL0	—	VREFH0	V	—
			AN016 to AN018	VREFL0	—	VREFH0	V	VCC ≥ VREFH0
				VREFL0	—	VCC	V	VCC < VREFH0
			AN019 to AN022	VREFL0	—	VREFH0	V	VCC2 ≥ VREFH0
				VREFL0	—	VCC2	V	VCC2 < VREFH0
		Unit 1	AN006 to AN011, AN013, AN015	VREFL	—	VREFH	V	—
			AN016 to AN018	VREFL	—	VREFH	V	VCC ≥ VREFH
				VREFL	—	VCC	V	VCC < VREFH
			AN019 to AN022	VREFL	—	VREFH	V	VCC2 ≥ VREFH
				VREFL	—	VCC2	V	VCC2 < VREFH
	Differential input voltage[*1]	Unit 0	AN000 to AN005	-VREFH0	—	+VREFH0	V	—
		Unit 1	AN006 to AN011	-VREFH	—	+VREFH	V	—

Note: t_{ADcyc}: ADCLK cycle

Note: t_{Cmp}: Successive approximation time

Note 1. Differential input voltage is (A_{INP} - A_{INN}).

A/D Converter Unit 0:

- A_{INP} is input voltage of A_{Nx}, and VREFL0 ≤ A_{INP} ≤ VREFH0.
- A_{INN} is input voltage of A_{Ny}, and VREFL0 ≤ A_{INN} ≤ VREFH0.

A/D Converter Unit 1:

- A_{INP} is input voltage of A_{Nx}, and VREFL ≤ A_{INP} ≤ VREFH.
- A_{INN} is input voltage of A_{Ny}, and VREFL ≤ A_{INN} ≤ VREFH.

(x = 2i, y = 2i +1, i = 0, 1, 2… (any integer))

Table 2.87 A/D conversion characteristics (SAR mode : DCDC mode) (1 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Resolution					—	—	12	bit	—
SAR mode	Single-ended input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.16	—	—	µs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±3	±6.5	LSB	BGA package
						—	±3	±7.5	LSB	LQFP package
					Full-scale error	—	±3	±6.5	LSB	BGA package
						—	±3	±7.5	LSB	LQFP package
					Absolute accuracy	—	±4	±11	LSB	BGA package
						—	±4	±14	LSB	LQFP package
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	BGA package
						—	±1	-1 to +2.0	LSB	LQFP package
					INL integral nonlinearity error	—	±2	±3	LSB	BGA package
						—	±2	±5	LSB	LQFP package
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.00	—	—	µs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 35 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	BGA package
						—	±1.5	±7.5	LSB	LQFP package
					Full-scale error	—	±1.5	±6.75	LSB	BGA package
						—	±1.5	±7.5	LSB	LQFP package
					Absolute accuracy	—	±5	±10.5	LSB	BGA package
						—	±5	±11.5	LSB	LQFP package
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	BGA package
						—	±1	-1 to +2.0	LSB	LQFP package
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	BGA package
						—	±2.5	±5.5	LSB	LQFP package

Table 2.87 A/D conversion characteristics (SAR mode : DCDC mode) (2 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.26	—	—	μs	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±4.5	LSB	BGA package
						—	±1.5	±5.5	LSB	LQFP package
					Full-scale error	—	±1.5	±4.5	LSB	BGA package
						—	±1.5	±5.5	LSB	LQFP package
					Absolute accuracy	—	±4	±7	LSB	BGA package
						—	±4	±10	LSB	LQFP package
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	BGA package
						—	±1	-1 to +2.0	LSB	LQFP package
					INL integral nonlinearity error	—	±2	±3	LSB	BGA package
						—	±2	±5	LSB	LQFP package
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.72	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 63 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 16 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	BGA package
						—	±1.5	±7.5	LSB	LQFP package
					Full-scale error	—	±1.5	±6.75	LSB	BGA package
						—	±1.5	±7.5	LSB	LQFP package
					Absolute accuracy	—	±4.5	±9	LSB	BGA package
						—	±4.5	±9.5	LSB	LQFP package
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	BGA package
						—	±1	-1 to +2.0	LSB	LQFP package
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	BGA package
						—	±2.5	±4.5	LSB	LQFP package

Table 2.87 A/D conversion characteristics (SAR mode : DCDC mode) (3 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	Normal mode	Middle-speed channels (AN012 to AN015)	Conversion time*1	0.28	—	—	μs	• ADCLK: 50 MHz • Sampling time: 9 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	BGA package
					—	±1.5	±6.5	LSB	LQFP package
				Full-scale error	—	±1.5	±6.5	LSB	BGA package
					—	±1.5	±6.5	LSB	LQFP package
				Absolute accuracy	—	±4	±11	LSB	BGA package
					—	±4	±15	LSB	LQFP package
				DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	BGA package
					—	±1	-1 to +2.0	LSB	LQFP package
				INL integral nonlinearity error	—	±2	±3	LSB	BGA package
					—	±2	±3	LSB	LQFP package
			Low-speed channels (AN016 to AN022)	Conversion time*1	0.5	—	—	μs	• ADCLK: 50 MHz • Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	—
				Full-scale error	—	±1.5	±6.5	LSB	—
				Absolute accuracy	—	±5.5	±11	LSB	—
				DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—

Table 2.87 A/D conversion characteristics (SAR mode : DCDC mode) (4 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	High accuracy mode	Middle-speed channels (AN012 to AN015)	Conversion time*1	0.5	—	—	μs	• ADCLK: 50 MHz • Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±4.5	LSB	BGA package
					—	±1.5	±4.5	LSB	LQFP package
				Full-scale error	—	±1.5	±4.5	LSB	BGA package
					—	±1.5	±4.5	LSB	LQFP package
				Absolute accuracy	—	±4	±7	LSB	BGA package
					—	±4	±11	LSB	LQFP package
				DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	BGA package
					—	±1	-1 to +2.0	LSB	LQFP package
				INL integral nonlinearity error	—	±2	±3	LSB	BGA package
					—	±2	±4.5	LSB	LQFP package
			Low-speed channels (AN016 to AN022)	Conversion time*1	0.94	—	—	μs	• ADCLK: 50 MHz • Sampling time: 42 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±4.5	LSB	—
				Full-scale error	—	±1.5	±4.5	LSB	—
				Absolute accuracy	—	±5.5	±8	LSB	—
				DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—

Table 2.87 A/D conversion characteristics (SAR mode : DCDC mode) (5 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Differential input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.16	—	—	μs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±2	±3.5	LSB	—
					Full-scale error	—	±2	±3.5	LSB	—
					Absolute accuracy	—	±3	±6	LSB	—
					DNL differential nonlinearity error *3	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.00	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 35 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	—
					Full-scale error	—	±1.5	±6.75	LSB	—
					Absolute accuracy	—	±3.5	±10.5	LSB	—
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	—

Table 2.87 A/D conversion characteristics (SAR mode : DCDC mode) (6 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Differential input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.26	—	—	μs	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1	±2.5	LSB	—
					Full-scale error	—	±1	±2.5	LSB	—
					Absolute accuracy	—	±2	±4	LSB	—
					DNL differential nonlinearity error *3	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.72	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 63 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 16 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	—
					Full-scale error	—	±1.5	±6.75	LSB	—
					Absolute accuracy	—	±3.5	±9	LSB	—
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	—

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Without channel dedicated sample and hold circuits; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 2. With channel-dedicated sample-and-hold circuits; The conversion time is the sum of the sampling time of channel-dedicated sample-and-hold circuits, the hold mode switching time, the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 3. DNL is measured using the Histogram Method, so the lower limit value is -1.

Table 2.88 A/D conversion characteristics (SAR mode : External VDD mode) (1 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Resolution					—	—	12	bit	—
SAR mode	Single-ended input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time[*1]	0.16	—	—	μs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±3	±6.5	LSB	—
					Full-scale error	—	±3	±6.5	LSB	—
					Absolute accuracy	—	±4	±11	LSB	—
					DNL differential nonlinearity error [*3]	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2	±3	LSB	—
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time[*2]	1.00	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 35 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	—
					Full-scale error	—	±1.5	±6.75	LSB	—
					Absolute accuracy	—	±5	±10.5	LSB	—
					DNL differential nonlinearity error [*3]	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	—

Table 2.88 A/D conversion characteristics (SAR mode : External VDD mode) (2 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.26	—	—	μs	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±4.5	LSB	—
					Full-scale error	—	±1.5	±4.5	LSB	—
					Absolute accuracy	—	±4	±7	LSB	—
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2	±3	LSB	—
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.72	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 63 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 16 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	—
					Full-scale error	—	±1.5	±6.75	LSB	—
					Absolute accuracy	—	±4.5	±9	LSB	—
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	—

Table 2.88 A/D conversion characteristics (SAR mode : External VDD mode) (3 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	Normal mode	Middle-speed channels (AN012 to AN015)	Conversion time*1	0.28	—	—	μs	• ADCLK: 50 MHz • Sampling time: 9 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	—
				Full-scale error	—	±1.5	±6.5	LSB	—
				Absolute accuracy	—	±4	±11	LSB	—
				DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±3	LSB	—
			Low-speed channels (AN016 to AN022)	Conversion time*1	0.5	—	—	μs	• ADCLK: 50 MHz • Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	—
				Full-scale error	—	±1.5	±6.5	LSB	—
				Absolute accuracy	—	±5.5	±11	LSB	—
				DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—

Table 2.88 A/D conversion characteristics (SAR mode : External VDD mode) (4 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	High accuracy mode	Middle-speed channels (AN012 to AN015)	Conversion time[*1]	0.5	—	—	μs	• ADCLK: 50 MHz • Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±4.5	LSB	—
				Full-scale error	—	±1.5	±4.5	LSB	—
				Absolute accuracy	—	±4	±7	LSB	—
				DNL differential nonlinearity error [*3]	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±3	LSB	—
			Low-speed channels (AN016 to AN022)	Conversion time[*1]	0.94	—	—	μs	• ADCLK: 50 MHz • Sampling time: 42 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±4.5	LSB	—
				Full-scale error	—	±1.5	±4.5	LSB	—
				Absolute accuracy	—	±5.5	±8	LSB	—
				DNL differential nonlinearity error [*3]	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—

Table 2.88 A/D conversion characteristics (SAR mode : External VDD mode) (5 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Differential input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.16	—	—	μs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±2	±3.5	LSB	—
					Full-scale error	—	±2	±3.5	LSB	—
					Absolute accuracy	—	±3	±6	LSB	—
					DNL differential nonlinearity error *3	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.00	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 35 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	—
					Full-scale error	—	±1.5	±6.75	LSB	—
					Absolute accuracy	—	±3.5	±10.5	LSB	—
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	—

Table 2.88 A/D conversion characteristics (SAR mode : External VDD mode) (6 of 6)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Differential input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.26	—	—	μs	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1	±2.5	LSB	—
					Full-scale error	—	±1	±2.5	LSB	—
					Absolute accuracy	—	±2	±4	LSB	—
					DNL differential nonlinearity error *3	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—
			High-speed channels (AN000 to AN005) (AN006 to AN011)	With channel dedicated sample and hold circuits	Conversion time*2	1.72	—	—	μs	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: 63 ADCLK • Hold mode switching time of channel-dedicated sample-and-hold circuits: 2 ADCLK • Sampling time: 16 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±6.75	LSB	—
					Full-scale error	—	±1.5	±6.75	LSB	—
					Absolute accuracy	—	±3.5	±9	LSB	—
					DNL differential nonlinearity error *3	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2.5	±3.5	LSB	—

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Without channel dedicated sample and hold circuits; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 2. With channel-dedicated sample-and-hold circuits; The conversion time is the sum of the sampling time of channel-dedicated sample-and-hold circuits, the hold mode switching time, the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 3. DNL is measured using the Histogram Method, so the lower limit value is -1.

Table 2.89 A/D conversion characteristics (SAR mode : DCDC mode) (1 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Resolution					—	—	12	bit	—
SAR mode	Single-ended input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.64	—	—	μs	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±3	±6.5	LSB	BGA package
						—	±3	±8	LSB	LQFP package
					Full-scale error	—	±3	±6.5	LSB	BGA package
						—	±3	±8	LSB	LQFP package
					Absolute accuracy	—	±5.5	±11	LSB	BGA package
						—	±5.5	±15	LSB	LQFP package
					DNL differential nonlinearity error *2	—	±1	-1 to +1.5	LSB	BGA package
						—	±1	-1 to +2.0	LSB	LQFP package
					INL integral nonlinearity error	—	±2	±3	LSB	BGA package
						—	±2	±3.5	LSB	LQFP package
SAR mode	Single-ended input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	1	—	—	μs	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±4.5	LSB	BGA package
						—	±1.5	±5	LSB	LQFP package
					Full-scale error	—	±1.5	±4.5	LSB	BGA package
						—	±1.5	±5	LSB	LQFP package
					Absolute accuracy	—	±5.0	±8	LSB	BGA package
						—	±5.0	±11	LSB	LQFP package
					DNL differential nonlinearity error *2	—	±1	-1 to +1.5	LSB	BGA package
						—	±1	-1 to +1.5	LSB	LQFP package
					INL integral nonlinearity error	—	±2	±3	LSB	BGA package
						—	±2	±3.5	LSB	LQFP package

Table 2.89 A/D conversion characteristics (SAR mode : DCDC mode) (2 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	Normal mode	Middle-speed channels (AN012 to AN015)	Conversion time[*1]	0.76	—	—	μs	• ADCLK: 50 MHz • Sampling time: 28 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	—	±6.5	LSB	BGA package
					—	±1.5	±7	LSB	LQFP package
				Full-scale error	—	±1.5	±6.5	LSB	BGA package
					—	±1.5	±7	LSB	LQFP package
				Absolute accuracy	—	±4	±11	LSB	BGA package
					—	±4	±15	LSB	LQFP package
				DNL differential nonlinearity error [*2]	—	±1	-1 to +1.5	LSB	BGA package
					—	±1	-1 to +2.0	LSB	LQFP package
				INL integral nonlinearity error	—	±2	±3	LSB	BGA package
					—	±2	±4	LSB	LQFP package
			Low-speed channels (AN016 to AN022)	Conversion time[*1]	1	—	—	μs	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	—
				Full-scale error	—	±1.5	±6.5	LSB	—
				Absolute accuracy	—	±5.5	±11	LSB	—
				DNL differential nonlinearity error [*2]	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—

Table 2.89 A/D conversion characteristics (SAR mode : DCDC mode) (3 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	High accuracy mode	Middle-speed channels (AN012 to AN015)	Conversion time*1	1.4	—	—	μs	• ADCLK: 50 MHz • Sampling time: 60 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±4.5	LSB	BGA package
					—	±1.5	±5	LSB	LQFP package
				Full-scale error	—	±1.5	±4.5	LSB	BGA package
					—	±1.5	±5	LSB	LQFP package
				Absolute accuracy	—	±4	±8	LSB	BGA package
					—	±4	±13	LSB	LQFP package
				DNL differential nonlinearity error *2	—	±1	-1 to +1.5	LSB	BGA package
					—	±1	-1 to +2.0	LSB	LQFP package
				INL integral nonlinearity error	—	±2	±3	LSB	BGA package
					—	±2	±4	LSB	LQFP package
			Low-speed channels (AN016 to AN022)	Conversion time*1	1.88	—	—	μs	• ADCLK: 50 MHz • Sampling time: 84 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±4.5	LSB	—
				Full-scale error	—	±1.5	±4.5	LSB	—
				Absolute accuracy	—	±5.5	±8	LSB	—
				DNL differential nonlinearity error *2	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—
SAR mode	Differential input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Conversion time*1	0.64	—	—	μs	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±2	±3.5	LSB	—
				Full-scale error	—	±2	±3.5	LSB	—
				Absolute accuracy	—	±4.5	±6	LSB	—
				DNL differential nonlinearity error *2	—	±0.75	±1	LSB	—
				INL integral nonlinearity error	—	±1.5	±2	LSB	—

Table 2.89 A/D conversion characteristics (SAR mode : DCDC mode) (4 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Differential input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time[*1]	1	—	—	μs	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1	±2.5	LSB	—
					Full-scale error	—	±1	±2.5	LSB	—
					Absolute accuracy	—	±3.5	±4.5	LSB	—
					DNL differential nonlinearity error [*2]	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Without channel dedicated sample and hold circuits; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 2. DNL is measured using the Histogram Method, so the lower limit value is -1.

Table 2.90 A/D conversion characteristics (SAR mode : External VDD mode) (1 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Resolution					—	—	12	bit	—
SAR mode	Single-ended input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time[*1]	0.64	—	—	μs	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±3	±6.5	LSB	—
					Full-scale error	—	±3	±6.5	LSB	—
					Absolute accuracy	—	±5.5	±11	LSB	—
					DNL differential nonlinearity error [*2]	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2	±3	LSB	—
SAR mode	Single-ended input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time[*1]	1	—	—	μs	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±4.5	LSB	—
					Full-scale error	—	±1.5	±4.5	LSB	—
					Absolute accuracy	—	±5.0	±8	LSB	—
					DNL differential nonlinearity error [*2]	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2	±3	LSB	—

Table 2.90 A/D conversion characteristics (SAR mode : External VDD mode) (2 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	Normal mode	Middle-speed channels (AN012 to AN015)	Conversion time[*1]	0.76	—	—	μs	• ADCLK: 50 MHz • Sampling time: 28 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	—
				Full-scale error	—	±1.5	±6.5	LSB	—
				Absolute accuracy	—	±4	±11	LSB	—
				DNL differential nonlinearity error [*2]	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±3	LSB	—
			Low-speed channels (AN016 to AN022)	Conversion time[*1]	1	—	—	μs	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
				Offset error	—	±1.5	±6.5	LSB	—
				Full-scale error	—	±1.5	±6.5	LSB	—
				Absolute accuracy	—	±5.5	±11	LSB	—
				DNL differential nonlinearity error [*2]	—	±1	-1 to +1.5	LSB	—
				INL integral nonlinearity error	—	±2	±4	LSB	—

Table 2.90 A/D conversion characteristics (SAR mode : External VDD mode) (3 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Single-ended input	High accuracy mode	Middle-speed channels (AN012 to AN015)		Conversion time*1	1.4	—	—	μs	• ADCLK: 50 MHz • Sampling time: 60 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±4.5	LSB	—
					Full-scale error	—	±1.5	±4.5	LSB	—
					Absolute accuracy	—	±4	±8	LSB	—
					DNL differential nonlinearity error *2	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2	±3	LSB	—
			Low-speed channels (AN016 to AN022)		Conversion time*1	1.88	—	—	μs	• ADCLK: 50 MHz • Sampling time: 84 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1.5	±4.5	LSB	—
					Full-scale error	—	±1.5	±4.5	LSB	—
					Absolute accuracy	—	±5.5	±8	LSB	—
					DNL differential nonlinearity error *2	—	±1	-1 to +1.5	LSB	—
					INL integral nonlinearity error	—	±2	±4	LSB	—
SAR mode	Differential input	Normal mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time*1	0.64	—	—	μs	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±2	±3.5	LSB	—
					Full-scale error	—	±2	±3.5	LSB	—
					Absolute accuracy	—	±4.5	±6	LSB	—
					DNL differential nonlinearity error *2	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—

Table 2.90 A/D conversion characteristics (SAR mode : External VDD mode) (4 of 4)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter						Min	Typ	Max	Unit	Test conditions
SAR mode	Differential input	High accuracy mode	High-speed channels (AN000 to AN005) (AN006 to AN011)	Without channel dedicated sample and hold circuits	Conversion time[*1]	1	—	—	μs	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less
					Offset error	—	±1	±2.5	LSB	—
					Full-scale error	—	±1	±2.5	LSB	—
					Absolute accuracy	—	±3.5	±4.5	LSB	—
					DNL differential nonlinearity error [*2]	—	±0.75	±1	LSB	—
					INL integral nonlinearity error	—	±1.5	±2	LSB	—

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Without channel dedicated sample and hold circuits; The conversion time is the sum of the sampling time and the successive approximation time. Each of the above state is indicated for the test conditions.

Note 2. DNL is measured using the Histogram Method, so the lower limit value is -1.

Table 2.91 A/D conversion characteristics (Oversampling mode and Hybrid mode) (1)

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode and Hybrid mode	Resolution			—	—	16	bit	—
	Oversampling period	Oversampling mode		0.16	—	—	μs	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Without disconnection detection assist function • Signal source impedance: 50 Ω or less
		Hybrid mode[*2]		0.18	—	—	μs	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Without disconnection detection assist function • Signal source impedance: 50 Ω or less
	Digital filter characteristics[*1]	Sinc filter	Initial delay	—	22	—	/Fos	—
			Group delay	—	11	—		—
			Normalized Cutoff Frequency	—	0.033	—	Fin/Fos	—

Note: Fos is oversampling frequency.
When in Hybrid mode, Fos is 1/ (the sum of the oversampling periods of each analog channel assigned to the scan group).

Note 1. See Figure 2.125.

Note 2. Value per channel.

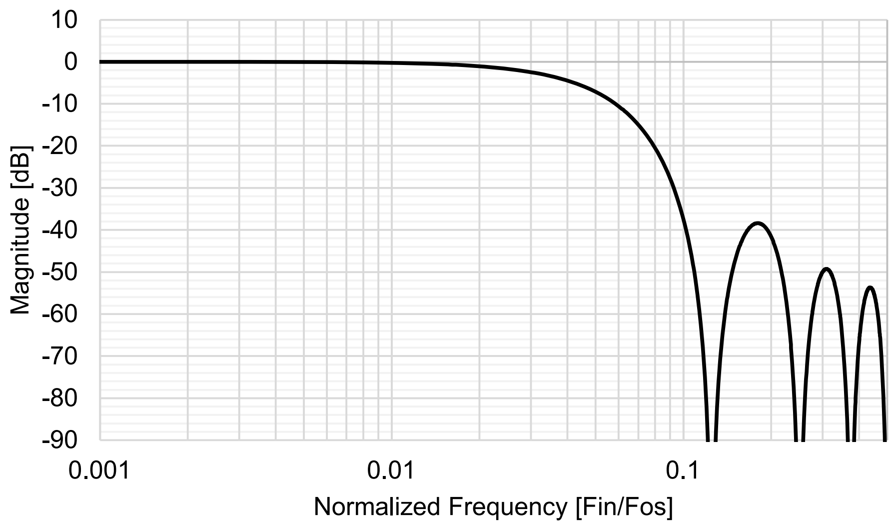


Figure 2.125 Digital filter characteristics (Sinc filter)

Table 2.92 A/D conversion characteristics (Oversampling mode and Hybrid mode) (2)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode and Hybrid mode	Sinc filter	Single-ended input (AN000 to AN005) (AN006 to AN011) (AN012 to AN015)	SNDR signal-to-noise and distortion ratio	—	80	—	dB	● ADCLK: 50 MHz ● Sampling time: – High-speed channels (Oversampling mode): 3 ADCLK – High-speed channels (Hybrid mode): 8 ADCLK – Middle-speed channels (Oversampling mode): 10 ADCLK – Middle-speed channels (Hybrid mode): 22 ADCLK ● Successive approximation time: 5 ADCLK ● Signal source impedance: 50 Ω or less ● Input frequency: – Oversampling mode: 5 kHz – Hybrid mode: 5 kHz ● Without channel dedicated sample and hold circuits
			ENOB effective number of bits	—	13	—	bit	
		Differential input (AN000 to AN005) (AN006 to AN011)	SNDR signal-to-noise and distortion ratio	—	86	—	dB	
			ENOB effective number of bits	—	14	—	bit	

Table 2.93 A/D conversion characteristics (Oversampling mode and Hybrid mode) (3)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode and Hybrid mode	Sinc filter	Single-ended input (AN000 to AN005) (AN006 to AN011) (AN012 to AN015)	SNDR signal-to-noise and distortion ratio	—	74	—	dB	• ADCLK: 50 MHz • Sampling time: – High-speed channels (Oversampling mode): 22 ADCLK – High-speed channels (Hybrid mode): 40 ADCLK – Middle-speed channels (Oversampling mode): 28 ADCLK – Middle-speed channels (Hybrid mode): 60 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Input frequency: – Oversampling mode: 5 kHz – Hybrid mode: 5 kHz • Without channel dedicated sample and hold circuits
			ENOB effective number of bits	—	12	—	bit	
		Differential input (AN000 to AN005) (AN006 to AN011)	SNDR signal-to-noise and distortion ratio	—	80	—	dB	
			ENOB effective number of bits	—	13	—	bit	

Table 2.94 A/D conversion characteristics (Oversampling mode)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode	Single-ended input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error (Single/ Continuous mode) *3	—	±1	±4	LSB	
			Gain error (One-channel continuous mode) *3	—	±1	±5	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +1.5	-1 to +2.5	LSB	
			INL integral nonlinearity error*1	—	±4	±8	LSB	
		Middle-speed channels (AN012 to AN015)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 10 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error *3	—	±1	±4	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +4	LSB	
			INL integral nonlinearity error*1	—	±4	±8	LSB	
		Low-speed channels (AN016 to AN022)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 20 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error *3	—	±1	±4	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +4	LSB	
			INL integral nonlinearity error*1	—	±4	±12	LSB	
	Differential input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *3	—	±0.25	±2	LSB	• ADCLK: 50 MHz • Sampling time: 3 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error (Single/ Continuous mode) *3	—	±0.5	±2	LSB	
			Gain error (One-channel continuous mode) *3	—	±0.5	±2.5	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +1.5	-1 to +2.0	LSB	
			INL integral nonlinearity error*1	—	±3	±6	LSB	

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Test conditions: 0.2% to 99.8% of the analog input voltage range.

Note 2. DNL is measured using the Histogram Method, so the lower limit value is -1.

Note 3. This value is based on a 12-bit resolution.

Table 2.95 A/D conversion characteristics (Oversampling mode)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter				Min	Typ	Max	Unit	Test conditions
Oversampling mode	Single-ended input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error (Single/ Continuous mode) *3	—	±1	±4	LSB	
			Gain error (One-channel continuous mode) *3	—	±1	±5	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +2.5	LSB	
			INL integral nonlinearity error*1	—	±4	±8	LSB	
		Middle-speed channels (AN012 to AN015)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 28 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error *3	—	±1	±4	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +4	LSB	
			INL integral nonlinearity error*1	—	±4	±8	LSB	
		Low-speed channels (AN016 to AN022)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error *3	—	±1	±4	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +4	LSB	
			INL integral nonlinearity error*1	—	±4	±12	LSB	
	Differential input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *3	—	±0.25	±2	LSB	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
			Gain error (Single/ Continuous mode) *3	—	±0.5	±2	LSB	
			Gain error (One-channel continuous mode) *3	—	±0.5	±2.5	LSB	
			DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +2.5	LSB	
			INL integral nonlinearity error*1	—	±3	±6	LSB	

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Test conditions: 0.2% to 99.8% of the analog input voltage range.
Note 2. DNL is measured using the Histogram Method, so the lower limit value is -1.
Note 3. This value is based on a 12-bit resolution.

Table 2.96 A/D conversion characteristics (Hybrid mode)

Conditions: AVCC: 2.7 to 3.63 V, VCC: 2.7 to 3.63 V, VREFH0/VREFH: 2.7 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
Hybrid mode	Without channel dedicated sample and hold circuits	Single-ended input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *4	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *4	—	±1	±5	LSB	
				DNL differential nonlinearity error*2 *3	—	-1 to +1.5	-1 to +2.5	LSB	
				INL integral nonlinearity error*2	—	±4	±8	LSB	
			Middle-speed channels (AN012 to AN015) *1	Offset error *4	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 22 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *4	—	±1	±5	LSB	
				DNL differential nonlinearity error*2 *3	—	-1 to +2	-1 to +4	LSB	
				INL integral nonlinearity error*2	—	±4	±8	LSB	
			Low-speed channels (AN016 to AN022) *1	Offset error *4	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 42 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *4	—	±1	±5	LSB	
				DNL differential nonlinearity error*2*3	—	-1 to +2	-1 to +4	LSB	
				INL integral nonlinearity error*2	—	±4	±12	LSB	
		Differential input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *4	—	±0.25	±2	LSB	• ADCLK: 50 MHz • Sampling time: 8 ADCLK • Successive approximation time: 5 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *4	—	±0.5	±2.5	LSB	
				DNL differential nonlinearity error*2 *3	—	-1 to +1.5	-1 to +2	LSB	
				INL integral nonlinearity error*2	—	±3	±6	LSB	
	With channel dedicated sample and hold circuits	Single-ended input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *4	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: * ADCLK • Hold mode switching time of channel dedicated sample-and-hold circuits: * ADCLK • Sampling time: * ADCLK • Successive approximation time: * ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *4	—	±0.5	±4	LSB	
				DNL differential nonlinearity error*2 *3	—	±1	-1 to +2	LSB	
				INL integral nonlinearity error*2	—	±12	±16	LSB	
		Differential input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *4	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time of channel-dedicated sample-and-hold circuits: * ADCLK • Hold mode switching time of channel dedicated sample-and-hold circuits: * ADCLK • Sampling time: * ADCLK • Successive approximation time: * ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *4	—	±0.5	±4	LSB	
				DNL differential nonlinearity error*2 *3	—	±1	-1 to +2	LSB	
				INL integral nonlinearity error*2	—	±4	±16	LSB	

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Channel-dedicated sample-and-hold circuits are not available in these channels.
Note 2. Test conditions: 0.2% to 99.8% of the analog input voltage range.
Note 3. DNL is measured using the Histogram Method, so the lower limit value is -1.
Note 4. This value is based on a 12-bit resolution.

Table 2.97 A/D conversion characteristics (Hybrid mode)

Conditions: AVCC: 1.62 to 2.7 V, VCC: 1.62 to 2.7 V, VREFH0/VREFH: 1.62 V to AVCC

Parameter					Min	Typ	Max	Unit	Test conditions
Hybrid mode	Without channel dedicated sample and hold circuits	Single-ended input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *3	—	±1	±5	LSB	
				DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +2.5	LSB	
				INL integral nonlinearity error*1	—	±4	±8	LSB	
			Middle-speed channels (AN012 to AN015)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 60 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *3	—	±1	±5	LSB	
				DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +4	LSB	
				INL integral nonlinearity error*1	—	±4	±8	LSB	
			Low-speed channels (AN016 to AN022)	Offset error *3	—	±0.5	±4	LSB	• ADCLK: 50 MHz • Sampling time: 84 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error*3	—	±1	±5	LSB	
				DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +4	LSB	
				INL integral nonlinearity error*1	—	±4	±12	LSB	
		Differential input	High-speed channels (AN000 to AN005) (AN006 to AN011)	Offset error *3	—	±0.25	±2	LSB	• ADCLK: 50 MHz • Sampling time: 40 ADCLK • Successive approximation time: 10 ADCLK • Signal source impedance: 50 Ω or less • Digital filter: Sinc filter
				Gain error *3	—	±0.5	±2.5	LSB	
				DNL differential nonlinearity error*1 *2	—	-1 to +2	-1 to +2.5	LSB	
				INL integral nonlinearity error*1	—	±3	±6	LSB	

Note: These specification values are applicable when only one ADC16H is operating, DAC12 and ACMPHS are not operating, and there is no access to the external bus during A/D conversion.
If other ADC unit, DAC12, or ACMPHS is operating or bus access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the ADC16H is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and ADC16H input voltage is stable.

Note 1. Test conditions: 0.2% to 99.8% of the analog input voltage range.
Note 2. DNL is measured using the Histogram Method, so the lower limit value is -1.
Note 3. This value is based on a 12-bit resolution.

Table 2.98 A/D internal reference voltage characteristics (1 of 2)

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	0.77	0.8	0.84	V	—

Table 2.98 A/D internal reference voltage characteristics (2 of 2)

Parameter	Min	Typ	Max	Unit	Test conditions
Sampling time	4.15	—	—	μs	—

Table 2.99 A/D conversion characteristics of D/A output

Parameter	Min	Typ	Max	Unit	Test conditions
Sampling time	1	—	—	μs	—

2.6 DAC12 Characteristics

Table 2.100 D/A conversion characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		—	—	—	12	Bits	—
INL	VREFH ≥ 2.7V	—	—	±2.0	±4.0	LSB	—
	VREFH < 2.7V	—	—	±4.0	±8.0		
DNL	VREFH ≥ 2.7V	—	—	±0.5	±1.0	LSB	—
	VREFH < 2.7V	—	—	±1.0	±2.0		
Conversion time	VREFH ≥ 2.7V	t_{DCONV1}, t_{DCONV2}	—	—	3.5	μs	—
	VREFH < 2.7V		—	—	6		
Output destination switching time	VREFH ≥ 2.7V	$t_{DSLPUP1}$, $t_{DSLPUP2}$	—	—	3.5	μs	—
	VREFH < 2.7V		—	—	6		
Buffer preparation time	VREFH ≥ 2.7V	t_{DISOUT}	—	—	3.5	μs	—
	VREFH < 2.7V		—	—	6		
Setup time		t_{SU}	—	—	4	ns	—
Resistive load		—	5	—	—	kΩ	—
Capacitive load		—	—	—	50	pF	—
Output voltage range	VREFH ≥ 2.7V	—	0.20	—	VREFH – 0.20	V	—
	VREFH < 2.7V	—	0.34	—	VREFH – 0.34		

2.7 TSN Characteristics

Table 2.101 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	-1.0	—	1.0	°C	A/D converter error is not included.
Temperature slope	—	—	2.7	—	mV/°C	—
Output voltage (at 25 °C)	—	—	0.83	—	V	—
Temperature sensor stabilization time	t_{TSTBL}	—	—	30	μs	—
Comparator stabilization time	t_{RSTBL}	—	—	30	μs	—
Sampling time	—	4.15	—	—	μs	—

2.8 OSC Stop Detect Characteristics

Table 2.102 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.126

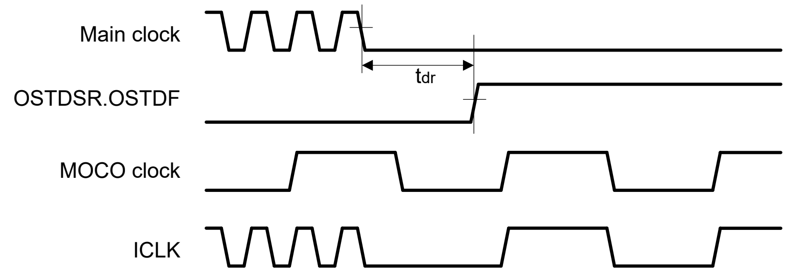


Figure 2.126 Oscillation stop detection timing

Table 2.103 Sub-clock oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time for startup	t_{sosdup}	100	—	—	μs	Figure 2.127
Detection time	t_{dr}	—	—	2	ms	Figure 2.128

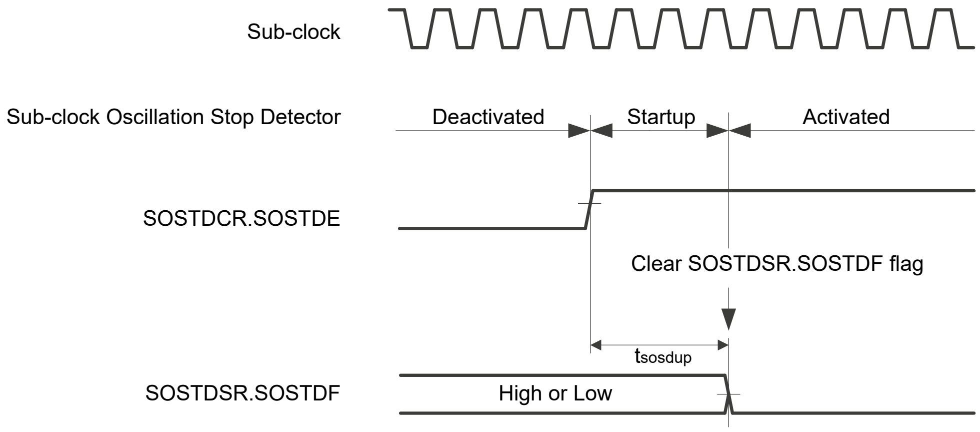


Figure 2.127 Sub-clock Oscillation Stop Detector start-up time

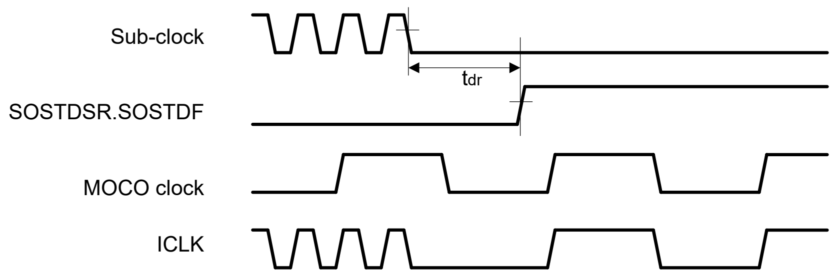


Figure 2.128 Sub-clock oscillation stop detection timing

2.9 POR and PVD Characteristics

Table 2.104 Power-on reset circuit and voltage detection circuit characteristics (1 of 2)

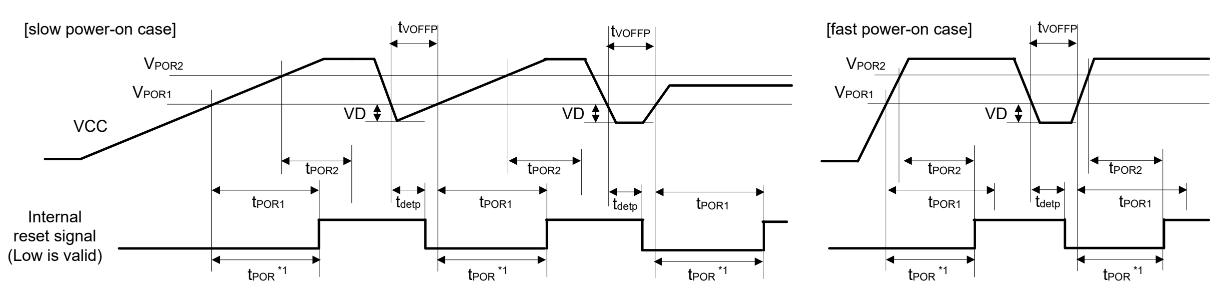
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	V_{POR1}	1.52	1.56	1.61	V	Figure 2.129
		V_{POR2}	—	—	1.73		
	Voltage detection circuit (PVD0)	V_{det0_0}	2.76	2.85	2.94		Figure 2.130
		V_{det0_1}	2.50	2.58	2.66		
		V_{det0_2}	2.08	2.15	2.22		
		V_{det0_3}	1.93	2.00	2.07		
		V_{det0_4}	1.84	1.90	1.96		
		V_{det0_5}	1.74	1.80	1.86		
		V_{det0_6}	1.62	1.67	1.73		
		V_{det0_7}	1.51	1.56	1.61		
	Voltage detection circuit (PVDn) (n = 1, 2, 4, 5)	$V_{detn\_3\_rise}$	3.78	3.92	4.05		Figure 2.131
		$V_{detn\_3\_fall}$	3.72	3.86	3.99		
		$V_{detn\_4\_rise}$	3.09	3.20	3.30		
		$V_{detn\_4\_fall}$	3.03	3.14	3.24		
		$V_{detn\_5\_rise}$	3.05	3.16	3.26		
		$V_{detn\_5\_fall}$	2.99	3.10	3.20		
		$V_{detn\_6\_rise}$	3.03	3.14	3.24		
		$V_{detn\_6\_fall}$	2.97	3.08	3.18		
		$V_{detn\_7\_rise}$	2.81	2.91	3.00		
		$V_{detn\_7\_fall}$	2.75	2.85	2.94		
		$V_{detn\_8\_rise}$	2.79	2.89	2.98		
		$V_{detn\_8\_fall}$	2.73	2.83	2.92		
		$V_{detn\_9\_rise}$	2.76	2.86	2.95		
		$V_{detn\_9\_fall}$	2.70	2.80	2.89		
		$V_{detn\_10\_rise}$	2.58	2.67	2.75		
		$V_{detn\_10\_fall}$	2.53	2.62	2.70		
		$V_{detn\_11\_rise}$	2.30	2.38	2.46		
		$V_{detn\_11\_fall}$	2.25	2.33	2.41		
		$V_{detn\_12\_rise}$	1.88	1.94	2.00		
		$V_{detn\_12\_fall}$	1.84	1.90	1.96		
		$V_{detn\_13\_rise}$	1.84	1.90	1.96		
		$V_{detn\_13\_fall}$	1.80	1.86	1.92		
		$V_{detn\_14\_rise}$	1.72	1.78	1.84		
		$V_{detn\_14\_fall}$	1.68	1.74	1.80		
		$V_{detn\_15\_rise}$	1.66	1.72	1.77		
		$V_{detn\_15\_fall}$	1.62	1.68	1.73		

Table 2.104 Power-on reset circuit and voltage detection circuit characteristics (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Internal reset time*1	Power-on reset time	t_{POR1}	—	—	6.7	ms	Figure 2.129
		t_{POR2}	—	—	1.6		
	PVD0 reset time	t_{PVD0}	—	—	*1		Figure 2.129
	PVD1 reset time	t_{PVD1}	—	—	*1		Figure 2.130
	PVD2 reset time	t_{PVD2}	—	—	*1		
	PVD4 reset time	t_{PVD4}	—	—	*1		
	PVD5 reset time	t_{PVD5}	—	—	*1		
Minimum VCC downtime (POR)*2	50mV < VD	t_{VOFFP}	900	—	—	µs	Figure 2.129
	VD ≤ 50mV		2000	—	—		
Minimum VCC downtime (PVD)*2	PVD0	t_{VOFF}	25	—	—	µs	Figure 2.130
	PVD1, PVD2, PVD4, PVD5		25	—	—		
Response delay time (POR)	50mV < VD	t_{detp}	—	—	900	µs	Figure 2.129
	VD ≤ 50mV		—	—	2000		
Response delay time (PVD)	PVD0	t_{det}	—	—	25	µs	Figure 2.130, Figure 2.131
	PVD1, PVD2, PVD4, PVD5		—	—	25		
PVDn operation stabilization time (after PVD is enabled) (n = 1, 2, 4, 5)		$T_{d\ (E-A)}$	—	—	20	µs	Figure 2.131

Note 1. The maximum value of t_{PVD0}, t_{PVD1}, t_{PVD2}, t_{PVD4}, t_{PVD5} are equal to t_{DSBY} because the internal reset time is maximized when returning from Deep Software Standby mode.

Note 2. The minimum VCC downtime indicates the time when VCC is below the minimum value of voltage detection levels V_{POR1}, V_{det0}, V_{det1}, V_{det2}, V_{det4} and V_{det5} for the POR / PVD.



Note 1. t_{POR} is determined by the earlier point in time when the t_{POR1} has passed after crossing V_{POR1} or when the t_{POR2} has passed after crossing V_{POR2}.

Figure 2.129 Power-on reset timing

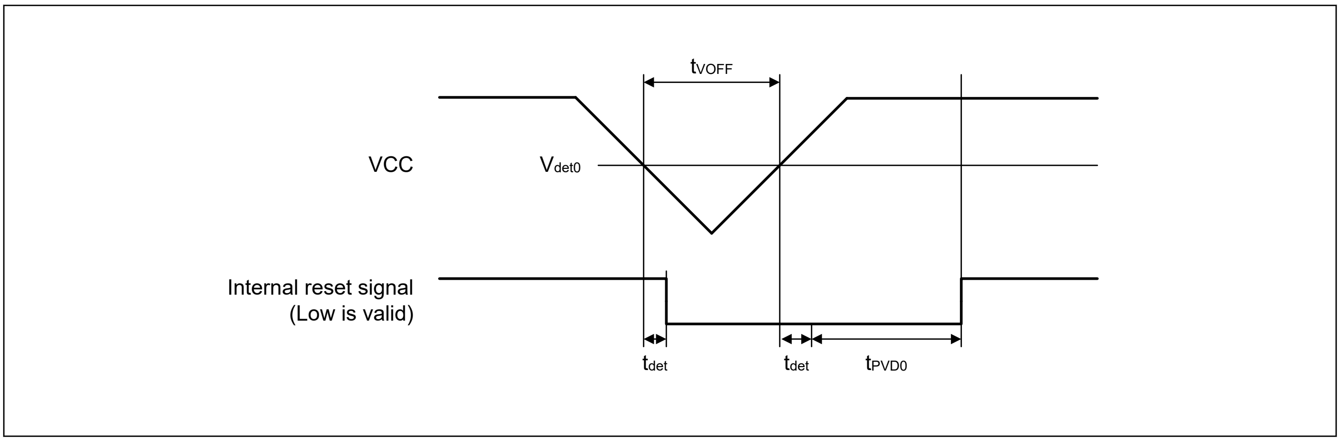


Figure 2.130 Voltage detection circuit timing (V_{det0})

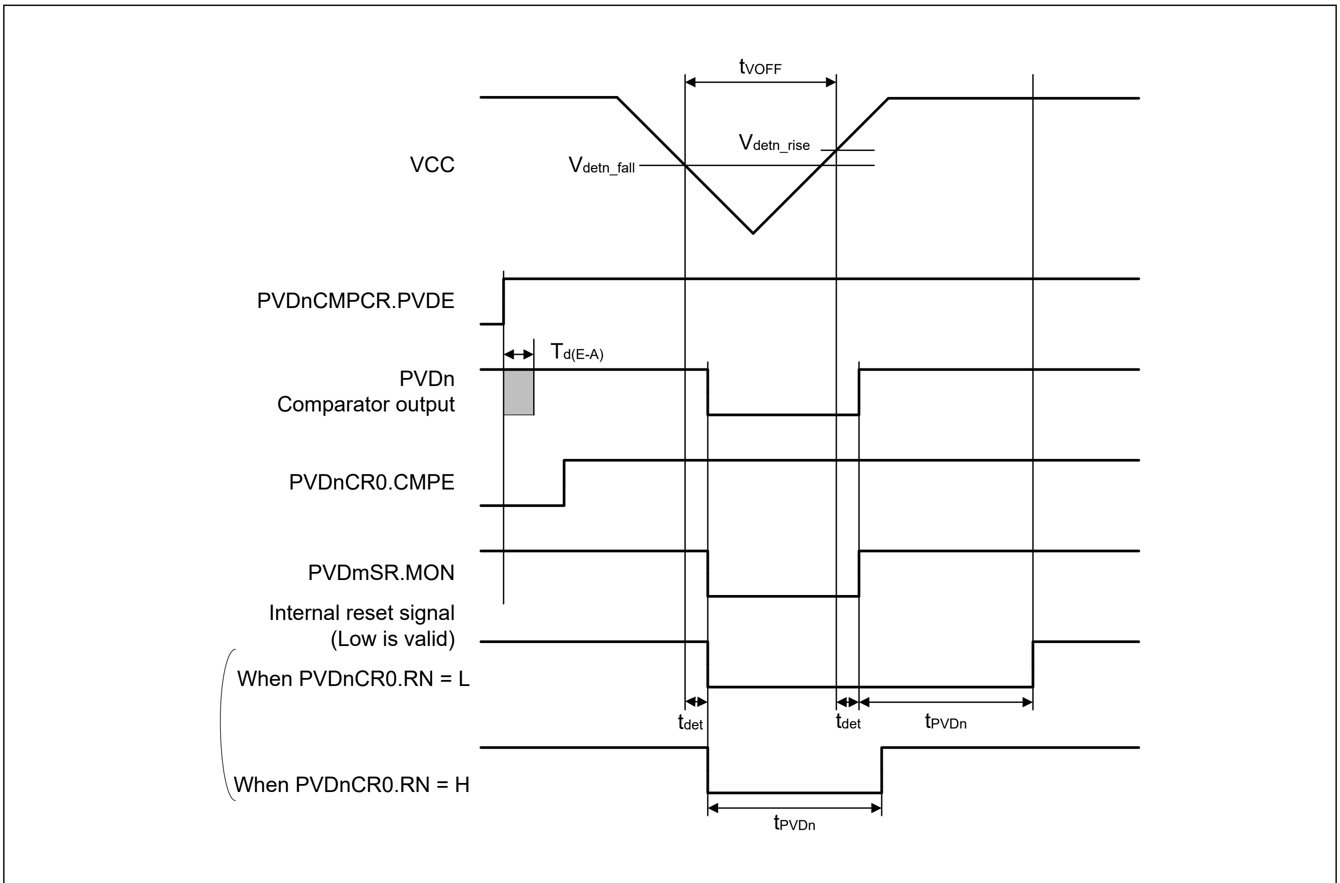


Figure 2.131 Voltage detection circuit timing (V_{detn}) (n = 1, 2, 4, 5)

2.10 External VDD Timing Characteristics

Table 2.105 External VDD timing characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Reset hold time at power up of external VDD with using RES pin	t_{EXTVRH}	600.00	—	—	µs	Figure 2.132 Figure 2.133
VDD rise time at power up of external VDD without using RES pin	t_{EXTVDD}	—	—	550	µs	

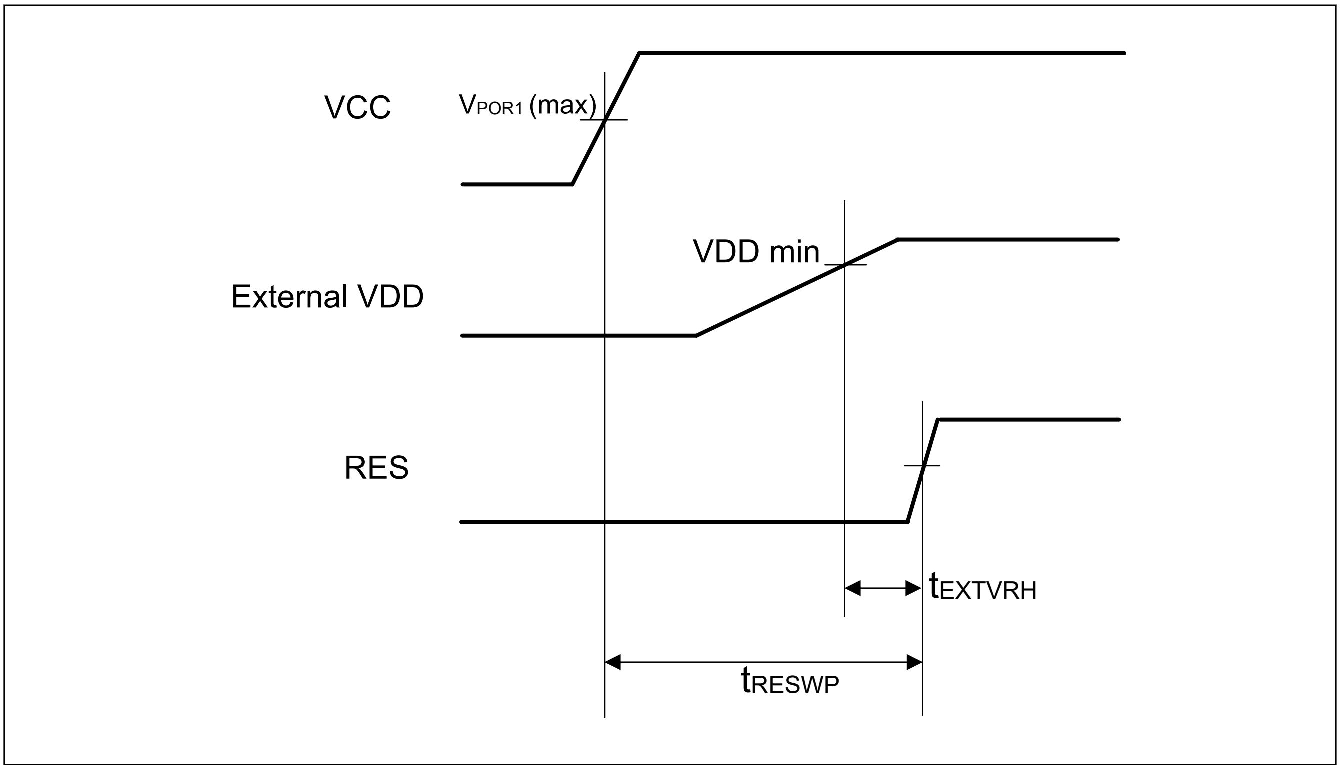


Figure 2.132 Power-up sequence of external VDD mode with using RES pin

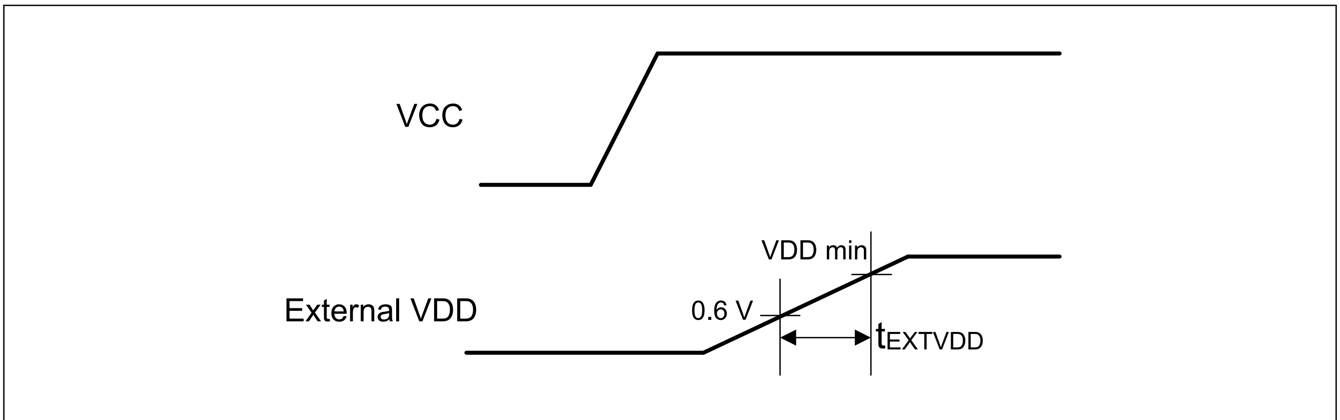


Figure 2.133 Power-up sequence of external VDD mode without using RES pin

2.11 Core Voltage Monitor Reset Characteristics

Table 2.106 Core voltage monitor reset characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Core voltage monitor reset (CVMR)		V_{det_VDDH}	1.05	1.10	1.15	V	Figure 2.134
			V_{det_VDDL}	0.55	0.58	0.61		
Internal reset time	Core voltage monitor reset time	DCDC mode	t_{CVM}	—	—	0.18	ms	
		External VDD mode		—	—	2.6		
Minimum VDD down /up time (CVMR)			t_{CVMOFF}	45	—	—	µs	
Response delay time (CVMR)			t_{CVMdet}	—	—	45	µs	
Hysteresis width (CVMR)			V_{CVMH}	—	0.225	—	V	

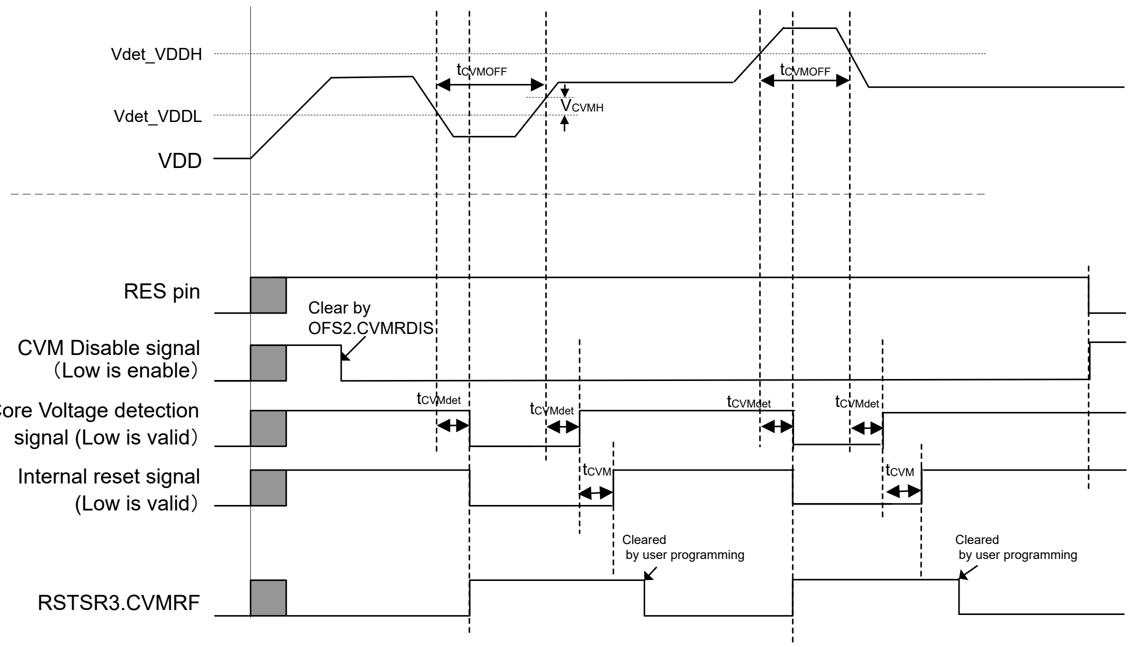


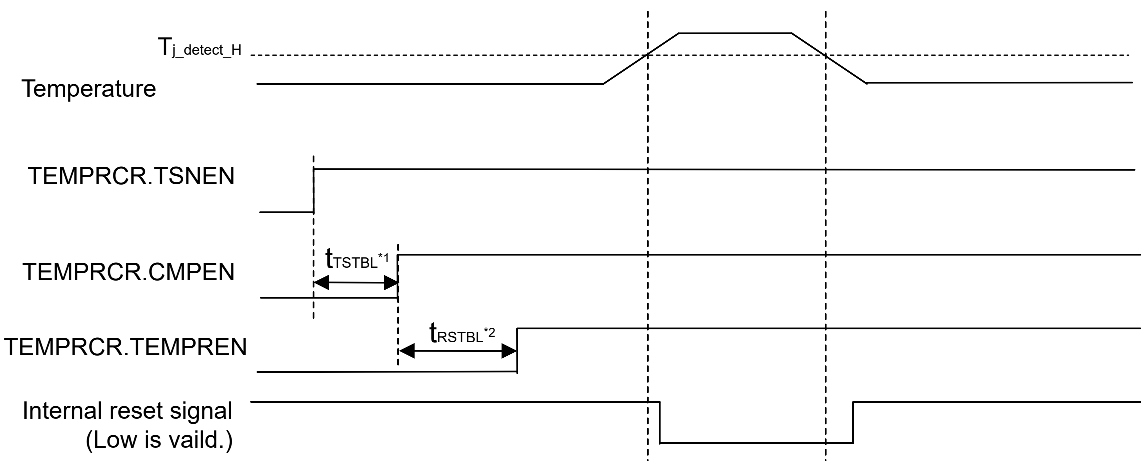
Figure 2.134 Timing of core voltage monitor reset

2.12 Temperature Monitor Reset Characteristics

Table 2.107 Temperature monitor reset characteristics

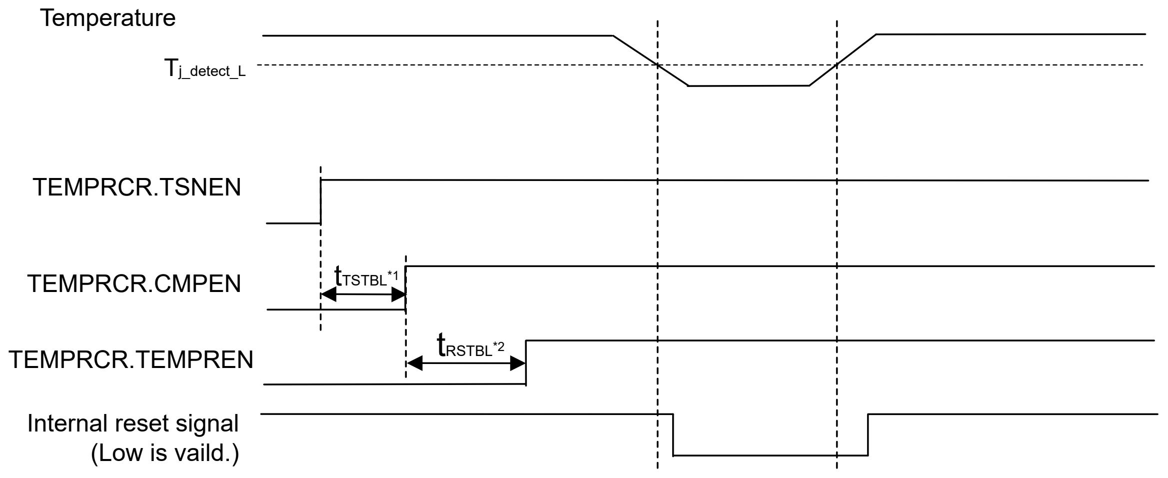
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
High threshold temperature	$T_{j\_detect\_H}$	105	—	125	°C	Figure 2.135 Figure 2.136
Low threshold temperature	$T_{j\_detect\_L}$	-40	—	-20	°C	

Note: Temperature monitor reset is not supported in 0 to 95 °C product (product group A).



Note 1. t_{TSTBL} is the stabilization wait time of TSN.
Note 2. t_{TSTBL} is the stabilization wait time of the comparator in TSN.

Figure 2.135 Timing of temperature monitor reset (High-temperature detection)



Note 1. t_{TSTBL} is the stabilization wait time of TSN.
Note 2. t_{TSTBL} is the stabilization wait time of the comparator in TSN.

Figure 2.136 Timing of temperature monitor reset (Low-temperature detection)

2.13 VBATT Characteristics

Table 2.108 Battery backup function characteristics (1 of 2)

Conditions: VCC = VCC_DCDC = VCC_USB = 1.62 to 3.63 V, VBATT = 1.62 to 3.63 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup OFS1.PVDAS and PVDLPSEL are 0 in Deep Software Standby mode 1, 2 (VDETVATT_n follows VDSEL[2:0] setting for PVD0)	$V_{DETBATT\_0}$	2.760	2.850	2.940	V	Figure 2.137
	$V_{DETBATT\_1}$	2.500	2.580	2.660		
	$V_{DETBATT\_2}$	2.080	2.150	2.220		
	$V_{DETBATT\_3}$	1.935	2.000	2.065		
	$V_{DETBATT\_4}$	1.840	1.900	1.960		
	$V_{DETBATT\_5}$	1.740	1.800	1.860		
	$V_{DETBATT\_6}$	1.620	1.670	1.730		
Voltage level for switching to battery backup (Other than above)	$V_{DETBATT\_0}$	2.710	2.800	2.890	V	
	$V_{DETBATT\_1}$	2.450	2.530	2.610		
	$V_{DETBATT\_2}$	2.030	2.100	2.170		
	$V_{DETBATT\_3}$	1.885	1.950	2.015		
	$V_{DETBATT\_4}$	1.790	1.850	1.910		
	$V_{DETBATT\_5}$	1.690	1.750	1.810		
VCC drop detection stabilization wait time*2	t_{DETWT}	—	—	20	µs	—
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	1.8	—	—	V	Figure 2.137
VCC-off period for starting power supply switching*1 (OFS1.PVDAS and PVDLPSEL are 0 in Deep Software Standby mode 1, 2)	$t_{VOFFBATT}$	25	—	—	µs	
VCC-off period for starting power supply switching*1 (Other than above)		25	—	—		

Table 2.108 Battery backup function characteristics (2 of 2)

Conditions: VCC = VCC_DCDC = VCC_USB = 1.62 to 3.63 V, VBATT = 1.62 to 3.63 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Backup domain power-down detection level	$V_{PDR\ (BATR)}$	1.43	1.47	1.52	V	Figure 2.138
Time delay in assertion of the reset signal for the backup domain*3	$t_{p\ (PDRL)}$	—	—	2000	μs	
Time delay in negation of the reset signal for the backup domain	$t_{p\ (PDRH)}$	—	—	3000		
VBATT monitor operation stabilization time (after VBATTMNSELR.VBTMNSEL is changed to 1)	t_{MONWT}	—	—	4.2	μs	—
VBATT voltage monitor level	$V_{MONBATT}$	—	VBATT / 6	—	V	—
VBATT current increase (when VBATTMNSELR.VBTTMNSEL is 1 compared to the case that VBATTMNSELR.VBTTMNSEL is 0)	$I_{VBATTSELB}$	—	1.35	2.00	μA	—
VCC current increase (when VBATTMNSELR.VBTTMNSEL is 1 compared to the case that VBATTMNSELR.VBTTMNSEL is 0)	$I_{VBATTSELC}$	—	15	25	μA	—

Note 1. The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).
In addition, this period indicates the time tVOFFP when VCC is below the minimum value of voltage detection levels V_{POR1}.

Note 2. Stable time when VBTBPCR2.VDETLVL is changed or VBTBPCR1. BPWSWSTP is changed from 1 to 0.

Note 3. When the VBATT_R recovers within this period, the backup domain reset signal may not be generated.

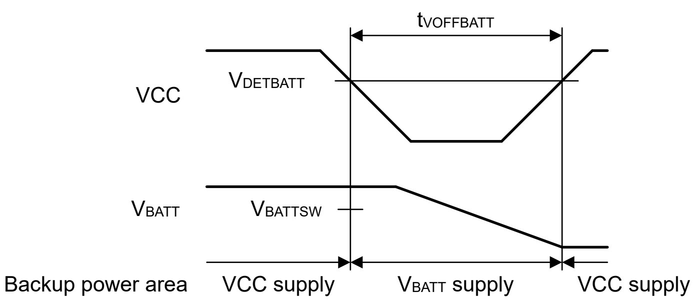


Figure 2.137 Battery backup function characteristics

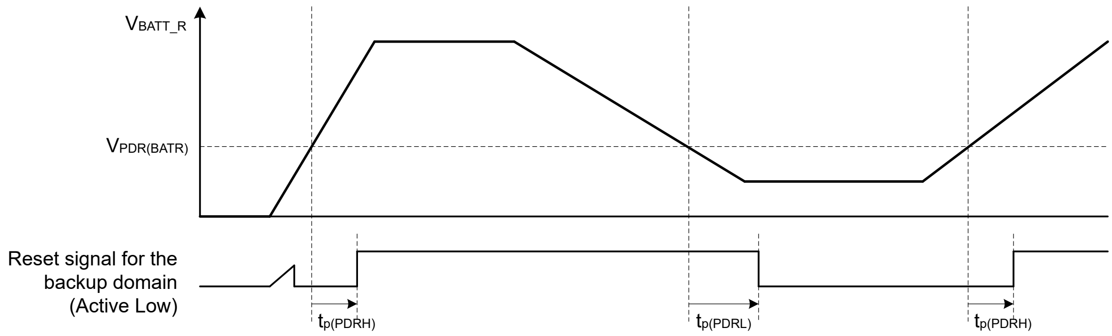


Figure 2.138 Backup domain reset characteristics

2.14 ACMPHS Characteristics

Table 2.109 ACMPHS

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range			VREF	0	—	AVCC0	V	—
Input voltage range	ACMPHS0, 1	IVCMP1 to IVCMP3	VI	0	—	AVCC0	V	—
		IVCMP0		0	—	AVCC0		VCC ≥ AVCC0
				0	—	VCC		VCC < AVCC0
	ACMPHS2, 3			0	—	AVCC0		—
Output delay*1			Td	—	50	100	ns	VI = VREF ± 100mV
Internal reference voltage			Vref	0.77	0.8	0.84	V	—

Note 1. This value is the internal propagation delay.

2.15 MRAM Characteristics

2.15.1 Code MRAM Characteristics

Table 2.110 Code MRAM Characteristics (1 of 2)

Parameter		Symbol	MRICLK = 250 MHz			MRICLK = 200 MHz			MRICLK = 150 MHz			MRICLK = 133 MHz			Unit	Test conditions
			Min	Typ *4	Max	Min	Typ *4	Max	Min	Typ *4	Max	Min	Typ *4	Max		
Programming time of 32-byte*7 *8	Normal program mode (MRPSC.MHSPEN = 0)	tPMC	—	6.7 *5 *6	83.3 *6	—	6.74 *5 *6	83.6 *6	—	6.92 *5 *6	85.6 *6	—	7.09 *5 *6	87.3 *6	μs	—
	High speed program mode (MRPSC.MHSPEN = 1)	tPMC	—	4.7 *5 *6	81.3 *6	—	4.74 *5 *6	81.6 *6	—	4.92 *5 *6	83.6 *6	—	5.09 *5 *6	85.3 *6	μs	—

Table 2.110 Code MRAM Characteristics (2 of 2)

Parameter	Symbol	MRICLK = 250 MHz			MRICLK = 200 MHz			MRICLK = 150 MHz			MRICLK = 133 MHz			Unit	Test conditions
		Min	Typ *4	Max	Min	Typ *4	Max	Min	Typ *4	Max	Min	Typ *4	Max		
Reprogramming cycle*9	N_{PC}	100000 *1	—	—	100000 *1	—	—	100000 *1	—	—	100000 *1	—	—	Times	—
Data hold time*2	t_{DRP}	10 *2 *3	—	—	10 *2 *3	—	—	10 *2 *3	—	—	10 *2 *3	—	—	Years	Tj = +125°C

Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.
Note 5. Perform rewrite 50% of bits at Typ. condition.
Note 6. If MRPCLK < 125MHz, add the time of MRPCLK 1cycle to the Program time.
Note 7. To calculate the updating time at other frequencies, using approximate formula below listed.
If MRPCLK < 125MHz, add 1/FMRPCLK [us] to the formula. (F_{MRICLK}: frequency of MRICLK [MHz], F_{MRPCLK}: frequency of MRPCLK [MHz])
t_{PMC} (Typ) = 137.8/F_{MRICLK} + 6.452 [μs], t_{PMC} (Max) = 1879/F_{MRICLK} + 78.75 [μs] for normal program mode.
t_{PMC} (Typ) = 137.8/F_{MRICLK} + 4.452 [μs], t_{PMC} (Max) = 1879/F_{MRICLK} + 76.75 [μs] for high speed program mode.
Note 8. Read and program operations for the code MRAM cannot be executed simultaneously. This value is for independent program operation without arbitration between read and program.
Note 9. The reprogramming cycle is the number of programming per 32-byte code MRAM address space. Programming the same data to the same address also increases the reprogramming cycle count by one. For a reprogramming cycle of n times (n = 100,000), programming can be performed n times for every 32-byte code MRAM address space.

2.15.2 Option Setting Memory (configuration area) Characteristics

Table 2.111 Option Setting Memory (configuration area) characteristics

Parameter		Symbol	MRPCLK = 125 MHz			MRPCLK = 100 MHz			MRPCLK = 75 MHz			MRPCLK = 66 MHz			Unit	Test conditions
			Min	Typ *4	Max	Min	Typ *4	Max	Min	Typ *4	Max	Min	Typ *4	Max		
Command time for configuration set*5 *6	Normal program mode (MRPSC.MHSPEN = 0)	t_{PCFG}	—	0.35	8.19	—	0.356	8.3	—	0.372	8.83	—	0.399	9.42	ms	—
	High speed program mode (MRPSC.MHSPEN = 1)		—	0.0665	7.85	—	0.0725	7.96	—	0.0882	8.5	—	0.0978	9.06	ms	—
Update cycle*7		N_{CUPC}	100000 *1	—	—	100000 *1	—	—	100000 *1	—	—	100000 *1	—	—	Times	—
Data hold time*2		t_{DRP}	10 *2 *3	—	—	10 *2 *3	—	—	10 *2 *3	—	—	10 *2 *3	—	—	Years	Tj = +125°C

Note 1. This is the minimum number of times to guarantee all the characteristics after update. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when update is performed within the specified range.
Note 3. This result is obtained from reliability testing.
Note 4. The reference value at VCC = 3.3 V and room temperature.
Note 5. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK}: frequency of MRPCLK [MHz])

t_{PCFG} (Typ) = 6.146/F_{MRPCLK} + 0.3133 [msec], t_{PCFG} (Max) = 266.5/F_{MRPCLK} + 6.331 [msec] for normal program mode.
t_{PCFG} (Typ) = 5.184/F_{MRPCLK} + 0.02754 [msec], t_{PCFG} (Max) = 267.5/F_{MRPCLK} + 6.025 [msec] for high speed program mode.

Note 6. Read and program operations for the extra MRAM cannot be executed simultaneously. This value is for independent program operation without arbitration between read and program.

Note 7. The update cycle is the number of a configuration set command that can be issued configuration area. Programming the same data to the same address also increases the update cycle count by one.

2.15.3 Option Setting Memory (OTP area with ECC) Characteristics

Table 2.112 Option setting memory (OTP area with ECC) characteristics

Parameter		Symbol	MRPCLK = 125 MHz			MRPCLK = 100 MHz			MRPCLK = 75 MHz			MRPCLK = 66 MHz			Unit	Test conditions
			Min	Typ *1	Max	Min	Typ *1	Max	Min	Typ *1	Max	Min	Typ *1	Max		
Programming time of 16-byte*3 *4	Normal speed write mode (MWMCR.MWM[1:0] = 00)	t_{OTPE}	—	8.05 *2	113	—	8.05 *2	113	—	8.05 *2	113	—	8.05 *2	113	ms	—
	High speed write mode 0 (MWMCR.MWM[1:0] = 01)		—	4.03 *2	56.7	—	4.03 *2	56.7	—	4.03 *2	56.7	—	4.03 *2	56.7	ms	—
	High speed write mode 1 (MWMCR.MWM[1:0] = 10)		—	0.229*2	3.14	—	0.229*2	3.14	—	0.229*2	3.14	—	0.229*2	3.14	ms	—

Note 1. The reference value at VCC = 3.3 V and room temperature.

Note 2. Perform rewrite 50% of bits at Typ. condition.

Note 3. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK}: frequency of MRPCLK [MHz])
t_{OTPE} (Typ) = 0.5065/F_{MRPCLK} + 8.123 [ms], t_{OTPE} (Max) = 4.433/F_{MRPCLK} + 114.1 [ms] for normal speed mode.
t_{OTPE} (Typ) = 0.3389/F_{MRPCLK} + 4.067 [ms], t_{OTPE} (Max) = 2.428/F_{MRPCLK} + 57.08 [ms] for high speed mode 0.
t_{OTPE} (Typ) = 0.1458/F_{MRPCLK} + 0.2312 [ms], t_{OTPE} (Max) = 0.3904/F_{MRPCLK} + 3.166 [ms] for high speed mode 1.

Note 4. Read and program operations for the extra MRAM cannot be executed simultaneously. This value is for independent program operation without arbitration between read and program.

2.15.4 Option Setting Memory (OTP area without ECC) Characteristics

Table 2.113 Option Setting Memory (OTP area without ECC) Characteristics

Parameter		Symbol	MRPCLK = 125 MHz			MRPCLK = 100 MHz			MRPCLK = 75 MHz			MRPCLK = 66 MHz			Unit	Test conditions
			Min	Typ*1	Max	Min	Typ*1	Max	Min	Typ*1	Max	Min	Typ*1	Max		
Programming time of 16-byte*3 *4	Normal speed write mode (MWMCR.MWM[1:0] = 00)	t_{OTPENE}	—	14.1*2	200	—	14.1*2	200	—	14.1*2	200	—	14.1*2	200	ms	—
	High speed write mode 0 (MWMCR.MWM[1:0] = 01)		—	7.07*2	100	—	7.07*2	100	—	7.07*2	100	—	7.07*2	100	ms	—
	High speed write mode 1 (MWMCR.MWM[1:0] = 10)		—	0.458*2	6.28	—	0.458*2	6.28	—	0.458*2	6.28	—	0.458*2	6.28	ms	—

Note 1. The reference value at VCC = 3.3 V and room temperature.
Note 2. Perform rewrite 50% of bits at Typ. condition.
Note 3. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK}: frequency of MRPCLK [MHz])
t_{OTPENE} (Typ) = 0.8486/F_{MRPCLK} + 14.25 [ms], t_{OTPENE} (Max) = 7.711/F_{MRPCLK} + 201.5 [ms] for normal speed mode.
t_{OTPENE} (Typ) = 0.5479/F_{MRPCLK} + 7.133 [ms], t_{OTPENE} (Max) = 4.148/F_{MRPCLK} + 100.8 [ms] for high speed mode 0.
t_{OTPENE} (Typ) = 0.2571/F_{MRPCLK} + 0.4627 [ms], t_{OTPENE} (Max) = 0.7401/F_{MRPCLK} + 6.333 [ms] for high speed mode 1.
Note 4. Read and program operations for the extra MRAM cannot be executed simultaneously. This value is for independent program operation without arbitration between read and program.

2.15.5 MACI Command Characteristics

Table 2.114 MACI command Characteristics

Parameter	Symbol	MRPCLK = 125 MHz			MRPCLK = 100 MHz			MRPCLK = 75 MHz			MRPCLK = 66 MHz			Unit	Test conditions
		Min	Typ*1	Max	Min	Typ*1	Max	Min	Typ*1	Max	Min	Typ*1	Max		
Command time for forced stop command*2	t_{FS}	—	—	3.35	—	—	3.38	—	—	3.47	—	—	3.7	μs	—
Command time for increment counter*2	t_{INCC}	—	0.252	1.61	—	0.252	1.61	—	0.252	1.61	—	0.252	1.61	ms	—
Command time for read counter*2	t_{RDC}	—	—	0.156	—	—	0.182	—	—	0.243	—	—	0.276	μs	—

Note 1. The reference value at VCC = 3.3 V and room temperature.
Note 2. To calculate the updating time at other frequencies, using approximate formula below listed. (F_{MRPCLK}: frequency of MRPCLK [MHz])
t_{FS} (Max) = 38.62/F_{MRPCLK} + 3.155 [us]
t_{INCC} (Typ) = 0.3348/F_{MRPCLK} + 0.2533 [msec], t_{INCC} (Max) = 0.8698/F_{MRPCLK} + 1.62 [msec]
t_{RDC} (Max) = 19.13/F_{MRPCLK} + 0.004099 [usec]

2.15.6 Zeroizing of W-HUK

Table 2.115 Zeroizing of W-HUK Characteristics

Parameter	Symbol	MRPCLK = 125 MHz			MRPCLK = 100 MHz			MRPCLK = 75 MHz			MRPCLK = 66 MHz			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Acton time of Zeroing of W-HUK*1	t_{ZWH}	—	—	793	—	—	793	—	—	793	—	—	793	ms	—

Note 1. To calculate the updating time at other frequencies, using approximate formula below listed. (FMRPCLK: frequency of MRPCLK [MHz])
t_{ZWH} (Max) = 34.52/FMRPCLK + 799 [μs]

2.15.7 MRAM Magnetic Field Immunity Characteristics

Table 2.116 MRAM Magnetic field Immunity Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Operation	Write state	G_{max_wr}	—	—	200	Gauss	—
	Read state	G_{max_rd}	—	—	200	Gauss	—
	No access state	G_{max_noac}	—	—	500	Gauss	—
Storage		G_{max_stg}	—	—	500	Gauss	The applied temperature is T_{stg}.

2.16 Boundary Scan

Table 2.117 Boundary scan characteristics (1 of 2)

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	1.62 V or above	t_{TCKcyc}	100	—	—	ns	Figure 2.139
TCK clock high pulse width	1.62 V or above	t_{TCKH}	0.45	—	—	t_{TCKcyc}	
TCK clock low pulse width	1.62 V or above	t_{TCKL}	0.45	—	—	t_{TCKcyc}	
TCK clock rise time	1.62 V or above	t_{TCKr}	—	—	0.05*2	t_{TCKcyc}	
TCK clock fall time	1.62 V or above	t_{TCKf}	—	—	0.05*2	t_{TCKcyc}	
TMS setup time	1.62 V or above	t_{TMSS}	20	—	—	ns	Figure 2.140
TMS hold time	1.62 V or above	t_{TMSH}	20	—	—	ns	
TDI setup time	1.62 V or above	t_{TDIS}	20	—	—	ns	
TDI hold time	1.62 V or above	t_{TDIH}	20	—	—	ns	
TDO data delay	1.62 V or above	t_{TDOD}	—	—	40	ns	

Table 2.117 Boundary scan characteristics (2 of 2)

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
Capture register setup time	1.62 V or above	t_{CAPTS}	20	—	—	ns	Figure 2.141
Capture register hold time	1.62 V or above	t_{CAPTH}	20	—	—	ns	
Update register delay time	1.62 V or above	$t_{UPDATED}$	—	—	40	ns	
Boundary scan circuit startup time*1	1.62 V or above	T_{BSSTUP}	t_{RESWP}	—	—	—	Figure 2.142

Note 1. Boundary scan does not function until the power-on reset becomes negative.
Note 2. 1 μs at the longest

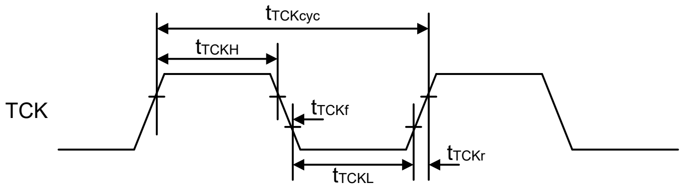


Figure 2.139 Boundary scan TCK timing

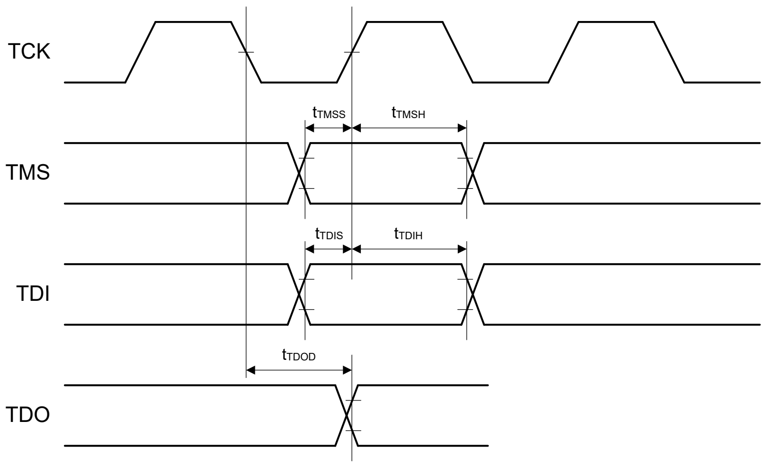


Figure 2.140 Boundary scan input/output timing (1)

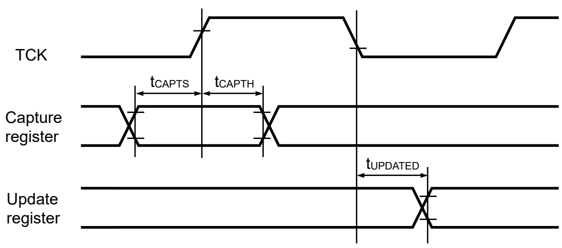


Figure 2.141 Boundary scan input/output timing (2)

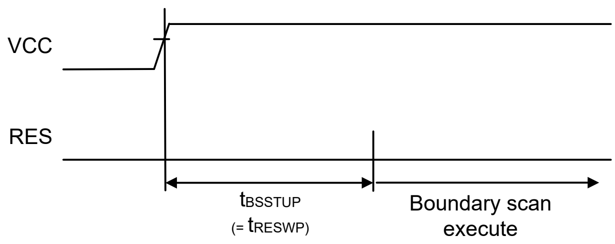


Figure 2.142 Boundary scan circuit startup timing

2.17 Joint European Test Action Group (JTAG)

Table 2.118 JTAG (1 of 2)

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	2.7 V or above	t_{TCKcyc}	40.0	—	—	ns	Figure 2.143
	1.62 V or above		40.0	—	—	ns	
TCK clock high pulse width	2.7 V or above	t_{TCKH}	0.375	—	—	t_{TCKcyc}	
	1.62 V or above		0.375	—	—	t_{TCKcyc}	
TCK clock low pulse width	2.7 V or above	t_{TCKL}	0.375	—	—	t_{TCKcyc}	
	1.62 V or above		0.375	—	—	t_{TCKcyc}	
TCK clock rise time	2.7 V or above	t_{TCKr}	—	—	0.125*1	t_{TCKcyc}	
	1.62 V or above		—	—	0.125*1	t_{TCKcyc}	
TCK clock fall time	2.7 V or above	t_{TCKf}	—	—	0.125*1	t_{TCKcyc}	
	1.62 V or above		—	—	0.125*1	t_{TCKcyc}	

Table 2.118 JTAG (2 of 2)

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	2.7 V or above	t_{TMSS}	8.0	—	—	ns	Figure 2.144
	1.62 V or above		8.0	—	—	ns	
TMS hold time	2.7 V or above	t_{TMSH}	8.0	—	—	ns	
	1.62 V or above		8.0	—	—	ns	
TDI setup time	2.7 V or above	t_{TDIS}	8.0	—	—	ns	
	1.62 V or above		8.0	—	—	ns	
TDI hold time	2.7 V or above	t_{TDIH}	8.0	—	—	ns	
	1.62 V or above		8.0	—	—	ns	
TDO data delay time	2.7 V or above	t_{TDOD}	—	—	20.0	ns	
	1.62 V or above		—	—	28.0	ns	

Note 1. 1 μs at the longest

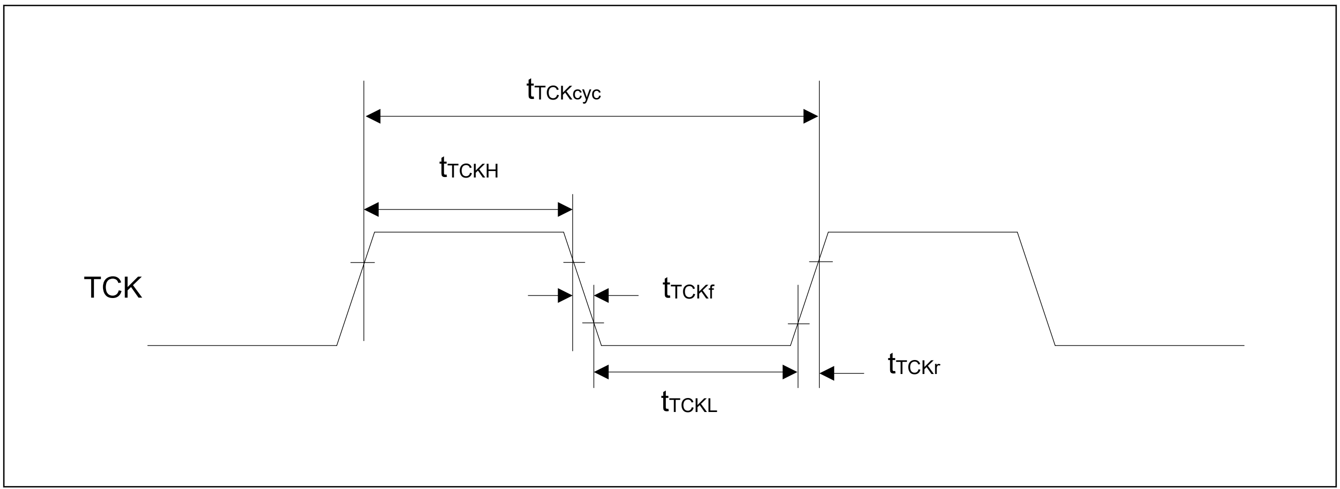


Figure 2.143 JTAG TCK timing

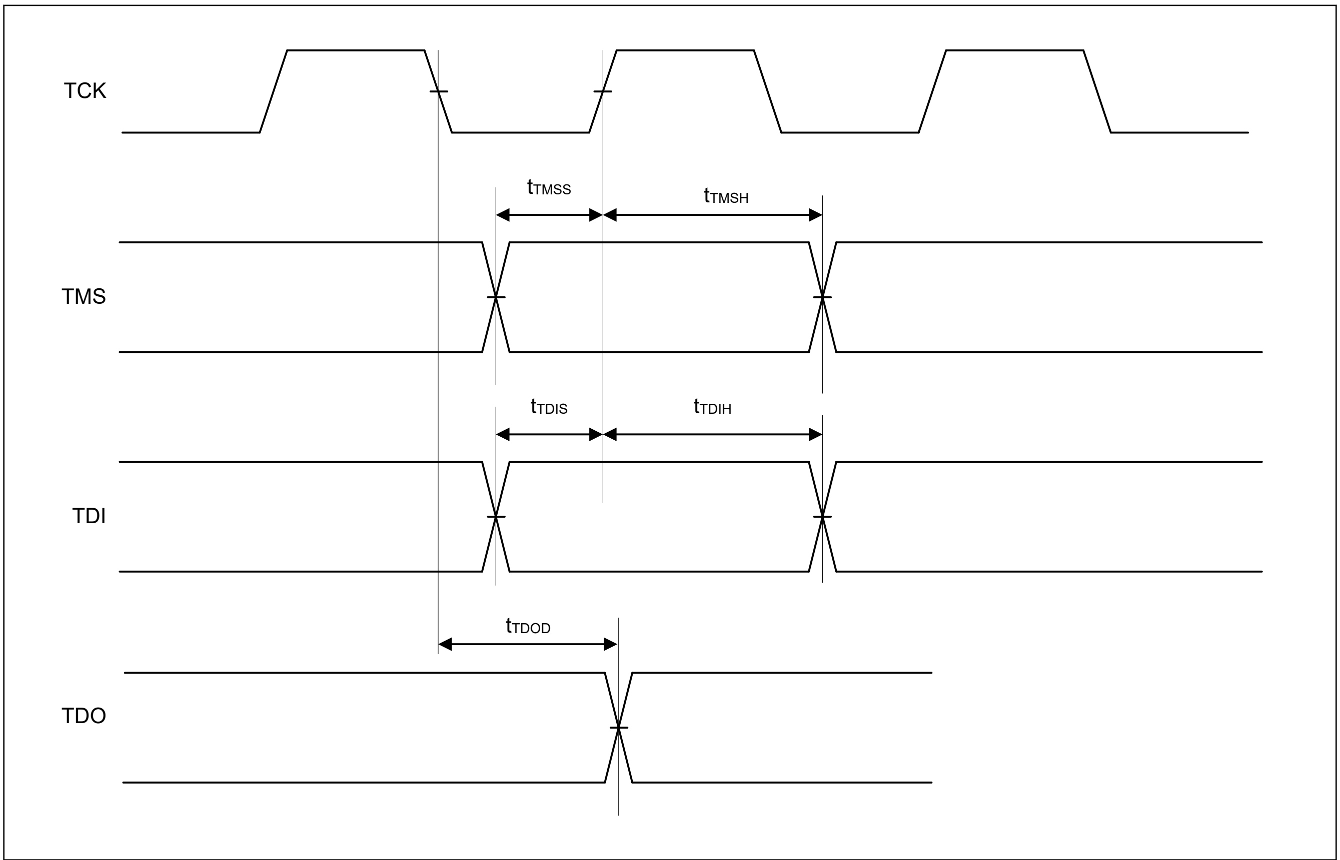


Figure 2.144 JTAG input/output timing

2.18 Serial Wire Debug (SWD)

Table 2.119 SWD (1 of 2)

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	2.7 V or above	$t_{SWCKcyc}$	40.0	—	—	ns	Figure 2.145
	1.62 V or above		40.0	—	—	ns	
SWCLK clock high pulse width	2.7 V or above	t_{SWCKH}	0.375	—	—	$t_{SWCKcyc}$	
	1.62 V or above		0.375	—	—	$t_{SWCKcyc}$	
SWCLK clock low pulse width	2.7 V or above	t_{SWCKL}	0.375	—	—	$t_{SWCKcyc}$	
	1.62 V or above		0.375	—	—	$t_{SWCKcyc}$	
SWCLK clock rise time	2.7 V or above	t_{SWCKr}	—	—	0.125*1	$t_{SWCKcyc}$	
	1.62 V or above		—	—	0.125*1	$t_{SWCKcyc}$	
SWCLK clock fall time	2.7 V or above	t_{SWCKf}	—	—	0.125*1	$t_{SWCKcyc}$	
	1.62 V or above		—	—	0.125*1	$t_{SWCKcyc}$	

Table 2.119 SWD (2 of 2)

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
SWDIO setup time	2.7 V or above	t_{SWDS}	8.0	—	—	ns	Figure 2.146
	1.62 V or above		8.0	—	—	ns	
SWDIO hold time	2.7 V or above	t_{SWDH}	8.0	—	—	ns	
	1.62 V or above		8.0	—	—	ns	
SWDIO data delay time	2.7 V or above	t_{SWDD}	2.0	—	28.0	ns	
	1.62 V or above		2.0	—	32.0	ns	

Note 1. 1 µs at the longest

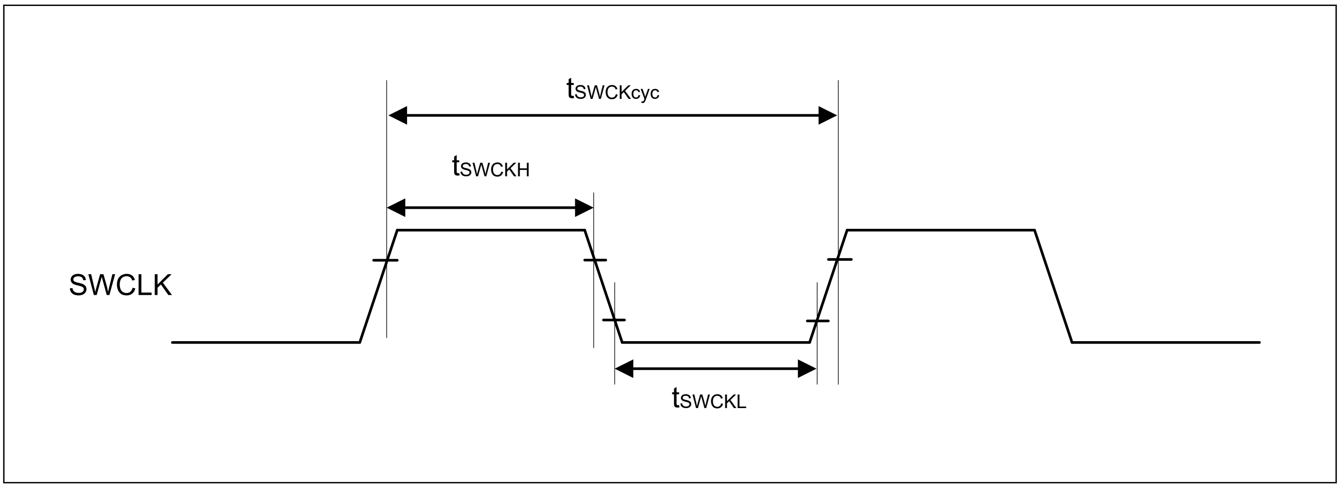


Figure 2.145 SWD SWCLK timing

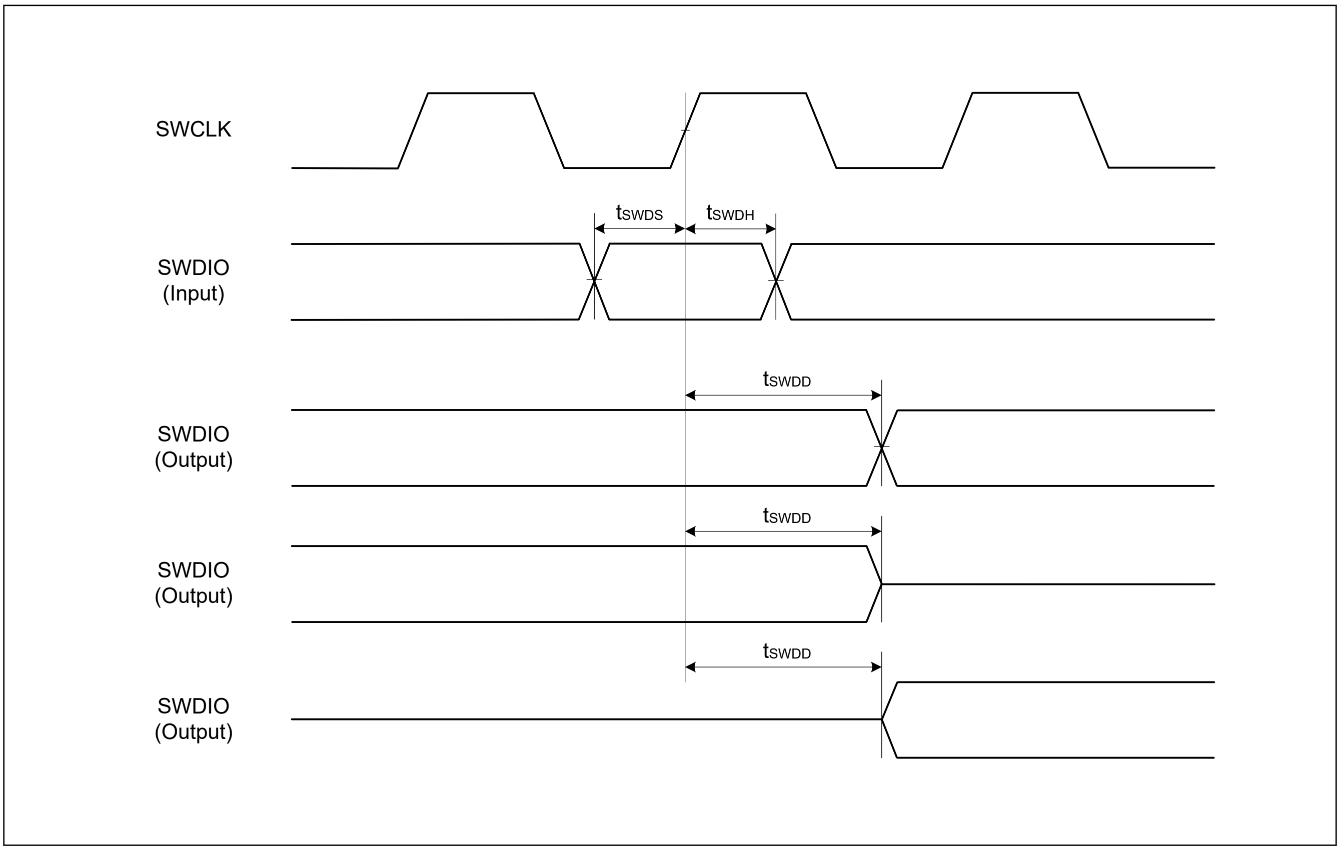


Figure 2.146 SWD input/output timing

2.19 Embedded Trace Macro Interface (ETM)

Table 2.120 ETM (1 of 2)

Conditions: High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	2.7 V or above	$t_{TCLKcyc}$	16	—	—	ns	Figure 2.147
	1.62 V or above		16	—	—	ns	
TCLK clock high pulse width	2.7 V or above	t_{TCLKH}	7	—	—	ns	
	1.62 V or above		6	—	—	ns	
TCLK clock low pulse width	2.7 V or above	t_{TCLKL}	7	—	—	ns	
	1.62 V or above		6	—	—	ns	
TCLK clock rise time	2.7 V or above	t_{TCLKr}	—	—	1.0	ns	
	1.62 V or above		—	—	2.0	ns	
TCLK clock fall time	2.7 V or above	t_{TCLKf}	—	—	1.0	ns	
	1.62 V or above		—	—	2.0	ns	

Table 2.120 ETM (2 of 2)

Conditions: High-speed high drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter	VCC	Symbol	Min	Typ	Max	Unit	Test conditions
TDATA[3:0] output valid time	2.7 V or above	t_{TRDV}	—	—	$t_{TCLKcyc}$/4 + 1.5	ns	Figure 2.148
	1.62 V or above		—	—	$t_{TCLKcyc}$/4 + 1.5	ns	
TDATA[3:0] output hold time	2.7 V or above	t_{TRDH}	1.5	—	—	ns	
	1.62 V or above		1.5	—	—	ns	

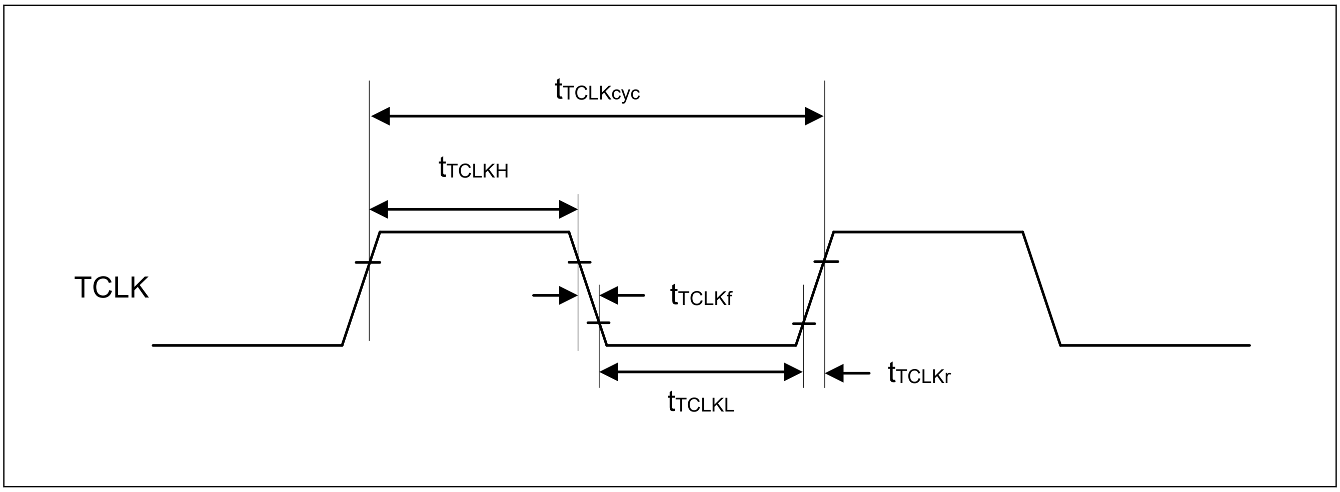


Figure 2.147 ETM TCLK timing

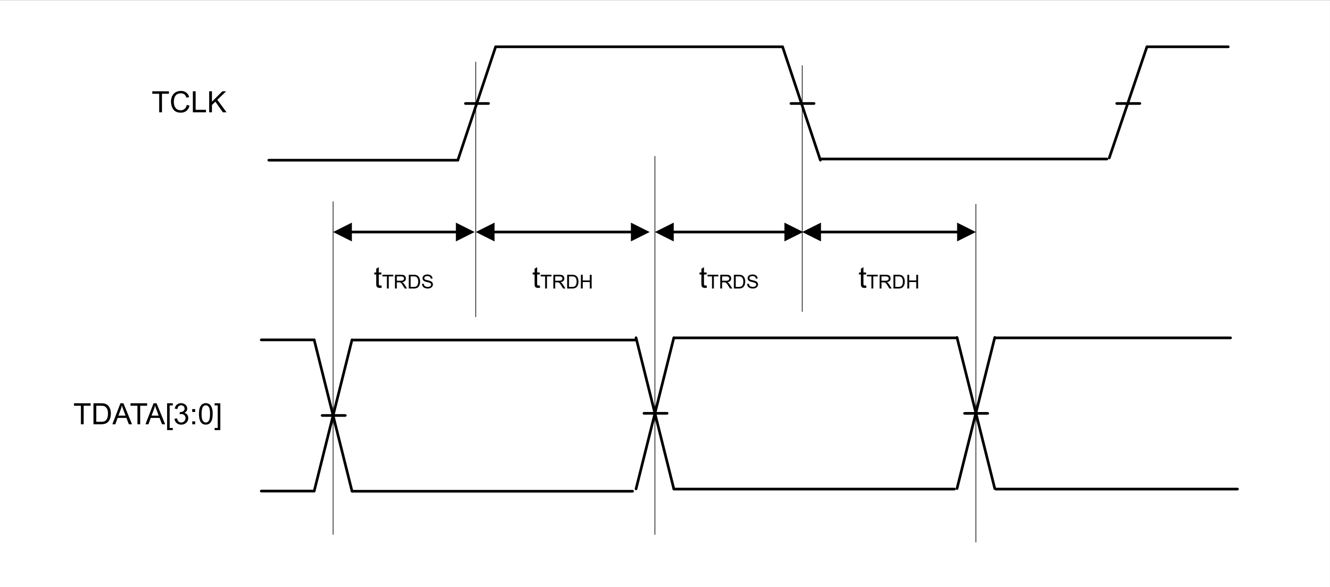


Figure 2.148 ETM output timing

Appendix 1. Port States in Each Processing Mode

Function	Pin function	Reset	Software Standby mode (SSTBY)		Deep Software Standby mode 1, 2, 3 (DSTBY1, 2, 3)		After Deep Software Standby mode is canceled (return to startup mode)	
			OPE = 0	OPE = 1	DSTBY1	DSTBY2/ DSTBY3	IOKEEP = 0	IOKEEP = 1[*1]
Mode	MD	Pull-up	Keep-I		Keep		Pull-up	Keep
JTAG/SWD	TCK/TMS/TDI/SWCLK	Pull-up	TCK/TDI/TMS/SWCLK input		TCK/TDI/TMS/SWCLK input		TCK/TDI/TMS/SWCLK input	
	TDO	Output	TDO output		TDO output		TDO output	
	SWDIO	Pull-up	SWDIO inout		SWDIO inout		SWDIO inout	
Trace	TCLK/TDATAx/SWO	TCLK/ TDATAx/SWO output	TCLK/TDATAx/SWO output		TCLK/TDATAx/SWO output		TCLK/TDATAx/SWO output	
IRQ	IRQx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	IRQx-DS (x: Other than 5)	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	Keep
	IRQ5-DS	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	
AGT	AGTIOn	Hi-Z	AGTIOn inout		Keep		Hi-Z	Keep
	AGTOn/AGTOAn/ AGTOBn	Hi-Z	AGTOn/AGTOAn/AGTOBn output		Keep		Hi-Z	Keep
ULPT	ULPTEEn/ULPTEVIn	Hi-Z	ULPTEEn/ULPTEVIn input		Keep		Hi-Z	Keep
	ULPTEEn-DS/ ULPTEVIn-DS	Hi-Z	ULPTEEn-DS/ULPTEVIn-DS input		ULPTEEn-DS/ ULPTEVIn-DS input	Hi-Z	Hi-Z	Keep
	ULPTOn/ ULPTOAn/ ULPTOBn	Hi-Z	ULPTOn/ULPTOAn/ULPTOBn output		Keep		Hi-Z	Keep
	ULPTOn-DS/ ULPTOAn-DS/ ULPTOBn-DS	Hi-Z	ULPTOn/ULPTOAn-DS/ ULPTOBn-DS output		ULPTOn/ULPTOAn-DS/ ULPTOBn-DS output	Keep	Hi-Z	From DSTBY1: ULPTOn/ ULPTOAn-DS/ ULPTOBn-DS output From DSTBY1, 2: Keep
IIC	SCLn/SDAn	Hi-Z	Keep-O[*2]		Keep		Hi-Z	Keep
I3C	I3C_SCL0/I3C_SDA0	Hi-Z	Keep-O[*2]		Hi-Z		Hi-Z	
USBFS	USB_OVRCURx	Hi-Z	Hi-Z[*2]		Keep		Hi-Z	Keep
	USB_OVRCURx-DS/ USB_VBUS	Hi-Z	Hi-Z[*2]		Keep[*3]	Keep	Hi-Z	Keep
	USB_DP/USB_DM	Hi-Z	Keep-O[*4]		Keep[*3]	Keep	Hi-Z	Keep
RTC	RTCICx	Hi-Z	Hi-Z[*2]		Keep[*3]		Hi-Z	Keep
	RTCOUT	Hi-Z	RTCOUT output		Keep		Hi-Z	Keep
ACMPHS	VCOUT	Hi-Z	VCOUT output		Keep		Hi-Z	Keep
CLKOUT	CLKOUT	Hi-Z	CLKOUT output		Keep		Hi-Z	Keep
DAC	DAn	Hi-Z	D/A output retained		Keep		Hi-Z	Keep
External bus (CS, SDRAM area)	EBCLK/SDCLK	Hi-Z	High-level output		Keep		Hi-Z	Keep
	Dxx/DQxx	Hi-Z	Hi-Z		Hi-Z		Hi-Z	
	Axx/DQMx	Hi-Z	Hi-Z	Keep-O	Keep		Hi-Z	Keep
	BCx/CSx/RD/WRx/WE	Hi-Z	Hi-Z	High-level output	Keep		Hi-Z	Keep
	ALE	Hi-Z	Hi-Z	Low-level output	Keep		Hi-Z	Keep
	CKE/SDCS/RAS/CAS	Hi-Z	Hi-Z	SDSELF.SFEN = 0: High-level output SDSELF.SFEN = 1: Low-level output	Keep		Hi-Z	Keep
P400/P401	Other than function IRQ5-DS	Hi-Z	Keep-O[*2]		Hi-Z		Hi-Z	
Others	—	Hi-Z	Keep-O		Keep		Hi-Z	Keep

Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep-I: Pin states are retained the same as during periods in Normal mode.

Keep: Pin states are retained the same as during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.

Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.

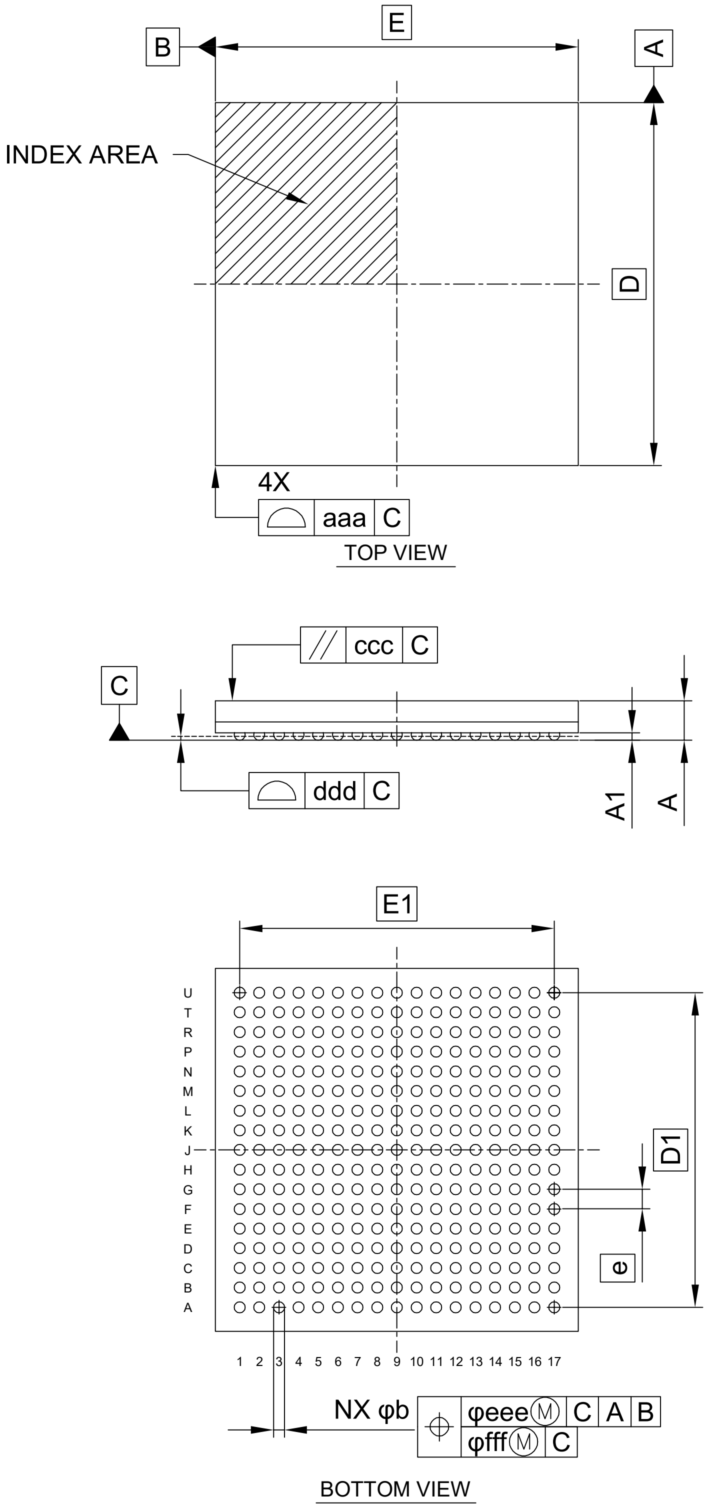
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.

Note 4. Input is enabled while the pin is used as an input pin.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

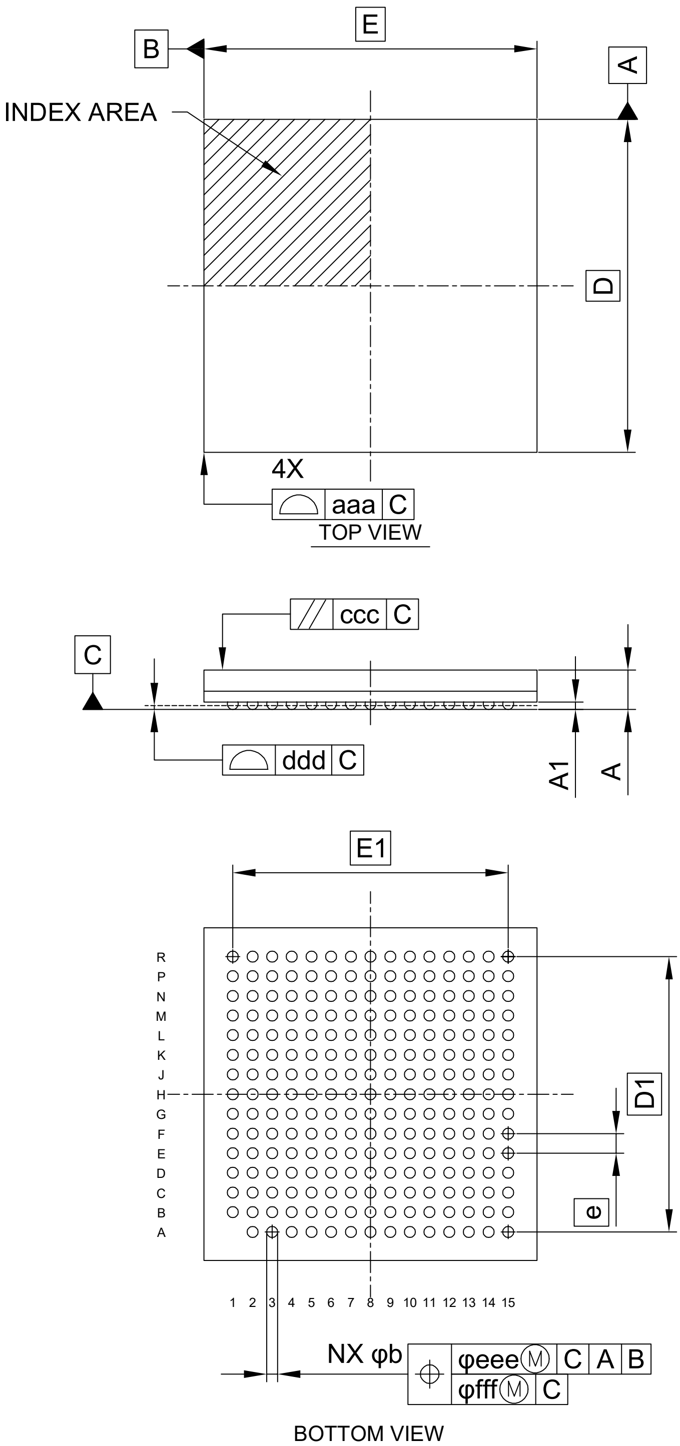
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA289-12x12-0.65	PLBG0289JA-A	0.38



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	12.00	—
E	—	12.00	—
D1	—	10.40	—
E1	—	10.40	—
A	—	—	1.38
A1	0.20	—	—
b	0.31	0.36	0.41
e	—	0.65	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.10
eee	—	—	0.15
fff	—	—	0.08
N	—	289	—

Figure A2.1 BGA 289-pin

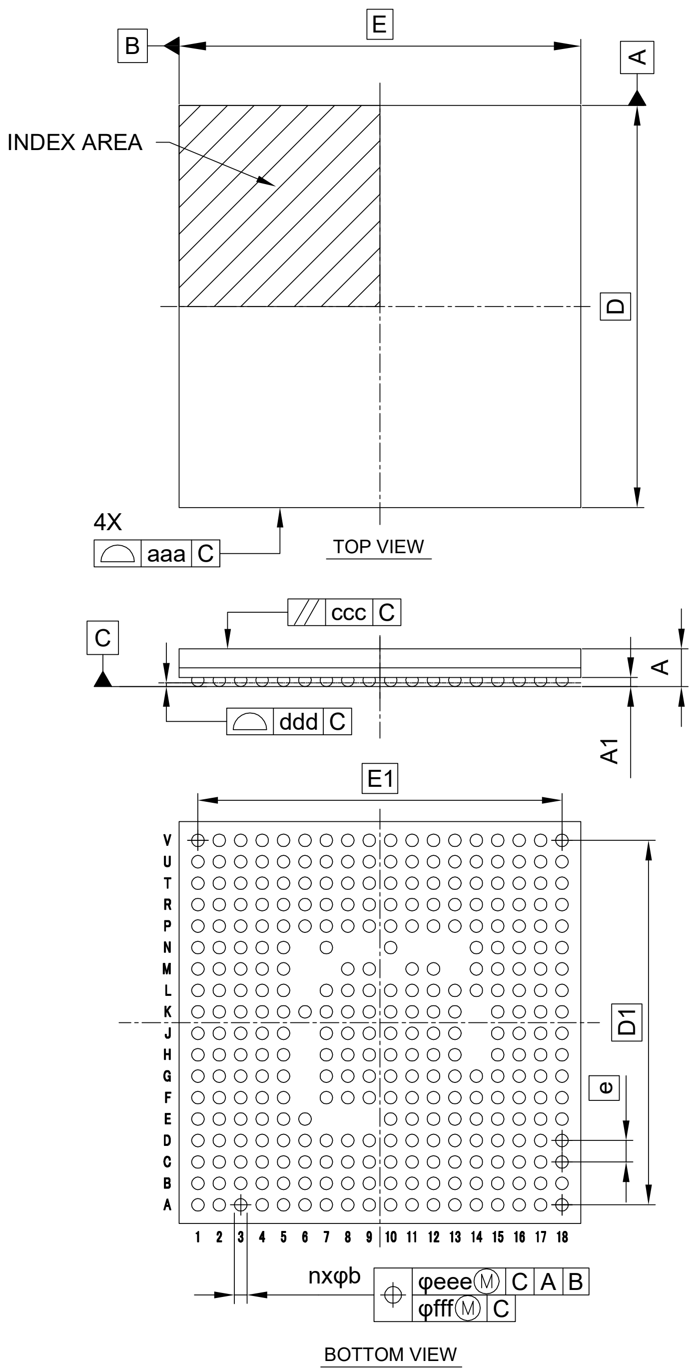
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA224-11x11-0.65	PLBG0224JA-A	0.32



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	11.00	—
E	—	11.00	—
D1	—	9.10	—
E1	—	9.10	—
A	—	—	1.38
A1	0.20	—	—
b	0.31	0.36	0.41
e	—	0.65	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.10
eee	—	—	0.15
fff	—	—	0.08
N	—	224	—

Figure A2.2 BGA 224-pin

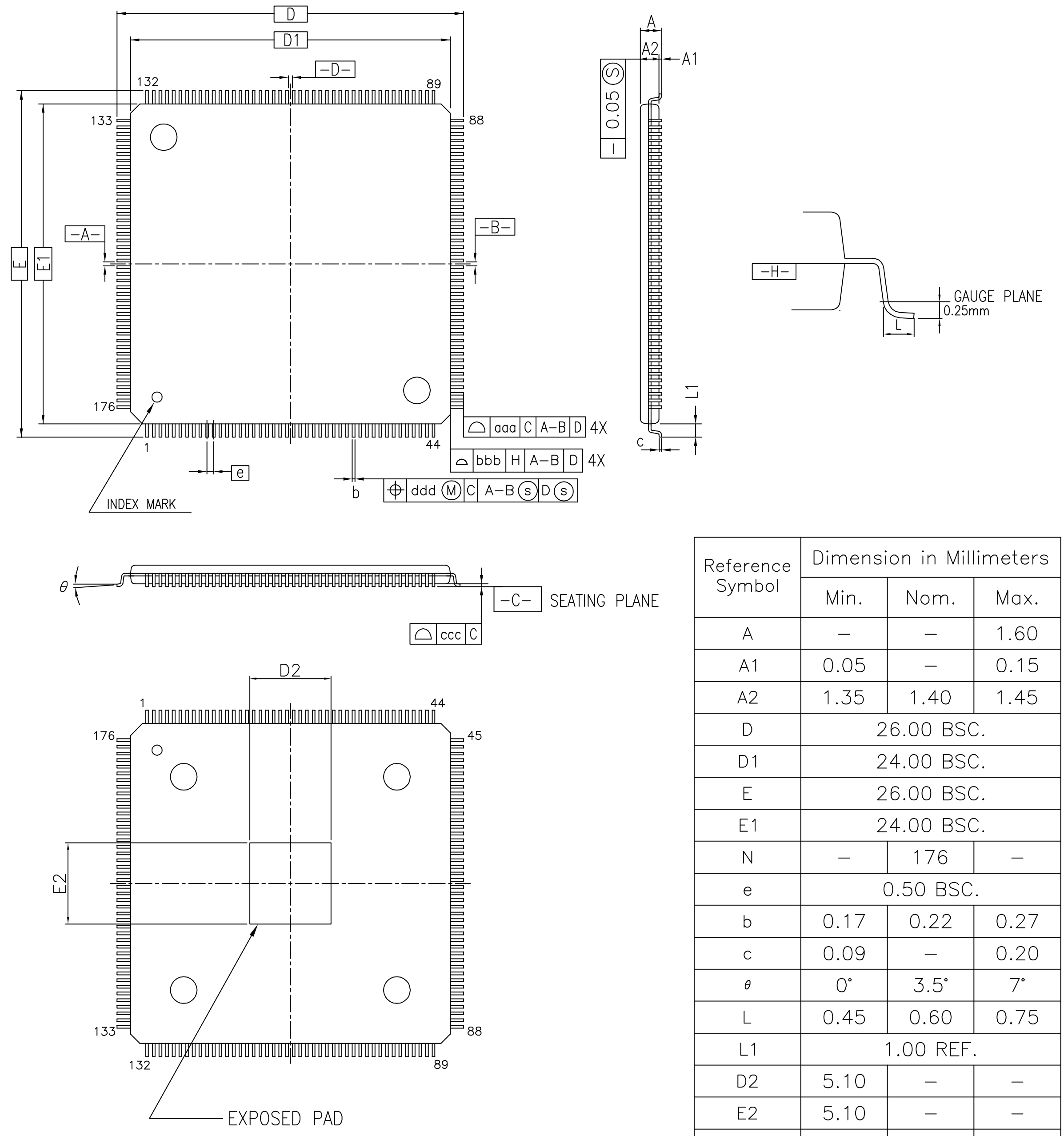
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA303-15x15-0.80	PLBG0303GA-A	0.63



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	15.00	—
E	—	15.00	—
D1	—	13.60	—
E1	—	13.60	—
A	—	—	1.50
A1	0.29	—	—
b	0.42	0.47	0.52
e	—	0.80	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.20
eee	—	—	0.15
fff	—	—	0.08
N	—	303	—

Figure A2.3 BGA 303-pin

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HLQFP176-24x24-0.50	PLQP0176KK-A	1.90



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
D	26.00 BSC.		
D1	24.00 BSC.		
E	26.00 BSC.		
E1	24.00 BSC.		
N	–	176	–
e	0.50 BSC.		
b	0.17	0.22	0.27
c	0.09	–	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		
D2	5.10	–	–
E2	5.10	–	–
aaa	–	–	0.20
bbb	–	–	0.20
ccc	–	–	0.08
ddd	–	–	0.08

Figure A2.4 HLQFP 176-pin

Appendix 3. I/O Registers

This appendix describes I/O register address and access cycles by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual. Table A3.1 shows the name, description, and the base address of each peripheral.

Table A3.1 Peripheral base address (1 of 4)

Description	Name of secure registers	Base address of secure registers in secure alias region	Name of non-secure registers	Base address of non-secure registers in non-secure alias region
Renesas Memory Protection Unit	RMPU	0x4000_0000	RMPU_NS	0x5000_0000
SRAM Control	SRAM	0x4000_2000	SRAM_NS	0x5000_2000
BUS Control	BUS	0x4000_3000	BUS_NS	0x5000_3000
Common Interrupt Controller	ICU_COMMON	0x4000_6000	ICU_COMMON_NS	0x5000_6000
CPU System Security Control Unit	CPSCU	0x4000_8000	CPSCU_NS	0x5000_8000
Direct Memory Access Controller 00	DMAC00	0x4000_A000	DMAC00_NS	0x5000_A000
Direct Memory Access Controller 01	DMAC01	0x4000_A040	DMAC01_NS	0x5000_A040
Direct Memory Access Controller 02	DMAC02	0x4000_A080	DMAC02_NS	0x5000_A080
Direct Memory Access Controller 03	DMAC03	0x4000_A0C0	DMAC03_NS	0x5000_A0C0
Direct Memory Access Controller 04	DMAC04	0x4000_A100	DMAC04_NS	0x5000_A100
Direct Memory Access Controller 05	DMAC05	0x4000_A140	DMAC05_NS	0x5000_A140
Direct Memory Access Controller 06	DMAC06	0x4000_A180	DMAC06_NS	0x5000_A180
Direct Memory Access Controller 07	DMAC07	0x4000_A1C0	DMAC07_NS	0x5000_A1C0
DMAC Module Activation 0	DMA0	0x4000_A800	DMA0_NS	0x5000_A800
Data Transfer Controller 0	DTC0	0x4000_AC00	DTC0_NS	0x5000_AC00
Interrupt Controller	ICU	0x4000_C000	ICU_NS	0x5000_C000
CPU Control Registers	CPU_CTRL	0x4000_F000	CPU_CTRL_NS	0x5000_F000
On-Chip Debug	CPU_OCD	0x4001_1000	CPU_OCD_NS	0x5001_1000
Debug Function	CPU_DBG	0x4001_B000	CPU_DBG_NS	0x5001_B000
CACHE	CACHE	0x4001_C000	CACHE_NS	0x5001_C000
TCM	TCM	0x4001_C800	TCM_NS	0x5001_C800
System Control	SYSC	0x4001_E000	SYSC_NS	0x5001_E000
Inter-Processor Communication	IPC	0x4002_0000	IPC_NS	0x5002_0000
Temperature Sensor Data	TSD	0x02C1_EDA0	TSD_NS	0x12C1_EDA0
MRAM System Register area	MRAM	0x4013_C000	MRAM_NS	0x5013_C000
Event Link Controller	ELC	0x4020_1000	ELC_NS	0x5020_1000
Realtime Clock	RTC	0x4020_2000	RTC_NS	0x5020_2000
Independent Watchdog Timer	IWDT	0x4020_2200	IWDT_NS	0x5020_2200
Clock Frequency Accuracy Measurement Circuit	CAC	0x4020_2400	CAC_NS	0x5020_2400
Watchdog Timer 0	WDT0	0x4020_2600	WDT0_NS	0x5020_2600
Watchdog Timer 1	WDT1	0x4020_2700	WDT1_NS	0x5020_2700
Module Stop Control A, B, C, D, E	MSTP	0x4020_3000	MSTP_NS	0x5020_3000

Table A3.1 Peripheral base address (2 of 4)

Description	Name of secure registers	Base address of secure registers in secure alias region	Name of non-secure registers	Base address of non-secure registers in non-secure alias region
Peripheral Security Control Unit	PSCU	0x4020_4000	PSCU_NS	0x5020_4000
Port Output Enable Module for GPT	POEG	0x4021_2000	POEG_NS	0x5021_2000
Ultra-Low Power Timer 0	ULPT0	0x4022_0000	ULPT0_NS	0x5022_0000
Ultra-Low Power Timer 1	ULPT1	0x4022_0100	ULPT1_NS	0x5022_0100
Low Power Asynchronous General Purpose Timer 0	AGT0	0x4022_1000	AGT0_NS	0x5022_1000
Low Power Asynchronous General Purpose Timer 1	AGT1	0x4022_1100	AGT1_NS	0x5022_1100
12-bit D/A Converter 0	DAC120	0x4023_3000	DAC120_NS	0x5023_3000
12-bit D/A Converter 1	DAC121	0x4023_3100	DAC121_NS	0x5023_3100
Temperature Sensor	TSN	0x4023_5000	TSN_NS	0x5023_5000
High-Speed Analog Comparator 0	ACMPHS0	0x4023_6000	ACMPHS0_NS	0x5023_6000
High-Speed Analog Comparator 1	ACMPHS1	0x4023_6100	ACMPHS1_NS	0x5023_6100
High-Speed Analog Comparator 2	ACMPHS2	0x4023_6200	ACMPHS2_NS	0x5023_6200
High-Speed Analog Comparator 3	ACMPHS3	0x4023_6300	ACMPHS3_NS	0x5023_6300
USB 2.0 FS Module	USBFS	0x4025_0000	USBFS_NS	0x5025_0000
SD Host Interface 0	SDHI0	0x4025_2000	SDHI0_NS	0x5025_2000
SD Host Interface 1	SDHI1	0x4025_2400	SDHI1_NS	0x5025_2400
Inter-Integrated Circuit 0	IIC0	0x4025_E000	IIC0_NS	0x5025_E000
Inter-Integrated Circuit 0 Wake-up Unit	IIC0WU	0x4025_E014	IIC0WU_NS	0x5025_E014
Inter-Integrated Circuit 1	IIC1	0x4025_E100	IIC1_NS	0x5025_E100
Inter-Integrated Circuit 2	IIC2	0x4025_E200	IIC2_NS	0x5025_E200
Octal Serial Peripheral Interface 0	OSPI0_B	0x4026_8000	OSPI0_B_NS	0x5026_8000
Octal Serial Peripheral Interface 1	OSPI1_B	0x4026_8400	OSPI1_B_NS	0x5026_8400
Decryption On-The-Fly 0	DOTF0	0x4026_8800	DOTF0_NS	0x5026_8800
Decryption On-The-Fly 1	DOTF1	0x4026_8900	DOTF1_NS	0x5026_8900
CRC Calculator	CRC	0x4031_0000	CRC_NS	0x5031_0000
Data Operation Circuit	DOC_B	0x4031_1000	DOC_B_NS	0x5031_1000
General PWM 32-bit Timer 0	GPT320	0x4032_2000	GPT320_NS	0x5032_2000
General PWM 32-bit Timer 1	GPT321	0x4032_2100	GPT321_NS	0x5032_2100
General PWM 32-bit Timer 2	GPT322	0x4032_2200	GPT322_NS	0x5032_2200
General PWM 32-bit Timer 3	GPT323	0x4032_2300	GPT323_NS	0x5032_2300
General PWM 32-bit Timer 4	GPT324	0x4032_2400	GPT324_NS	0x5032_2400
General PWM 32-bit Timer 5	GPT325	0x4032_2500	GPT325_NS	0x5032_2500
General PWM 32-bit Timer 6	GPT326	0x4032_2600	GPT326_NS	0x5032_2600
General PWM 32-bit Timer 7	GPT327	0x4032_2700	GPT327_NS	0x5032_2700
General PWM 32-bit Timer 8	GPT328	0x4032_2800	GPT328_NS	0x5032_2800
General PWM 32-bit Timer 9	GPT329	0x4032_2900	GPT329_NS	0x5032_2900
General PWM 32-bit Timer 10	GPT3210	0x4032_2A00	GPT3210_NS	0x5032_2A00

Table A3.1 Peripheral base address (3 of 4)

Description	Name of secure registers	Base address of secure registers in secure alias region	Name of non-secure registers	Base address of non-secure registers in non-secure alias region
General PWM 32-bit Timer 11	GPT3211	0x4032_2B00	GPT3211_NS	0x5032_2B00
General PWM 32-bit Timer 12	GPT3212	0x4032_2C00	GPT3212_NS	0x5032_2C00
General PWM 32-bit Timer 13	GPT3213	0x4032_2D00	GPT3213_NS	0x5032_2D00
Output Phase Switching Controller	GPT_OPS	0x4032_3F00	GPT_OPS_NS	0x5032_3F00
General PWM Timer Clock Controller	GPT_GTCLK	0x4032_3F10	GPT_GTCLK_NS	0x5032_3F10
PWM Delay Generation Circuit	PDG	0x4032_4000	PDG_NS	0x5032_4000
Delta-Sigma Modulators 0	DSMIF0	0x4032_A000	DSMIF0_NS	0x5032_A000
Delta-Sigma Modulators 1	DSMIF1	0x4032_A800	DSMIF1_NS	0x5032_A800
16-bit A/D Converter	ADC_B	0x4033_8000	ADC_B_NS	0x5033_8000
Serial Communication Interface 0	SCI0_B	0x4035_8000	SCI0_B_NS	0x5035_8000
Serial Communication Interface 1	SCI1_B	0x4035_8100	SCI1_B_NS	0x5035_8100
Serial Communication Interface 2	SCI2_B	0x4035_8200	SCI2_B_NS	0x5035_8200
Serial Communication Interface 3	SCI3_B	0x4035_8300	SCI3_B_NS	0x5035_8300
Serial Communication Interface 4	SCI4_B	0x4035_8400	SCI4_B_NS	0x5035_8400
Serial Communication Interface 5	SCI5_B	0x4035_8500	SCI5_B_NS	0x5035_8500
Serial Communication Interface 6	SCI6_B	0x4035_8600	SCI6_B_NS	0x5035_8600
Serial Communication Interface 7	SCI7_B	0x4035_8700	SCI7_B_NS	0x5035_8700
Serial Communication Interface 8	SCI8_B	0x4035_8800	SCI8_B_NS	0x5035_8800
Serial Communication Interface 9	SCI9_B	0x4035_8900	SCI9_B_NS	0x5035_8900
Serial Peripheral Interface 0	SPI0_B	0x4035_C000	SPI0_B_NS	0x5035_C000
Serial Peripheral Interface 1	SPI1_B	0x4035_C100	SPI1_B_NS	0x5035_C100
I3C Bus Interface	I3C	0x4035_F000	I3C_NS	0x5035_F000
Error correction circuit for MBRAM0	ECCMB0	0x4036_F200	ECCMB0_NS	0x5036_F200
Error correction circuit for MBRAM1	ECCMB1	0x4036_F300	ECCMB1_NS	0x5036_F300
CANFD Module 0	CANFD0	0x4038_0000	CANFD0_NS	0x5038_0000
CANFD Module 1	CANFD1	0x4038_2000	CANFD1_NS	0x5038_2000
EtherCAT Slave Controller	ESC	0x403A_0000	ESC_NS	0x503A_0000
Initial Configuration 1 for EtherCAT Slave Controller	ESC_INI	0x403A_4000	ESC_INI_NS	0x503A_4000
Ethernet Message Forwarding Engine	MFWD	0x403C_0000	MFWD_NS	0x503C_0000
Layer 3 Ethernet Switch Module	ESWM	0x403C_8000	ESWM_NS	0x503C_8000
Ethernet Common Agent	COMA	0x403C_9000	COMA_NS	0x503C_9000
Ethernet Agent 0	ETHA0	0x403C_A000	ETHA0_NS	0x503C_A000
Ethernet MAC 0	RMAC0	0x403C_B000	RMAC0_NS	0x503C_B000
Ethernet Agent 1	ETHA1	0x403C_C000	ETHA1_NS	0x503C_C000
Ethernet MAC 1	RMAC1	0x403C_D000	RMAC1_NS	0x503C_D000
Ethernet CPU Agent	GWCA0	0x403C_E000	GWCA0_NS	0x503C_E000
Ethernet Generic PTP Timer	GPTP	0x403E_0000	GPTP_NS	0x503E_0000
Port 0 Control Registers	PORT0	0x4040_0000	PORT0_NS	0x5040_0000
Port 1 Control Registers	PORT1	0x4040_0020	PORT1_NS	0x5040_0020

Table A3.1 Peripheral base address (4 of 4)

Description	Name of secure registers	Base address of secure registers in secure alias region	Name of non-secure registers	Base address of non-secure registers in non-secure alias region
Port 2 Control Registers	PORT2	0x4040_0040	PORT2_NS	0x5040_0040
Port 3 Control Registers	PORT3	0x4040_0060	PORT3_NS	0x5040_0060
Port 4 Control Registers	PORT4	0x4040_0080	PORT4_NS	0x5040_0080
Port 5 Control Registers	PORT5	0x4040_00A0	PORT5_NS	0x5040_00A0
Port 6 Control Registers	PORT6	0x4040_00C0	PORT6_NS	0x5040_00C0
Port 7 Control Registers	PORT7	0x4040_00E0	PORT7_NS	0x5040_00E0
Port 8 Control Registers	PORT8	0x4040_0100	PORT8_NS	0x5040_0100
Port 9 Control Registers	PORT9	0x4040_0120	PORT9_NS	0x5040_0120
Port A Control Registers	PORTA	0x4040_0140	PORTA_NS	0x5040_0140
Port B Control Registers	PORTB	0x4040_0160	PORTB_NS	0x5040_0160
Port C Control Registers	PORTC	0x4040_0180	PORTC_NS	0x5040_0180
Port D Control Registers	PORTD	0x4040_01A0	PORTD_NS	0x5040_01A0
Port E Control Registers	PORTE	0x4040_01C0	PORTE_NS	0x5040_01C0
Port F Control Registers	PORTF	0x4040_01E0	PORTF_NS	0x5040_01E0
Port G Control Registers	PORTG	0x4040_0200	PORTG_NS	0x5040_0200
Pmn Pin Function Control Register	PFS	0x4040_0800	PFS_NS	0x5040_0800

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.
- The number of write access cycles indicates the number of cycles obtained by non-bufferable write access.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table A3.2 Access cycles (1 of 3)

Peripheral base address symbol	Address*1		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*2		Cycle unit	Related function
	From	To	Read	Write	Read	Write		
RMPU, SRAM, BUS, ICU_COMMON, CPSCU, DMAC0n, DMA0, DTC0, ICU, CPU_CTRL, CPU_OCD, CPU_DBG	0x4000_0000	0x4001_BFFF	3	2	3	2	ICLK	Renesas Memory Protection Unit, SRAM Control, BUS Control, Common Interrupt Controller, CPU System Security Control Unit, Direct memory access controller 0 n, DMAC Module Activation 0, Data Transfer Controller 0, Interrupt Controller, CPU Control Registers, On-Chip Debug, Debug Function
CACHE, TCM	0x4001_C000	0x4001_CFFF	5	4	5	4	ICLK	CM33 Cache, CM33 Tightly Coupled Memory
SYSC	0x4001_E000	0x4001_E9FF	4	3	2 to 4	1 to 3	PCLKB	System Control
SYSC	0x4001_EA00	0x4001_ED7F	7	6	5 to 7	4 to 6	PCLKB	System Control
IPC	0x4002_0000	0x4002_FFFF	3	2	3	2	ICLK	Inter-Processor Communication
ELC, RTC	0x4020_1000	0x4020_21FF	4	3	2 to 4	1 to 3	PCLKB	Event Link Controller, Realtime Clock
IWDT	0x4020_2200	0x4020_22FF	4	65	2 to 4	63 to 65	PCLKB	Independent Watchdog Timer
CAC, WDTn, MSTP, PSCU, POEG	0x4020_2400	0x4021_2FFF	4	3	2 to 4	1 to 3	PCLKB	Clock Frequency Accuracy Measurement Circuit, Watchdog Timer n, Module Stop Control, Peripheral Security Control Unit, Port Output Enable Module for GPT
ULPTn	0x4022_0000	0x4022_01FF	6	65	4 to 6	63 to 65	PCLKB	Ultra-Low Power Timer n
AGTn	0x4022_1000	0x4022_11FF	6	3	4 to 6	1 to 3	PCLKB	Low Power Asynchronous General purpose Timer n
DAC12n, TSN	0x4023_3000	0x4023_5FFF	4	3	2 to 4	1 to 3	PCLKB	12-bit D/A Converter n, Temperature Sensor
ACMPHSn	0x4023_6000	0x4023_63FF	3	3	1 to 3	1 to 3	PCLKB	High-Speed Analog Comparator n
USBFS	0x4025_0000	0x4025_03FF	5	4	3 to 5	2 to 4	PCLKB	USB 2.0 FS Module
USBFS	0x4025_0400	0x4025_04FF	4	65	2 to 4	63 to 65	PCLKB	USB 2.0 FS Module
SDHIn, IICn, OSPIn, DOTFn	0x4025_2000	0x4026_89FF	4	3	2 to 4	1 to 3	PCLKB	SD Host Interface n, Inter-Integrated Circuit n, Octal Serial Peripheral Interface n, Decryption On-The-Fly n
CRC, DOC	0x4031_0000	0x4031_1FFF	4	3	2 to 4	1 to 3	PCLKA	CRC Calculator, Data Operation Circuit

Table A3.2 Access cycles (2 of 3)

Peripheral base address symbol	Address*1		Number of access cycles					
			ICLK = PCLK		ICLK > PCLK*2		Cycle unit	Related function
	From	To	Read	Write	Read	Write		
GPT32n, GPT_OPS	0x4032_2000	0x4032_3F0F	9	6	7 to 9	4 to 6	PCLKA	General PWM 32-Bit Timer n, Output Phase Switching Controller
GPT_GTCLK	0x4032_3F10	0x4032_3F1F	4	3	2 to 4	1 to 3	PCLKA	General PWM Timer Clock Control
PDG	0x4032_4000	0x4032_4FFF	3	2	1 to 3	0 to 2	PCLKA	PWM Delay Generation Circuit
DSMIFn	0x4032_A000	0x4032_AFFF	3	3	1 to 3	1 to 3	PCLKA	Delta-Sigma Modulators n
ADC_B	0x4033_8000	0x4034_7FFF	4	3	2 to 4	1 to 3	PCLKA	A/D Converter
SCIn, SPIn, I3C	0x4035_8000	0x4035_FFFF	4	3	2 to 4	1 to 3	PCLKA	Serial Communication Interface n, Serial Peripheral Interface n, I3C Bus Interface
ECCMBn	0x4036_F200	0x4036_F3FF	5	4	3 to 5	2 to 4	PCLKA	Error correction circuit for MBRAMn
CANFDn	0x4038_0000	0x4038_3FFF	4	3	2 to 4	1 to 3	PCLKA	CANFD Module n
ESWM	0x403C_0000	0x403E_FFFF	—	—	7 to 12	2 to 4	PCLKA	Layer 3 Ethernet Switch Module
ESC	0x403A_0000	0x403A_3FFF	66	60	66 to 67	59 to 60	PCLKA	EtherCAT Slave Controller 32bit access
ESC	0x403A_0000	0x403A_3FFF	52	37	51 to 52	36 to 37	PCLKA	EtherCAT Slave Controller 16bit access
ESC	0x403A_0000	0x403A_3FFF	41	30	40 to 41	29 to 30	PCLKA	EtherCAT Slave Controller 8bit access
ESC_INI	0x403A_4000	0x403A_4FFF	4	3	3 to 4	2 to 3	PCLKA	Initial Configuration 1 for EtherCAT Slave Controller
PORTn	0x4040_0000	0x4040_01FF	4	2	4	2	ICLK	Port n Control Registers
PFS	0x4040_0800	0x4040_0FFF	8	2	8	2	ICLK	Pmn Pin Function Control Register
RSIP-E50D	-	-	3 to 5	2	1 to 6	0 to 2	PCLKA	Renesas Secure IP

Table A3.2 Access cycles (3 of 3)

Peripheral base address symbol	Address*1		Number of access cycles					
			ICLK = MRPCLK		ICLK > MRPCLK*2		Cycle unit	Related function
	From	To	Read	Write	Read	Write		
MRAM	0x4013_0000	0x4013_FFFF	4	3	2 to 4	1 to 3	MRPCLK	MRAM control

Note 1. This table only shows secure address. Access cycle of the non-secure address is the same as its secure address.
Note 2. If the number of PCLK or MRPCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.

Appendix 4. Notes for Register R/W

- A secure bus master issues a secure access using an address marked as secure by IDAU/SAU or MSAU
- A secure bus master issues a non-secure access using an address marked as non-secure by IDAU/SAU or MSAU
- A non-secure bus master issues a non-secure access using an address marked as non-secure by IDAU/SAU or MSAU.

Table A4.1 Type of register notes (S-TYPE)

TYPE	UM description
S-TYPE-1	Only Secure access can write to this register. Read access is always allowed. Non-secure write access is ignored, but TrustZone access error is not generated.
S-TYPE-2	Read access is always allowed If the security attribution is configured as Secure: ● Secure write access is allowed ● Non-secure write access is ignored, but TrustZone access error is not generated.
	If the security attribution is configured as Non-secure: ● Secure write access is ignored, but TrustZone access error is not generated ● Non-secure access is allowed.
S-TYPE-3	If the security attribution is configured as Secure: ● Secure access is allowed ● Non-secure write access is ignored and Non-secure read access is read as 0, TrustZone access error is generated.
	If the security attribution is configured as Non-secure: ● Secure write access is ignored and Secure read access is read as 0, TrustZone access error is generated ● Non-secure access is allowed.
S-TYPE-4	If the security attribution is configured as Secure: ● Secure access is allowed ● Non-secure write access is ignored and Non-secure read access is read as 0, but TrustZone access error is not generated.
	If the security attribution is configured as Non-secure: ● Secure write access is ignored and Secure read access is read as 0, but TrustZone access error is not generated ● Non-secure access is allowed.
S-TYPE-5	Access is always allowed.
S-TYPE-6	Secure access is allowed. Non-secure write access is ignored, and Non-secure read access is read as 0, TrustZone access error is generated.
S-TYPE-7	Secure write access is ignored, and Secure read access is read as 0, TrustZone access error is generated. Non-secure access is allowed.

Note: A non-secure bus master does NOT issue any access using an address marked as secure by IDAU/SAU or MSAU.

Table A4.2 Type of register notes (P-TYPE)

TYPE	UM description
P-TYPE-1	Privileged write access is allowed. Read access is always allowed. Unprivileged write access is ignored, but TrustZone access error is not generated.
P-TYPE-2	Privileged access is allowed. Unprivileged write access is ignored, and Unprivileged read access is read as 0, TrustZone access error is generated.
P-TYPE-3	If the privilege attribution is configured as Privileged: ● Privileged access is allowed ● Unprivileged write access is ignored and Unprivileged read access is read as 0, TrustZone access error is generated.
	If the privilege attribution is configured as Unprivilege: ● Privileged access and Unprivileged access are allowed.
P-TYPE-4	If the privilege attribution is configured as Privileged: ● Privileged access is allowed ● Unprivileged write access is ignored and Unprivileged read access is read as 0, TrustZone access error is not generated.
	If the privilege attribution is configured as Unprivilege: ● Privileged access and Unprivileged access are allowed.
P-TYPE-5	Access is always allowed.

Appendix 5. Peripheral Variant

Table A5.1 shows the correspondence between the module name used in this manual and the peripheral variant.

Table A5.1 Module name vs peripheral variant

Module name	Peripheral variant
SCI	SCI_B
SPI	SPI_B
OSPI	OSPI_B
ADC16H	ADC_B
DAC12	DAC_B
DOC	DOC_B

Revision History

Revision 1.00— February 14, 2025

First edition, issued

Revision 1.10 — May 16, 2025

1. Overview:
- Updated Figure 1.2 Part numbering scheme.
- Updated Table 1.15 Pin list for the Standard product.
- Updated Table 1.16 Pin list for the SiP product.

2. Electrical Characteristics:
- Updated 2. Electrical Characteristics.
- Updated 2.1 Absolute Maximum Ratings.
- Updated 2.2.5 Operating and Standby Current.
- Updated 2.3.10 SPI Timing.
- Updated 2.3.11 OSPI Timing.
- Updated 2.6 ADC Characteristics.
- Added 2.11 External VDD timing Characteristics.

Appendix:
- Updated Figure A2.3 HLQFP 176-pin in Appendix 2.
- Updated Table A5.1 Module name vs peripheral variant in Appendix 5.

Revision 1.20 — Jul 31, 2025

1. Overview:
- Updated Table 1.8 Communication interfaces
- Updated Figure 1.2 Part numbering scheme
- Updated Table 1.12 Product list
- Updated Table 1.14 Pin functions
- Updated Table 1.15 Pin list for the Standard product
- Updated Table 1.16 Pin list for the SiP product

2. Electrical Characteristics:
- Updated Table 2.16 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock ON (DCDC mode)
- Updated Table 2.18 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock OFF (DCDC mode)
- Updated Table 2.19 Current of high-speed mode, maximum data processing (MVE operation), peripheral clock OFF (External VDD mode)
- Updated Table 2.20 Current of high-speed mode, maximum data processing (MVE operation), CPU0 active, CPU1 Deep Sleep, peripheral clock OFF (DCDC mode)
- Updated Table 2.21 Current of high-speed mode, maximum data processing (MVE operation), CPU0 active, CPU1 Deep Sleep, peripheral clock OFF (External VDD mode)
- Updated Table 2.22 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock OFF (DCDC mode)
- Updated Table 2.23 Current of high-speed mode, maximum data processing, CPU0 Deep Sleep, CPU1 active, peripheral clock OFF (External VDD mode)
- Updated Table 2.24 Current of high-speed mode, CPU Sleep mode (DCDC mode)
- Updated Table 2.26 Current of high-speed mode, CPU0 Sleep, CPU1 Deep Sleep (DCDC mode)
- Updated Table 2.28 Current of high-speed mode, CPU0 Deep Sleep, CPU1 Sleep (DCDC mode)
- Updated Table 2.30 Current of high-speed mode, CPU Deep Sleep mode (DCDC mode)

Revision 1.30 — Feb 27, 2026

1. Overview:
- Updated Figure 1.2 Part numbering scheme
- Updated Table 1.12 Product list
- Updated Table 1.13 Function Comparison
- Updated Table 1.14 Pin functions
- Updated Figure 1.7 Pin assignment for BGA 303-pin
- Updated Table 1.15 Pin list for the Standard product
- Updated Table 1.16 Pin list for the SiP product

Revision 1.30 — Feb 27, 2026

2. Electrical Characteristics:

- Updated Table 2.2 Recommended operating conditions
- Updated Table 2.34 Coremark and normal mode current, CPU0 Deep Sleep, CPU1 active. (DCDC mode and External VDD mode)
- Added Table 2.42 VCC_USB rise gradient characteristics at power on
- Updated Table 2.43 Thermal Resistance
- Updated Table 2.44 Power consumption of each unit (DCDC mode)
- Updated Table 2.45 Power consumption of each unit (External VDD mode)
- Updated Table 2.48 Clock timing except for sub-clock oscillator
- Updated Table 2.50 Reset timing
- Updated Table 2.51 Timing of recovery from low power modes
- Updated Table 2.62 SPI timing
- Updated Table 2.63 OSPI timing
- Updated Figure 2.86 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)
- Updated Table 2.75 PDG Timing
- Updated Table 2.101 TSN characteristics
- Updated Table 2.103 Sub-clock oscillation stop detection circuit characteristics
- Added Figure 2.127 Sub-clock Oscillation Stop Detector start-up time
- Updated Table 2.104 Power-on reset circuit and voltage detection circuit characteristics
- Updated Figure 2.129 Power-on reset timing
- Updated Figure 2.130 Voltage detection circuit timing (Vdet0)
- Updated Figure 2.131 Voltage detection circuit timing (Vdetn) (n = 1, 2, 4, 5)
- Updated 2.15 MRAM Characteristics
- Updated Table 2.110 Code MRAM Characteristics
- Updated 2.15.2 Option Setting Memory (Configuration area) Characteristics
- Updated Table 2.114 MACI command Characteristics

Appendix:

- Added Figure A2.3 BGA 303-pin
- Updated Table A3.2 Access cycles

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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