RAA223021

700V AC/DC Buck Regulator with Ultra-Low Standby Power

The RAA223021 is a universal input AC/DC switching buck regulator with ultra-low standby power that features a 700V integrated MOSFET capable of delivering up to 12W output power. It supports output voltage as low as 5V.

The RAA223021 combines constant off-time control for heavy load and Pulse Frequency Modulation (PFM) for light-load operation. Constant off-time controls switching frequency above the audible frequency around 43kHz. PFM eliminates any potential audible noises while offering superior light-load efficiency and ultra-low power consumption (<20mW at no load). The efficiency is achieved up to 80%. The built-in frequency dithering further reduces EMI noise spectrum.

The RAA223021 also features input brownout protection that prevents input circuitry from the overcurrent at low input voltage, and hiccup protections for output fault conditions such as short-circuit, overload, overvoltage, and open feedback.

The RAA223021 is available in a small 7 Ld SOIC package.

Features

- Ultra-low standby power (<20mW)
- No audible noise
- Low quiescent current (<80µA)
- Output voltage as low as 3.3V
- Low EMI with frequency dithering
- 7 Ld SOIC package
- Programmable PFM allows optimization of C_{OUT} for various standby power requirements
- Protection features: Short-Circuit Protection (SCP), Overload Protection (OLP), Overvoltage Protection (OVP), open feedback protection, and Over-Temperature Protection (OTP).

Applications

- Home appliances
- Home automation, IoT, and sensors
- Metering and Industry control
- Bias power

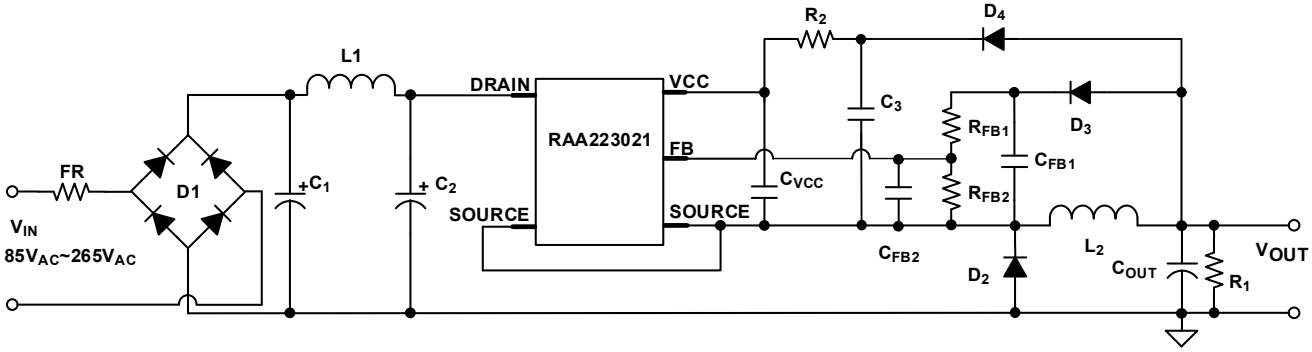


Figure 1. Typical RAA223021 Buck Application Circuit

Table 1. Maximum Output Current (Maximum Ambient 85°C)

Output Setting Voltage (V)	$120V_{AC}$	$230V_{AC}$	$90V_{AC}$~$265V_{AC}$
3.3	0.67A	0.58A	0.56A
5	0.67A	0.66A	0.6A
9	0.64A	0.6A	0.56A
12	0.56A	0.54A	0.5A
15	0.56A	0.52A	0.5A
24	0.49A	0.5A	0.46A

Contents

1. Overview

1.1 Block Diagram

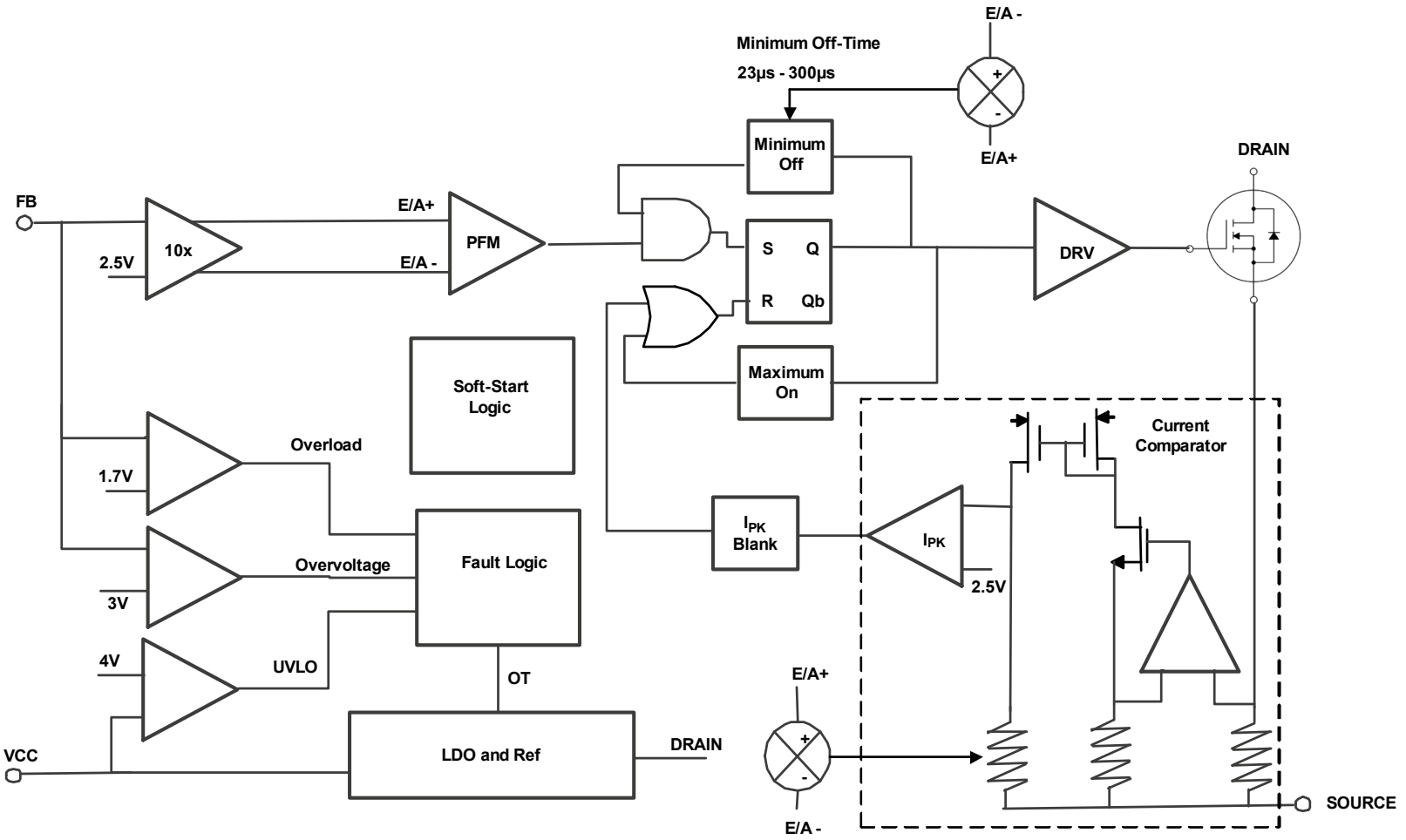
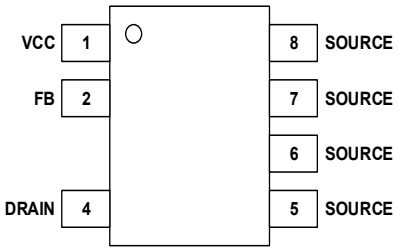


Figure 2. Block Diagram of RAA223021

2. Pin Information

2.1 Pin Assignments



7 Ld SOIC
Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	VCC	IC supply voltage
2	FB	Feedback pin
4	DRAIN	Internal power MOSFET drain
5-8	SOURCE	Internal power MOSFET source

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC	-0.3	+6.5	V
VFB	-0.3	+6.5	V
DRAIN (to SOURCE)	- 0.3	700V	V
Continuous Power Dissipation (T_A = +25°C)		1	W
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	1.2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
7 Ld SOIC	50	23

1. θ_{JA} is measured in free air with the component mounted on a 1-layer test board with thermal copper 555mm^2 in size and 1oz Cu (35µm) thickness.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-60	+150	°C
Pb-Free Reflow Profile	See TB493		

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DRAIN}		375	V
Ambient Temperature	-40	+85	°C
Output Voltage	3.3		V

3.4 Electrical Specifications

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Startup and Power FET						
Internal V_{CC} Startup Current	I_{VCC_START}	V_{CC} = 4V		2.5		mA
Drain Leakage Current	I_{D_LEAK}	V_{CC} = 0V, V_{DRAIN} = 325V, V_{FB} = 2.6V		1		µA
I_{DRAIN} Bias	I_{D_BIAS}	V_{DRAIN} = 375V			10	µA
Power FET Breakdown Voltage	$V_{DS(BR)}$	T_J = 25°C	700			V
Power FET On-Resistance	$r_{DS(ON)}$	T_J = 25°C, I_{DS} = 30mA, V_{CC} = 5.8V		4	5.5	Ω
		T_J = 125°C		7	8.5	Ω
V_{CC} Supply						
V_{CC} Start (Rising)	V_{CC_START}		5.6	6	6.4	V
V_{CC} when Internal Regulator Off	V_{CC_OFF}		5.6	6	6.4	V
V_{CC} (Falling) Regulator On at Startup	V_{CC_ON}		5.45	5.9	6.25	V
Internal V_{CC} On/Off Hysteresis	V_{CC_HYS}		0.10	0.15		V
V_{CC} (Fallng) Regulator On after Startup	$V_{CC\_ON\_SS}$		4.3	4.5	4.9	V
V_{CC} Undervoltage Threshold (Falling)	V_{CC_UVLO}	IC stop switching	3.8	4	4.4	V
V_{CC} Shunt Regulator On (Rise)	V_{CC_SON}	External V_{CC} supply, internal shunt on		6.2	6.5	V
V_{CC} Shunt Regulator Off (Fall)	V_{CC_SOFF}	External V_{CC} supply, internal shunt off		6.1	6.45	V
V_{CC} Quiescent Current	I_{VCC_Q}	V_{FB} > 2.5V, no switching		80	125	µA
V_{CC} Current During Switching	I_{VCC}	V_{FB} < 2.5V, switching frequency = 43kHz, D = 0.15, V_{CC} = V_{CC_ON} + 0.1V		225	325	µA
V_{CC} Discharging Current Hiccup Timing	I_{QVCC3}	V_{CC} discharge timing for fault hiccup delay		20	33	µA
Current Sense						
Peak Current Limit	I_{PK}	di/dt = 600mA/µs, T_J = 25°C, V_{CC} = 5.8V	875	1100	1325	mA
SCP Threshold[2]	I_{SC_TH}			1.73		A
Minimum Peak Current	I_{PKMIN}	V_{IN} = 85V_{AC}, I_{OUT} = 0, V_{CC} = 5.8V		158		mA
Leading Edge Blank Time	t_{LEB}	T_J =25°C, V_{CC} = 5.8V	200	250		ns
Feedback						
Feedback Voltage	V_{FB}	T_J =25°C, V_{CC} = 5.8V	2.4	2.5	2.64	V
Transconductance	GM	I_{PK} GM, V_{CC} = 5.8V		22		S
Feedback Undervoltage Threshold	V_{FBUV}	V_{CC} = 5.7V	1.6	1.7	1.8	V
Feedback Threshold for Increased Off-Time	$V_{FB\_TOFFMIN}$	V_{CC} = 5.0V		0.88		V
Feedback Overvoltage	V_{FBOV}		2.8	3	3.35	V
Timing						
Minimum Off-Time	t_{OFF_MIN}	V_{CC} = 5.0V	18	23	32	µs

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, T_J = -40 to +125°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Maximum On-Time	t_{ON_MAX}	V_{CC} = 5.0V	11	14	18	µs
Minimum Off-Time in Short-Circuit	t_{OFFMIN_SC}	V_{CC} = 5.0V		150		µs
Hiccup Restart Delay	t_{HICC}	C_{VCC} = 1µF		90		ms
OLP Timer	t_{OLP}	f_{SW} = 43kHz, V_{FB} < 1.7V, V_{CC} = 5.0V		1032		cycle
Thermal						
Over-Temperature Threshold	OTP_{TH}			150		°C
Over-Temperature Hysteresis	OTP_{HYS}			45		°C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Compliance to limits is established by design.

4. Typical Characterization Graphs

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, V_{OUT} = 12V, I_{OUT} = 667mA, L2 = 680µH, C_{OUT} = 330µF, unless otherwise specified.

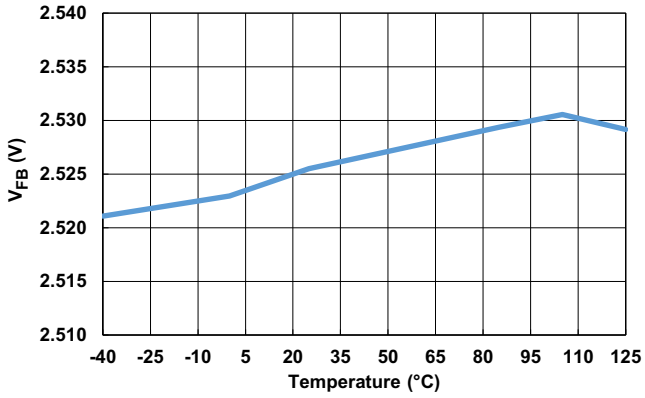


Figure 3. Feedback Voltage vs Temperature

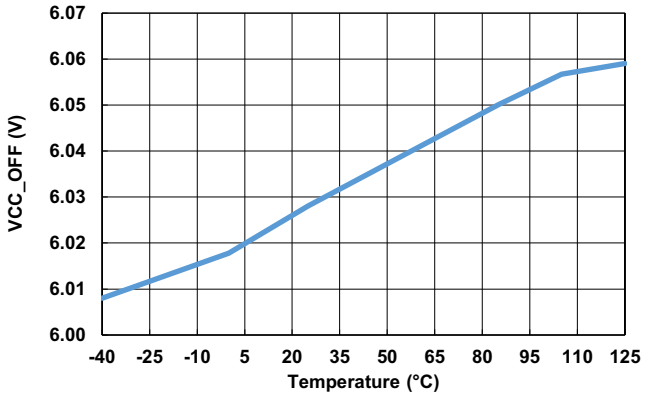


Figure 4. V_{CC} Start/Upper Limit vs Temperature

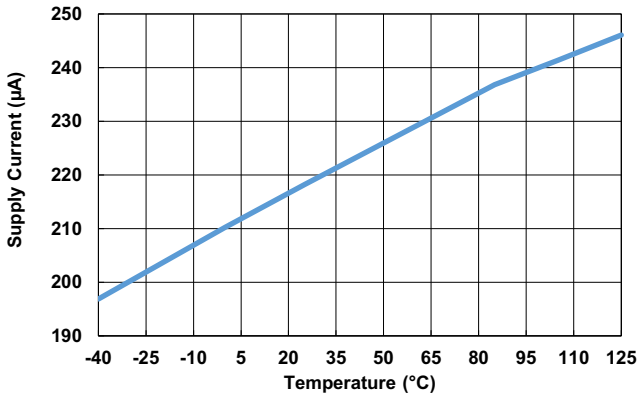


Figure 5. IC Supply Current vs Temperature

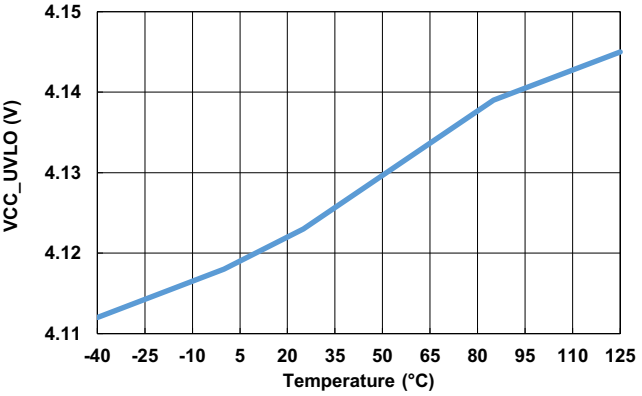


Figure 6. V_{CC} Undervoltage Threshold vs Temperature

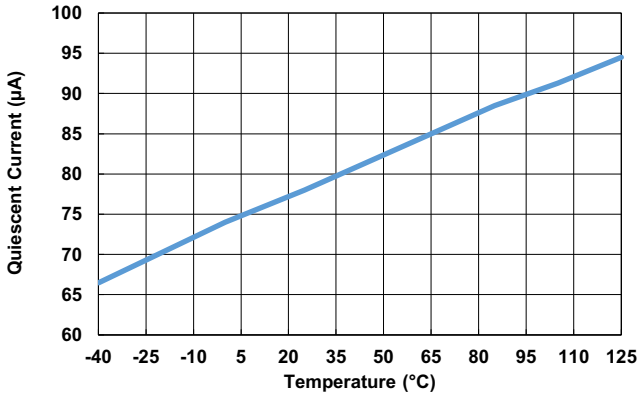


Figure 7. IC Quiescent Current vs Temperature

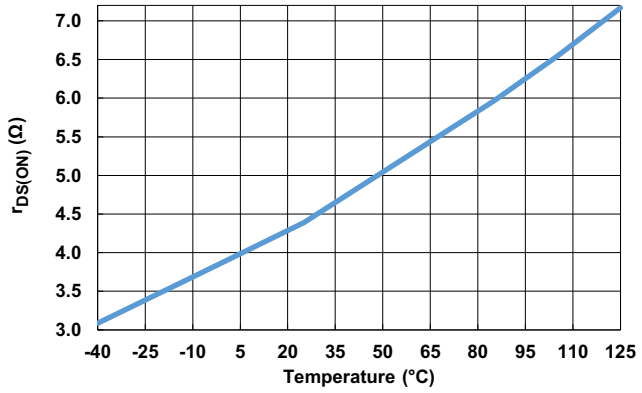


Figure 8. On-Resistance vs Temperature

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, V_{OUT} = 12V, I_{OUT} = 667mA, L2 = 680µH, C_{OUT} = 330µF, unless otherwise specified. (Cont.)

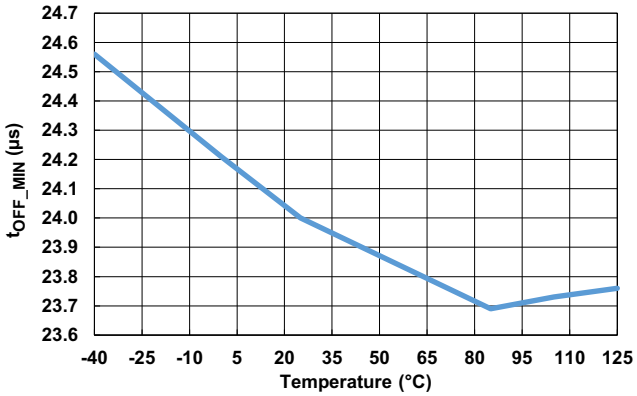


Figure 9. Minimum Off-Time vs Temperature

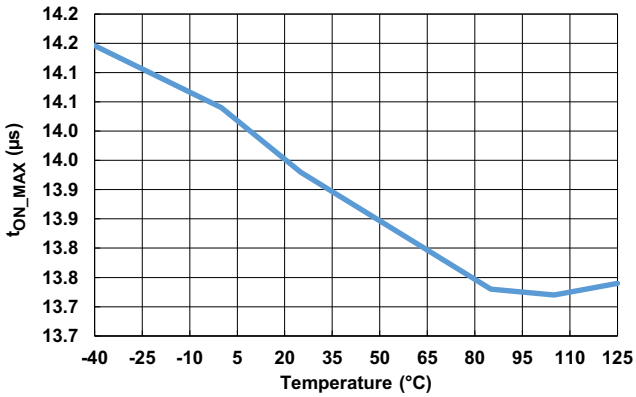


Figure 10. Maximum On-Time vs Temperature

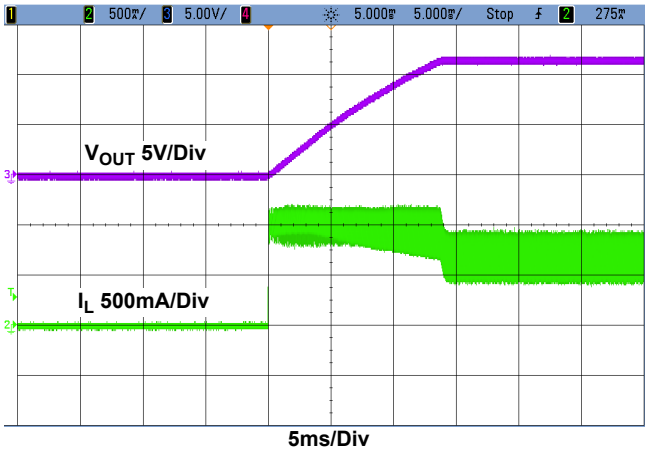


Figure 11. Startup (V_{IN} = 230V_{AC})

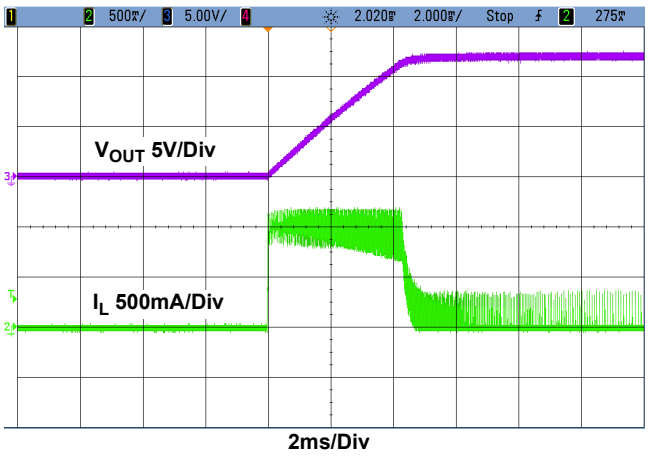


Figure 12. Startup (V_{IN} = 230V_{AC}, No Load)

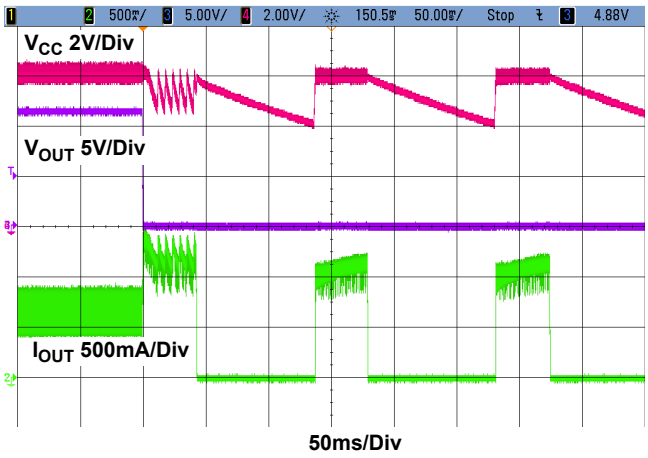


Figure 13. Short-Circuit Protection (V_{IN} = 230V_{AC})

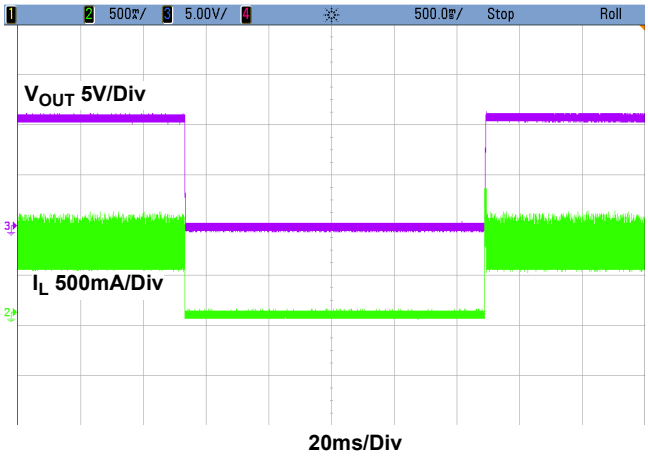


Figure 14. Over-Temperature Protection (V_{IN} = 230V_{AC})

Typical operating conditions at 25°C, V_{DRAIN} = 100V, V_{CC} = 5.6V, V_{OUT} = 12V, I_{OUT} = 667mA, L2 = 680µH, C_{OUT} = 330µF, unless otherwise specified. (Cont.)

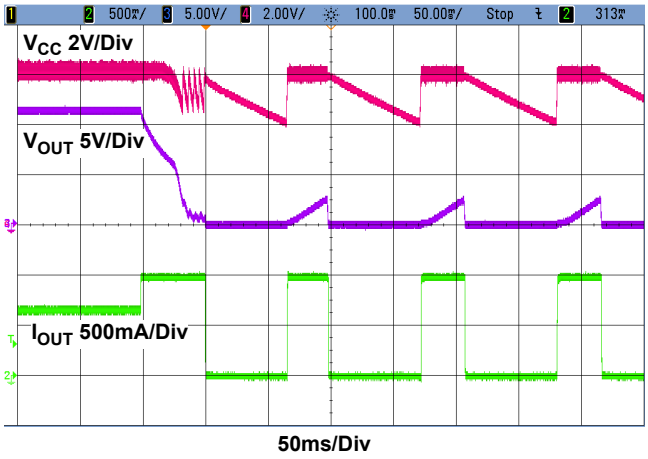


Figure 15. Overload Protection (V_{IN} = 230V_{AC})

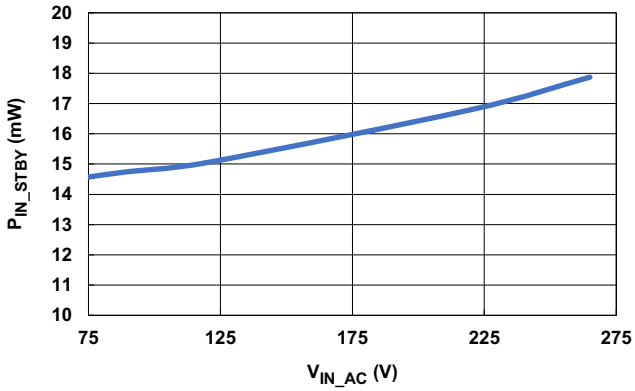


Figure 16. No Load Power Loss

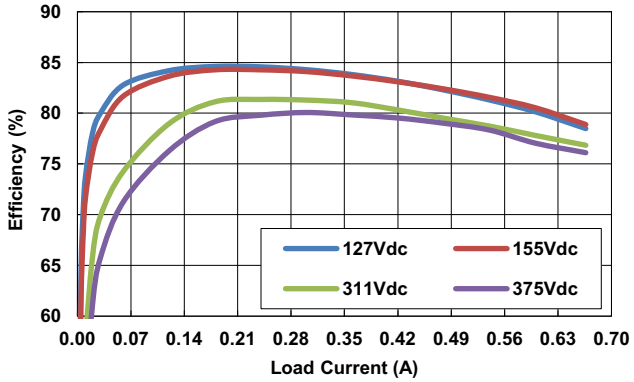


Figure 17. Efficiency with 12V Output

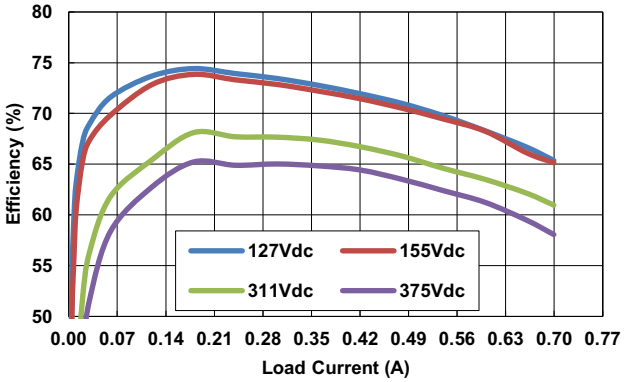


Figure 18. Efficiency with 5V Output

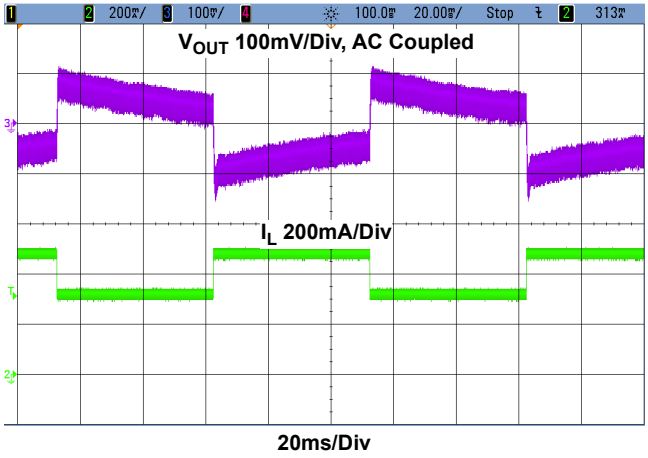


Figure 19. Dynamic Load (V_{IN} = 230V_{AC})

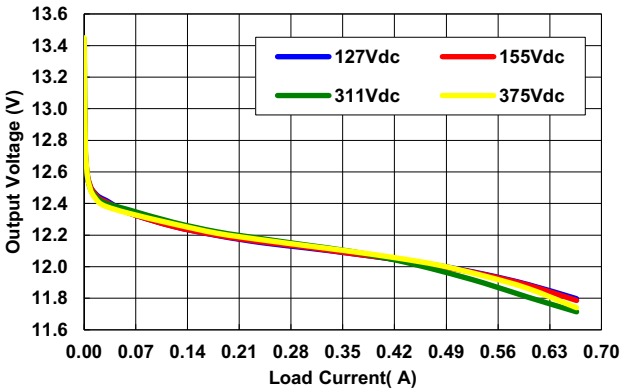


Figure 20. Load Regulation

5. Detailed Description

The RAA223021 adopts the high-side float switching topology as Figure 1 shows. A floating VCC supplies IC operation. The output voltage is sensed on the FB pin from an RC sampling network connected to the output, and compared with the internal reference through an error amplifier that controls the peak current accordingly.

5.1 Constant Off-Time Mode

In heavy load, the power FET is turned on after a constant off-time. Because the on-time is comparably much smaller than the off-time, the IC operates with quasi-constant frequency. When the load current goes lower, the peak current becomes lower while still switching around 43kHz until it hits the minimum peak current limit. Because the switching frequency is always kept around 43kHz in the operation, no audible noises can be heard.

5.2 PFM Mode

When the load current decreases below a certain value, the peak current is kept at the minimum level, while the off-time is gradually increased to maintain the output regulation. The IC goes into Pulse Frequency Modulation (PFM) operation as Figure 21 shows; therefore, losses are reduced because of switching frequency reduction. During this mode, while the switching frequency is reduced below 1kHz at no load, the audible noise is minimized by keeping the peak current at the minimum level. In the meantime, because of the low IC biasing current and small peak current, the standby power can be achieved below 20mW. The above operation is illustrated in Figure 22 and Figure 23.

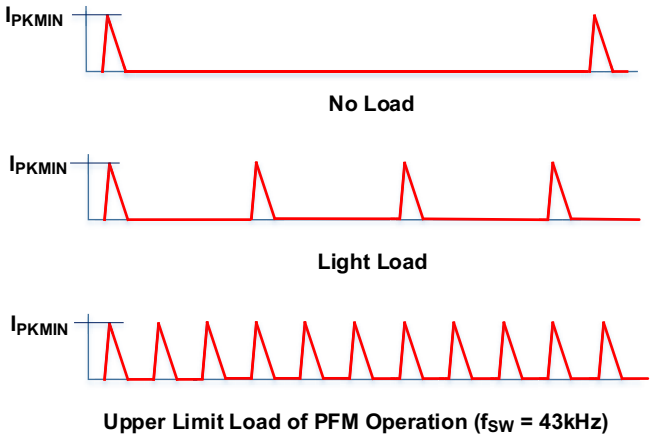


Figure 21. PFM Operation in Light Load

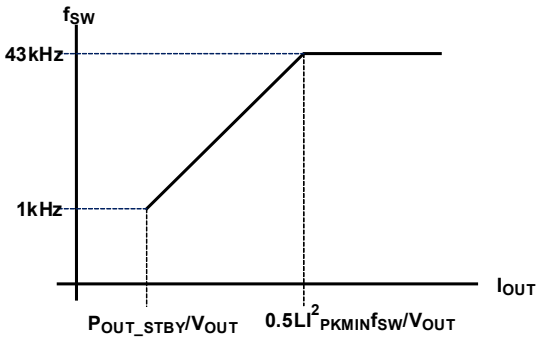


Figure 22. Switching Frequency vs I_{OUT}

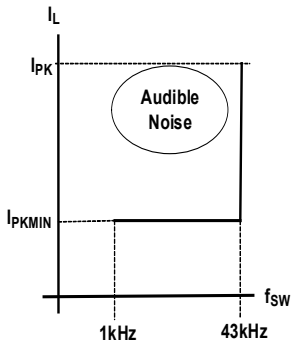


Figure 23. Peak Current vs Switching Frequency

5.3 Output Voltage Sampling

The RC sampling network samples the output voltage through a forward-biased D_3 when D_2 is free-wheeling. When the D_2 cathode goes high and D_2 stops conducting current, the sampled voltage across C_{FB1} is discharged by R_{FB1} and R_{FB2}. In constant off-time operation, the FB pin voltage is slightly below the internal reference. The power FET is set on after a constant off-time. In PFM mode, when the sampled voltage on FB pin drops to internal reference, the power FET is clocked on. In this way, the light-load switching is set by the C_{FB1}, R_{FB1}, and R_{FB2} for the corresponding load. Therefore, the required no-load standby power is achieved by choosing C_{FB1}, allowing you the flexibility to design your circuit for various standby power requirements. For detailed design guidance, see Feedback Capacitor (CFB1) Selection.

5.4 Soft Start-Up

The RAA223021 starts up with the V_{CC} capacitor charged by an internal HV current source. When the V_{CC} reaches up to 6V, the IC begins switching, the internal HV current source is turned off, and a start-up timer begins. When V_{CC} drops below 5.9V, the HV current source is on again, which is determined by the actual IC supply current. During the start-up, the output voltage ramps up gradually, which is controlled by a variable off-time set by the feedback voltage. After the timer expires (start-up is finished), the HV current source is on again only when V_{CC} drops to 4.5V. When V_{OUT} is established, V_{CC} can be supplied by V_{OUT} (optional) to save power consumption for high-efficiency and low-standby power, as Figure 24 shows.

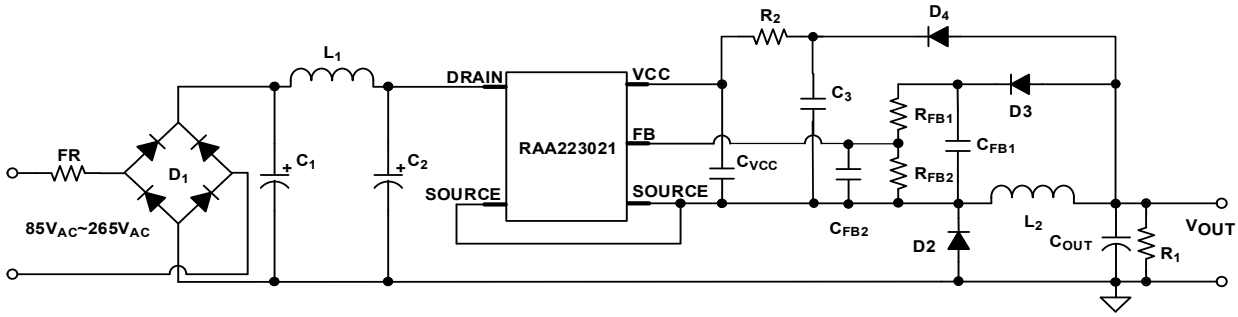


Figure 24. RAA223021 Low Standby Power Buck Regulator

Figure 25 shows the start-up diagram.

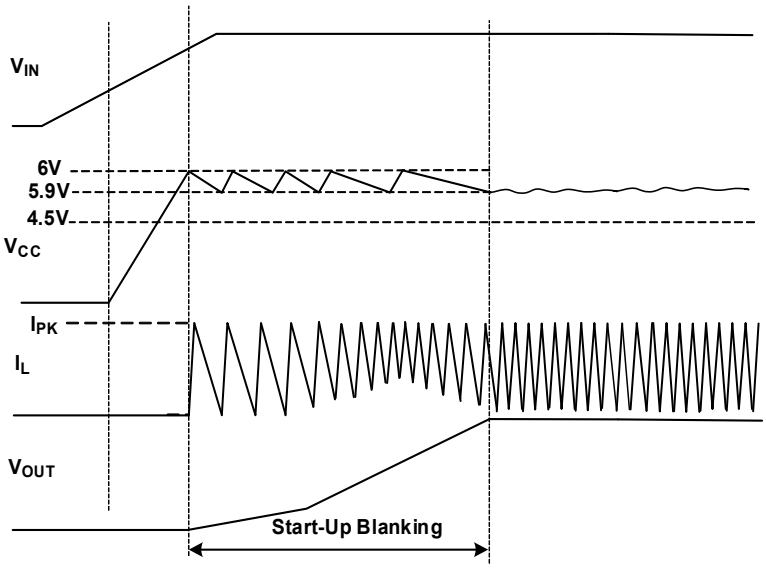


Figure 25. RAA223021 Start-Up Diagram

5.5 Overload Protection

With the fixed minimum off-time (when $V_{FB} \geq 0.825V$), the maximum load current that the RAA223021 allows is limited for a given output voltage and inductor, and therefore, is the maximum output current. However, when the output voltage continues to drop during the overload, the FET power losses increase and can cause potential IC overheating. Therefore, when V_{FB} reaches 1.7V, an internal comparator is triggered and starts an Overload Protection (OLP) timer. When the timer is expired, the overload situation is identified and the IC is shut off. V_{CC} is discharged by a 20µA internal current source to 4V and then charged up to 6V to resume switching (the interval without switching is the hiccup time). The overload protection time sequence is shown in Figure 26.

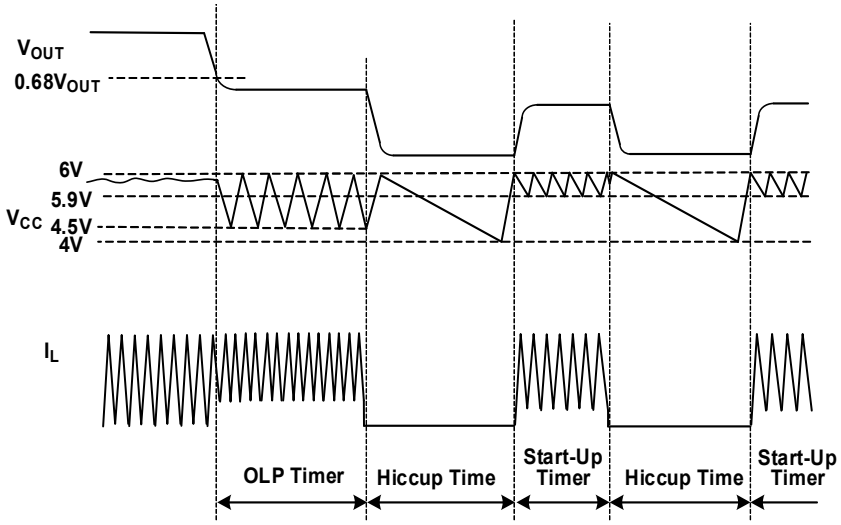


Figure 26. RAA223021 Overload Protection Diagram

5.6 Short-Circuit Protection

When the output is shorted, $V_{OUT} = 0$, V_{FB} drops to zero because of the feedback network, introducing a delay. Before V_{FB} drops to $V_{FB\_TOFFMIN}$, the RAA223021 operates with t_{ON_MAX} and t_{OFF_MIN}, which quickly builds up a high current (>1.3A) because the inductor peak current does not get reset. When the current reaches I_{SC_TH}, a timer is started. If the inductor current reaches I_{SC_TH} for four consecutive cycles, the RAA223021 determines that a short-circuit is present and immediately shuts off switching. The IC then quickly charges V_{CC} up to 6V and discharges it with a 20µA current source to 4V. When V_{CC} drops to 4V, a 2.5mA current source charges V_{CC} back to 6V where the IC resumes switching.

When the RAA223021 resumes switching, assuming V_{FB} drops to zero, the IC operates with the increased t_{OFFMIN_MAX} so the inductor current can fully reset below the maximum peak limit. The RAA223021 operates in CCM with the inductor peak current being limited at 1100mA. The part remains in hiccup mode until the short is removed. When the short is removed, V_{OUT} returns to normal. This procedure is shown in Figure 27.

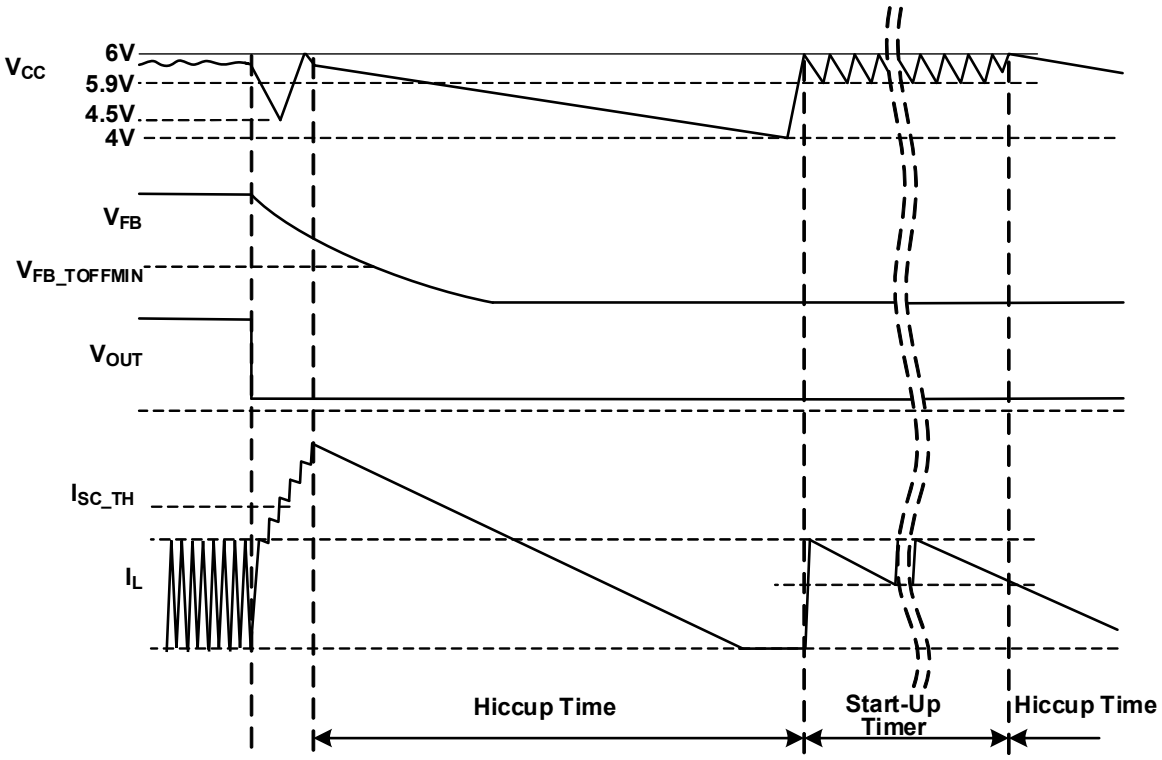


Figure 27. RAA223021 Short-Circuit Protection Diagram

6. Application Topologies

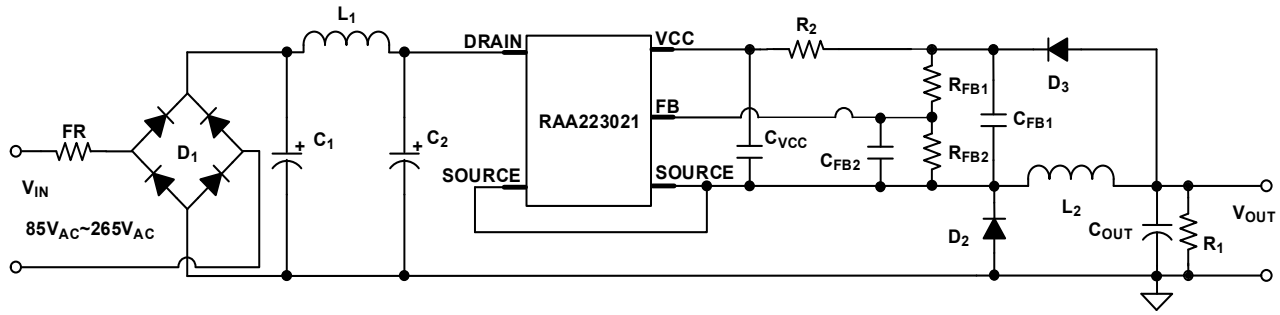


Figure 28. RAA223021 Buck with VCC Backfeed from C_{FB1}

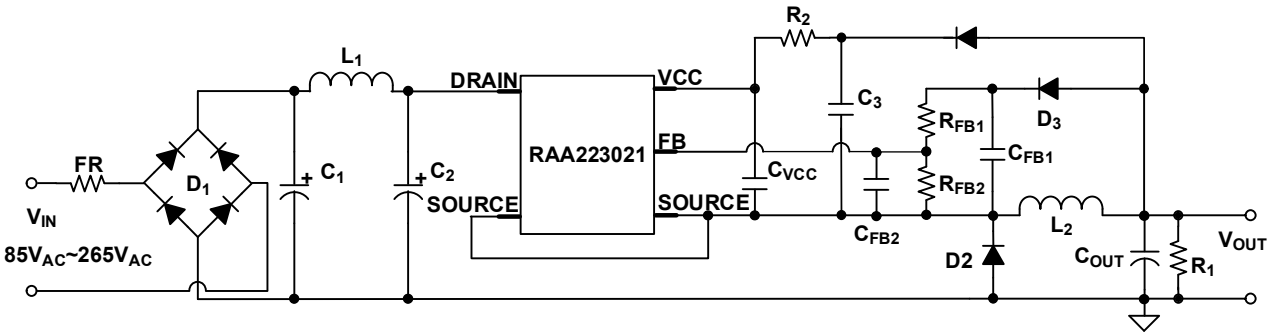


Figure 29. RAA223021 Buck with 5V Output

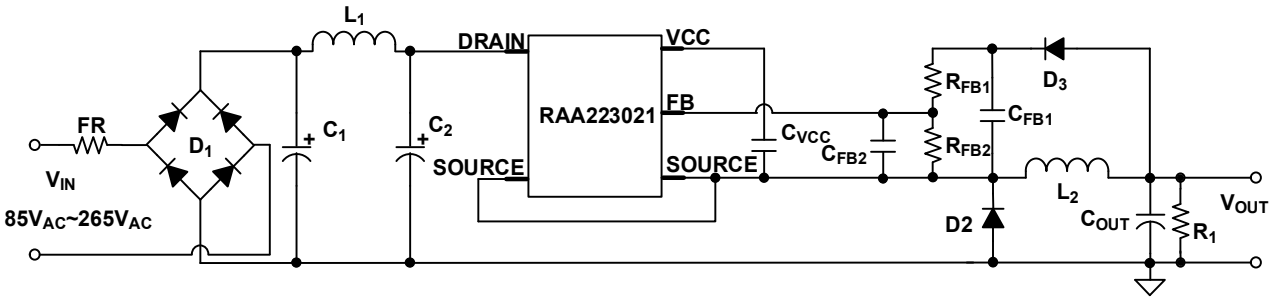


Figure 30. RAA223021 Buck with 3.3V Output

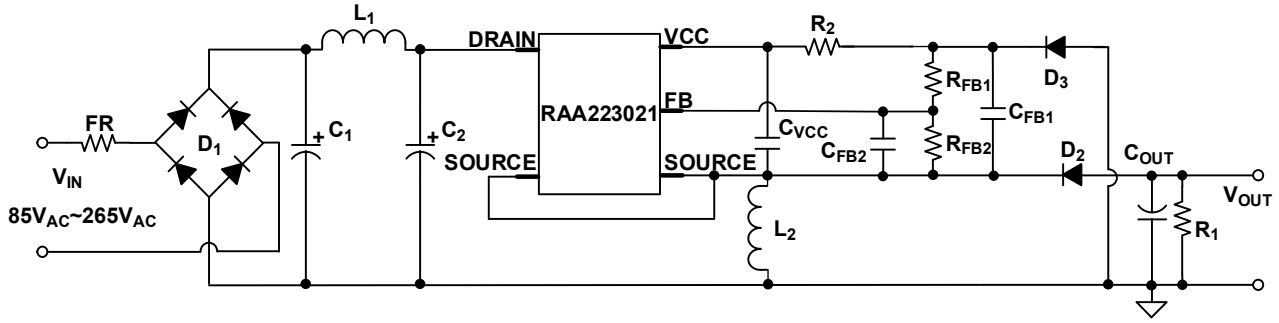


Figure 31. RAA223021 Buck/Boost

7. Design Guidance

To simplify the analysis, the following design guidelines are based on the circuit shown in Figure 1.

7.1 Feedback Resistor Selection

The output voltage is set by the resistor divider of R_{FB1} and R_{FB2}. Because of the diode forward voltage mismatch between the feedback diode D_3 and free-wheeling diode D_2, an additional 0.5V offset is added in Equation 1 to calculate the resistor values of R_{FB1} and R_{FB2}. A series resistor with D_3 can help decrease the mismatch affect.

(EQ. 1) $$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT} + 0.5}{V_{FB}} - 1$$

7.2 Output Inductor Selection

Because the buck regulator is designed with a constant off-time of 23µs at full load, design the output inductor according to Equation 2:

(EQ. 2) $$L \geq \frac{V_{OUT} t_{OFF\_MIN}}{2(I_{PK} - I_{O\_MAX})}$$

For example, if V_{OUT} = 12V, if I_{O_MAX} = 660mA, $L \geq \frac{12 \times 23 \times 10^{-6}}{2 \times (1.1 - 0.66)} = 314\mu H$

7.3 Feedback Capacitor (CFB1) Selection

The feedback capacitor C_{FB1} determines the pulse frequency at no load condition. The corresponding inductor current is shown in Figure 32.

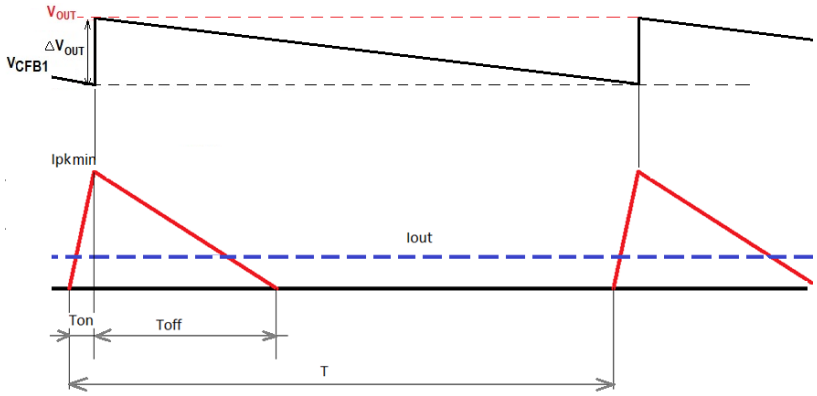


Figure 32. The Inductor Current at No Load Operation

The average output current can be written as Equation 3.

(EQ. 3) $$\frac{I_{PKMIN}(t_{ON} + t_{OFF})}{2T} = I_{OUT\_MIN}$$

Because $t_{ON} << t_{OFF}$, I_{OUT_MIN} can be written as:

$$\frac{I_{PKMIN} t_{OFF}}{2T} = I_{OUT\_MIN}, \text{ where } t_{OFF} = \frac{L I_{PKMIN}}{V_{OUT}}$$

Therefore:

(EQ. 4) $$I_{OUT\_MIN} = \frac{L(I_{PKMIN})^2}{2V_{OUT}T}$$

To have the required input standby power, P_{IN_STBY}, the power delivered to the output should satisfy Equation 5:

(EQ. 5) $$V_{OUT}I_{OUT\_MIN} = P_{IN\_STBY}\eta$$

where η is the light-load efficiency.

Replacing I_{OUT_MIN} with Equation 4 gives you Equation 6.

(EQ. 6) $$V_{OUT}\left(\frac{L(I_{PKMIN})^2}{2V_{OUT}T}\right) = P_{IN\_STBY}\eta$$

The required time interval T is calculated using Equation 7:

(EQ. 7) $$T = \frac{L(I_{PKMIN})^2}{2P_{IN\_STBY}\eta}$$

Because the time interval T is primarily determined by the sampling network, it is related to C_{FB1} in Equation 8:

(EQ. 8) $$C_{FB1} = \frac{V_{OUT}T}{\Delta V_{OUT}(R_{FB1}+R_{FB2})}$$

where ΔV_{OUT} is the output voltage increase above the nominal V_{OUT} at no load.

From Equation 8, it can be seen that a bigger sampling capacitor leads to a smaller ΔV_{OUT}, but C_{FB1} can not be too big as it calls for a huge C_{OUT}. A small ΔV_{OUT} can cause erratic logic function of the internal PFM comparator in mode transition. Therefore, choose ΔV_{OUT} properly according to the highest V_{OUT} allowed in the applications. When ΔV_{OUT} is picked, C_{FB1} is calculated by using Equation 8.

7.4 Output Capacitor Selection

The output capacitor needs to meet the requirement of the output ripple voltage and load transient response. Also, it needs to ensure the slew rate of the output voltage is slower than the discharging rate of the sampling capacitor (C_{FB1}) in a defined step load transient, as shown in Figure 33. Therefore, C_{OUT} is first calculated according to V_{OUT} discharging by Equation 9.

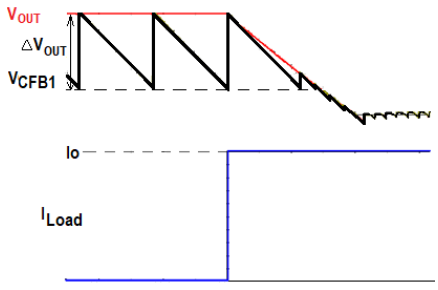


Figure 33. Output Capacitor Discharging at Step Load

(EQ. 9) $$C_{OUT} \geq \frac{C_{FB1}\Delta I_{OUT}(R_{FB1} + R_{FB2})}{V_{OUT}}$$

However, the output capacitor should also be large enough to provide sufficient transient voltage support to load step (if any), as with the pulses being separated with a big time interval at no load the controller most likely cannot detect the voltage change and take action promptly.

(EQ. 10) $$C_{OUT} \geq \frac{\Delta I_{OUT} T}{0.07 V_{OUT}}$$

where 7% voltage drop is used in this example.

7.5 Bias Capacitor Selection

7.5.1 V_{CC} Hold Up Capacitor C_3 Selection

The C_3 capacitor holds up the V_{CC} voltage during PFM mode. In PFM mode, this capacitor provides hold up energy from output to the IC during off-time. This can achieve better light-load efficiency instead of taking energy from the input side. Renesas recommends setting the output ripple voltage smaller than 1V at no load condition with maximum input voltage, which is the worst case with the output capacitor keeping the no-load output voltage from getting too high. Its value is calculated from Equation 11.

(EQ. 11) $$C_3 = \frac{P_{IN\_STBY} \times T \times 2}{V_{OUT}^2 - (V_{OUT} - 1)^2}$$

7.5.2 V_{CC} Capacitor C_{VCC} Selection

The C_{VCC} capacitor filters the V_{CC} voltage and sets the hiccup time when OLP is triggered. After OLP is triggered, the V_{CC} capacitor is discharged by a discharge current, I_{QVCC3}. When the voltage of C_{VCC} drops to 4.5V, the IC restarts, and C_{VCC} is charged by I_{VCC_START} to V_{CC_OFF} again. Therefore, choose C_{VCC} based Equation 12.

(EQ. 12) $$t_{hiccup} = C_{VCC} \times 2 \times \left(\frac{1}{I_{QVCC3}} + \frac{1}{I_{VCC-START}}\right)$$

However, C_{VCC} also protects the V_{CC} voltage from overshoot from C_3 when the chip is shut down. Therefore, for design consideration, the C_{VCC} capacitance should be at least doubled to C_3.

7.5.3 Input Capacitor Selection

Typically, the input capacitance affects the inrush current, and therefore the input fuse and bridge selection. When using a bridge rectifier, the input capacitor is chosen as 1.5 ~ 2µF/W for the universal input condition (Equation 13).

(EQ. 13) $$C_{IN} = V_{OUT} \times I_{OUT} \times 1.5\mu F/W \div \eta$$

where $\eta = 0.75$

7.6 Dummy Resistor Selection

At a no-load condition, the system standby power is determined by the IC quiescent current, feedback resistor bleeding current. If the required standby power is not low and to keep the no-load output voltage from getting too high, a dummy resistor can be added in parallel with the output capacitor. Its value is calculated using Equation 14.

(EQ. 14)
$$R_0 = \frac{V_{OUT}}{\left(\frac{P_{IN\_STBY}\eta}{V_{OUT}} - I_q - \frac{VFB}{R_{FB2}}\right)}$$

where η = 0.4

7.7 Power Capability

The maximum power the RAA223021 can deliver depends on the ambient temperature, output voltage, input voltage, and even PCB thermal design. In general, higher input voltage with lower ambient temperature allows a bit more power than a low input voltage at a higher ambient temperature. Also, it delivers more power at higher output voltages. Table 1 summarizes the maximum power the RAA223021 can deliver with ambient temperature up to 85°C. This table should be used as a reference and may vary because of actual PCB thermal design power capability.

7.8 PCB Layout Guidance

Proper layout is important to ensure a stable operation, good thermal behavior, EMI performance, and reliable operation for various operating environments. Pay attention to the following layout recommendations.

- Leave proper spacing (minimum 1.4mm) between high voltage (max 400V) traces and low voltage traces.
- Keep a small loop from the input filter capacitor to the IC, switching inductor, output capacitor, and to the ground of the input capacitor. Also, a small loop consisting of a switching inductor, output capacitor, and freewheeling diode.
- Keep sufficient copper area on the IC drain and/or source pin for better thermal performance
- Keep the switching inductor away from the input EMI inductor to avoid noise coupling, especially when an unshielded switching inductor is used.
- Place the V_{CC} decoupling capacitor and the FB pin decoupling capacitor close to the pins. A single-sided PCB layout example is shown in Figure 34.

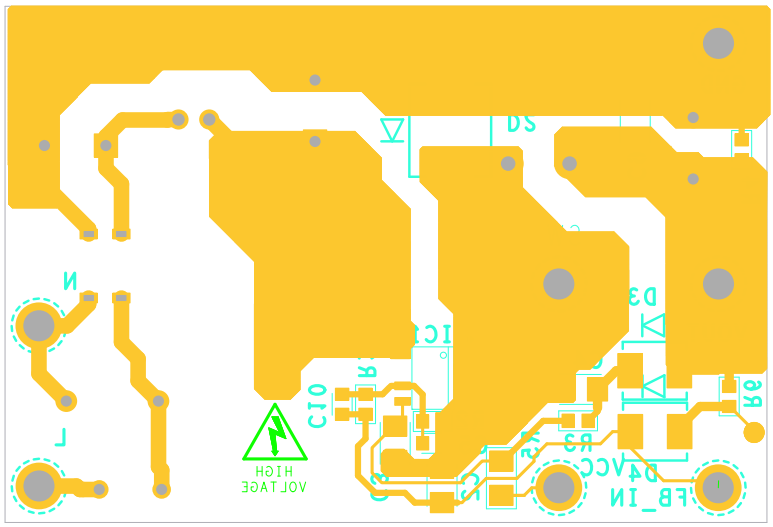


Figure 34. Example PCB Layout

8. EMI Performance

Conducted EMI compliance for EN55022/CISPR22 (12V/600mA output)

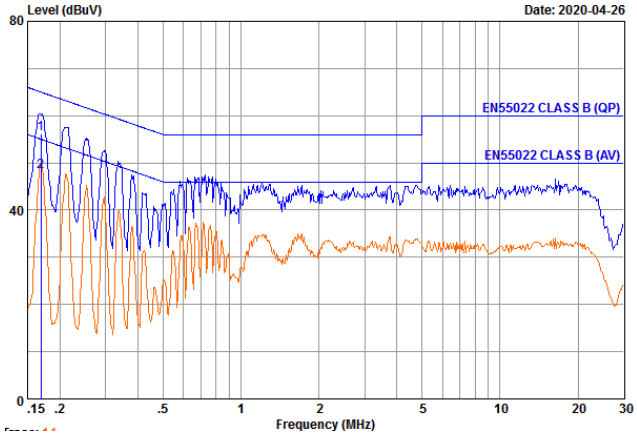


Figure 35. Line, 120V_{AC}

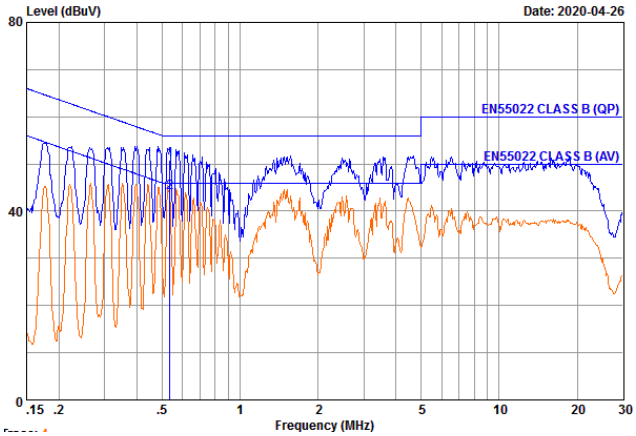


Figure 36. Line, 230V_{AC}

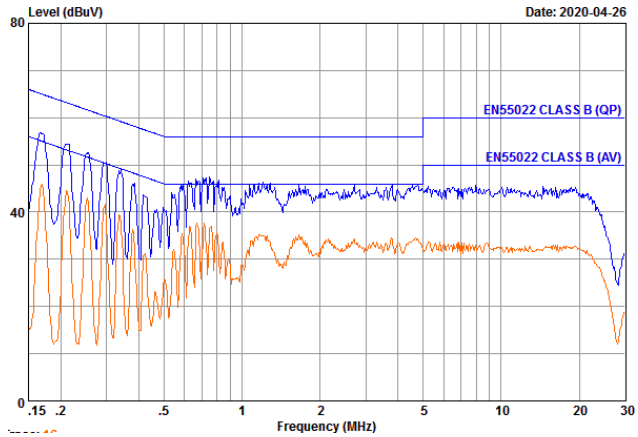


Figure 37. Neutral, 120V_{AC}

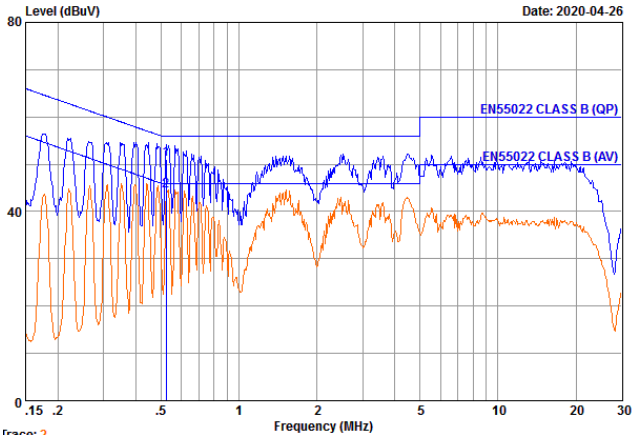


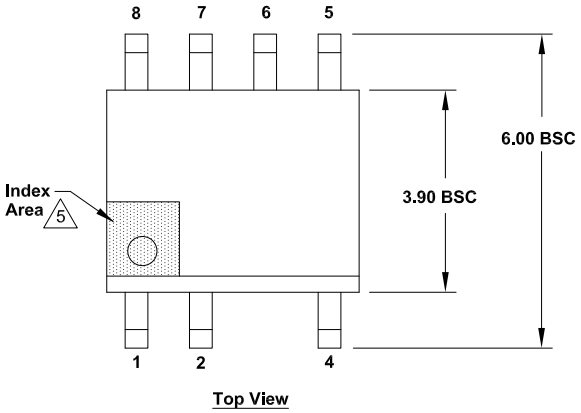
Figure 38. Neutral, 230V_{AC}

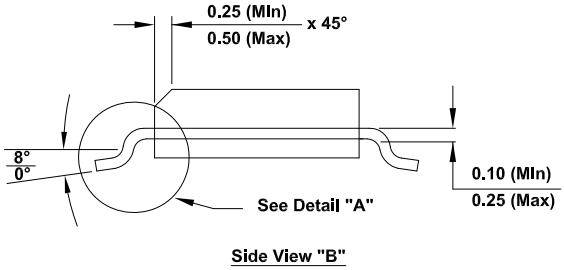
9. Package Outline Drawing

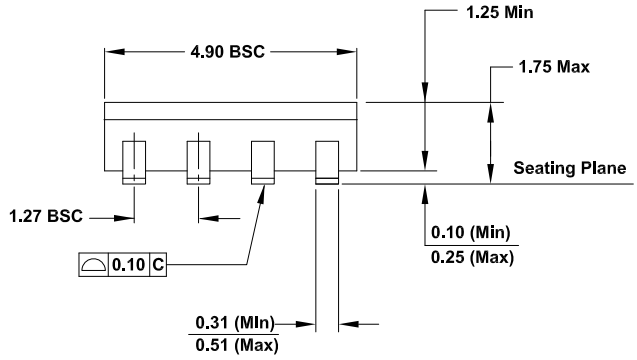
For the most recent package outline drawing, see M7.15A.

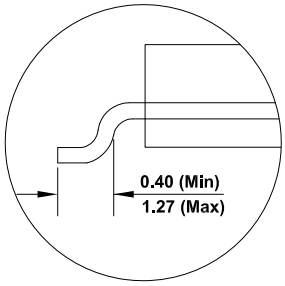
M7.15A

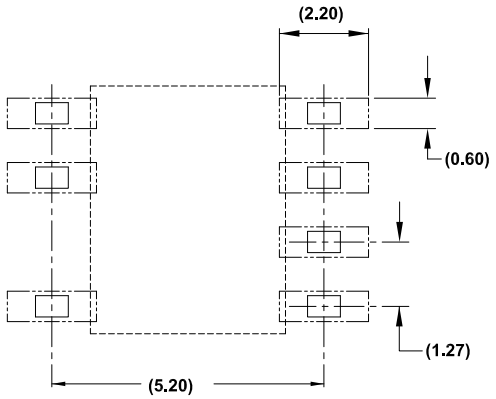
7 Lead Narrow Body Small Outline Plastic Package (SOIC)
Rev 1,12/20











Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.255mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA2230214GSP#AA1	223021	7 Ld SOIC	M7.15A	Tube	-40 to +125°C
RAA2230214GSP#HA1				Reel, 2.5k	
RAA2230214GSP#MA1				Reel, 250	
RTKA223021DE0000BU	Universal input, Buck, 12V, 8W Evaluation Board				
RTKA223021DE0010BU	Universal input, Flyback, 12V, 12W Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA223021 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 2. Key Differences between Family of Parts

Device	$r_{DS(ON)}$ (Ω)	I_{PK} (mA)	t_{OFF_MIN} (µs)	Package Options
RAA223011	14.5	520	32	8 Ld SOIC, 7 Ld SOIC, 5 Ld TSOT
RAA223012	14.5	335	19	8 Ld SOIC, 5 Ld TSOT
RAA223021	4	1100	23	7 Ld SOIC

11. Revision History

Revision	Date	Description
1.02	Dec 7, 2022	Updated the output power listed on page 1 from 8W to 12W. Updated revision numbers to the correct Renesas format.
1.01	May 12, 2021	Updated Table 1: added 24V output setting.
1.00	Feb 12, 2021	Initial release.

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(Rev.1.0 Mar 2020)

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