RAA236100, RAA236105

Ultra-low IQ Buck-Boost Regulators with Bypass

The RAA236100 and RAA236105 (RAA23610x) are highly efficient and integrated synchronous buck-boost regulators. The device features an ultra-low input quiescent current of 130nA in normal regulation mode and <22nA when disabled. It can be programmed to the Forced Bypass mode where the current consumption is 105nA. This power-saving mode can be chosen if voltage regulation is not required. It is accessible using the I^2C interface bus or a pin to allow fast entry/exit.

The device supports input voltages from 1.8V to 5.5V and is designed for stand-alone applications, featuring various default output voltage options at Power-On Reset (POR). After POR, the output voltage can be independently adjusted using the I2C interface bus (RAA236100).

The device can deliver up to 400mA of output current (V_{IN} > 2.5V). It also features pin-controlled Dynamic Voltage Scaling (DVS) with programmable slew rate options.

RAA23610x comes in multiple versions. The RAA236100 uses an I^2C interface to adjust the output voltages in 50mV steps. The RAA236105 uses one pin reader with an external resistor to select output voltages and another to select the input current limit.

The total solution requires as little as a single 0603-size inductor and two external capacitors for full load support. For pin reader options, two additional external resistors are needed.

The RAA23610x is available in a 2.5×2.5mm 10-lead DFN package with 0.5mm pitch. It is specified for operation from -40°C to +85°C ambient temperature range.

Features

- Single output buck-boost converter
- 130nA input quiescent current
- 96% peak efficiency (V_{IN} = 3.6V; V_{OUT} = 3.3V)
- Output current: up to 400mA (V_{IN} > 2.5V, V_{OUT} = 3.3V)
- Input voltage range: 1.8V to 5.5V, supports single-cell Li-ion, 2x or 3×1.5V AA/AAA batteries
- Output voltage range: 1.8V to 5.0V
- Output voltage control using a pin reader (RAA236105)
- Selectable input current limit
- DVS with settable slew rate control
- Selectable forced bypass power saving mode
- PWM/PFM and buck/boost with seamless transition
- Ultrasonic mode for audible noise suppression
- I^2C control and voltage adjustability (RAA236100 only)
  - Standard, Fast, and High-Speed mode
- 10-Ld DFN package
- Pb-free (RoHS compliant)

Applications

- Smart watches/wristbands, wireless earphones
- Internet of Things (IoT) devices
- Water, gas, and oil meters
- Energy harvesting

Versions

- I^2C interface (RAA236100)
- Pin reader output voltage with input current limit (RAA236105)

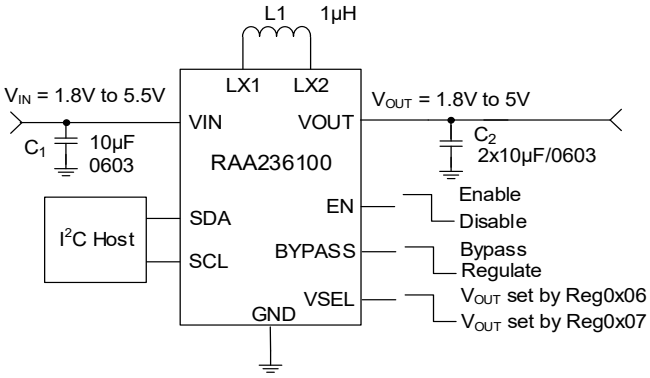


Figure 1. Typical Application (RAA236100)

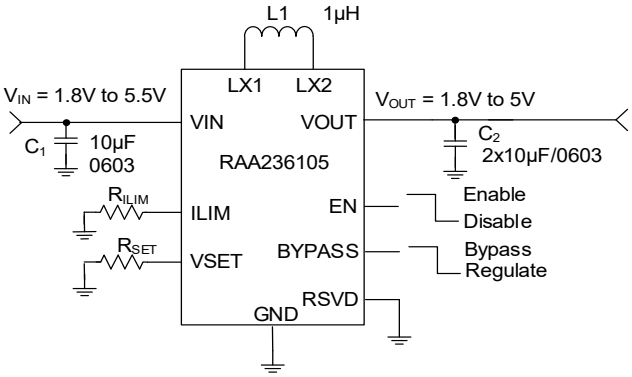


Figure 2. Typical Application (RAA236105)

Contents

1. Overview

1.1 Block Diagram

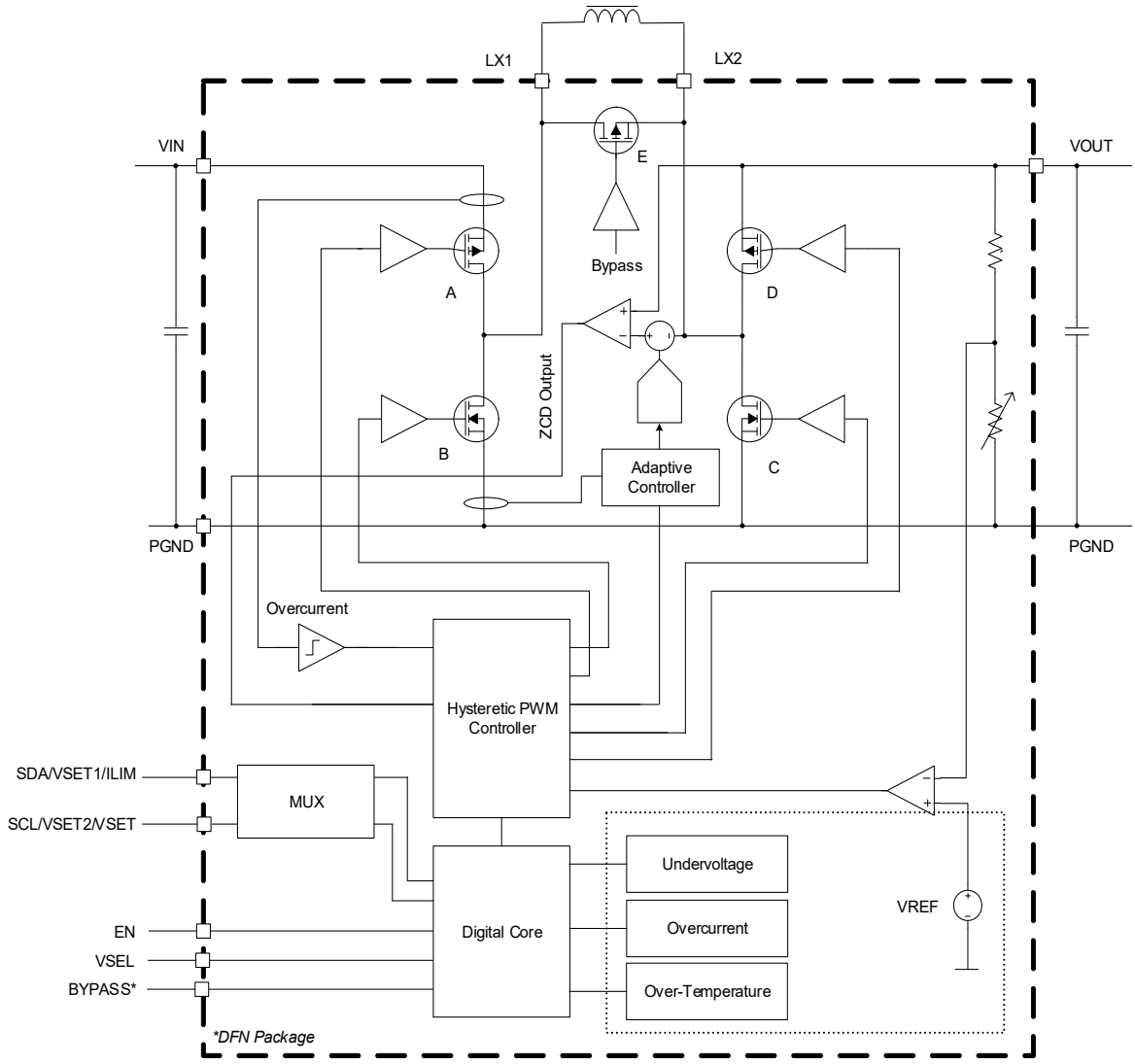


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

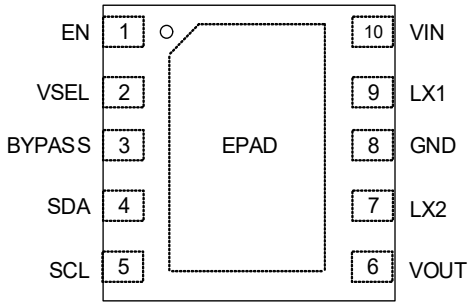


Figure 4. 10 Ld DFN (RAA236100) - Top View

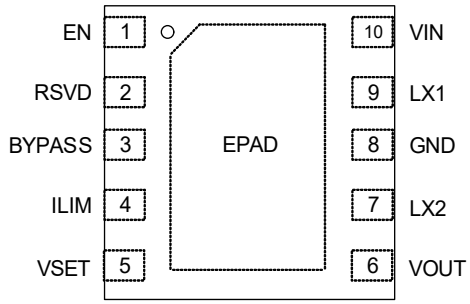


Figure 5. 10 Ld DFN (RAA236105) - Top View

2.2 Pin Descriptions

Table 1. RAA236100 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	EN	Input	Active high, device enable input. Do not leave floating.
2	VSEL	Input	Fast DVS input to select different targets for the output voltage. Do not leave floating.
3	BYPASS	Input	Active high, buck-boost forced bypass control input. Do not leave floating.
4	SDA	Input/Output	I^2C bi-directional serial data connection (high impedance input / open drain output). Pull down to GND if not being used. Do not leave floating.
5	SCL	Input	I^2C serial clock connection (high impedance input). Pull down to GND if not being used. Do not leave floating.
6	VOUT	Output	Buck-boost converter output voltage pin.
7	LX2	Power	Switch node for boost, output side terminal of the inductor.
8	GND	Ground	Main controller ground pin.
9	LX1	Power	Switch node for the buck, input side terminal of the inductor.
10	VIN	Input	Input voltage supply pin.
EPAD	EPAD	Ground	Exposed Pad to optimize thermal performance. Must be soldered and connected to ground on PCB.

Table 2. RAA236105 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	EN	Input	Active high, device enable input. Do not leave floating.
2	RSVD	-	Reserved. Do not leave floating. Pull down to GND.
3	BYPASS	Input	Active high, buck-boost forced bypass control input. Do not leave floating.
4	ILIM	Input	Pin reader input to set the input current limit. Do not leave floating.
5	VSET	Input	Pin reader input to set the output voltage target. Do not leave floating.
6	VOUT	Output	Buck-boost converter output voltage pin.
7	LX2	Power	Switch node for boost, output side terminal of the inductor.
8	GND	Ground	Main controller ground pin.
9	LX1	Power	Switch node for the buck, input side terminal of the inductor.
10	VIN	Input	Input voltage supply pin.
EPAD	EPAD	Ground	Exposed Pad to optimize thermal performance. Must be soldered and connected to ground on PCB.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
VIN, VOUT	-0.3	6.0	V
LX1, LX2	-0.3	6.0	V
LX1, LX2 (less than 10ns)	-2	8	V
All other pins	-0.3	6.0	V
Maximum Junction Temperature (T_J)	-	+125	°C
Maximum Storage Temperature Range (T_S)	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	±2k	V
Charged Device Model (Tested per JS-002-2022)	-	±1k	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. Voltage (to GND unless otherwise stated)

3.2 Recommended Operation Conditions

Parameter[1]	Minimum	Maximum	Unit
Ambient Temperature Range (T_A)	-40	+85	°C
Supply Voltage (V_{IN}) Range	1.8	5.5	V
Load Current (I_{OUT}) Range (DC)	0	400	mA
Effective Output Capacitance (C_{OUT})	6	-	µF
Effective Input Capacitance (C_{IN})	5	-	µF

1. Voltages referred to GND unless otherwise stated.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	10 Ld DFN Package	θ_{JA}[1]	Junction to ambient	75	°C/W
		θ_{JC}[2]	Junction to case	29	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For $\theta_{JC,}$ the case temperature location is the center of the exposed metal pad on the package underside. See TB379.

3.4 Electrical Specifications

V_{IN} = V_{EN} = 4.0V, V_{OUT}= 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise.**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Power Supply						
Input Voltage Range	V_{IN}	-	1.8	-	5.5	V
V_{IN} Undervoltage Lockout Threshold and Hysteresis	V_{UVLO_R}	V_{IN} rising	1.62	-	1.78	V
	$HYST_{UVLO}$	-	35	46	80	mV
V_{IN} Quiescent Current	I_Q	No switching; V_{IN} = 4.0V, V_{OUT} = 3.5V overdriven	-	130	**750**	nA
V_{OUT} Quiescent Current	I_{Q_VOUT}	V_{IN} = 4.0V, V_{OUT} = 3.5V	-	100	140	nA
V_{IN} Supply Current Shutdown	I_{SD}	EN = LOW	-	22	110	nA
V_{IN} Supply Current, Standby (RAA236100)	I_{STBY}	EN = HIGH, shutdown using I^2C register	-	45	150	nA
V_{IN} Supply Current, Forced Bypass Mode	I_{FBYP}	Forced Bypass Mode using I^2C register or V_{BYPASS} = HIGH	-	105	-	nA
Output Voltage Regulation						
Output Voltage Range	V_{OUT}	V_{IN} = 1.8V to 5.5V, I_{OUT} = 1mA	1.8	3.3	5.0	V
Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = 4.0V, V_{OUT} = 3.3V I_{OUT} = 1mA, PFM	**-3.0**	-	**+3.0**	%
		V_{IN} = 4.0V, V_{OUT} = 3.3V I_{OUT} = 100µA, PWM	**-3.0**	-	**+3.0**	%
Output Voltage Resolution	V_{OUT_STEP}	I^2C enabled	-	50	-	mV
Output Voltage Resolution Pin Reader	$V_{OUT\_STEP\_PR}$	I^2C disabled; Pin Reader enabled (RAA236105)	-	100	-	mV
Output Voltage Ripple	V_{OUT_RIP}	V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM mode	-	80	-	mV_{P-P}
		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PWM mode	-	15	-	mV_{P-P}
Load Regulation	$V_{OUT\_LOAD\_REG}$	V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{LOAD} 0mA vs. 400mA	-	±1	-	%
Line Regulation	$V_{OUT\_LINE\_REG}$	V_{OUT} = 3.3V, I_{LOAD} = 120mA, V_{IN} 1.8V vs. 5.5V	-	±0.5	-	%
Soft-Start and Soft Discharge						
Time to read OTP (RAA236100)	t_{OTP_I2C}	Time from when V_{IN} > V_{UVLO_R} and EN signal asserts to when output voltage ramp starts. V_{IN} ramp rate faster than 3V/ms	-	400	-	µs

V_{IN} = V_{EN} = 4.0V, V_{OUT}= 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Time to read OTP (RAA236105)	t_{OTP_PR}	Time from when V_{IN} > V_{UVLO_R} and EN signal asserts to when output voltage ramp starts. V_{IN} ramp rate faster than 3V/ms	-	400	-	µs
V_{OUT} Ramp Rate for Soft-Start	DVSRATE	Default at POR	-	3.125	-	mV/µs
		Programmable using I^2C after POR (only RAA36100)	-	6.25 1.5625 0.78125	-	mV/µs
V_{OUT} Soft Discharge Resistance (RAA236100)	r_{DISCHG}	EN < EN_{IL} or shutdown using I^2C register	-	125	-	Ω
Inrush current amplitude	I_{RUSH}	I_{OUT} = 1mA, output cap C_2 as specified. Does not include current into input cap C_1	-	0.5	-	A
P-Channel MOSFET ON-Resistance (Buck)	$r_{DS(ON)\_A}$	V_{IN} = 3.6V, V_{OUT} = 3.6V	-	90	-	mΩ
N-Channel MOSFET ON-Resistance (Buck)	$r_{DS(ON)\_B}$		-	90	-	mΩ
P-Channel MOSFET ON-Resistance (Boost)	$r_{DS(ON)\_D}$		-	90	-	mΩ
N-Channel MOSFET ON-Resistance (Boost)	$r_{DS(ON)\_C}$		-	90	-	mΩ
P-Channel MOSFET ON-Resistance (Bypass)	$r_{DS(ON)\_E}$		-	1.3	-	Ω
Inductor Peak Current Limit						
Peak Current Limit	I_{LIM}	2.5V < V_{IN} ≤ 5.5V	-	2	-	A
		1.8V ≤ V_{IN} ≤ 2.5V	-	1.8×(V_{IN}/2)	-	A
Output Current						
Maximum Load Current[3]	I_{OUT_MAX}	V_{IN} and V_{OUT} ≥ 2.5V (Buck Mode)	400	-	-	mA
Maximum Current Derating at Minimum V_{IN}[3]	$I_{OUT\_MAX\_DERATING}$	V_{IN} = 1.8V, V_{OUT} = 5.0V	86.4	-	-	mA

V_{IN} = V_{EN} = 4.0V, V_{OUT}= 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Input Current Limit Function (RAA236100 and RAA236105)						
Average Current Limit on the input	I_{CL}	V_{IN} = 4.0V, V_{OUT} under ridden, I_{CL} setting=1mA	-	1	-	mA
		V_{IN} = 4.0V, V_{OUT} under ridden, I_{CL} setting=2mA	-	2	-	mA
		V_{IN} = 4.0V, V_{OUT} under ridden, I_{CL} setting=5mA	-	5	-	mA
		V_{IN} = 4.0V, V_{OUT} under ridden, I_{CL} setting=10mA	-	10	-	mA
		V_{IN} = 4.0V, V_{OUT} under ridden, I_{CL} setting=20mA	-	20	-	mA
		V_{IN} = 4.0V, V_{OUT} under ridden, I_{CL} setting=50mA	-	50	-	mA
Efficiency						
Efficiency	η	V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 50mA	-	94	-	%
		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 50mA	-	96	-	
		V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 50mA	-	91	-	
		V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 10µA	-	92	-	
		V_{IN} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 10µA	-	92	-	
		V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 10µA	-	86	-	
Switching Frequency						
Regulator switching frequency	f_{SW_PWM}	V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 1mA, Forced PWM	-	2.0	-	MHz
	f_{SW_US}	V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0mA, Ultrasonic Mode (RAA236100)	-	42	-	kHz
Fault Management						
Hiccup Time	t_{HICCUP}	Fault occurrence time from shutdown to restart	-	100	-	ms
Thermal Shutdown Temperature	T_{SD}	Temperature Rising	-	140	-	°C
Thermal Shutdown Hysteresis	T_{SD_HYST}	Temperature Falling	-	20	-	°C

V_{IN} = V_{EN} = 4.0V, V_{OUT}= 3.3V, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (1.8V to 5.5V), unless specified otherwise. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Logic Levels						
Input Leakage	I_{LEAK}	EN pin, (V_{IN} = 3.6V)	-	-	70	nA
		SCL pin, (V_{IN} = 3.6V)	-	-	25	
		SDA pin, (V_{IN} = 3.6V)	-	-	25	
		LX1 pin, (V_{IN} = 3.6V)	-	-	160	
		LX2 pin, (V_{IN} = 3.6V)	-	-	160	
		VSEL pin, (V_{IN} = 3.6V)	-	-	70	
		BYPASS pin (DFN package), (V_{IN} = 3.6V)	-	-	25	
EN/VSEL/ BYPASS Input High Voltage	$EN/VSEL/BYP_{IH}$	-	1.45	-	-	V
EN/VSEL/BYPASS Input Low Voltage	$EN/VSEL/BYP_{IL}$	-	-	-	0.4	V
SCL/SDA Input High Voltage (RAA236100)	SCL/SDA_{IH}	-	1.45	-	-	V
SCL/SDA Input Low Voltage (RAA236100)	SCL/SDA_{IL}	-	-	-	0.4	V

1. All the C_{OUT} listed in Test Condition area are nominal values (not derated), unless stated as derated or effective. For details on the recommended components, see External Component Selection.
2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
3. Parameters established by bench testing and/or design. Not production tested.

4. Typical Performance Curves

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, f_{SW} = 2MHz, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise.

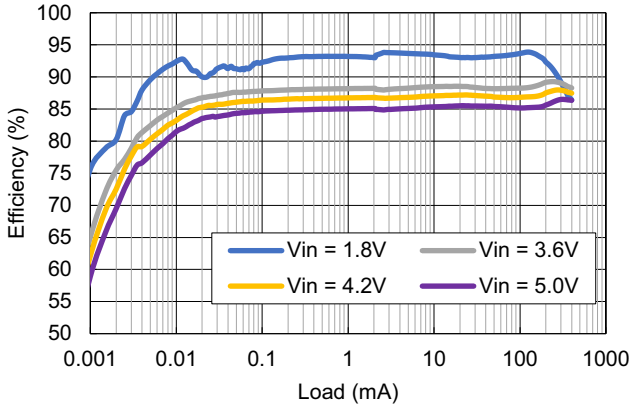


Figure 6. Efficiency vs Load Current: V_{OUT} = 1.8V, T_A = +25°C

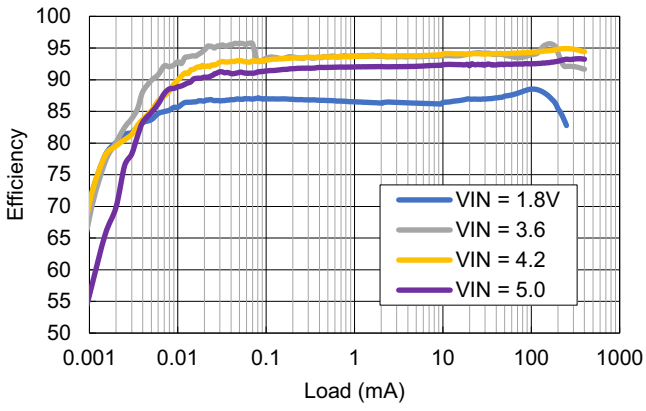


Figure 7. Efficiency vs Load Current: V_{OUT} = 3.3V, T_A = +25°C

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, f_{SW} = 2MHz, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise. (Cont.)

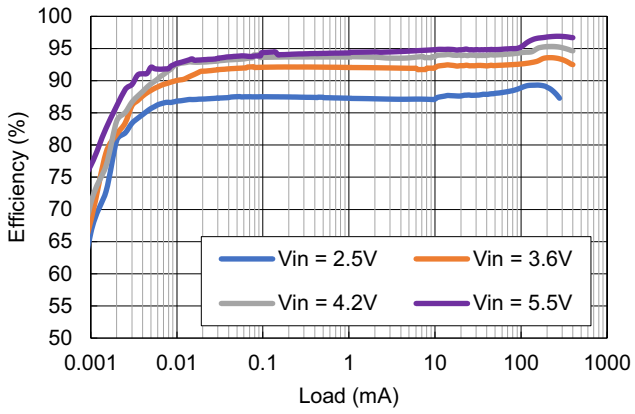


Figure 8. Efficiency vs Load Current: V_{OUT} = 5.0V, T_A = +25°C

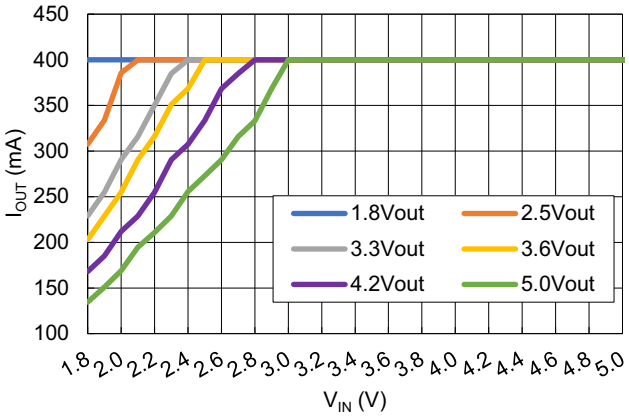


Figure 9. Maximum Load Current vs. Input Voltage

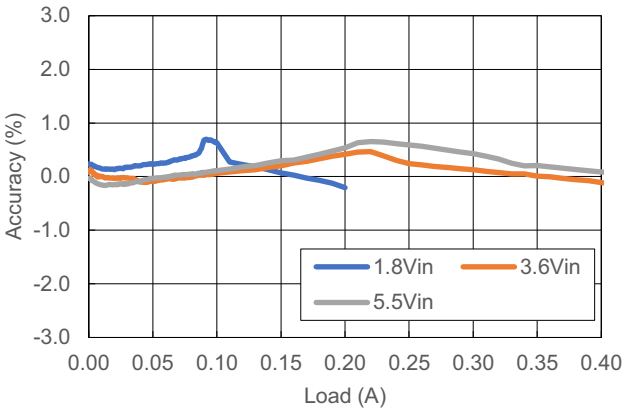


Figure 10. Output Voltage Accuracy vs. Load Current, V_{OUT} = 3.3V

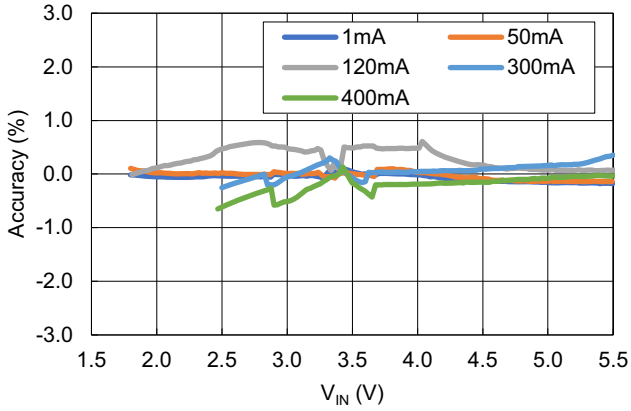


Figure 11. Output Voltage Accuracy vs. Input Voltage, V_{OUT} = 3.3V

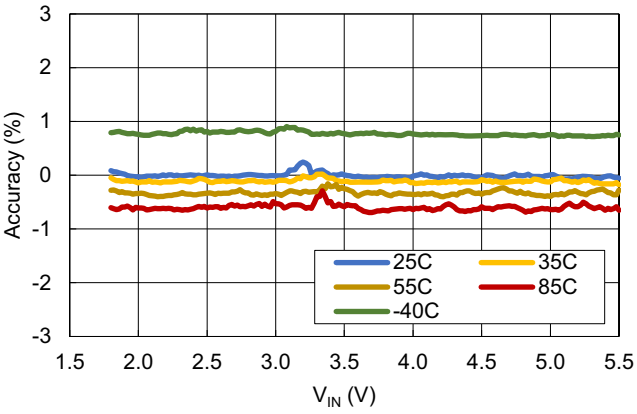


Figure 12. Output Voltage Accuracy vs V_{IN} vs Temperature, V_{OUT} = 3.3V, no load

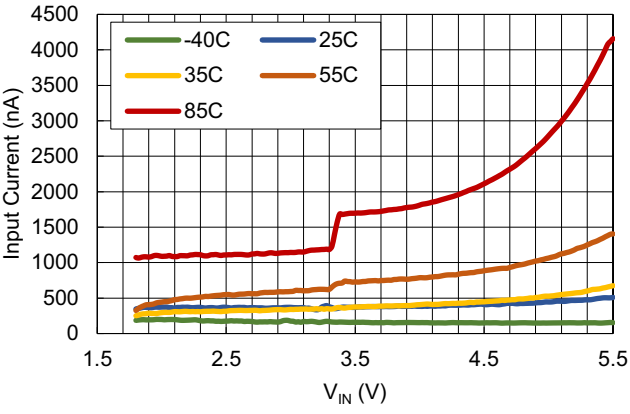


Figure 13. Input Switching Current vs V_{IN} vs Temperature, V_{OUT} = 3.3V, no load

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, f_{SW} = 2MHz, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise. (Cont.)

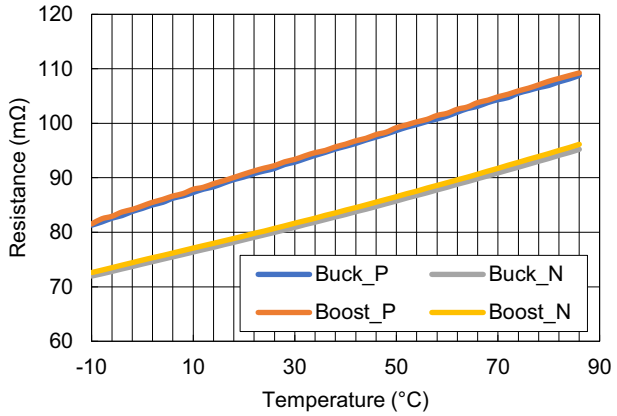


Figure 14. Switch Resistance (DFN) vs Temperature

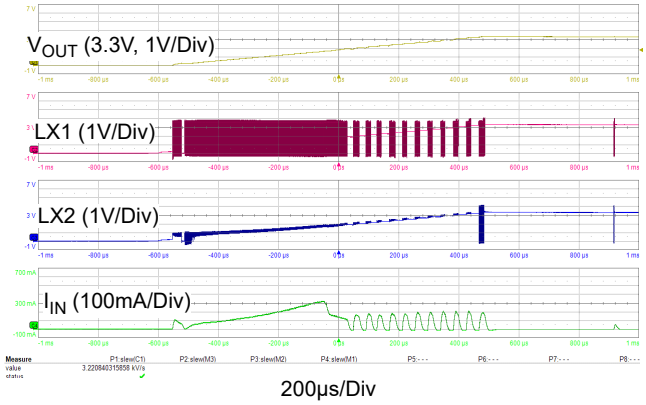


Figure 15. Inrush Current: V_{IN} = 3.6V, V_{OUT} = 3.3V

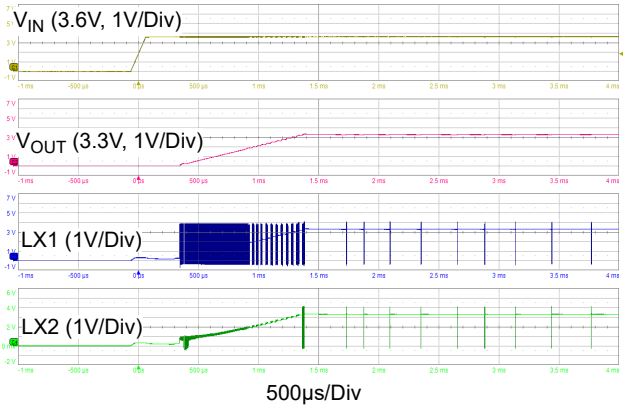


Figure 16. Soft-Start with Fast VIN Ramp Rate

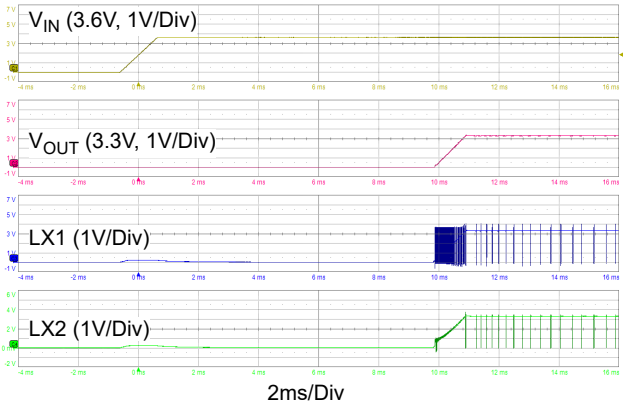


Figure 17. Soft-Start with Slow VIN Ramp Rate

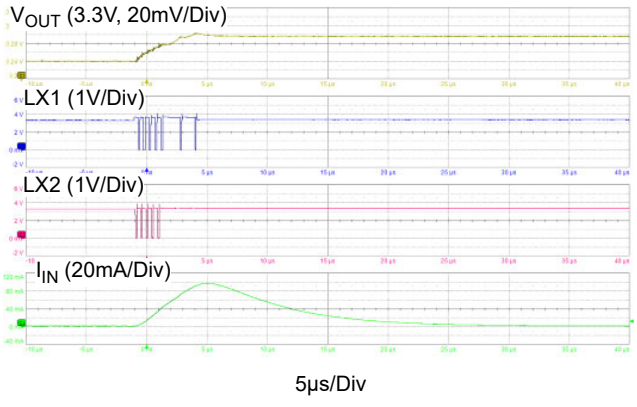


Figure 18. Steady State, PFM mode, Load = 3.3MΩ

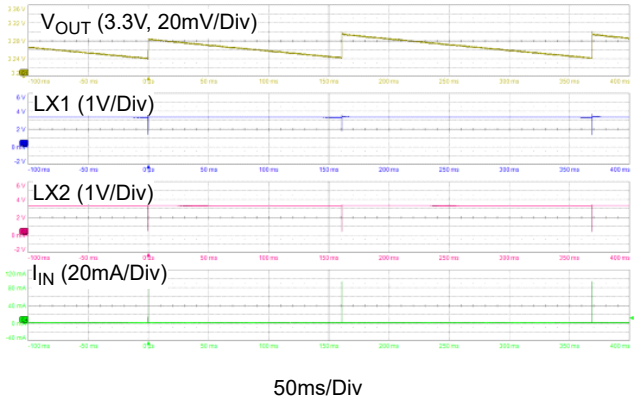


Figure 19. Steady State, PFM mode, Load = 3.3MΩ

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, f_{SW} = 2MHz, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise. (Cont.)

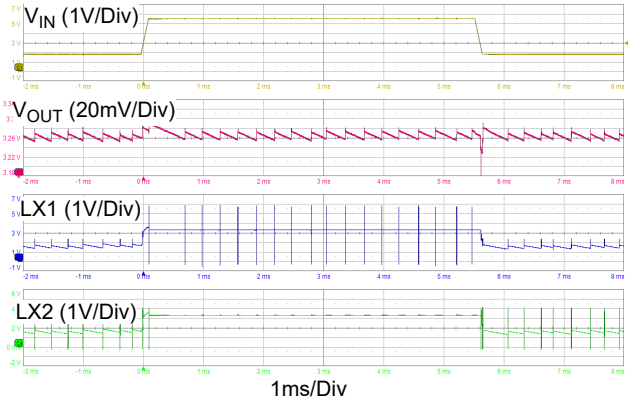


Figure 20. Line Transient: V_{OUT} = 3.3V; 1mA Load

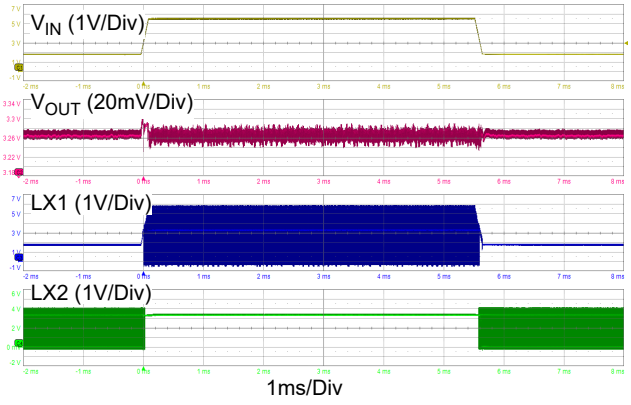


Figure 21. Line Transient: V_{OUT} = 3.3V; 130mA Load

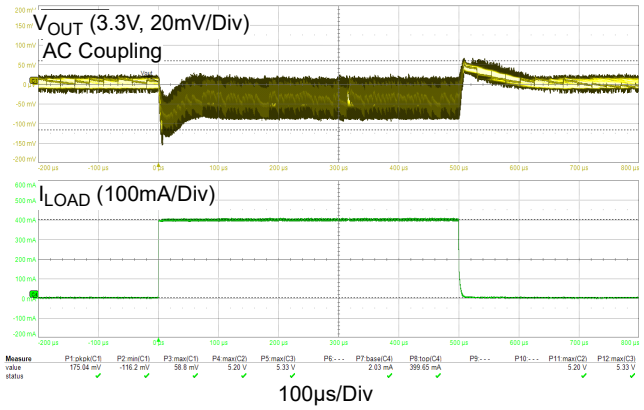


Figure 22. Load Transient: V_{IN} = 3.6V, V_{OUT} = 3.3V, Load Current = 3mA - 400mA Pulsing, US Frequency

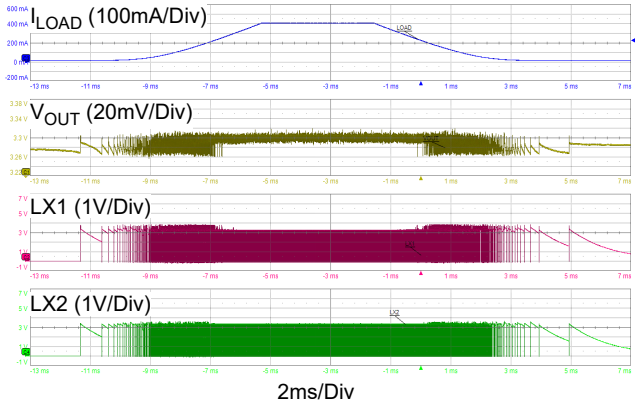


Figure 23. PFM-PWM Transition: V_{IN} = 3.3V, V_{OUT} = 3.3V, Load Current = 1mA - 400mA Ramping

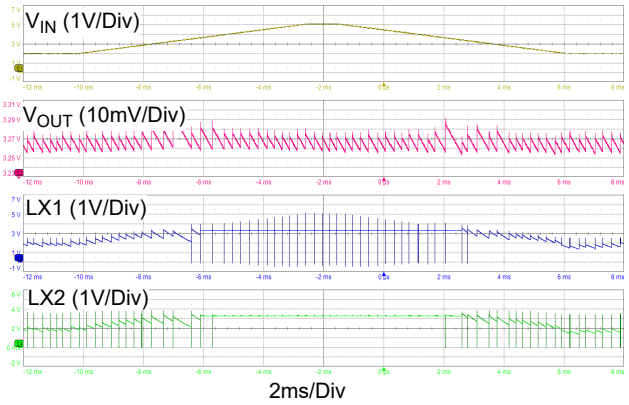


Figure 24. Buck-Boost Transition: V_{OUT} = 3.3V; Load = 1mA, PFM mode

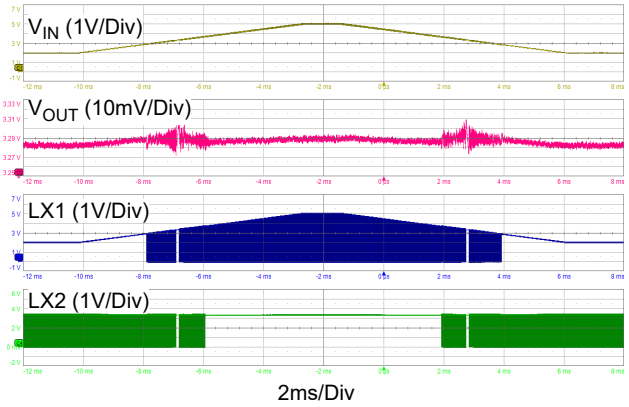


Figure 25. Buck-Boost Transition: V_{OUT} = 3.3V; Load = 1mA, Forced PWM mode

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 3.3V, f_{SW} = 2MHz, I^2C pull-up voltage = V_{IN}, L_1 = 1µH, C_1 = 10µF, effective C_2 = 6µF, T_A = +25°C, unless specified otherwise. (Cont.)

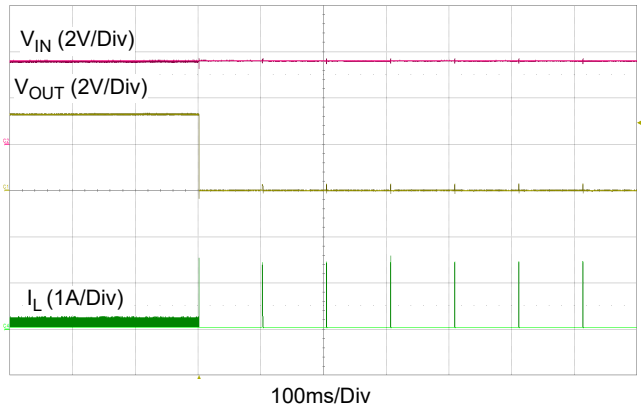


Figure 26. Output Short-Circuit Behavior; Hiccup Mode

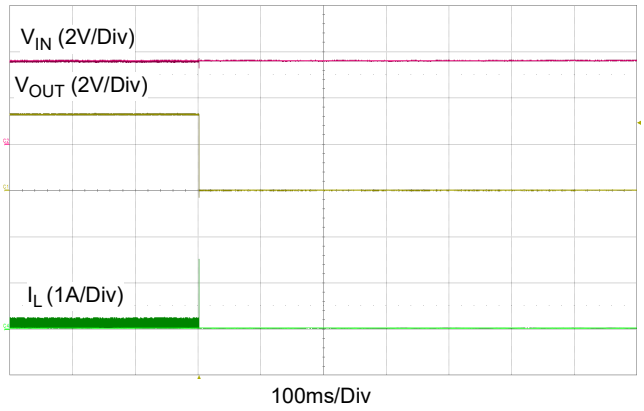


Figure 27. Output Short-Circuit Behavior; Shutdown Mode

5. Functional Description

The RAA236100 integrates a complete buck-boost switching regulator with a PWM controller, internal switches, voltage reference, protection circuitry, and control circuits. A block diagram of the IC can be seen in Figure 3. The PWM controller automatically switches between Buck and Boost modes to maintain a steady output stage with changing input voltages and dynamic external loads in this non-inverting four-switch buck-boost. Transitions between PFM and PWM modes are seamless as well.

5.1 Output Voltage and VSEL for RAA236100 (I^2C Variant)

The buck-boost converter output voltage settings are contained in the bckBst_0 and bckBst_1 registers, addresses 0x07 and 0x06, respectively. The following equations show that the output voltage can be set in 50mV steps using these registers. The dedicated voltage selection (VSEL) pin can be used to select which register value is used, with the target taken from the bckBst_0 register when VSEL is low and bckBst_1 when high. The seven LSB of bckBst_0 and bckBst_1 registers are for the output voltage setting.

- If VSEL is LOW, V_{OUT} = 1.8V + bckBst_0[6:0] × 50mV
- If VSEL is HIGH, V_{OUT} = 1.8V + bckBst_1[6:0] × 50mV

The output voltage range is digitally limited to 5.0V. Setting values above this limit results in the output voltage ramping up to the limit and staying there. The output voltage can be changed after the IC is enabled and operating by writing over these registers or using the VSEL pin. When the output voltage changes, it ramps at the rate set using the bckBst slew rate bits of the STARTUP DISCHARGE register.

5.2 Output Voltage and Input Current Limit for RAA236105 (Current Limit variant)

In this version, the pin readers determine the output voltage level and the input current limit. The trade-off is that the DVS capability is unavailable as only one pin sets the output voltage. The resistance reading on ILIM determines the input current limit and the output voltage in conjunction with the resistance reading on VSET. The resistance on VSET determines the precise output voltage target in 100mV steps. In contrast, the resistance on ILIM determines whether the output is on the lower or upper half of the output range. Table 3 and Table 4 provide the complete set of decoded combinations.

Table 3. Pin Reader Resistor (R_{EXT}) Decoding for Current Limit

Resistance on I_{LIM} (Ω)	Input Current Limit (mA)
0k	Disabled
3.01k	1
6.81k	2
11.5k	5
17.4k	10
24.9k	20
34.0k	50
60.4k	Disabled
76.8k	1
100k	2
127k	5
162k	10

Table 3. Pin Reader Resistor (R_{EXT}) Decoding for Current Limit (Cont.)

Resistance on I_{LIM} (Ω)	Input Current Limit (mA)
205k	20
261k	50

Table 4. Pin Reader Resistor (R_{EXT}) Decoding for Output Voltage

Resistance on VSET (Ω)	V_{OUT} (V)	
	If resistance on ILIM is between 0kΩ and 34kΩ	If resistance on ILIM is between 60.4kΩ and 261kΩ
0k	1.8	3.4
3.01k	1.9	3.5
6.81k	2.0	3.6
11.5k	2.1	3.7
17.4k	2.2	3.8
24.9k	2.3	3.9
34.0k	2.4	4.0
45.3k	2.5	4.1
60.4k	2.6	4.2
76.8k	2.7	4.3
100k	2.8	4.4
127k	2.9	4.5
162k	3.0	4.6
205k	3.1	4.7
261k	3.2	4.8
332k	3.3	5.0

The pin reader resistors must be selected from the E96 series resistors, which have a 1% tolerance. Changing resistance at ILIM/VSET pins after the part has started does not change the input current limit and output voltage as the reading is done only once during startup. There is no option to change output voltage using VSEL for this chip variant.

5.3 Power-On Sequencing

5.3.1 RAA236100

The power-on sequence begins when EN is asserted high for more than 5µs, and the input voltage exceeds the undervoltage lockout threshold. First, the IC is initialized, and its One-Time Programmable (OTP) memory is read. After the OTP has been read and the controller knows the target output voltage and ramp rate, soft-start begins, and the output voltage rises at the default ramp rate until it reaches the target output voltage.

The I^2C interface (RAA236100) is active within 120µs of EN going high and remains active as long as VIN>UVLO.

During soft start, the output voltage and current limit are ramped to their final values to control inrush and the rate at which VOUT comes up. VOUT ramp rate is about 3.12V/ms. A typical power-on sequence is seen in Figure 28.

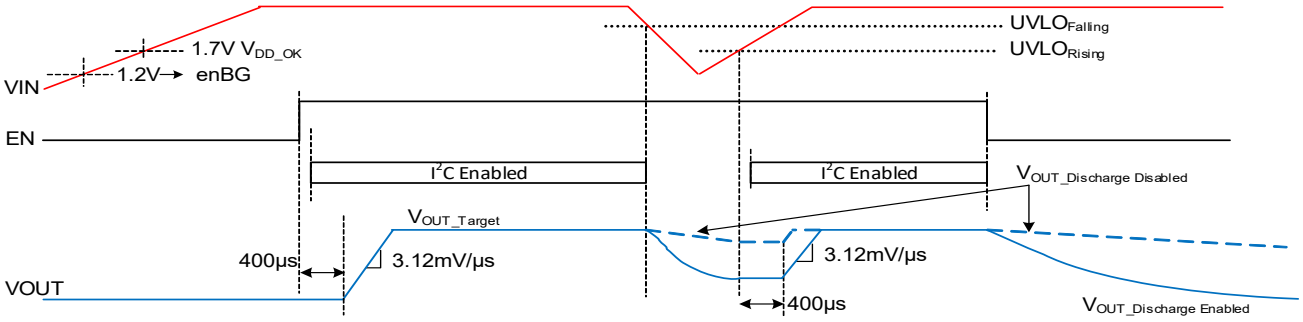


Figure 28. RAA236100 Power-On Sequence

New target voltage levels are accepted and actioned at all times after the I^2C interface is activated. If the output voltage level is changed, either by writing to the selected output voltage register (bckBst_0 or bckBst_1) or by changing the state of the VSEL pin or VSEL override bits in the ENABLE register, the converter slews to the new value at 3.12mV/µs.

EN pin can be tied to the PVIN. See Electrical Specifications for pin capability.

Driving EN LOW invokes Power-Down mode in which most internal device functions are disabled, including I^2C communications. When the device is disabled by driving EN LOW, the output discharges. Driving EN LOW does not reset the register values.

5.3.2 RAA236105

As the EN asserts high, internal calibration is carried out on the pin reader versions. Based on the values of external resistors on the VSETx pins, VOUT ramps up to the desired target voltage. On the RAA236105, the current limit is set by the external resistor on the ILIM pin

EN pin can be tied to the PVIN. See Electrical Specifications for pin capability.

Driving EN LOW invokes Power-Down mode, in which most internal device functions are disabled. When the device is disabled by driving EN LOW, the output discharges naturally based on the load current.

5.4 VIN Ramp Rate

If V_{IN} ramps up at a rate slower than 6.5V/ms, which corresponds to the time between POR and UVLO (time for the BG to enter low power mode from enable), the start-up time is increased by a further 12ms. In a typical case when V_{IN} = 3.6V, if ramp time > 500µs, the start-up time is increased by 12ms.

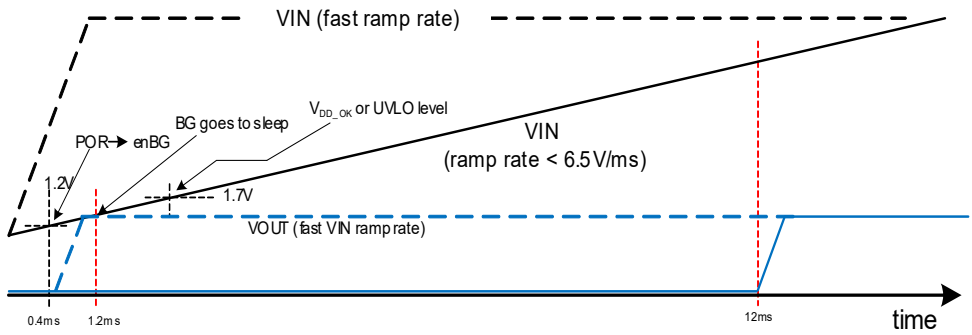


Figure 29. VIN Ramp Rate

5.5 Input Current Limit (ICL)

The RAA236100 features a programmable average input current limit ranging from 1mA to 50mA, which can be set by Reg0x00 [2:0]. The ICL should not be changed on the fly. To enable or select the current limit levels, the output first needs to be disabled by resetting the Regulator EN bit (Reg0x00 [4] = 0'b) before making the change in ICL setting. When the ICL setting is done, the output can be enabled (Reg0x00[4] = 1'b). The input current limit function cannot include the current that goes into the input capacitors. This function is not available in forced PWM mode.

Input current control works in PFM only. It regulates the time between PFM pulses. When ICL is enabled, the modulator tri-states switch D (Figure 31) in the buck tri-state, resulting in lower efficiency.

On the RAA236105, the current limit is set by an external resistor on the ILIM pin.

5.6 Dynamic Voltage Scaling (DVS)

The RAA236100 also features pin-controlled Dynamic Voltage Scaling (DVS) with programmable slew rate options. There are two banks of registers to store two different target voltages: Reg0x06 and Reg0x07. The VSEL pin determines the selected output bank. Do not leave the VSEL pin floating. If VSEL is LOW, the value of Reg0x07 decides the V_{OUT} target. However, if VSEL is HIGH, V_{OUT} is determined by the value of Reg0x06.To help slew down to the lower voltage target quickly, there is an option for the converter to enter forced PWM mode when slewing down (Reg0x0C [3]).

This option is not available on the RAA236105.

5.7 Soft Discharge

An internal discharge resistor between VOUT and PGND can be activated to discharge the output capacitor slowly. This internal discharge resistor has a typical resistance of 130Ω. The soft discharge function is accessed using I^2C while keeping the EN pin high. Using the STARTUP/DISCHARGE register, set the Discharge_enable bit to 1 and disable the IC by setting the Regulator_enable bit to 0. In case of a WOC or OTP fault, this setting overrides the response to a fault in the Reg0x08 [3:0] setting.

All devices, excluding the RAA236100, are discharged naturally based on the load current.

5.8 Device Protection

The RAA236100 features extensive protection mechanisms to handle failure conditions and protect the IC and application from damage automatically, including cycle-by-cycle monitoring of inductor current, V_{OUT} under regulation level, and die temperature. Monitoring V_{OUT} and inductor current begins after the soft-start is complete and ends when the regulator is disabled.

Fault conditions are monitored and reported by the FAULT REPORT register. Latched faults are actioned as defined by the FAULT CONFIG MASTER register. Clear the latched faults by writing 0 to the registers, setting EN low, or V_{IN}<UVLO.

The Fault Report is not available in pin reader options (RAA236105).

5.8.1 Undervoltage Lockout (UVLO)

When V_{IN} falls below the UVLO_falling level, the RAA236100 is disabled. Configure the output to be actively discharged using the internal discharge resistor (soft-discharge) or discharge naturally based on the load current. All devices, excluding the RAA236100, are discharged naturally based on the load current.

V_{IN} must go below 1.1V for more than 5µs to soft-reset (POR).

5.8.2 Overcurrent and Undervoltage Protection

The fault of overcurrent (way-overcurrent, WOC) and undervoltage are OR'ed together, shown as BUBO WOC in the FAULT REPORT register. The RAA236100 provides overcurrent protection by monitoring the inductor current. When the peak inductor current hits its current limit, the BUBO WOC latched bit is set high in the FAULT REPORT register. When the BUBO WOC Latched bit is set, the IC enters Hiccup mode, a hard shutdown, or No action mode according to the setting of the FAULT_CONFIG register (RAA236100). During Hiccup mode, the IC shuts down for 100ms and then tries to restart. The WOC feature is disabled during the soft start.

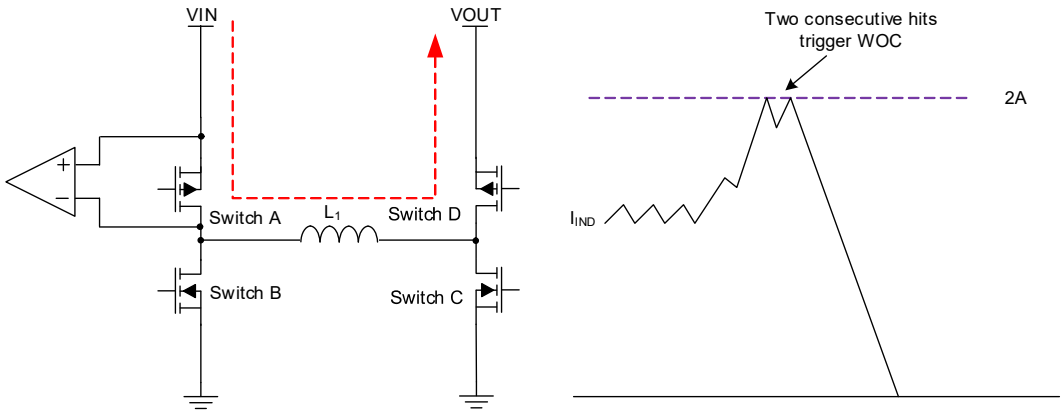


Figure 30. Overcurrent Protection

When the output voltage is <1.6V, the BUBO WOC Latched bit is set high in the FAULT REPORT register. The RAA236100 can be configured to ignore the fault or shut down. If shut down, it can be configured to restart in 100ms or stay shut down.

For the pin reader part, when the WOC and/or Undervoltage occurs, the IC enters Hiccup mode. During Hiccup mode, the IC shuts down for 100ms and then tries to restart.

5.8.3 Thermal Shutdown

The RAA23610x features a thermal shutdown that protects the device from damage due to overheating. When the temperature exceeds T_{SD}, the device stops switching. When the temperature falls by T_{SDHYS}, the controller first goes through the soft-start phase and then starts regulating at the target output voltage as defined by the I^2C register value or the external resistors.

5.9 Output Discharge and Pre-Bias Startup

The RAA236100 has an internal discharge resistance that can be enabled/disabled. However, if the discharge resistor is disconnected (disabled) or the discharge resistance is not sufficient to discharge the load during the time in {SHUTDOWN} or {STANDBY} state, the output capacitor may have residual charge and thus a non-zero output voltage at (re)start (such as pre-biased). The converter turns back on (without fully discharging the output to ground) and does not allow negative current flow into ground or VIN.

5.10 Audible Noise Prevention

The RAA236100 restricts the minimum buck-boost switching frequency to prevent it from switching down into/near the audible frequency range under light or no-load conditions.

The audible noise prevention can be enabled/disabled by FMODE bits in the CONFIG register (ultrasonic frequency switching), and the low-frequency limit is about 35kHz. When ultrasonic frequency switching is enabled, and before lowering the target VOUT setting, the Slew Mode must be set to enable FPWM slew down (Reg0x0C Bit[3] = 1'b) to prevent excessive negative current flowing into ground or VIN.

This feature is not available in the pin reader option (RAA236105).

5.11 Buck-Boost Conversion Topology

The RAA23610x operates in either a pure Buck or a pure Boost mode. When operating in conditions in which VIN is close to V_{OUT}, the RAA23610x alternates between Buck and Boost mode as necessary to provide a regulated output voltage.

Figure 31 shows a simplified diagram of the internal switches and an external inductor.

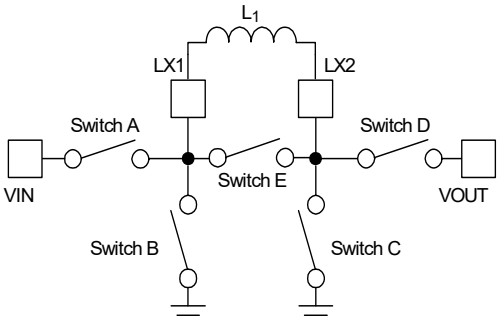


Figure 31. Buck-Boost Topology

5.11.1 Pulse Width Modulation (PWM) Operation

In Buck PWM mode, Switch D is kept permanently closed, and Switch C is permanently open. Switches A and B operate as in a synchronous buck converter. Initially, Switch A is turned ON, and this ramps up the inductor current with a slope of $(V_{IN} - V_{OUT})/L$ (in buck mode, $V_{IN} > V_{OUT}$). When the inductor current hits the upper threshold, as dictated by the hysteretic controller, Switch A is turned OFF. This is followed by a small dead time where both the switches are OFF. During this interval, the inductor current keeps flowing, finding its path through the body diode of Switch B. When the dead time is over, Switch B is turned ON, and the inductor current ramps down with a slope of $-(V_{OUT})/L$. When it hits the lower hysteretic threshold, Switch B is turned OFF, followed by another dead-time interval. After this, Switch A is turned ON again, and the entire sequence repeats.

In Boost PWM mode, Switch A is kept permanently closed, and Switch B is permanently open. Switches C and D operate as in a synchronous boost converter. Initially, Switch C is turned ON, and this ramps up the inductor current with a slope of V_{IN}/L. When the inductor current hits the upper threshold, as dictated by the hysteretic controller, Switch C is turned OFF. This is followed by a small dead time where both the switches are OFF. During this interval, the inductor current keeps flowing, finding its path through the body diode of Switch D. When the dead time is over, Switch D is turned ON, and the inductor current ramps down with a slope of $(V_{IN} - V_{OUT})/L$ (in boost mode, $V_{IN} < V_{OUT}$). When it hits the lower hysteretic threshold, Switch D is turned OFF, followed by another dead-time interval. After this, Switch C is turned ON again, and the entire sequence repeats.

The device operates in PWM mode under two conditions: load is sufficiently high in the Normal Mode (Auto PFM/PWM mode), or Forced PWM mode is enabled by setting the FMODE bits in the CONFIG register to 0x01.

The optimal switching frequency is determined by the hysteretic controller and is centered around 2.0MHz, for V_{IN} = 3.6V and V_{OUT} = 1.8V.

5.11.2 Pulse Frequency Modulation (PFM) Operation

During PFM operation in Buck mode, Switch D is kept permanently closed, and Switch C is permanently open. Switches A and B operate in Discontinuous Conduction Mode (DCM). Just like the Buck PWM operation, Switch A is turned ON, followed by a dead time, and then Switch B is turned ON. The inductor current ramps up and down, respectively, and the energy contained in this current pulse charges up V_{OUT}. After this, unlike the PWM operation, both switches remain OFF until V_{OUT} discharges down to the lower threshold of the hysteretic controller. The switching cycle repeats after that.

During PFM operation in Boost mode, unlike Buck mode, Switch A is not kept permanently closed, although Switch B does remain permanently open. Switches C and D operate in DCM. At the start of the PFM pulse, Switch

A is turned ON. Then, just like the Boost PWM operation, Switch C is turned ON, followed by a dead time, and then Switch D is turned ON. The inductor current ramps up and down, respectively, and the energy contained in this current pulse charges up V_{OUT}. After this, unlike the PWM operation, both switches remain OFF, and even Switch A is turned OFF, until V_{OUT} discharges down to the lower threshold of the hysteretic controller. The switching cycle repeats after that.

In most operating conditions, multiple switching pulses are needed to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the V_{OUT} target. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold. In low Iq mode, the lower threshold is 60mV below the V_{OUT} target. As load increases, the frequency of PFM pulses increases as V_{OUT} gets discharged faster and needs to be recharged more often. This continues until the PFM pulses start bunching together, and the part then makes a seamless transition to sustained PWM operation. The converter operates in PFM mode under only one condition: load is light enough in the Normal Mode (Auto PFM/PWM mode).

5.11.3 Operation With V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the RAA23610x rapidly and smoothly switches between Boost, Buck-Boost, and Buck modes to maintain the regulated output voltage. This behavior provides excellent efficiency and low output voltage ripple.

When $V_{IN} = V_{OUT}$, there are two possible cycles that regulate. One is the non-switching one, and the other is buck-boost cycles. The part can stay in one or another or can flip between the two. Under high V_{IN} and high V_{OUT} conditions ($V_{IN} = V_{OUT} > 4V$), there are more disturbances to the inductor current - small changes in the timing of the LX switching converter have a bigger effect on the inductor current. The part has more difficulty finding this non-switching state. When it does find it, it stays there.

5.11.4 Forced Operating Modes

Forced operating modes include Forced PWM mode and Forced Bypass mode. Forced operating modes are selected using the FMODE bits in the CONFIG register. The power-up default mode is Normal operation with automatic mode transitions to optimize efficiency.

Forced PWM mode can be selected to minimize the switching frequency variation and to obtain a tight VOUT accuracy, although this comes at the expense of increased input current. Forced PWM mode is available only in the RAA236100.

Forced Bypass mode can be selected to minimize power losses when output voltage regulation is not required. When the device enters Bypass mode, Switches A, D, and E are turned ON, providing a direct path from the input to output through the inductor. In Bypass mode, all other blocks, except POR and I2C, are turned off to minimize quiescent current consumption. For the DFN package, the Forced Bypass mode can also be selected by asserting the BYPASS pin.

5.11.5 Adaption Scheme for Zero Crossing Detector

The converter employs an adaptive scheme to dynamically adapt the crossing point of the inductor current. The scheme adjusts the offset of the zero cross comparator every 16 switching cycles and corrects variation on V_{IN}, $V_{OUT,}$ temperature, process, and mismatch to try and give a crossing point, which is as close as possible to 0A, optimizing the efficiency and avoiding reverse currents.

6. Serial Interface

The RAA236100 includes a standard I^2C serial interface. The two-wire interface links one or more Masters and uniquely addressable Slave devices. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line, and the serial data (bidirectional) is on the SDA line.

The RAA236100 supports clock rates up to 3.4MHz (High-Speed Mode) and is backward compatible with standard 100kHz (Standard mode) and 400kHz (Fast mode) clock rates.

The SDA and SCL lines must be HIGH when the bus is free (not in use). An external pull-up resistor (typically 1kΩ to 4.7kΩ depending on pull-up voltage and bus capacitance) or current source is required for SDA and SCL.

6.1 I²C General Operation

6.1.1 Data Validity

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is low (except to create a START or STOP condition). The voltage levels used to indicate a logical 0 (LOW) and logical 1 (HIGH) are determined by the V_{IL} and V_{IH} thresholds, respectively; see Electrical Specifications.

6.1.2 START and STOP Condition

All I²C communication begins with a START condition - indicating the beginning of a transaction, and ends with a STOP condition, signaling the end of the transaction.

A START condition is signified by a HIGH to LOW transition on the serial data line (SDA) while the serial clock line (SCL) is HIGH. A STOP condition is signified by a LOW to HIGH transition on the SDA line while SCL is HIGH. See timing specifications in Electrical Specifications.

The Master always initiates START and STOP conditions. After a START condition, the bus is considered busy. After a STOP condition, the bus is considered free. The RAA236100 also supports repeated STARTs, where the bus remains busy for continued transaction(s).

6.1.3 Byte Format

Every byte on SDA must be eight bits in length. After every byte of data sent by the transmitter, there must be an acknowledge bit (from the receiver) to signify that the previous eight bits were transferred successfully. Data is always transferred on SDA with the most significant bit (MSB) first. If the data is larger than eight bits, then it can be separated into multiple 8-bit bytes.

6.1.4 Acknowledge (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The acknowledge bit signifies that the previous eight bits of data were transferred successfully (master-slave or slave-master).

When the Master sends data to the Slave (such as during a WRITE transaction), after the 8th bit of a data byte is transmitted, the Master tri-states the SDA line during the 9th clock. The Slave device acknowledges that it received all eight bits by pulling down the SDA line, generating an ACK bit.

When the Master receives data from the Slave (such as during a data READ transaction), after the 8th bit is transmitted, the Slave tri-states the SDA line during the 9th clock. The Master acknowledges that it received all eight bits by pulling down the SDA line, generating an ACK bit.

6.1.5 Not Acknowledge (NACK)

A Not Acknowledge (NACK) is generated when the receiver does not pull down the SDA line during the acknowledge clock (for example, the SDA line remains HIGH during the 9th clock). This indicates to the Master that it can generate a STOP condition to end the transaction and free the bus.

A NACK can be generated for various reasons, for example:

- After an I²C device address is transmitted, there is NO receiver on the bus with that address to respond.
- The receiver is busy performing an internal operation (such as reset or recall) and cannot respond.
- The Master (acting as a receiver) needs to indicate the end of a transfer with the Slave (acting as a transmitter).

6.1.6 Device Address and R/$\overline{W}$ Bit

After a valid START condition, the first byte sent in a transaction contains the 7-bit Device (Slave) Address plus a direction (R/$\overline{W}$) bit (Device Address Byte). The Device Address identifies which device (of up to 127 addresses on the I^2C bus) the Master wishes to communicate with.

After a START condition, the RAA236100 monitors the first 8 bits received (Device Address byte) and checks for its 7-bit Device Address in the MSBs. If it recognizes the correct Device Address, it ACK and becomes ready for further communication. If it does not see its Device Address, it sits idle until another START condition is issued on the bus.

Note: The eighth bit/LSB of the Device Address byte indicates the direction of transfer, READ or WRITE (R/$\overline{W}$). A 0 indicates a WRITE operation - the Master transmits data to the RAA236100 (receiver). A 1 indicates a Read operation - the Master receives data from the RAA236100 (transmitter).

6.2 RAA236100 Communication Protocol

6.2.1 Device Addresses Byte

The RAA236100 includes a factory, fuse programmable 7-bit I^2C device/slave addresses set to 0x18. The LSB is a direction bit, which can be 0 for WRITE or 1 for READ. This is not part of the unique 7-bit I^2C device address.

6.2.2 Register Size

All the RAA236100 device registers contain 8-bit (byte) data. The data is latched in after the 8th bit (LSB) is received. If a partial data byte is received, that transaction is ignored.

6.2.3 I^2C Write Operation

A Write operation consists of the master sending a START condition, followed by a valid device address byte (R/W bit set to 0), a Register Address Byte, a Data Byte, and a STOP condition. After each byte, the RAA236100 responds with an ACK. The I^2C protocol supports burst writing (automatic incrementing of address pointer). After every successfully transmitted data byte, the device automatically increments the internal register address so subsequent data bytes are written to sequentially incremental register locations. The master must send a STOP condition after sending at least one full data byte and receiving the associated ACK. If a STOP is issued in the middle of a data byte, the write is not performed. The basic write transaction structure is shown below.

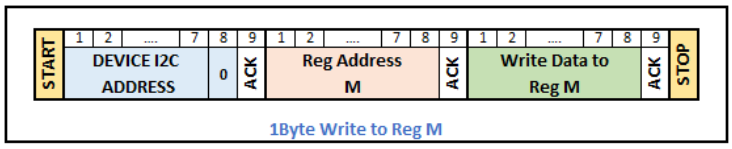


Figure 32. 1-Byte Write to Register M

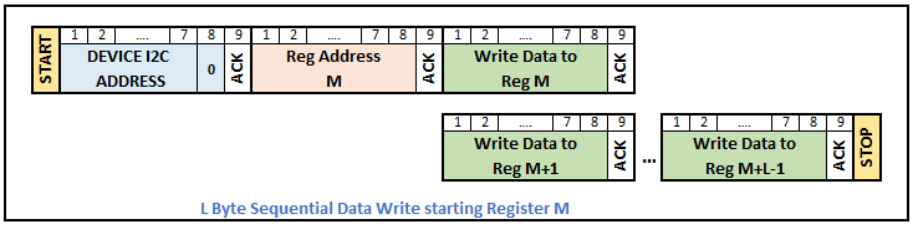


Figure 33. Sequential Data Write Starting at Register M

6.2.4 I²C Read Operation

The master sends a START condition, followed by a valid device address byte (R/W bit set to 0), a register address byte, a second (repeated) START, and a valid device address byte (R/W bit set to 1). After each of the three bytes, the RAA236100 responds with an ACK. The RAA236100 then transmits data bytes back to the master and the master ACKs after each byte. The master terminates the Read operation by issuing a NACK and sending a STOP condition. After every data byte, the RAA236100 auto increments the register address so subsequent data bytes are sent from sequentially incremental register locations.

After every successfully transmitted data byte, the device automatically increments the internal register address so subsequent data bytes are sent out from sequentially incremental register locations.

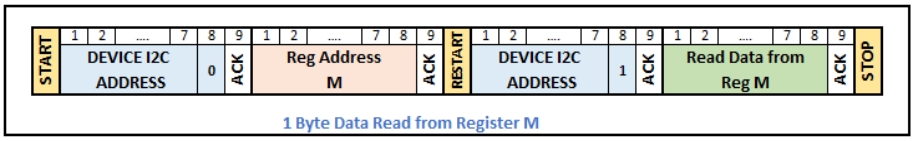


Figure 34. 1-Byte Read to Register M

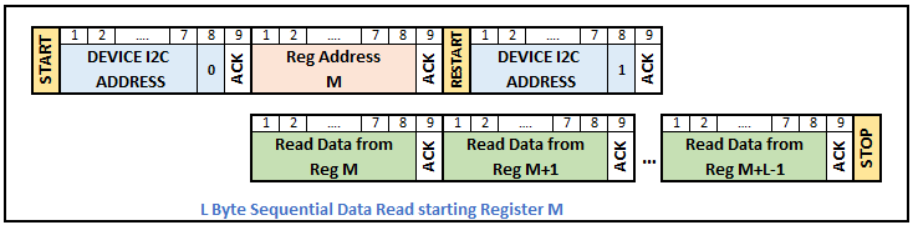


Figure 35. Sequential Data Read Starting at Register M

6.2.5 I²C Timing

The timing specifications of the I²C I/O from the I²C specification are shown in Figure 36 and Table 5. The I²C controller provides a slave I²C transceiver capable of interpreting I²C protocol in Standard, Fast, Fast+, and High-Speed modes.

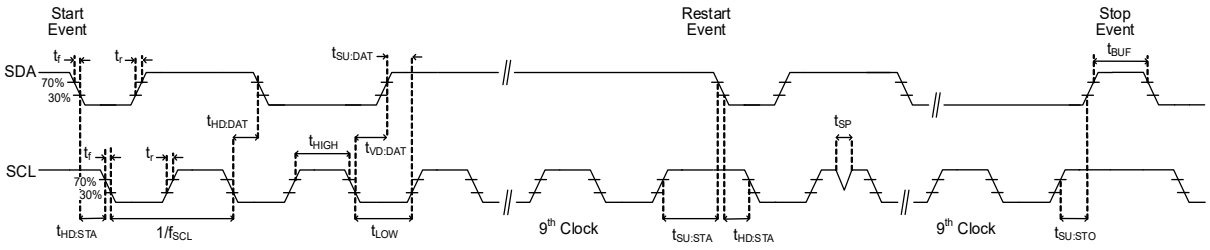


Figure 36. I²C Timing

Table 5. I²C Timing Characteristics

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Frequency	f_{SCL}	0	100	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition (after this period, the first clock pulse is generated)	t_{HD};STA	4000	-	600	-	260	-	160	-	ns

Table 5. I²C Timing Characteristics (Cont.)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LOW Period of the SCL Clock	t_{LOW}	4700	-	1300	-	500	-	160	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	4000	-	600	-	260	-	60	-	ns
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4700	-	600	-	260	-	160	-	ns
Data Hold Time[1]	$t_{HD;DAT}$	15	-	15	-	15	-	15	70	ns
Data Setup Time	$t_{SU;DAT}$	250	-	100	-	50	-	10	-	ns
Rise Time of SCL	t_{rCL}	-	1000	-	300	-	120	-	40	ns
Fall Time of SCL	t_{fCL}	-	300	-	300	20 × (V_{DD}/5.5V)[2]	120	-	40	ns
Rise Time of SDA	t_{rDA}	-	1000	20	300	-	120	10	80	ns
Fall Time of SDA	t_{fDA}	-	300	20 × (V_{DD}/5.5V)	300	20 × (V_{DD}/5.5V)	120	10	80	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4000	-	600	-	260	-	160	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700	-	1300	-	500	-	-	-	ns
Capacitive Load for each Bus Line	C_b	-	400	-	400	-	400	-	100	pF
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	-	-	0	50	0	50	0	10	ns
Input Capacitance for each SDA and SCL	C_i	-	10	-	10	-	10	-	10	pF

1. Measured from the falling edge of SCL, applies to data in transmission and acknowledge
2. V_{DD} = external pull-up voltage

6.3 Unimplemented Registers

All register addresses that are defined in the register map ACK write commands and return data to read commands that address them. Unimplemented register addresses ACK write commands, but data is ignored/disregarded and return a fixed value of (0×00) to read commands.

7. External Component Selection

The RAA23610x works with small physical size components to optimize the PCB area and layout. It also works with low-profile components, making it ideal for applications where thickness is a key factor. Switching MOSFETs are fully integrated, and no additional external MOSFETs or diodes are needed.

7.1 Inductor Selection

Inductors should have sufficient saturation current ratings to keep them from saturating under worst-case operating conditions. They also should have low DCR and core loss to help achieve high efficiency.

Table 6 contains recommended inductors. Other similarly specified components may also be acceptable in the application.

Table 6. Recommended Output Inductors

Manufacturer	Part Number	L× W×H (mm)	Value (µH)	DCR mΩ (typ)	I_{SAT} (typ)
Murata	DFE18SBN1ROME0	1.6x0.8x0.8	1	100	1.9
Murata	DFE18SAN1R0MG0	1.6x0.8x1	1	107	2.1

7.2 Output Capacitor Selection

The amount of output capacitance required is based on the parameters of the maximum load step, the slew rate of the load step, and the maximum allowable voltage regulation tolerance during the transient. The amount of ripple voltage at the output capacitor is also a design constraint; the total peak-to-peak ripple voltages produced from the output capacitor are equal to its ESR multiplied by the worst-case inductor ripple current.

Ceramic capacitors have temperature and voltage (bias) coefficients, which can significantly derate their effective capacitance value. When choosing capacitors, the effective capacitance rating for a given package size, voltage rating, applied temperature, and DC bias must be considered to ensure enough capacitance is used in the design. X7R and X5R type capacitors are recommended.

Table 7 contains recommended output capacitors. Other similarly specified components may also be acceptable in the application.

Table 7. Recommended Output Capacitors

Manufacturer	Part Number	Imperial (Metric) Size	Value (µF)	Voltage Rating (V)
Murata	GRM188R60J106ME47D	0603 (1608)	10	6.3
Murata	GRM188R60J226MEA0D	0603 (1608)	22	6.3
Murata	GRM188R61A226ME15D	0603 (1608)	22	10

7.3 Input Capacitor Selection

Ceramic input capacitors source the AC component of the input current flowing into the high-side MOSFETs. Place them as close to the IC as possible. If long wires are used to bring power to the IC, use additional bulk capacitors between C_{IN} and the battery/power supply to dampen ringing and overshoot at startup.

Table 8 contains recommended input capacitors. Other similarly specified components may also be acceptable in the application.

Table 8. Recommended Input Capacitors

Manufacturer	Part Number	Imperial (Metric) Size	Value (µF)	Volt (V)
Samsung	CL05A10MP5NUNC	0402 (1005)	10	10

Table 8. Recommended Input Capacitors (Cont.)

Manufacturer	Part Number	Imperial (Metric) Size	Value (µF)	Volt (V)
Murata	GRM188R61A106MAAL	0603	10	10
Murata	GRM188R60J106ME47D	0603 (1608)	10	6.3

8. Register Map

Any register addresses (pointers) not indicated in the following section are reserved and should not be used.

REGISTER POINTER	REGISTER BIT(S)	BIT(S)/FUNCTION NAME	DESCRIPTION	SETTING/RANGE	DEFAULT
0x00	Register Name - ENABLE Type - (RW)				0x10 / 16
	[7]	Software reset	The defaults are reloaded by performing an eprom read. The chip will be restarted by initiating a new startup sequence.	0 = Do nothing 1 = Reset IC and reload defaults	<0>
	[6]	EN hold	Do not use		<0>
	[5]	VSEL override	Do not use		<0>
	[4]	Regulators enable		0 = EN pin high enables the bias of the chip but doesn't start regulator 1 = EN pin high enables the bias and initiate the startup sequencing Note: EN pin low always disables the IC and regulator	<1>
	[3]	not used			<0>
	[2:0]	Input CL level	These settings will enforce an average input current limit function for the buck-boost regulator. This is not available in forced PWM (FMODE_bckBst = '10')	000 current limit disabled 001 = 1mA 010 = 2mA 011 = 5mA 100 = 10mA 101 = 20mA 110 = 50 mA 111 = reserved	<000>

0x01	Register Name - CONFIG Type - (RW)				0x4D / 77
	[7:6]	SDAslewRate	This setting adjust SDA falling time depending on which I2C mode we are in (Standard, Fast, Fast plus, High Speed etcetera)	00 = slowest 01 = slow 10 = fast 11 = fastest	<01>
	[5:4]	FMODE bckBst	buck-boost operating modes	00 = normal operation, automatic PFM/PWM transitions and ultra sonic disabled 01 = normal operation, automatic PFM/PWM transitions and ultra sonic enabled 10 = forced PWM mode 11 = forced bypass, disable switching	<00>
	[3]	set VDD I2C to VIN		0 = external VDD_I2C is a fixed 1.8 or 3.3V rail 1 = external VDD_I2C pulled up to VIN	<1>
	[2]	FLL EN bckBst	Enable Frequency control loop (FLL) on buck-boost. When the FLL is enabled the frequency is locked at a 2MHz in PWM and Ton+Toff=1/2MHz in PFM mode	0 = FLL disabled 1 = FLL enabled	<1>
	[1]	not used			<0>
	[0]	EN INT bckBst		Enables integrator in buck-boost error amplifier 0 = Type I error amplifier for best transient response with voltage positioning 1 = Type II error amplifier for best DC accuracy	<1>
0x02	Register Name - ID Type - (Read-Only)				0x30 / 48
	[7:5]	Family ID	This is an identifier to distinguish between Renesas stand alone regulators and PMIC	001 = 2nd gen stand alone converter	<001>
	[4:3]	Chip Rev	This setting indicates the silicon revision	00 = first revision 01 = second revision 10 = third revision 11 = final revision	<10>
	[2:0]	Chip ID	This setting refer to different regulators type; i.e. buck-boost, buck or boost converters	000 = buck boost with Vin_min=1.8V	<000>
0x03	Reserved for Renesas Internal Use				
0x04	Reserved for Renesas Internal Use				
0x05	Reserved for Renesas Internal Use				

0x06	Register Name - bckBst 1 Type - (RW)				0x1E / 30
	[7]	not used			<0>
	[6:0]	bckBst setting 1	VOUT_target when VSEL pin is "HIGH" VOUT_target = 1.8V + N x 50mV where N is bckBst_setting_1 code in decimal	Output voltage examples: 0x00 = 1.8 — 0x10 = 2.6V — 0x1E = 3.3V — 0x40 = 5.0V 0x41 = 5.0V 0x42 = 5.0V — 0x7F = 5.0V	<0011110>
0x07	Register Name - bckBst 0 Type - (RW)				0x1E / 30
	[7]	not used			<0>
	[6:0]	bckBst setting 0	VOUT_target when VSEL pin is "LOW" VOUT_target = 1.8V + N x 50mV where N is bckBst_setting_0 code in decimal	Output voltage examples: 0x00 = 1.8 — 0x10 = 2.6V — 0x1E = 3.3V — 0x40 = 5.0V 0x41 = 5.0V 0x42 = 5.0V — 0x7F = 5.0V	<0011110>

0x08	Register Name - FAULT CONFIG MASTER Type - (RW)				0x1D / 29
	[7]	Master Fault	0->1 transition if any of the latched faults (register 0x09<6:4>) transition from 0->1	0 = no fault 1 = fault	<0>
	[6:5]	not used			<00>
	[4]	EnUvProt	If the under voltage protection is enabled the threshold is fixed at Vout_uv=1.65V. The action of the fault is defined by the content of bits <3:2>: 00 = No Action 01 = Hard shutdown. Requires restart over I2C or EN pin 10 = Hiccup mode (100ms wait) with discharge allowed 11 = Hiccup mode (100ms wait) with discharge inhibited	0 = Under Voltage disabled 1 = Under Voltage enabled	<1>
	[3:2]	bckBst WOC action	bckBst Way Over Current handling mode: No action: the regulator will keep switching using a cycle by cycle current limit Hard shutdown: the regulator will stop switching - it requires a restart using either Software_reset bit, EN pin "HIGH" -> "LOW" -> "HIGH" transition or VIN power cycle Hiccup mode: the regulator will stop switching for 100msec - the regulator will go through a startup sequence again after this time The option to discharge or not discharge is overridden by Discharge_bckBst_enable bitfield	00 = No Action 01 = Hard shutdown 10 = Hiccup mode (100ms wait) with discharge resistor enabled 11 = Hiccup mode (100ms wait) with discharge resistor disabled	<11>
	[1:0]	Over temperature action	Over temperature handling mode Hard shutdown: the regulator will stop switching - it requires a restart using either Software_reset bit, EN pin "HIGH" -> "LOW" -> "HIGH" transition or VIN power cycle The option to discharge or not discharge is overridden by Discharge_bckBst_enable bitfield	00 = Shut down+ start when cooled (discharge resistor enabled) 01 = Shut down+ start when cooled (discharge resistor disabled) 1X = Hard shutdown	<01>

0x09	Register Name - FAULT REPORT Type - (RW)				0x00 / 0
	[7]	not used			<0>
	[6]	bckBst WOC latch	Latched if way over current protection is hit Cleared by writing low. Will set again if fault still present/reoccurs	0 = no fault 1 = latched fault	<0>
	[5]	Over temperature latch	Latched if way over temperature protection is hit Cleared by writing low. Will set again if fault still present/reoccurs	0 = no fault 1 = latched fault	<0>
	[4]	UVLO latch	This bit shows the status of the Vin UVLO comparator. If high Latch high on falling edge of the comparator output (vddOk from "HIGH" to "LOW"). The comparator output is ignored for at least 10us after EN goes high. Cleared by writing low. Will set again if fault still present/reoccurs	0 = no fault (VIN>UVLO) 1 = latched fault (VIN≤UVLO)	<0>
	[3]	bckBst BOOSTING	This bit is only active during switching operation and indicates that Vout is 0.4V above Vin and the regulator will only issue boost cycle, without any buck cycle. The bit is not latched	0 = VOUT≤VIN+0.4 1 = VOUT>VIN+0.4	<0>
	[2]	eprom reading fault	This bit is set if the eprom reading at startup has failed. A new attempt can be made by executing a Software_reset or VIN power cycle	0 = no fault 1 = latched fault	<0>
	[1]	bckBst WOC live	This bit will indicate the 'live' status of the Way Over Current comparator. It is not latched as bit<6> and clears itself if fault condition is removed	0 = no fault 1 = live fault	<0>
	[0]	Over temperature live	This bit will indicate the 'live' status of the over temperature comparator. It is not latched as bit<5> and clears itself if fault condition is removed	0 = no fault 1 = live fault	<0>
0x0A	Reserved for Renesas Internal Use				
0x0B	Reserved for Renesas Internal Use				

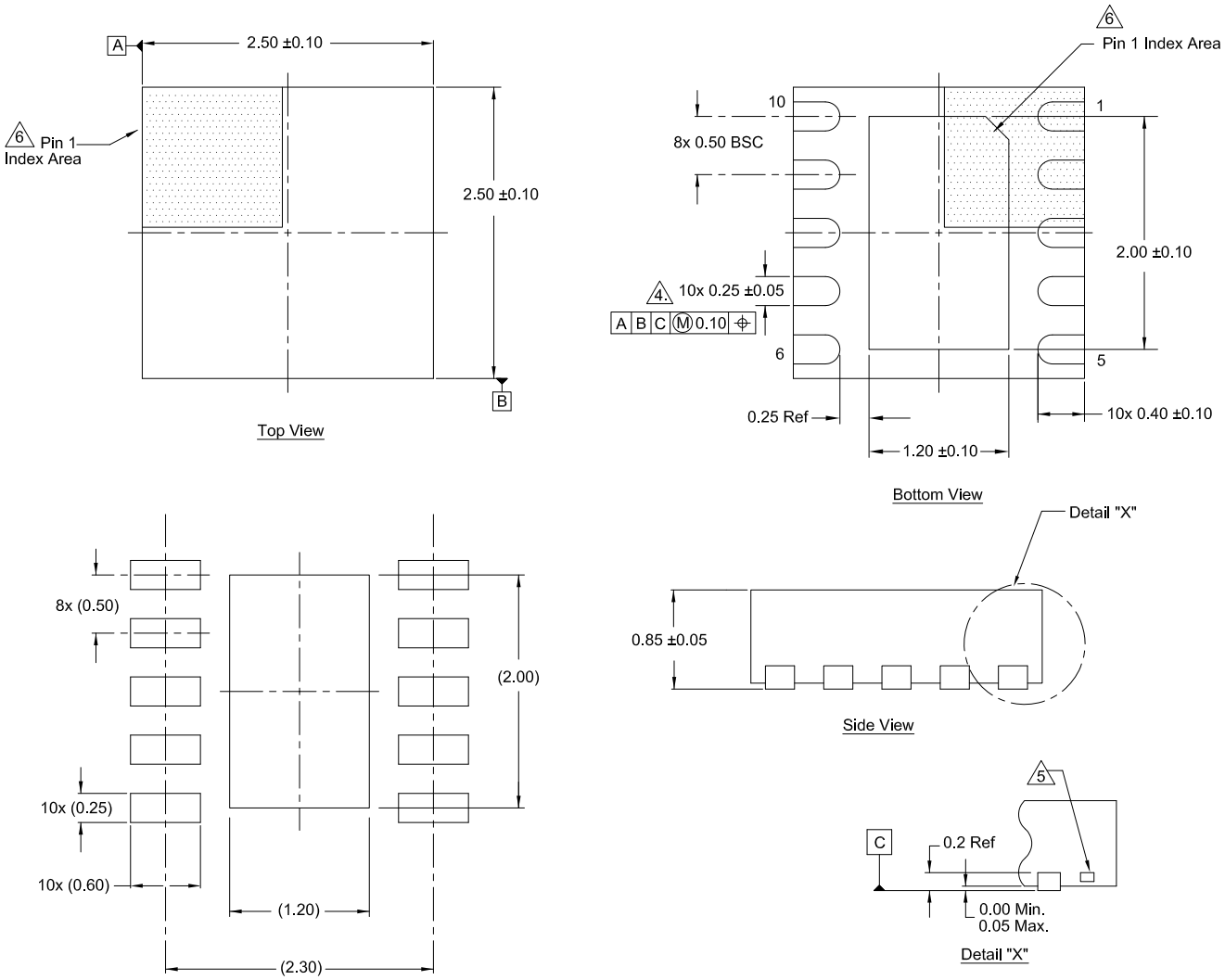
0x0C	Register Name - STARTUP DISCHARGE Type - (RW)				0xA0 / 160
	[7:6]	bckBst slew rate	buck-boost soft start and slew rate between levels	00 = 0.78125mV/us 01 = 1.5625mV/us 10 = 3.125mV/us 11 = 6.25mV/us	<10>
	[5:4]	bckBst fast DVS			<10>
	[3]	bckBst slew mode	This bit, if set, allows a faster ramp down rate if no load is applied. Once Vout reaches the new target the forced in PWM condition will be removed	0 = device stays in normal mode when VOUT is changed downwards 1 = device goes to forced PWM mode during VOUT change downwards	<0>
	[2]	bckBst entry byp mode	This bit will force PWM when entrying bypass until the Vout voltage is close to Vin. Once Vout~Vin the bypass switch will be turned on and the forced PWM mode condition is removed. By setting this bit high the entry in forced bypass mode will be indipendent from the external load. If bit[3] above is set then this bit here is not relevant.	0 = device stays in normal mode when entering bypass and VOUT is going downwards 1 = device goes to forced PWM mode when entering bypass and VOUT is going downwards	<0>
	[1]	not used			<0>
	[0]	Discharge bckBst enable	Discharge resistor is disabled indipendently from this setting when VIN goes below the internal POR level. In case of a WOC or OTP fault This setting overrides reg0x08<3:0> setting	0 = Discharge resistor disabled 1 = Discharge resistor enabled	<0>

9. Package Outline Drawings

For the most recent package outline drawing, see L10.2.5x2.5.

L10.2.5x2.5

10 Lead 2.5x2.5 Dual Flat No-Lead Plastic Package
Rev 0, 11/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier is either a mold or mark feature.

10. Ordering Information

Part Number[1]	Part Marking	Default V_{OUT} (V)	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA2361002GNP#HC5[4]	610	3.3; I^2C programmable	10 Ld DFN 0.5mm pitch	L10.2.5x2.5	Reel, 6k	-40 to +85°C
RAA2361052GNP#HC5[4]	105	1.8 to 4.8 in100mV steps and 5.0V; pin reader	10 Ld DFN 0.5mm pitch	L10.2.5x2.5	Reel, 6k	-40 to +85°C
RTKA236100DE0010BU	Evaluation Board for RAA2361002GNP#HC5					
RTKA236105DE0010BU	Evaluation Board for RAA2361052GNP#HC5					

1. For Moisture Sensitivity Level (MSL), see the RAA236100, RAA236105 product pages. For more information about MSL, see TB363.
2. For the Pb-Free Reflow Profile, see TB493.
3. See TB347 for details about reel specifications.
4. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

11. Revision History

Revision	Date	Description
1.03	Jan 24, 2025	Updated the Forced Bypass mode current consumption on page 1.
1.02	Nov 11, 2024	Updated input quiescent current values on page 1 to match spec values. Corrected mislabeled pin 2 on RAA236105 diagram.
1.01	Jun 25, 2024	Updated Electrical Specifications: - V_{IN} Quiescent Current, Typical, from 100 to 130nA. - Output Voltage Accuracy, from I_{OUT} = 1mA to I_{OUT} = 100µA. - Removed SCL/SDA Input High and Low Voltage High Speed Mode (RAA236100)
1.00	Mar 27, 2024	Initial release

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