

#### RAA271041

Cold Crank Boost and Buck Controller with Drivers for ASIL-D Automotive Applications

## Description

The RAA271041 is a controller for a dual regulator system capable of supporting ASIL-D automotive systems which must operate during battery dropout conditions. The Channel 2 boost regulator maintains the voltage rail which supplies the downstream Channel 1 buck regulator, allowing the buck output to maintain regulation during a battery dropout event such as cold cranking.

For Cold Crank applications, the Channel 2 Boost has an adjustable output and is active when the  $V_{BAT}$  input voltage falls below a user-programmable threshold. The boost channel can also be configured as an independent boost with separate Enable (WAKE2) control.

The boost output from Channel 2 supplies the input for Channel 1 buck. The buck output can be configured either as 3.3V, 5V, or as an adjustable voltage from 0.8V to 12V using a resistor divider.

The RAA271041 requires a typical input voltage of 5.5V at the VIN pin for start-up. The Channel 2 Boost has an input range from 2.2V to 42V while the Channel 1 Buck has an input range from 3.5V to 42V.

The RAA271041 buck channel can operate in Energy Conservation Mode (ECM) to reduce quiescent current draw to 8µA typical when no external load is applied. The buck switching frequency is factory programmable to 440kHz or 2.2MHz. The boost switching frequency is also factory programmable to 440kHz, or 2.2MHz if the buck channel is also set to 2.2MHz. Optional spread spectrum operation is available to reduce EMI and noise levels.

#### **Features**

- ASIL-D Functional Safety
- 42V boost and buck integrated driver controller
- FET drivers support source/sink current of 1A/1A for high-side, and 1A/1.5A for low-side
- Low I<sub>Q</sub> with ECM mode of 8µA typical (buck Channel 1 only)
- Separate or Combined Wake (Enable) inputs for each channel
- Minimized FET ON and OFF times (25ns and 45ns)
- High-efficiency buck exceeding 80% at 10mA
- Buck frequency options 440kHz or 2.2MHz
- Boost frequency options 440kHz or 2.2MHz
   (2.2MHz Boost requires 2.2MHz Buck frequency)
- VBATS sense for boost enable during cold crank
- Optional pseudo-random spread spectrum clocking
- External synchronization using SYNC pin
- Dual Over-temperature protection monitors
- Extensive protection mechanisms for OV/UV/OC/OT
- 6x6mm 36Ld SC-QFN package
- AEC-Q100 grade 1 qualified
- Functional Safety Features
  - · Built-in Self Test (LBIST and ABIST) at power up
  - Recurring Checks: Internal References, PWM clock, System Clock, PGND/AGND connection, Dual Over-Temperature monitor, VCC supply, Logic Pin Stuck Low.
  - Independent References and feedback sense paths for Buck and Boost OV/UV detection
  - Independent Fault Indicators for Buck and Boost
  - Fail-Safe Output, logic high indicates a trusted device state and all safety monitors are active.

## **Applications**

- Automotive battery supplied applications
- In cabin systems
- ADAS: Advanced Driver Assist Systems
- Start-stop protected systems (such as head unit, cluster, e-Mirror)



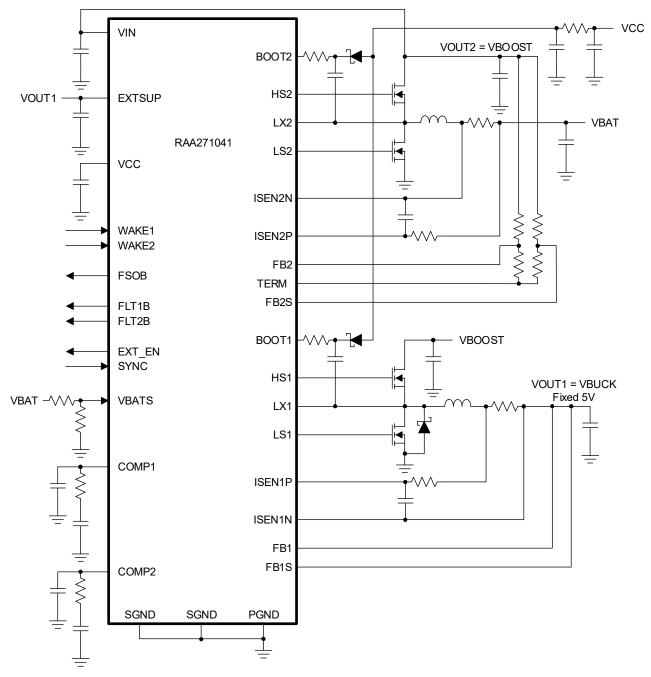


Figure 1. Typical Application Schematic

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# 1. Overview

# 1.1 Typical Application Schematics

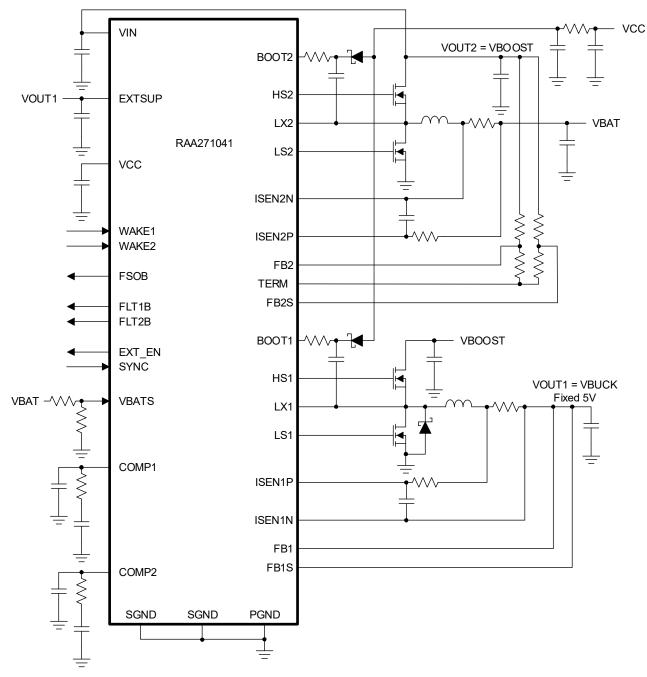


Figure 2. Typical Cold Crank Applications Schematic (VOUT1 Fixed 5V, EXTSUP Connected to VOUT1)

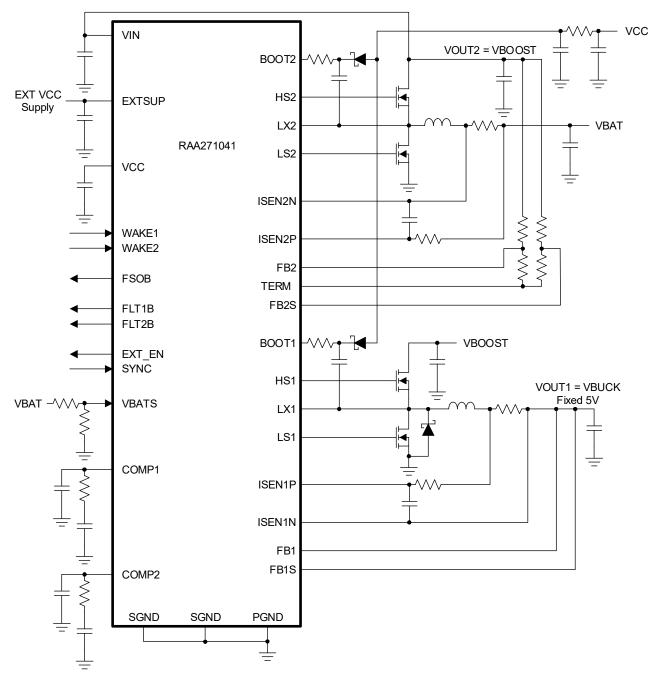


Figure 3. Typical Cold Crank Applications Schematic (VOUT1 Fixed 5V, EXT VCC Supplied)

# 1.2 Block Diagram

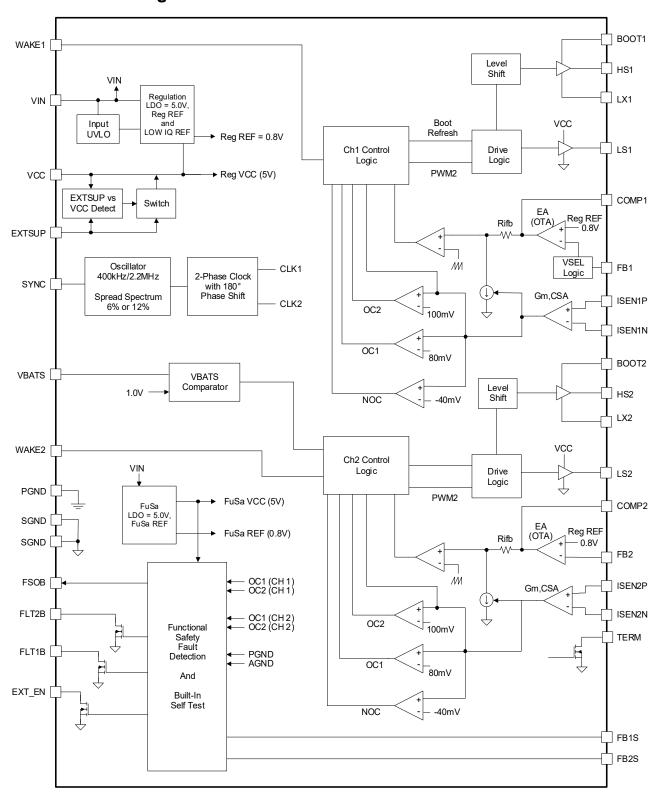


Figure 4. Block Diagram

# 2. Pin Information

# 2.1 Pin Assignments

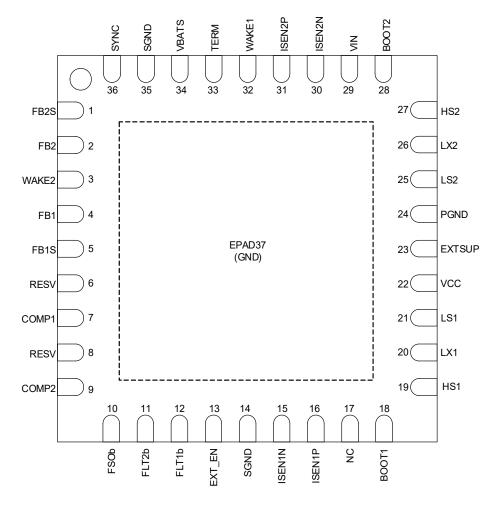


Figure 5. Pin Assignments - Top View

# 2.2 Pin Descriptions

Pin Number	Pin Names	Description		
1	FB2S	OV/UV sense input for Channel 2 boost regulator. Connect to a resistor divider from Channel 2 Boost output to the TERM pin. For ASIL protection, this resistor divider must be a separate copy of the divider used for pin FB2.		
2	Feedback input for Channel 2 adjustable-output boost regulator. Connect to a resistor divider from Channel 2 I output to the TERM pin. FB2 is regulated to 0.8V.			
3	WAKE2	Enable input for both channels for Enable Fuse option 1. Enable input for Channel 2 only for Enable Fuse option 2. Logic high activates the enable.		
4	Feedback input for Channel 1 buck regulator. For fixed output voltages of 5.0V or 3.3V, this pin connects directly the output of Channel 1 buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output ground, and the FB1 voltage is regulated to 0.8V.			
5	FB1S	OV/UV sense input for Channel 1 buck regulator. For fixed output voltages of 5.0V or 3.3V, this pin connects directly to the output of Channel 1 buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output to ground. For ASIL protection, this resistor divider must be a separate copy of the divider used for pin FB1.		
6, 8	RESV	Reserved, connect to SGND.		
7	COMP1	Loop compensation pin for Channel 1 with a resistor/capacitor/capacitor network connected to ground, to provide control loop compensation for Channel 1 buck regulator.		
9	COMP2	Loop compensation pin for Channel 2 with a resistor/capacitor/capacitor network connected to ground, to provide control loop compensation for Channel 2 boost regulator.		
10	FSOb	Fail Safe Output (Indicator). Asserted high indicates the device is not in a Fail State and all safety monitors are active.		
11	FLT2b	Open drain Fault Indicator for Channel 2 (boost). Output low state indicates a Channel 2 fault.		
12	FLT1b	Open drain Fault indicator for Channel 1 (buck). Output low state indicates a Channel 1 fault.		
13	EXT_EN	Open drain indicator for Channel 1. Open state indicates that Channel 1 buck is enabled and is operating in regulation.		
14, 35	SGND	Analog ground, connect to PGND pin in the top copper trace under the IC.		
15	ISEN1N	Negative input to Channel 1 buck output current sense. Connect to the output voltage of Channel 1.		
16	ISEN1P	Positive input to Channel 1 buck output current sense. Connect through an R-C filter to the positive (inductor) side of the Channel 1 output current sense resistor.		
17	NC	Leave this pin unconnected to allow proper node clearance.		
18	BOOT1	Floating supply voltage for Channel 1 high-side MOSFET gate driver. Connect to a 0.1uF ceramic capacitor which connects from BOOT1 to LX1. The capacitor is charged using an external diode connected to VCC through an R-C filter.		
19	HS1	Output of Channel 1 high-side MOSFET gate driver.		
20	LX1	Channel 1 switch node, and return path for the high-side MOSFET gate driver between BOOT1 and LX1.		
21	LS1	Output of Channel 1 low-side MOSFET gate driver; switches between VCC and GND.		
22	VCC	Bias supply (5V typical) for the IC and the MOSFET gate drivers. Decouple with a 10μF ceramic capacitor. This pin is supplied by the internal LDO during start-up. After initial start-up, the bias voltage can be supplied from either the buck 5V output or an external supply, using the automatic switchover feature of the EXTSUP pin.		
23	EXTSUP	Input to the automatic switchover circuit for the VCC bias supply. EXTSUP accepts an external 5V supply derived from either a Channel 1 output of 5V or an independent 5V supply. Do Not apply External bias to EXTSUP until VIN has exceeded initial start-up voltage; however, a voltage such that EXTSUP - VIN ≤ 0.5V can be tolerated.		
24	PGND	Connection point for power ground of the switching circuits for Channel 1 and Channel 2, and is the return path for the low-side MOSFET gate drivers.		
25	LS2	Output of Channel 2 low-side MOSFET gate driver, switches between VCC and GND.		
26	LX2	Channel 2 switch node, also is the return path for the high-side MOSFET gate driver between BOOT2 and LX2.		
27	HS2	Output of Channel 2 high-side MOSFET gate driver.		

## RAA271041 Datasheet

Pin Number	Pin Names	Description
28	BOOT2	Floating supply voltage for Channel 2 high-side MOSFET gate driver. Connect to a 0.1µF ceramic capacitor which connects from BOOT2 to LX2. The capacitor is charged using an external diode connected to VCC through an R-C filter.
29	VIN	For Cold Crank (CC) applications, connect this pin to the output of the Boost Channel 2. For Individual Buck/Boost (IBB) applications, connect this pin to the VBAT power input. This pin is decoupled using a 0.1µF or larger ceramic capacitor.
30	ISEN2N	Negative input to Channel 2 boost input current sense. Connect through an R-C filter to the negative (inductor) side of the Channel 2 input current sense resistor.
31	ISEN2P	Positive input to Channel 2 boost input current sense. Connect to the positive side of the Channel 2 input current sense resistor, typically connected to VBAT which is the DC input voltage.
32	WAKE1	Enable input for Channel 1 buck.
33	TERM	Open drain pull-down for the bottom side of the FB2 and FB2S resistor dividers. This pin becomes open (float) when the boost channel is disabled, to eliminate power loss in the FB2 and FB2S resistor dividers.
34	VBATS	VBAT sense input which sets the boost turn-on threshold for when the battery input falls below normal, such as during Cold Crank. Connect to a resistor divider to set the voltage threshold which enables the boost channel. VBATS threshold is 1.0V. <i>Note</i> : The VBATS turn on/off function for the boost channel is disabled when Individual Buck/Boost operation is selected using factory OTP.
36	SYNC	The SYNC pin selects modes of operation including FCCM (SYNC = logic high), ECM and DCM (SYNC = logic low), and synchronization to an external oscillator in FCCM. Please refer to the SYNC section in applications information for details.
EPAD37	GND	Bottom pad, used for thermal heat dissipation. Connect to PCB GND layers, using multiple vias to conduct heat away from the device.

# 3. Specifications

# 3.1 Absolute Maximum Ratings

**Caution:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter <sup>[1]</sup>	Minimum	Maximum	Unit
VIN, WAKE1, FB2, FB2S, ISEN2N, ISEN2P, TERM, VBATS, LX1, LX2	-0.3	45	V
HS1, HS2, BOOT1, BOOT2	-0.3	51.5	V
WAKE2, COMP1, COMP2, SYNC	-0.3	6.5	V
LS1, LS2, VCC, EXTSUP, FLT1b, FLT2b, FSOb, EXT_EN	-0.3	6.5	V
ISEN1N, ISEN1P, FB1, FB1S	-0.3	42 <sup>[2]</sup>	V
SGND to PGND	-0.3	0.3	V
All Other Pins	-0.3	6.5	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per AEC-Q100-002)	-	2	kV
Charged Device Model (Tested per AEC-Q100-001)	-	750	V
Latch-Up (Tested per AEC-Q100-004)	-	100	mA

Operations above the junction temperature of 150°C and up to a maximum of 170°C can be sustained by the RAA271041 for a limited duration, but with a degradation of the lifetime. Above 170°C, the operation of both FuSa and regulation TSDs (TSD\_FuSa and TSD\_REG) and full device cannot be guaranteed and can also lead to permanent damage.

# 3.2 Recommended Operating Condition

Parameter <sup>[1]</sup> [2]	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+125	°C
Junction Operating Temperature Range	-40	+150	°C
Startup Voltage Range V <sub>IN</sub>	6.0	42	V
Battery Voltage Range V <sub>BAT</sub> (Cold Crank)	2.2	42	V
Buck Channel 1 V <sub>OUT</sub> Fixed options	3.3	5.0	V
Buck Channel 1 V <sub>OUT</sub> Adjustable Range	0.8	12	V
Boost Channel 2 V <sub>OUT</sub> Adjustable Range	5.0	40	V

<sup>1.</sup> The device can handle load dump voltage up to maximum voltage and should not exceed the Absolute Maximum Ratings. 42V continuous input voltage is possible but not recommended.

#### 3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	36-SCQFN part 6.0× 6.0 mm	θ <sub>JA</sub> [1]	Junction to ambient	27	°C/W
Thomas Resistance	00-00Q1 N part 0.0% 0.0 mm	θ <sub>JC</sub> <sup>[2]</sup>	Junction to case	0.9	°C/W

<sup>1.</sup>  $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.



<sup>2.</sup> In case of a high-side FET short, FB1 can tolerate 42V. Long term exposure to voltage exceeding 14V can adversely impact product reliability and result in failures not covered by warranty.

<sup>2.</sup> Higher input voltage can result in higher thermal dissipation within the device. For such applications improved thermal performance might be required. Consult section 3.3 for Thermal Information.

2. For  $\theta_{JC}$ , the case temperature location is the center of the exposed metal pad on the package underside.

# 3.4 Electrical Specifications

 $V_{IN}$  = 12V,  $T_A$  = +25°C. Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ <sup>[2]</sup> )	Max( <sup>[1]</sup> )	Unit
Power Supply				!		Į
V <sub>IN</sub> Undervoltage Lockout Threshold	V <sub>IN,UVLO</sub>	Rising voltage sensed at VIN pin	5.35	5.5	5.65	V
Boost On/Off Threshold (V <sub>IN</sub>	V	Turn-on threshold rising, measured at ISEN2P	2.7	2.8	2.9	V
Monitor, sensed at ISEN2P pin)	V <sub>INL</sub>	Turn-off threshold falling, measured at ISEN2P	2.0	2.1	2.2	V
		VBATS turn-on threshold, falling	0.9	1.0	1.1	V
VBATS Threshold (VBATS Monitor)	V <sub>VBATS</sub>	VBATS turn-off threshold, rising	0.97	1.07	1.17	V
,		VBATS hysteresis	-	70	-	mV
V <sub>IN+EXTSUP</sub> Supply Current in ECM	I <sub>QECM</sub>	ECM mode, no external load on V <sub>OUT</sub> <sup>[3]</sup>	-	8	30	μА
V <sub>IN+EXTSUP</sub> Supply Current		PWM mode, no external load on V <sub>OUT1</sub> , WAKE1 = WAKE2 = HIGH, f <sub>SW</sub> = 440kHz, No Load, Channel 2 off (sum of current into VIN and EXTSUP pins, excluding gate driver currents)	-	15	25	mA
during Normal Switching	I <sub>Q</sub>	PWM mode, no external load on V <sub>OUT</sub> , WAKE1 = WAKE2 = HIGH, f <sub>SW</sub> = 2.2MHz, No Load, Channel 2 off (sum of current into VIN and EXTSUP pins, excluding gate driver currents)	-	20	30	mA
V <sub>IN</sub> Overvoltage Threshold	V <sub>IN,OV</sub>	VIN pin or VBATS pin (per factory programming)	40	43	45	V
V <sub>IN</sub> Supply Current, Shutdown	I <sub>SD</sub>	WAKE1 = WAKE2 = SGND	-	0.5	10	μA
LDO and EXTSUP				•		!
Output Voltage of Internal LDO	V <sub>VCC</sub>	V <sub>IN</sub> = 6.0V to 42V, I <sub>OUT</sub> = 130mA	4.75	5.00	5.25	V
Output Current of Internal LDO	I <sub>VCC</sub>	V <sub>IN</sub> = 6.0 to 42V	-	-	0.13	Α
Dropout Voltage of Internal LDO	D <sub>VCC</sub>	V <sub>IN</sub> = 5.1V, I <sub>LDO</sub> = 130mA	-	0.55	1.2	V
Low (Min) VIN LDO Reset	-	I <sub>LDO</sub> = 130mA and V <sub>CC</sub> drops to VCC UVLO falling threshold	4.75	-	-	V
1000		V <sub>CC</sub> = 4.5V	120	180	250	mA
LDO Current Limit	I <sub>LMTLDO</sub>	V <sub>CC</sub> = 0V	110	300	450	mA
VCC Undervoltage Lockout Threshold	V <sub>VCCUVLO</sub>	Falling	3.85	4.0	4.15	V
External Bias Voltage Range	V <sub>EXTSUP</sub>	For VOUT1 buck = 5V ±5%	4.75	5.00	5.25	V
		Rising	-	4.55	4.7	V
External Bias Voltage Switchover Threshold	VTH <sub>EXTSUP</sub>	Falling	4.2	4.33	-	V
sieveeonoid		Hysteresis	-	0.22	-	V
Oscillator, Spread Spectrum	1			1		1
Internal Switching Range - Low	f <sub>SWIR1</sub>	Range 1	400	440	480	kHz
Internal Switching Range - High	f <sub>SWIR2</sub>	Range 2	2.0	2.2	2.4	MHz
Frequency Tolerance	F <sub>reqTol</sub>	Internal 440kHz or 2.2MHz	-10	-	+10	%

 $V_{IN}$  = 12V,  $T_A$  = +25°C. Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ <sup>[2]</sup> )	Max( <sup>[1]</sup> )	Unit
External Switching Fraguency	f <sub>SWEXR1</sub>	Range 1; applied to SYNC pin	400	-	480	kHz
External Switching Frequency	f <sub>SWEXR2</sub>	Range 2; applied to SYNC pin	2.0	-	2.4	MHz
Spread Spectrum Narrow Mode	F <sub>SSNAR</sub>	Spread Spectrum ON, narrow mode	-	+6	-	%
Spread Spectrum Wide Mode	F <sub>SSWID</sub>	Spread Spectrum ON, wide mode	-	+12	-	%
Controller 1 Specification (Buck	x)		!	•		1
Output Voltage during normal	V <sub>OUT1_3</sub>	Fixed 3.3V selected; SYNC = VCC	-1.5%	3.3	+1.5%	V
operation	V <sub>OUT1_5</sub>	Fixed 5.0V selected; SYNC = VCC	-1.5%	5.0	+1.5%	V
FB1 Pin Voltage Regulation (Adj)	V <sub>FB1</sub>	Adjustable output selected; SYNC = VCC	-1.5%	0.8	+1.5%	V
		V <sub>OUT</sub> = Fixed 3.3V; SYNC = GND	-2%	3.3	+2%	V
V <sub>OUT1</sub> Comparator Threshold at ECM	V <sub>ECMTH1</sub>	V <sub>OUT</sub> = Fixed 5.0V; SYNC = GND	-2%	5.0	+2%	V
		V <sub>FB</sub> = 0.8V (adjustable V <sub>OUT1</sub> ); SYNC = GND	-2%	0.80	+2%	V
FB1/FB1S Pin Leakage Current	I <sub>FBCH1</sub>	-	-	0.2	1.5	μΑ
Forward CH1 Cycle-by-Cycle Current Limit (OC1) Voltage Threshold	I <sub>LMT1CH1+</sub>	VISEN1P - VISEN1N	60	80	100	mV
Forward CH1 Hiccup Current Limit (OC2) Voltage Threshold	I <sub>LMT2CH1+</sub>	VISEN1P - VISEN1N	75	100	125	mV
Negative CH1 Current Limit (NOC) Voltage Threshold	I <sub>LMTCH1</sub> -	V <sub>ISEN1P</sub> - V <sub>ISEN1N</sub>	-55	-40	-25	mV
CH1 Zero Cross	V <sub>ZCD1</sub>	-	-7	0	7	mV
	T <sub>DTLH1S</sub>	Low-side low to high-side high	15	25	45	ns
CH1 Dead Time	T <sub>DTHL1S</sub>	High-side low to low-side high	20	45	70	ns
Citi Dead Time	T <sub>DTLH1L</sub>	Low-side low to high-side high	70	95	120	ns
	T <sub>DTHL1L</sub>	High-side low to low-side high	70	95	120	ns
CH1 Maximum Duty	T <sub>DTMAX1</sub>	-	-	98.5	-	%
CH1 Minimum On-time	T <sub>ONMIN1</sub>	-	10	25	50	ns
CH1 Minimum Off-time	T <sub>OFFMIN1</sub>	-	30	45	60	ns
CH1 Soft-Start Time	T <sub>SSCH1</sub>	FB1 from 0V to regulation point	-	630	-	μs
CH1 Buck Error Amp (OTA) Transconductance	CH1 <sub>Gm,EA</sub>	-	-	1.7	-	mS
		Rising	3.35	3.5	3.65	V
BOOT1 Refresh Threshold	V <sub>B1RFRESH</sub>	Falling	3.25	3.4	3.55	V
		Hysteresis	-	0.1	-	V
CH1 Warning Overvoltage Threshold	OV <sub>THCH1</sub>	Rising Threshold (options = +6%, +8%, +12%)	-2	-	+2	%
CH1 Severe Overvoltage Threshold	SOV <sub>THCH1</sub>	Rising Threshold (options = +12%, +15%)	-2	-	+2	%
CH1 Warning Undervoltage Threshold	UV <sub>THCH1</sub>	Falling Threshold (options = -5%, -8%, -12%)	-2	-	+2	%
CH1 Severe Undervoltage Threshold	SUV <sub>THCH1</sub>	Falling Threshold (options = -12%, -15%)	-2	-	+2	%
		Rising	17	18.5	20	V
CH1 V <sub>IN</sub> ECM Lockout Threshold	VTH <sub>ECMLO</sub>	Falling	16.5	18	19.5	V
		Hysteresis	-	0.5	-	V

 $V_{IN}$  = 12V,  $T_A$  = +25°C. Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ <sup>[2]</sup> )	Max( <sup>[1]</sup> )	Unit
		Rising	5.4	5.55	5.7	V
CH 1 ECM Entry Threshold	VTH <sub>ECMENT</sub>	Falling	5.1	5.25	5.4	V
		Hysteresis	-	0.3	-	V
Controller 2 Specification (Boos	st)		1	1		1
FB2 Pin Voltage Regulation	V <sub>FBCH2</sub>	V <sub>OUT</sub> adjustable	-1.5%	0.8	+1.5%	V
FB2/FB2S Pin Leakage Current	I <sub>FBCH2</sub>	-	-	0.1	0.25	μΑ
Forward CH2 Cycle-by-Cycle Current Limit (OC1) Voltage Threshold	I <sub>LMT1CH2+</sub>	V <sub>ISEN2P</sub> - V <sub>ISEN2N</sub>	60	80	100	mV
Forward CH2 Hiccup Current Limit (OC2) Voltage Threshold	I <sub>LMT2CH2+</sub>	V <sub>ISEN2P</sub> - V <sub>ISEN2N</sub>	75	100	125	mV
Negative CH2 Current Limit (NOC) Voltage Threshold	I <sub>LMTCH2</sub> -	V <sub>ISEN2P</sub> - V <sub>ISEN2N</sub>	-55	-40	-25	mV
CH2 Zero Cross	V <sub>ZCD2</sub>	-	-7	0	7	mV
	T <sub>DTLH2S</sub>	Low-side low to high-side high	10	25	45	ns
CH2 Dead Time	T <sub>DTHL2S</sub>	High-side low to low-side high	20	45	70	ns
CH2 Dead Time	T <sub>DTLH2L</sub>	Low-side low to high-side high	70	95	120	ns
	T <sub>DTHL2L</sub>	High-side low to low-side high	70	95	120	ns
CH2 Maximum Duty	D <sub>MAX2</sub>	-	-	95	-	%
CH2 Minimum On-time	T <sub>ONMIN2</sub>	-	10	25	50	ns
CH2 Minimum Off-time	T <sub>OFFMIN2</sub>	-	25	45	55	ns
CH2 Soft-Start Time	T <sub>SSCH2</sub>	Not applicable to Boost Cold Crank startup. Applies to Independent Buck/Boost mode only.	-	630	-	μs
Boost Error Amp (OTA) Transconductance	CH2 <sub>Gm,EA</sub>	-	-	1.7	-	mS
CH2 Warning Overvoltage Threshold	OV <sub>THCH2</sub>	Rising Threshold (options = +6%, +8%, +12%)	-2	-	+2	%
CH2 Severe Overvoltage Threshold	SOV <sub>THCH2</sub>	Rising Threshold (options = +12%, +15%)	-2	-	+2	%
CH2 Warning Undervoltage Threshold	UV <sub>THCH2</sub>	Falling Threshold (options = -5%, -8%, -12%)	-2	-	+2	%
CH2 Severe Undervoltage Threshold	SUV <sub>THCH2</sub>	Falling Threshold (options = -12%, -15%)	-2	-	+2	%
Output Drivers						
High-Side Drive Source Current	I <sub>HS,SRC</sub>	V <sub>HS</sub> - V <sub>LX</sub> = 2.5V, V <sub>BOOT</sub> - V <sub>LX</sub> = 4.4V	-	1	-	Α
High-Side Drive Source Resistance	R <sub>HS,SRC</sub>	100mA source current, V <sub>BOOT</sub> - V <sub>LX</sub> = 4.4V	-	2	-	Ω
High-Side Drive Sink Current	I <sub>HS,SNK</sub>	V <sub>HS</sub> - V <sub>LX</sub> = 2.5V, V <sub>BOOT</sub> - V <sub>LX</sub> = 4.4V	-	1	-	Α
Hide-Side Drive Sink Resistance	R <sub>HS,SNK</sub>	100mA sink current, V <sub>BOOT</sub> - V <sub>LX</sub> = 4.4V	-	1.5	-	Ω
Low-Side Drive Source Current	I <sub>LS,SRC</sub>	V <sub>LS</sub> - V <sub>PGND</sub> = 2.5V, VCC = 5V	-	1	-	Α
Low-Side Drive Source Resistance	R <sub>LS,SRC</sub>	100mA source current, VCC = 5V	-	2	-	Ω
Low-Side Drive Sink Current	I <sub>LS,SNK</sub>	V <sub>LS</sub> - V <sub>PGND</sub> = 2.5V, V <sub>CC</sub> = 5V	-	1.5	-	Α
Low-Side Drive Sink Resistance	R <sub>LS,SNK</sub>	100mA sink current, V <sub>CC</sub> = 5V	-	1.5	-	Ω

 $V_{IN}$  = 12V,  $T_A$  = +25°C. Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise. (Cont.)

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ <sup>[2]</sup> )	Max( <sup>[1]</sup> )	Unit
Input Pins				I		
WAKE1 Input Low Voltage threshold	VIL <sub>WAKE1</sub>	WAKE1 = CH1 = buck turned OFF; CH2 can be ON/OFF	0.4	0.85	-	V
WAKE1 Input High Voltage threshold	VIH <sub>WAKE1</sub>	WAKE1 = CH1 = buck turned ON; CH2 can be ON/OFF	-	1.25	1.6	٧
WAKE1 Leakage Current	ILK <sub>WAKE1</sub>	WAKE1 = 12V	-0.5	-	0.5	μA
WAKE2 Input Low Voltage threshold	VIL <sub>WAKE2</sub>	WAKE2 = CH2 = Boost turned OFF; CH1 can be ON/OFF	0.4	0.85	-	V
WAKE2 Input High Voltage threshold	VIH <sub>WAKE2</sub>	WAKE2 = CH2 = Boost turned ON; CH1 can be ON/OFF	-	1.25	1.6	V
WAKE2 Leakage Current	ILK <sub>WAKE2</sub>	WAKE2 = VCC	-0.5	-	0.5	μΑ
SYNC Input Low Voltage	VILSYNC	-	-	-	0.3×VCC	V
SYNC Input High Voltage	VIH <sub>SYNC</sub>	-	0.7×VCC	-	-	V
SYNC Pulse Width High	T <sub>SYNCMINH</sub>	-	50	-	-	ns
SYNC Pulse Width Low	T <sub>SYNCMINL</sub>	-	50	-	-	ns
Switching Frequency SYNC Range	f <sub>SYNC</sub>	-	-10	-	10	%
Output Pins						
FLT1b Pin Voltage	VOL <sub>FLT1b</sub>	V <sub>OUTCH1</sub> = OFF; Sink Current = 3mA	-	0.1	0.4	V
FLT2b Pin Voltage	VOL <sub>FLT2b</sub>	V <sub>OUTCH2</sub> = OFF; Sink Current = 3mA	-	0.1	0.4	V
FLT1b Pin Leakage Current	ILK <sub>FLT1b</sub>	V <sub>PULL-UP</sub> = 5V	-	0.01	1	μΑ
FLT2b Pin Leakage Current	ILK <sub>FLT2b</sub>	V <sub>PULL-UP</sub> = 5V	-	0.01	1	μΑ
EXT_EN Pin Voltage	VOL <sub>EXT_EN</sub>	EXT_EN = low; sink Current = 3mA	-	0.1	0.4	V
EXT_EN Pin Leakage Current	ILK <sub>EXT_EN</sub>	V <sub>PULL-UP</sub> = 5V	-	0.01	1	μΑ
FSOb Output High Voltage	FSOb <sub>VH</sub>	With respect to VCC; FSO Source Current = 3mA	-0.6	-0.3	-	V
FSOb Output Low Voltage	FSOb <sub>VL</sub>	FSOb Sink Current = 3mA	-	0.3	0.6	V
TERM Pin Resistance	R <sub>TERM</sub>	-	10	30	70	Ω
TERM Leakage Current	ILK <sub>TERM</sub>	-	-	0.01	1	μΑ
Thermal Shutdown <sup>[4]</sup>	T <sub>OTP</sub>	Rising	151	160	175	°C
Thermal Shutdown LDO	T <sub>TSL</sub>	Rising	160	170	180	°C

<sup>1.</sup> Parameters with MIN and/or MAX limits are 100% tested at +50°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

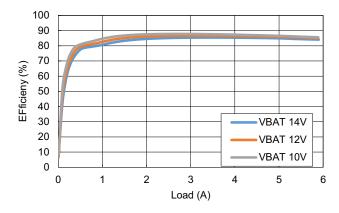
<sup>2.</sup> Typical values are for  $T_A$  = +25°C and  $V_{IN}$  = 12V.

 $<sup>3. \</sup>quad \text{Quiescent current measurements are taken when the output is not switching. (Condition VIN = 12V, VOUT1 = 5V, EXTSUP = VOUT1).}$ 

<sup>4.</sup> MIN and MAX based on Design Spec or Simulations. Not tested on ATE.

# 4. Typical Perfomance Curves

Unless otherwise noted, operating conditions are:  $T_A = +25$ °C,  $V_{IN} = 12$ V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation.



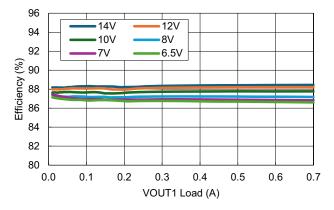
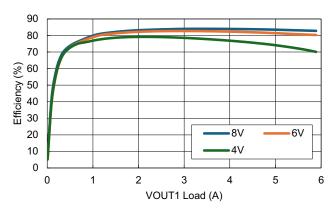


Figure 6. CCM Efficiency (Buck) VOUT1 = 5V, 2.2MHz, EXTSUP = GND

Figure 7. ECM Efficiency (Buck) VOUT1 = 5V, 2.2MHz, EXTSUP = VOUT1



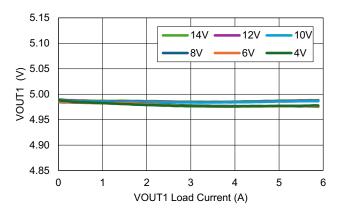


Figure 8. CCM Efficiency (Boost) VOUT2 = 12V, 2.2MHz

Figure 9. CCM VOUT1 Load Regulation, VOUT1 = 5V, 2.2MHz

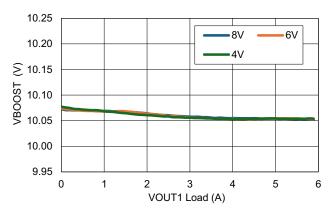


Figure 10. CCM VOUT2 Load Regulation, VOUT2 = 10V, 2.2MHz

Unless otherwise noted, operating conditions are: T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. (Cont.)

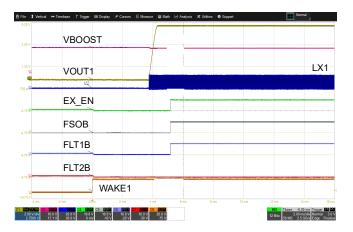


Figure 11. Startup, VBAT = 12V, WAKE1 = VBAT

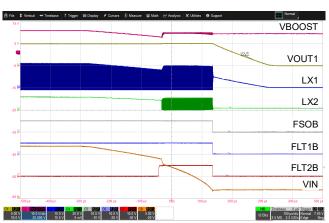


Figure 12. Shutdown using VBAT Ramp Down, VBAT = 12V, WAKE1 = VBAT

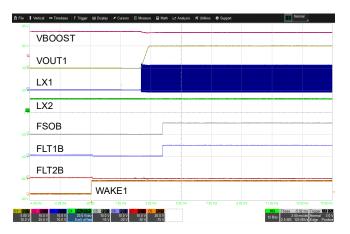


Figure 13. Startup using WAKE1 Toggle, VBAT = 12V



Figure 14. Shutdown using WAKE1 toggle, VBAT = 12V



Figure 15. Startup at 12V with WAKE1 Switched to VIN

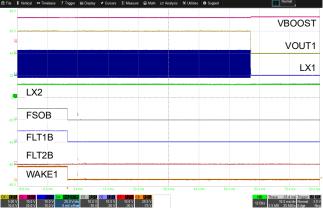


Figure 16. Shutdown at 12V with WAKE1 Switched to GND, No load

Unless otherwise noted, operating conditions are: T<sub>A</sub> = +25°C, V<sub>IN</sub> = 12V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. (Cont.)



## VBOOST

VOUT1

LX1

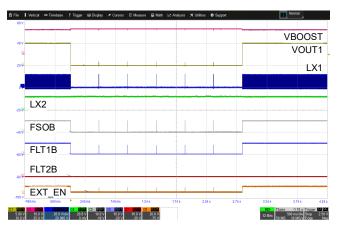
LX1

## FSOB

## FLT2B

Figure 17. BUCK1 Startup with Wake1 Switched High with SYNC Low

Figure 18. BUCK1 Output Shorted with Latch Off





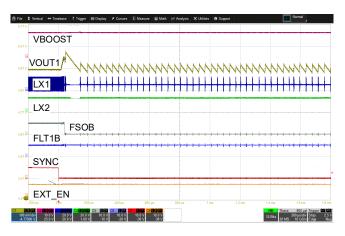


Figure 20. Buck1 ECM Entry with SYNC Driven Low

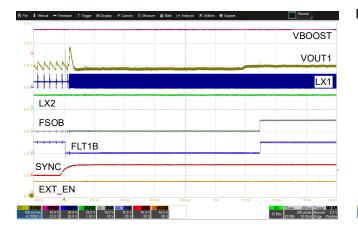


Figure 21. Buck1 ECM Exit with SYNC Driven High

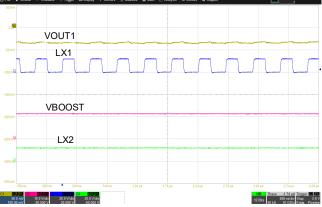


Figure 22. Buck1 FCCM Switching Operation, Buck1 at 75mA Load

# 5. Functional Description

The RAA271041 contains controllers to support two DC/DC channels, Buck and Boost, which are configurable in various modes and operate across a VBAT supply range of 2.2V to 42V. Buck Channel 1 can be configured as a fixed 3.3V, fixed 5.0V, or as an adjustable output voltage from 0.8V to 12.0V.

Boost Channel 2 is an adjustable output with an output voltage range from 5V to 40V. The RAA271041 can be configured such that the Boost output operates as an input for the Buck, often referred to as Cold Crank configuration (CC mode). Alternatively, the RAA271041 can be configured such that the Buck and Boost channels operate independently (IBB mode).

# 5.1 Synchronous Buck and Boost

To improve efficiency, the RAA271041 employs both a synchronous buck and synchronous boost architecture. In the synchronous buck, the LS1 output drives the synchronous low-side MOSFET, which replaces the freewheeling diode and improves efficiency. The HS1 signal provides the buck controller PWM information and is complementary to the LS1 signal. HS1 is powered from a boot supply voltage, which is generated using an external diode from VCC to BOOT1 to charge an external capacitor between BOOT1 and LX1 when LS1 is high and LX1 is low.

In the synchronous boost, the operation of the high-side MOSFET(s) and low-side MOSFET(s) are interchanged. The HS2 output drives the synchronous high-side MOSFET, which acts as the blocking/freewheeling diode to improve efficiency. The LS2 signal is complementary to the HS2 signal and provides boost controller PWM information to the low-side MOSFET(s). The HS2 signal is powered from a boot supply voltage (from BOOT2 to LX2), which is generated using an external diode from VCC to BOOT2 to charge an external capacitor between BOOT2 and LX2 when LS2 is high and LX2 is low.

When the Cold Crank configuration is used, the boost channel powers up only when the VBAT voltage drops below a user-programmable threshold, while under normal conditions the boost is not switching.

# 5.2 Start-Up Operation in Cold Crank Configuration (CC Mode)

For the Cold Crank configuration, the VBAT supply is the input to the Boost channel. Under normal operation, the Boost channel is off, and the Boost output is powered from VBAT using the body diode of the boost high-side MOSFET. If VBAT falls below a user-programmable threshold, the Boost channel turns on and regulates the Boost output to a programmed voltage. In the Cold Crank configuration, the VIN pin of the RAA271041 is connected to the boost output. This arrangement allows the device to be powered from the boost output during Cold Crank events in which the VBAT supply might fall too low to provide sufficient operating voltage. The RAA271041 does not start until the VIN pin exceeds the undervoltage lockout rising threshold of 5.5V typical.

In cold crank applications, Buck Channel 1 is typically enabled first using WAKE1, which might be connected to VBAT or driven by an external signal. This configuration allows the internal LDO regulator to supply  $V_{CC}$  bias, enabling the device to begin switching and proceed through the soft-start sequence. The boost controller does not need to switch for the buck controller to power up.

In the typical cold crank application, the WAKE1 and WAKE2 pins are internally joined (OR'd) using factory programming. Boost Channel 2 is typically off when  $V_{BAT}$  is at the nominal level of 12V. As  $V_{BAT}$  decreases, such as during Cold Cranking, the VBATS pin voltage also decreases. When the VBATS pin falls below 1.0V, the Boost output quickly powers up and maintains the Boost output voltage, which feeds the downstream Buck channel. This allows the Buck output to continue operating, until VBAT drops to the boost turn-off falling threshold of 2.2V. If  $V_{BAT}$  rises such that the VBATS pin exceeds the rising edge threshold of 1.07V, the boost channel turns off and the boost output is supplied from VBAT using the body diode of the boost high-side MOSFET.

The FLT2b pin is in an open-drain state when both the boost channel is on, and the boost output voltage is within the programmed range. The FLT2b pin is in a logic low state when the boost channel is off. The boost channel can be off due to either not enabled by a WAKE input or because the VBATS pin is above 1V.



# 5.3 Start-Up Operation with Individual Buck and Boost (IBB Mode)

For Individual Buck and Boost (IBB) operation, the VIN pin of the device is typically connected to VBAT. The RAA271041 remains off until the VIN pin voltage exceeds the undervoltage lockout rising threshold (5.5V typical). After this condition is met, startup is initiated when either WAKE1 or WAKE2 is set to logic high. This activates the internal VCC regulator which supplies bias power for the device and gate drivers.

Buck Channel 1 operation is controlled by the WAKE1 input. After WAKE1 transitions to logic high, the Buck output goes through a soft-start interval to increase the output voltage to the programmed level. After the buck output reaches regulation, the FLT1b pin remains at logic low for 800µs and then transitions to an open-drain state.

For use in individual boost configuration, the Channel 2 Boost operation is typically controlled by the WAKE2 input only and ignores the VBATS pin. Before the boost is enabled, the output  $V_{BOOST}$  is charged to a voltage one diode drop below  $V_{IN}$  through the body diode of the high-side MOSFET. After being enabled, the boost channel goes through an initial soft-start interval and ramps the boost output voltage to the programmed level. After the boost output reaches regulation, the FLT2b pin remains at logic low for  $800\mu s$  and then transitions to an open-drain state.

## 5.4 WAKE1 and WAKE2 Operation

The WAKE1 pin can withstand up to 42V and can connect to VBAT through a resistor for initial start-up.

The WAKE2 pin is a low voltage (5V) pin and should not be connected to VIN or VBAT. WAKE2 can be enabled using a pull-up resistor to VCC after WAKE1 is high, or connected to an external signal, which does not exceed 5V. For simultaneous start-up of Buck and Boost, the enable pins (WAKE1 and WAKE2) can be resistively pulled to respective logic levels when VBAT is applied.

If the WAKE pins are OR'd with either WAKE pin high, the IC continues operation until the VCC voltage decreases below the VCC UVLO falling threshold (4.2V typical), or when VBAT falls below 2.2V.

# 5.5 VCC Regulator and EXTSUP

The VCC regulator (internal LDO) derives power from the VIN pin and provides VCC 5V bias during startup, which can also be used in continuous operation. In this state, VCC provides bias power for both the IC supply and gate drivers, which can produce high power dissipation in the VCC regulator. To minimize IC dissipation and increase system efficiency, in some applications the EXTSUP pin can supply 5V from an external voltage source. The IC monitors the EXTSUP voltage; if the EXTSUP voltage exceeds 4.5V, the IC connects the EXTSUP pin to the VCC pin and turns off the VCC regulator. This reduces IC power loss and system power loss. If the EXTSUP feature is not used, ground the EXTSUP pin and the VCC regulator powers the IC.

In some applications with VOUT1 set to 5V, VOUT1 can be connected to the EXTSUP pin so that after startup, VOUT1 can supply VCC bias power and eliminate the LDO dissipation in normal operation.

There might be applications where EXTSUP is not used. When the RAA271041 is used in an ASIL system, consult the Safety Application Note (SAN) for application information. During restarts, the internal EXTSUP switch is turned OFF, and this power handover between LDO to EXTSUP pin takes place during each power up. If Channel 1 is not set to 5V, the EXTSUP input can accept 5V from an independent source, such as a small 3.3V to 5V boost converter. If the external bias is applied before VIN is applied, power the enable circuit from the external bias source (and not VIN).

#### 5.6 Oscillator

The buck switching frequency is factory-programmable with options for 440kHz and 2.2MHz. The boost switching frequency is also factory-programmable for either 440kHz or 2.2MHz, however, the boost frequency cannot exceed the Channel 1 buck frequency. External synchronization can be implemented by connecting an external signal source of 440kHz or 2.2MHz (±10%) to the SYNC pin.



# 5.7 Phase Shift and Spread Spectrum

The switching of buck and boost channels are 180° out of phase, which helps lower overall noise by reducing peak currents during switching. The 180° phase shift is between the buck high-side MOSFET on-time and the boost low-side MOSFET on-time.

The Spread Spectrum is derived from an internal triangular 3kHz wave oscillator with a modulation depth of 6% or 12% in a pseudo-random manner. Spread spectrum is configured by factory OTP, which selects spread spectrum ON/OFF and modulation depth, with 5-bit resolution to create 32 discrete frequencies.

## 5.8 FLTb Signals

The Fault Indicators FLT1b and FLT2b are provided for fault monitoring on the respective buck and boost channels. The pins provide an open-drain output to indicate that the soft-start cycle has completed, and the output voltage is within regulation. An external pull-up resistor is required for each pin, pulled up to VCC or to an external DC supply (5.5V maximum). These pins are pulled low during startup or when the respective output is off.

## 5.9 EXT EN Signal

The EXT\_EN output is an open-drain indicator that can enable external devices or circuits. The EXT\_EN pin can be factory-programmed to monitor Channel 1 only, or Channel 2 only, or both channels. A high (open) state indicates that the selected channel(s) is enabled and is not shut down. During power-up, the EXT\_EN pin is low until soft-start is completed and the selected channel(s) are operating in regulation.

## 5.10 Fail-Safe Output (FSOb)

The FSOb indicator is a fail-safe (push-pull) output that is in the high state when the device is in a trusted state. FSOb transitions to low when a severe fault is detected or when ECM is entered.

*Note*: When FSOb is high (normal operation), the pin is internally connected to the VCC supply, typically 5V. Logic devices which connect to FSOb should be able to tolerate 5V signals.

#### 5.11 Fault Protection Overview

The RAA271041 provides multiple fault detection features, including:

- Warning Undervoltage and Overvoltage detection for channels 1 and 2.
- Severe Undervoltage/Overvoltage detection and shutdown for channels 1 and 2.
- Separate internal voltage references for UV/OV detection versus output regulation for channels 1 and 2.
- Separate feedback paths for UV/OV detection versus output regulation for channels 1 and 2.
- FLT1b and FLT2b outputs for indicating faults on channels 1 and 2, respectively.
- Separate internal regulator to provide bias power for functional safety references, circuits, and logic.
- Monitor that compares the output regulation reference to the separate UV/OV reference.
- Redundant logic state machines with separate input skewing to prevent spurious noise corruption.
- Built-In Self Test (BIST) at startup and at ECM exit:
  - · UV/OV comparators test
  - Fault Indication stuck-high test (FLT1b, FLT2b, EXT\_EN)
  - · VCC LDO over-temperature monitor
  - FuSa internal LDO supply over-temperature monitor
  - PGND/SGND connection monitor
  - · System and PWM clock monitors
  - · VCC UV/OV monitors
  - State machine comparison monitor
  - · CRC check on internal registers after initialization
- In addition to BIST at startup, the device provides continual functional safety checking for the following:



- · CRC check of internal registers
- State machine comparison

When the device is placed in ECM, all non-essential circuits are powered off and alternate ultra-low power circuits are activated. During this time, the device is less accurate at detecting faults and as such is not in a trusted state, and the Fail-Safe Output (FSOb) is low. When the device exits ECM by setting the SYNC input to high, the device immediately begins BIST and rechecks protective functions. After the device has successfully completed BIST, protective functions are re-enabled, the controller exits ECM operation, and the FSOb output transitions to high.

#### 5.12 Pin Fault Detection

The device can detect a stuck-high condition on each of the four logic indicators: FSOb, FLT1b, FLT2b, and EXT\_EN. A stuck-high fault is a condition in which the device expects a logic low level on the signal pin but detects a logic high level, indicating a fault related to the pin or the external pull-up circuitry.

When a stuck-high pin fault is detected, there is a 500µs delay on fault response. If the pin fault persists longer than 500µs, the device immediately shuts off both Channel 1 Buck and Channel 2 Boost. The outputs then either enter a hiccup/restart cycle or latch off, depending on factory programming.

# 5.13 Output Voltage Selection

The Channel 1 buck stage operates with an input voltage range of 3.75V to 42V and is offered in fixed output voltage options of 5.0V, 3.3V, or adjustable. In adjustable mode, the Buck output can be set in the range  $V_{OUT1} = 0.8V$  to 12V using an external resistive voltage divider from VOUT1 to SGND, with the midpoint connected to FB1.

*Note*: An identical resistive divider must be used with the midpoint connected to FB1S (OV/UV sense input), to provide robust OV/UV detection if the feedback path to FB1 is interrupted.

Use Equation 1 to derive the  $R_{UPPER1}$  and  $R_{LOWER1}$  resistor values, where  $R_{UPPER1}$  is the resistor between VOUT1 and FB1, and  $R_{LOWER1}$  is the resistor between FB1 and GND.

(EQ. 1) 
$$V_{OUT1} = 0.8V \times (1 + (R_{UPPER1})/(R_{LOWER1}))$$

The VOUT threshold accuracy is  $\pm 1.5\%$  in normal mode and is  $\pm 2\%$  in the Energy Conservation Mode (ECM). Error amplifier compensation is achieved by connecting a Type 2 compensation network to COMP1.

## 5.14 Bootstrap for High-side NMOS Drive

To provide high-side gate voltage, the RAA271041 employs a bootstrap circuit using an external boot capacitor  $(C_{BOOT1})$  and external diode. The capacitor charges from the VCC supply when the buck low-side MOSFET is on.

#### 5.14.1 Boot Refresh for Buck Channel in ECM

If the Buck channel is in Pulse Skip mode or in ECM mode, the long time between LX1 pulses can result in the BOOT1 voltage falling. The BOOT1 to LX1 voltage is constantly monitored and if it falls lower than 3.4V (typical), the device inserts a 180ns (or optional 360ns) pulse to the Buck low-side gate, which recharges the BOOT1 capacitor.

#### 5.14.2 Current Limit and Overcurrent Protection

For Buck Channel 1, an external current sense resistor and internal current sense amplifier provide overcurrent protection. The current sense resistor is in series with the inductor, with a resistance value selected to provide 50mV at full load. Inductor DCR current sensing, which uses a small RC filter to sense the inductor current signal can also be used. If the load increases such that the voltage across the current sense resistor rises to 80mV (OC1 threshold), the PWM controller terminates the high-side pulse, on a cycle-by-cycle basis. If the load continues to increase and the current sense resistor signal reaches 100mV (OC2 threshold), the OC2 protection limit is



reached; switching operation ceases and the output is shut down and either enters a hiccup/restart cycle or latches off.

#### 5.14.3 Undervoltage and Overvoltage (UV and OV) Protection

The RAA271041 channels 1 and 2 have factory-programmable options for the following:

- Warning overvoltage at +6%, +8%, and +12%,
- Warning undervoltage options of -5%, -8%, and -12%.
- Severe overvoltage at +12% and +15%
- Severe undervoltage at -12% and -15%.
- Channel 1 and Channel 2 provide separate selections for Warning UV, Warning OV, Severe UV, and Severe OV.

A Warning UV or OV detection causes the corresponding FLT1b or FLT2b indicator to pull low. However, the output continues switching. If the output voltage returns to normal, the FLT1b or FLT2b pin also returns to its high (open drain) state.

A Severe UV or OV detection causes the output to shut down, and the corresponding FLT1b or FLT2b pin also drives low (if not already low due to Warning UV or OV).

Note: All UV and OV conditions are detected at the FB1S and FB2S pins, not the FB1 or FB2 pins, which are used to regulate the outputs. The separate paths for OV/UV detection versus feedback regulation protect against single-point failures in the output feedback path.

## 5.14.4 Boost Input Overvoltage (VBAT OV)

The RAA271041 detects overvoltage at the VBAT input. When the VBAT voltage reaches 44V, the device detects an input OV condition and immediately shuts down both channels. *Note*: The input OV condition is sensed at the VIN pin for Cold Crank options (see Device Response versus Boost Operating Option). For Individual Buck/Boost applications, (Device Response versus Boost Operating Option) the input OV condition is sensed at the VBATS pin.

#### 5.15 Boost Channel 2

#### 5.15.1 Boost Operating Range

The synchronous boost stage operates across a  $V_{BAT}$  input voltage range of 2.2V to 42V and has an adjustable  $V_{BOOST}$  output voltage range of 5V to 40V. The  $V_{BOOST}$  output voltage is set using two resistor dividers: one divider connects to the FB2 pin, and a second identical divider connects to the FB2S pin. For most applications, the purpose of the boost channel is to maintain an input supply for the Buck channel during low-battery events such as cold cranking, allowing the Buck channel to continue normal operation.

#### 5.15.2 Boost Operation Options

The boost channel is factory-programmed to operate in one of four options:

- Option 0 (Cold Crank 0) This option is for applications where the boost channel runs directly from the battery
  input, and the buck channel runs directly from the boost output. The boost output powers the buck input but
  does not power any other external loads.
  - Under normal VBAT conditions, the boost channel is off and the VBAT voltage passes directly to the boost output through the body diode of the boost high-side MOSFET. When the VBAT input decreases to a user-programmable threshold, set by the VBATS pin threshold of 1.0V, the boost channel quickly powers up and brings the boost output up to the programmed voltage. The boost channel remains on until the VBATS pin voltage rises above the VBATS rising threshold of 1.07V, at which point the boost channel turns off.

*Note*: The boost output voltage might be below the programmed voltage setting, caused by VBAT being below normal levels but not low enough to reach the VBATS falling threshold. In this condition, the boost channel is still off, and the boost output decreases as the VBAT input decreases.



In this operation option, the boost output undervoltage and overvoltage fault detections are disabled. Undervoltage detection is disabled because the boost output might be lower than normal while the VBAT input is below the user-programmed boost output voltage yet is not low enough to turn on the boost channel using the VBATS pin. Overvoltage detection is also disabled because the VBAT input might be much higher than normal during a Load Dump event, which can force the  $V_{BOOST}$  output voltage far above the user-programmed boost output voltage.

- Option 1 (Cold Crank 1) This option is like Cold Crank 0, however in this case, the boost output feeds both the buck channel input and an external load. The overall operation is the same as Cold Crank 0.
- Option 2 (Individual Buck/Boost 0) This option allows for separate operation of the Boost and Buck channels. In this mode, the Boost channel operates as controlled by the WAKE2 pin (or using OR'd WAKE pins) and ignores the VBATS pin. This mode is intended for applications in which the Boost channel must also tolerate Load Dump (high VBAT) events. During a Load Dump event it is possible for the Boost output voltage to exceed the normal regulation voltage, therefore the OV fault detection is disabled. However, the UV fault detection and response is enabled and is active whenever the Boost is on (using WAKE input).
- Option 3 (Individual Buck/Boost 1) This option allows for the separate operation of the Boost and Buck channels when powered from regulated power input. In this mode, the Boost channel operates as controlled by the WAKE2 pin (or using OR'd WAKE pins) and ignores the VBATS pin. This mode is intended for applications in which the Boost channel does not need to tolerate Load Dump (high VBAT) events, and therefore the Boost channel has enabled fault detection and response for Warning UV/OV and for Severe UV/OV conditions.

The system architecture assumptions for each Boost operating option are listed in Table 1.

**Table 1. System Architecture Assumptions** 

Option	Name	System Architecture
0	Cold Crank 0 CC_0	The Boost channel is active (switching) only when VBAT drops during Cold Crank, to ensure that Buck operation continues.  System requires tolerance of Load Dump and Cold Crank.  Boost OV faults are ignored due to possible Load Dump event causing V <sub>BOOST</sub> to exceed normal levels.  Boost UV faults are ignored due to possible low VBAT causing V <sub>BOOST</sub> to fall below normal levels. If VBAT falls low enough to force the VBATS pin to 1V, the boost turns on and supports the Buck input.  VBAT feeds the boost input. The boost output powers only the buck input, no other loads on boost.
1	Cold Crank 1 CC_1	The Boost channel is active (switching) only when VBAT drops during Cold Crank, to ensure that Buck operation continues.  System requires tolerance of Load Dump and Cold Crank.  Boost OV faults are ignored due to possible Load Dump event causing V <sub>BOOST</sub> to exceed normal levels.  Boost UV faults are ignored due to possible low VBAT causing V <sub>BOOST</sub> to fall below normal levels. If VBAT falls low enough to force the VBATS pin to 1V, the boost turns on and supports the Buck input.  VBAT feeds the boost input. The boost output powers the buck input and/or other external loads.
2	Individual Buck/Boost 0 IBB_0	System might require that the boost channel is always on.  System requires tolerance of Load Dump and Cold Crank.  Boost OV faults are ignored due to possible Load Dump event causing V <sub>BOOST</sub> to exceed normal levels.  Boost UV fault response is enabled when the boost is active.  VBAT feeds the boost input. The buck channel can be powered from the boost output, or from VBAT, or from a separate input supply.
3	Individual Buck/Boost 1 IBB_1	System might require that the boost channel is always on.  System does not require tolerance of Load Dump and Cold Crank (VBAT supply is pre-regulated).  Boost OV fault response is enabled when the boost is active.  Boost UV fault response is enabled when the boost is active.  VBAT feeds the boost input. The buck channel can be powered from the boost output, or from VBAT, or from a separate input supply.

The device response for each of the operating options is shown in Table 2.

Table 2. Device Response versus Boost Operating Option

Option Number	Option Name	Cold Crank Tolerant	Load Dump Tolerant	Boost Enable	Boost Output OV Faults	Boost Output UV Faults	Boost Input OV Fault (VBAT OV)
0	Cold Crank 0 CC_0	Yes	Yes	Wake = High and VBATS ≤ 1V	No response	No response	Response enabled sensed at VIN pin
1	Cold Crank 1 CC_1	Yes	Yes	Wake = High and VBATS ≤ 1V	No response	No response	Response enabled sensed at VIN pin
2	Individual Buck/Boost 0 IBB_0	Yes	Yes	Wake = High VBATS ignored	No response	Response enabled when boost is active	Response enabled sensed at VBATS pin
3	Individual Buck/Boost 1 IBB_1	Yes	No	Wake = High VBATS ignored	Response enabled when boost is active	Response enabled when boost is active	Response enabled sensed at VBATS pin

#### 5.15.3 Boost Output Voltage Programming

To program the Boost output voltage, connect a resistor divider from  $V_{BOOST}$  to the TERM pin, with the midpoint connected to the FB2 pin. Use Equation 2 to calculate the required resistor values, where  $R_1$  is the resistor between VOUT2 and FB2, and  $R_2$  is the resistor between FB2 and TERM.

(EQ. 2) 
$$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right)$$

*Note*: Place an identical resistor divider from V<sub>BOOST</sub> to the TERM pin, with the midpoint connected to the FB2s pin.

When designing the PCB, include a GND guard band around the feedback resistor networks to reduce noise and improve accuracy and stability. Place resistors  $R_1$  and  $R_2$  close to the FB pin.

#### 5.15.4 Current Limit and Overcurrent Protection (OC1 and OC2)

For the Boost channel, an external current sense resistor provides overcurrent protection. The current sense resistor is in series with the  $V_{BAT}$  input, with a resistance value that produces a 50mV signal between ISEN2P and ISEN2N when the full load current is applied to the output in CCM. Inductor DCR current sensing, which uses a small RC filter to sense the inductor current signal can also be used. If the load increases such that the voltage across the current sense resistor reaches 80mV, the PWM circuit begins limiting current on a cycle-by-cycle basis (OC1). If the load continues to increase and the current sense resistor signal reaches 100mV, the OC2 protection limit is reached and the output shuts down, and then enters a hiccup/restart cycle or latches off, based on factory programming.

*Note*: If the boost output falls below VBAT, current is free to flow from VBAT to the boost output through the high-side MOSFET body diode, even if the MOSFETs are not switching.

Also, the current sensing is done at the boost input. The input current of a boost channel is inversely proportional to the input voltage. When selecting the sense resistor value, the lowest expected operating input voltage ( $V_{BAT}$ ) gives the highest expected input current and use this value to select the resistor value.

The RAA271041 boost Channel 2 also has reverse (negative) current limiting at -40mV typical.



## 5.15.5 Boost Turn-On Threshold in Cold Crank (VBATS Threshold)

For Cold Crank applications, the Boost channel is typically not switching until the VBAT input decreases (such as during a Cold Crank event), at which point the Boost channel turns on to provide a regulated input to the downstream Buck channel. The RAA271041 provides a VBATS pin (Pin 34) which allows the user to program the VBAT voltage at which the Boost channel turns on. To program the VBAT voltage which enables the Boost channel, connect a voltage divider from VBAT to the TERM pin (Pin 33), with the midpoint connected to VBATS (pin 34). When the VBATS pin falls below 1.0V, the boost turns on and brings the VBOOST output voltage to the programmed voltage, allowing the Buck channel to continue operation.

To prevent the VBATS input from triggering on switching noise, Renesas recommends placing a 220pF capacitor connected from VBATS to GND.

#### 5.15.6 Over-Temperature Shutdown

The RAA271041 has an over-temperature shutdown threshold of 160°C with 15°C hysteresis. When crossing the threshold, the device shuts down for 100ms and then attempts to restart the device. The device resumes operation when the over-temperature fault is cleared.

# 5.16 Customer Options Table of Selections in OTP Creator

There are many potential options available in the RAA271041 which can be specified using the OTP Creator. Contact a Renesas Representative for assistance in creating a custom OTP configuration.

Table 3. Customer Options	
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Configuration	Selections		
Channel 1 output voltage selection	5V fixed (default) 3.3V fixed adjustable		
Wake pin control for regulators	Either WAKE1 or WAKE2 high enables both regulators. (default) WAKE1 and WAKE2 act as individual regulator enables.		
PWM frequency for CCM mode operation	2.2MHz (default) 440kHz		
Channel 2 frequency relative to Channel 1 frequency	1x CH1 0.2x CH1		
Buck/Boost mode selection	Cold Crank 0 Cold Crank 1 Individual Buck/Boost 0 Individual Buck/Boost 1		
Boot refresh control	180ns (default) 360ns		
Spread spectrum pause control	Use random pause periods. (default) Use fixed pause periods.		
Spread spectrum pause algorithm	Min repeating length (default) Intermediate repeating length Max repeating length		
Spread spectrum	Spread spectrum disabled (default) Spread spectrum enabled at 12% modulation Spread spectrum enabled at 6% modulation		
Delay from WAKE input falling to regulator 2 end of switching	64ms (default) 48ms 32ms 0ms		

# Table 3. Customer Options (Cont.)

Configuration	Selections
Delay from WAKE input rising to regulator 2 start of switching	0ms (default) 32ms 48ms 64ms
Delay from WAKE input falling to regulator 1 end of switching	64ms (default) 48ms 32ms 0ms
Delay from WAKE input rising to regulator 1 start of switching	0ms (default) 32ms 48ms 64ms
OV warn fault thresholds	6% (default) 8% 12%
UV warn fault thresholds	-5% (default) -8% -12%
OV severe fault thresholds	12% (default) 15%
UV1 severe fault thresholds	-12% (default) -15% Fixed 2.8V if in fixed 3.3/5V Vout1 mode, -15% if in adjustable Vout1 mode
UV2 severe fault thresholds	-12% (default) -15%
Soft-start typical transition rate	600μs (default) 1200μs
Select which regulator(s) are safety related and affect FSOb	Only regulator 1 is safety related. (default) Both regulators are safety related. Only regulator 2 is safety related. Neither regulator is safety related. FSOb set high after FuSa boot up.
Controls if WAKE signal can cancel an ongoing opt_reg_fault_to_off_dly timing if WAKE returns low during the programmed delay period.	WAKE going low cancels an on-going opt_reg_fault_to_off period. Regulation enters either the latchoff of hiccup immediately as programmed by opt_hicn_lat. (default) WAKE going low is ignored during the opt_reg_fault_to_off period. Entire programmed period is executed, then regulation enters either latchoff or hiccup as programmed by opt_hicn_lat.
Delay from FSOb low assertion to regulator shutdown due to over/under voltage faults (only when programmed to be faults with shutdown)	Oms (default) 32ms 48ms 64ms

# Table 3. Customer Options (Cont.)

Configuration	Selections
Controls if WAKE signal can cancel opt_toffx_dly timing if WAKE returns high during the programmed delay period.	WAKE returning high is ignored during the toffx_dly period. Entire programmed toff_dly period is executed, then WAKE is re-evaluated. WAKE returning high cancels an on-going toff_dly period. Regulator continues switching if WAKE goes high prior to end of the toff_dly period.
Fault handling for warning UV fault, regulator 2	FSOb does not respond (default) FSOb goes low on fault (regulator also shuts down)
Fault handling for warning OV fault, regulator 2	FSOb does not respond (default) FSOb goes low on fault (regulator also shuts down)
Fault handling for warning UV fault, regulator 1	FSOb does not respond (default) FSOb goes low on fault (regulator also shuts down)
Fault handling for warning OV fault, regulator 1	FSOb does not respond (default) FSOb goes low on fault (regulator also shuts down)
Dependent fault handling. Controls if regulator 2 OC2 faults trigger regulator 1 shutdown	No dependent fault handling (default) Dependent fault handling
Dependent fault handling. Controls if regulator 1 OC2 faults trigger regulator 2 shutdown	No dependent fault handling (default) Dependent fault handling
Controls if regulator 2 severe OV or severe UV faults trigger regulator 1 shutdown.	No dependent fault handling (default) Dependent fault handling
Controls if regulator 1 severe OV or severe UV faults trigger regulator 2 shutdown.	No dependent fault handling (default) Dependent fault handling
Fault handling for PWM clock fault	FSOb does not respond (default) FSOb goes low on fault (regulator also shuts down)
Fault reaction hiccup or latchoff Hiccup: On detection of a fault, switching stops for 500ms and a restart from soft-start is attempted. This operation is repeated up to 8 times or until the fault conditions are removed. Latch-off: On detection of a fault, switching stops. Recovery from a latch off condition requires the latched off regulator(s) to be cycled off then on using the associated WAKE pin(s).	hiccup (default) latch-off
Control FLT1b and FLT2b assertion during the re-BISTing phase after ECM exit.  After ECM exit, the FuSa core re-BISTs logic and analog prior to re-evaluating the safe state condition. During this period, FSOb is driven low. However, the FuSa core cannot simultaneously self-test and provide FLTxb status. This option provides drive flexibility of the FLT1b and FLT2b pins during this self-test period.	Drive FLT1b and FLT2b low during re-BISTing phase (default) Hi-Z FLT1b and FLT2b during re-BISTing phase
FLT1b and FLB2b low assert duration on fault detection	FLTxb low only for duration of fault (default) FLTxb low for 10ms minimum or until fault is cleared FLTxb low for 50ms minimum or until fault is cleared FLTxb low for 200ms minimum or until fault is cleared

Configuration	Selections
EXT_EN pin channel reaction EXT_EN high indicates the selected regulators are enabled with their associated WAKE pins and not faulted.	Channel 1 is enabled. Channel 2 status is ignored. (default) Both channels enabled Channel 2 is enabled. Channel 1 status is ignored. Both channels enabled
Severe OVUV filter Fault digital debounce time (Ch1 and Ch2 programmed separately)	1μs (default) 5μs 10μs 25μs
Warning OVUV filter Fault digital debounce time (Ch1 and Ch2 programmed separately)	10μs (default) 25μs 50μs 100μs
VCC OV/UV, PGND OV/UV, and BG OV/UV fault Digital debounce time	10μs (default) 25μs 50μs 100μs
FuSa over-temperature filter Fault digital debounce time	50μs (default) 100μs 1000μs

#### 5.17 SYNC Pin

The SYNC pin allows users to select Channel to operate in Continuous Conduction Mode (CCM) switching, Diode Emulation Mode (DEM) switching, or Energy Conservation Mode (ECM) switching. ECM is available only for Buck Channel 1 and provides extremely low power consumption at light loads. Entry and exit into ECM mode is enabled by the SYNC pin (Pin 36).

With the SYNC pin set to logic high, Buck and Boost operation is always CCM, regardless of load on either output.

When the SYNC pin is driven to logic low, the Buck regulator, depending on load, operates in one of three modes:

- For loads where the voltage across the Buck RSNS resistor is 10mV or greater, the device continues to operate
  in FCCM. In FCCM operation, both high-side and low-side MOSFETs are switched on and off on every
  switching cycle.
- For loads where the voltage across the Buck RSNS resistor is between 2mV and 10mV at the moment when SYNC is set to GND, the device operates in DEM. DEM uses variable frequency to reduce switching losses and improve light-load efficiency, but unlike ECM operation protective functions are still active.
- For loads where the voltage across the Buck RSNS resistor is 2mV or less, the device enters ECM operation. Note: When the device enters ECM, the controller can remain in ECM operation even if the load increases and Buck RSNS voltage increases to 10mV. To enter ECM operation, the voltage on the VIN pin (Pin 29) must be in the range from 6V to 18.5V and the SYNC pin must be logic low. Note: In ECM operation, the device operates in an extremely low power state, which does not provide full FuSa support.

The RAA271041 can be configured to allow the Buck Controller to enter ECM to reduce power consumption. ECM allows the buck channel to provide a regulated output (with no load) while the device draws typically 8µA from the VCC supply. During ECM operation, the RAA271041 buck channel delivers power pulses to the output filter and loads at a frequency much lower than the normal switching frequency. Each power pulse supplies sufficient energy to supply small load currents with no requirement for a high-frequency multi-pulse burst operation. In the time interval between consecutive ECM power pulses, the RAA271041 drastically reduces its current consumption to minimize average standby current drawn from the input supply.

To enter ECM operation, the voltage on VIN (Pin 26) must be in a range from 6V to 18.5V and the SYNC pin must be logic low. If SYNC is directly connected to VCC, the circuit always operates in CCM. SYNC can be held low to command ECM operation when the load is small, and then SYNC can be driven high before a larger load is supplied, to force mode change to CCM and support the higher load. Alternatively, beginning with SYNC low at light load, SYNC can be driven by an external clock for synchronized operation, which forces ECM exit and CCM operation.

Note: During ECM operation, the device disables many FuSa functions to achieve an extremely low power state. Therefore, the Fail-Safe Output (FSOb) is driven low during ECM operation. When the device exits ECM operation, the Functional Safety BIST is performed. After all BIST functions are verified, the FSOb is driven high.

Also, the Boost controller must be off when Controller 1 is in ECM operation. If the boost controller is active using WAKE2, the buck controller does not enter ECM operation. If the buck controller is in ECM operation, the boost channel remains off until the Buck controller exits ECM from either a large load increase or the SYNC pin driven high to force ECM exit.

*Note*: This also means that if Buck is operating in ECM, the boost channel does not automatically turn on even if the VBATS voltage falls below 1V. This is because in ECM, most fault detection functions including the VBATS detection are disabled, to reduce operating current to an ultra-low state.

Note: There is no ECM operation available for the Boost Channel 2.

#### 5.17.1 Overview of ECM Setup and Operation

If Channel 1 (buck) is configured to allow ECM at light loads, the channel enters ECM operation if the following conditions are present:

- SYNC pin is set to logic low.
- VIN is between 6V to 18.5V.
- Buck load causes the voltage across the Buck RSEN resistor to be less than 2mV.
- Boost Channel 2 is off. For Cold Crank applications, the boost is typically off when the input voltage is at normal levels (VBATS pin is above 1V).

During ECM operation, the buck channel uses a voltage comparator in conjunction with an accurate current sense resistor and amplifier to detect load current. In between switching pulses, most of the device is off or in a very low-power state, resulting in extremely low operating current, and the load is supplied by the output capacitors. The output falls until the comparator detects the lower voltage threshold, at which point the IC energizes enough circuitry to generate a power pulse, which replenishes the output capacitors. Each ECM power pulse is terminated by one of two methods:

- Inductor current reaching the ECM peak current threshold.
- Output voltage reaching the overvoltage threshold.

Individual ECM power pulses are generated by the following procedure. First, the high-side MOSFET is turned ON (HS1 signal drives high) to apply  $V_{BOOST}$  (for Cold Crank) or  $V_{IN}$  (for IBB operation) to the output inductor. The inductor current ramps up from zero at a rate determined by the inductance and voltage from LX1 to VOUT1.

The current sense amplifier monitors the voltage level across the current sense resistor until the voltage reaches 13mV. When the 13mV threshold is attained, the high-side MOSFET is turned off and the low-side MOSFET is turned on. This forces the inductor current to ramp down to approximately 0A at which time an internal zero current comparator turns the low-side MOSFET off. After the low-side MOSFET is turned off, the IC returns to ultra-low guiescent current consumption.

Alternatively, if the output rises to approximately 3% of  $V_{OUT}$  before the peak current is detected, the high-side pulse is terminated followed by the low-side MOSFET turning on.



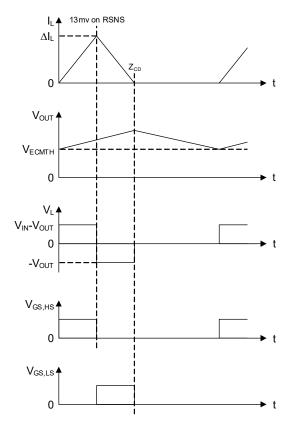


Figure 23. Energy Conservation Mode (ECM) Operational Waveforms

#### 5.17.2 ECM Entry and Exit

The current sense resistor and amplifier set thresholds that allow ECM entry and control power pulse generation. To understand ECM power pulse operation, the current sense resistor (in series with the power inductor) is selected to produce a 50mV signal between ISEN1P and ISEN1N when the full load current is applied to the output. If ECM is allowed (SYNC = GND) and the load reduces to a level at which the signal across the current sense resistor is 2mV (typical), the circuit enters ECM. The circuit remains in ECM as the load is further reduced to minimal or no load.

If the load increases, the circuit remains in ECM operation, but it cannot support load currents in which the RSNS signal exceeds approximately 6.5mV.

# 6. Application Information

Several factors should be considered when selecting components for buck and boost regulators. This section discusses some examples of how to decide the parameters of the external components based on the typical application schematic shown in Figure 4. In the actual application, the parameters might need to be adjusted and also a few more additional components might need to be added for the application-specific noise, physical sizes, thermal, testing, and other requirements.

# 6.1 Buck Channel Components

#### 6.1.1 Buck Inductor Selection

While the buck channel is operating in a stable Continuous Conduction Mode (CCM), the output voltage and on-time of the high-side transistor is determined by Equation 3, where T is the switching cycle ( $1/f_{SW}$ ) and D =  $t_{ON}/T$  is the on-duty of the high-side transistor.



(EQ. 3) 
$$V_{OUT} = V_{IN} \times \frac{t_{ON}}{T} = V_{IN}D$$

Under this CCM condition, the inductor ripple current can be defined as Equation 4:

(EQ. 4) 
$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} = t_{OFF} \times \frac{V_{OUT}}{L}$$

From the previous equations, use Equation 5 to determine the inductor value.

(EQ. 5) 
$$L = \frac{V_{IN} - V_{OUT}}{f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In general, when the inductor value is determined, the ripple current varies by the input voltage. At the maximum input voltage, the on-duty becomes the minimum and the ripple current becomes the maximum. Therefore, use Equation 6 to estimate the minimum inductor value.

(EQ. 6) 
$$L_{min} = \frac{V_{IN,max} - V_{OUT}}{f_{SW} \times \Delta I_{I,max}} \times \frac{V_{OUT}}{V_{IN,max}}$$

In a Buck regulator, this ripple current is normally selected to be between 20% and 50% of the maximum DC output current. A typical starting point is to set the ripple current to 30% of the maximum DC output current. Larger inductor values reduce the ripple current and ripple voltage. However, larger inductor values can slow the response time of the channel to load transients. Also, the larger inductance reduces the RSNS current ramp signal and can result in noise sensitivity.

Under stable operation, the peak current flow in the inductor is the sum of output current and 1/2 of ripple current.

(EQ. 7) 
$$I_{L,pk} = \frac{\Delta I_L}{2} + I_{OUT}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current can be observed at the startup or heavy load transient. Therefore, the size of the inductor should be determined with the consideration of these conditions. Also, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the saturation current rating of the inductor.

*Note*: The OC1 signal is fixed at 80mV (1.6x of full load) and the OC2 hiccup threshold is fixed at 100mV (2x of full load); therefore, the inductor should have a saturation value exceeding 2x full load current.

ECM operation is based on a fixed peak signal of 13mV, which is well below the OC1 level, therefore, there are no special considerations for inductor selection for ECM.

## 6.1.2 Buck Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, output capacitors are required. The current mode control loop allows the usage of low ESR ceramic capacitors for smallest size, and/or electrolytic and polymer capacitors that offer larger capacitance values but with higher ESR and increased physical size. While the ceramic capacitor offers excellent overall performance and reliability, the actual capacitance can be reduced considerably when operated with significant DC bias voltage. Carefully review the capacitor manufacturer's information when selecting output capacitors.

The following are equations for the required capacitance value to meet the required ripple voltage level. Additional capacitance can lower the ripple voltage and to improve transient response.

For the ceramic capacitor (low ESR):



(EQ. 8) 
$$V_{OUT,rip} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}$$

where  $\Delta I_L$  is the inductor's peak-to-peak ripple current,  $f_{SW}$  is the switching frequency and  $C_{OUT}$  is the output capacitor.

Required minimum output capacitance based on ripple current is:

(EQ. 9) 
$$C_{OUT,min} = \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT,rip}}$$

If using electrolytic capacitors, the ESR is the dominant portion of the ripple voltage.

(EQ. 10) 
$$V_{OUT.rip.ESR} = \Delta I_L \times ESR$$

Therefore, to reduce the ripple voltage, select the electrolytic capacitor based on maximum ESR, use multiple capacitors in parallel to reduce the ESR, or increase inductor value to reduce the ripple current.

The output capacitor value selected for CCM might require adjustment for ECM operation depending on the magnitude of ripple voltage allowed on VOUT. In standard ECM operation when there is no external loading, the output capacitor must absorb the complete pulse of energy from the output inductor peak current of 120% of full load current. Both the capacitance value and ESR should be considered for ECM operation. The capacitance should be large enough to absorb the energy with acceptable voltage rise and the ESR must be small enough to control the potentially large step in voltage equal to lpk, ECM × ESR.

In addition to output voltage ripple requirements, select the buck output capacitor value in conjunction with the inductor to meet output deviation requirements during normal CCM operation, ECM, and load transients.

Equation 11 calculates the value of C<sub>OUT</sub> required during load reduction and the output voltage overshoots the nominal level.

(EQ. 11) 
$$C_{OUT\_MIN\_STEP\_DOWN} = \frac{L\left(I_{STEP} + \frac{\Delta I_{L}}{2}\right)^{2}}{2 \times V_{OUT} \times \Delta V}$$

When the load is increased, the output undershoots the nominal value and the value of C<sub>OUT</sub> required is calculated using Equation 12.

(EQ. 12) 
$$C_{OUT\_MIN\_STEP\_UP} = \frac{L\left(I_{STEP} + \frac{\Delta I_{L}}{2}\right)^{2}}{2 \times (V_{IN} - V_{OUT}) \times \Delta V}$$

#### 6.1.3 Buck Input Capacitor

The Buck input power rail can incorporate a combination of electrolytic and ceramic capacitors to provide a stable input voltage while supplying pulse currents at the buck switching frequency. The voltage rating of the capacitors should exceed the maximum input voltage, a 20% margin is typically a good starting point.

The minimum value of the Buck input capacitors can be estimated by limiting the drop in VIN ( $\Delta V_{IN}$  below) to approximately 1% when delivering the full load current during the on-time of the high-side MOSFET:

$$\text{(EQ. 13)} \quad C_{IN,min} = \frac{I_{OUT,max} \times D \times (1-D)}{f_{SW} \times \Delta V_{IN}}$$

The specific capacitor(s) used should be selected with an RMS current capability exceeding the value estimated by the relation shown in Equation 14.



(EQ. 14) 
$$I_{CIN RMS} \cong I_{OUT max} \times \sqrt{D \times (1 - D)}$$

#### 6.1.4 Buck MOSFET Selection

The external MOSFETs that are driven by the RAA271041 controller need to be carefully selected to optimize the design of the synchronous buck regulator. The input voltage is typically the automotive range for battery supply, so the MOSFETs are normally rated at 40V BVdss. As the high-side and low-side gate drivers are a 5V output, the MOSFET VGS needs to be specified in this range. The MOSFET should have a low total gate charge (Qgd) and low specified ON-resistance  $(r_{DS(ON)})$  at VGS = 4.5V or 5V. Renesas recommends ensuring the minimum VGS threshold is higher than 1.2V, but not exceeding 2.5V to ensure the MOSFETs can be switched off reliably throughout the complete  $V_{CC}$  range.

#### 6.1.5 Control Loop Compensation Components for the Buck Channel

Several components selected for the power, filtering, and current sense circuits play a role in the determination of the compensating components.

To determine the external component values of the compensator, start by understanding the uncompensated loop gain transfer function that is defined in Equation 15. This forms the basis for designing the compensator.

$$\text{(EQ. 15)} \quad \text{$T_{uncompensated}(s)$} = \frac{\text{$H \times K_m \times G_{vd}(s)$}}{1 + (\text{$K_m \times G_{id}(s) \times R_i)$}}$$

where,

- H is the output voltage feedback gain.
- K<sub>m</sub> is the modulator gain.
- $G_{vd}$  (s) is the voltage-to-duty cycle transfer function.
- $G_{id}$  (s) is the current-to-duty cycle transfer function.
- R<sub>i</sub> is the total current sensing gain.

#### 6.1.5.1 Parameter Definitions

The following are listed parameter definitions for guidance with the equations.

$$H = \frac{V_{ref}}{V_{out}}$$

$$V_{ref} = 0.8V$$

$$K_{m} = \frac{1}{V_{in} \times ramp\_slope}$$

$$ramp\_slope = \frac{38.1mV}{V \text{ of } V_{in}}$$

$$G_{vd}(s) = G_{vd0} \times \frac{1 + \frac{s}{\omega_{z1}}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q\omega_0} + 1}$$



$$G_{vd0} \,=\, V_{in} \times \frac{R}{R_L + R}$$

$$\omega_{z1} = \frac{1}{C \times R_C}$$

$$\omega_0 = \sqrt{\frac{R + R_L}{L \times C \times (R + R_c)}}$$

$$Q = \frac{\sqrt{L \times C \times (R + R_L) \times (R + R_C)}}{C \times (R_L \times R + R_L \times R_C + R \times R_C) + L}$$

$$G_{id}(s) = G_{id0} \times \frac{1 + \frac{s}{\omega_{z2}}}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q\omega_0} + 1}$$

$$G_{id0} = V_{in} \times \frac{1}{R_L + R}$$

$$\omega_{z2} = \frac{1}{C \times (R + R_C)}$$

R = output resistance

$$R_L = DCR + R_{sense}$$

 $R_C = ESR$  of output capacitor

$$R_i = R_{IFB} \times R_{sense} \times G_{m,CSA}$$

$$R_{IFB} = 60k\Omega$$

$$R_{sense} = \frac{50mV}{I_{out}}$$

$$G_{m, CSA} = 91.25 \mu S$$

$$G_{m, EA} = 1.7mS$$

#### 6.1.5.2 Steps to Calculate Compensation Components

The following section focuses on the steps to calculate external component values for Type II compensation network.

#### RAA271041 Datasheet

1. Select the required crossover frequency (f<sub>c</sub>) using Equation 16.

(EQ. 16) 
$$f_{c} = \frac{f_{sw}}{10}$$

(EQ. 17) 
$$\omega_{\rm C} = 2 \times \pi \times f_{\rm C}$$

2. Find the uncompensated loop gain ( $G_{fc}$ ) and phase ( $\phi_{fc}$ ) at  $f_c$  using Equation 18 and Equation 19, respectively.

(EQ. 18) 
$$G_{fc} = |T_{uncompensated}(j\omega_c)|$$

(EQ. 19) 
$$\varphi_{fc} = \angle T_{uncompensated}(j\omega_c)$$

Renesas recommends using a tool such as MATLAB, Mathcad, or Python to accurately estimate the phase at the crossover frequency ( $\phi_{PM.fc}$ ).

(EQ. 20) 
$$\phi_{PM,fc} = 180 + \phi_{fc}$$

*Note*: To meet the phase margin target ( $\phi_{PM,target}$ ) of ≥55°,  $\phi_{PM,fc}$  must be ≥55° when using a Type II compensator. If not, reduce  $f_c$  or switch to a Type III compensator.

3. Use Equation 22 to compute for the phase contribution ( $\phi_{boost}$ ) required from the compensator at  $f_c$ . Phase margin targets of 45° to 60° are considered safe values. For Type II compensator, only less than 90° phase boost can be achieved.

(EQ. 21) 
$$\varphi_{comp\_target} = \varphi_{PM, target} - \varphi_{PM, fc}$$

(EQ. 22) 
$$\varphi_{boost} = 90 + \varphi_{comp target}$$

4. Use Equation 23 to determine the location of the high frequency pole (fp) of the compensator.

$$\text{(EQ. 23)} \quad \text{ } f_p = \left( tan \bigg( \phi_{boost} \times \frac{\pi}{180} \bigg) + \sqrt{tan \bigg( \phi_{boost} \times \frac{\pi}{180} \bigg)^2 + 1} \right) \times f_c$$

5. To find the location of the zero  $(f_z)$  of the compensator, first evaluate the location of the ESR zero  $(f_{z,ESR})$ , which can be calculated using Equation 24.

(EQ. 24) 
$$f_{z,ESR} = \frac{1}{2\pi \times R_C \times C}$$

a. If  $f_p$  is lower than  $f_{z,ESR}$ , calculate  $f_z$  using Equation 25.

(EQ. 25) 
$$f_z = \frac{f_c^2}{f_p}$$

b. If  $f_p$  is higher than  $f_{z,ESR}$ , set  $f_{z,ESR}$  as the new value of the high frequency pole ( $f_{p,new}$ ). Consequently, there is a new crossover frequency ( $f_{c.new}$ ) defined by Equation 26.

(EQ. 26) 
$$f_{c, new} = min(\frac{f_{p, new}}{2.5}, f_c)$$

Using  $f_{c,new}$  as the crossover frequency, repeat Steps 2 and 3 to determine the new target phase boost  $(\phi_{boost,new})$ . Using  $f_{c,new}$  and  $\phi_{boost,new}$ , estimate the position of  $f_z$  using Equation 27.

$$\text{(EQ. 27)} \quad f_{\text{Z}} = \frac{f_{\text{c, new}}}{\left( tan \left( \phi_{\text{boost,new}} \times \frac{\pi}{180} \right) + \sqrt{tan \left( \phi_{\text{boost,new}} \times \frac{\pi}{180} \right)^2 + 1} \right)}$$

The preceding procedure gives the necessary phase boost at crossover but does not guarantee that it occurs at the crossover point. To extract maximum phase boost from the compensator, recalculate  $f_{c,new}$  using Equation 28. This shifts the crossover to the geometric mean of  $f_z$  and  $f_{p,new}$ , reducing loop bandwidth while maximizing phase boost.

(EQ. 28) 
$$f_{c, new} = \sqrt{f_{p, new} \times f_z}$$

Using  $f_{c,new}$ , recalculate the uncompensated loop gain  $G_{fc}$  in Step 2.

6. Use Equation 29 to determine the compensator gain at the selected crossover frequency.

(EQ. 29) 
$$G_{comp} = 10^{\left(\frac{-G_{fc}}{20}\right)}$$

7. Use Equation 30, Equation 31, and Equation 32 to calculate the external compensation components.

(EQ. 30) 
$$R_{comp} = \frac{G_{comp}}{G_{m, EA}}$$

(EQ. 31) 
$$C_z = \frac{1}{2\pi \times R_{comp} \times f_z}$$

(EQ. 32) 
$$C_p = \frac{1}{2\pi \times R_{comp} \times f_p}$$

### 6.1.6 Design Example

#### 6.1.6.1 Application

Design the buck regulator operating in CCM to meet the following specification:

- Input voltage range V<sub>IN</sub>: 7.5V to 42V, 12V typical
- Output voltage V<sub>OUT</sub>: 5V
- Output current I<sub>OUT</sub>: 6A
- Overcurrent1 limit OC1: 10A
- Switching frequency f<sub>sw</sub>: 2.2MHz
- Output ripple voltage V<sub>OUT.rip</sub>: <1%</li>

### **6.1.6.2** Solution

$$D = \frac{5V}{12V} = 0.417$$

$$T = \frac{1}{2.2MHz} = 454.55ns$$

$$t_{ON} = 0.417 \times 454.55 \text{ns} = 189.39 \text{ns}$$

$$t_{OFF} = (1 - 0.417) \times 454.55 \text{ns} = 265.15 \text{ns}$$

Set the inductor ripple current  $\Delta I_L$  to 50% of  $I_{OUT}$ .

$$L_{min} = \frac{42V - 5V}{2.2MHz \times (0.5 \times 6A)} \times \frac{5V}{42V} = 0.667 \mu H$$

Let  $L = 1\mu H$ .

$$\Delta I_L = 189.39 \text{ns} \times \frac{12V - 5V}{1\mu H} = 1.326 \text{A}$$

$$I_{L, pk} = \frac{1.326A}{2} + 6A = 6.663A$$

$$C_{OUT,min} = \frac{1.326A}{8 \times 2.2MHz \times (0.01 \times 5V)} = 1.507 \mu F$$

Set the acceptable overshoot when load goes from 90% to 10% of  $I_{OUT}$  to 100mV

$$C_{OUT\_MIN\_STEP\_DOWN} = \frac{1.8 \mu H \times \left( (0.8 \times 6A) + \frac{0.737A}{2} \right)^2}{2 \times 5V \times 100 mV} = 48.08 \mu F$$

Set the acceptable undershoot when load goes from 10% to 90% of I<sub>OUT</sub> to 100mV

$$C_{OUT\_MIN\_STEP\_DOWN} = \frac{1.8 \mu H \times \left( (0.8 \times 6A) + \frac{0.737A}{2} \right)^2}{2 \times (12V - 5V) \times 100 mV} = 34.34 \mu F$$

Pick  $C_{OUT} = 5 \times 22 \mu F$ .

Limit the drop in V<sub>IN</sub> to 1% when delivering the full load current during the on-time of the high side MOSFET.

$$C_{IN,min} = \frac{6A \times 0.417 \times (1 - 0.417)}{2.2MHz \times (0.01 \times 12V)} = 5.524 \mu F$$

$$I_{CIN.RMS} \cong 6A \times \sqrt{0.417 \times (1 - 0.417)} = 2.96A$$

Calculate the sense resistor.

$$R_{\text{sense}} = \frac{50\text{mV}}{6\Delta} = 0.00833\Omega$$

Let R<sub>sense</sub> = 8mΩ.

Calculate the parameters defined in Section 6.1.5.1.

$$H = \frac{0.8V}{5V} = 0.16$$

$$K_{m} = \frac{1}{12V \times \frac{38.1mV}{V}} = \frac{2.187}{V}$$

$$R = \frac{5V}{6A} = 0.833\Omega$$

$$R_L \,=\, 0.0056\Omega + 0.008\Omega \,=\, 0.014\Omega$$

$$G_{vd0} \,=\, 12 V \times \frac{0.833 \Omega}{0.014 \Omega + 0.833 \Omega} \,=\, 11.807 V$$

$$\omega_{z1} = \frac{1}{(5 \times 22 \mu F) \times 0.005 \Omega} = 1.818 MHz$$

$$\omega_0 \,=\, \sqrt{\frac{0.833\Omega + 0.014\Omega}{1\mu H \times (5 \times 22\mu F) \times (0.833\Omega + 0.005\Omega)}} \,=\, 95.834$$

$$Q = \frac{\sqrt{1\mu H \times (5 \times 22\mu F) \times (0.833\Omega + 0.014\Omega) \times (0.833\Omega + 0.005\Omega)}}{(5 \times 22\mu F) \times (0.014\Omega \times 0.833\Omega + 0.014\Omega \times 0.005\Omega + 0.833\Omega \times 0.005\Omega) + 1\mu H} = 3.258$$

$$G_{id0} = 12V \times \frac{1}{0.014\Omega + 0.833\Omega} = 14.169A$$

$$\omega_{Z2} = \frac{1}{(5 \times 22 \mu F) \times (0.833 \Omega + 0.005 \Omega)} = 10.844 kHz$$

$$R_{j}~=~60k\Omega\times0.008\Omega\times91.25\mu S~=~0.044\Omega$$

Using the calculated values, simplify the uncompensated loop gain transfer function.

$$T_{uncompensated}(s) = \frac{0.16 \times \frac{2.187}{V} \times G_{vd}(s)}{1 + \left(\frac{2.187}{V} \times G_{id}(s) \times 0.044\Omega\right)}$$

Select the required crossover frequency.

$$f_c = \frac{2.2MHz}{10} = 220kHz$$

$$\omega_{_{\textstyle C}} \, = \, 2 \times \pi \times 220 kHz \, = \, 1.382 MHz$$

Plot the derived uncompensated loop gain transfer function to estimate the gain and phase at the crossover frequency.

$$G_{fc} = -34.26$$

$$\phi_{fc} = -102^{\circ}$$

$$\phi_{PM\ fc} = 180^{\circ} - 102^{\circ} = 78^{\circ}$$

$$\phi_{comp\ target} = 60^{\circ} - 78^{\circ} = -18^{\circ}$$

$$\varphi_{boost} = 90^{\circ} - 18^{\circ} = 72^{\circ}$$

$$f_p = \left(tan\left(72^{\circ} \times \frac{\pi}{180}\right) + \sqrt{tan\left(72^{\circ} \times \frac{\pi}{180}\right)^2 + 1}\right) \times 220 \text{kHz} = 1.389 \text{MHz}$$

$$f_{z,ESR} = \frac{1}{2\pi \times 0.005\Omega \times (5 \times 22\mu F)} = 289.373kHz$$

Since  $f_p$  is higher than  $f_{z,ESR}$ , the value of  $f_{z,ESR}$  is set as the new value of  $f_p$ .

$$f_{p. new} = 289.373 kHz$$

$$f_{c, new} = min\left(\frac{289.373kHz}{2.5}, 220kHz\right) = 115.749kHz$$

$$\omega_{c,new} = 2 \times \pi \times 115.749 \text{kHz} = 727.273 \text{kHz}$$

$$\begin{split} G_{fc,new} &= -27.58 \\ \phi_{fc,new} &= -99^{\circ} \\ \phi_{PM,\,fc,new} &= 180^{\circ} - 99.31^{\circ} = 81^{\circ} \\ \phi_{comp\_target,new} &= 60^{\circ} - 80.69^{\circ} = -21^{\circ} \\ \phi_{boost,new} &= 90^{\circ} - 20.69^{\circ} = 69^{\circ} \\ f_{z} &= \frac{115.7 \text{kHz}}{\left( \text{tan} \left( 69.31^{\circ} \times \frac{\pi}{180} \right) + \sqrt{\text{tan} \left( 69.31^{\circ} \times \frac{\pi}{180} \right)^{2} + 1} \right)} = 21.453 \text{kHz} \end{split}$$

To extract maximum phase boost from the compensator, recalculate  $f_{c,new}$ .

$$f_{c, new} = \sqrt{289.373 \text{kHz} \times 21.453 \text{kHz}} = 78.79 \text{kHz}$$

$$G_{fc, new} = -23.85$$

Use the uncompensated loop gain  $G_{fc}$  at  $f_{c,new}$  to calculate the compensation network components.

$$\begin{split} G_{comp} &= 10 & = 15.578 \\ R_{comp} &= \frac{15.578}{1.7 \text{mS}} = 9.163 \text{k}\Omega \\ C_{z} &= \frac{1}{2\pi \times 9.163 \text{k}\Omega \times 21.453 \text{kHz}} = 0.81 \text{nF} \\ C_{p} &= \frac{1}{2\pi \times 9.163 \text{k}\Omega \times 289.373 \text{kHz}} = 60.022 \text{pF} \end{split}$$

The calculated component values are theoretical and serve as a starting point. Actual performance can vary depending on various factors such as board layout and parasitics. Further tuning on the actual board can be necessary to meet design targets.

If the phase margin is lower than the target, consider either increasing  $C_z$  or decreasing  $C_p$  to improve stability.

## 6.2 Boost Channel Components

### 6.2.1 Bootstrap Resistor Circuit

In an application board, it is common to have ringing noise when the LX and BOOT nodes swing with high dv/dt. This is a result of parasitic inductance and capacitance in the LX node and Boot capacitor routing on the printed circuit board and in the MOSFET structure. The generated noise can disrupt portions of the control circuit analog sense lines and might require some suppression. A simple method to reduce the noise involves placing a resistor of small value (typically from  $1\Omega$  to  $10\Omega$ ) between the BOOT pin and the junction of the boot diode and boot capacitor. This slows down the high-side MOSFET turn-on to reduce the dv/dt of the LX rising edge.

#### 6.2.2 Boost Inductor Selection

While the boost channel is operating in stable Continuous Conduction Mode (CCM), the output voltage and the low-side transistor on-time is determined by Equation 33, where  $\eta$  is the efficiency of the converter, T is the switching cycle (1/f<sub>SW</sub>), and D = t<sub>ON</sub>/T is the high-side on-duty of the transistor.



(EQ. 33) 
$$V_{OUT} = \frac{V_{IN} \times \eta}{1 - \frac{t_{ON}}{T}} = \frac{V_{IN} \times \eta}{1 - D}$$

Under this CCM condition, the inductor ripple current can be defined using Equation 34.

(EQ. 34) 
$$\Delta I_L = D \times T \times \frac{V_{IN}}{I}$$

The previous equations can be rearranged to determine the inductor value using Equation 35.

(EQ. 35) 
$$L = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{V_{IN}}{\Delta I_L \times f_{SW}}\right)$$

In all the previous equations, the Boost minimum input voltage must be considered. *Note*: If a boost regulator is maintaining a fixed output voltage and a fixed load current, the Boost output power is constant. The boost input power must also remain relatively constant. Due to this constraint, as the input voltage falls, the boost input current must rise to maintain constant power. Therefore, the boost input current is maximum at the lowest input voltage and the maximum boost load. This relationship can significantly affect the selection of both the inductor and the power MOSFETs.

Therefore, as the boost input voltage falls, the inductor and MOSFET current-handling capacity must increase proportionally. Renesas recommends setting the minimum input voltage as high as possible in accordance with the input voltage requirements to minimize the size and cost of the inductor and MOSFETs.

In a Boost regulator, the inductor ripple current is normally selected to be between 20% and 50% of the maximum DC input current. A typical starting point is to set the ripple current to 30% of the maximum DC input current. Larger inductor values reduce the ripple current and ripple voltage. However, larger inductor values can slow the response time of the channel to load transients. Also, the larger inductance reduces the RSNS current ramp signal and can result in noise sensitivity.

Under stable operation, the peak current flow in the inductor is the sum of maximum input current (full load and minimum  $V_{IN}$ ) and 1/2 of ripple current.

(EQ. 36) 
$$I_{L,pk} = \frac{\Delta I_L}{2} + I_{IN}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current can be observed at the startup, heavy load transient, and minimum input voltage. Therefore, the inductor's size must be determined with the consideration of these conditions. Also, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the inductor's saturation current rating.

*Note*: The OC1 signal is fixed at 80mV (160% of full load) and the OC2 hiccup threshold is fixed at 100mV; therefore, the inductor should have a saturation value exceeding 2x full load current.

#### 6.2.3 Boost Output Capacitor

Output capacitors are required to filter the inductor current ripple and to provide energy storage to support transient load conditions, and a combination of electrolytic and ceramic capacitors is normally used. The ceramic capacitors filter the high-frequency spikes of the main switching devices and absorb the highest frequency components of the trapezoidal output current flowing through the output rectifier of a boost channel. In layout, place these output ceramic capacitors as close as possible to the main switching devices to maintain the smallest switching loop. To maintain capacitance over the biased voltage and temperature range, Renesas recommends using high-quality capacitors such as X7R or X5R. The electrolytic capacitors handle the load transient and output ripples.



Use Equation 37 to estimate the minimum output capacitor.

(EQ. 37) 
$$C_{OUT,min} = \frac{I_{OUT} \times D}{f_{sw} \times V_{OUT,rip}}$$

The boost output ripple at the switching frequency is mainly determined by the trapezoidal rectifier current and output capacitance value. For the boost channel, the maximum output voltage ripple can be estimated using Equation 38, where  $I_{OUT,max}$  is the load current at output, C is the total capacitance at output, and  $D_{MIN}$  is the minimum duty cycle at  $V_{IN,max}$  and  $V_{OUT,min}$ .

(EQ. 38) 
$$V_{OUT,rip} = \frac{I_{OUT,max} \times (1 - D_{MIN})}{8C \times 2 \times f_{SW}}$$

### 6.2.4 Control Loop Compensation Components for the Boost Channel

To determine the external component values of the compensator, start by understanding the uncompensated loop gain transfer function, defined in Equation 39. This forms the basis for designing the compensator.

(EQ. 39) 
$$T_{uncompensated}(s) = H \times G_{vc}(s)$$

where,

- H is the output voltage feedback gain.
- $G_{vc}(s)$  is the voltage-to-control transfer function.

#### 6.2.4.1 Parameter Definitions

$$H = \frac{V_{ref}}{V_{out}}$$

$$V_{ref} = 0.8V$$

$$G_{vc}(s) = \frac{G_{vd}(s) \times Z_L}{\frac{Z_L}{F_m} + V_{out} \times R_i - G_{vd}(s) \times (1 - D) \times R_i}$$

$$G_{vd}(s) = G_{vd0} \times \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \times \left(1 - \frac{s}{\omega_{z2}}\right)}{\left(\frac{s}{\omega_{0}}\right)^{2} + \frac{s}{Q\omega_{0}} + 1}$$

$$G_{vd0} = \frac{V_{out}}{1 - D} \times \frac{(1 - D)^2 \times R - R_L}{(1 - D)^2 \times R + R_L}$$

$$\omega_{z1} = \frac{1}{C \times R_C}$$

$$\omega_{z2} = \frac{(1-D)^2 \times R - R_L}{L}$$

$$\omega_0 \, = \, \sqrt{\frac{\left(1-D\right)^2 \times R + R_L}{L \times C \times (R + R_c)}}$$

$$Q = \frac{\sqrt{L \times C \times ((1-D)^2 \times R + R_L) \times (R + R_C)}}{C \times (R_L \times R + R_L \times R_C + R \times R_C \times (1-D)^2) + L}$$

R = output resistance

$$R_I = DCR + R_s$$

 $R_C = ESR$  of output capacitor

$$Z_I = s \times L + R_I$$

$$F_{m} = \frac{1}{V_{ramp}}$$

$$V_{ramp} = 0.8V$$

$$R_i = R_{IFB} \times R_{sense} \times G_{m,CSA}$$

$$R_{IFB} = 144k\Omega$$

$$R_{\text{sense}} = \frac{50 \text{mV}}{I_{\text{out}}}$$

$$G_{m. CSA} = 91.25 \mu S$$

$$G_{m,EA} = 1.7mS$$

### 6.2.4.2 Steps to Calculate Compensation Components

The following section focuses on the steps to calculate external component values for Type II compensation network.

1. Select the required crossover frequency (f<sub>c</sub>) using Equation 42.

(EQ. 40) 
$$f_{c1} = \frac{f_{sw}}{10}$$

(EQ. 41) 
$$f_{c2} = \frac{1}{5} \times \frac{\omega_{z2}}{2\pi}$$

**(EQ. 42)** 
$$f_c = min(f_{c1}, f_{c2})$$

(EQ. 43) 
$$\omega_{\rm C} = 2 \times \pi \times f_{\rm C}$$

2. Find the uncompensated loop gain ( $G_{fc}$ ) and phase ( $\phi_{fc}$ ) at  $f_c$  using Equation 44 and Equation 45, respectively.

(EQ. 44) 
$$G_{fc} = |T_{uncompensated}(j\omega_c)|$$

(EQ. 45) 
$$\varphi_{fc} = \angle T_{uncompensated}(j\omega_c)$$

Renesas recommends using a tool such as MATLAB, Mathcad, or Python to accurately estimate the phase at the crossover frequency ( $\phi_{PM fc}$ ).

(EQ. 46) 
$$\phi_{PM, fc} = 180 + \phi_{fc}$$

Note: To meet the phase margin target (φ<sub>PM,target</sub>) of ≥55°, φ<sub>PM,fc</sub> must be ≥55° when using a Type II compensator. If not, reduce f<sub>c</sub> or switch to a Type III compensator.

3. Use Equation 47 to compute for the phase contribution ( $\phi_{boost}$ ) needed from the compensator at  $f_c$ . Phase margin targets of 45° to 60° are considered safe values. For Type II compensator, only less than 90° phase boost can be achieved.

(EQ. 47) 
$$\varphi_{comp\_target} = \varphi_{PM, target} - \varphi_{PM, fc}$$

(EQ. 48) 
$$\phi_{boost} = 90 + \phi_{comp target}$$

4. Use Equation 49 to determine the location of the high frequency pole (f<sub>p</sub>) of the compensator.

$$\text{(EQ. 49)} \quad f_p = \left(tan\Big(\phi_{boost} \times \frac{\pi}{180}\Big) + \sqrt{tan\Big(\phi_{boost} \times \frac{\pi}{180}\Big)^2 + 1}\right) \times f_c$$

To find the location of the zero  $(f_z)$  of the compensator, first evaluate the location of the ESR zero  $(f_{z,ESR})$ , which can be calculated using Equation 50.

(EQ. 50) 
$$f_{z,ESR} = \frac{1}{2\pi \times R_C \times C}$$

a. If  $f_D$  is lower than  $f_{Z,ESR}$ , calculate  $f_Z$  using Equation 51.

(EQ. 51) 
$$f_z = \frac{f_c^2}{f_p}$$

b. If  $f_p$  is higher than  $f_{z,ESR}$ , set  $f_{z,ESR}$  as the new value of the high frequency pole ( $f_{p,new}$ ). Consequently, there will be new crossover frequency ( $f_{c,new}$ ) defined by Equation 52.

**(EQ. 52)** 
$$f_{c, \text{ new}} = \min(\frac{f_{p, \text{ new}}}{2.5}, f_{c})$$

Using f<sub>c.new</sub> as the crossover frequency, repeat Steps 2 and 3 to determine the new target phase boost  $(\phi_{boost,new})$ . Using  $f_{c,new}$  and  $\phi_{boost,new}$ , estimate the position of  $f_z$  using Equation 53.

$$\text{(EQ. 53)} \quad f_{\text{Z}} = \frac{f_{\text{c, new}}}{\left( \text{tan} \Big( \phi_{\text{boost,new}} \times \frac{\pi}{180} \Big) + \sqrt{\text{tan} \Big( \phi_{\text{boost,new}} \times \frac{\pi}{180} \Big)^2 + 1 \right)}$$

The above procedure provides the necessary phase boost at crossover but doesn't guarantee it occurs at the crossover point. To extract maximum phase boost from the compensator, recalculate f<sub>c,new</sub> using Equation 54. This shifts the crossover to the geometric mean of fz and fp,new, reducing loop bandwidth while maximizing phase boost.

(EQ. 54) 
$$f_{c, \text{ new}} = \sqrt{f_{p, \text{ new}} \times f_z}$$

Using  $f_{c.new}$ , recalculate the uncompensated loop gain  $G_{fc}$  in Step 2.



6. Use Equation 55 to determine the compensator gain at the selected crossover frequency.

(EQ. 55) 
$$G_{comp} = 10^{\left(\frac{-G_{fc}}{20}\right)}$$

7. Use Equation 56, Equation 57, and Equation 58 to calculate the external compensation components.

(EQ. 56) 
$$R_{comp} = \frac{G_{comp}}{G_{m, EA}}$$

(EQ. 57) 
$$C_z = \frac{1}{2\pi \times R_{comp} \times f_z}$$

(EQ. 58) 
$$C_p = \frac{1}{2\pi \times R_{comp} \times f_p}$$

### 6.2.5 Design Example

### 6.2.5.1 Application

Design the boost regulator to meet the following specification:

- Input voltage V<sub>IN</sub>: 7.5V minimum, 8V typical
- Output voltage V<sub>OUT</sub>: 12V
- Output current I<sub>OUT</sub>: 3A
- Switching frequency f<sub>sw</sub>: 2.2MHz
- Output ripple voltage V<sub>OUT.rip</sub>: <1%</li>

#### 6.2.5.2 Solution

Assume that the efficiency of the boost regulator is 80%.

$$D = 1 - \frac{8V \times 0.8}{12V} = 0.467$$

$$D_{max} = 1 - \frac{7.5V \times 0.8}{12V} = 0.5$$

Set the inductor ripple current  $\Delta I_L$  to 50% of  $I_{OUT}$ .

$$\Delta I_{L} = 0.5 \times 3A \times \frac{12V}{8V} = 2.25A$$

$$L_{min} = \left(1 - \frac{8V}{12V}\right) \times \left(\frac{8V}{2.25 \times 2.2MHz}\right) = 0.539 \mu H$$

Let  $L = 0.68 \mu H$ .

$$\Delta I_L = \frac{7.5V \times 0.5}{2.2MHz \times 0.68\mu H} = 2.507A$$

$$I_{L, pk} = \frac{3A}{1 - 0.5} + \frac{\Delta I_{L}}{2} = 7.253A$$

$$C_{OUT,min} = \frac{3A \times 0.5}{2.2MHz \times (0.01 \times 12)} = 5.682 \mu F$$

Pick  $C_{OUT} = 3 \times 10 \mu F$ .

Let 
$$R_{\text{sense}} = 3m\Omega$$
.

Calculate the parameters defined in Section 6.2.4.1.

$$H = \frac{0.8V}{12V} = 0.067$$

$$G_{vd0} = \frac{12V}{1 - 0.467} \times \frac{(1 - 0.467)^2 \times 4\Omega - 0.0068\Omega}{(1 - 0.467)^2 \times 4\Omega + 0.0068\Omega} = 22.233V$$

$$\omega_{z1} = \frac{1}{(3 \times 10 \mu F) \times 0.005 \Omega} = 6.667 MHz$$

$$\omega_{Z2} = \frac{\left(1 - 0.467\right)^2 \times 4\Omega - 0.0068\Omega}{0.68 \mu H} = 1.663 MHz$$

$$\omega_0 = \sqrt{\frac{(1 - 0.467)^2 \times 4\Omega + 0.0068\Omega}{0.68\mu H \times (3 \times 10\mu F) \times (4\Omega + 0.005\Omega)}} = 118.36kHz$$

$$Q = \frac{\sqrt{0.68 \mu H \times (3 \times 10 \mu F) \times ((1 - 0.467)^2 \times 4 \Omega + 0.0068 \Omega) \times (4 \Omega + 0.005 \Omega)}}{(3 \times 10 \mu F) \times (0.0068 \Omega \times 4 \Omega + 0.0068 \Omega \times 0.005 \Omega + 4 \Omega \times 0.005 \Omega \times (1 - 0.467)^2) + 0.68 \mu H} = 5.799$$

$$R_1 \ = \ 0.0038\Omega + 0.003\Omega \ = \ 0.0068\Omega$$

$$F_{\rm m} = \frac{1}{0.8 \text{V}} = \frac{1.25}{\text{V}}$$

$$R_i = 144 k\Omega \times 0.003\Omega \times 91.25 \mu S = 0.039\Omega$$

Using the calculated values, simplify the uncompensated loop gain transfer function.

$$\begin{aligned} T_{uncompensated}(s) = \ 0.067 \times \frac{G_{vd}(s) \times (s \times 0.68 \mu H + 0.0068 \Omega)}{\frac{1.25}{V} + 12 V \times 0.039 \Omega - G_{vd}(s) \times (1 - 0.467) \times 0.039 \Omega} \end{aligned}$$

Select the required crossover frequency.

$$f_c = min\left(\frac{2.2MHz}{10}, \frac{1}{5} \times \frac{\omega_{z2}}{2\pi}\right) = 52.941kHz$$

$$\omega_{_{\boldsymbol{C}}} = 2 \times \pi \times 52.941 \text{kHz} = 332.641 \text{kHz}$$

Plot the derived uncompensated loop gain transfer function to estimate the gain and phase at the crossover frequency.

$$G_{fc} = -21.88$$

$$\varphi_{fc} = -114^{\circ}$$

$$\phi_{PM\ fc} = 180^{\circ} - 114^{\circ} = 66^{\circ}$$

$$\phi_{\text{comp target}} = 60^{\circ} - 66^{\circ} = -6^{\circ}$$

$$\phi_{\mbox{boost}} = \, 90^{\circ} - 6^{\circ} \, = \, 84^{\circ}$$

$$f_p = \left( tan \left( 84^\circ \times \frac{\pi}{180} \right) + \sqrt{tan \left( 84^\circ \times \frac{\pi}{180} \right)^2 + 1} \right) \times 220 \text{kHz} = 1.01 \text{MHz}$$

$$f_{z,ESR} = \frac{1}{2\pi \times 0.005 \Omega \times (3 \times 10 \mu F)} = 1.061 MHz$$

$$f_z = \frac{52.941 \text{kHz}^2}{1.01 \text{MHz}} = 2.775 \text{kHz}$$

Use the uncompensated loop gain G<sub>fc</sub> to calculate the compensation network components.

$$G_{comp} = 10^{\left(\frac{-21.88}{20}\right)} = 12.417$$

$$R_{comp} = \frac{12.417}{1.7mS} = 7.304k\Omega$$

$$C_{z} = \frac{1}{2\pi \times 7.304k\Omega \times 2.775kHz} = 7.854nF$$

$$C_{p} = \frac{1}{2\pi \times 7.304k\Omega \times 1.01MHz} = 21.571pF$$

The calculated component values are theoretical and serve as a starting point. Actual performance can vary depending on various factors such as board layout and parasitics. Further tuning on the actual board can be necessary to meet design targets.

If the phase margin is lower than the target, consider either increasing C<sub>7</sub> or decreasing C<sub>n</sub> to improve stability.

### 6.3 Recommended PCB Layout

Correct PCB layout is critical for proper operation of the RAA271041. Each channel requires specific attention to minimize the power loop area for highly efficient, stable operation. It is also important to consider routing the shared common areas between the two channels. Route the primary paths in a single layer copper if possible to reduce parasitic inductance in the power current paths.

The following layout instructions see Figure 24 and Figure 25 as noted.

- In Figure 24, connect the common connection between input capacitors, output capacitors, and the low-side FET for each channel through the central ground (gray) area.
- When the high-side MOSFET is switched ON and OFF the power current alternates flowing through the input capacitor and high-side MOSFET, or the low-side MOSFET. Minimize the loop area between CIN, high-side MOSFET, and low-side MOSFET to reduce interference from the high di/dt intervals as the current alternates between the MOSFETs.
- The first inner layer below the top copper layer with power components should be a ground layer that is as complete as possible, as indicated in Figure 25 using the light green fill. This provides a tightly coupled ground return path for the power circuitry. This layer is also used in conjunction with many vias to create a low-impedance connection from the common power GND region to the RAA271041 controller, and the thermal pad is connected to this plane using multiple vias.
- Connect the signal ground (Pin 14) to the thermal pad ground directly under the IC. For best noise immunity, signal pins such as COMP, RT, and configuration resistors can be connected in a small SGND pour that connects to Pin 14, which connects to PGND in a single point connection under the IC.
- Each channel has ISNS connections that should be routed as shown in Figure 25. The ISNS traces are routed
  on the second inner layer, which is shielded from power switching currents by the ground area on the inner
  layer 1. Begin the ISNS traces as a kelvin connection through a via in the center of the sense resistor in each
  channel.
- Minimize the trace lengths on the feedback loop and route around switching power circuits to minimize noise pick-up.
- Place the capacitors on VIN and VCC close to respective pins and ground connection.



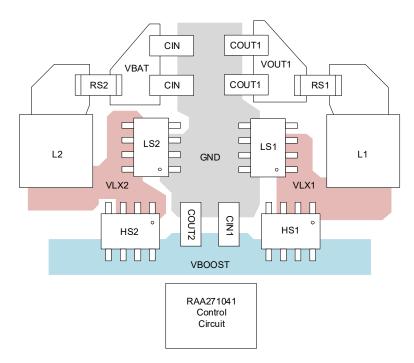


Figure 24. PCB Layout Illustrating Power Component Placement

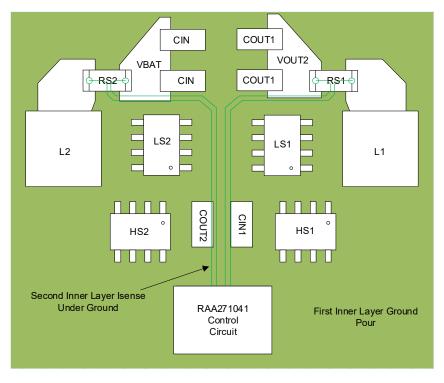


Figure 25. PCB Layout Illustrating Current Sense Routing

## 7. Package Outline Drawing

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

## 8. Ordering Information

Part Number <sup>[1][2]</sup>	Part Marking	Package Description <sup>[3]</sup> (RoHS Compliant)	Pkg. Dwg.#	Carrier Type <sup>[4]</sup>	Temperature Range	
RAA2710414081HNP#AA0	271041	36 Ld 6x6 QFN	L36.6x6D	Tray	-40 to +125°C	
RAA2710414081HNP#HA0	081HNP	30 Ed 0x0 Q1 N	LSO.OXOD	Reel, 4k	-40 to 1 123 C	
RTKA271041E00000BU	RAA271041 Evaluation Board					

These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin
plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free
products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.

Table 4. Key Differences Between Family of Parts

Part #	Channel 1	Channel 2	Channel 1 Output Range	Channel 2 Output Range
RAA271041	Buck	Boost	3.3V, 5V, 0.8V to 12V Adjustable	5V to 40V Adjustable
RAA271040	Buck	Buck	3.3V, 5V, 0.8V to 12V Adjustable	0.8V to 32V Adjustable

<sup>2.</sup> For Moisture Sensitivity Level (MSL), see the RAA271041 device page. For more information about MSL see TB363.

<sup>3.</sup> For the Pb-Free Reflow Profile, see TB493.

<sup>4.</sup> See TB347 for details about reel specifications.

# 9. Revision History

Revision	Date	Description
1.03	Oct 24, 2025	Updated the Feature for FET drivers support source/sink current Updated the typical application schematics, figures 1, 2, and 3. Updated the block diagram, figure 4, by moving Boot Refresh. In the Electrical Specification:  - Updated the unit for parameters: "Internal Switching Range - Low" and "External Switching Frequency" from MHz to kHz.  - Renamed "Forward CH1 Cycle-by-Cycle Current Limit" and updated Test Conditions.  - Renamed "Forward CH1 Hiccup Current Limit" and updated Test Conditions.  - Renamed "Negative CH1 Current Limit (NOC)" and updated Test Conditions.  - Renamed "CH1 Buck Error Amp (OTA) GM" and updated the Symbol.  - Renamed "Boost Error Amp (OTA) GM" and updated the Symbol.  - Renamed "Forward CH2 Cycle-by-Cycle Current Limit" and updated Test Conditions.  - Renamed "Forward CH2 Hiccup Current Limit" and updated Test Conditions.  - Renamed "Negative CH2 Current Limit (NOC)" and updated Test Conditions.  - Renamed "Boost Error Amp (OTA) GM" and updated the Symbol.  Updated the Functional Description by correcting "V <sub>IN</sub> range" to "VBAT supply range".  Updated WAKE1 and WAKE2 Operation by correcting "V <sub>IN</sub> " to "VBAT".  In section 5, minor updates to the following sections: Updated Phase Shift and Spread Spectrum, Fail-Safe Output (FSOb), Fault Protection Overview, Output Voltage Selection, Boost Operation Options, and SYNC Pin.  Added to section 5, Customer Options Table of Selections in OTP Creator.  Updated Gontrol Loop Compensation Components for the Buck Channel and added Parameter Definitions, Steps to Calculate Compensation Components, and Design Example.  Updated Control Loop Compensation Components for the Boost Channel and added Parameter Definitions, Steps to Calculate Compensation Components, and Design Example.  Updated all part numbers in the Ordering Information.
1.02	May 27, 2025	Corrected Ordering Information table.
1.01	May 20, 2025	Added Note to Abs max section.  Updated Figures 11, 20, and 21.  Fixed labels for Figures 11 to 22.  Removed typical spec for Low (Min) VIN LDO Reset.  Updated Min/Max spec for FB2 Pin Voltage Regulation, changed from 0.788 to -1.5% and 0.812 to +1.5%.  Updated min spec for Channel 2 Boost input from 2.1V to 2.2V throughout document.  Minor text updates to the following sections:  Output Voltage Selection  Current Limit and Overcurrent Protection  Current Limit and Overcurrent Protection (OC1 and OC2)  Ordering Information  Added ECAD Information.
1.00	Dec 16, 2024	Initial release.

# A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

# A.1 Part Number Indexing

Orderable Part Number Number of Pins		Package Type	Package Code/POD Number	
RAA2710414081HNP#AA0	36	QFN	L36.6x6D	
RAA2710414081HNP#HA0	36	QFN	L36.6x6D	

## A.2 Symbol Pin Information

### A.2.1 36-QFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	FB2S	Input	-
2	FB2	Input	-
3	WAKE2	Input	-
4	FB1	Input	-
5	FB1S	Input	-
6	RESV	Passive	-
7	COMP1	Output	-
8	RESV	Passive	-
9	COMP2	Output	-
10	FSOb	Output	-
11	FLT2b	Output	-
12	FLT1b	Output	-
13	EXT_EN	Output	-
14	SGND	Power	-
15	ISEN1N	Input	-
16	ISEN1P	Input	-
17	NC	Passive	-
18	BOOT1	Power	-
19	HS1	Output	-
20	LX1	Input	-
21	LS1	Output	-
22	VCC	Power	-
23	EXTSUP	Power	-
24	PGND	Power	-
25	LS2	Output	-
26	LX2	Input	-
27	HS2	Output	-
28	BOOT2	Power	-
29	VIN	Power	-
30	ISEN2N	Input	-
31	ISEN2P	Input	-
32	WAKE1	Input	-
33	TERM	Output	-
34	VBATS	Input	-
35	SGND	Power	-
36	SYNC	Input	-
EPAD37	GND	Power	-

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# A.3 Symbol Parameters

Orderable Part Number	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	RoHS	Output Type	Max Output Frequency
RAA2710414081HNP#AA0	Automotive	SMD	-40 °C	+125 °C	2.2 V	42 V	Compliant	Channel 1 Buck, Channel 2 Boost	2.2 MHz
RAA2710414081HNP#HA0	Automotive	SMD	-40 °C	+125 °C	2.2 V	42 V	Compliant	Channel 1 Buck, Channel 2 Boost	2.2 MHz

# A.4 Footprint Design Information

### A.4.1 36-QFN

IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFN	L36.6x6D	36

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	5.95	PitchE
Maximum body span (vertical side)	Dmax	6.05	→  ← n-1 n
Minimum body span (horizontal side)	Emin	5.95	1 <u> </u>
Maximum body span (horizontal side)	Emax	6.05	
Minimum Lead Width	Bmin	0.20	PitchD CH 2
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	T D2 D
Maximum Lead Length	Lmax	0.65	<u> </u>
Number of pins (vertical side)	PinCountD	9	B
Number of pins (horizontal side)	PinCountE	9	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.50	F2 F2
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.50	E———► Bottom View
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side (center).	Pin1	S2	- Bollotti view
Thermal pad Chamfer. If not present give hyphen (-).	CH	0.35	
Minimum thermal pad size (vertical side)	D2min	4.0	
Maximum thermal pad size (vertical side)	D2max	4.2	
Minimum thermal pad size (horizontal side)	E2min	4.0	
Maximum thermal pad size (horizontal side)	E2max	4.2	
Maximum Height	Amax	0.90	
Minimum Standoff Height	A1min	0	]
Minimum Lead Thickness	cmin	0.15	Amax
Maximum Lead Thickness	cmax	0.25	↑ A1min - ↑ ↑ Side View

Recommended Land Pattern					
Description	Dimension	Value (mm)	Diagram		
Distance between left pad toe to right pad toe (horizontal side)	ZE	6.4			
Distance between top pad toe to bottom pad toe (vertical side)	ZD	6.4	GE—→ı Package		
Distance between left pad heel to right pad heel (horizontal side)	GE	4.9	n n-1 Outline		
Distance between top pad heel to bottom pad heel (vertical side)	GD	4.9			
Pad Width	X	0.50	2		
Pad Length	Y	0.75	ZD GD P P P P P P P P P P P P P P P P P P		

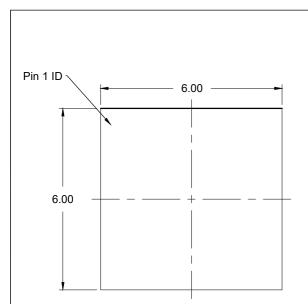
# **Package Outline Drawing**

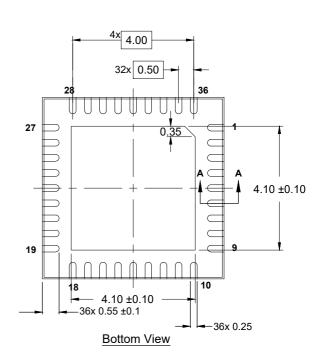


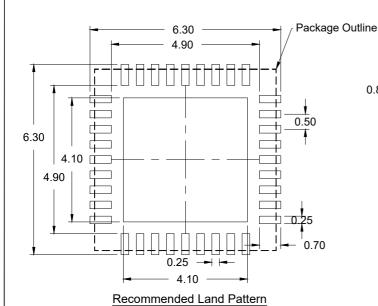
L36.6x6D SQ0036AA

36 Lead Step Cut Quad Flat N0-Lead Plastic Package (SCQFN)

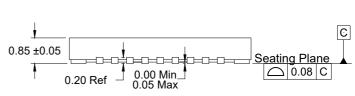
Rev.01, Aug 29, 2025



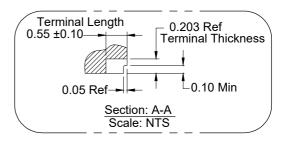




Top View



### Side View



### Notes:

- 1. JEDEC compatible.
- 2. All dimensions are in mm and angles are in degrees.
- 3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
- 4. Numbers in ( ) are for references only.

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