RAA2P3200

Single Coil high-speed Inductive Position Sensor IC with SPI, UART, ABI Step/Direction and UVW Interfaces

RAA2P3200 is a high-speed magnet-free, inductive position sensor IC that can be used for high-speed absolute and incremental position sensing in industrial, medical, and consumer applications. It operates on the principle of eddy currents to detect the position of a simple metallic target that is moving above a set of coils, comprising one transmitter coil and two receiver coils.

These coils are typically copper traces on a printed circuit board (PCB). The transmitter coil induces a secondary voltage in the receiver coils, which varies depending on the position of the metallic target above them.

A signal representative of the target's position relative to the coils is calculated by demodulating and processing the secondary voltages from the receiver coils. The target can be made of various metals, including aluminum, steel, or a PCB with a printed copper layer.

The RAA2P3200 is equipped with:

- 14-bit SPI interface
- 14-bit High-speed UART interface (up to 2Mbit/s)
- 12/14-bit Incremental interfaces ABI and Step/Direction
- UVW interface
- AB (Step/Direction) 12/14-bit + PWM Output

The device operates at rotation speeds up to 600 000rpm (electrical). An ultra-low propagation delay of less than 100 ns provides high dynamic control for fast spinning motors.

Available Support

Renesas provides application modules that demonstrate RAA2P3200 rotary position sensing applications.

Typical Applications

Rotor position detection for brushless DC motors with digital interfaces, adaptable to any pole pair count, rotary and linear encoders.

Features

- Cost-effective; no magnet required
- Immune to magnetic stray fields; no shielding required
- Suitable for harsh environments and high temperatures
- True-power-on position information, obtained by digital interfaces (SafeSPI, UART), PWM or with ABI with fast incremental start-up burst
- Programmable through UART interface and SafeSPI protocols
- Nonvolatile memory enables multiple programming options
- Single IC supports on-axis and off-axis rotation, linear motion, and arc motion sensing
- Adaptable to any full-scale angle range through coil design
- High accuracy: ≤ 0.1% full scale (with ideal coils), enabling sensor solutions up to 11-bit electrical accuracy
- Overvoltage and reverse polarity protection: ±18V on both supply and output pins
- Supply voltage programmable for 3.3V ±0.3V or 5.0V±0.5V
- Qualified for industrial application use from -40°C to +125°C ambient temperature
- 48 bits nonvolatile user ID memory space
- Small 16-TSSOP package (4.4mm ×5.0mm)

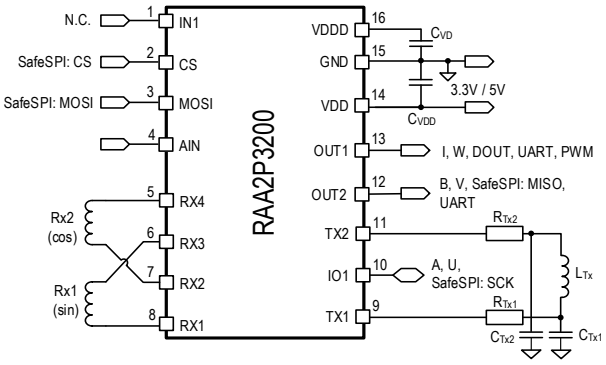

Figure 1: Application Circuit Example

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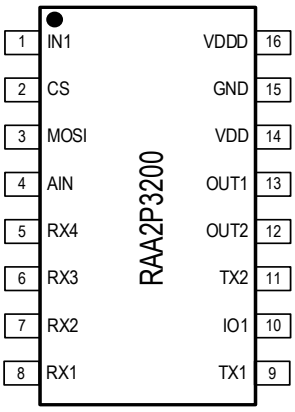


Figure 2. RAA2P3200 pinout

Table 1. Pin Description, RAA2P3200

Pin Number	Name	Type	Description
1	IN1	Digital Input	SPI: not used Incremental/UVW: not used UART: not used
2	CS		SPI: CS chip select input (active low) Incremental/UVW: Not used UART: Optional address pin strapping input ADR0
3	MOSI		SPI: MOSI data input Incremental/UVW: not used UART: Optional address pin strapping input ADR1
4	AIN	Analog Input	Auxiliary analog (12-bit) input for external analog signal, readable over SPI and UART interface
5	RX4	Sensor Input	Receiver coil (COS_N)
6	RX3		Receiver coil (SIN_N)
7	RX2		Receiver coil (COS)
8	RX1		Receiver coil (SIN)
9	TX1	Transmitter Output	Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND.
10	IO1	Digital I/O	SPI: SCK clock input Incremental/UVW: A, Step, U UART: not used
11	TX2	Transmitter Output	See description of pin #9 (TX1)
12	OUT2	Digital Output	SPI: MISO output Incremental/UVW: B, Direction, V UART: TxD
13	OUT1	Digital I/O	SPI: Digital output Incremental/UVW: Index, W, PWM UART: Bi-directional TxD/ RxD Single Wire programming interface
14	VDD	Supply	External supply voltage (3.3V or 5V).
15	GND	Supply	Common ground connection.
16	VDDD	Supply	Internally regulated digital supply voltage.

2. Specification

2.1 Absolute Maximum Ratings

The absolute maximum ratings listed in Table 2 are stress ratings only. Exceeding these limits can cause permanent damage to the device. The functional operation of the RAA2P3200 at these maximum ratings is not guaranteed. Exposure to the absolute maximum rating conditions could impact device's reliability. All voltage levels are referenced to GND.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{VDDmax}	External supply voltage: VDD	Continuous	-18	18	V
V_{IO1}	Digital input pin voltage				
V_{OUT2}	Digital I/O pin voltage				
V_{OUT1}	Analog/Digital output pin voltage				
V_{RX1}	Sensor Receiver coil input pin voltage (RX1)	Continuous	-12	12	V
V_{RX2}	Sensor Receiver coil input pin voltage (RX2)				
V_{RX3}	Sensor Receiver coil input pin voltage (RX3)				
V_{RX4}	Sensor Receiver coil input pin voltage (RX4)				
V_{DIN}	Digital input pin voltage				
V_{ADR0}	Digital input pin voltage				
V_{ADR1}	Digital input pin voltage				
V_{AIN}	Analog input pin voltage				
V_{Tx1}	Transmitter output pin (TX1) voltage	Continuous	-0.3	5.5	V
V_{Tx2}	Transmitter output pin (TX2) voltage				
$V_{VDDDmax}$	Internal digital supply voltage, VDDD	VDDD is internally regulated with an external capacitor to GND. No other connection to external voltages.	-0.3	2.0	V
T_{AMB}	Ambient temperature		-40	125	ºC
T_J	Junction temperature		-40	135	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125°C to prevent pre-aging	-55	160	ºC
R_{THJA}	Thermal resistance junction to ambient: 16-TSSOP package	Velocity = 0m/s with 2s2p PCB test board (JEDEC 51-2, JEDEC 51-7)		89.5	K/W
R_{THJC}	Thermal resistance junction to case: 16-TSSOP package	Junction to top of package		38.38	K/W

2.2 ESD Ratings

Table 3. ESD Ratings

Symbol	Parameter	Conditions	Maximum	Units
V_{ESD}	ESD tolerance for all pins Human Body Model: 100pF/1.5kΩ	According to JEDEC JS-001, classification 2	±2	kV
V_{CDM}	ESD tolerance for all pins: Charged-Device Model (CDM)	According to JEDEC JS-001, classification C2b	±750	V

2.3 Operating Conditions

All minimum/maximum specification limits are guaranteed by design, production testing, and/or statistical characterization. Conditions: T_{AMB} = -40°C to 125°C unless otherwise specified. C_{VDD} = 470nF, C_{VDDD} = 100nF.

Typical values are based on characterization results at default measurement conditions and are informative only.

Table 4. Electrical Characteristics, 5V and 3.3V Modes

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{VDD5}	Supply voltage, 5V mode		4.5	5.0	5.5	V
$V5_{UV}$	Undervoltage detection level, 5V mode	An undervoltage alarm is created if VDD falls below this limit	3.95	4.1	4.45	V
$V5_{OV}$	Overvoltage detection level, 5V mode	An overvoltage alarm is created if VDD rises above this limit	5.55	6.15	6.5	V
V_{VDD3}	Supply voltage, 3.3V mode		3.0	3.3	3.6	V
$V3_{UV}$	Undervoltage detection level, 3.3V mode	An undervoltage alarm is created if VDD falls below this limit	2.7	2.8	2.98	V
$V3_{OV}$	Overvoltage detection level, 3.3V mode	An overvoltage alarm is created if VDD rises above this limit	3.65	3.85	4.04	V
$V_{VDD\_TH\_H}$	Power-on reset (POR), high threshold	Power-on reset (POR): the device is activated when VDD increases above this threshold		2.61	2.7	V
$V_{VDD\_TH\_L}$	Power-on reset (POR), low threshold	The device is deactivated when VDD decreases below this threshold	2.3	2.38		V
$V_{VDD\ POR\_HYST}$	Power-on reset hysteresis		200	250	300	mV
$t_{stup\ PE}$	Start-up times	Power-on reset (POR) to valid output signal, programming enabled			5	ms
$t_{stup\ PL}$		Power-on reset (POR) to valid output signal, programming locked			3	ms
$t_{stup\ cmd}$	Command timeout time	Time to wait before sending first command	1.5			ms
t_{ProgEn}	Programming window enable time	Timeout window after POR, in which a first programming enable command must be sent			5	ms
t_{ProgUL}	Programming window unlock time	Timeout window after programming enable in which a second unlock command must be completely sent[i]			75	ms

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{VDDD}	Digital supply voltage	Internally regulated. Connect capacitor C_{VDDD} = 100nF from VDDD to GND.	1.75	1.8	1.85	V
I_{AUXIN}	Auxiliary Input on VDDD maximum external load current	VDDD must be connected to a capacitor C_{VDDD}.	0		4	mA
$I_{SHORT\ VDDD}$	VDDD short circuit current limitation		18.5	27	40	mA
I_{CC}	Current consumption	Without coils, no load	10	15	20	mA
C_{VDDD}	Capacitor from VDDD pin to GND		100			nF
C_{VDD}	Capacitor from VDD pin to GND	Nominal value	100	470		nF

Table 5. Position Resolution and Update Rate

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
RES_{UART}	Position resolution UART interface			14		
RES_{SPI}	Resolution of calculated position over SafeSPI interface			14		bits
RES_{INC_BIN}	Position resolution incremental interfaces (ABI,Step/Direction)	Binary Mode Counts per 1 coil period (programmable)		512 1024 2048 4096		cpr
RES_{INC_DEC}		Decimal Mode Counts per 1 coil period (programmable)		500 1000 2000 4000		cpr
RES_{PWM}	Position resolution PWM interface		12		14	
Acc	Position accuracy SPI, UART, ABI (12-bit),Step/Dir (12-bit), UVW, PWM	Ambient temperature, nominal supply	-0.1		0.1	%FS
		Over temperature and supply range	-0.2		0.2	%FS
t_{POS}	Position refresh rate	Internal refresh rate of position information	2		3	µs

Table 6. Non-volatile Memory Parameters[i]

Parameter	Conditions	Minimum	Typical	Maximum	Units
Data retention	Qualified according to JEDEC 22-A117	15 @T_J = 100°C			Years
	Over product lifetime		>100 @T_J = 25°C		

[i] Guaranteed by memory supplier

Parameter	Conditions	Minimum	Typical	Maximum	Units
Write temperature	Allowed ambient temperature range for read and write access	-40		125	°C
Read temperature		-40		125	ºC
Endurance[ii]	Over product lifetime			1000	NVM Write Cycles
Read Cycles		5x 10^{11}	1x 10^{12}		NVM Read events

Table 7. LC Oscillator Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{LC}	Excitation frequency	LC oscillator frequency is determined by external components L and C.	2		5.5	MHz
R_{Peq}	Equivalent parallel resistance of the LC resonant circuit		250			Ω
V_{TX_PP}	LC oscillator amplitude at VDD = 5.0V ±10%	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. Adjustable by coil current.			8.8	Vpp
	LC oscillator amplitude at VDD = 3.3V ±10%				2* V_{VDD3}	
I_{LC}	Programmable transmitter coil drive current	$T_{ambient}$ = -40 to +160°C	0	[1]	16	mA
R_{Tx1}, R_{Tx2}	LC oscillator series resistors	Depending on coil design and excitation frequency (f_{LC})		10		Ω

[1] The required transmitter coil current is determined by the equivalent parallel resistance of the LC circuit, depending on coil design.

Table 8. Receiver Coils Front-End Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{RX}	RX coil amplitude	Differential coil input	5		200	mV_{pp}
A_{IN_mm}	Maximum amplitude mismatch correction	Programmable gain mismatch correction of RX coil signals (SIN and COS)			15	%
$A_{IN\_OFFS\_RANGE\%}$	Input offset correction range	Differential input offsets of sine or cosine signal, percentage of transmitter coil amplitude.	-0.2		0.2	%
D_{OFFSET}	Coil input offset temperature drift	Over temperature range T_{AMB}	-2.5		2.5	%
C_{RX1} to C_{RX8}	Receiver input filter capacitors	For improved EMC immunity		220		pF
$Noise_{SP}$	Signal path noise level	Digital filtering = OFF V_{RX}= 50mV			0.1	° el. rms
		Digital filtering = OFF V_{RX}= 5mV			0.5	° el. rms

[ii] Verified number of program/erase cycles. Qualified with 2000 cycles.

2.4 Interface Pin Characteristics

Table 9. UART Interface

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{OL_UART}	Output low voltage	3mA sink current, VDD = 3.0 to 5.5V OUT1 pin 13 OUT2 pin 12	0		0.4	V
V_{OH_UART}	Output high voltage	3mA source current, VDD = 3.0 to 5.5V OUT1 pin 13 OUT2 pin 12 (Push-Pull condition)	0.8 × VDD		VDD	V
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold	OUT2 pin 12	8			mA
$I_{OUT2\ sc\ lim}$	OUT2 output short current limitation[1]	OUT2 pin 12 Short to VDD, GND VDD = 3.0V to 5.5V Open Drain mode	14		26	mA
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold	OUT1 pin 13	35			mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation[2]	OUT1 pin 13 Short to VDD, GND VDD = 3.0 to 5.5V Push-pull mode	28			mA
$I_{OUT1\ sc\ lim}$	Output short current limitation[2]	OUT1 pin 13 Short to VDD, GND VDD = 3.0V to 5.5V Open Drain Mode	28		56	mA
V_{IL_UART}	OUT1 low level input voltage	VDD = 5V	-0.3		0.2 × VDD	V
		VDD = 3.3V	-0.3		0.3 × VDD	V
V_{IH_UART}	OUT1 high level input voltage	VDD = 5V	0.7 × VDD		VDD + 0.3	V
		VDD = 3.3V	0.7 × VDD		VDD + 0.3	V

[1] With OUT2 drive strength set to “00” and OUT2 drive strength for open drain disabled. (out2_io1_drv = “00”)

[2] With digital mode configuration (out1_drv=”10”)

Table 10. SPI Interface

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VOL	Output low voltage	3mA sink current VDD = 3.0V to 5.5V OUT2 pin 12	0		0.4	V
VOH	Output high voltage	3mA source current VDD = 3.0V to 5.5V OUT2 pin 12	0.8 × VDD		VDD	V
VOH_{SPI3}	Output high voltage	3mA source current VDD = 3.3V ±10% SafeSPI mode Pin OUT2	V_{VDD} - 0.4		V_{VDD}	V
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold	OUT2 pin 12	8			mA
$I_{OUT2\ sc\ lim}$	OUT2 output short current limitation[1]	OUT2 pin 12 Short to VDD, GND VDD = 3.0V to 5.5V	33		70	mA
t_{rf}	Output rising edge, push/pull mode. MISO (SafeSPI) pin	Load capacitance 60pF Output voltage rising from 10% to 90%, 5V			55	ns
t_{rf}	Output falling edge, push/pull mode. MISO (SafeSPI) pin	Load capacitance 60pF Output voltage falling from 90% to 10%, 5V			55	ns

Table 11. Incremental Interfaces

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{inc}	Single channel Pulse Rate	ABI Step/Direction interfaces			2	MHz
V_{OH_inc}	Output high voltage ABI - Step/Direction	3mA source current VDD = 3.0V to 5.5V Pin 13 (OUT1) Pin 12 (OUT2) Pin 10 (IO1)	0		0.4	V
V_{OL_inc}	Output low voltage ABI - Step/Direction	3mA sink current VDD = 3.0V to 5.5V Pin 13 (OUT1) Pin 12 (OUT2) Pin 10 (IO1)	0.8 × VDD		VDD	V
$I_{OUT2\ IO1\ lim\ thr}$	Current limitation threshold A,B or Step/Direction pins	Pin 12 (OUT2) Pin 10 (IO1) In overload condition	6			mA
$I_{OUT2\ IO1\ sc\ lim}$	Output short current limitation [1] A,B or Step/Direction pins	Pin 12 (OUT2) Pin 10 (IO1) Short to VDD, GND VDD = 3.3V to 5V	32		70	mA
$I_{OUT1\ lim\ thr}$	Current limitation threshold [1] Index pin	Pin 13 (OUT1) In overload condition	35			mA

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
$I_{OUT1\ sc\ lim}$	Output short current limitation [1] Index pin	Pin 13 (OUT1) Short to VDD, GND VDD = 3.3V to 5V	28		58	mA
t_{r_local}	Output rising edge embedded applications	Load capacitance 60pF Output voltage rising from 10% to 90% VDD = 3.0 to 5.5V			55	ns
$t_{f\ local}$	Output falling edge, embedded applications	Load capacitance 60pF Output voltage falling from 90% to 10% VDD = 3.0V to 5.5V			55	ns
$t_{r\ remote}$	Output rising edge remote applications	Load capacitance 4.7nF Output voltage rising from 10% to 90% VDD = 3.0V to 5.5V			4	us
$t_{f\ remote}$	Output falling edge remote applications	Load capacitance 4.7nF Output voltage falling from 90% to 10% VDD = 3.0V to 5.5V			4	us

[1] With digital mode configuration (out1_drv="10").

[2] With OUT2 fast configuration (out2_io1_drv="11")

Table 12. PWM Interface

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
$I_{IO1\ lim\_thr\ PWM}$	IO1 current limitation threshold	Pin 10 (IO1) In overload condition	6			mA
$I_{IO1\ sc\ lim\ PWM}$	IO1 Output short current limitation[2]	Pin 10 (IO1) Short to VDD, GND VDD = 3.3V to 5V	32		70	mA
DC_{PWM}	PWM duty cycle	Normal operation	5.56		94.44	%
DC_{PWM_DHI}	PWM duty cycle	Diagnostic low mode		2.78		%
DC_{PWM_DLO}	PWM duty cycle	Diagnostic high mode		97.24		%
ft_{PWM}	PWM frequency tolerance		-5		5	%
t_{PWM_r}	PWM output rising edge, push-pull mode.	Load capacitance 4.7nF Output voltage rising from 10% to 90% @ 5V			5	us
t_{PWM_f}	PWM output falling edge, push-pull mode	Load capacitance 4.7nF Output voltage falling from 90% to 10% @ 5V			5	us

[1] With digital mode configuration (out1_drv= "10").

[2] With OUT2 fast configuration (out2_io1_drv="11")

3. Detailed Description

3.1 Overview

The RAA2P3200 sensor IC consists of one transmitter coil and one pair of receiver coils, which are typically designed as traces on a printed circuit board. The receiver coils are designed as two wire loops with anti-serial connection. The “sine” coil and the “cosine” coil are shifted by 90 electrical degrees. A metal target is placed above the coil arrangement.

When the IC drives an AC current into the transmitter coil, it generates an alternating magnetic field. This magnetic field induces secondary voltages in the receiver coils. Without a target, the induced voltages in the loops of the receiver coils cancel each other out, resulting in a net receiver voltage of zero.

When a metal target is placed above the coils, the magnetic field generates eddy currents on its surface. These eddy currents create a counter magnetic field, reducing the total flux density underneath. This leads to a reduction in the voltage induced in the receiver coil areas underneath the target, creating an imbalance in the anti-serial coil segment voltages.

The IC demodulates, offsets and corrects the amplitude of the signals from the two receiver coils with a 90° electrical phase shift design, which generates sine and cosine shaped voltages as the target is moving.

The RAA2P3200 IC amplifies, rectifies, and filters the receiver voltages, converting them into digital representation with an ADC. The digital sine and cosine signals are converted into a 0°to 360° absolute position. The signal accuracy can be further enhanced through a 2-dimentional,16-point linearization process.

The position can be read over SPI, UART, or Incremental interfaces: ABI, Step/Direction, UVW.

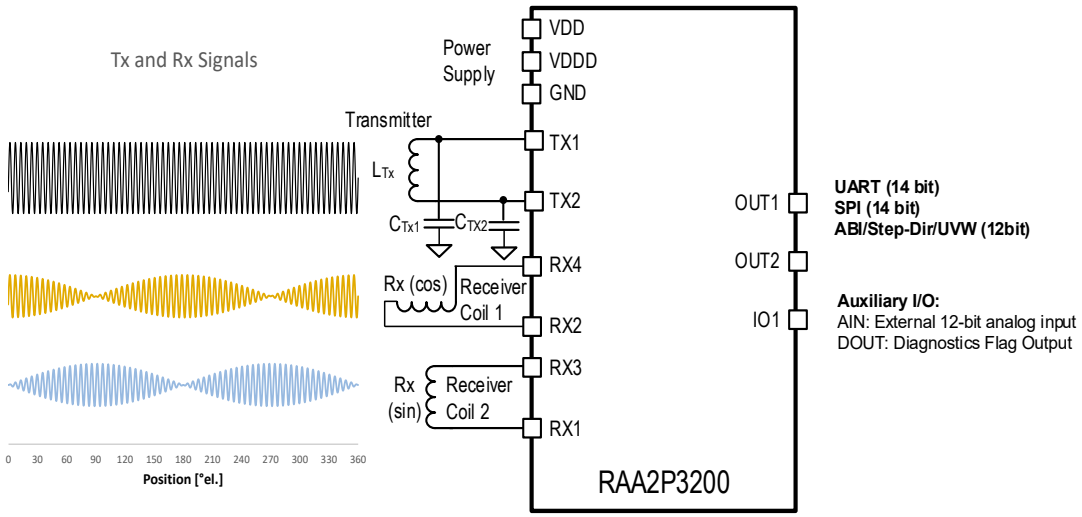


Figure 3. RAA2P3200 Input/Output Signals

3.2 Block Diagram

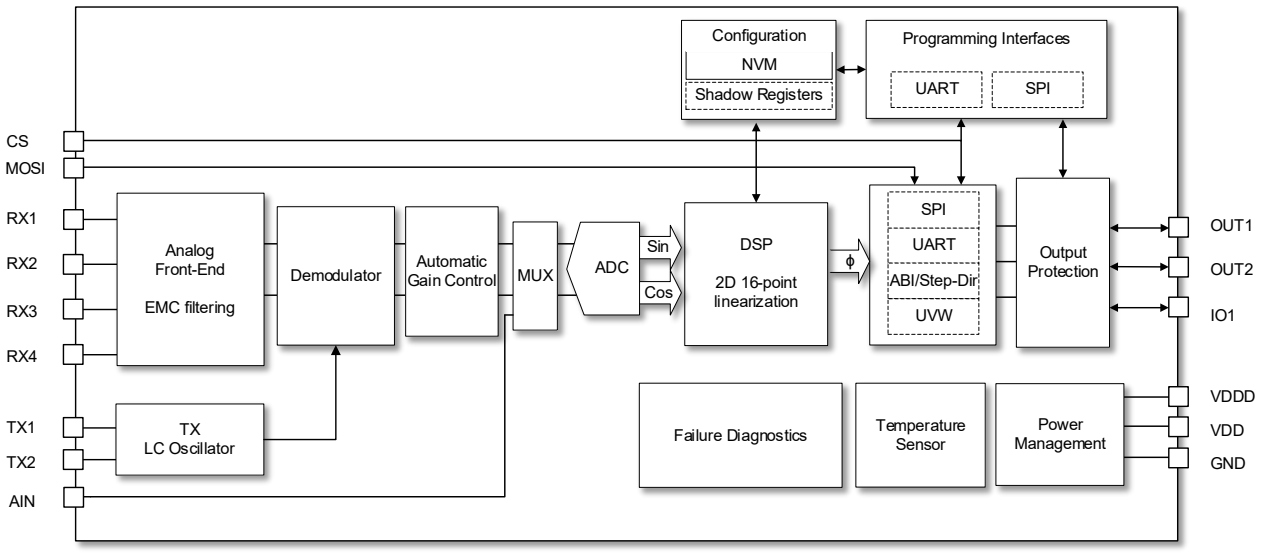


Figure 4. Block Diagram

The main building blocks include:

- Analog front-end: Input filter, offset, and gain control for the receiver signals.
- Demodulator: Converting RF modulated position signal to LF demodulated raw sine and cosine signals.
- Automatic Gain Control: Automatically adjusts the raw sine and cosine signal levels.
- High Speed ADC: Converts raw signals into digital format for further digital signal processing.
- Digital signal processing: Converts digital sine and cosine raw signals into synchronized absolute position information for both channels.
- 2D 16-point linearization: Supports up to 16 two-dimensional linearization points with freely programmable X- and Y- coordinates for each point (X= Position input, Y= Position output).
- SPI, UART, INC, PWM: Carries out post processing, clamping, signal integrity checks. Decodes channel information and other diagnostics info into the selected output format (SPI, UART, Incremental).
- TX Oscillator: Generates the transmitter coil signal.
- Temperature sensor: Internal temperature sensor, used for chip diagnostics.
- Protection: All outputs are fully protected against overvoltage, reverse polarity and short circuit, enabling direct cable connection to these outputs, and eliminating the need for additional line driver ICs.
- Power Management: Operates with supply voltages ranging from 3.0V to 5.5V. External capacitors are required for the supply voltage VDD, and for the digital power supply, VDDD. All other supplies, such as analog circuits, do not need any external capacitor.
- Programming interface: Accessible via one-wire UART or SPI interface.
- Configuration, NVM: Stores nonvolatile, storage of factory and user-programmable settings. User configuration parameters can be programmed multiple times.
- On-chip failure diagnostics: Performs internal diagnosis of critical blocks.
- Auxiliary I/O include, AIN (12-bit analog input for external analog signals), DOUT (Diagnostic Output) accessible over serial interfaces.

3.3 LC Oscillator

The transmitter circuit of the RAA2P3200 generates the required RF magnetic field for operating the sensor as determined by an external parallel LC circuit, see Figure 5. To ensure low emission of harmonics, the capacitive part of the LC circuit is split into two equal-value capacitors: CTx1 and CTx2. Additionally, two series resistors RTx1 and RTx2 are added as shown in Figure 5.

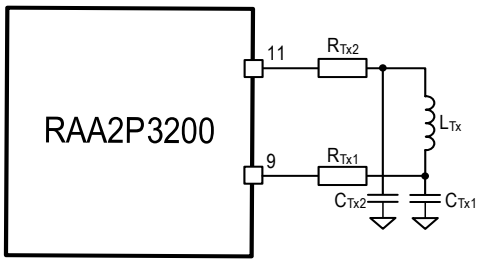


Figure 5. TX LC Oscillator

3.3.1 Parallel LC Resonator Calculations

A resonator, comprising an inductor (L) and a capacitor (C) in parallel, is essential for generating specific frequencies in RF applications. Accurate calculations of the equivalent parallel resistance (R-Peq) ensure proper resonator function. In the RAA2P3200 transmitter circuit, this resonator minimizes harmonic emissions.

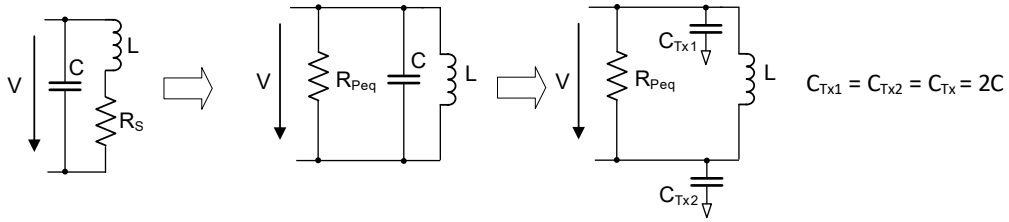


Figure 6. Parallel Resonator Circuit

Equivalent parallel resistance from Coil series resistance:

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C}$$ **Equation 1**

For $C_{Tx1} = C_{Tx2} = C_{Tx} = 2C$:

$$R_{Peq} = \frac{1}{R_S} \times \frac{2 \times L}{C_{Tx}}$$ **Equation 2**

Equivalent parallel resistance from Quality factor Q:

$$R_{Peq} = Q \times \sqrt{\frac{L}{C}} = Q \times \sqrt{\frac{2L}{C_{Tx}}}$$ **Equation 3**

Ideal LC Oscillator frequency with split Tx capacitors C_{Tx}

$$f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{Tx}}{2}}}$$ **Equation 4**

Oscillator frequency with split Tx capacitor C_{Tx} and coil series resistor R_s

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{R_S}{L}\right)^2}$$ **Equation 5**

Oscillator frequency with split Tx capacitor C_{Tx} and equivalent parallel resistor R_{Peq}

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{2}{R_{Peq}C_{Tx}}\right)^2}$$ **Equation 6**

$$Q = R_{Peq}\sqrt{\frac{C}{L}} = \frac{1}{R_S}\sqrt{\frac{L}{C}}$$ **Equation 7**

Coil quality factor

$$Q = \omega\frac{L}{R_S} = 2\pi f_{TX}\frac{L}{R_S}$$ **Equation 8**

Where:

R_{Peq}	Equivalent parallel resistance of the LC circuit at the transmitter frequency in Ohms
R_S	Serial resistance of the transmitter coil at the transmitter frequency in Ohms
f_{Tx}	Resonant circuit frequency in Hertz, 1/s
L	Resonant circuit coil impedance in Henry
C	Resonant circuit capacitance in Farad
C_{Tx1}, C_{Tx2}	Capacitance of the split capacitors in Farad
Q	Resonant circuit quality factor (unitless)
ω	Angular frequency 2*π*f_{Tx} in Hertz, 1/s

3.4 Coil Design

Figure 7 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$V_{Cos\ Loop1} = -V_{Cos\ Loop2}$ **Equation 9**

In the absence of a target, the secondary voltages balance out as follows:

$V_{Cos} = V_{Cos\ Loop1} – V_{Cos\ Loop2} = 0V$ **Equation 10**

With a target placed above the coils, the secondary voltage induced in the covered area decreases compared to the secondary voltage when no target is present above it.

$V_{Cos\ Loop1} \neq -V_{Cos\ Loop2}$ **Equation 11**

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage ≠ 0V is generated, depending on the location of the target.

$V_{Cos} = V_{Cos\ Loop1} – V_{Cos\ Loop2} \neq 0V$ **Equation 12**

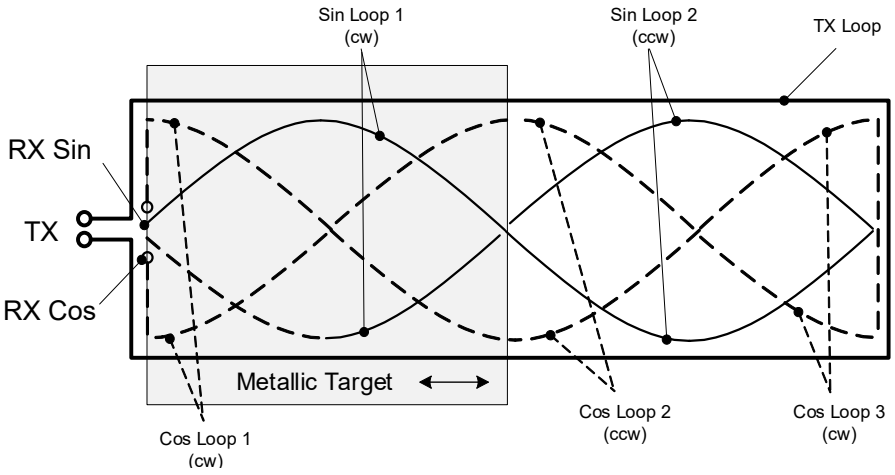


Figure 7. Coil Design for a Linear Motion Sensor

The same principles shown for the linear motion sensor can be applied to a rotary sensor as shown in Figure 8.

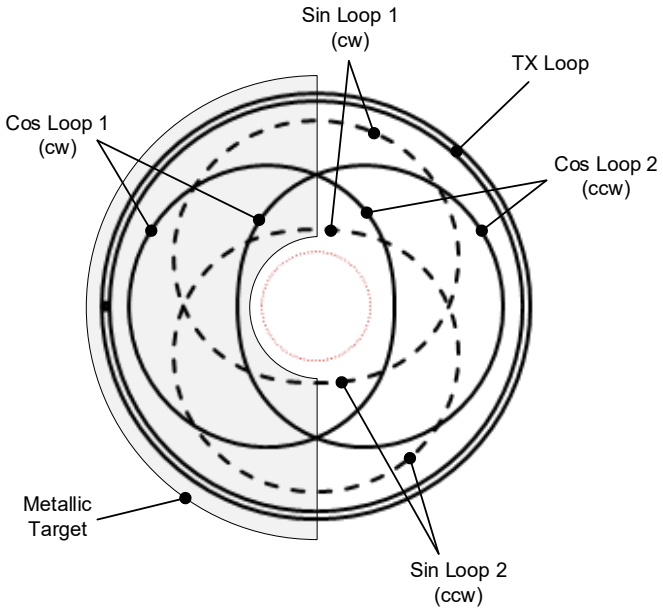


Figure 8. Coil Design for a 360° Rotary Sensor

3.4.1 Multi-periodic Coil Design Application Examples

Applying the same fundamental design principles, coils with multiple periods per turn can be designed. Multi-periodic designs improve mechanical accuracy compared to single-periodic coil designs. For example, a 4-periodic coil design (4 × 90°) improves mechanical accuracy by a factor of 4. Consequently, for angular designs, requiring < 360° movement range, coil designs with multiple periods are recommended. these designs not only improve mechanical accuracy but are also more robust against mechanical target misalignment and tilt.

3.4.2 Electrical versus Mechanical degrees

The RAA2P3200 converts the movement of a target across a single period of the receiver coil into a precise electrical signal. This conversion spans the full angular range from 0°to 360°, producing a digital output ranging from 0 to (2^N-1) LSBs. The position output is thus absolute over a full turn of 360 mechanical degrees.
As illustrated in Figure 9, the single-periodic coil design establishes a direct 1:1 relationship between electrical and mechanical domains as the following:

- Coil Period: 360° electrical
- Mechanical Range: 360° mechanical
- Conversion Factor: 1:1 (1°el. = 1° mechanical)

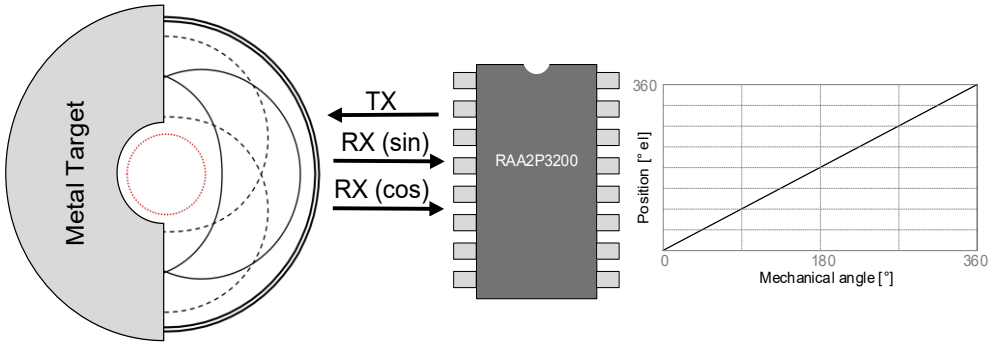


Figure 9. Coil Design Using 1-Periodic Coil

As illustrated in Figure 10, a coil design with four receiver coil periods within a single full mechanical turn, results in four electrical rotations for every complete mechanical turn and provides the following advantages in accuracy and resolution.

- Higher Resolution: Position output resolution increases proportionally with period count by

$$\text{Mechanical Resolution} = \text{Sensors\_Periods} * \text{Electrical Resolution}$$

  In this configuration one electrical degree (°el) equals 0.25 mechanical degrees (°). The provided output resolution is four times higher compared to the single-periodic design.

- Improved accuracy: Mechanical error is reduced by the period factor

$$Mechanical\ Error = \frac{Electrical\ Error}{Sensor\ Periods}$$

  This configuration is particularly well-suited for:

  - Multi-pole motors requiring precise commutation
  - Limited-range applications (<180° mechanical travel)
  - Systems demanding high-resolution incremental feedback

Select the number of periods based on application requirements to optimize measurement performance. Proper period selection is critical for achieving maximum system accuracy.

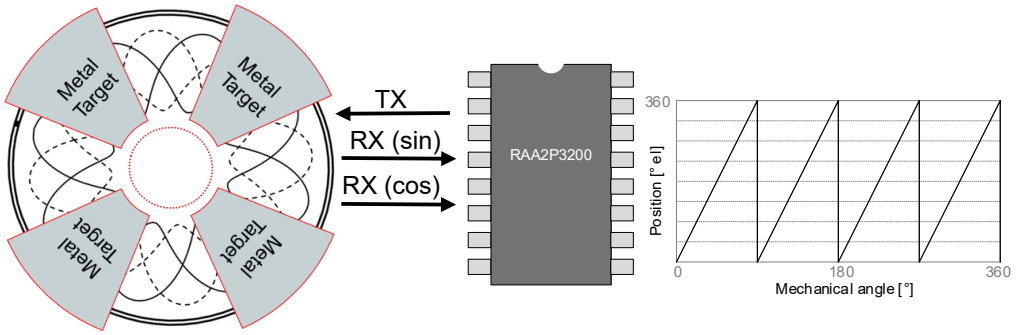


Figure 10. Coil Design Using 4-Periodic Coil

4. Linearization

The RAA2P3200 offers a very flexible linearization feature to enhance sensor accuracy. The linearization algorithm is applied digitally after an angle calculation. The linearization is performed with 12-bits resolution over a 360° electrical range (el.). Up to 16 programmable linearization points can be positioned within a grid of 0.088° in both X (position) and Y (expected output) directions.

Figure 11 illustrates an example of the impact of linearization, showing that the total error is significantly reduced.

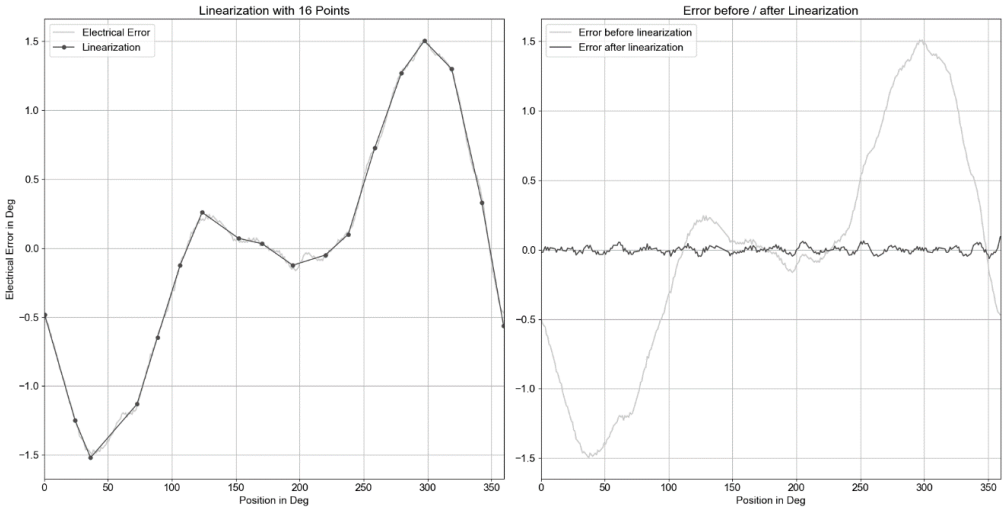


Figure 11. Example of 16-Point Linearization

Table 13. Linearization Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
N_{P_Lin}	Number of linearization points				16	
$Grid_{LIN}$	Placement grid of linearization points	In X and Y		0.088		°el
Res_{Lin}	Resolution of linearization transfer function	X and Y coordinates		12		bits

Note: The slope of each segment (ΔY / ΔX) is automatically calculated from the X and Y parameters of adjacent linearization points. If two adjacent points are positioned with a slope outside the specified range (see Table 13), the slope is reset to 0 to prevent an overflow of the calculated slope value.

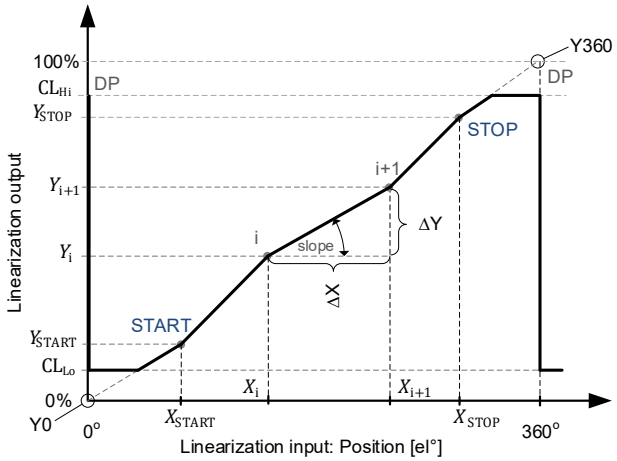


Figure 12. Linearization Transfer Function Parameters

Table 14. Linearization Parameter Settings

Parameter	Description	Programming Options	Resolution
P_{Lin}	Number of linearization options	0,2,4,6,8,16	
D_P	Discontinuity point, Zero position transition from 0°/360°	0° to <360° el.	0.088°el. per LSB
X_{Start}	Mechanical start position, first linearization point		
Y_{Start}	Expected output at XStart, first linearization point		
X_i	Mechanical position of linearization point (i = 1 to 16, including start and stop)		
Y_i	Expected output at linearization point (i = 1 to 16 including start and stop)		
X_{Stop}	Mechanical end position, last linearization point		
Y_{Stop}	Expected output at XStop, last linearization point		
CL_{Hi}	Output Clamping level, high	0% to 100% VDD	12 bits (VDD / 4096) per LSB
CL_{Lo}	Output Clamping level, low		
Y0	Position at DP, start value at X = 0°	0° / 360° el.	
Y360	Position at DP, stop value at X = 360°	0° / 360° el.	

5. Interfaces

The RAA2P3200 offers SafeSPI, UART, ABI or Step/Direction. A summary of the maximum speed for each high-speed interface is shown in Table 15.

Table 15. Interfaces overview

Interfaces	Number of I/f Wires	Resolution	Features	Other options
SafeSPI	4	14 bits	Interface Speed: 10MHz Fastest Position Update rate:3.9µs	Analog Input (pin 4)
UART	1 or 2	14 bits	Interface Speed: 2MHz Fastest Position update rate: 15µs	Analog Input (pin 4)
UVW	3	6 - 48 counts per period	600 krpm	1-8 programmable pole pairs per period
ABI	3	9-12	max. edge rate = 8MHz: speed ≤600 krpm @9bit 468 krpm @10bit 234 krpm @11 bit 117 krpm @12 bit	Binary and decimal based resolutions
AB + PWM				
Step/Direction + Index				
Step/Direction + PWM				

5.1 SafeSPI Interface

The SafeSPI Serial Peripheral Interface for Automotive Safety is an open standard based on the de-facto Serial Peripheral Interface (SPI) industry standard. The RAA2P3200 was developed in accordance with SafeSPI specification version 1.0. Further details can be found at: https://safespi.org.

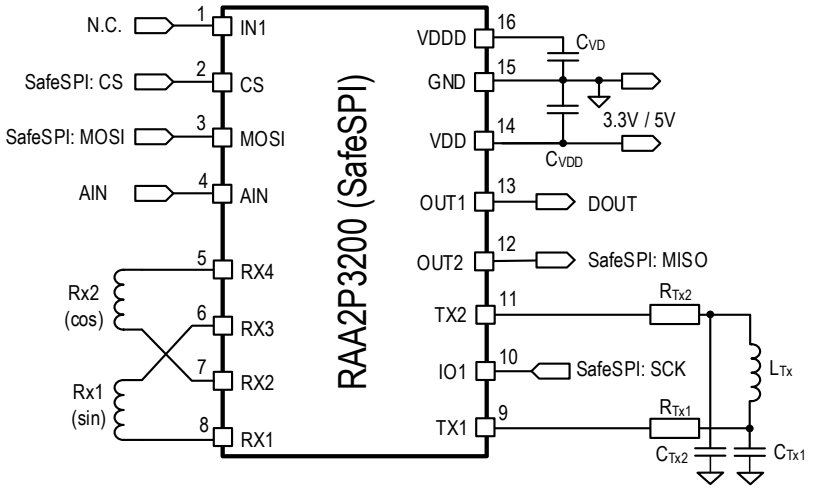


Figure 13. Safe SPI - Input/Output Pins

The RAA2P3200 supports the following features:

- Command frame according to SafeSPI standard.
- Out-Of-Frame communication protocol.
- Data read is frozen/latched on the rising edge of CS.
- Multi-slave configuration with dedicated chip selects.
- 32-bit frame format, 16-bit data per frame.
- Frame starts with MSB first.
- Supports Burst Write mode.
- Programmable Clock phase CPHA
- Programmable Clock polarity CPOL
- Operation on both at 3.0V and 3.3V (as specified in SafeSPI standard), and at 4.5V to 5.5V supply voltage.

Data transfer over the SafeSPI interface is controlled by the Chip Select (CS) signal. While the CS signal is high, incoming data is ignored at the data input MOSI (Master-Out-Slave-In) and the data output MISO (Master-In-Slave-Out) remains in high impedance state.

A low signal at the Chip Select (CS) activates the SafeSPI interface, enabling data transfer between the SafeSPI Master and Slave. The Serial Clock (SCK) defines the data transfer speed, synchronizing all data transmission and reception.

Commands are transmitted from the master to the slave via the MOSI line, with the SPI Slave responding through the MISO line, see Figure 14 for details.

5.1.1 Timing Specifications

Table 16. SafeSPI Output User Programming Options

SafeSPI Interface Programming Parameter	Number of options	Programming option
SCK Clock polarity: CPOL	2	0: Clock idles at 0, each cycle consists of a pulse of 1 1: Clock idles at 1, each cycle consists of a pulse of 0.
SCK Clock phase: CPHA	2	0: Output data is latched on the trailing edge of the preceding clock cycle, while the input data captures the data on the leading edge of the clock cycle. 1: Output data is latched on the leading edge of the preceding clock cycle, while the input data captures the data on the trailing edge of the clock cycle.

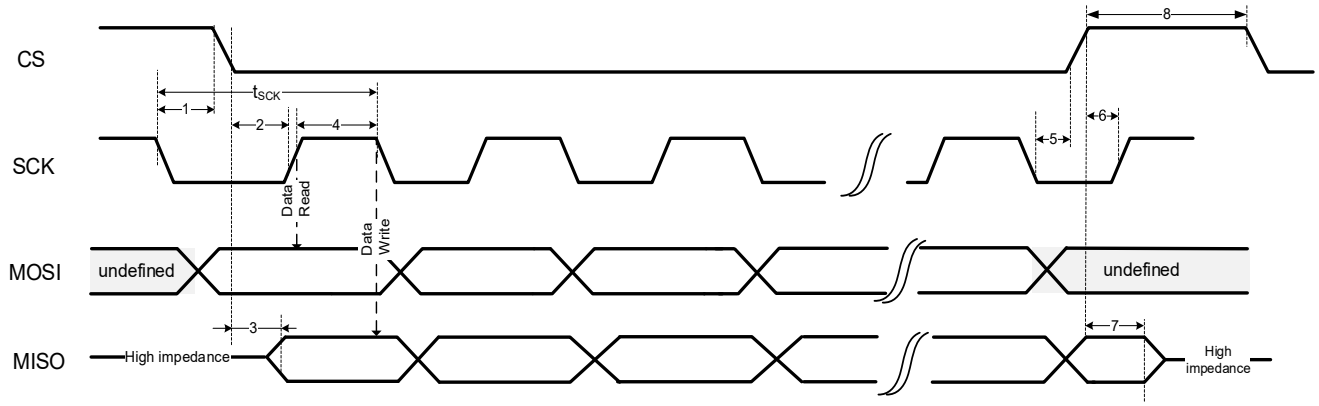


Figure 14. Safe SPI Timing Diagram for Mode 0 (CPOL=0; CPHA=0)

The incoming data is received on the rising edge and transmitted on the falling edge of clock signal SCK.
For CPOL and CPHA parameters, refer to Table 16.
The incoming data is received on the rising edge and transmitted on the falling edge of the clock signal SCK.

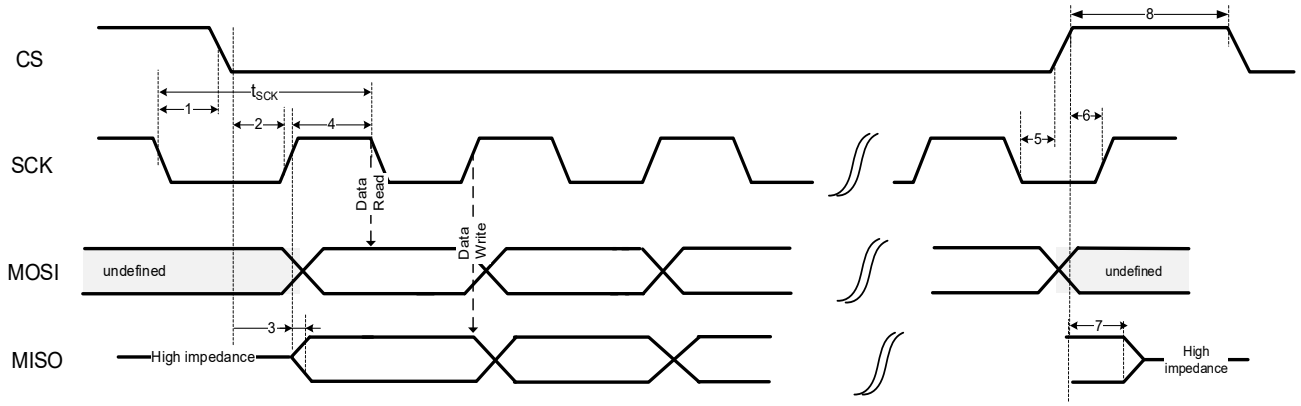


Figure 15. Safe SPI Timing Diagram for Mode 0 (CPOL=0; CPHA=1)

The incoming data is received on the falling edge and transmitted on the rising edge of clock signal SCK.
For CPOL and CPHA parameters, refer to Table 16.

Table 17. SafeSPI Timing Requirements

Symbol		Parameter	Min	Typ	Max	Units
1	$t_{sck\_dis\_lo}$	SCK disable lead time, time between the falling edge of SCK and falling edge of CS	10			ns
2	$t_{sck\_en\_hi}$	SCK enable lead time, time between the falling edge of CS and rising edge of SCK	40			ns
3	$t_{MISO\_valid\_lo}$	MISO data valid time, time between the falling edge of CS and the start of MISO operation			40	ns
4	t_{SCK_hi}	SCK high time, time between rising edge and falling edge of SCK	40			ns
5	$t_{SCK\_en\_lo}$	SCK enable lag time, time between the falling edge of SCK and rising edge of CS	20			ns
6	$t_{SCK\_dis\_hi}$	SCK disable lag time, time between the rising edge of CS and rising edge of SCK	10			ns
7	t_{MISO_dis}	MISO data disable lag time, time between the rising edge of CS and disabling of MISO data			50	ns
8	t_{CS_hi}	Sequential transfer delay	700			ns
f_{SCK}		SCK clock frequency		10	12.5	MHz
n_{Fps}		Frame rate (32 bit frame + t_{CS_hi})		256.4	306.7	kFrames / second

5.1.2 SafeSPI Frame

5.1.2.1 SafeSPI Out of Frame Logical Layer

The Out-Of-Frame communication protocol ensures simultaneous data reading and command broadcasting in parallel. The response from the SafeSPI slave (the RAA2P3200) is always synchronized with the subsequent command frame of the Master.

For example, while the Master transmits Command #2 over the MOSI line, it simultaneously receives the response from Command #1 over the MISO line.

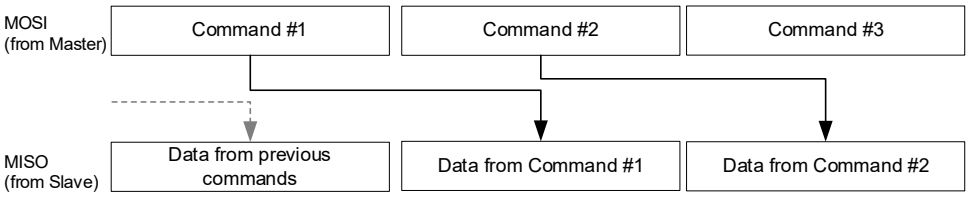


Figure 16. Out-Of-Frame communication

5.1.2.2 SafeSPI Protocol

The SafeSPI data frame consists of 32 bits. MSB is transmitted first.

5.1.2.3 SafeSPI Master Commands

The master initiates communication over the MOSI line. The interface supports various read and write operations determined by a 3-bit command field as the following:

- Sensor Read (0b000): reads the linearized, speed compensated 14-bit position.
- Read from register (0b001): specifies the register address to read from, see Table 19 for examples.
- Write to register (0b010): two frames are required for register write: the first frame contains the address, and the second frame contains the data to be written to that address.
- Write Burst to registers (0b011): performs a sequence of write commands on contiguous registers.

Table 18. SafeSPI Commands

Command [2:0]	SafeSPI Command
0b000	Sensor Read (Position)
0b001	Read from Register
0b010	Write Register
0b011	Burst Write
0b1xx	Undefined (error)

5.1.2.4 SafeSPI Response Slave to Master

Response sequence by the Slave over the MISO line is the following:

1. D: 1-bit data identifier, which defines whether the response contains sensor data (D= 1) or not (D=0).
2. SA: 10-bit Slave Address uniquely identifying the content of the response data (Sensor Data [15:0]). Only the 3 MSBs are used in the RAA2P3200, the remaining 7 bits are not assigned (N/A)
3. S1: status bit (S1, MSB) indicating the status of the sensor, see Table 20.
4. Data [15:0]: 16 bits of data, which can be either sensor data (identified by D=1) or other data (identified by D=0), as requested in the previous frame. See Table 19 for examples.
5. S0: the second status bit (S0, LSB) indicating the status of the sensor, see Table 20 for status descriptions.
6. CRC: 3-bit cyclic redundancy check

Table 19 shows an abstract of the main registers that are accessible through the SafeSPI interface. A comprehensive list of all accessible registers is provided in the *RAA2P3200 Programming Manual* document, available on request from Renesas.

5.1.2.5 Sensor Read

With the Sensor Data Read, users can obtain the 14-bit compensated position information by transmitting two 32-bit SafeSPI frames. When the D bit is set to 1 (indicating Sensor Data), the sensor's response is received on the MISO output during the second frame, as shown in Figure 18.

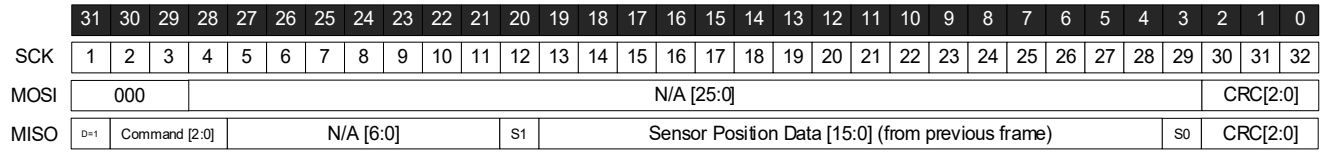


Figure 17. SafeSPI Frame for Reading Sensor Data

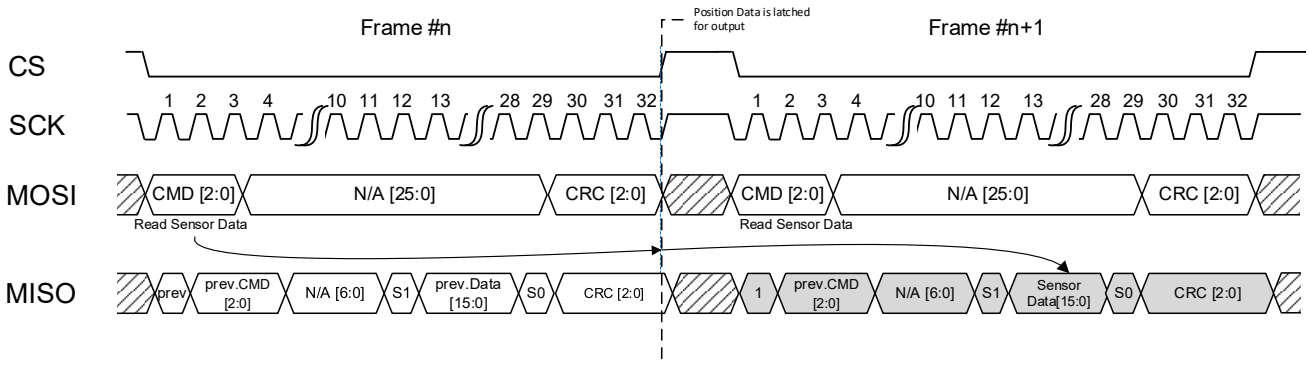


Figure 18. SafeSPI Signal Diagram for Reading Sensor Data (CPHA = 0)

5.1.2.6 Register Data Read

Register Data Read allows users to access internal register information using two 32-bit SafeSPI frames. When the D bit is set to 0 (indicating Register Read), the sensor's response is received on the MISO output during the second frame, as shown in Figure 20. The available registers are listed in Table 19.

Table 19. SafeSPI Available Register Data

Address	Type of data	Length [bits]	R/W	Note
0x0276	Raw Position Data	16	R	Raw Position after angle calculation
0x026A	Linearized position	14	R	Position after angle calculation + linearization
0x026E	Speed compensated position	14	R	Position after angle calculation + linearization + speed compensation (correction of speed related propagation delay) This register is also read by the “read sensor” command
0x02A2	Interpolated Position	14	R	Position after angle calculation + linearization + speed compensation (correction of speed related propagation delay) + position interpolation
0x0282	Turns counter	12	R	±2048 turns; increments/decrements at every zero-crossing of the position data. Counter is reset after Power-on-reset
0x0286	Chip internal temperature	8	R	Internal temperature sensor, measuring the junction temperature of the chip
0x0296	Analog input	13	R	Voltage at pin AIN
0x0298	VDDD voltage	13	R	Measurement of the VDDD reference voltage, for external temperature measurement using an NTC
0x0270	Signal magnitude	14	R	Magnitude of input signal: sqrt (V_{sin}^2 + V_{cos}^2)
0x027A	Sine raw data	13+1	R	Raw data of sine coil inputs after AGC + inversion bit
0x027C	Cosine raw data	13+1	R	Raw data of cosine coil inputs after AGC + inversion bit
0x029E	DOUT FLAG output	1	R/W	Control of digital FLG output by writing 0/1 into a register
0x0264	Customer ID 0	16	R	Customer ID information
0x0266	Customer ID 1	16	R	Customer ID information
0x0268	Customer ID 2	16	R	Customer ID information

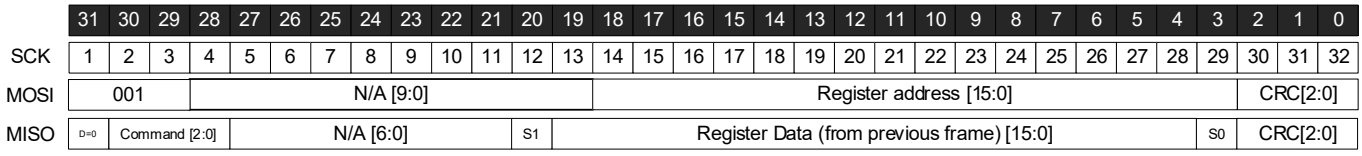


Figure 19. SafeSPI Frame for Reading Register Data

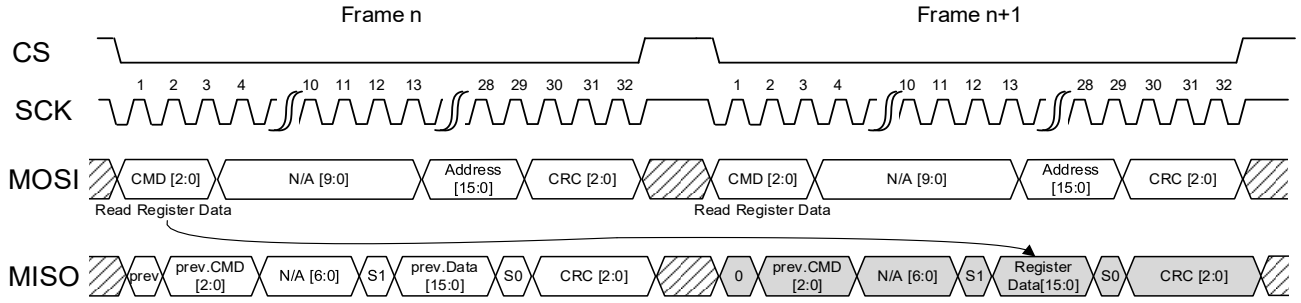


Figure 20. SafeSPI Signal Diagram for Reading Register Data (CPHA = 0)

5.1.2.7 Register Data Write

The Register Data Write function allows users to write on internal registers using two 32-bit SafeSPI frames. When the D bit is set to 0, the first frame includes the address, and the second frame contains the data, as illustrated in Figure 22.

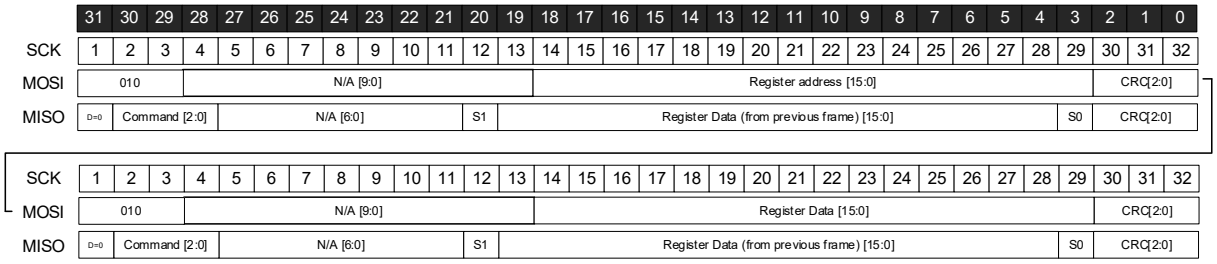


Figure 21. SafeSPI Frame for Writing Register Data

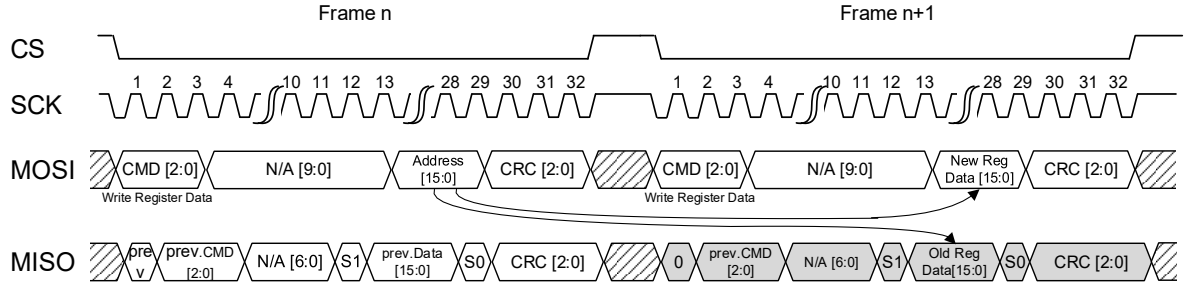


Figure 22. SafeSPI Signal Diagram for Writing Register Data (CPHA = 0)

5.1.2.8 Register Data Burst Write

The RAA2P3200 supports Burst Write mode, which facilitates rapid consecutive register writes. In this mode, the register address automatically increments with each frame, allowing the master to efficiently write data to the memory.

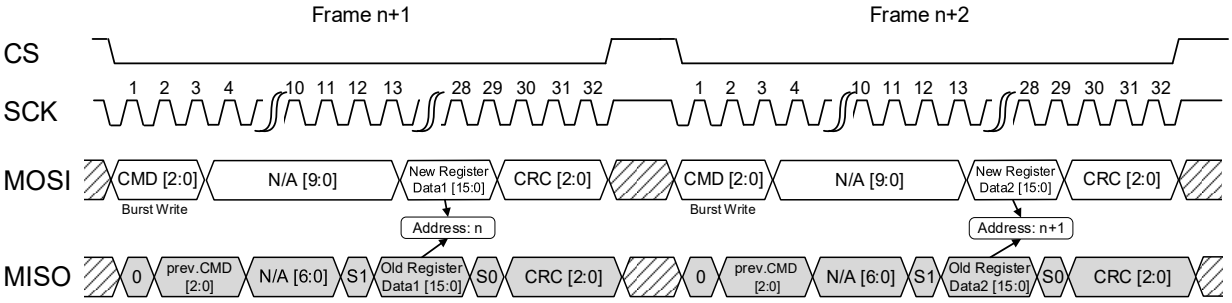


Figure 23. SafeSPI Signal Diagram for Burst Writing Register Data (CPHA = 0)

Table 20. SafeSPI Status Bit Indication

Status bit S1	Status bit S0	Status Indication
0	0	Valid sensor data
0	1	Sensor is in error state
1	0	Sensor is in programming mode
1	1	Sensor is in initialization state. Data [15:0] still contains data

5.1.2.9 CRC Protection

The Cyclic Redundancy Check (CRC) is calculated over bits 31:3 using the polynomial of $x^3 + x + 1$ (binary 1011). The initial value is set to 0xb101, and value is 0xb000. For more information, see the *RAA2P3200 Programming Manual* document.

5.2 Incremental Interfaces

The RAA2P3200 includes incremental and BLDC motor commutation interfaces such as ABI, Step/Direction, and UVW, making it ideal for replacing optical and magnetic encoders in industrial applications. All incremental interfaces utilize three channels on OUT1, OUT2 and IO1 pins, as shown in Figure 24.

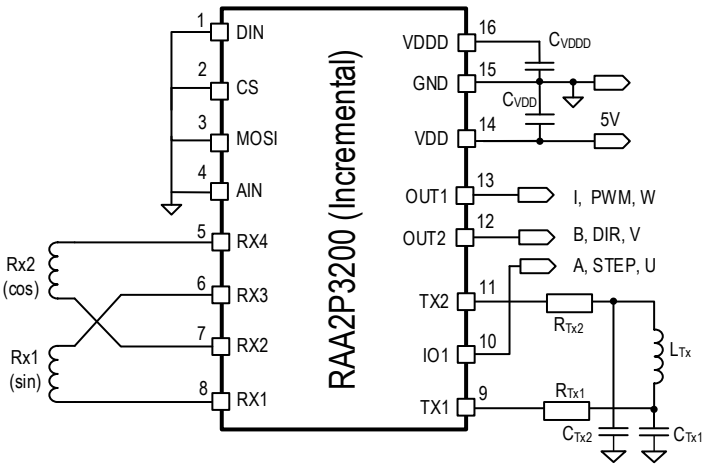


Figure 24. Incremental Interfaces Input/Output Pins

Table 21. Incremental Interfaces User Programming Options

Parameter		Number of options	Programming Options	
Incremental mode		5	ABI, AB+PWM, Step/Direction+Index, Step/Direction+PWM, UVW	
Index pulse length		2	For ABI and Step/Direction mode: 1 LSB, 3 LSBs	
Index position		4	For ABI and Step/Direction mode	
Interpolation factors	Base	12	Binary	Decimal
	Pulses per period [el.]		128 / 256 / 512 / 1024	125 / 250 / 500 / 1000
	Counts per period [el.]		512 / 1024 / 2048 / 4096	500 / 1000 / 2000 / 4000
UVW pulses per period [el.]		8	1, 2, 3, 4, 5, 6, 7, 8	
Startup counter burst mode		5	Burst generator enabled/disabled If enabled: Frequency of startup burst generator	
Startup counter wait time		4	If enabled: wait time of burst generator after POR	
Delay compensation		2	Enable/Disable	

5.2.1 ABI Interface

The ABI interface uses two quadrature channels, A and B, which toggle with a 50% duty cycle. The I (Index) signal provides a pulse once per revolution, marking the zero-angle position. Each cycle of channels A and B generates four unique states.

Counting up or down occurs at each edge of channels A and B, resulting in four count increments or decrements per pulse. Consequently, the number of counts per period is four times the number of pulses per period. The counting direction of the receiving counter depends on the state of the channels at each edge (see Figure 25). In clockwise rotation, a rising edge of channel A occurs when channel B is low, whereas in counterclockwise rotation, the rising edge of channel A occurs when channel B is high.

The RAA2P3200 device also allows for programmable reversal of rotational direction, enabling easy adaptation to different requirements.

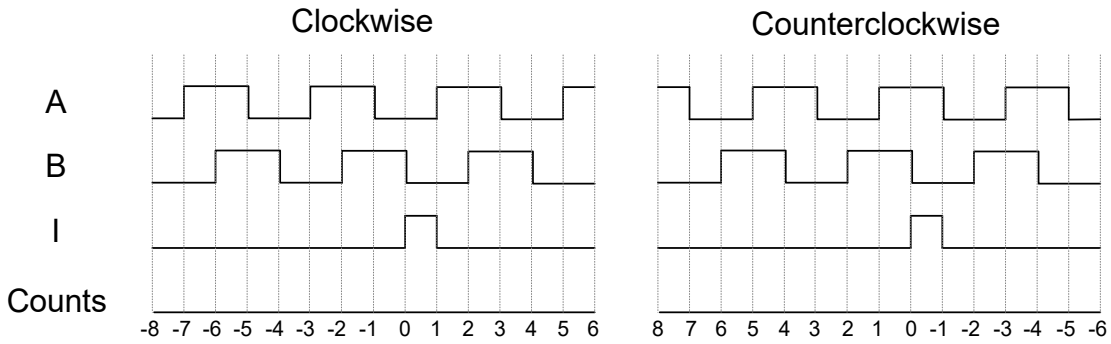


Figure 25. ABI Protocol

5.2.2 Step/Direction

The RAA2P3200 can be configured for the Step/Direction protocol. In this protocol, one pin (Step) delivers one pulse per count, while the other (Direction) is held high or low to indicate the rotational direction. As a result, the Step pin outputs double the number of pulses compared to A pin in ABI mode.

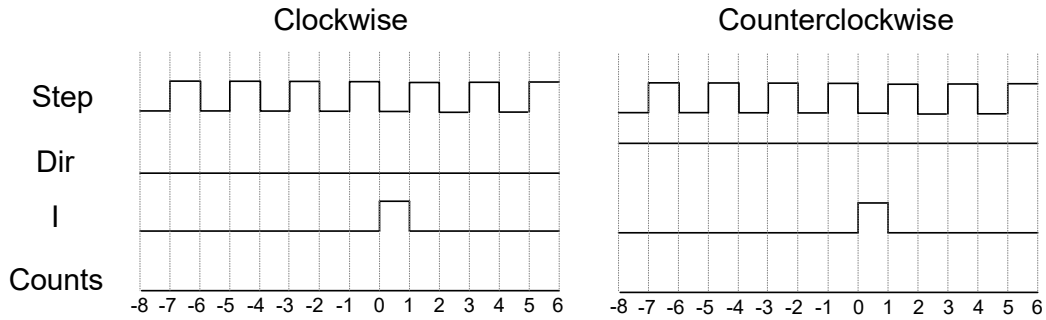


Figure 26. Step/Direction Protocol

5.2.3 UVW Motor Commutation Interface

The UVW interface is designed to replace the simple block commutation scheme used in brushless DC motors that employ three discrete magnetic switches. It works as an incremental interface, providing three channels with one pulse per period, each channel phase shifted by 120° electrically (see Figure 27).

In normal operation, this interface can exhibit six states. The two states that do not occur during normal operation are UVW = 000 and UVW = 111. These two states are reserved for diagnostic indication.

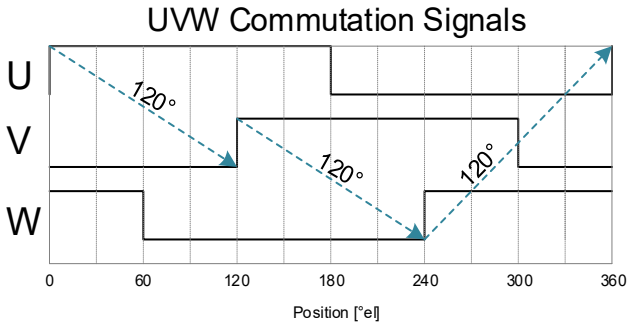


Figure 27. UVW Decoding Scheme within One Electrical Period

The sequence of three-phase shifted UVW signals appears once per electrical phase of the e-motor. For motors with n-pole-pairs, the sequence repeats n times per mechanical turn. The number of UVW pulses per electrical period is programmable from 1 to 8.

Multi-periodic coil designs offer flexibility to match the number of pole pairs on the motor with an equivalent number of periods in the coil design. For example, a four-pole pair motor can be matched with the following:

- a four periodic coil design with 1 UVW pulse per period

- a one periodic coil design with 4 UVW pulses per period

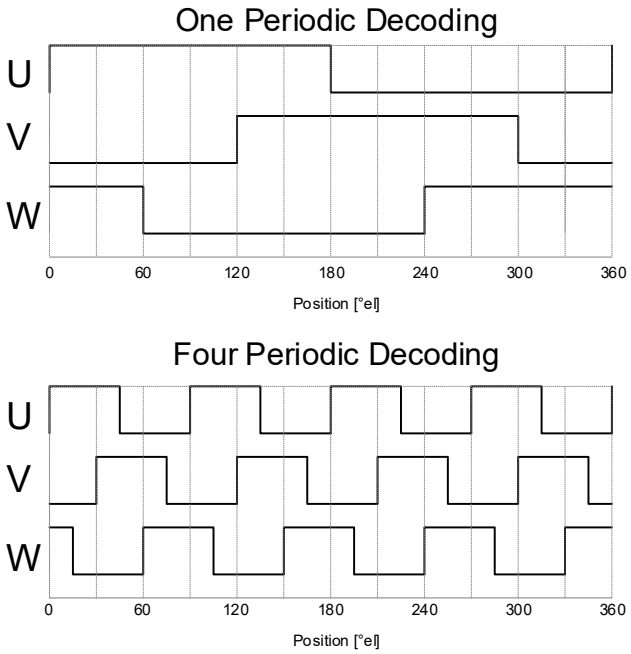


Figure 28. Decoding Examples for 1 and 4 Pulses per Period

5.2.4 Interpolation Factor/Resolution

The incremental interfaces for the RAA2P3200 device offer four interpolation settings (9-bit,10-bit,11-bit,12-bit) in both binary and decimal formats. The interpolation factor is the number of counts per electrical period. “Pulses per period” denote the pulses generated on one channel during a single electrical period (360° el.). These settings determine the counts per electrical period, which must be multiplied by the number of primary coil periods to get the total counts per mechanical period.

5.2.5 Maximum Speed

The maximum rotation speed is defined by the maximum output pulse rate at channels A and B, which is 2MHz. Additionally, the maximum rotation speed is influenced by the interpolator resolution and the number of pole pairs of the coil. In addition, the maximum rotation speed is constrained by the maximum input frequency, which is 10kHz (600 000 rpm) as shown in Table 22.

Table 22. Maximum Speed

Interpolation Factor, Resolution	Maximum Counts per Revolution	Maximum Electrical Speed [rpm]	Maximum Pulse Rate, Outputs A and B	Maximum Edge Rate
9-bit	512	600 000	2MHz	8MHz
10-bit	1024	468 000		
11-bit	2048	234 000		
12-bit	4096	117 000		

For UVW mode, the interpolation factor must be set to 12-bit, offering a maximum speed of up to 117krpm (both electrical and mechanical), regardless of the pole pair (pulses per period) setting as shown in Table 23.

Table 23. UVW Maximum Speed

Pulses per Period	Maximum Electrical and Mechanical Speed [rpm]	Maximum Pulse Rate, Outputs U, W and W [kHz]
1	117 000	1.95
2		3.9

Pulses per Period	Maximum Electrical and Mechanical Speed [rpm]	Maximum Pulse Rate, Outputs U, W and W [kHz]
3		5.85
4		7.8
5		9.75
6		11.7
7		13.65
8		15.6

Note: the maximum mechanical speed is determined by dividing the maximum electrical speed by the number of periods per turn for the specific coil design. For example, a coil design with 5 periods and 10-bit interpolation has a maximum speed of 468krpm / 5 = 93600rpm.

5.2.6 Index Pulse

Encoders' incremental interfaces send an index pulse to indicate their zero position. The receiver uses this pulse to synchronize and subsequently utilizes the A/B and Step/Direction signals to track of the position accurately. To support a variety of receivers, this pulse is programmable in both width and position.

Two programmable options are available for the index pulse width: either a duration of 1 count or 3 counts. Additionally, there are four programmable options for the index pulse position (index_cfg). Each configuration defines the resulting diagnostic state as described in Table 24.

Table 24. ABI Index Configurations

Index Pulse Position	ABI Diagnostic State	Step/Direction Diagnostic State
A = 0, B = 0	A = 1, B = 1, I = 1	Step = 1, Dir = X , I = 1
A = 1, B = 1	A = 0, B = 0, I = 1	Step = 0, Dir = X , I = 1
A = 0, B = 1	A = 0, B = 0, I = 1	Step = 1, Dir = X , I = 1
A = 1. B = 0	A = 0, B = 1, I = 1	Step = 0, Dir = X, I = 1

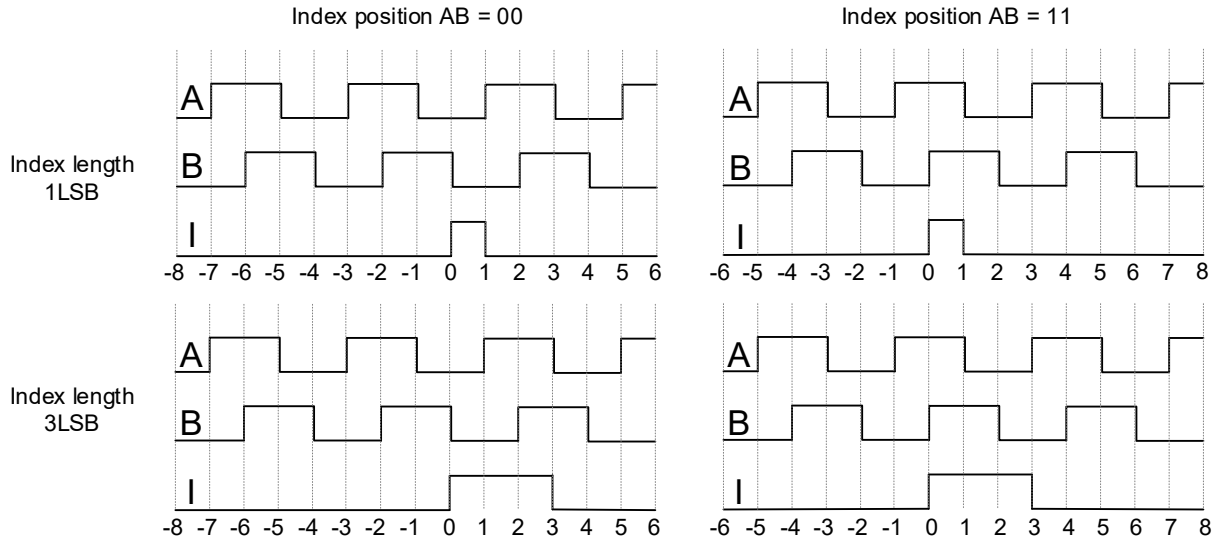


Figure 29. ABI Index Position and Length Configurations

The index configuration defines the diagnostic state indication. The unique combination of the three signals in diagnostic mode ensures that it does not occur during normal operation.

5.2.7 True-Power-On Absolute Position Information

Incremental interfaces lack the capability to deliver absolute position information immediately upon power-up.

At power-up, the absolute position remains unknown if the measured object, such as a motor, is stationary. Motion is required to detect the first index and calculate the position accurately.

RAA2P3200 is capable of calculating the absolute position internally, and provides it over the incremental interface after power-up, before any rotation starts. This is implemented by sending an artificial burst of pulses. (see Figure 30).

After a programmable wait time, an index pulse is generated to reset the external counter at the receiving end, followed by a series of AB pulses that indicate the absolute position. The frequency of this pulse train is programmable, ensuring synchronization of the counter at the receiving end with the correct absolute position. The rotor must remain stationary during the initial pulse train sequence. This feature can be enabled or disabled by user programming.

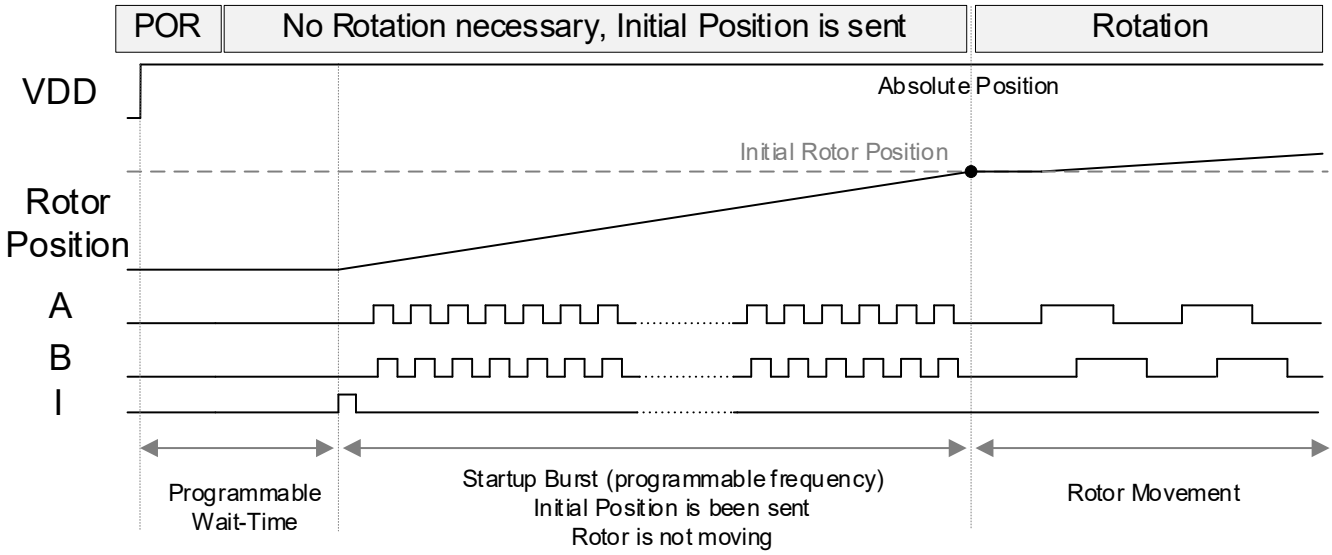


Figure 30. ABI True-Power-On Burst Delivering Absolute Position at Startup Without Rotation

5.2.7.1 True Power-On with AB + PWM Mode

In AB+PWM mode, the index output is replaced with a PWM output, allowing users to determine the exact position during start-up based on the PWM output. Once the measured object begins to move, the position can be calculated from the pulses of the A and B outputs. The PWM signal is available in a wide frequency range, see Table 25 for details.

5.2.7.2 True Power-On with SD + PWM Mode

In addition to the AB+PWM mode, a 3-wire mode with Step/Direction, and PWM is available. This versatile setup ensures precise position control and flexibility in various applications.

5.2.8 PWM Interface (AB + PWM, Step/Direction + PWM)

The PWM interface can be used in combination with the incremental A + B or Step/Direction outputs to provide the absolute position, replacing the Index output. It can either be configured as push-pull or open drain output on pin 13 as shown in Figure 31. The PWM interface can be configured for push/pull or open drain output.

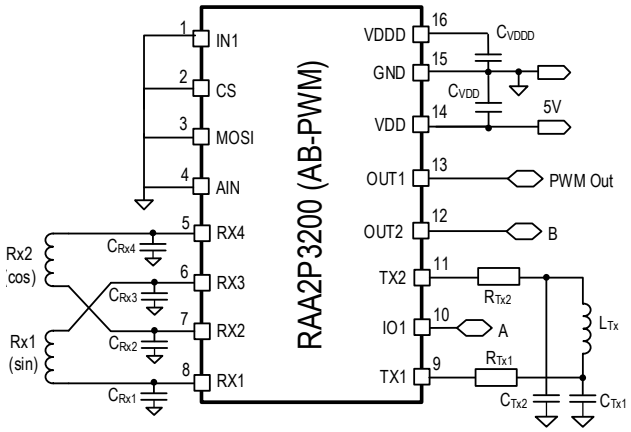


Figure 31. AB + PWM Configuration

Table 25. PWM Interface User Programming Options

Incremental Interface Programming Parameter	Number of options	Programming Option
PWM frequency	8	109, 219, 547, 1094, 1641, 2188, 3282, or 4376 Hz
PWM output mode	2	Push-pull or open-drain
PWM polarity	2	Position information is either active low or active high
PWM resolution	2	12 -bit (all PWM frequencies) or 14-bit (PWM frequencies from 109-1094 Hz)
Diagnostic mode indicated by PWM signal	3	Disabled, Diagnostic mode enabled with low duty cycle, Diagnostic mode enabled with high duty cycle

The 12-bit PWM signal frame is composed of a 256 LSB high level header, followed by the 12-bit Position Data ranging from 0 to 4095 LSBs. This is marked by a high-level section and a corresponding low-level section ensuring a total of 4095 LSBs. The frame concludes with a 256 LSB low-level trailer as shown in Figure 32.

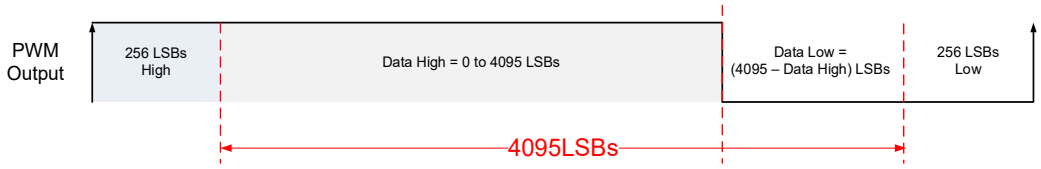


Figure 32. 12-bit PWM Signal in Normal Operation

The minimum 12-bit duty cycle can be calculated with Position data = 0 LSB High, 4095 LSBs low:

$$DC_{min} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{256}{256 + (4095 + 256)} = 5.557\%$$ **Equation 13**

The maximum 12-bit duty cycle can be calculated with Position data = 4096 LSBs High, 0 LSBs low:

$$DC_{max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{256 + 4095}{(256 + 4095) + 256} = 94.443\%$$ **Equation 14**

The 14-bit PWM signal frame shown in Figure 33 is structured similarly as the 12-bit PWM signal frame shown in Figure 32, with the key difference being an increased resolution by a factor of 4.

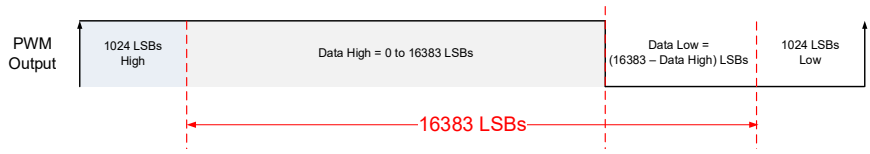


Figure 33. 14-bit PWM Signal in Normal Operation

The minimum 14-bit duty cycle can be calculated with Position data = 0 LSB High, 16383 LSBs low:

$$DC_{min} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{1024}{1024 + (16383 + 1024)} = 5.556\%$$ **Equation 15**

The maximum 14-bit duty cycle can be calculated with Position data = 16384 LSBs High, 0 LSBs low:

$$DC_{max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{1024 + 16383}{(1024 + 16383) + 1024} = 94.44\%$$ **Equation 16**

5.2.8.1 PWM Diagnostics Mode

In PWM diagnostics mode, the duty cycle is forced to a range not utilized in normal operation. This mode can be configured as the following:

- Diagnostic low mode, see Figure 34 and Figure 36
- Diagnostic high mode, see Figure 35 and Figure 37

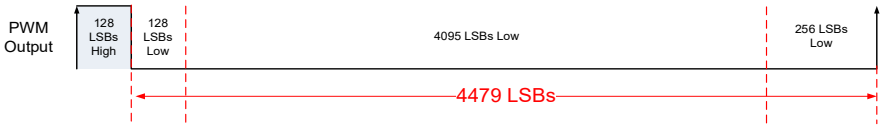


Figure 34. 12-bit PWM Signal in Diagnostics Low Mode

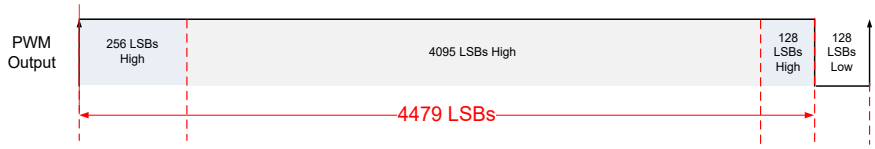


Figure 35. 12-bit PWM Signal in Diagnostics High Mode

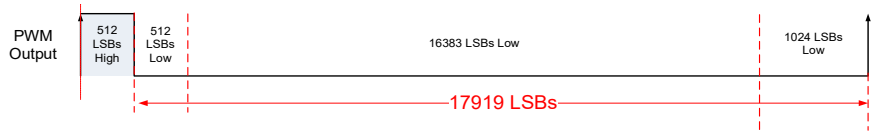


Figure 36. 14-bit PWM Signal in Diagnostics Low Mode

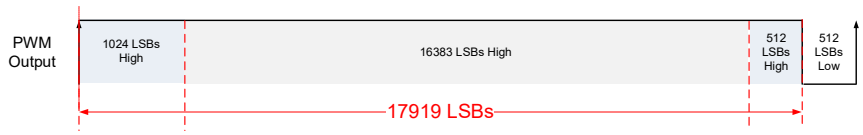


Figure 37. 14-bit PWM Signal in Diagnostics High Mode

5.3 High Speed UART Interface

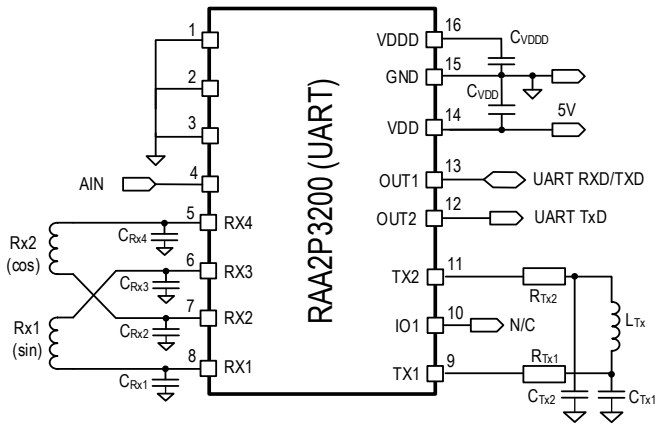


Figure 38. UART Interface with Input/Output Pins

The UART interface is utilized as a one-wire programming interface and serves as primary back-end interface in the following modes:

- single wire bidirectional
- dual wire unidirectional
- dual wire differential bidirectional

Note: all UART modes operate in half duplex data transmission.

Table 26. UART Operation Modes

Operating mode:	OUT1 (Pin 13)	OUT2 (Pin 12)
Single Wire Bidirectional	RxD/TxD	Not Used
Dual Wire Unidirectional	RxD/TxD complementary	TxD
Dual Wire Differential Bidirectional	RxD	TxD

Table 27. UART Interface User Programming Options

UART Programming Parameter	Number of Options	Programming Option
UART output drive	2	Open drain or push-pull
UART slave address	4	2 LSBs of general slave address
UART Baud rate [1]	6	{9600, 57600, 115200, 230400,1M,2M} bit/sec
UART operation mode	3	Single wire bidirectional Dual wire unidirectional Dual wire differential bidirectional
UART error warnings	7	Baud rate, framing, CRC errors

[1] Maximum data rate may be reduced by external capacitive and resistive loads when open drain configuration is used.

5.3.1 Single Wire Bidirectional UART

In Single Wire UART mode, the device communicates with the ECU using only the OUT1 pin, which can be configured in either push-pull or open drain mode. The Single Wire UART mode is suitable for point-to-point connection, where one device interfaces with an ECU (Figure 39), or for implementing a multi-slave single wire bidirectional connection. (Figure 40).

In open drain mode, a Master can address up to four sensors over a single wire, one sensor at a time. Each sensor is identified by its unique slave address, stored in the NVM or by address pin strapping.

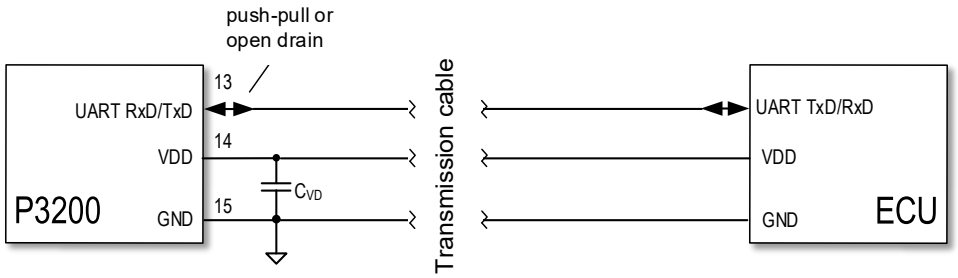


Figure 39. UART Point-to-Point Single Wire Bidirectional Connection

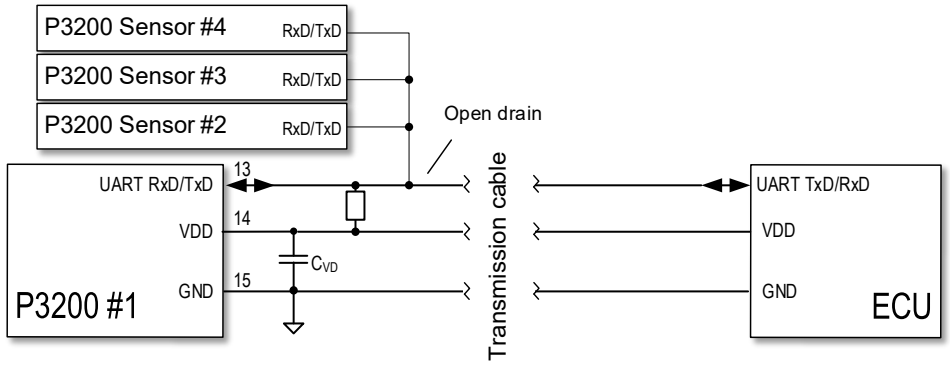


Figure 40. UART Multi-Slave Single Wire Bidirectional Connection

5.3.2 Dual Wire Bidirectional UART with Pseudo-Differential TX

In Dual Wire UART mode, the device uses both OUT1 and OUT2 pins for communication. This mode can implement point-to-point connection, similar to those shown in Figure 39. This communication mode uses OUT1 as single wire transceiver as shown in Figure 41.

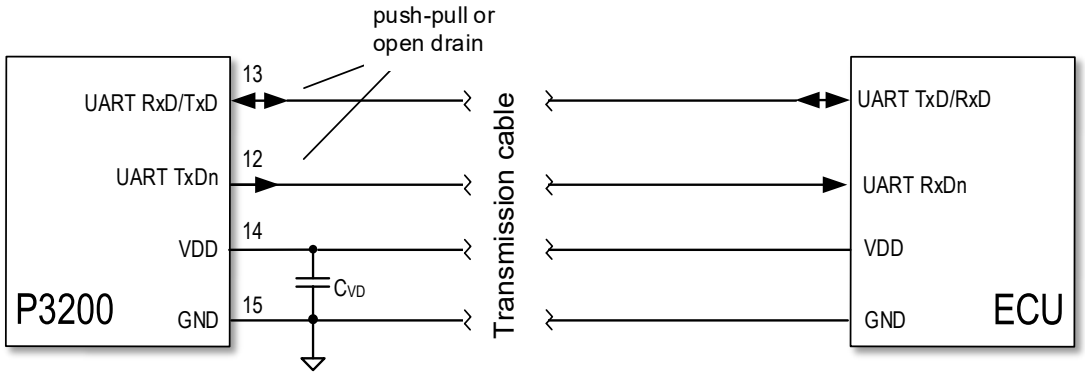


Figure 41. UART 2-wire Point-to-Point Connection with Pseudo-Differential TX

In pseudo differential mode, the OUT2 (pin 12) functions as transmitter while OUT1 (pin 13) is used for both transmitting and receiving. The data on OUT1 is an inverted version of the data transmitted on OUT2, creating a pseudo differential signal that enhances safer data transmission reliability. While receiving, OUT1 remains in a high state.

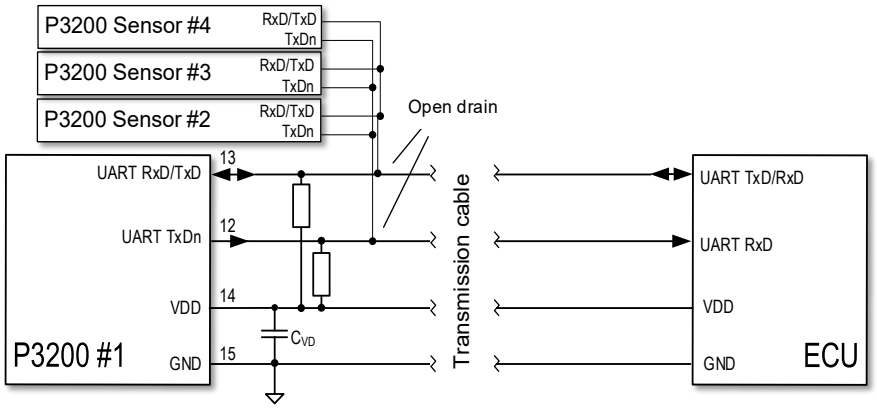


Figure 42. UART 2-Wire Connection with Pseudo-Differential TX and Multiple Slaves

In pseudo-differential mode with open drain configuration, a single Master can address up to four sensors, one at a time. Each sensor is identified by its unique slave address, stored in the NVM or by address pin strapping.

5.3.3 Dual Wire Unidirectional UART

In dual wire mode, separate unidirectional lines are used for transmitting and receiving data. The transmitter can be configured for either push-pull or open-drain output. Use push-pull mode for achieving data rates up to 2Mbit/s. In open-drain mode, data rates can be limited based on the capacitive load of the transmission cable and the resistance of the pull-up resistor.

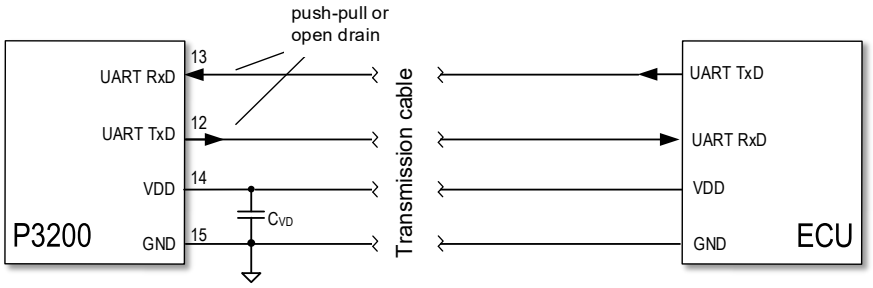


Figure 43. UART 2-Wire Unidirectional Connection

In dual wire unidirectional mode, a single Master can address up to four sensors, one at a time. Each sensor is identified by its unique slave address stored in the NVM or by address pin strapping. For parallel connection of multiple sensors on the same line, the transmitter output (TxD) must be configured for open drain output.

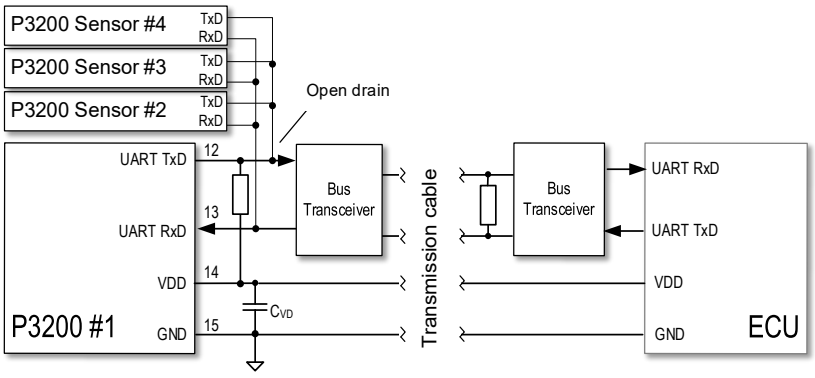


Figure 44. UART 2-Wire Unidirectional Connection with Multiple Slaves and Bus Transceivers

The transmission cable can be extended with external bus transceiver circuits as shown in Figure 44, offering enhanced robustness and reduced capacitive load for the UART TxD output pin. This setup supports high data rates up to 2 Mbit/s.

5.3.4 UART Address Pin Strapping

The two least significant bits (LSBs) of the RAA2P3200 UART's slave address can be set either through programming or by hardware pin strapping.

In pin strapping mode, two pins set the address:

- Pin #2: ADR0 - Address bit 0
- Pin #3: ADR1 - Address bit 1

5.3.5 UART Operating Commands

The RAA2P3200 provides the following UART operating modes:

- 16-bit register write (Figure 45)
- 16-bit register read (Figure 46)
- Fast read mode of two registers within one frame with 12,14 or 16 bits of data per register (Figure 47)

5.3.5.1 Gap Time

A minimum pause (gap) time is implemented between the messages to ensure the controller returns to idle before the next communications begins. The minimum gap time foreach UART baud rate configuration is outlined in Table 28.

Table 28. UART wait time between measurements

UART Baud Rate [bits/sec]	Minimum Gap Time [bits]
9600, 57600, 115200, 230400	10
1M, 2M	12

5.3.5.2 UART Register Write

This mode writes one register per frame. Each frame contains 8 bytes, with each byte including a start and stop bit, totaling 8x10bits. A short wait (GAP) time is required between frames. All bytes are written by the Master and sent to the chip.

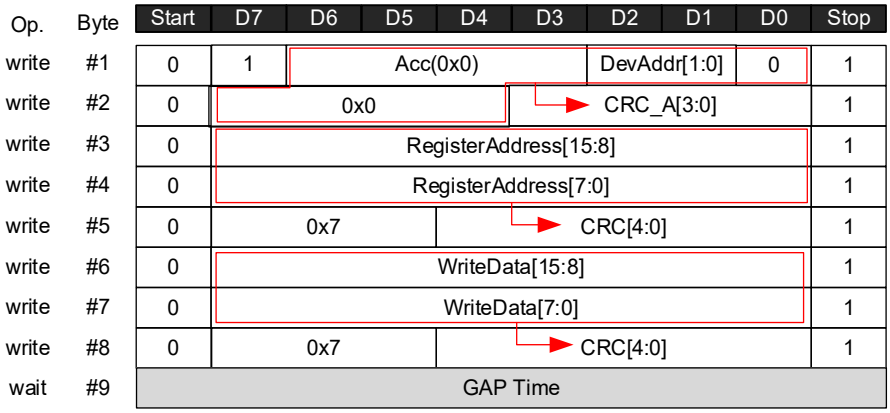


Figure 45. UART Register Write Mode

The Write Frame structure can be seen in Figure 45 where:

- Acc: Access type 0x0 for register write.
- DevAddr: The device address if several sensors are connected in parallel, it defines their slave address (0x1-0x3). The default is 0x0.
- Register Address: The target register.
- Write Data: The data to be written.
- CRC, CRC_A: Cyclic redundancy check.

5.3.5.3 UART Register Read

In read mode, the device reads one register per frame. The first five bytes are sent from the Master to the chip, while bytes six to eight are read from the chip by the UART in read access mode. In all modes, the bit order is MSB to LSB. The read frame contains eight bytes, each with a start and stop bit, totalling 8x10 bits. A short wait (GAP) time required between each frame.

During data read operations, the Master must add an additional wait bit when switching from sending to receiving data due to the generation of the differential start and stop bits. This results in each frame containing either 91 bits (for data rates up to 230.4 kbit/s) or 93 bits (for 1Mbit and 2Mbit data rates).

In register read mode, an additional wait bit must be added at the end of byte five before the chip can start transmitting data (start bit of byte six). The *ReadData* content is latched at the stop bit of byte five.

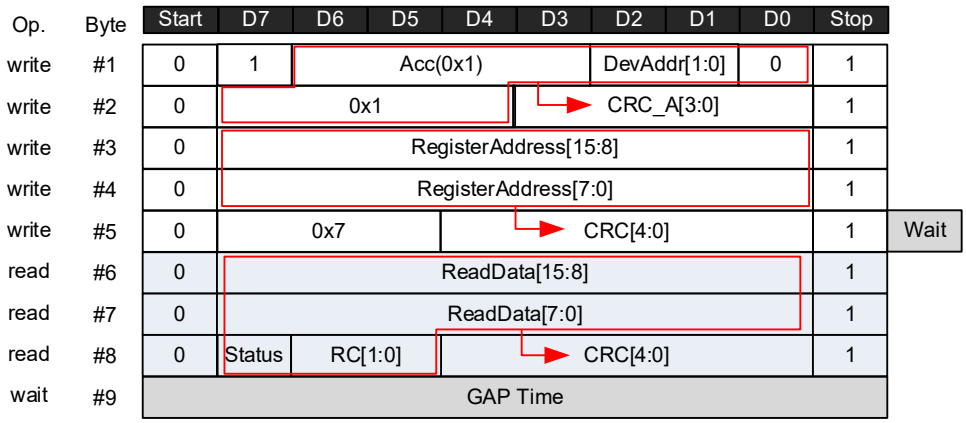


Figure 46. Register Read Mode Frame

The Read Frame structure can be seen Figure 46 where:

- Acc: Access type 0x1 for register read.
- DevAddr: The device address if several sensors are connected in parallel, it defines their slave address (0x1-0x3). The default is 0x0.
- Register Address: The target register.
- Read Data: The data contents of the target register.
- CRC, CRC_A: Cyclic redundancy check.
- Status: 1 bit status flag information of the sensor (0: normal operation, 1: error)
- RC: Rolling counter, a counter that increments with each frame and wraps around 0 when overflowing.
- Wait: 1 bit wait time for master before receiving data (in pseudo-differential mode only).

5.3.5.4 UART Fast Two-Register Read

This mode facilitates the efficient reading of a defined subset of two registers per frame. The first two bytes of the frame specify which subset of the predefined registers is to be read, defined by a 4-bit access code, The access type is set on the *Acc1* and *Acc2* bitfields (see Table 29). The read data for the first register is contained in bytes three to five, and for the second register, it is in with bytes six to eight.

Table 29. UART Fast Access Mode

Acc Type1/2	Byte#3 / Byte#6	Byte#4 / Byte#7		Byte#5 / Byte#8		
2	Sensor Data[11:4]	Sensor Data[3:0]	RC[5:2]	S	RC[1:0]	CRC[4:0]
4	Sensor Data[13:6]	Sensor Data[5:0]	RC[3:2]	S	RC[1:0]	CRC[4:0]
7	Chip Temperature	0x0	RC[5:2]	S	RC[1:0]	CRC[4:0]
8	Analog input [12:5]	Analog input [4:0]	0 RC[3:2]	S	RC[1:0]	CRC[4:0]
11 = 0xB	IRQ Status 0 [15:8]	IRQ Status 0 [7:0]		S	RC[1:0]	CRC[4:0]

Acc Type1/2	Byte#3 / Byte#6	Byte#4 / Byte#7	Byte#5 / Byte#8		
12 = 0xC	IRQ Status 1 [15:8]	IRQ Status 1 [7:0]	S	RC[1:0]	CRC[4:0]
13 = 0xD	IRQ Status 2 [15:8]	IRQ Status 2 [7:0]	S	RC[1:0]	CRC[4:0]
14 = 0xE	IRQ Status 3 [15:8]	IRQ Status 3 [7:0]	S	RC[1:0]	CRC[4:0]
15 = 0xF	IRQ Status 4 [15:8]	IRQ Status 4 [7:0]	S	RC[1:0]	CRC[4:0]

[1] RC: Rolling counter

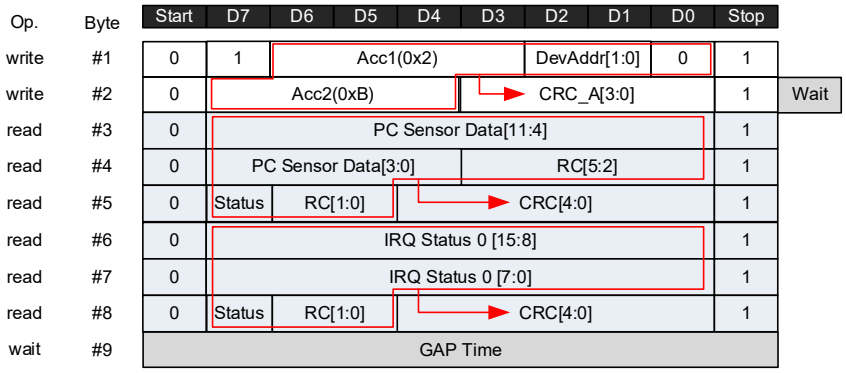


Figure 47. UART Fast Read Mode Example with Different Access Codes

The frame structure can be seen in Figure 47, an example of reading 12-bit primary coil sensor data (Acc1 = 0x2) and 16-bit IRQ status 0 (Acc2 = 0xB), the frame bitfield are described in the list below:

- Acc1, Acc2: Access code: 0x2 to 0xF (see Table 29)
- DevAddr: Device address: (default = 0x0. If several sensors are connected in parallel, it defines their slave address (0x1-0x3).
- CRC, CRC_A: Cyclic redundancy check.
- Status: 1 bit status flag information of the sensor (0: normal operation, 1: error)
- ReadData: the data answer from the IC are the PC Sensor Data + RC for Byte #3 and #4 according to ACC1=0x2, while for ACC2=0xB the device provides IRQ_Status on Byte#6 and #7. (see Table 29). The ReadData is latched at the stop bit of Byte#2 for Acc1, and at the stop bit of Byte#5 for Acc2.
- RC: Rolling counter, a counter that increments with each frame and wraps around 0 when overflowing
- Wait: 1 bit wait time for master before receiving data (in pseudo-differential mode only)

In fast read mode, an additional wait bit must be added at the end of byte #2 before the chip can begin transmitting data.

5.3.5.5 UART Fast Read Mode with Same Access Code

Reading the same register twice provides two results from the same input at different sampling timestamps. For example, the primary coil sensor data can be read twice (see Figure 48). The first reading (Acc1= 0x2) is sampled at the end of byte two, while the second reading (Acc2 = 0x2) is sampled at the end of byte five. This results in an interval of 30 bits between the two samples in the UART clock (3 bytes, including start and stop bits).

By repeating this sequence, users can obtain two samples within a 92-bit frame. The timeframe between consecutive sample is 30 UART clock cycles, which equates to 15µs at 2M/s Baud-rate. The time interval between each frame is 46µs at the same Baud-rate.

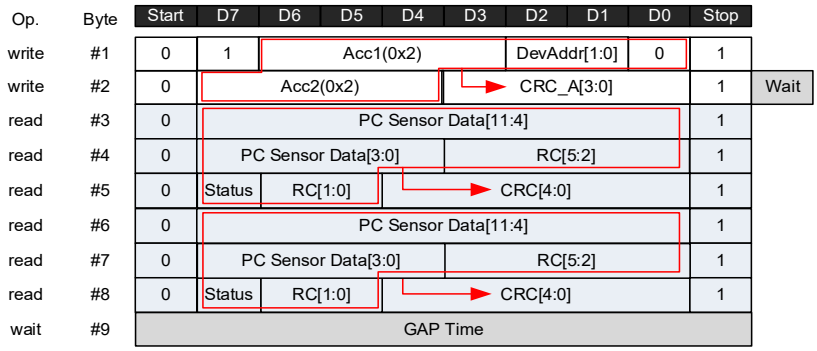


Figure 48. UART Fast Read Mode of the Same Register

In Table 30 there is a summary of the UART interface speed, depending on the selected Baud rate and mode. Note that one frame can perform a register read, a register write, or two consecutive register read (fast read mode).

Table 30. UART Data Access Speed with *uart_start_bit_cfg = 0*

UART Baud Rate [bits/sec]	Bits per Frame (incl. Gap Time)	Time per Frame [µs]	Frame Rate [frames/sec]
9600	91	9479.4	105.5
57600	91	1580	633
115200	91	789.9	1265
230400	91	395	2532
1M	93	93	10.75k
2M	93	46.5	21.5k

5.4 UART Programming Interface

Any user programmable parameter can be accessed through the 2-wire programming process, with UART protocol.

Performing an end-of-line calibration or in-line programming of a position sensor module containing the RAA2P3200, requires no additional wires. The chip is programmed through the OUT1 and OUT2 outputs at the operative supply voltage range (5V ±10%, 3.3V ±10%).

A short programming window is enabled after POR and requires a digital unlock password to enable programming. If no password is sent, the chip resumes its normal operating mode.

For more details, please refer to the *RAA2P3200 Programming Manual* document.

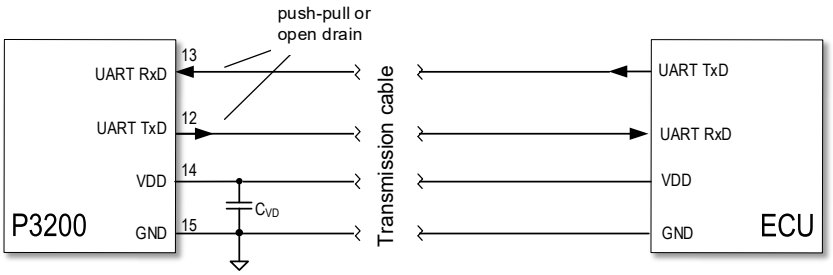


Figure 49. UART NVM Programming

5.4.1 Lock Feature

The RAA2P3200 includes a user configurable lock bit option to restrict write and/or read access. Once the lock bits are enabled, no further write or read operations to the RAA2P3200 are prohibited. Note that once a RAA2P3200 part locked, it cannot be unlocked.

For more details, refer to the *RAA2P3200 Programming Manual* document.

6. Auxiliary Input and Outputs

One analog auxiliary input is available for connecting external devices with analog outputs, that can be read through the SPI or UART interface. Further, a digital output pin is available indicating user programmable features. A summary is shown in Table 31.

Table 31. Auxiliary Inputs and Digital Output Options

Interface	Analog Input	Digital Output
		Register Flag (OD)
SafeSPI	Yes (pin 4)	Yes (pin 13)
UART	Yes (pin 4)	n/a
Incremental	n/a	n/a

6.1.1 Analog Input

The analog input is available on pin 4 (AIN) can be used to read analog voltages from external sensors via SPI or UART interfaces. See Table 32 for the key parameters of this input. The analog value must be in relation to VDDD.

Table 32. AIN Analog Input Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_AIN}	AIN voltage range		0.1		1.2	V
RES_{AIN}	ADC resolution			12		bits
T_{Smp_AIN}	Sampling rate		4.4			kHz
ACC_{AIN}	Analog Input Accuracy		-1.2		1.2	% VDDD

Both the analog input and the VDDD reference voltages are internally measured and stored in registers. The external load on VDDD cannot exceed 4 mA as specified in Table 4.

6.1.2 Digital Output

An optional digital output is available and can be configured for various functions, depending on the selected interface, as shown in Table 31.

6.1.2.1 Register Flag

In this configuration, available in UART mode, the DOUT output can be used to drive external circuits. It is controlled by writing either of the following options to a register bit to the address 0x029E [0]:

- Register bit 0: FLG output is low
- Register bit 1: FLG output is high

This function can be integrated with a heartbeat feature to provide diagnostic status information alongside the flag value. This status is indicated by a 1.5KHz pulse, see Figure 50 with a duty cycle of 97% when the flag is high and 3% when the flag is low.

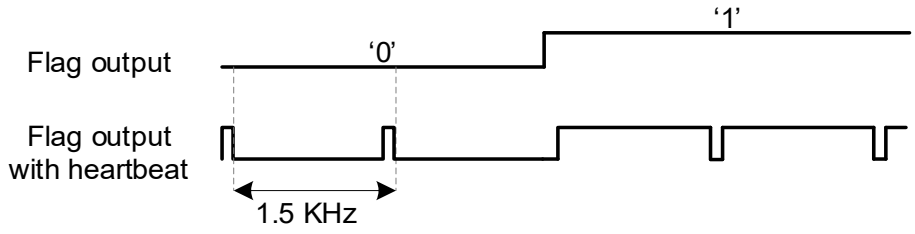


Figure 50. Flag Output Configurations

7. On-Chip Diagnostics

The RAA2P3200 includes on-chip diagnostics featuring an extensive number of internal diagnostic monitors (DM).

For detailed description, see the *RAA2P3200 Programming Manual* document.

Table 33. Diagnostic Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_{FDTI}	Failure detection time interval (time to detect and internally set a flag describing the error condition)	fdti_cfg=1			2.3	ms
		fdti_cfg=0			20	ms

Table 34. Diagnostic Monitors

Category	Diagnostic Monitors (DM)	Description
Monitoring of external supply	VDD Monitor	External VDD supply out of range
Monitoring of internal supplies	VDDA Monitor	Internal VDDA (Analog supply) out of range / undervoltage /overvoltage
	VDDD Monitor	▪ Internal VDDD (Digital supply) out of range ▪ Short on VDDD ▪ Overcurrent at VDDD pin
	Internal Supply Monitor	Internal supply out of range
	Internal pre-regulators Monitor	▪ Internal pre-regulator for power management (bandgap, analog parts) out of range ▪ Internal pre-regulator for output stages out of range
	Driver Regulator Monitor	OUT2 regulator driver out of range
	Oscillator Regulator Monitor	LC oscillator regulator out of range
	Bias Current Monitor	Bias current diagnostic out of range
Monitoring of RX coils	RX coil Sine Monitor	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX SIN
	RX coil Cosine Monitor	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX COS
	RX coil Sine/Cosine neighbor inputs short	Short check between Sine/Cosine coil set detected
Monitoring of TX coils	TX Voltage Monitor	▪ Common mode voltage of TX1/TX2 out of range ▪ Flag for broken pins of LC oscillator
	LC Oscillator Monitor	▪ LC oscillator stuck detected ▪ LC oscillator frequency out of range
Monitoring of system clock	System clock Monitor	▪ Fault in internal system clock: frequency out of range ▪ Fault in internal system clock: stuck detected
Monitoring of the internal communication channel	Internal digital logic failure Monitor	Internal digital logic failure detected such as APB Diagnostic failure, IC internal registers failure, FSM failure, CORDIC failure, other digital failures.
Monitoring the internal memory	Non-Volatile Memory Monitor	▪ CRC mismatch over the NVM or internal shadow register ▪ NVM read timeout fail
Data path diagnostics	Data path WD/OF/UF/DO Monitor	Internal errors, such as overflow, underflow, division by 0, or watchdogs
Position Range Monitoring	Position Range Monitor	Position outside of the defined range failure
Temperature monitoring	Temperature Monitor	▪ Temperature warning detected ▪ Temperature error (shutdown) detected

Category	Diagnostic Monitors (DM)	Description
Magnitude evaluation	Magnitude static Monitor	Magnitude static check error detected on RX coils
Monitoring of analog signal path offset	ADC temperature sensor offset fail Monitor	Compensation of the internal offset not sufficient
Monitoring of the mechanical stress /cracks	Broken chip check Monitor	IC die mechanical failures detected
LPF check for signal path	LPF Monitoring	Failure in internal LPF
AGC monitoring	AGC error Monitoring	▪ Automatic gain control loop not converging ▪ Pre-defined acceptable gains for the AGC not sufficient for RX
Monitoring of the output interfaces	Output Interfaces monitors	▪ Failure of the SPI interface ▪ Failure of the UART interface
Analog input	Analog Input Monitoring	Failure on analog input range
OUT2 and IO1 pins monitoring	OUT2/IO1 pins Monitoring	▪ Overvoltage/undervoltage ▪ Short on OUT2/IO1 detection

In diagnostic mode, the incremental outputs enter a combination of logic levels that do not occur in normal operation. The diagnostic state depends on the settings of index pulse width and index pulse position as outlined in Table 35. Additionally, the diagnostic status indication varies based on the incremental mode selected.

A summary of the diagnostic state indication is shown in Table 35.

Table 35. Incremental Output Diagnostic States

Selected ABI Index/Zero Position	Diagnostic State Indication			
	ABI Mode	Step/Direction Mode	AB+ PWM Mode	UVW Mode
Zero / Index: ABI = 001	ABI = 111	SDI = 1x1	PWM = 2.5% duty cycle	UVW = 111
Zero / Index: ABI = 111	ABI = 001	SDI = 0x1	PWM = 97.5% duty cycle	UVW = 000
Zero / Index: ABI = 011	ABI = 101	SDI = 1x1	PWM = 97.5% duty cycle	UVW = 000
Zero / Index: ABI = 101	ABI = 011	SDI = 0x1	PWM = 2.5% duty cycle	UVW = 111

7.1 Shorted and Broken Wire Detection

A fault from a broken or shorted wire refers to the connection between the sensor IC and the control unit (such as MCU or ECU). This includes the soldering of the IC pins, PCB traces, connectors, and cables.

7.1.1 Shorted Wires

Shorts between ground, signal, and supply wires can be safely detected, as shown in Table 36.

Table 36.Detection of Shorts between Wires

Cable connections	Supply	Output	Ground
Supply	Short between two supplies. Only applicable for isolated, redundant sensor IC supplies. Must be monitored and controlled by the external power supply unit supplying the sensors.	Short between Supply and Output. Output switches to tri-state when the output current exceeds the overcurrent threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between Supply and Ground. Overcurrent in the supply line. Must be monitored and controlled by the external power supply unit supplying the sensor.

Cable connections	Supply	Output	Ground
Output	See description for short between Output and Supply	Short between two different outputs. Outputs switch to tri-state when their output current exceeds the overcurrent threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between Output and Ground. Output switches off when the output current exceeds the overcurrent threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.
Ground	See description for short between ground and supply	See description for short between Output and Ground	Short between Ground and Ground: Separate ground lines are not recommended for EMC reasons

7.1.2 Broken Supply Lines, Incremental Output Modes

As shown in Table 35, the diagnostic state of the incremental outputs depends on the settings for the following:

- Incremental mode
- Index pulse width
- Index position

If a fault occurs due to a broken supply line, the outputs enter a high ohmic state. Therefore, the diagnostic state must be indicated by pull-up and/or pull-down resistors, as shown in Figure 51 and Figure 52.

In ABI and Step/Direction mode, depending on Index pulse programming, the diagnostic states are either ABI = 001 or ABI = 111. Therefore, the external pull-up or pull-down resistors must be connected accordingly, as shown in Figure 51.

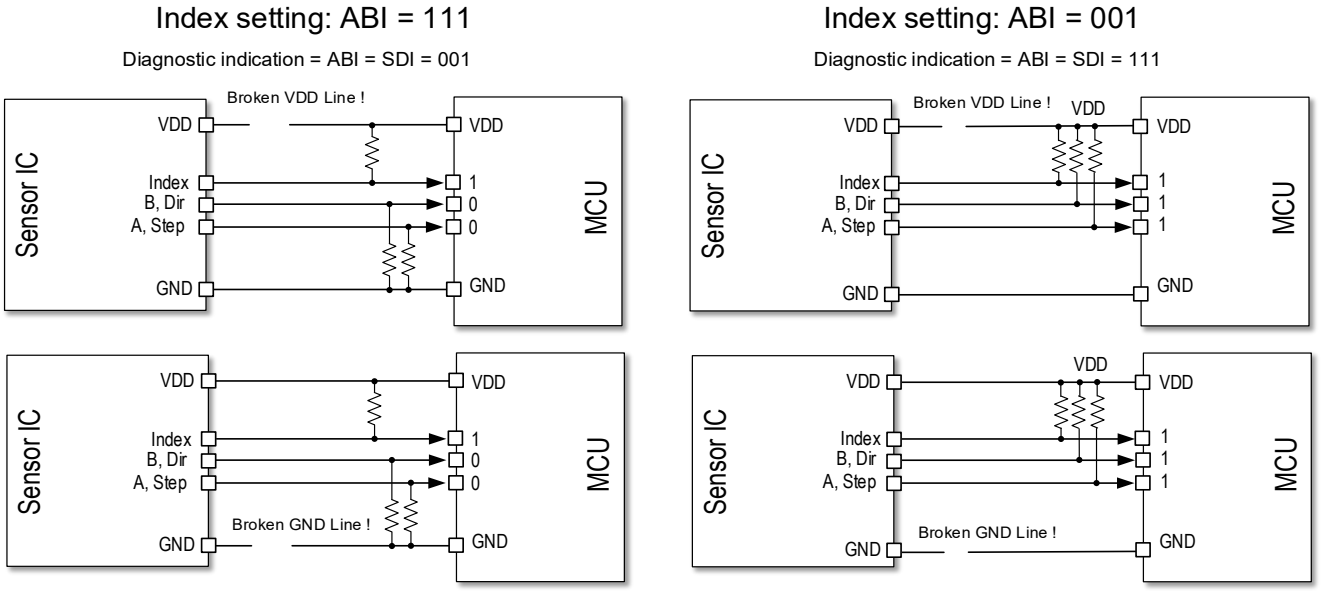


Figure 51. Broken Supply Diagnostic Indication: ABI and Step/Direction Modes

In UVW mode, the diagnostic states are determined by the Index pulse programming. These states are either be UVW = 000 or UVW = 111. Therefore, the external pull-up or pull-down resistors must be connected as shown in Figure 52.

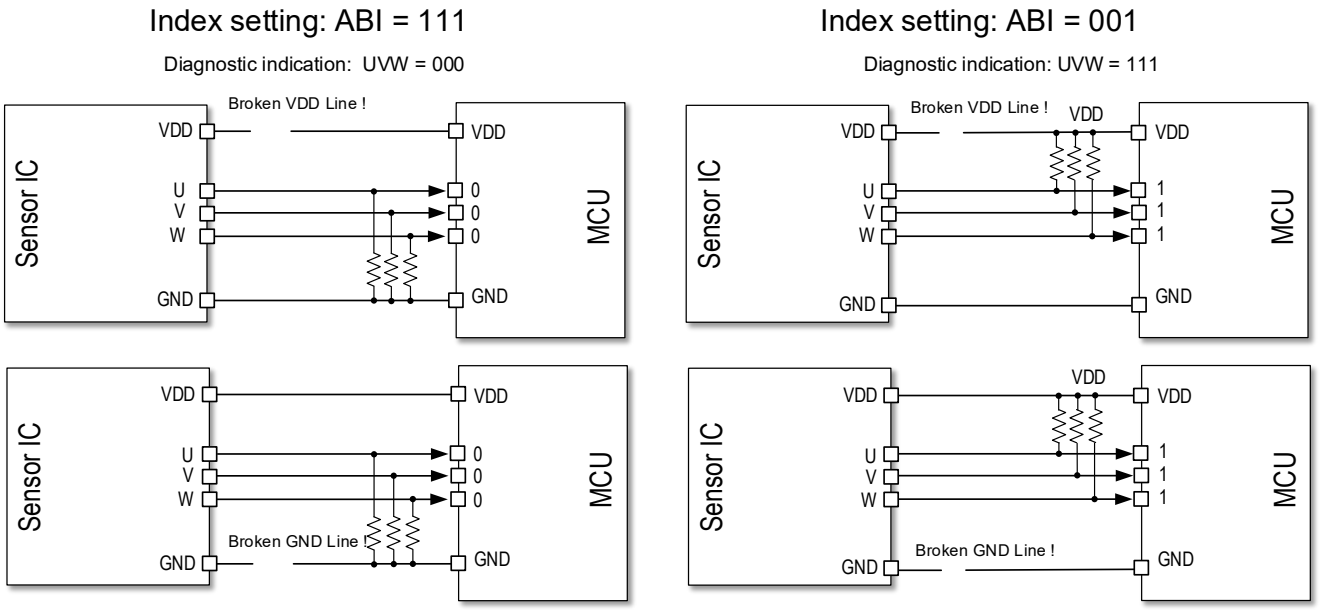


Figure 52. Broken Supply Diagnostic Indication: UVW Mode

7.1.3 Broken Supply and Signal Lines, SafeSPI Mode

Both broken supply lines and broken signal wires can be easily detected in SafeSPI mode through data transmission errors, such as incorrect CRC or Slave data responses. Therefore, additional pull-up or pull-down resistors for diagnostic checks are not required in SafeSPI mode.

7.1.4 Broken Signal Wires, Incremental Output Modes

While a fault caused by a broken supply line can be detected immediately, faults from a broken signal line in incremental output modes cause the signal to be stuck at a high or low level, depending on the connection of the external pull-up or pull-down resistors. In a rotating system, this eventually leads to a logical combination of the outputs that resembles a diagnostic state, and thus indicating a fault. It can take up to one electrical period of rotation before this state has been reached.

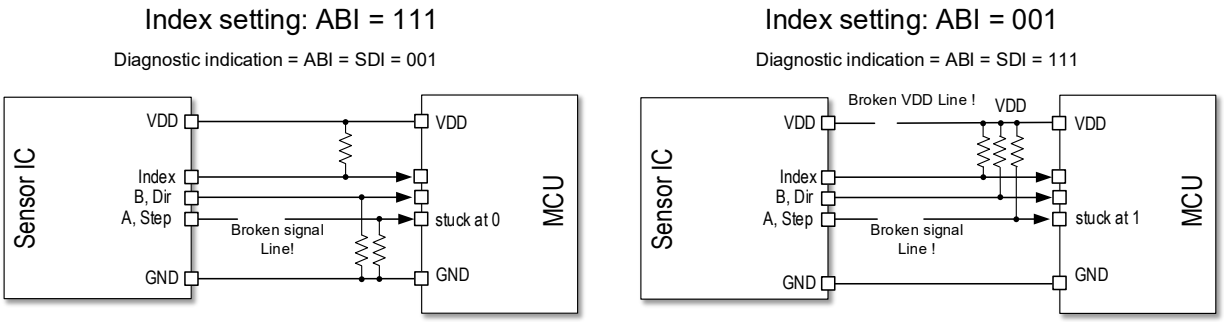


Figure 53. Broken Signal Wires

8. User Programming Options

Table 37 shows an extract of the main configuration options. A detailed description is provided in the RAA2P3200 programming manual, available on request from Renesas.

Table 37. Programming Options

Programming Option	Number of options	Description
Power supply mode	2	3.3V ±10% or 5.0V ±10%
Interface options	6	SPI, UART, ABI, AB+PWM, Step/Direction interface, UVW interface
Initial receiver gain coil	27	Initial receiver gain
Automatic gain control AGC	2	Enabled / disabled
Hysteresis	8	0 to 112 LSBs
Number of linearization points	16 points	2/4/6/8/16 linearization points, programmable in x and y
Linearization points resolution	12-bit	Up to 16 linearization points are freely programmable in X (position) and Y (value) with 12-bit resolution
Magnitude alarm reference limits	2 x 14-bit	Upper and Lower limits programmability
Zero (discontinuity) point	12-bit	0° to <360° in 12-bit steps, position output switches from maximum to minimum value (with increasing position movement) or from minimum to maximum value (with decreasing position movement) at this position
Sine and cosine signal offset correction	2 x 8-bit	±127 LSBs for sine and cosine
Sine and Cosine amplitude mismatch correction	2 x 15-bit	0% to 199% adjustment range per channel
Digital low pass filter	5	Depth of digital low pass filter for position output
Turns counter option	2	Behavior of 12bit turns counter when overflowing: stop at max/min, wrap around
Customer ID	48-bit	Scratchpad register for customer specific data

9. Related Documents

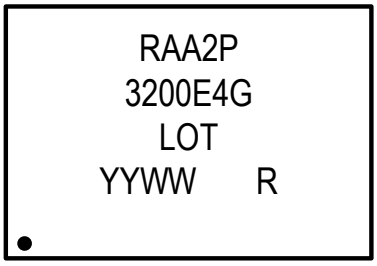
- RAA2P3200 Programming Guide

10. 16-TSSOP Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

16-TSSOP Package Outline Drawing 4.4mm Body, 0.65mm Pitch PGG16T1

11. Marking Diagram



Line 1: First characters of part code RAA2P

Line 2: Next five characters of the part code:
3200E: Single Coil High Speed
followed by:
4 = Operation temperature range, Industrial
G = Industrial Qualified

Line 3: “LOT” = Lot number

Line 4: “YYWW” = Manufacturing date:
YY = last two digits of manufacturing year
WW = manufacturing week
R = RoHS compliant statement

12. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
RAA2P3200E4GSP#HA0	16-TSSOP, 4.4 ×5.0 mm	1	13” Reel, 4000 parts / reel	-40° to +125°C
For communication and programming, the RAA2P3200 Application Modules listed below require an RAA2P-COMBOARD, which is available separately.				

13. Glossary

Term	Description
ABI	ABI quadrature interface
AC	Alternating Current
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
APB	Advanced Peripheral Bus
BLDC	Brushless Direct Current
CDM	Charged-Device Model
CORDIC	Coordinate Rotation Digital Computer
CPHA	SPI Clock Phase
CPOL	SPI Clock Polarity
CS	Chip Select
CRC	Cyclic Redundancy Check
DC	Direct Current
DP	Discontinuity Point
ECU	Electronic Control Unit
EMC	Electromagnetic compatibility
ESD	Electrostatic Discharge
FDM	Failure Detection Mechanisms
FSM	Finite-State Machine
GND	Ground
FSM	Finite State Machine
HK	House Keeping
I/O	Input / Output
I2C	Inter-Integrated Circuit Interface
IC	Integrated Circuit
ID	Identification

Term	Description
LC	Resonant Inductor-Capacitor Circuit
LF	Low Frequency
LPF	Low Pass Filter
LSB	Least Significant Bit
MCU	Micro Controller Unit
MISO	Master In Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
MUX	Multiplexer
NVM	Non-Volatile Memory
OD	Open Drain
PCB	Printed Circuit Board
PP	Push-Pull
RF	Radio Frequency
RX	Receiver
SCL	I2C Clock
SDA	I2C Data
TSSP	Thin Shrink Small Outline Package
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter
UVW	UVW Motor Commutation Interface

14. Revision History

Revision	Date	Description
1.1	Dec 8, 2025	Added paragraph 5.3.4, Corrections in table 15, table 1, table 5, table 7, table 12, paragraph 5.3.1, 5.3.2, 5.3.3
1.0	Sep 8, 2025	Initial release

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