RAA2P3226

High Speed Dual Coil Inductive Position Sensor ICs with UART ABI, Step/Dir and I2C Interfaces

RAA2P3226 product is a high-speed magnet-free, inductive position sensor ICs that can be used for absolute and incremental position sensing in industrial, medical, and consumer applications. The RAA2P3226 IC uses the physical principle of eddy currents to detect the position of a simple metallic target that is moving above a set of coils, consisting of one transmitter coil and two sets of receiver coils.

The coils are typically copper traces on a printed circuit board (PCB). The transmitter coil induces a secondary voltage in the receiver coils, which varies depending on the position of the metallic target above them.

A signal representative of the target's position relative to the coils is calculated by demodulating and processing the secondary voltages from the receiver coils. The target can be made of various metals, including aluminum, steel, or a PCB with a printed copper layer.

The device can achieve high positional accuracy, with up to 15-bit accuracy and 19-bit resolution, while operating at rotational speeds of up to 600000 rpm (electrical). An ultra-low propagation delay of less than 100ns provides high dynamic control for fast spinning motors.

The RAA2P3226 is equipped with:

- Up to 19-bit High-speed UART interface (up to 2Mbit/s)
- Up to 17-bit Incremental interfaces ABI and Step/Direction
- Up to 19-bit I2C interface (up to 400Kbit/s)

Available Support

Renesas provides application modules that demonstrate RAA2P3226 position sensing applications.

Typical Applications

- Optical and magnetic encoder replacement in robotics and industrial automation.
- Rotor position detection for BLDC motors with digital interfaces, adaptable to any pole pair count

Features

- Cost-effective; no magnet required
- Immune to magnetic stray fields; no shielding required
- Suitable for harsh environments and high temperatures
- Dual Coil inputs enabling high accuracy position sensing: up to 19-bit resolution, 15-bit accuracy
- True power-on position, obtained by UART, ABI, Step/Dir (Startup burst generator) or I2C
- Programmable through digital interface with UART or I2C
- Nonvolatile memory enables multiple programming options
- Single IC supports on-axis and off-axis rotation, linear motion, and arc motion sensing
- Adaptable to any full-scale angle range through coil design
- Overvoltage and reverse-polarity protection: ±18V on both supply and output pins
- Supply voltage programmable for 3.3V ±0.3V or 5.0V±0.5V
- 48 bits nonvolatile user ID memory space
- Qualified for industrial application use from -40°C to +125°C ambient temperature
- Small 16 TSSOP package (4.4mm x 5.0mm)

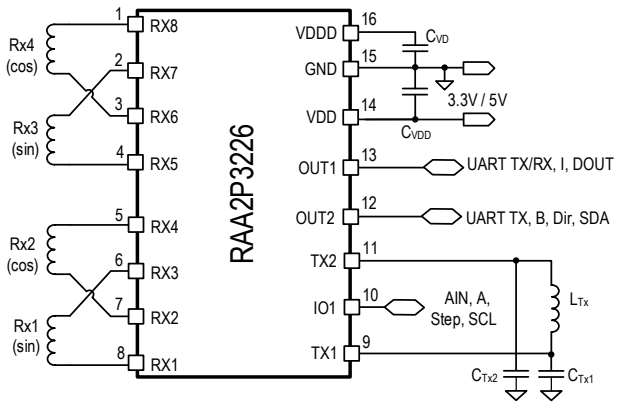

Figure 1. Application Circuit Example

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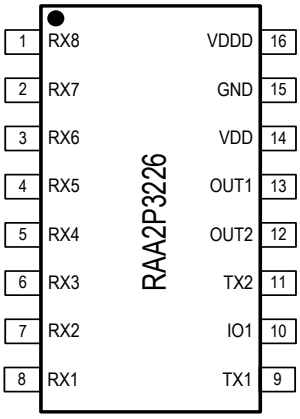


Figure 2. RAA2P3226 Pinout

Table 1. Pin Description

Pin Number	Name	Type	Description
1	RX8	Sensor Input	Receiver coil set #2 (COS_N); secondary receiver coil
2	RX7		Receiver coil set #2 (SIN_N); secondary receiver coil
3	RX6		Receiver coil set #2 (COS); secondary receiver coil
4	RX5		Receiver coil set #2 (SIN); secondary receiver coil
5	RX4		Receiver coil set #1 (COS_N); primary receiver coil
6	RX3		Receiver coil set #1 (SIN_N); primary receiver coil
7	RX2		Receiver coil set #1 (COS); primary receiver coil
8	RX1		Receiver coil set #1 (SIN); primary receiver coil
9	TX1	Transmitter Output	Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND
10	IO1	Digital I/O Analog Input	I2C: SCL UART: Auxiliary Analog Input ABI: A Step/Dir: Step
11	TX2	Transmitter Output	Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND
12	OUT2	Digital I/O	I2C: SDA UART: TxD (2-wire) or Digital output ABI: B Step/Dir: Direction
13	OUT1	Digital I/O	I2C: Digital output UART: Bi-directional TxD/RxD (1-wire), RxD input (2-wire) or inverted TxD. ABI: Index Step/Dir: Index Single Wire programming interface
14	VDD	Supply	External supply voltage (3.3V/5V)
15	GND	Supply	Common ground connection
16	VDDD	Supply	Internally regulated digital supply voltage.

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings listed in Table 2 are stress ratings only. Exceeding these limits can cause permanent damage to the device. The functional operation of the RAA2P3226 at these maximum ratings is not guaranteed. Exposure to the absolute maximum rating conditions could impact device's reliability. All voltage levels are referenced to GND.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{VDDmax}	External supply voltage: VDD	Continuous	-18	18	V
V_{IO1}	Digital I/O pin voltage				
V_{OUT2}	Digital I/O pin voltage				
V_{OUT1}	Digital output pin voltage				
V_{RX1}	Sensor Receiver coil input pin voltage (RX1)	Continuous	-12	12	V
V_{RX2}	Sensor Receiver coil input pin voltage (RX2)				
V_{RX3}	Sensor Receiver coil input pin voltage (RX3)				
V_{RX4}	Sensor Receiver coil input pin voltage (RX4)				
V_{RX5}	Sensor Receiver coil input pin voltage (RX5)				
V_{RX6}	Sensor Receiver coil input pin voltage (RX6)				
V_{RX7}	Sensor Receiver coil input pin voltage (RX7)				
V_{RX8}	Sensor Receiver coil input pin voltage (RX8)				
V_{Tx1}	Transmitter pin (TX1) voltage	Continuous	-0.3	5.5	V
V_{Tx2}	Transmitter pin (TX2) voltage				
$V_{VDDDmax}$	Internal digital supply voltage, VDDD	VDDD is internally regulated with external capacitor to GND.	-0.3	2.0	V
T_{AMB}	Ambient temperature		-40	125	ºC
T_J	Junction temperature		-40	135	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125°C to prevent pre-aging	-55	160	ºC
R_{THJA}	Thermal resistance junction to ambient: 16-TSSOP package	Velocity = 0m/s with 2s2p PCB test board (JEDEC 51-2, JEDEC 51-7)		89.5	K/W
R_{THJC}	Thermal resistance junction to case: 16-TSSOP package	Junction to top of package		38.38	K/W

2.2 ESD Ratings

Table 3. ESD Ratings

Symbol	Parameter	Conditions	Maximum	Units
V_{ESD}	ESD tolerance for all pins Human Body Model: 100pF / 1.5kΩ	According to JEDEC JS-001, classification 2	±2	kV
V_{CDM}	ESD tolerance for all pins. Charged-Device Model (CDM)	According to JEDEC JS-002, classification C2b	±750	V

2.3 Operating Conditions

All minimum/maximum specification limits are guaranteed by design, production testing, and/or statistical characterization. Conditions: T_{AMB} = -40°C to 125°C unless otherwise specified. C_{VDD} = 470nF, C_{VDDD} = 100nF.

Typical values are based on characterization results at default measurement conditions and are informative only.

Table 4. Electrical Characteristics, 5V and 3.3V Modes

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{VDD5}	Supply voltage, 5V mode		4.5	5.0	5.5	V
$V5_{UV}$	Undervoltage detection level, 5V mode	An under-voltage alarm is created if VDD falls below this limit	3.95	4.1	4.45	V
$V5_{OV}$	Overvoltage detection level, 5V mode	An overvoltage alarm is created if VDD rises above this limit	5.55	6.15	6.5	V
V_{VDD3}	Supply voltage, 3.3V mode		3.0	3.3	3.6	V
$V3_{UV}$	Undervoltage detection level, 3.3V mode	An under-voltage alarm is created if VDD falls below this limit	2.7	2.8	2.98	V
$V3_{OV}$	Overvoltage detection level, 3.3V mode	An overvoltage alarm is created if VDD rises above this limit	3.65	3.85	4.04	V
$V_{VDD\_TH\_H}$	Power-on reset (POR), high threshold	Power-on reset (POR): the device is activated when VDD increases above this threshold		2.61	2.7	V
$V_{VDD\_TH\_L}$	Power-on reset, low threshold	The device is deactivated when VDD decreases below this threshold	2.3	2.38		V
V_{DDPOR_HYST}	Power-on reset hysteresis		200	250	300	mV
$t_{stup\ PE}$	Start-up time	Power-on reset (POR) to valid output signal, programming enabled			5	ms
$t_{stup\ PL}$		Power-on reset (POR) to valid output signal, programming locked			3	ms
$t_{stup\ cmd}$	Command timeout time	Time to wait before sending first command	1.5			ms
t_{ProgEn}	Programming window enable time	Timeout window after POR, in which a first programming enable command must be sent			5	ms
t_{ProgUL}	Programming window unlock time	Timeout window after programming enable in which a second unlock command must be completely sent[i]			75	ms

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{VDDD}	Digital supply voltage	Internally regulated. Connect capacitor C_{VDDD} = 100nF from VDDD to GND	1.75	1.8	1.85	V
I_{AUXIN}	VDDD external load current	VDDD must be connected to a capacitor C_{VDDD}.	0		4	mA
$I_{SHORT\ VDDD}$	VDDD short circuit current limitation		18.5	27	40	mA
I_{CC}	Current consumption	Without coils, no load	10	15	20	mA
C_{VDDD}	Capacitor from VDDD pin to GND		100			nF
C_{VDD}	Capacitor from VDD pin to GND	Nominal value	100	470		nF

Table 5. Position Resolution and Update Rate

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
RES_{I2C}	Position Resolution I2C Interface			14		bit
RES_{UART}	Position Resolution UART Interface			14		bit
RES_{INC_BIN}	Position Resolution Incremental Interfaces (ABI,Step/Dir)	Binary Mode Counts per 1 coil period (programmable)		512 1024 2048 4096		cpr
RES_{INC_DEC}		Decimal Mode Counts per 1 coil period (programmable)		500 1000 2000 4000		cpr
ACC	Position Accuracy UART, ABI, Step/Dir, I2C	Ambient Temperature, Nominal Supply	-0.1		0.1	%FS
		Over temperature and supply range	-0.2		0.2	%FS
t_{POS}	Position refresh rate	Internal Refresh rate of position information	4		6	µs

Table 6. Non-volatile Memory Parameters [1]

Parameter	Conditions	Minimum	Typical	Maximum	Units
Data retention	Qualified according to JEDEC 22-A117	15 @T_J = 100°C			Years
	Over product lifetime		>100 @T_J = 25°C		
Write temperature	Allowed ambient temperature range for read and write access	-40		125	°C
Read temperature		-40		125	ºC
Endurance [2]	Over product lifetime			1000	NVM Write Cycles
Read Cycles		5x 10^{11}	1x 10^{12}		NVM Read events

[1] Guaranteed by memory supplier

[2] Verified number of program/erase cycles. Qualified with 2000 cycles.

Table 7. LC Oscillator Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{LC}	Excitation frequency	LC oscillator frequency is determined by external components L and C	2		5.5	MHz
R_{Peq}	Equivalent parallel resistance of the LC resonant circuit		250			Ω
V_{TX_PP}	LC oscillator amplitude at VDD = 5.0V ±10%	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. Adjustable by coil current.			6.4	Vpp
	LC oscillator amplitude at VDD = 3.3V ±10%				5.7	
I_{LC}	Programmable transmitter coil drive current	$T_{ambient}$ = -40 to +125°C	0	[1]	16	mA
R_{Tx1}, R_{Tx2}	LC oscillator series resistors	Depending on coil design and excitation frequency (f_{LC})		10		Ω

[1] The required transmitter coil current is determined by the equivalent parallel resistance of the LC circuit, depending on coil design.

Table 8. Receiver Coils Front-End Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{RX}	RX coil amplitude	Differential coil input	5		200	mV_{pp}
A_{IN_mm}	Maximum amplitude mismatch correction	Programmable gain mismatch correction of RX coil signals (SIN and COS)			15	%
$A_{IN\_OFFS\_RANGE\%}$	Input offset correction range	Differential input offsets of sine or cosine signal, percentage of transmitter coil amplitude.	-0.2		0.2	%
D_{OFFSET}	Coil input offset temperature drift	Over temperature range T_{AMB}	-2.5		2.5	%
C_{RX1} to C_{RX8}	Receiver input filter capacitors	For improved EMC immunity		220		pF
$Noise_{SP}$	Signal path noise level	Digital filtering = OFF V_{RX}= 50mV			0.1	° el. rms
		Digital filtering = OFF V_{RX}= 5mV			0.5	° el. rms

2.4 Interface Pin Characteristics

Table 9. UART Interface

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{OL_UART}	Output low voltage	3mA sink current, VDD = 3.0 to 5.5V OUT1 pin 13 OUT2 pin 12	0		0.4	V
V_{OH_UART}	Output high voltage	3mA source current, VDD = 3.0 to 5.5V OUT1 pin 13 OUT2 pin 12 (Push-Pull condition)	0.8 × VDD		VDD	V
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold	OUT2 pin 12	8			mA
$I_{OUT2\ sc\ lim}$	OUT2 output short current limitation[1]	OUT2 pin 12 Short to VDD, GND VDD = 3.0 to 5.5V Open Drain mode	14		26	mA
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold	OUT1 pin 13	35			mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation[2]	OUT1 pin 13 Short to VDD, GND VDD = 3.0 to 5.5V Push-pull mode	28			mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation[2]	OUT1 pin 13 Short to VDD, GND VDD = 3.0 to 5.5V Open Drain mode	28		56	mA
V_{IL_UART}	OUT1 low level input voltage	VDD = 5V	-0.3		0.2 × VDD	V
		VDD = 3.3V	-0.3		0.3 × VDD	V
V_{IH_UART}	OUT1 high level input voltage	VDD = 5V	0.7 × VDD		VDD + 0.3	V
		VDD = 3.3V	0.7 × VDD		VDD + 0.3	V

[1] With OUT2 drive strength set to “00” and OUT2 drive strength for open drain disabled. (out2_io1_drv = “00”)

[2] With digital mode configuration (out1_drv=”10”)

Table 10. I2C Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{I2C}	I2C clock rate				400	Kbit/s
t_{SCL_LOW}	Low level state of SCL clock	Normal mode	4.7			µs
		Fast mode	1.3			µs
t_{SCL_HIGH}	High level state of SCL clock	Normal mode	4.0			µs
		Fast mode	0.6			µs
$t_{R\_SDA\_SCL}$	Rise time of SDA/SCL (30% to 70%) $R_{SDA/SCL}$=2kΩ	Normal mode			1000	ns
		Fast mode	20		300	ns
$t_{F\_SDA\_SCL}$	Fall time of SDA/SCL (70% to 30%) $R_{SDA/SCL}$=2kΩ	Normal mode	20		300	ns
		Fast mode	20			ns
V_{IH_I2C}	High level input voltage	SCL clock input, SDA data input	0.7× VDD		VDD+0.5	V
V_{IL_I2C}	Low level input voltage		-0.5		0.3× VDD	V

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
		DIN, ADR0, ADR1				
V_{I2C_hyst}	Hysteresis of Schmitt trigger input	SCL clock input SDA, DIN, ADR0, ADR1	0.05 × VDD			V
I_{LEAK}	Input leakage current	VDD = 0V to 5.5V	-10		10	µA
$I_{SDA\ lim\ thr}$	SDA current limitation threshold	OUT2 pin 12 (SDA)	8			mA
$I_{SDA\ sc\ lim}$	SDA output short current limitation[1]	Short to VDD, GND VDD = 3.3V, 5V	14		26	mA
V_{OL_SDA}	Output low voltage SDA low level output voltage open drain	3mA sink current VDD = 3.0 to 5.5V	0		0.4	V
I_{OL}	Low level output current	V_{OL} = 0.4V, VDD=5.5V, $R_{SDA/SCL}$=2kΩ	3			mA
t_{SP}	Input spike suppression	Spikes shorter than t_{SP} are suppressed	400		426	ns
C_B	External capacitive load for each bus line				400	pF
R_{SDA}, R_{SCL}	External pull-up resistor at pins SDA and SCL	Resistor value and capacitive load on these pins are limiting the maximum clock frequency	1.8	4.7		kΩ
R_{ADR}	External resistor at pin ADR for I2C address selection	Pull-up/pull-down, depending on I2C address setting.	1.8	4.7		kΩ
$I_{DOUT\ lim\ thr\ I2C}$	DOUT current limitation threshold[2]	OUT1 pin 13 in overload condition	35		56	mA
$I_{DOUT\ sc\ lim\ I2C}$	DOUT output short current limitation[2]	OUT1 pin 13	28		58	mA

[1] With OUT2 drive strength set to “00” and OUT2 drive strength for open drain disabled. (out2_io1_drv = “00”)

[2] With digital mode configuration (out1_drv=”10”)

Table 11. Incremental Interfaces Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{inc}	Single channel Pulse Rate	ABI Step/Dir interfaces			2	MHz
V_{OH_inc}	Output high voltage ABI -Step /Dir	3mA source current, VDD = 3.0 to 5.5V Pin 13 (OUT1) Pin 12 (OUT2) Pin 10 (IO1)	0		0.4	V
V_{OL_inc}	Output low voltage ABI -Step /Dir	3mA sink current, VDD = 3.0 to 5.5V Pin 13 (OUT1) Pin 12 (OUT2) Pin 10 (IO1)	0.8 × VDD		VDD	V

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
$I_{OUT2\ IO1\ lim\ thr}$	Current limitation threshold A,B / Step, Dir pins	Pin 12 (OUT2) Pin 10 (IO1) in overload condition	6			mA
$I_{OUT2\ IO1\ sc\ lim}$	Output short current limitation [1] A,B / Step, Dir pins	Pin 12 (OUT2) Pin 10 (IO1) Short to VDD / GND VDD = 3.3V,5V	32		70	mA
$I_{OUT1\ lim\ thr}$	Current limitation threshold [1] Index pin	Pin 13 (OUT1) in overload condition	35			mA
$I_{OUT1\ sc\ lim}$	Output short current limitation [1] Index pin	Pin 13 (OUT1) Short to VDD / GND VDD = 3.3V,5V	28		58	mA
t_{r_local}	Output rising edge embedded applications	Load capacitance 60pF Output voltage rising from 10% to 90% VDD = 3.0 to 5.5V			55	ns
$t_{f\ local}$	Output falling edge, embedded applications	Load capacitance 60pF Output voltage falling from 90% to 10% VDD = 3.0 to 5.5V			55	ns
$t_{r\ remote}$	Output rising edge remote applications	Load capacitance 4.7nF Output voltage rising from 10% to 90% VDD = 3.0 to 5.5V			4	us
$t_{f\ remote}$	Output falling edge remote applications	Load capacitance 4.7nF Output voltage falling from 90% to 10% VDD = 3.0 to 5.5V			4	us

[1] With digital mode configuration (out1_drv="10").

[2] With OUT2 fast configuration (out2_io1_drv="11")

3. Detailed Description

3.1 Overview

The RAA2P3226 sensor IC consists of one transmitter coil and two pairs of receiver coils, which are typically designed as traces on a printed circuit board. The receiver coils are designed as two wire loops with anti-serial connection. The “sine” coil and the “cosine” coil are shifted by 90 electrical degrees. A metal target is placed above the coil arrangement.

RAA2P3226 IC supports two sets of independent receiver coils enabling dual track high resolution designs.

When the IC drives an AC current into the transmitter coil, it generates an alternating magnetic field. This magnetic field induces secondary voltages in the receiver coils. Without a target, the induced voltages in the loops of the receiver coils cancel each other out, resulting in a net receiver voltage of zero.

When a metal target is placed above the coils, the magnetic field generates eddy currents on its surface. These eddy currents create a counter magnetic field, reducing the total flux density underneath. This leads to a reduction in the voltage induced in the receiver coil areas underneath the target, creating an imbalance in the anti-serial coil segment voltages.

For every channel, the IC demodulates, offsets and corrects the amplitude of the signals from the two receiver coils with a 90° electrical phase shift design, which generates sine and cosine shaped voltages as the target is moving

The RAA2P3226 IC amplifies, rectifies, and filters the receiver voltages, converting them into digital representation with an ADC. The digital sine and cosine signals from the two channels are converted into a 0° to 360° absolute position. The signal accuracy can be further enhanced through a 2-dimentional,16-point linearization process.

The absolute position can be read in digital format by UART, ABI, Step/Dir or I2C interface.

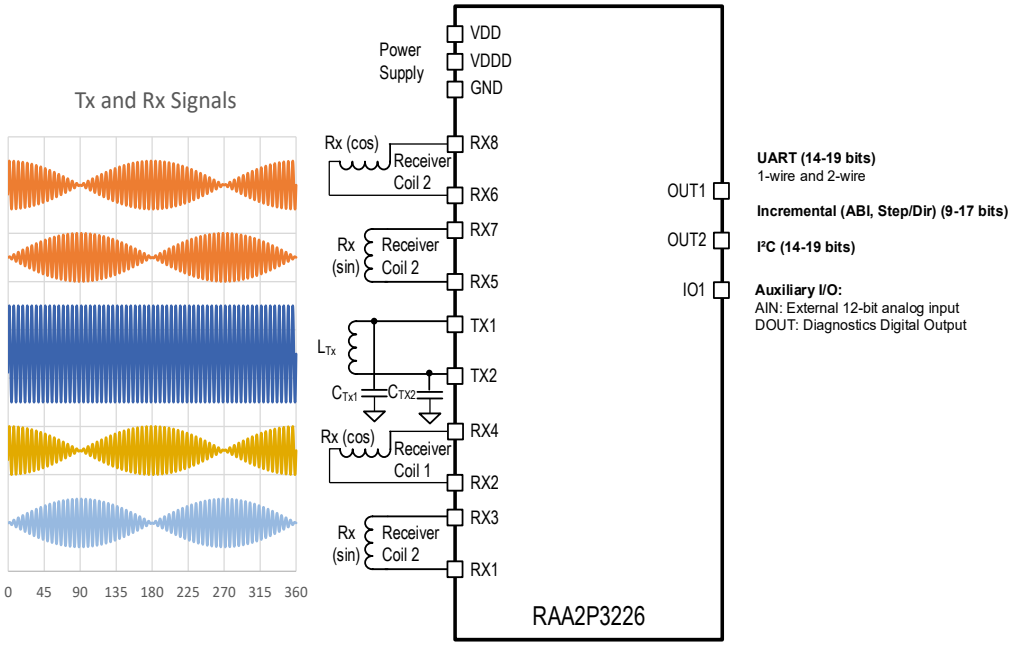


Figure 3. RAA2P3226 Input/Output Signals

3.2 Block Diagram

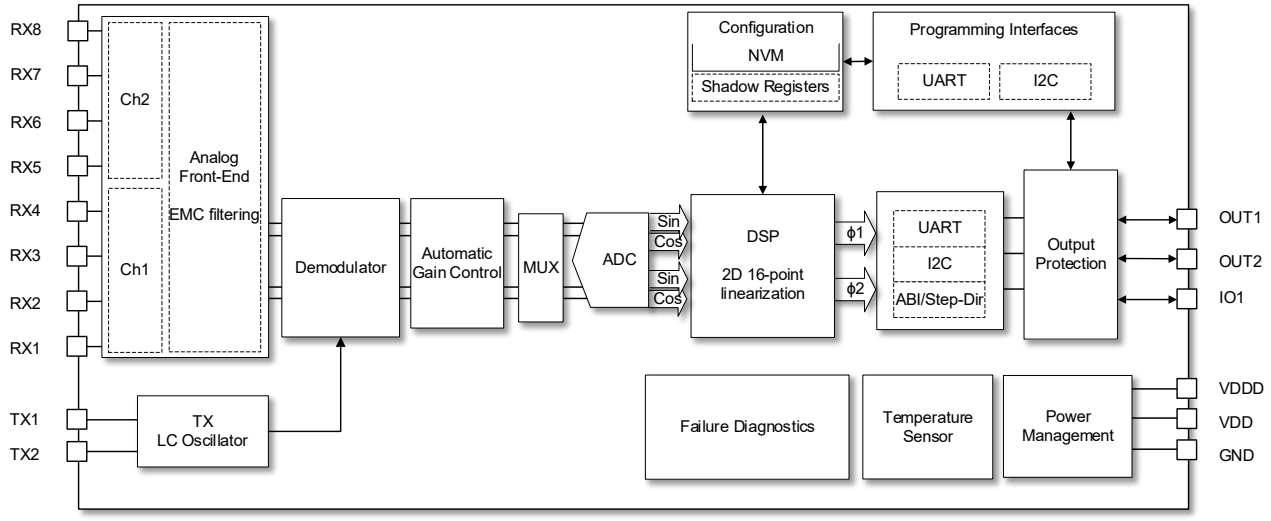


Figure 4. Block Diagram

The main building blocks include:

- Analog front-end: Input filter, offset, and gain control for the receiver signals.
- Input Multiplexer: Sequential selects the different receiver coils and other test signals for further signal processing.
- Demodulator: Converts RF modulated position signal to LF demodulated raw sine and cosine signals.
- Automatic Gain Control: Automatically adjusts raw sine and cosine signal levels.
- MUX: Multiplexer for ADC input.
- High Speed ADC: Converts raw signals into digital format for further processing.
- Digital signal processing: Converts digital sine and cosine raw signals into synchronized absolute position information.
- 2D 16-point linearization: Supports up to 16 two-dimensional linearization points with freely programmable X- and Y- coordinates for each point (X= Position input, Y= Position output).
- Digital Interfaces: Post processing, Delay correction, speed calculation, clamping, signal integrity checks. Decoding of Channel 1 and Channel 2 information and other diagnostics info into the selected output format (UART, ABI, Step/Dir or I2C).
- TX Oscillator: Generates the transmitter coil signal.
- Temperature sensor: Internal temperature sensor used for chip diagnostics.
- Protection: All outputs are fully protected against overvoltage, reverse polarity and short circuit, enabling direct cable connection to these outputs and eliminating the need for additional line driver ICs.
- Power Management: Operates with supply voltages ranging from 3.0V to 5.5V. External capacitors are required for the supply voltage VDD, and for the digital power supply, VDDD. All other supplies, such as the supply for the analog circuits do not need any external capacitor.
- Programming interface: Accessible via single-wire interface, based on a half-duplex UART protocol. If the I2C interface is selected, the NVM programming can also be performed by the I2C interface.
- Configuration, NVM: Stores non-volatile storage for factory and user-programmable settings. User configuration parameters can be programmed multiple times.
- On-chip failure diagnostics: Performs internal diagnosis of critical blocks.
- Auxiliary I/O including AIN (12-bit analog input for external analog signals), DOUT (Diagnostic Output) readable over I2C interfaces.

3.3 LC Oscillator

The transmitter circuit of the RAA2P3226 generates the required RF magnetic field for operating the sensor as determined by an external parallel LC circuit, see Figure 5. To ensure low emission of harmonics, the capacitive part of the LC circuit is split into two equal-value capacitors: CTx1 and CTx2. Additionally, two series resistors RTx1 and RTx2 are added as shown in Figure 5.

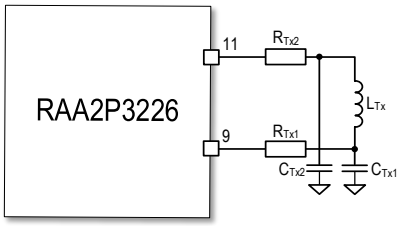


Figure 5. TX LC Oscillator Connection

3.3.1 Parallel LC Resonator Calculations

A resonator, comprising an inductor (L) and a capacitor (C) in parallel, is essential for generating specific frequencies in RF applications. Accurate calculations of the equivalent parallel resistance (R-Peq) ensure proper resonator function. In the RAA2P3226 transmitter circuit, this resonator minimizes harmonic emissions.

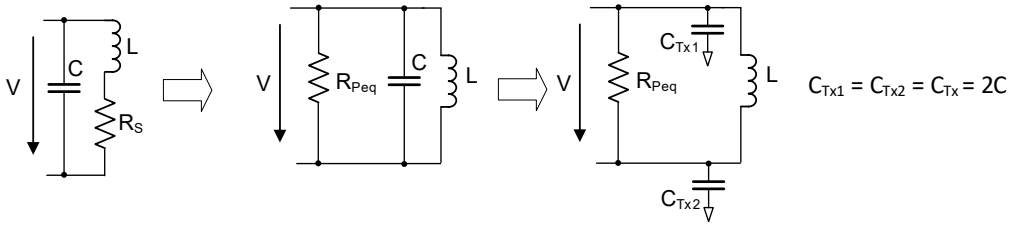


Figure 6. Parallel Resonator Circuit

Equivalent parallel resistance from Coil series resistance:

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C}$$ **Equation 1**

For $C_{Tx1} = C_{Tx2} = C_{Tx} = 2C$:

$$R_{Peq} = \frac{1}{R_S} \times \frac{2 \times L}{C_{Tx}}$$ **Equation 2**

Equivalent parallel resistance from Quality factor Q:

$$R_{Peq} = Q \times \sqrt{\frac{L}{C}} = Q \times \sqrt{\frac{2L}{C_{Tx}}}$$ **Equation 3**

Ideal LC Oscillator frequency with split Tx capacitors C_{Tx}

$$f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{Tx}}{2}}}$$ **Equation 4**

Oscillator frequency with split Tx capacitor C_{Tx} and coil series resistor R_s

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{R_S}{L}\right)^2}$$ **Equation 5**

Oscillator frequency with split Tx capacitor C_{Tx} and equivalent parallel resistor R_{Peq}

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{2}{R_{Peq}C_{Tx}}\right)^2}$$ **Equation 6**

$$Q = R_{Peq}\sqrt{\frac{C}{L}} = \frac{1}{R_S}\sqrt{\frac{L}{C}}$$ **Equation 7**

Coil quality factor

$$Q = \omega\frac{L}{R_S} = 2\pi f_{TX}\frac{L}{R_S}$$ **Equation 8**

Where:

R_{Peq}	Equivalent parallel resistance of the LC circuit at the transmitter frequency in Ohms
R_S	Serial resistance of the transmitter coil at the transmitter frequency in Ohms
f_{Tx}	Resonant circuit frequency in Hertz, 1/s
L	Resonant circuit coil impedance in Henry
C	Resonant circuit capacitance in Farad
C_{Tx1}, C_{Tx2}	Capacitance of the split capacitors in Farad
Q	Resonant circuit quality factor (unitless)
ω	Angular frequency 2*π*f_{Tx} in Hertz, 1/s

3.4 Coil Design

Figure 7 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$V_{Cos\ Loop1} = -V_{Cos\ Loop2}$ **Equation 9**

If no target is present, the secondary voltages cancel each other:

$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} = 0V$ **Equation 10**

With a target placed above the coils, the secondary voltage induced in the covered area is lower than the secondary voltage without a target above it.

$V_{Cos\ Loop1} \neq -V_{Cos\ Loop2}$ **Equation 11**

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage ≠ 0V is generated, depending on the location of the target.

$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} \neq 0V$ **Equation 12**

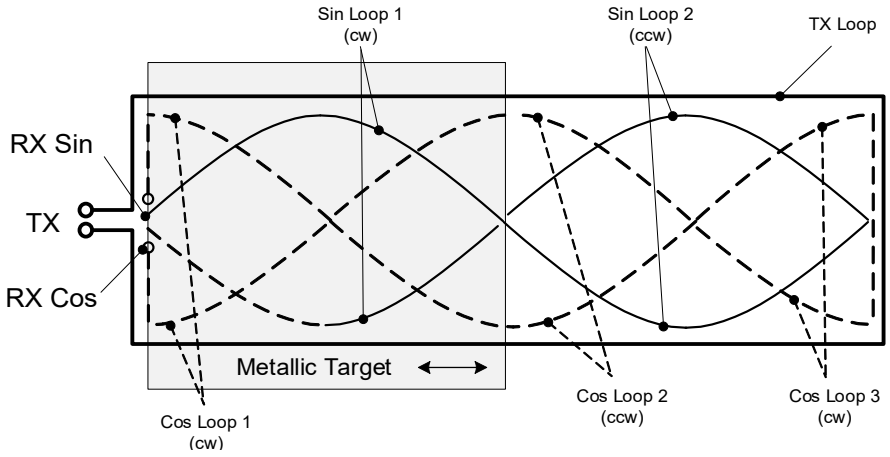


Figure 7. Coil Design for a Linear Motion Sensor

The same principles shown for the linear motion sensor can be applied to a rotary sensor as shown in Figure 8.

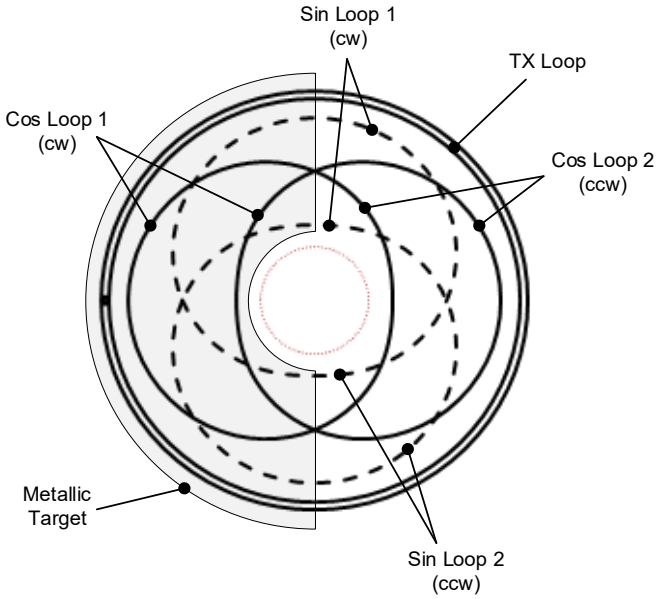


Figure 8. Coil Design for a 360° Rotary Sensor

3.4.1 Multi-periodic Coil Design Application Examples

Applying the same fundamental design principles, coils with multiple periods per turn can be designed. Multi-periodic designs improve mechanical accuracy compared to single-periodic coil designs. For example, a 4-periodic coil design (4 × 90°) improves mechanical accuracy by a factor of 4. Consequently, for angular designs, requiring < 360° movement range, coil designs with multiple periods are recommended. They not only improve mechanical accuracy, but such designs are also more robust towards mechanical target misalignment and tilt.

3.4.2 Electrical versus Mechanical Degrees

The RAA2P3226 converts the movement of a target across a single period of the receiver coil into a precise electrical signal. This conversion spans the full angular range from 0°to 360°, producing a digital output ranging from 0 to (2^N-1) LSBs. The position output is thus absolute over a full turn of 360 mechanical degrees.
As illustrated in Figure 9, the single-periodic coil design establishes a direct 1:1 relationship between electrical and mechanical domains as the following:

- Coil Period: 360° electrical
- Mechanical Range: 360° mechanical
- Conversion Factor: 1:1 (1°el. = 1° mechanical)

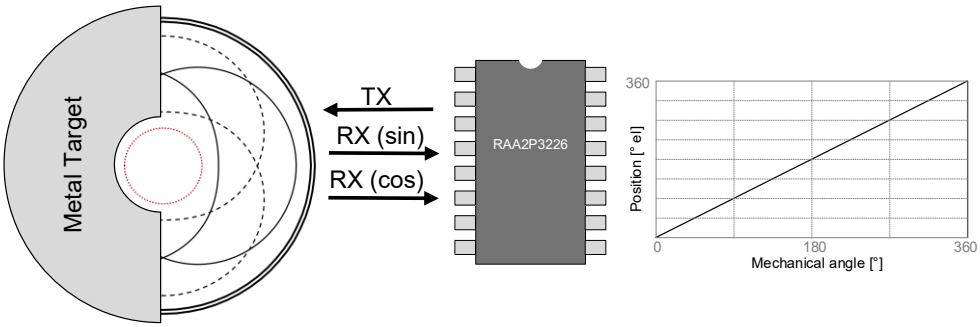


Figure 9. Coil Design Using 1-periodic Coil

As illustrated in Figure 10, a coil design with four receiver coil periods within a single full mechanical turn, results in four electrical rotations for every complete mechanical turn and provides the following advantages in accuracy and resolution.

- Higher Resolution: Position output resolution increases proportionally with period count by

$$\text{Mechanical Resolution} = \text{Sensors\_Periods} * \text{Electrical Resolution}$$

  In this configuration one electrical degree (°el) equals 0.25 mechanical degrees (°). The provided output resolution is four times higher compared to the single-periodic design.

- Improved accuracy: Mechanical error is reduced by the period factor

$$Mechanical\ Error = \frac{Electrical\ Error}{Sensor\ Periods}$$

  This configuration is particularly well-suited for:

  - Multi-pole motors requiring precise commutation
  - Limited-range applications (<180° mechanical travel)
  - Systems demanding high-resolution incremental feedback

Select the number of periods based on application requirements to optimize measurement performance. Proper period selection is critical for achieving maximum system accuracy.

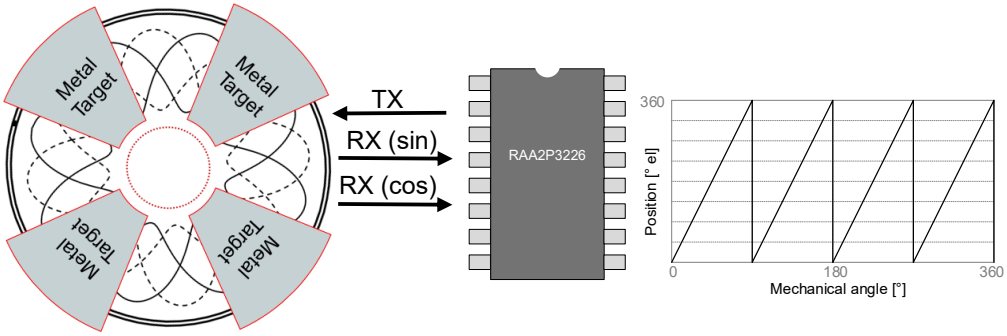


Figure 10. Coil Design Using 4-periodic Coil

3.4.3 Dual Coil High Resolution Mode

The RAA2P3226 is capable of handling two different sets of receiver coils and can be configured in high resolution mode. By defining a specific combination of receiver coils with a varying number of pole pairs on the primary and secondary receivers, the device can calculate position information with high accuracy. The primary coil features multiple periods, while the secondary coil serves as a reference track to identify the correct period of the primary. Two high resolution configurations are available: one track mode or Vernier mode. See Table 12 for configuration options and the resulting resolution.

Table 12. High Resolution Modes

High Resolution Mode	Primary Coil [periods]	Secondary Coil [periods]	Resolution [bits]
One Track Mode	4	1	16
	8		17
	16		18
	32		19
Vernier Mode	4	3	16
	8	7	17
	16	15	18
	32	31	19

By configuring the primary coil to 32 pole pairs, the device reaches its highest achievable resolution: 19 bits for UART and I2C. The maximum achievable resolution on ABI interface is 17-bit and it is provided by configuring 32 periods on the primary coil.

The high-resolution data is stored in two separate registers (hires_lsb 0x028A, hires_msb 0x028C). To ensure the data is consistently and accurately latched, it is essential to access the LSB first, followed by the MSB. Accessing the LSB via the digital interfaces (UART, I2C) freezes the MSB information automatically.

3.4.3.1 One Periodic Reference Track Mode

In this mode, the primary coil can be configured with 4,8,16 or 32 number of periods. The secondary coil serves as a reference track with a single pole pair, see Figure 11.

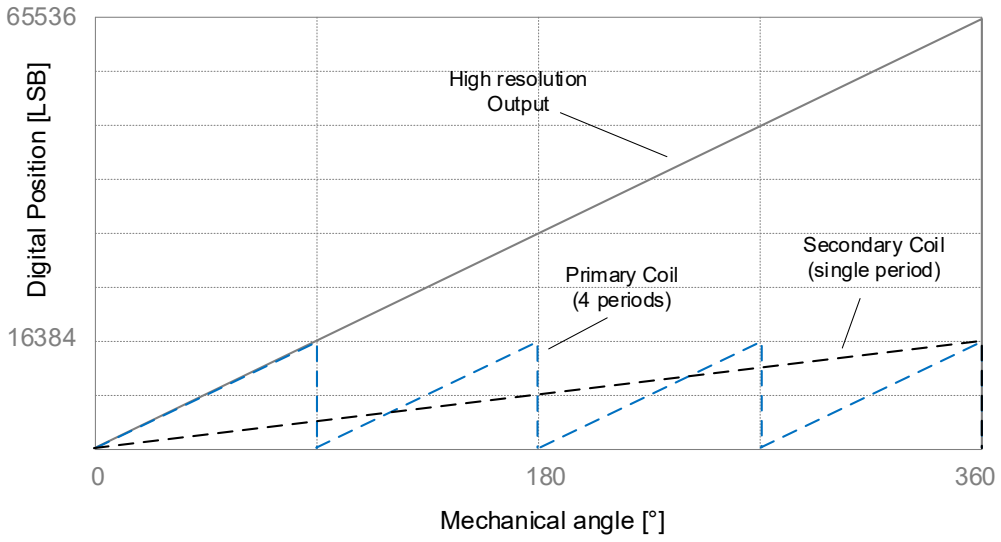


Figure 11. One Track Mode with Single Periodic Reference Track

3.4.3.2 Vernier Reference Track Mode

In Vernier reference track mode, the primary is configured to have 4,8,16 or 32 periods, while the secondary coil has one period less than the primary (3,7,15,31), see Figure 12.

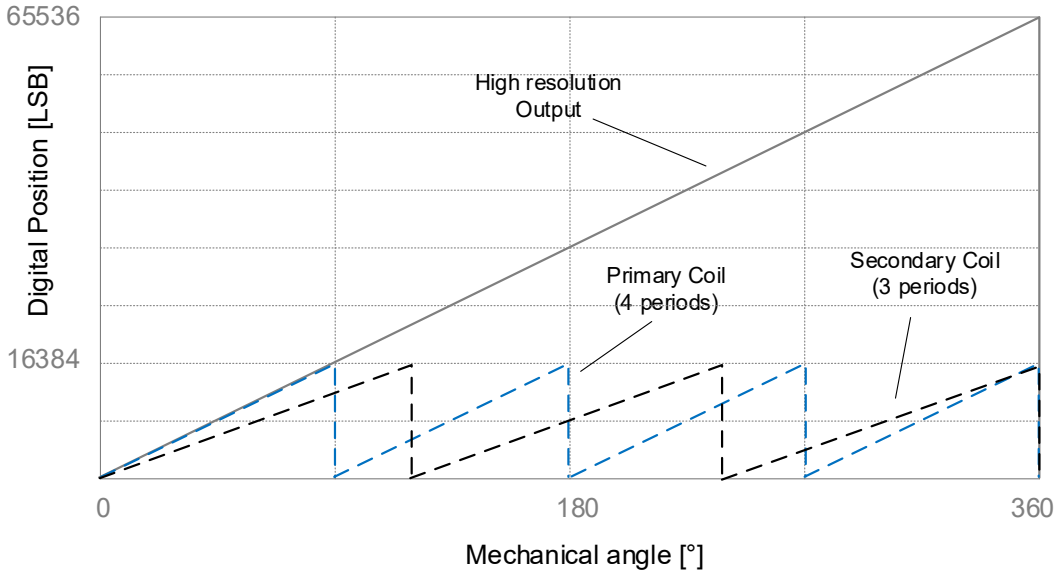


Figure 12. High Resolution Mode with Vernier Configuration

3.4.3.3 Coil Synchronization

Ensuring zero position synchronization between the primary and secondary coils is critical to avoid sudden jumps in the output position. The maximum allowable shift between the zero positions of the primary and secondary coils depends on the selected configuration for primary coils, as detailed in Table 13.

Table 13. Primary and Secondary Coils

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Z_{Sync}	Zero position shift between primary and secondary coil.	Primary coil periods = 4	-45		45	°mechanical
		Primary coil periods = 8	-22.5		+22.5	°mechanical
		Primary coil periods = 16	-11.25		+11.25	°mechanical
		Primary coil periods = 32	-5.625		+5.625	°mechanical

4. Linearization

The RAA2P3226 offers a very flexible linearization feature to enhance sensor accuracy. The linearization algorithm is applied digitally after the angle calculation. The linearization is performed with 16-bits resolution over a 360° electrical range (el.). Up to 16 programmable linearization points can be positioned within a grid of 0.088° in both X (position) and Y (expected output) directions and must be shared between primary and secondary coils.

Figure 13 illustrates an example of the impact of linearization, showing that the total error is significantly reduced.

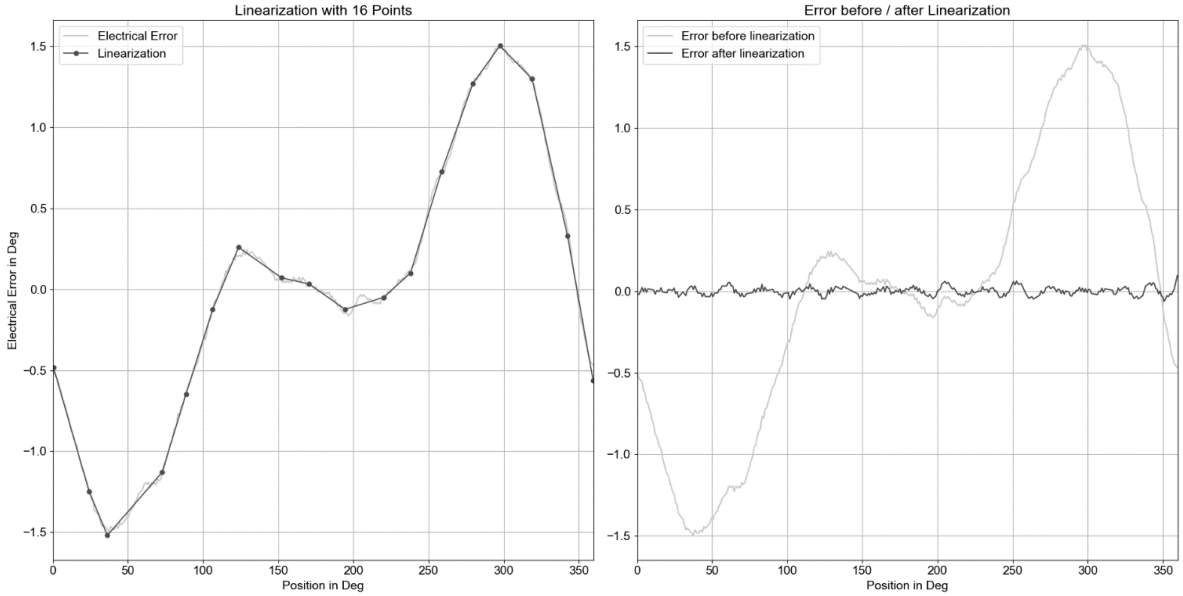


Figure 13. Example of a 16-point Linearization

Table 14. Linearization Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
N_{P_Lin}	Number of linearization points				16	
$Grid_{LIN}$	Placement grid of linearization points	In X and Y		0.088		°el
Res_{Lin}	Resolution of linearization transfer function	X and Y coordinates		12		bits

Note: The slope of each segment (ΔY / ΔX) is automatically calculated from the X and Y parameters of adjacent linearization points. If two adjacent points are positioned with a slope outside the specified range (see Table 14), the slope is reset to 0 to prevent an overflow of the calculated slope value.

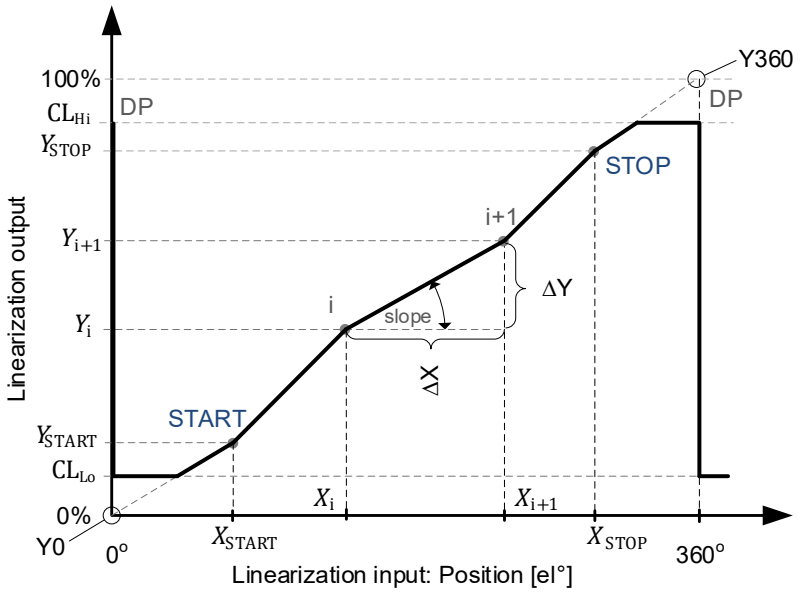


Figure 14. Linearization Transfer Function Parameters

Table 15. Linearization Parameter Settings

Parameter	Description	Programming Options	Resolution
P_{Lin}	Number of total linearization options [1]	Up to 16 points can be assigned to the primary and secondary coils in multiple combinations	
D_P	Discontinuity point, Zero position transition from 0°/360°	0° to <360° el.	0.088°el. / LSB
X_{Start}	Mechanical start position, first linearization point		
Y_{Start}	Expected output at XStart, first linearization point		
X_i	Mechanical position of linearization point (i =1 to 16, including start and stop)		
Y_i	Expected output at linearization point (i =1 to 16 including start and stop)		
X_{Stop}	Mechanical end position, last linearization point		
Y_{Stop}	Expected output at XStop, last linearization point		
CL_{Hi}	Output Clamping level, high	0% to 100% VDD	12 bits (VDD / 4096) / LSB
CL_{Lo}	Output Clamping level, low		
Y0	Position at DP, start value at X=0°	0° / 360° el.	
Y360	Position at DP, stop value at X=360°	0° / 360° el.	

[1] Up to 16 Linearization points can be shared between both coil sets. Several options are possible, for example, 8+8 configuration reserves 8 linearization points for the primary coil and 8 points for the secondary. For more information, see the *RAA2P3226 Programming Manual* document.

5. Interfaces

The RAA2P3226 offers an UART interface operating at up to 2Mbit/s and an I2C that can reach 400 KHz. A summary of the maximum speed for each high-speed interface is shown in Table 16.

Table 16. Interfaces Overview

Interfaces	Number of I/f Wires	Resolution	Features	Other options
UART	1 or 2	14-19 bit	▪ Speed ≤600 krpm, max. 2Mbit/s 92-bit frame, ≤21.7kHz frame rate (1 register read/write, 2 registers fast read)	▪ Half duplex, 1 or 2 wire interface, ▪ Supporting parallel connection up to 4 slaves, ▪ Auto baud rate adaptation ▪ Digital Output (pin 12) (single wire only) ▪ Analog Input (pin 10)
ABI Step/Direction	3	9-17 bit	▪ Maximum. edge rate = 8MHz ▪ See Table 26	▪ Configurable binary and decimal based resolution
I2C	2	14-19 bit	▪ Interface speed: 400KHz ▪ Position update rate: 2.7 KHz	Digital output (pin 13)

5.1 High Speed UART Interface

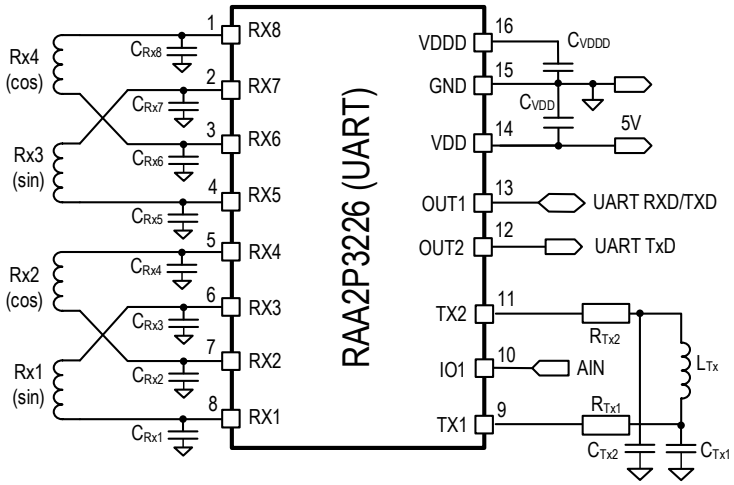


Figure 15. UART Interface with Dual Coil Input/Output Pins

The UART interface can be configured in the following modes:

- single wire bidirectional
- dual wire unidirectional
- dual wire differential bidirectional

Note: all UART modes operate in half duplex data transmission.

Table 17. UART Operation Modes

Operating Mode	OUT1 (Pin 13)	OUT2 (Pin 12)
Single wire bidirectional	RxD/TxD	Not Used
Dual wire unidirectional	RxD/TxD complementary	TxD
Dual wire differential bidirectional	RxD	TxD

Table 18. UART Interface User Programming Options

UART Programming Parameter	Number of Options	Programming Option
UART output drive	2	Open drain or push-pull
UART slave address	4	2 LSBs of general slave address
UART Baud rate [1]	6	{9600, 57600, 115200, 230400,1M,2M} bit/sec
UART operation mode	3	See Table 17
UART error warnings	7	Baud rate, framing, CRC errors

[1] Maximum data rate may be reduced by external capacitive and resistive loads when open drain configuration is used.

5.1.1 Single Wire Bidirectional UART

In single wire UART mode, the device communicates with the ECU using only OUT1 pin, which can be configured in either push-pull or open drain mode. This mode is suitable for point-to-point connections where one device interfaces directly with an ECU (Figure 16) or for implementing a multi-slave single bidirectional wire connection. (Figure 17).

In open drain mode, a single Master can address up to four sensors over a single wire, communicating with one sensor at a time. Each sensor is identified by its slave address, stored in the NVM.

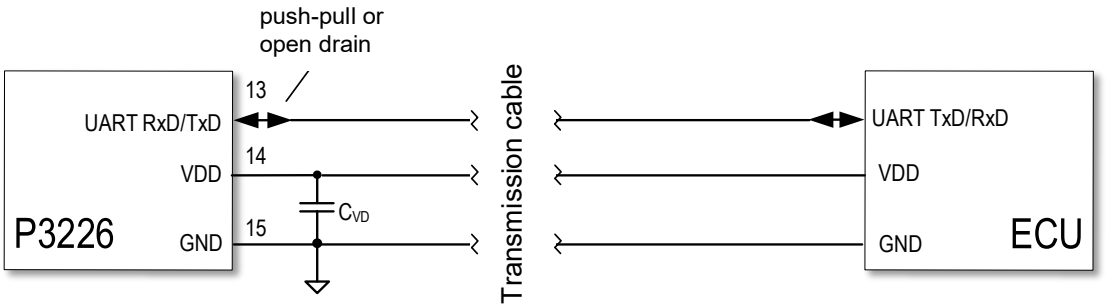


Figure 16. UART Point-to-Point Single Wire Bidirectional Connection

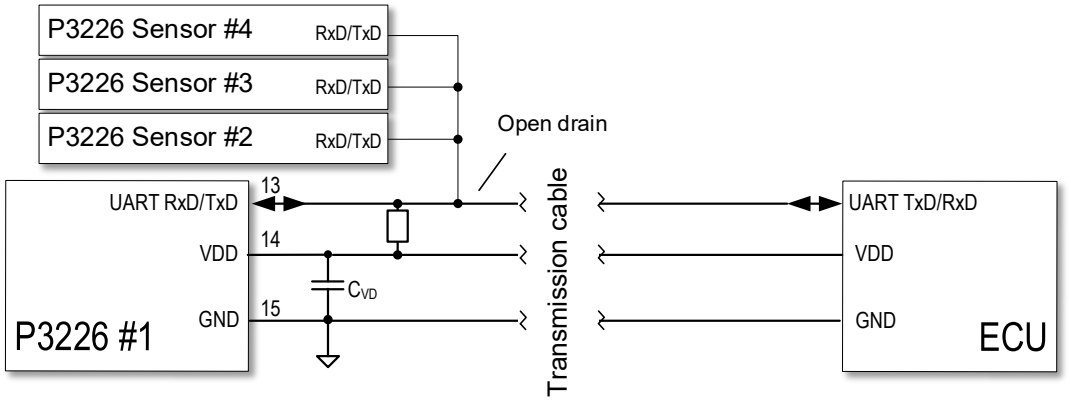


Figure 17. UART Multi-Slave Single Wire Bidirectional Connection

5.1.2 Dual Wire Bidirectional UART with Pseudo-Differential TX

In dual wire UART mode, the device uses both OUT1 and OUT2 pins for communication. A point-to-point connection can be implemented as shown in Figure 16. This communication mode employs OUT1 as a single wire transceiver. (Figure 18).

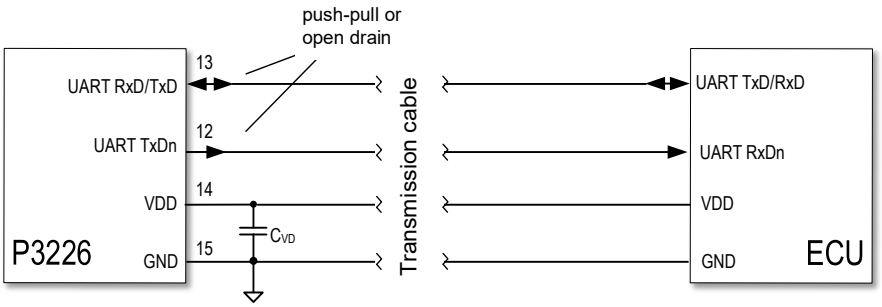


Figure 18. UART 2-Wire Point-to-Point Connection with Pseudo-Differential TX

In addition, OUT2 (pin 12) is used as the transmitter and OUT1 (pin 13) is used for both transmitting and receiving. OUT1 carries inverted information of the transmitted data, creating a pseudo differential signal for more reliable data transmission. During reception, OUT1 is kept in high state.

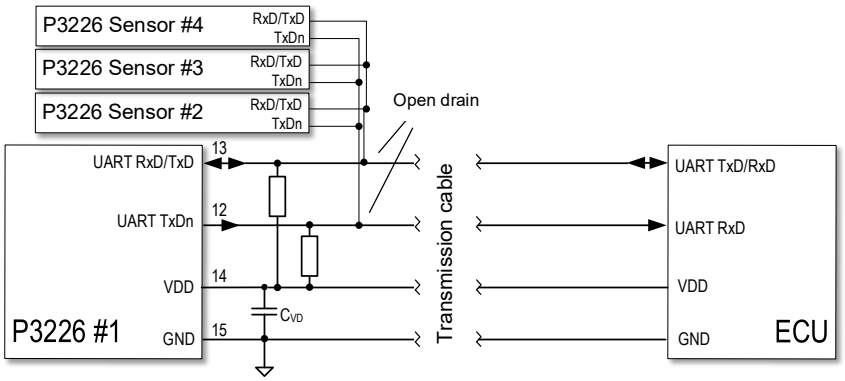


Figure 19. UART 2-Wire Connection with Pseudo-Differential TX and Multiple Slaves

In pseudo-differential mode, with open drain configuration, a single Master can address up to four sensors, communicating with one sensor at a time. Each sensor is identified by its slave address, stored in the NVM.

5.1.3 Dual Wire Unidirectional UART

In this dual wire mode, separate unidirectional lines are used for transmitting and receiving data. The transmitter can be configured either for push-pull or open-drain output. Push-pull mode is recommended for achieving data rates up to 2Mbit/s. In open-drain mode, data rates may be limited, depending on the capacitive load on the transmission cable and the resistance of the pull-up resistor.

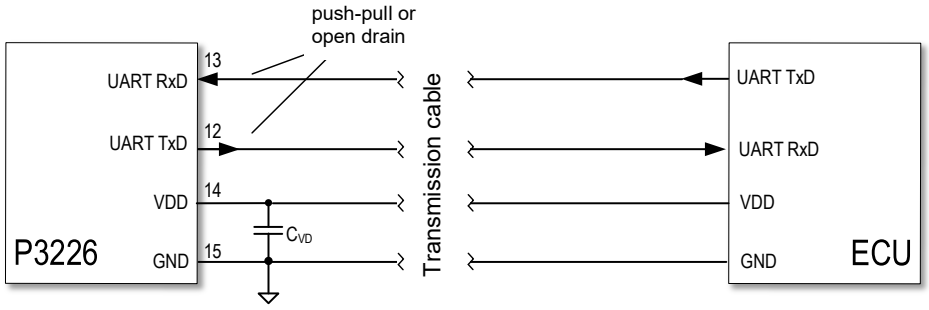


Figure 20. UART 2-wire Unidirectional Connection

In dual wire unidirectional mode, a single Master can address up to four sensors, communicating with one sensor at a time. Each sensor is identified by its slave address in the NVM. When connecting multiple sensors in parallel on the same line, the transmitter output (TxD) must be configured for open drain output.

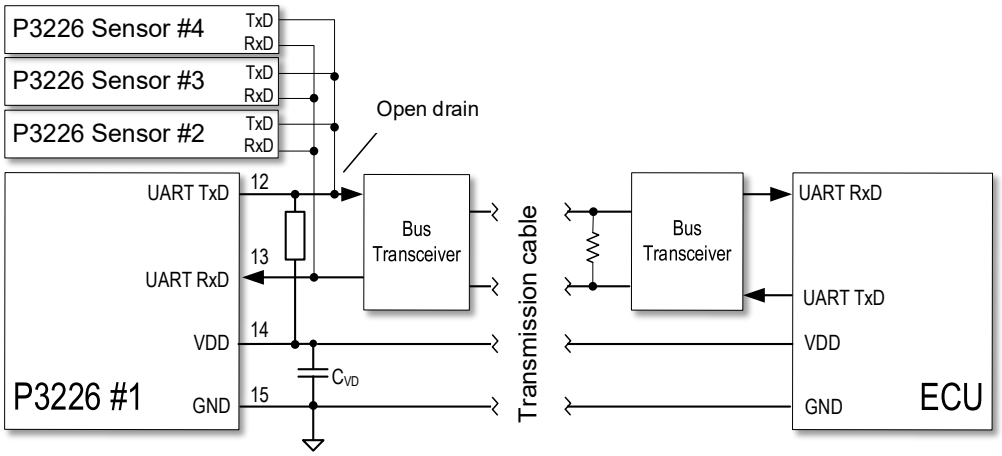


Figure 21. UART 2-Wire Unidirectional Connection with Multiple Slaves and Bus Transceivers

The transmission cable can be extended with external bus transceiver circuits as shown in Figure 21, providing extra robustness and low capacitive load for the UART TxD output pin, enabling high data rates up to 1Mbit/s.

5.1.4 UART Operating Commands

The RAA2P3226 provides the following UART operating modes:

- 16-bit register write (Figure 22)
- 16-bit register read (Figure 23)
- Fast read mode of two registers within one frame with 12,14 or 16 bits of data per register

5.1.4.1 Gap Time

A minimum pause (gap) time is implemented between messages to ensure the controller returns to an idle state before the next communications. The minimum gap time for each UART baud rate configuration is shown in Table 19.

Table 19. UART Wait Time between Measurements

UART Baud Rate [bits/sec]	Minimum Gap Time [bits]
9600, 57600, 115200, 230400	10
1M, 2M	12

5.1.4.2 UART Register Write

This mode writes one register per frame. Each frame consists of 8 bytes, each accompanied by a start and stop bit, resulting in 8x10bits. A short wait (gap) time is required between each frame to ensure proper data transmission. The frame structure permits write access for all bytes, with the data being transmitted from the master to the chip.

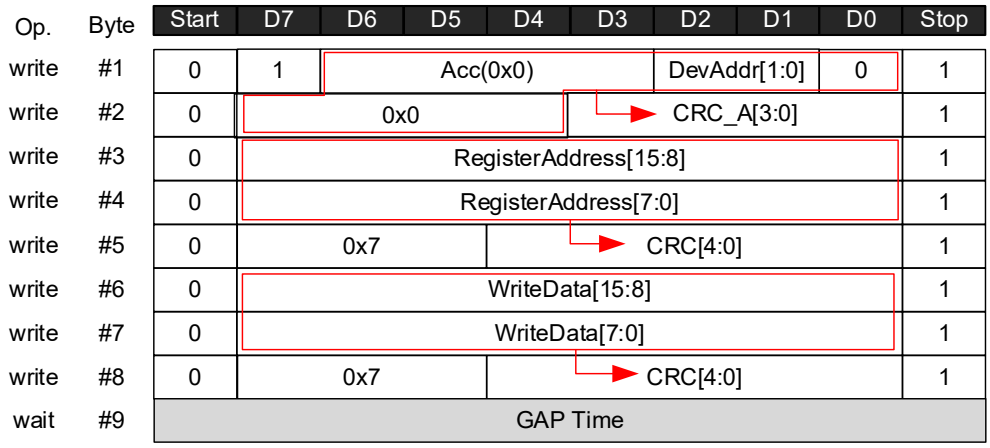


Figure 22. UART Register Write Mode

See the write frame structure on Figure 22 where:

- *Acc*: Access type 0x0 for register write.
- *DevAddr*: the device address if several sensors are connected in parallel, it defines their slave address (0x1-0x3) Default value is 0x0.
- *Register Address*: The target register.
- *Write Data*: The data to be written.
- *CRC*: Cyclic redundancy check.

5.1.4.3 UART Register Read

In read mode, the device reads one register per frame. The first 5 bytes are sent from master to the chip, while on bytes 6 to 8 are read from the chip. In all modes, the bit order is MSB to LSB. Each read frame contains 8 bytes, each with a start and stop bit, resulting in 8x10 bits. A short wait (gap) time is required between each frame.

For performing a data read operation, due to the generation of the differential start and stop bits, an additional wait bit must be added by the master when switching from sending data to receiving data. This results in each frame containing either 91 bits (for data rates up to 230.4 kbit/s) or 93 bits (for 1Mbit and 2Mbit data rates).

In register read mode, an additional wait bit must be added at the end of byte 5 before the chip can start transmitting data (start bit of byte 6). The *ReadData* content is latched at the stop bit of byte 5.

To ensure the accurate reading of high-resolution data, it is essential to begin by reading hires_lsb register first. This operation locks hires_msb that needs to be read subsequently.

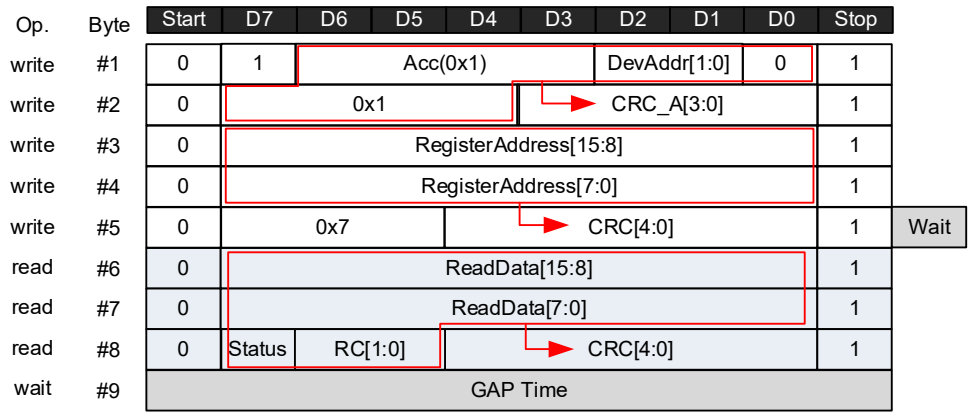


Figure 23. Register Read Mode Frame

See the read frame structure on Figure 23 where:

- *Acc*: Access type 0x1 for register read.
- *DevAddr*: the device address if several sensors are connected in parallel, it defines their slave address (0x1-0x3) Default value is 0x0.
- *Register Address*: the target register.
- *Read Data*: the data contents of the target register.
- *CRC*: cyclic redundancy check.
- *Status*: 1 bit status flag information of the sensor (0: normal operation, 1: error)
- *RC*: rolling counter, a counter that increments with each frame and wraps around 0 when overflowing.
- Wait: 1 bit wait time for master before receiving data (in pseudo-differential mode only).

5.1.4.4 UART Fast Two-Register Read

This mode enables a fast reading of a specific subset of two registers within each frame. The first two bytes of the frame allow the user to specify which subset of the two pre-defined registers to read, using a 4-bit access code. This is achieved by setting the access type on the *Acc1* and *Acc2* bitfields (see Table 20). The readout data for the first register is contained in bytes 3 to 5 while bytes 6 to 8 contain the data for the second register.

Table 20. UART Fast Access Mode

Acc Type1/2	Byte 3 / Byte 6	Byte 4 / Byte 7	Byte 5 / Byte 8		
2	PC sensor Data[11:4]	PC sensor Data[3:0] RC[5:2]	S	RC[1:0]	CRC[4:0]
3	SC sensor Data[11:4]	SC sensor Data[3:0] RC[5:2]	S	RC[1:0]	CRC[4:0]
4	PC sensor Data[13:6]	PC sensor Data[5:0] RC[3:2]	S	RC[1:0]	CRC[4:0]
5	SC sensor Data[13:6]	SC sensor Data[5:0] RC[3:2]	S	RC[1:0]	CRC[4:0]
6 (ACC1)	HiRes LSB [13:6]	HiRes LSB [5:0] RC[3:2]	S	RC[1:0]	CRC[4:0]
6 (ACC2)	HiRes MSB[4:0] 0x0	0x0 RC[3:2]	S	RC[1:0]	CRC[4:0]
7	Chip temperature	0x0 RC[5:2]	S	RC[1:0]	CRC[4:0]
8	Analog input [12:5]	Analog input [4:0] 0 RC[3:2]	S	RC[1:0]	CRC[4:0]
9	PWM input data high [15:8]	PWM input data high [7:0]	S	RC[1:0]	CRC[4:0]
10 = 0xA	PWM input data low [15:8]	PWM input data low [7:0]	S	RC[1:0]	CRC[4:0]
11 = 0xB	IRQ status 0 [15:8]	IRQ status 0 [7:0]	S	RC[1:0]	CRC[4:0]
12 = 0xC	IRQ status 1 [15:8]	IRQ status 1 [7:0]	S	RC[1:0]	CRC[4:0]
13 = 0xD	IRQ status 2 [15:8]	IRQ status 2 [7:0]	S	RC[1:0]	CRC[4:0]
14 = 0xE	IRQ status 3 [15:8]	IRQ status 3 [7:0]	S	RC[1:0]	CRC[4:0]
15 = 0xF	IRQ status 4 [15:8]	IRQ status 4 [7:0]	S	RC[1:0]	CRC[4:0]

[1] PC: Primary coil, SC: Secondary coil, RC: Rolling counter, HiRes: High resolution mode

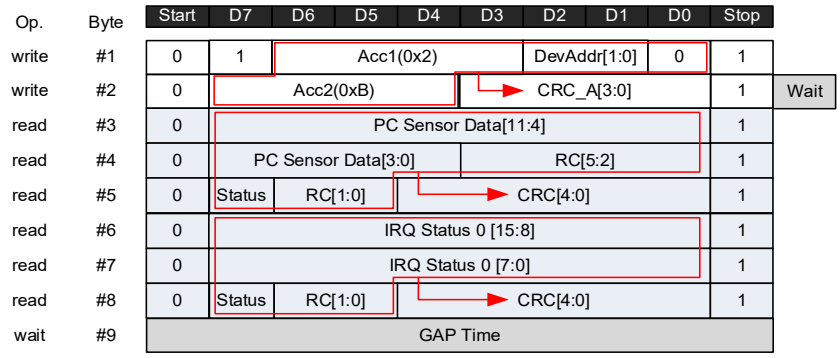


Figure 24. UART Fast Read Mode Example with Different Access Codes

See the frame structure on Figure 24 with an example of reading 12-bit primary coil sensor data (Acc1 = 0x2) and 16-bit IRQ status 0 (Acc2 = 0xB), the frame bitfields are the following:

- *Acc1, Acc2*: Access code: 0x2 to 0xF (see Table 20)
- *DevAddr* : Device address: (default = 0x0. If several sensors are connected in parallel, it defines their slave address (0x1-0x3).
- *CRC*: Cyclic redundancy check.
- *Status*: 1 bit status flag information of the sensor (0: normal operation, 1: error)
- *ReadData*: the data answer from the IC are the PC Sensor Data + RC for Byte #3 and #4 according to ACC1=0x2, while for ACC2=0xB the device provides IRQ_Status on Byte#6 and #7. (See Table 20). The *ReadData* is latched at the stop bit of Byte#2 for Acc1, and at the stop bit of Byte#5 for Acc2.
- *RC*: Rolling counter, a counter that increments with each frame and wraps around 0 when overflowing
- *Wait*: 1 bit wait time for master before receiving data (in pseudo-differential mode only)

In fast read mode, an additional wait bit must be added at the end of byte 2 before the device can start transmitting data.

5.1.4.5 UART Fast Read Mode with Same Access Code

Reading the same register twice provides two results from the same input but at different sampling time stamps. For example, in the configuration shown in Figure 25, the primary coil sensor data is read twice. The first reading (Acc1= 0x2) is sampled at the end of Byte 2, while the second reading (Acc2 = 0x2) is sampled at the end of Byte 5. The interval between these two results is 30 bits of the UART clock (3 bytes, including start and stop bits).

By repeating this sequence, the user can obtain two samples within a 92-bit frame. The timeframe between each consecutive sample is 30 UART clock cycles resulting in 15µs at 2M/s Baud rate. However, the time between each frame is 46µs at the same Baud-rate.

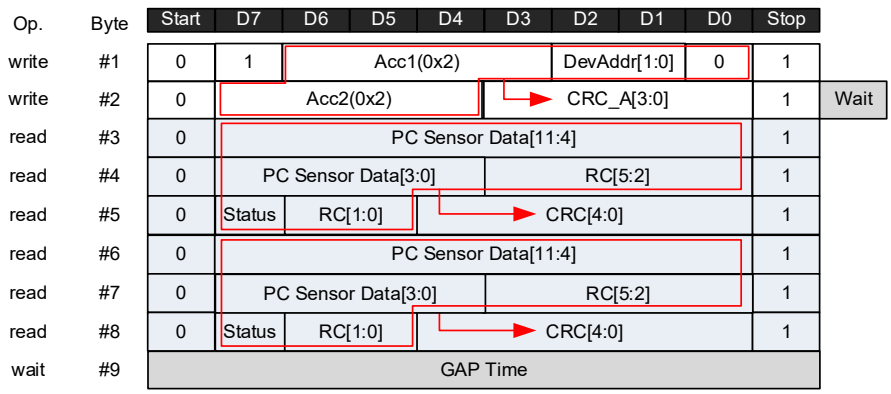


Figure 25. UART Fast Read Mode of the Same Register

5.1.4.6 High Resolution Mode Data

The device can provide high-resolution position information up to 19 bit. This requires two readings from the same access type (*Acc* = 0x6), split into the 14 LSBs and the 5 MSBs of the 19-bit data. In this mode, Bit D0 in byte 1 must be set to 0. The position is latched at the stop bit of Byte 2.

Both *Acc1* and *Acc2* must be set for access type 0x6. Bytes 3 to 8 transmit the full high resolution information including CRC and status bits.

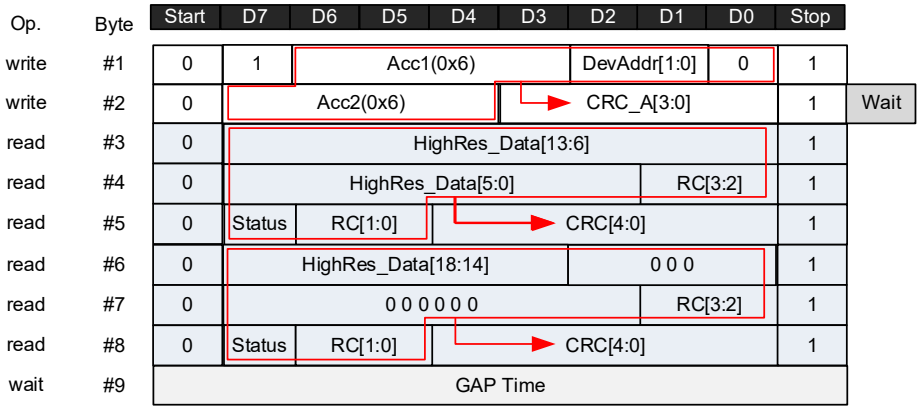


Figure 26. UART Fast Mode: High Resolution Position Information

Refer to Table 21 for a summary of the UART interface speed, based on the selected Baud rate and mode. Note that one frame can perform various operations such as register read, register write, or two consecutive register read (fast read).

Refer to Table 20 for a summary of the UART interface speed, based on the selected Baud rate and mode. Note that each frame can perform various operations such as register read, register write, or two consecutive register reads (fast read).

Table 21. UART Data Access Speed with *uart_start_bit_cfg* = 0

UART Baud rate [bits/sec]	Bits per Frame (incl. Gap Time)	Time per Frame [µs]	Frame Rate [frames/sec]
9600	91	9479.4	105.5
57600	91	1580	633
115200	91	789.9	1265
230400	91	395	2532
1M	93	93	10.75 k
2M	93	46.5	21.5 k

5.2 I2C Interface

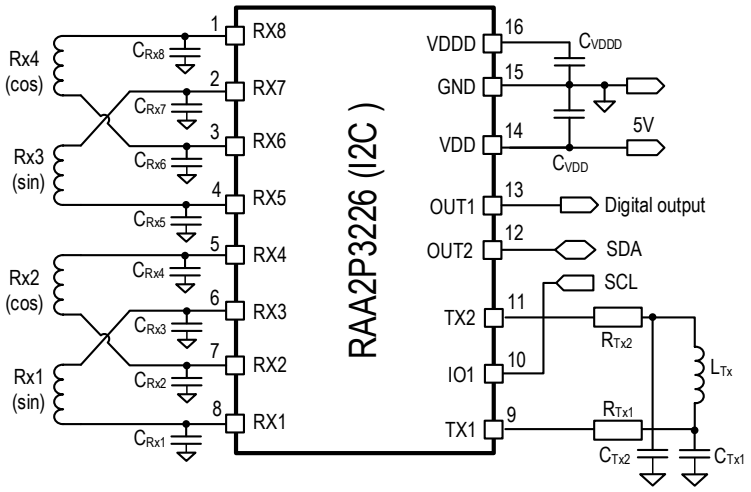


Figure 27. I2C Interface Input/Output Pins

The RAA2P3226 can be programmed for an I2C interface according to the UM10204 I2C-bus specification, utilizing pins 10 (SCL) and 12 (SDA) to address up to 14 slaves over the same 2-wire interface. The interface does not support clock stretching, 10-bit slave address, general call address, software reset, or device ID.

5.2.1 I2C Addressing

In RAA2P3226, two sets of receiver coils are connected. Pins 2 and 3 are used as coil inputs for the secondary coil set, therefore the hardware address selection on these two pins is not available.

If two devices are mounted on the same PCB sharing the same I2C bus, they initially share the same I2C address and cannot be addressed individually by the I2C bus master. To resolve this, the devices must be re-programmed to different I2C addresses.

This can be accomplished by initially enabling single coil inputs and hardware I2C address selection. Individual I2C addresses are set temporarily by forcing the address inputs ADR0 (Pin 2) and ADR1 (Pin 3) of each device to different combinations of VDD or GND (pin strapping). The status of these pins is reflected in I2C Address Bits (see Table 23).

For example, as shown in Figure 28, one device is pin strapped to I2C address 0x72, while the other is pin strapped to address 0x70. Once each device is separately selected, it can be re-programmed for dual coil inputs and unique NVM I2C address.

Table 22. I2C Interface User Programming Options

I2C Programming Parameter	Number of Options	Programming Option
I2C slave address	14	See Table 23
I2C address select by pin strapping	1	Enable/Disable (2 LSBs)
I2C CRC check for Rx data	1	Enable/Disable
I2C CRC check for command data	1	Enable/Disable
I2C protocol error detection	1	Enable/Disable

Refer to Table 23 for the various options available for selecting the I2C address. This can be achieved through combinations of pin addressing and settings in the NVM address register.

Table 23. I2C Address Selection Options in NVM

I2C Address Selection Mode	A6	A5	A4	A3	A2	A1	A0
Default setting	1	1	1	0	0	Pin 3 = ADR1	Pin 2 = ADR0
User programmable range, with I2C address selection by pins 2 and 3	0x02 to 0x1D					Pin 3 = ADR1	Pin 2 = ADR0
User programmable range, with fixed I2C address	0x08 to 0x77						

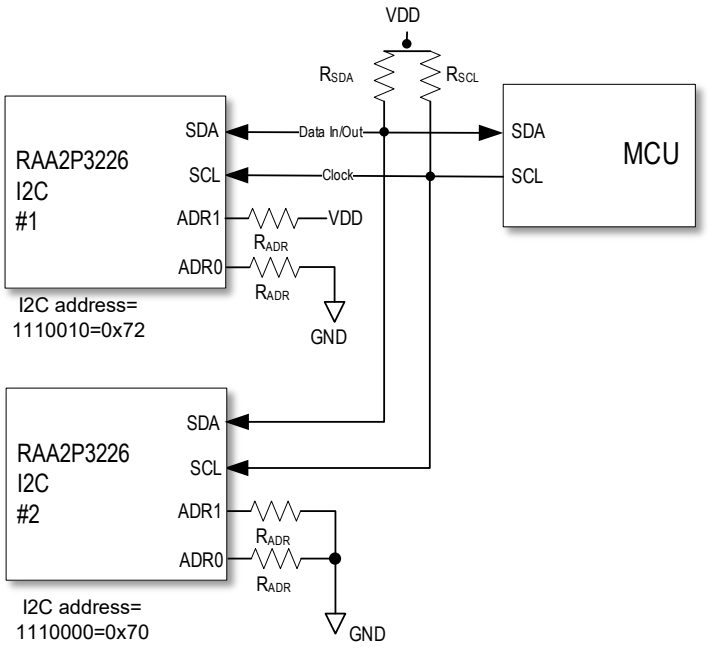


Figure 28. I2C Interface with Address Select

5.2.2 I2C Register Write

To access a register, the slave address must be sent by the master, followed by two bytes of register address (*MemAddr*), one byte of CRC data, and then by the write data *WrData*. If the CRC check is disabled, keep the CRC frame at zero. The write data consists of two bytes of data followed by one byte of CRC data as shown in Figure 29.

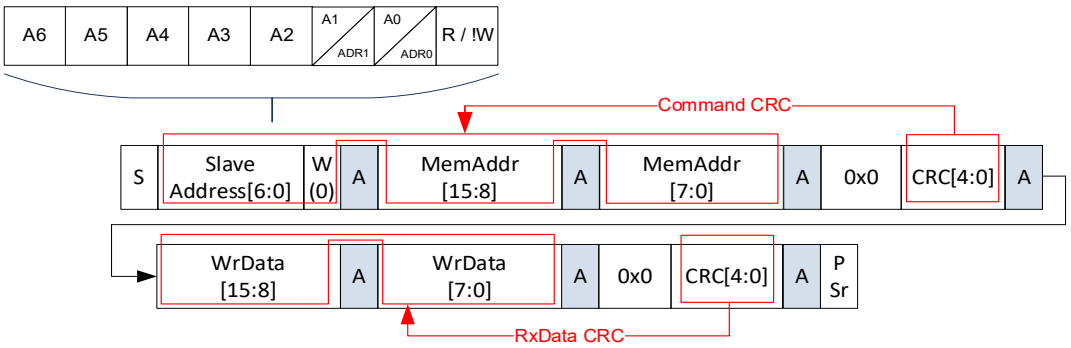


Figure 29. I2C Register Write Access

5.2.3 I2C Register Read

To read a register over the I2C interface, the master sends a write register command frame followed by a repeated start (*PSr*) and slave address with a read bit set. Upon acknowledgement, the device responds with two bytes of data followed by one byte CRC as shown in Figure 30.

To ensure the accurate reading of high-resolution data, it is essential to begin by reading hires_lsb register first. This operation locks hires_msb that needs to be read subsequently.

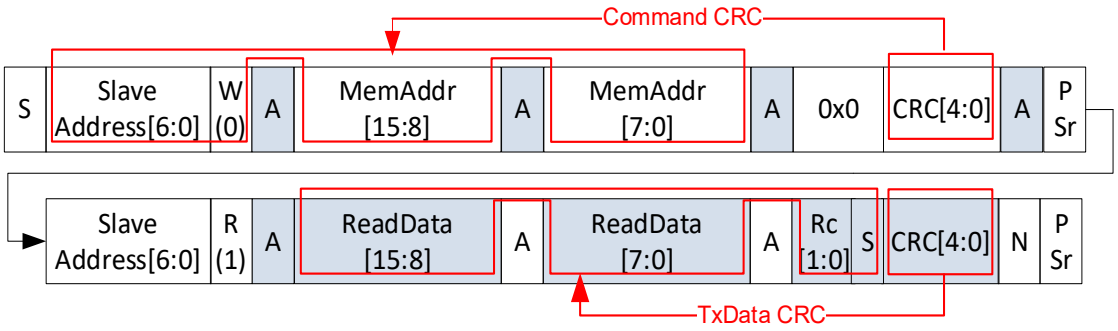


Figure 30. I2C Register Read Access

5.2.4 I2C CRC Check

For optimal communication with the RAA2P3226, it is recommended to enable the CRC check for I2C communication. Enabling it ensures that the device only responds to command frames that include correct CRC data. For more details, see the *RAA2P3226 Programming Manual* document.

5.3 Incremental Interfaces

The RAA2P3226 features incremental interfaces (ABI, Step/Direction), making it ideal for replacing optical and magnetic encoders in industrial applications. Both interfaces use three channels on OUT1, OUT2 and IO1 pins, as shown in Figure 31.

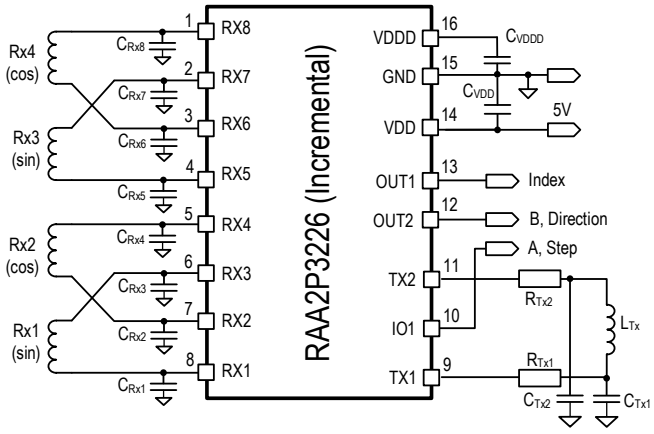


Figure 31. Incremental Interfaces Input/Output Pins

Table 24. Incremental Interfaces Programming Options

Programming parameter	Number of options	Programming option
Incremental mode	2	ABI, Step/Direction
Index pulse length	2	For ABI and Step/Direction mode: 1 LSB, 3 LSBs
Index pulse position	4	For ABI and Step/Direction mode

Programming parameter	Number of options	Programming option
Startup counter burst mode	5	Burst generator disabled If enabled: Frequency of startup burst generator (4)
Startup counter wait time	4	If enabled: wait time of burst generator after POR
Type of interpolation mode	2	Binary, decimal
Incremental resolution	4	Pulses per revolution or counts per revolution, see Table 25
High resolution absolute mode	4	4/8/16/32 periods on primary coil

5.3.1 ABI Interface

In ABI interface decoding, the A and B channels operate in quadrature, toggling a 50% duty cycle, while the I (Index) signal pulses once per revolution to mark the zero-angle position. Each cycle of the quadrature signals A and B contains four distinct states, facilitating precise counting and direction determination.

The counting mechanism increments or decrements the count by four per cycle, corresponding to the edges of channels A and B. As a result, the counts per period is four times higher than the number of pulses per period. Counting direction of the receiving counter is determined by the state of the channels at each edge. During clockwise rotation, a rising edge of channel A occurs when channel B is low. Conversely, during counterclockwise rotation, the rising edge of channel A occurs when channel B is high. RAA2P3226 also allows for the reversal of rotational direction via programming, providing flexibility to meet different application requirements.

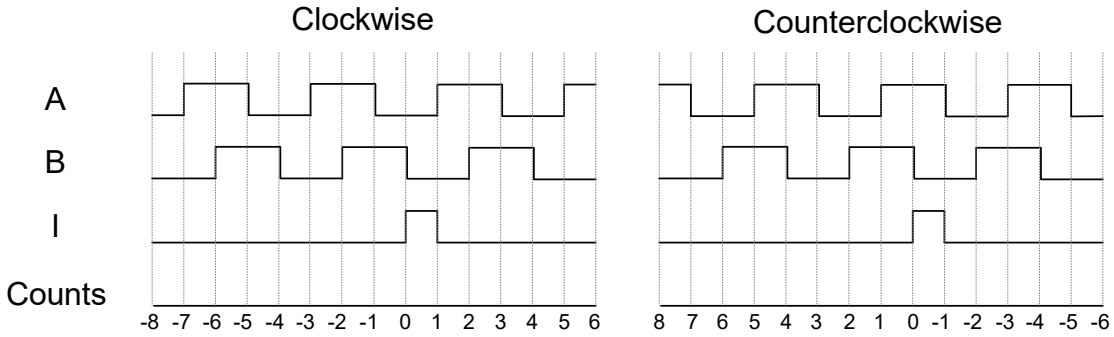


Figure 32. ABI Protocol

5.3.2 Step-Direction

RAA2P3226 can be configurable for Step-Direction protocol, in which one pin (Step) delivers one pulse per count, while the other pin (Direction) is kept high or low according to the rotational direction. As a result, the Step pin delivers double the number of pulses compared to the A pin in ABI mode.

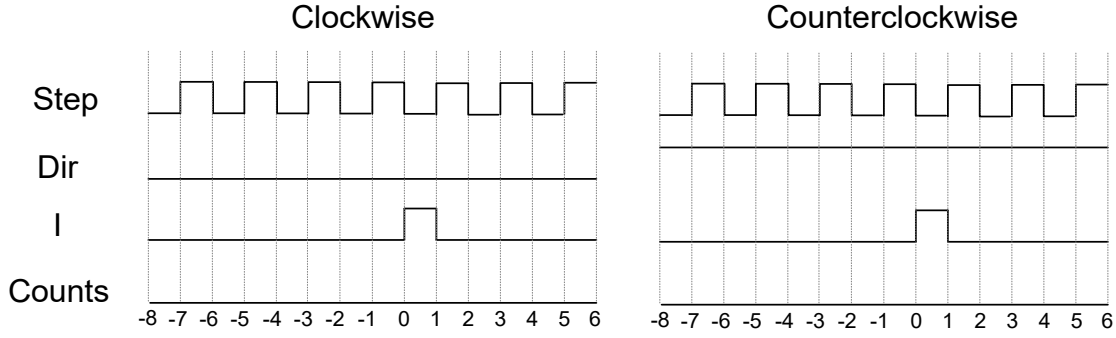


Figure 33. Step-Direction Protocol

5.3.3 Interpolator Factor/Resolution

The incremental interfaces for the RAA2P3226 device feature four interpolation factor settings (9-bit,10-bit,11-bit,12-bit), available in both binary and decimal formats. The interpolation factor is defined as the number of counts per electrical period. “Pulses per period” refers to the number of pulses generated on one channel over one electrical period (360° el.). The interpolator settings define the number of counts per electrical period, which must be multiplied by the number of primary coil periods to calculate the number of counts per mechanical period as shown in Table 25.

The maximum achievable resolution on ABI interface is 17-bit, which can be obtained by configuring 32 periods on the primary coil and utilizing the 12-bit interpolator. This configuration divides each mechanical period into 131072 counts.

Table 25. Counts per Mechanical Period and Resolution by Interpolator/Primary Coil settings

Primary Coil [Periods]	Binary				Decimal			
	9-bit	10-bit	11-bit	12-bit	9-bit	10-bit	11-bit	12-bit
4	2048 (11-bit)	4096 (12-bit)	8192 (13-bit)	16384 (14-bit)	2000	4000	8000	16000
8	4096 (12-bit)	8192 (13-bit)	16384 (14-bit)	32768 (15-bit)	4000	8000	16000	32000
16	8192 (13-bit)	16384 (14-bit)	32768 (15-bit)	65536 (16-bit)	8000	16000	32000	64000
32	16384 (14-bit)	32768 (15-bit)	65536 (16-bit)	131072 (17-bit)	16000	32000	64000	128000

5.3.4 Maximum Speed

The maximum rotation speed is defined by the maximum output pulse rate at channels A and B, which is 2MHz. Additionally, the maximum rotation speed depends on the interpolator resolution and the number of pole pairs of the primary coil.

Table 26. Maximum Mechanical Rotational Speed by Interpolator Setting

Primary Coil [Periods]	Interpolator settings [rpm]			
	9-bit [512]	10-bit [1024]	11-bit [2048]	12-bit [4096]
4	150000	117000	58000	29000
8	75000	58000	29000	15000
16	37000	29000	15000	7300
32	18000	15000	7300	3700

5.3.5 Index Pulse

Encoders' incremental interfaces send an index pulse to mark their zero position. The receiver uses this pulse to synchronize and subsequently utilize use the A/B and Step/Direction signal to maintain accurate position tracking. The index pulse width and position are programmable to support a wide range of receivers.

Two programmable options for the index pulse width are available: 1 count or 3 counts duration. Furthermore, there are four programmable options for the index pulse position (index_cfg), each defining the resulting diagnostic state as described in Table 27.

Table 27. ABI Index Configurations

Index Pulse Position	ABI Diagnostic State	Step/Dir Diagnostic State
A=0 B= 0	A=1, B=1, I=1	Step=1, Dir=X , I=1
A=1 B= 1	A=0, B=0, I=1	Step=0, Dir=X , I=1
A=0 B=1	A=0, B=0, I=1	Step=1, Dir=X , I=1
A=1 B=0	A=0, B=1, I=1	Step=0, Dir=X, I=1

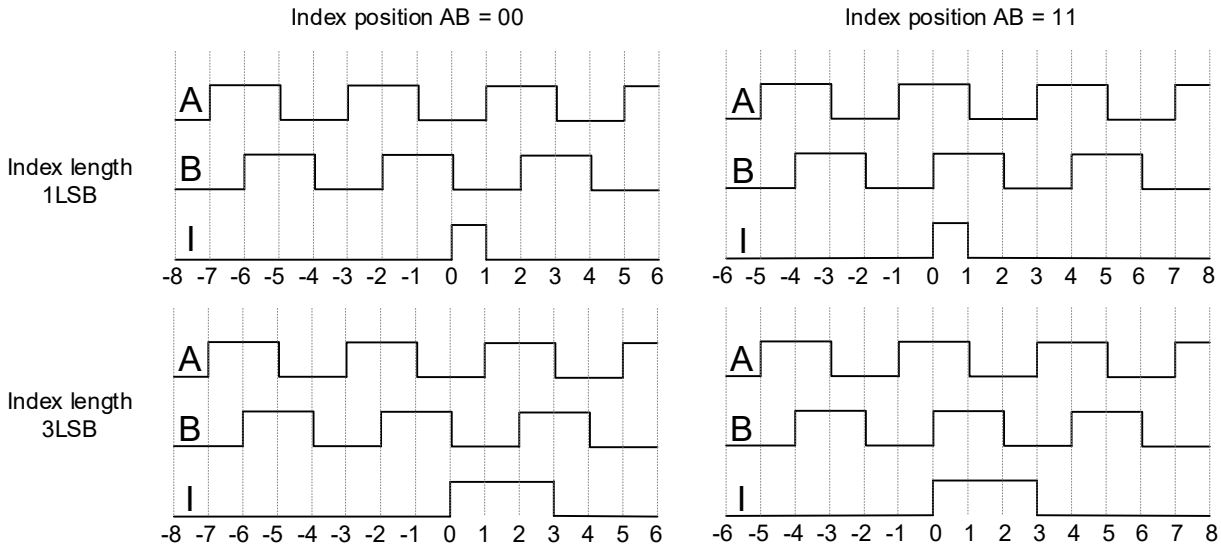


Figure 34. ABI Index Position and Length Configurations

The index configuration defines the diagnostic state indication. The combination of the three signals in Diagnostic Mode is the one that does not occur during normal operation.

5.3.6 True-Power-On Absolute Position Information

Incremental interfaces lack the capability to deliver absolute position information immediately upon power-up. At power-up, the absolute position remains unknown if the measured object, such as a motor, is stationary. Motion is required to detect the first index and calculate the position accurately.

RAA2P3226 is capable of calculating the absolute position internally and provides it over the incremental interface after power-up, before any rotation starts. This is implemented by sending an artificial burst of pulses (see Figure 35).

After a programmable wait time, an index pulse is generated to reset the external counter at the receiving end, followed by a series of AB pulses that indicate the absolute position. The frequency of this pulse train is programmable, ensuring synchronization of the counter at the receiving end with the correct absolute position. The rotor must remain stationary during the initial pulse train sequence. This feature can be enabled or disabled by user programming.

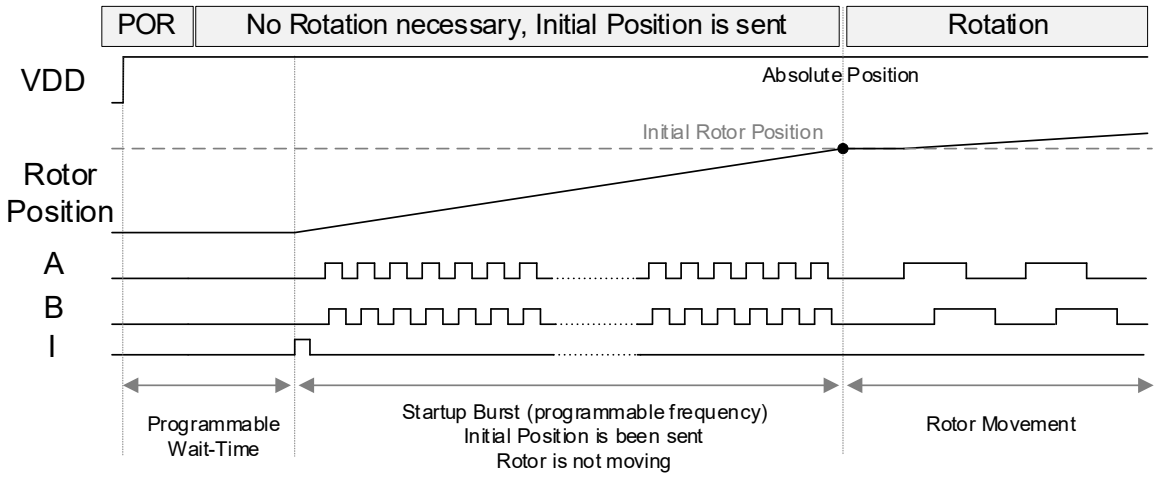


Figure 35. ABI True-Power-On Burst Delivering Absolute Position at Startup Without Rotation

5.3.7 Hysteresis

To prevent jitter in the position output when the system is stationary due to noise, hysteresis is implemented. If the rotational direction remains unchanged, hysteresis has no effect. It becomes noticeable when the rotational direction is reversed, see Figure 36. In such case, the indicated position in the opposite direction is offset by the selected amount of hysteresis. The hysteresis is programmable in 8 steps.

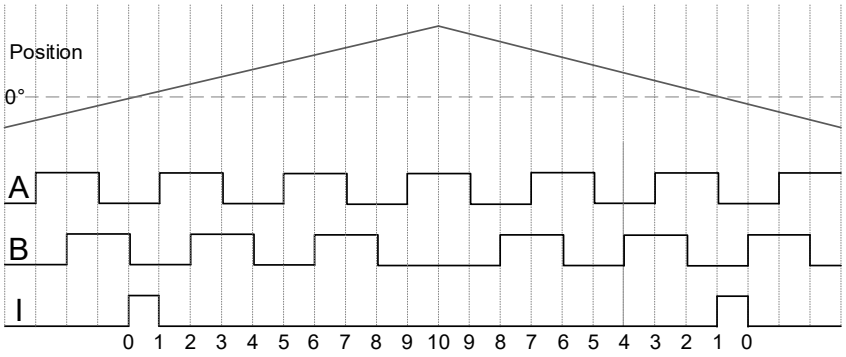


Figure 36. ABI Reversing Direction

5.4 UART Single Wire Programming Interface

Any user programmable parameter can be accessed through the single wire programming process, using a half-duplex UART protocol.

When performing an end-of-line calibration or in-line programming of a position sensor module containing the RAA2P3226, no additional wires are required. The chip is programmed through the OUT1 output at the operational supply voltage range (5V ±10%, 3.3V ±10%).

A short programming window is enabled after POR and requires a digital unlock password to activate programming mode. If no password is sent, the chip resumes its normal operating mode.

For more details, see the *RAA2P3226 Programming Manual* document.

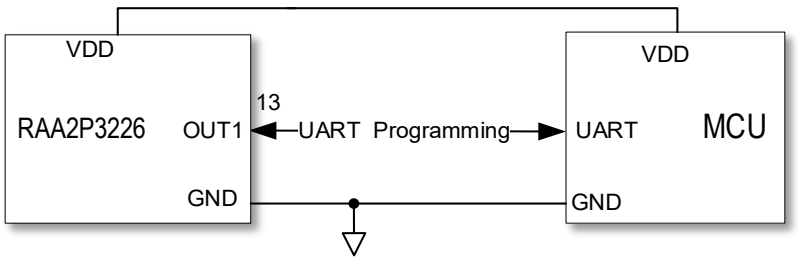


Figure 37. UART Single Wire NVM Programming

5.4.1 Lock Feature

The RAA2P3226 includes a lock bit feature that can be configured by the user. The lock feature allows for both write and read lock options. Once the corresponding lock bits are set, no further writing or reading to/from the RAA2P3226 is possible. It is important to note that a locked RAA2P3226 cannot be unlocked. For more details, see the *RAA2P3226 Programming Manual* document.

6. Auxiliary Inputs and Outputs

One auxiliary input is available for connecting external devices with UART interface. Further, a digital output pin is available indicating user programmable features. A summary is shown in Table 28.

Table 28. Auxiliary Inputs and Digital Output Options

Interface	Analog Input	Register Flag (Open-Drain)
1-wire UART	Yes (pin 10)	Yes (pin 12)
2-wire	Yes (pin 10)	n/a
I2C	n/a	Yes (pin 13)
ABI – Step/Dir	n/a	n/a

6.1 Analog Input

An analog input available on pin 10 (IO1) in UART mode and can be used to read buffered analog voltages from external sensors. See Table 29 for the key parameters of this input. The analog value must be in relation to VDDD.

Table 29. AIN Analog Input Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_AIN}	AIN voltage range		0.1		1.2	V
RES_{AIN}	ADC resolution			12		bits
T_{Smp_AIN}	Sampling rate		4.4			kHz
ACC_{AIN}	Analog Input Accuracy		-1.5		1.5	%VDDD

Both the analog input and the VDDD reference voltages are internally measured and stored in registers. The external load on VDDD cannot exceed 4 mA as specified in Table 4

6.2 Digital Output (Register Flag)

An optional digital output is available in UART and I2C mode. In this configuration, the DOUT output can be used to drive external circuits. DOUT is available on OUT2 pin for UART configuration, on OUT1 pin for I2C. It is controlled by writing either of the following options to the address 0x029E [0]:

- Register bit 0: FLG output is low
- Register bit 1: FLG output is high

This function can be integrated with a heartbeat feature to provide diagnostic status information alongside the flag value. This status is indicated by a 1.5KHz pulse, see Figure 38 with a duty cycle of 97% when the flag is high and 3% when the flag is low.

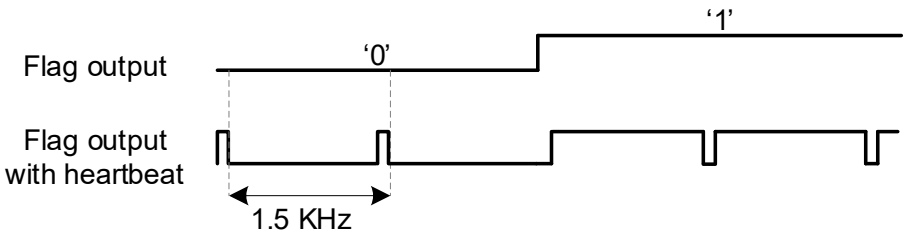


Figure 38. Flag Output Configurations

7. On-Chip Diagnostics

The RAA2P3226 includes on-chip diagnostics featuring an extensive number of internal diagnostic monitors (DM). For detailed description, see the *RAA2P3226 Programming Manual* document.

.

Table 30. Diagnostic Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_{FDTI}	Failure detection time interval (time to detect and internally set a flag describing the error condition)	fdti_cfg=1			2.3	ms
		fdti_cfg=0			20	ms

Table 31. Diagnostic Monitors

Category	Diagnostic Monitors (DM)	Description
Monitoring of external supply	VDD Monitor	External VDD supply out of range
Monitoring of internal supplies	VDDA Monitor	Internal VDDA (Analog supply) out of range / undervoltage /overvoltage
	VDDD Monitor	▪ Internal VDDD (Digital supply) out of range ▪ Short on VDDD ▪ Overcurrent at VDDD pin
	Internal Supply Monitor	Internal supply out of range
	Internal pre-regulators Monitor	▪ Internal pre-regulator for power management (bandgap, analog parts) out of range ▪ Internal pre-regulator for output stages out of range
	Driver Regulator Monitor	OUT2 regulator driver out of range
	Oscillator Regulator Monitor	LC oscillator regulator out of range
	Bias Current Monitor	Bias current diagnostic out of range
Monitoring of RX coils	RX coil Sine Monitor (Primary and Secondary)	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX SIN
	RX coil Cosine Monitor (Primary and Secondary)	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX COS
	RX coil Sine/Cosine neighbor inputs short	Short check between Sine/Cosine coil set detected
Monitoring of TX coils	TX Voltage Monitor	▪ Common mode voltage of TX1/TX2 out of range ▪ Flag for broken pins of LC oscillator
	LC Oscillator Monitor	▪ LC oscillator stuck detected ▪ LC oscillator frequency out of range
Monitoring of system clock	System clock Monitor	▪ Fault in internal system clock: frequency out of range ▪ Fault in internal system clock: stuck detected
Monitoring of the internal communication channel	Internal digital logic failure Monitor	Internal digital logic failure detected such as APB Diagnostic failure, IC internal registers failure, FSM failure, CORDIC failure, other digital failures.
Monitoring the internal memory	Non-Volatile Memory Monitor	▪ CRC mismatch over the NVM or internal shadow register ▪ NVM read timeout fail
Data path diagnostics	Data path WD/OF/UF/DO Monitor	Internal errors, such as overflow, underflow, division by 0, or watchdogs
Position Range Monitoring	Position Range Monitor	Position outside of the defined range failure
Temperature monitoring	Temperature Monitor	▪ Temperature warning detected ▪ Temperature error (shutdown) detected

Category	Diagnostic Monitors (DM)	Description
Magnitude evaluation	Magnitude static Monitor	Magnitude static check error detected on RX coils
Monitoring of analog signal path offset	ADC temperature sensor offset fail Monitor	Compensation of the internal offset not sufficient
Monitoring of the mechanical stress /cracks	Broken chip check Monitor	IC die mechanical failures detected
LPF check for signal path	LPF Monitoring	Failure in internal LPF
AGC monitoring	AGC error Monitoring	▪ Automatic gain control loop not converging ▪ Pre-defined acceptable gains for the AGC not sufficient for RX
Monitoring of the output interfaces	Output Interfaces monitors	▪ Failure of the I2C interface ▪ Failure of the UART interface
Analog input	Analog Input Monitoring	Failure on analog input range
OUT2 and IO1 pins monitoring	OUT2/IO1 pins Monitoring	▪ Overvoltage/undervoltage ▪ Short on OUT2/IO1 detection

A fault from a broken or short wire refers to the connection between sensor IC and control unit (MCU, ECU), including the soldering of the IC pins, PCB traces, connectors and cables. In this case, the diagnostic state depends on whether pull-up/pull-down resistors are installed at the receiver side.

8. User Programming Options

Table 32 shows an extract of the main configuration options. A detailed description is provided in the RAA2P3226 programming manual, available on request from Renesas.

Table 32. Global Programming Options, RAA2P3226

Programming Option	Number of options	Description
Power supply mode	2	3.3V ±10% or 5.0V ±10%
Interface Options	4	UART, I2C, ABI, Step/Dir
Initial receiver gain, primary and secondary coils	2 x 27	Initial receiver gain
Automatic gain control AGC	2	Enabled/disabled
Hysteresis	2 x 8	0 to 112 LSBs
Number of linearization points	16 points	Up to 16 linearization points are freely programmable on primary and secondary coil
Linearization points resolution	12-bit	Up to 16 linearization points are freely programmable in X (position) and Y (value) with 12-bit resolution
Magnitude alarm reference limits	2 x 14-bit	Upper and Lower limits programmability
Zero (discontinuity) point for primary and secondary coils	2 x 12-bit	0° to <360° in 12-bit steps, position output switches from maximum to minimum value (with increasing position movement) or from minimum to maximum value (with decreasing position movement) at this position
Sine and cosine signal offset correction	4 x 8-bit	±127 LSBs for sine/cosine for primary and secondary coils

Programming Option	Number of options	Description
Sine and Cosine amplitude mismatch correction on primary and secondary coil	4 x 15-bit	0% to 199% adjustment range per channel
Digital low pass filter on primary and secondary coil	2 x 8	Depth of digital low pass filter for primary coil position output
Turns counter for primary and secondary coil	2 x 12-bit	Behavior of 12bit primary coil turns counter when overflowing: stop at max/min, wrap around
Customer ID	48-bit	Scratchpad register for customer specific data

9. Related Documents

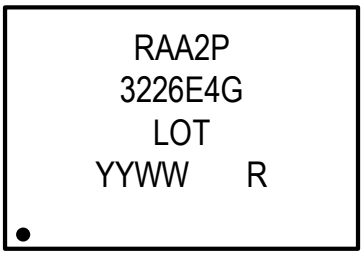
- RAA2P3226 Programming Manual

10. 16-TSSOP Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

16-TSSOP Package Outline Drawing 4.4mm Body, 0.65mm Pitch PGG16T1

11. Marking Diagram



Line 1: First characters of part code: RAA2P.
Line 2: Next five characters of the part code:
3226E: Dual Coil High Speed
followed by:
4 = Operation temperature range, Industrial
G = Industrial Qualified
Line 3: “LOT” = Lot number
Line 4: “YYWW” = Manufacturing date:
YY = last two digits of manufacturing year
WW = manufacturing week
R = RoHS compliant statement

12. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
RAA2P3226E4GSP#HA0	16-TSSOP, 4.4 ×5.0 mm	3	7” Reel, 1300 parts / reel	-40° to +125°C
For communication and programming, Renesas offers a RAA2P3226 Application Modules with a RAA2P-COMBOARD. A development programmer is available separately.				

13. Glossary

Term	Description
ADC	Analog to Digital Converter
BLDC	Brushless Direct Current
DC	Direct Current
DP	Discontinuity Point
GND	Ground
IC	Integrated Circuit
LF	Low Frequency
OD	Open Drain
PCB	Printed Circuit Board
Pk-pk	Peak to peak
PP	Push-Pull
UART	Universal Asynchronous Receiver / Transmitter
RF	Radio Frequency
RX	Receiver
TX	Transmitter

14. Revision History

Revision	Date	Description
1.0	Aug 7, 2025	Initial release

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