RAA2P4500

Single Coil Inductive Position Sensor IC with Analog, PWM, SENT and I2C Interfaces

RAA2P4500 is a magnet-free, inductive position sensor ICs that can be used for absolute rotary, linear, or arc position sensing applications in automotive applications. It operates on the principle of eddy currents to detect the position of a simple metallic target that is moving above a set of coils, comprising one transmitter coil and two receiver coils.

These coils are typically copper traces on a printed circuit board (PCB). The transmitter coil induces a secondary voltage in the receiver coils, which varies depending on the position of the metallic target above them.

A signal representative of the target's position relative to the coils is calculated by demodulating and processing the secondary voltages from the receiver coils. The target can be made of various metals, including aluminum, steel, or a PCB with a printed copper layer.

The RAA2P4500 is equipped with:

- 12-bit Analog Output
- 12/14-bit PWM Output
- 12/14-bit SENT interface
- 14-bit I2C interface
- Additional analog voltage input for external devices.
- Digital input for external digital sensors. The information from external analog or digital inputs is available over the I2C interface.

The RAA2P4500 has been developed according to ISO26262 for implementation in safety-relevant systems up to ASIL C. It can also be used in ASIL D system-level requirements according to ASIL Decomposition rules (i.e. ISO 26262:2018, Part 9, Clause 5") or proper risk analysis by the system integrator.

Available Support

Renesas provides application modules that demonstrate RAA2P4500 rotary, arc, and linear position sensing applications.

Features

- Cost-effective: no magnet required
- Immune to magnetic stray fields: no shielding required
- Suitable for harsh environments and high temperatures
- Analog, PWM, SENT, I2C interfaces
- SENT tick time programmable from 0.02 to 6µs
- Auxiliary 12-bit analog voltage input for external sensors
- Programmable through single wire UART and I2C protocol
- Nonvolatile memory enabling multiple programming options
- Single IC supports on-axis and off-axis rotation, linear motion, and arc motion sensing
- Adaptable to any full-scale angle range through coil design
- High accuracy position ≤0.1% full scale (with ideal coils), enabling sensor solutions up to 11-bit electrical accuracy
- Overvoltage and reverse polarity protection: ±18V on both supply and output pins
- Supply voltage programmable for: 3.3V ±0.3V or 5.0V ±0.5V
- Qualified for automotive application use from -40°C to +160°C ambient temperature
- Compliant to ISO26262 upto ASIL C
- 48 bits nonvolatile user ID memory space
- Small 16-TSSOP package (4.4mm × 5.0mm)

Typical Applications

Linear and Angle position sensing in automotive applications: gas and brake pedals, chassis, valves.

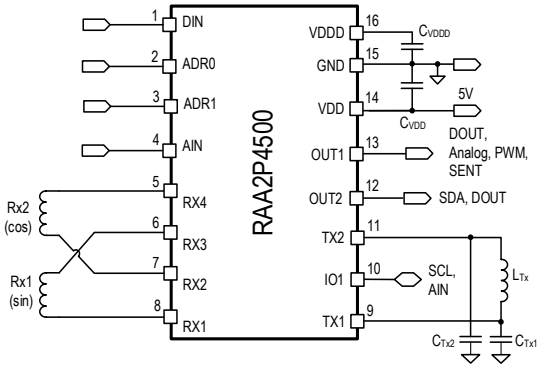

Figure 1. Application Circuit Example

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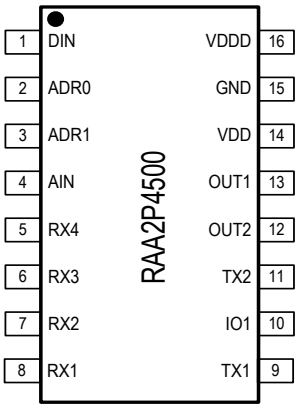


Figure 2. RAA2P4500

Table 1. Pin Description, RAA2P4500

Pin Number	Name	Type	Description
1	DIN	Digital Input	Auxiliary digital input for static or pulse signals, readable over I2C interface
2	ADR0		Address selection bit0 input for I2C interface (bit-strapping)
3	ADR1		Address selection bit1 input for I2C interface (bit-strapping)
4	AIN	Analog Input	Auxiliary analog (12-bit) input for external analog signal, readable over I2C interface
5	RX4	Sensor Input	Receiver coil (COS_N)
6	RX3		Receiver coil (SIN_N)
7	RX2		Receiver coil (COS)
8	RX1		Receiver coil (SIN)
9	TX1	Transmitter Output	Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND
10	IO1	Digital I/O	Analog: Not used PWM: Not used / PWM inverted SENT: Analog In I2C: SCL
11	TX2	Transmitter Output	Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND
12	OUT2	Digital I/O	Analog: Digital output PWM: Digital output / PWM output (differential PWM) SENT: Digital output I2C: SDA
13	OUT1	Analog output Digital I/O	Analog: 12-bit analog ramp output AOUT PWM:12-bit /14-bit PWM output SENT: SENT output I2C: Digital output Single wire programming interface
14	VDD	Supply	External supply voltage (3.3V or 5V)
15	GND	Supply	Common ground connection
16	VDDD	Supply	Internally regulated digital supply voltage

2. Specification

2.1 Absolute Maximum Ratings

The absolute maximum ratings listed in Table 2 are stress ratings only. Exceeding these limits can cause permanent damage to the device. The functional operation of the RAA2P4500 at these maximum ratings is not guaranteed. Exposure to the absolute maximum rating conditions could impact device's reliability. All voltage levels are referenced to GND.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{VDDmax}	External supply voltage: VDD	Continuous	-18	18	V
V_{IO1}	Digital input pin voltage				
V_{OUT2}	Digital I/O pin voltage				
V_{OUT1}	Analog/Digital output pin voltage				
V_{RX1}	Sensor receiver coil input pin Voltage (RX1)	Continuous	-12	12	V
V_{RX2}	Sensor receiver coil input pin Voltage (RX2)				
V_{RX3}	Sensor receiver coil input pin Voltage (RX3)				
V_{RX4}	Sensor receiver coil input pin Voltage (RX4)				
V_{DIN}	Digital input pin voltage				
V_{ADR0}	Digital input pin voltage				
V_{ADR1}	Digital input pin voltage				
V_{AIN}	Analog input pin voltage				
V_{Tx1}	Transmitter output pin (TX1) voltage	Continuous	-0.3	5.5	V
V_{Tx2}	Transmitter output pin (TX2) voltage				
$V_{VDDDmax}$	Internal digital supply voltage, VDDD	VDDD is internally regulated with an external capacitor to GND	-0.3	2.0	V
T_{AMB}	Ambient temperature		-40	160	ºC
T_J	Junction temperature		-40	170	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125°C to prevent pre-aging	-55	160	ºC
R_{THJA}	Thermal resistance junction to ambient: 16-TSSOP package	Velocity = 0m/s with 2s2p PCB test board (JEDEC 51-2, JEDEC 51-7)		89.5	K/W
R_{THJC}	Thermal resistance junction to case: 16-TSSOP package	Junction to top of package		38.38	K/W

2.2 ESD Ratings

Table 3. ESD Ratings

Symbol	Parameter	Conditions	Maximum	Units
V_{ESD_OUT}	ESD tolerance for pins with potential external cable connection: ▪ OUT1 ▪ VDD, VSS Human Body Model: 100pF / 1.5kΩ	According to AEC-Q100-002 classification 3A	±4	kV
V_{ESD}	ESD tolerance for all other pins not listed under V_{ESD_OUT} Human Body Model: 100pF / 1.5kΩ	According to AEC-Q100-002 classification 2	±2	kV
V_{CDM}	ESD tolerance for all pins: Charged-Device Model (CDM)	According to AEC-Q100-011 classification C2B	±750	V

2.3 Operating Conditions

All minimum/maximum specification limits are guaranteed by design, production testing, and/or statistical characterization. Conditions: T_{AMB} = -40°C to 160°C unless otherwise specified. C_{VDD} = 470nF, C_{VDDD} = 100nF.

Typical values are based on characterization results at default measurement conditions and are informative only.

Table 4. Electrical Characteristics, 5V and 3.3V modes

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{VDD5}	Supply voltage, 5V mode		4.5	5.0	5.5	V
$V5_{UV}$	Undervoltage detection level, 5V mode	An undervoltage alarm is created if VDD falls below this limit	3.95	4.1	4.45	V
$V5_{OV}$	Overvoltage detection level, 5V mode	An overvoltage alarm is created if VDD rises above this limit	5.55	6.15	6.5	V
V_{VDD3}	Supply voltage, 3.3V mode		3.0	3.3	3.6	V
$V3_{UV}$	Undervoltage detection level, 3.3V mode	An undervoltage alarm is created if VDD falls below this limit	2.7	2.8	2.98	V
$V3_{OV}$	Overvoltage detection level, 3.3V mode	An overvoltage alarm is created if VDD rises above this limit	3.65	3.85	4.04	V
$V_{VDD\_TH\_H}$	Power-on reset (POR), high threshold	Power-on reset (POR): the device is activated when VDD increases above this threshold		2.61	2.7	V
$V_{VDD\_TH\_L}$	Power-on reset (POR), low threshold	The device is deactivated when VDD decreases below this threshold	2.3	2.38		V
$V_{VDD\ POR\_HYST}$	Power-on reset hysteresis		200	250	300	mV
$t_{stup\ PE}$	Start-up times	Power-on reset (POR) to valid output signal, programming enabled			5	ms
$t_{stup\ PL}$		Power-on reset (POR) to valid output signal, programming locked			3	ms
$t_{stup\ cmd}$	Command timeout time	Time to wait before sending first command	1.5			ms

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
t_{ProgEn}	Programming window enable time	Timeout window after POR, in which a first programming enable command must be sent			5	ms
t_{ProgUL}	Programming window unlock time	Timeout window after programming enable in which a second unlock command must be completely sent[i]			75	ms
V_{VDDD}	Digital supply voltage	Internally regulated. Connect capacitor C_{VDDD} = 100nF from VDDD to GND.	1.75	1.8	1.85	V
I_{AUXIN}	Auxiliary Input on VDDD maximum external load current	VDDD must be connected to a capacitor C_{VDDD}.	0		4	mA
$I_{SHORT\ VDDD}$	VDDD short circuit current limitation		18.5	27	40	mA
I_{CC}	Current consumption	Without coils, no load	10	15	20	mA
C_{VDDD}	Capacitor from VDDD pin to GND		100			nF
C_{VDD}	Capacitor from VDD pin to GND	Nominal value	100	470		nF

Table 5. Position Resolution and Update Rate

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
RES_{I2C}	Position resolution I2C interface			14		bit
RES_{AOUT}	Position resolution Analog Output interface			12		bit
RES_{Pwm}	Position resolution PWM interface		12		14	bit
RES_{SENT}	Position resolution SENT interface		12		14	bit
$Acc_{SENT\ PWM\ I2C}$	Position accuracy SENT, PWM and I2C interface	Ambient temperature, nominal supply	-0.1		0.1	%FS
		Over temperature and supply range	-0.2		0.2	%FS
Acc_{AOUT}	Position accuracy Analog Output interface	Ambient temperature, nominal supply	-0.5		0.5	%FS
		Over temperature and supply range	-0.7		0.7	%FS
t_{POS}	Position refresh rate	Internal refresh rate of position information	2		3	µs

Table 6. Non-volatile Memory Parameters [1]

Parameter	Conditions	Minimum	Typical	Maximum	Units
Data retention	Qualified according to JEDEC 22-A117	15 @T_J = 100°C			Years
	Over product lifetime		>100 @T_J = 25°C		
Write temperature		-40		135	°C

Parameter	Conditions	Minimum	Typical	Maximum	Units
Read temperature	Allowed ambient temperature range for read and write access	-40		160	ºC
Endurance [2]	Over product lifetime			1000	NVM Write Cycles
Read Cycles		5x 10^{11}	1x 10^{12}		NVM Read events

[1] Guaranteed by memory supplier

[2] Verified number of program/erase cycles. Qualified with 2000 cycles.

Table 7. LC Oscillator Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{LC}	Excitation frequency	LC oscillator frequency is determined by external components L and C.	2		5.5	MHz
R_{Peq}	Equivalent parallel resistance of the LC resonant circuit		250			Ω
V_{TX_PP}	LC oscillator amplitude at VDD = 5.0V ±10%	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. Adjustable by coil current.			8.8	Vpp
	LC oscillator amplitude at VDD = 3.3V ±10%				2* V_{VDD3}	
I_{LC}	Programmable transmitter coil drive current	$T_{ambient}$ = -40 to +160°C	0	[1]	16	mA
R_{Tx1}, R_{Tx2}	LC oscillator series resistors	Depending on coil design and excitation frequency (f_{LC})		10		Ω

[1] The required transmitter coil current is determined by the equivalent parallel resistance of the LC circuit, depending on coil design.

Table 8. Receiver Coils Front-End Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{RX}	RX coil amplitude	Differential coil input	5		200	mV_{pp}
A_{IN_mm}	Maximum amplitude mismatch correction	Programmable gain mismatch correction of RX coil signals (SIN and COS)			15	%
$A_{IN\_OFFS\_RANGE\%}$	Input offset correction range	Differential input offsets of sine or cosine signal, percentage of transmitter coil amplitude.	-0.2		0.2	%
D_{OFFSET}	Coil input offset temperature drift	Over temperature range T_{AMB}	-2.5		2.5	%
C_{RX1} to C_{RX8}	Receiver input filter capacitors	For improved EMC immunity		220		pF
$Noise_{SP}$	Signal path noise level	Digital filtering = OFF V_{RX}= 50mV			0.1	° el. rms
		Digital filtering = OFF V_{RX}= 5mV			0.5	° el. rms

2.4 Interface Pin Characteristics

Table 9. I2C Specifications

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
f_{I2C}	I2C clock rate				400	Kbit/s
t_{SCL_LOW}	Low level state of SCL clock	Normal mode	4.7			µs
		Fast mode	1.3			µs
t_{SCL_HIGH}	High level state of SCL clock	Normal mode	4.0			µs
		Fast mode	0.6			µs
$t_{R\_SDA\_SCL}$	Rise time of SDA/SCL (30% to 70%) $R_{SDA/SCL}$ = 2kΩ	Normal mode			1000	ns
		Fast mode	20		300	ns
$t_{F\_SDA\_SCL}$	Fall time of SDA/SCL (70% to 30%) $R_{SDA/SCL}$ = 2kΩ	Normal mode	20		300	ns
		Fast mode	20			ns
V_{IH_I2C}	High level input voltage	SCL clock input, SDA data input DIN, ADR0, ADR1	0.7×VDD		VDD+0.5	V
V_{IL_I2C}	Low level input voltage		-0.5		0.3×VDD	V
V_{I2C_hyst}	Hysteresis of Schmitt trigger input	SCL clock input SDA, DIN, ADR0, ADR1	0.05 × VDD			V
I_{LEAK}	Input leakage current	VDD = 0V to 5.5V	-10		10	µA
$I_{SDA\ lim\ thr}$	SDA current limitation threshold	OUT2 pin 12 (SDA)	8		30	mA
$I_{SDA\ sc\ lim}$	SDA output short current limitation[1]	Short to VDD, GND VDD = 3.3V, 5V	14		26	mA
V_{OL_SDA}	Output low voltage SDA low level output voltage open drain	3mA sink current VDD = 3.0 to 5.5V	0		0.4	V
I_{OL}	Low level output current	V_{OL} = 0.4V, VDD = 5.5V, $R_{SDA/SCL}$ = 2kΩ	3			mA
t_{SP}	Input spike suppression	Spikes shorter than t_{SP} are suppressed	400		426	ns
C_B	External capacitive load for each bus line				400	pF
R_{SDA}, R_{SCL}	External pull-up resistor at pins SDA and SCL	Resistor value and capacitive load on these pins are limiting the maximum clock frequency	1.8	3.3		kΩ
R_{ADR}	External resistor at pin ADR for I2C address selection	Pull-up/pull-down, depending on I2C address setting.	1.8	4.7		kΩ
$I_{DOUT\ lim\ thr\ I2C}$	DOUT current limitation threshold[2]	OUT1 pin 13 in overload condition	35			mA
$I_{DOUT\ sc\ lim\ I2C}$	DOUT output short current limitation[2]	OUT1 pin 13	28		58	mA

[1] With OUT2 drive strength set to “00” (out2_io1_drv = “00”)

[2] With digital mode configuration (out1_drv=”10”)

Table 10. Analog Output

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
A_{OUT}	AOUT voltage range		5		95	%VDD
$I_{AOUT\ lim\ thr}$	AOUT current limitation threshold [1]	OUT1 pin 13 in overload condition	19			mA
$I_{AOUT\ sc\ lim}$	AOUT output short current limitation	OUT1 pin 13 Short to VDD / GND VDD = 3.3V or 5V	23		38	mA
$I_{DOUT\ lim\ thr\ AOUT}$	DOUT current limitation threshold	OUT2 pin 12 in overload condition	8			mA
$I_{DOUT\ sc\ lim\ AOUT}$	DOUT output short current limitation [2]	OUT2 pin 12 Short to VDD / GND VDD = 3.3V or 5V	14		26	mA
$C_{L,AOUT}$	Output buffer Load capacitance	Capacitor from AOUT to GND		47	100	nF
$SR_{\_AOUT}$	Output Buffer Slew Rate	At maximum load conditions	0.1			V/µs

[1] With Analog Out configuration (out1_drv="01")

[2] With OUT2 slow configuration (out2_io1_drv="00")

Table 11. PWM Interface Parameters

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
$I_{OUT1\ lim\ thr\ PWM}$	PWM Out limitation threshold [1]	Pin 13 (OUT1) PWM SE In overload condition	35			mA
$I_{OUT1\ sc\ lim\ PWM}$	PWM output short current limitation [1]	Pin 13 (OUT1) PWM SE Short to VDD / GND VDD = 3.3V,5V	28		58	mA
$I_{OUT2\ IO1\ lim\_thr\ PWM}$	OUT2 and IO1 current limitation threshold	Pin 12 (OUT2) Pin 10 (IO1) in overload condition	6			mA
$I_{OUT2\ IO1\ sc\ lim\ PWM}$	Output short current limitation[2]	Pin 12 (OUT2) Pin 10 (IO1) Short to VDD / GND VDD = 3.3V,5V	32		70	mA
$V_{OH\_OUT2\_PWM}$	Output high voltage Push-pull mode Pin 12 (OUT2)	VDD= 3.3V	2.64			V
		VDD= 5V	4			V
$V_{OL\_OUT2\_PWM}$	Output low voltage Push-pull mode Pin 12 (OUT2)	VDD= 3.3V, 5V			0.4	V
DC_{PWM}	PWM duty cycle	Normal operation	5.56		94.44	%
DC_{PWM_DHI}	PWM duty cycle	Diagnostic low mode		2.78		%
DC_{PWM_DLO}	PWM duty cycle	Diagnostic high mode		97.24		%
ft_{PWM}	PWM frequency tolerance		-5		5	%
t_{PWM_r}	PWM output rising edge, push-pull mode.	Load capacitance 4.7nF Output voltage rising from 10% to 90% @ 5V			5	us
t_{PWM_f}	PWM output falling edge, push-pull mode	Load capacitance 4.7nF Output voltage falling from 90% to 10% @ 5V			5	us
$R_{PULL-UP}$	Output Pull-up Resistance		1	2	10	kΩ

[1] With digital mode configuration (out1_drv="10")

[2] With OUT2 fast configuration (out2_io1_drv="11")

Table 12. SENT Interface

Symbol	Parameter	Description	Minimum	Typical	Maximum	Units
V_{OL_SENT}[3]	Output low voltage	3mA sink current, VDD = 4.5 to 5.5V OUT1 pin 13	0		0.5	V
V_{OH_SENT}[3]	Output high voltage	3mA source current, VDD = 4.5 to 5.5V OUT1 pin 13	4.1		5.5	V
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold[1]	OUT1 pin 13 in overload condition	55			mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation[1]	OUT1 pin 13 Short to VDD, GND VDD = 4.5 to 5.5V Push-pull mode	40		91	mA
t_{OVL}	Overload shutdown debounce time	Duration of overload condition, before output is shut off		2		ms
$I_{DOUT\ lim\ thr}$	DOUT current limitation threshold[2]	OUT2 pin 12 in overload condition	8			mA
$I_{DOUT\ lim\ thr}$	DOUT output short current limitation [2]	OUT2 pin 12	33		70	mA
C_{input}	Parasitic input capacitance from ESD protection				0.1	nF
I_{SUP}[3]	Average current consumption from Receiver 5V supply over one message				50	mA
I_{GND}[3]	Average current through Ground line over one message				50	mA
$I_{SUP\ RIPPLE}$[3]	Peak-to-peak variation in supply current consumption over one message at frequencies up 30 kHz				9	mA
T_{Fall}[3]	Falling time, tick time = 3 µs From V_{TH} = 3.8V to V_{TL} = 1.1V	$I_{SUP} \le 20$ mA			6.5	µs
		20 mA ≤ I_{SUP} < 50 mA			5	µs
T_{Rise}[3]	Rising time, tick time = 3 µs From V_{TL} = 1.1V to V_{TH} = 3.8V				18	µs
ΔT_{Fall}[3]	Edge to Edge Jitter with static environment for any pulse period tick time = 3 µs				0.1	µs
R_{Tau1}	Input filter resistor (1st stage)		448	560	672	Ω
C_{Tau1}	Input filter capacitor (1st stage)		1.54	2.2	2.86	nF
Tau_1	Input filter time 1st stage time constant defined by RTau1 and CTau1		0.74		1.73	µs
$R_{PULL-UP}$	Input Pull-up resistor		10		55	kΩ
R_F	Input filter resistor (2nd stage)		4			kΩ
C_F	Input filter capacitor (2nd stage)	Determined by TAU2 requirement				nF
R_V	Voltage divider, adjusting SENT output level to MCU input level	Optional, depends on MCU input level				kΩ
Tau_2	Input filter time 2nd stage time constant defined by RV,RF and CF		0.6		1.4	µs

[1] With SENT mode configuration (out1_drv=“”11”)

[2] With out2_io1_drv = “11”

[3] Refer to SENT Standard SAE J2716 Standard (Rev. April 2016)

3. Detailed Description

3.1 Overview

The RAA2P4500 sensor IC is designed to drive a single transmitter coil and receive signals from one pair of receiver coils, typically created as traces on a printed circuit board. The receiver coils consist of two wire loops connected in anti-serial fashion, with the “sine” and “cosine” coils shifted by 90 electrical degrees. A metal target is placed above this coil arrangement.

When the IC drives an AC current into the transmitter coil, it generates an alternating magnetic field. This magnetic field induces secondary voltages in the receiver coils. Without a target, the induced voltages in the loops of the receiver coils cancel each other out, resulting in a net receiver voltage of zero.

When a metal target is placed above the coils, the magnetic field generates eddy currents on its surface. These eddy currents create a counter magnetic field, reducing the total flux density underneath. This leads to a reduction in the voltage induced in the receiver coil areas underneath the target, creating an imbalance in the anti-serial coil segment voltages.

The IC demodulates, offsets and corrects the amplitude of the signals from the two receiver coils with a 90° electrical phase shift design, which generates sine and cosine shaped voltages as the target is moving.

The RAA2P4500 IC amplifies, rectifies, and filters the receiver voltages, converting them into digital representation with an ADC. The digital sine and cosine signals are converted into a 0°to 360° absolute position. The signal accuracy can be further enhanced through a 2-dimentional,16-point linearization process.

The absolute position can be read over Analog, PWM, SENT and I2C interfaces.

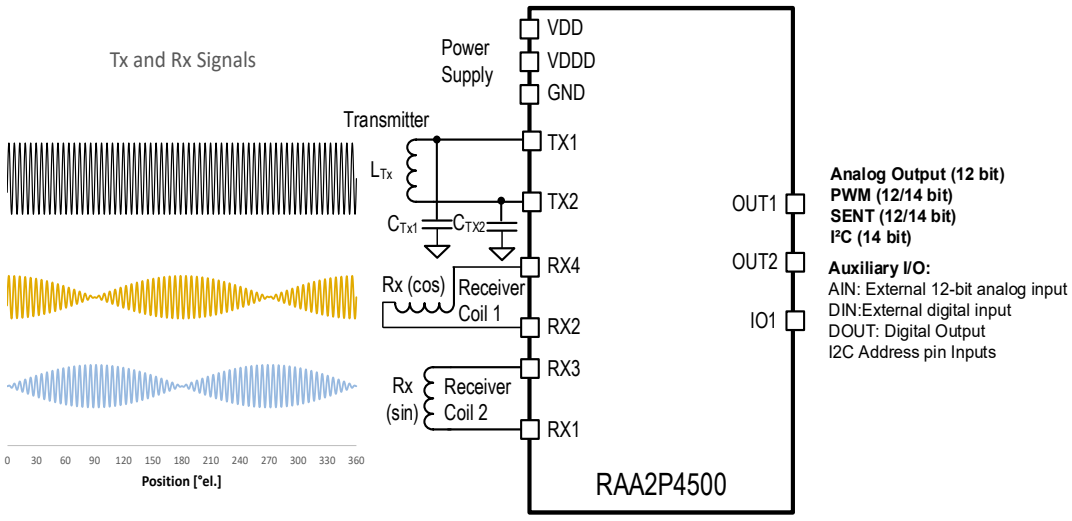


Figure 3. RAA2P4500 Input/Output Signals

3.2 Block Diagram

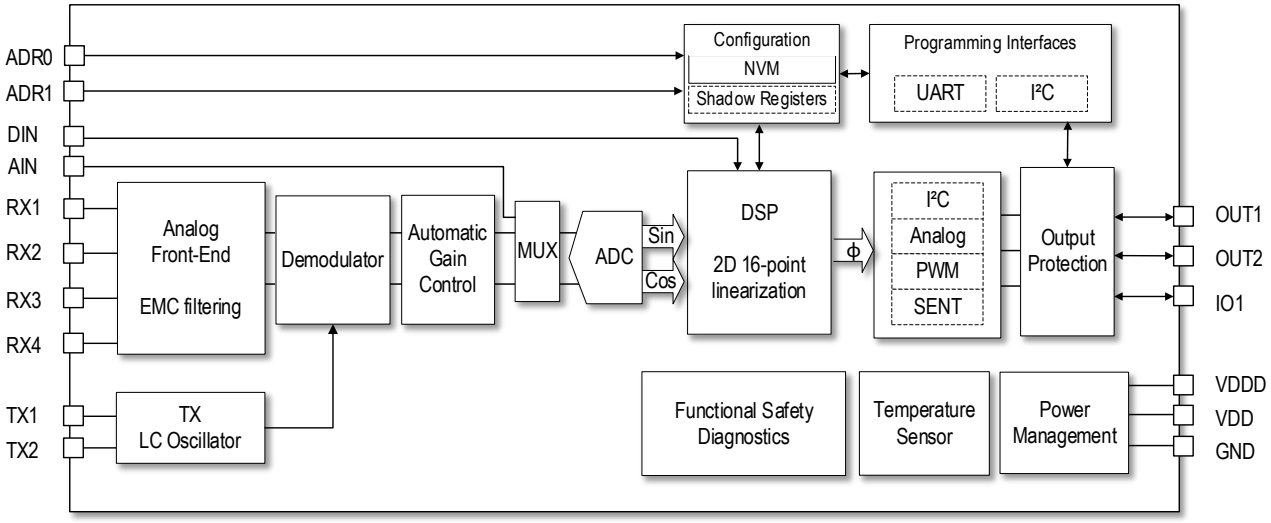


Figure 4. Block Diagram

The main building blocks include:

- Analog front-end: Input EMC filter, offset, and gain control for the receiver signals.
- Demodulator: Converting RF modulated position signals to LF demodulated raw sine and cosine signals.
- Automatic Gain Control: Automatically adjusts the raw sine and cosine signal levels.
- High Speed ADC: Converts raw signals into digital format for further processing.
- Digital signal processing: Converts digital sine and cosine raw signals into synchronized absolute position information.
- 2D 16-point linearization: Supports up to 16 two-dimensional linearization points with freely programmable X- and Y- coordinates for each point (X= Position input, Y= Position output).
- Analog, PWM SENT, I2C: Carries out post processing, clamping, signal integrity checks, and decodes channel information and other diagnostics information into the selected output format.
- TX Oscillator: Generates the transmitter coil signal.
- Temperature sensor: Internal temperature sensor used for chip diagnostics.
- Protection: All outputs are fully protected against overvoltage, reverse polarity and short circuit, enabling direct cable connection to these outputs and eliminating the need for additional line driver ICs.
- Power Management: Operates with supply voltages ranging from 3.0V to 5.5V. External capacitors are required for the supply voltage VDD, and for the digital power supply, VDDD.
- Programming interface: Accessible via one-wire UART interface or I2C interface.
- Configuration, NVM: Stores non-volatile storage for factory and user-programmable settings. User configuration parameters can be programmed multiple times.
- On-chip failure diagnostics: Performs internal diagnosis of critical blocks.
- ADR: Selects the address input for the I2C interface, see Table 26.
- Auxiliary I/O including DIN (Digital input), AIN (12-bit analog input for external analog signals), DOUT (Diagnostic Output) accessible over I2C interface.
- Functional Safety Diagnostics: Internal diagnostics of critical blocks to ensure functional safety up to ASIL-C on chip level.

3.3 LC Oscillator

The transmitter circuit of the RAA2P4500 generates the required RF magnetic field for operating the sensor as determined by an external parallel LC circuit, see Figure 5. To ensure low emission of harmonics, the capacitive part of the LC circuit is split into two equal-value capacitors: C_{Tx1} and C_{Tx2}. Additionally, two series resistors R_{Tx1} and R_{Tx2} are added as shown Figure 5.

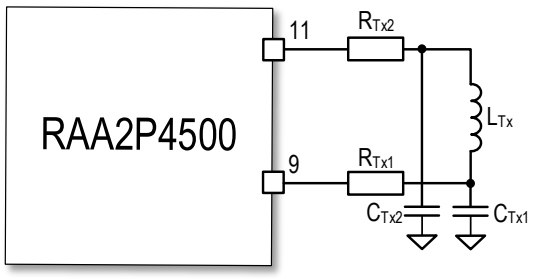


Figure 5. TX LC Oscillator Connection

3.3.1 Parallel LC Resonator Calculations

A resonator, comprising an inductor (L) and a capacitor (C) in parallel, is essential for generating specific frequencies in RF applications. Accurate calculations of the equivalent parallel resistance (R-Peq) ensure proper resonator function. In the RAA2P4500 transmitter circuit, this resonator minimizes harmonic emissions.

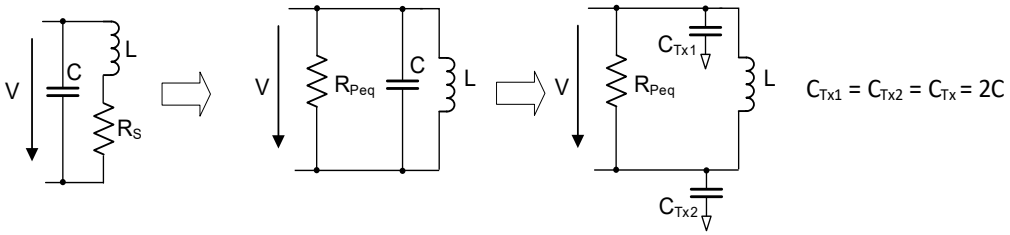


Figure 6. Parallel Resonator Circuit

Equivalent parallel resistance from Coil series resistance:

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C}$$ **Equation 1**

For $C_{Tx1} = C_{Tx2} = C_{Tx} = 2C$:

$$R_{Peq} = \frac{1}{R_S} \times \frac{2 \times L}{C_{Tx}}$$ **Equation 2**

Equivalent parallel resistance from Quality factor Q:

$$R_{Peq} = Q \times \sqrt{\frac{L}{C}} = Q \times \sqrt{\frac{2L}{C_{Tx}}}$$ **Equation 3**

Ideal LC Oscillator frequency with split Tx capacitors C_{Tx}

$$f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{Tx}}{2}}}$$ **Equation 4**

Oscillator frequency with split Tx capacitor C_{Tx} and coil series resistor R_s

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{R_S}{L}\right)^2}$$ **Equation 5**

Oscillator frequency with split Tx capacitor C_{Tx} and equivalent parallel resistor R_{Peq}

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{2}{R_{Peq}C_{Tx}}\right)^2}$$ **Equation 6**

$$Q = R_{Peq}\sqrt{\frac{C}{L}} = \frac{1}{R_S}\sqrt{\frac{L}{C}}$$ **Equation 7**

Coil quality factor

$$Q = \omega\frac{L}{R_S} = 2\pi f_{TX}\frac{L}{R_S}$$ **Equation 8**

Where:

R_{Peq}	Equivalent parallel resistance of the LC circuit at the transmitter frequency in Ohms
R_S	Serial resistance of the transmitter coil at the transmitter frequency in Ohms
f_{Tx}	Resonant circuit frequency in Hertz, 1/s
L	Resonant circuit coil impedance in Henry
C	Resonant circuit capacitance in Farad
C_{Tx1}, C_{Tx2}	Capacitance of the split capacitors in Farad
Q	Resonant circuit quality factor (unitless)
ω	Angular frequency $2*\pi*f_{Tx}$ in Hertz, 1/s

3.4 Coil Design

Figure 7 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$$V_{Cos\ Loop1} = -V_{Cos\ Loop2}$$ **Equation 9**

In the absence of a target, the secondary voltages balance out as follows:

$$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} = 0V$$ **Equation 10**

With a target placed above the coils, the secondary voltage induced in the covered area decreases compared to the secondary voltage when no target is present above it.

$$V_{Cos\ Loop1} \neq -V_{Cos\ Loop2}$$ **Equation 11**

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage ≠ 0V is generated, depending on the location of the target.

$$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} \neq 0V$$

Equation 12

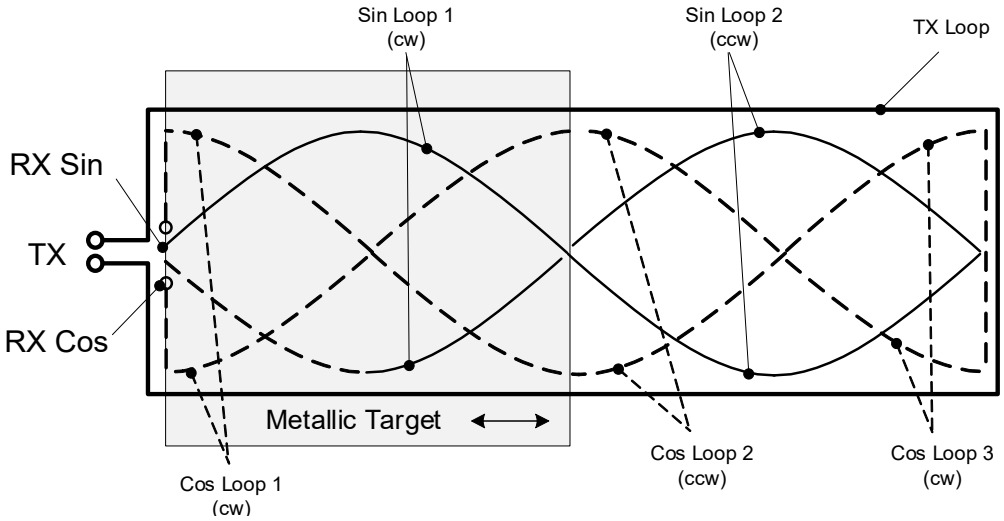


Figure 7. Coil Design for a Linear Motion Sensor

The same principles shown for the linear motion sensor can be applied to a rotary sensor as shown in Figure 8.

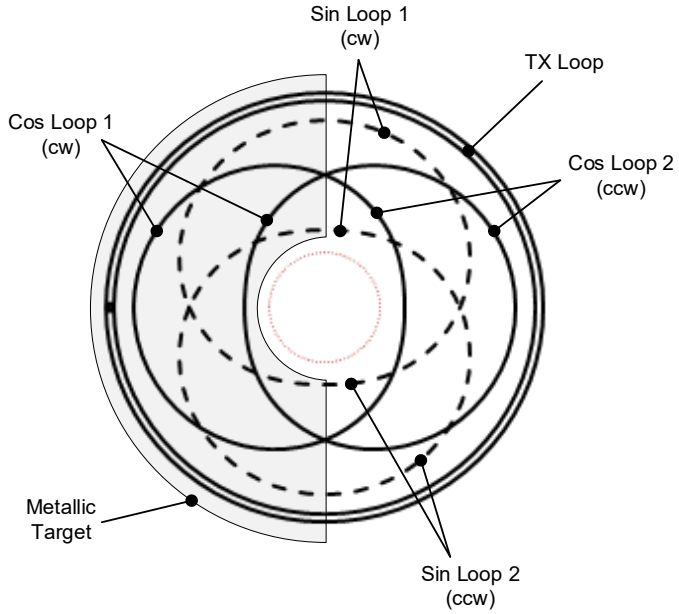


Figure 8. Coil Design for a 360° Rotary Sensor

3.4.1 Multi-periodic Coil Design Application Examples

Applying the same fundamental design principles, coils with multiple periods per turn can be designed. Multi-periodic designs improve mechanical accuracy compared to single-periodic coil designs. For example, a 4-periodic coil design (4 × 90°) improves mechanical accuracy by a factor of 4. Consequently, for angular designs, requiring < 360° movement range, coil designs with multiple periods are recommended.

3.4.2 Electrical vs. Mechanical Degrees

RAA2P4500 converts the movement of a target across a single period of the receiver coil into a precise electrical signal. This conversion spans the full angular range from 0°to 360°, producing a digital output ranging from 0 to (2^N-1) LSBs. The position output is thus absolute over a full turn of 360 mechanical degrees.
As illustrated in Figure 9, the single-periodic coil design establishes a direct 1:1 relationship between electrical and mechanical domains as the following:

- Coil Period: 360° electrical
- Mechanical Range: 360° mechanical
- Conversion Factor: 1:1 (1°el. = 1° mechanical)

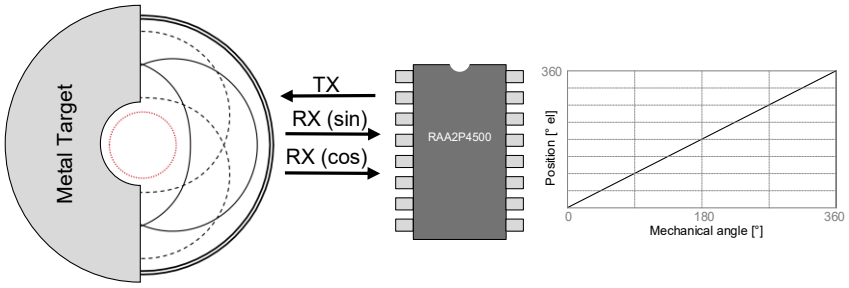


Figure 9. Coil Design Using Single-Periodic Coil

As illustrated in Figure 10, a coil design with four receiver coil periods within a single full mechanical turn, results in four electrical rotations for every complete mechanical turn and provides the following advantages in accuracy and resolution:

- Higher Resolution: Position output resolution increases proportionally with period count by

$$\text{Mechanical Resolution} = \text{Sensors\_Periods} * \text{Electrical Resolution}$$

In this configuration one electrical degree (°el) equals 0.25 mechanical degrees (°). The provided output resolution is four times higher compared to the single-periodic design

- Improved accuracy: Mechanical error is reduced by the period factor

$$Mechanical\ Error = \frac{Electrical\ Error}{Sensor\ Periods}$$

This configuration is particularly well-suited for:

- Multi-pole motors requiring precise commutation
- Limited-range applications (<180° mechanical travel)
- Systems demanding high-resolution incremental feedback

Select the number of periods based on application requirements to optimize measurement performance. Proper period selection is critical for achieving maximum system accuracy.

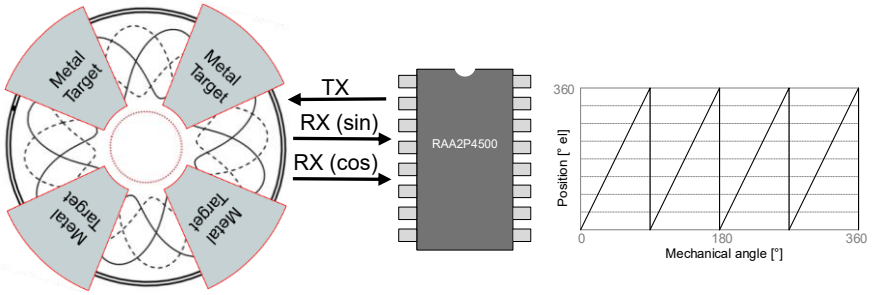


Figure 10. Coil Design Using 4-Periodic Coil

4. Linearization

The RAA2P4500 offers a very flexible linearization feature to enhance sensor accuracy. The linearization algorithm is applied digitally after an angle calculation. The linearization is performed with 12-bits resolution over a 360° electrical range (el.). Up to 16 programmable linearization points can be positioned within a grid of 0.088° in both X (position) and Y (expected output) directions.

Figure 11 illustrates an example of the impact of linearization, showing that the total error is significantly reduced.

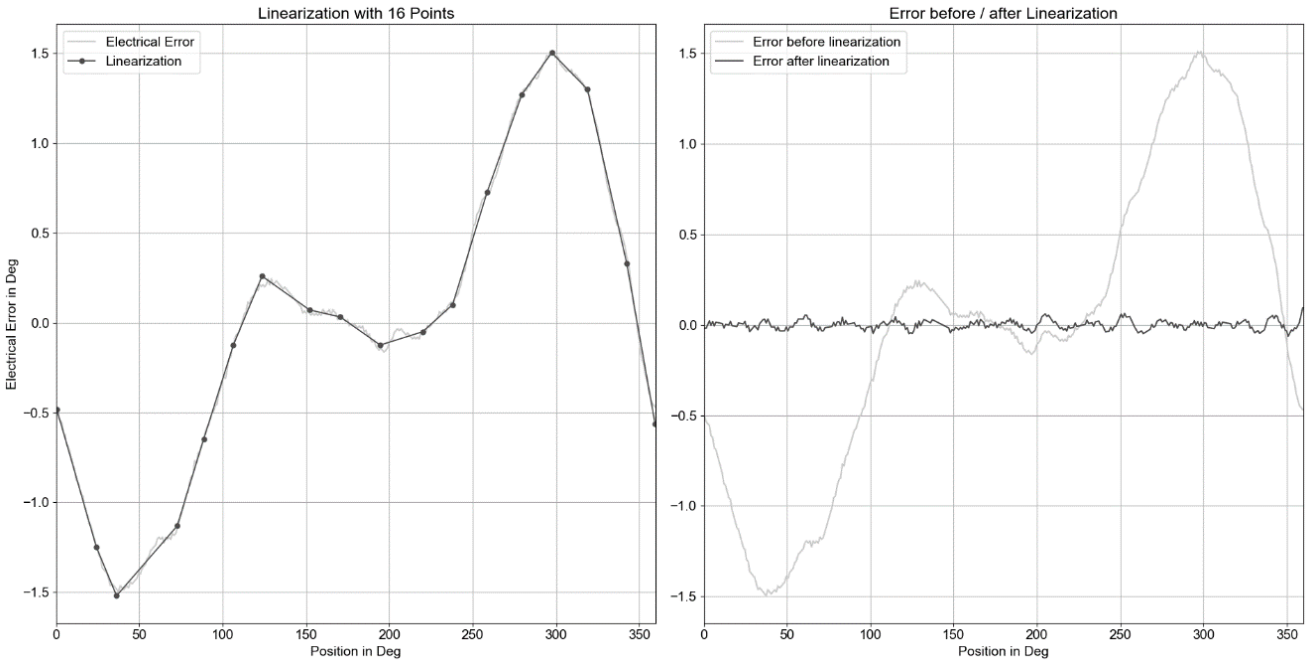


Figure 11. Example of 16-Point Linearization

Table 13. Linearization Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
N_{P_Lin}	Number of linearization points				16	
$Grid_{LIN}$	Placement grid of linearization points	In X and Y		0.088		°el
Res_{Lin}	Resolution of linearization transfer function	X and Y coordinates		12		bits

Note: The slope of each segment ($\Delta Y / \Delta X$) is automatically calculated from the X and Y parameters of adjacent linearization points. If two adjacent points are positioned with a slope outside the specified range (see Table 13), the slope is reset to 0 to prevent an overflow of the calculated slope value.

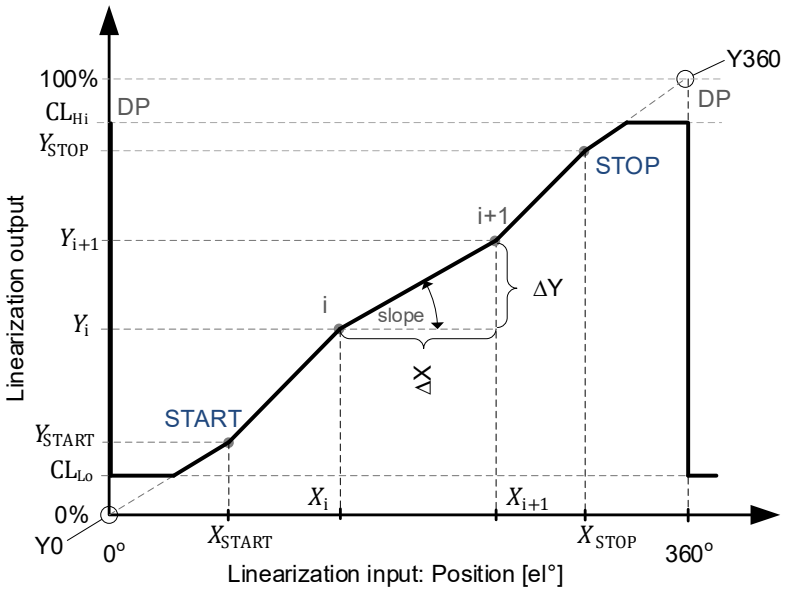


Figure 12. Linearization Transfer Function Parameters

Table 14. Linearization Parameter Settings

Parameter	Description	Programming Options	Resolution
P_{Lin}	Number of linearization options	0,2,4,6,8,16	
D_P	Discontinuity point, Zero position transition from 0°/360°	0° to <360° el.	0.088°el. per LSB
X_{Start}	Mechanical start position, first linearization point		
Y_{Start}	Expected output at XStart, first linearization point		
X_i	Mechanical position of linearization point (i = 1 to 16, including start and stop)		
Y_i	Expected output at linearization point (i = 1 to 16 including start and stop)		
X_{Stop}	Mechanical end position, last linearization point		
Y_{Stop}	Expected output at XStop, last linearization point		
CL_{Hi}	Output Clamping level, high	0% to 100% VDD	12 bits (VDD / 4096) per LSB
CL_{Lo}	Output Clamping level, low		
Y0	Position at DP, start value at X = 0°	0° / 360° el.	
Y360	Position at DP, stop value at X = 360°	0° / 360° el.	

5. Interfaces

The RAA2P4500 offers an Analog Output, a PWM, a SENT and an I2C. A summary is shown in Table 15.

Table 15. Interfaces Overview

Interfaces	Number of I/f Wires	Resolution	Features	Other options
Analog Output	1	12 bit	Analog out Position update rate: 20 KHz	Digital Output (pin 12)
PWM	1/2	12 / 14 bit	PWM output (push-pull or open drain) PWM frequency: 109 Hz to 4376 Hz	Digital Output (pin 12)
SENT	1	12 / 14 bit	Programmable tick time: 0.02 to 6 µs Fast Channel / Enhanced Serial Message	Auxiliary Analog input (pin 10) Digital Output (pin 12)
I2C	2	14 bit	Interface speed: 400KHz Fastest position update rate 5.4 KHz	Digital Output (pin 13)

5.1 Analog Interface

An analog interface is included to accommodate legacy applications that utilize potentiometers or position sensors with linear ramp output, such as magnetic position sensors.

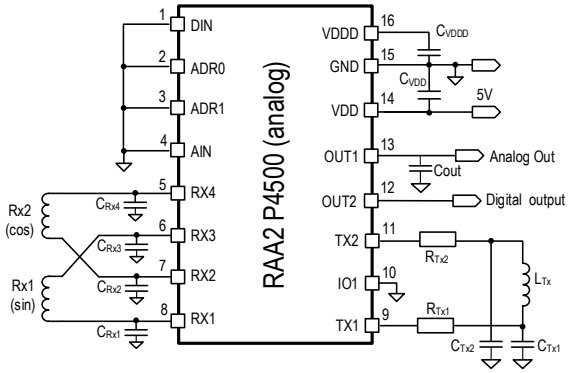


Figure 13. Analog Interface Input/Output Pins

The analog output is generated by converting the digitally processed angle data into an analog voltage through a 12-bit DAC and an analog output buffer. This buffer is protected against overvoltage, reverse polarity, overcurrent, and short circuits to GND and positive supply voltage.

The full electrical 360° range is operational, with programmable clamping levels from 5%VDD to 95%VDD, see Figure 14 and Table 16). The analog position is indicated as a linear ramp between these clamping levels, and the output voltage is ratiometric to the supply voltage VDD, ensuring stability against supply voltage changes.

Adjusting the clamping level limits allows for full range mapping (0° to 360°) over a 5 to 95 VDD% voltage range. Diagnostic mode is indicated by a high-ohmic tri-state mode, detectable as an out-of-range voltage level with external pull-up or pull-down resistors. Broken ground or broken supply condition can also be detected this way.

A separate digital output pin (pin 12) indicates additional information, such as an out-of-range position or out-of-range magnitude or magnitude value (PWM).

Table 16. Analog Interface User Programming Options

Analog Interface Programming Parameter	Number of Options	Programming Option
Output high clamp level	4096	0% to 100% VDD in 12-bit steps
Output low clamp level	4096	0% to 100% VDD in 12-bit steps

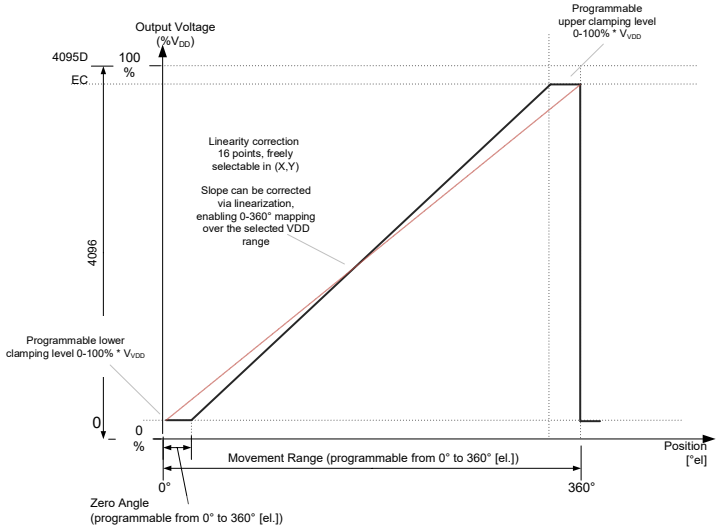


Figure 14. Analog Output Transfer Function

5.2 PWM Interface

The PWM interface can be configured for single wire PWM interface with push-pull or open drain output, as well as a dual wire differential PWM interface with push-pull outputs. In differential mode, an inverted signal is provided on pin 10 as shown in Figure 15.

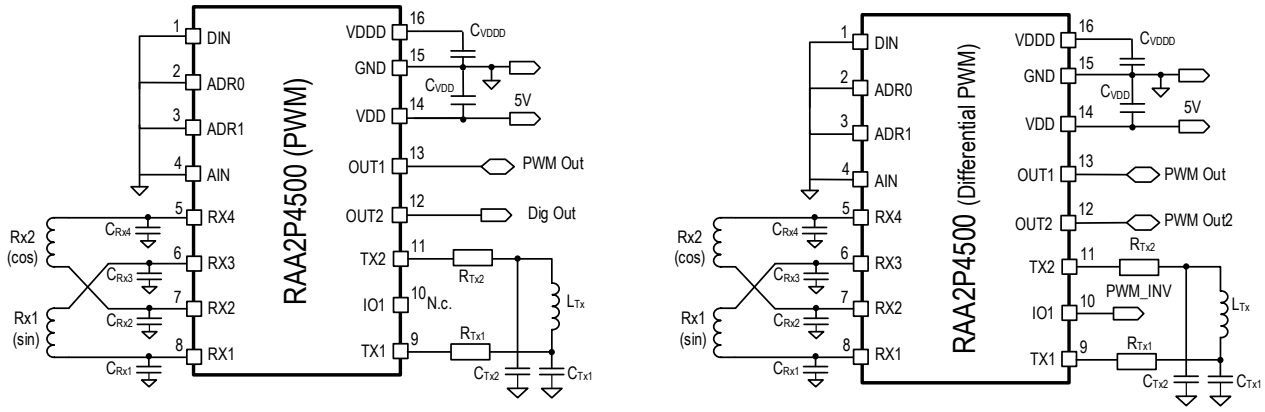


Figure 15. PWM Interfaces (Standard and Differential Mode) Input/Output Pins

Table 17. PWM Interface User Programming Options

PWM Programming Parameter	Number of Options	Programming Option
PWM frequency	8	109Hz, 219Hz, 547Hz, 1094Hz, 1641Hz, 2188Hz, 3282Hz, or 4376Hz
PWM output mode	2	Push-pull or Open-drain
PWM polarity	2	Position information is Active Low or Active High
PWM resolution	2	12-bit (all PWM frequencies) or 14-bit (PWM frequencies: 109Hz to 1094Hz)
Diagnostic mode indicated by PWM signal	3	Disabled, Diagnostic mode enabled with low duty cycle, Diagnostic mode enabled with high duty cycle

The 12-bit non-inverted PWM signal frame consists of a 256 LSB high level header, followed by the 12-bit Position Data, which ranges from 0 to 4095 LSBs high-level and the corresponding number of low-level LSBs to complete a total length of 4095 LSBs. The frame is terminated with a 256 LSBs low-level trailer as shown in Figure 16. The PWM signal can also be inverted, resulting the signal frames shown in Figure 16 and Figure 17.

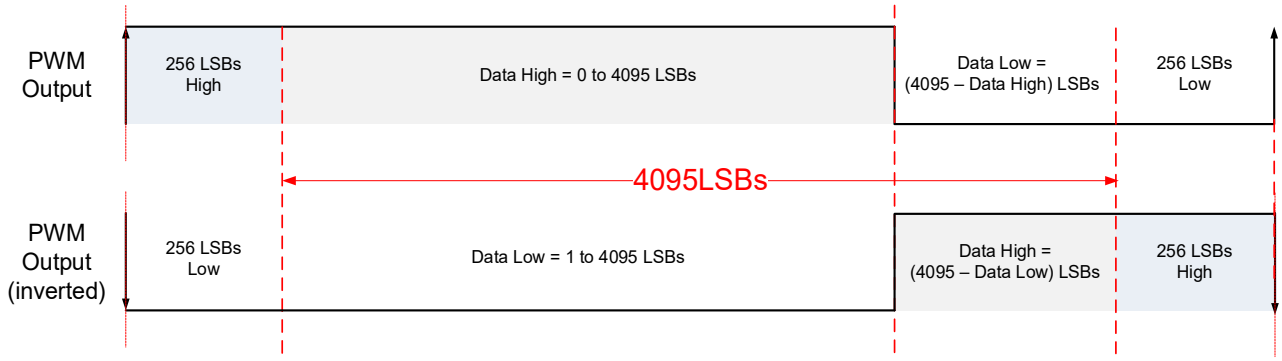


Figure 16. 12-bit PWM Signal in Normal Operation Mode

The minimum 12-bit duty cycle can be calculated with Position data = 0 LSB high, 4095 LSBs low:

$$DC_{min} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{256}{256 + (4095 + 256)} = 5.557\%$$

Equation 13

The maximum 12-bit duty cycle can be calculated with Position data = 4096 LSBs high, 0 LSBs low:

$$DC_{max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{256 + 4095}{(256 + 4095) + 256} = 94.443\%$$

Equation 14

The 14-bit PWM signal frame shown in Figure 17 is structured similarly to the 12-bit PWM signal frame shown in Figure 16, with the key difference being an increased resolution by a factor of 4.

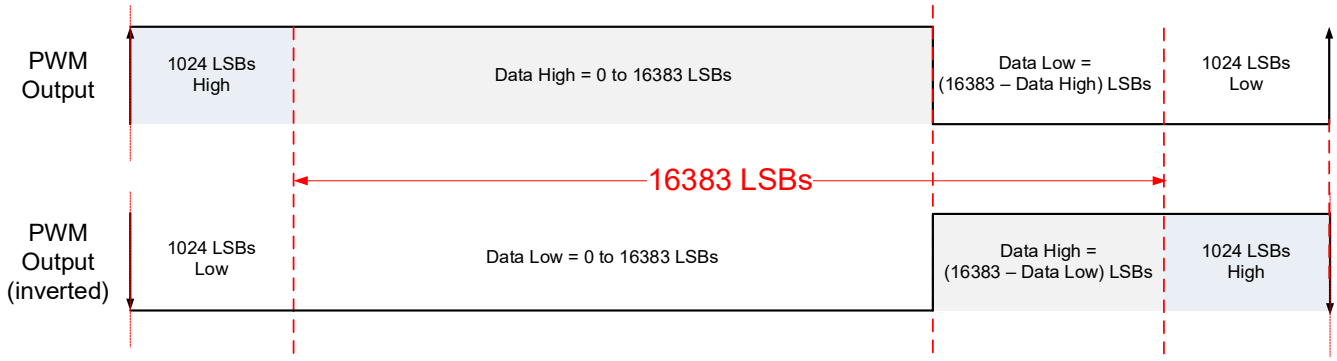


Figure 17. 14-bit PWM Signal in Normal Operation Mode

The minimum 14-bit duty cycle can be calculated with Position data = 0 LSB High, 16383 LSBs low:

$$DC_{min} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{1024}{1024 + (16383 + 1024)} = 5.556\%$$

Equation 15

The maximum 14-bit duty cycle can be calculated with Position data = 16384 LSBs High, 0 LSBs low:

$$DC_{max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{1024 + 16383}{(1024 + 16383) + 1024} = 94.44\%$$

Equation 16

5.2.1 PWM Diagnostics Mode

In PWM diagnostics mode, the duty cycle is forced to a range not utilized in normal operation. This mode can be configured as the following:

- Diagnostic low mode, see Figure 18 and Figure 20;
- Diagnostic high mode, see Figure 19 and Figure 21;

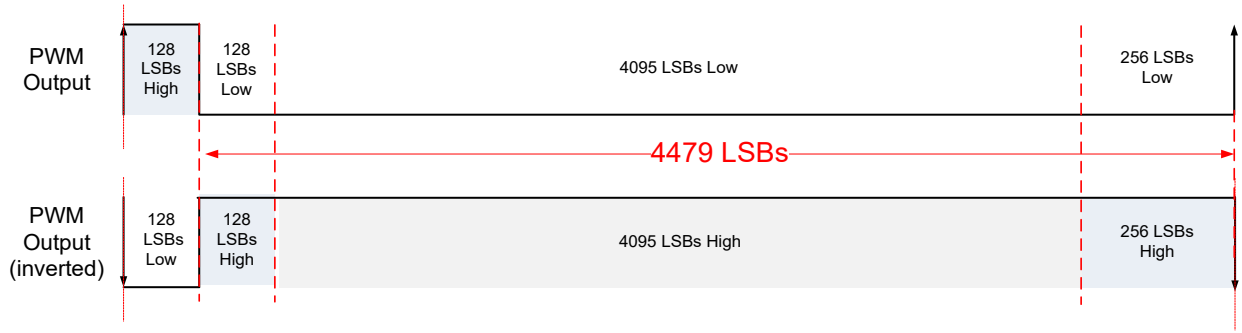


Figure 18. 12-bit PWM Signal in Diagnostics Low Mode

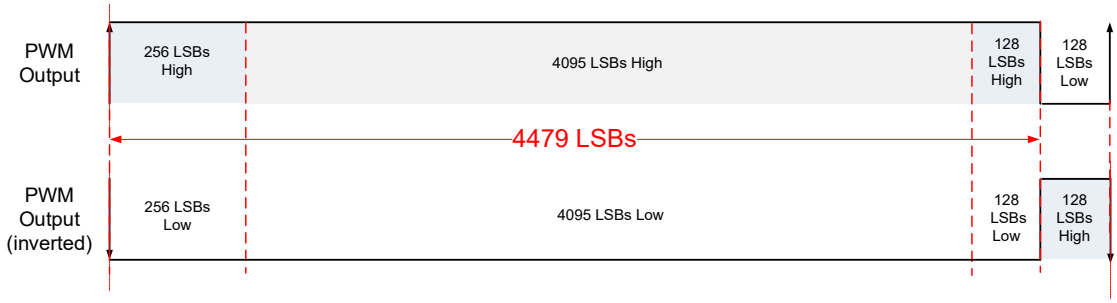


Figure 19. 12-bit PWM Signal in Diagnostics High Mode

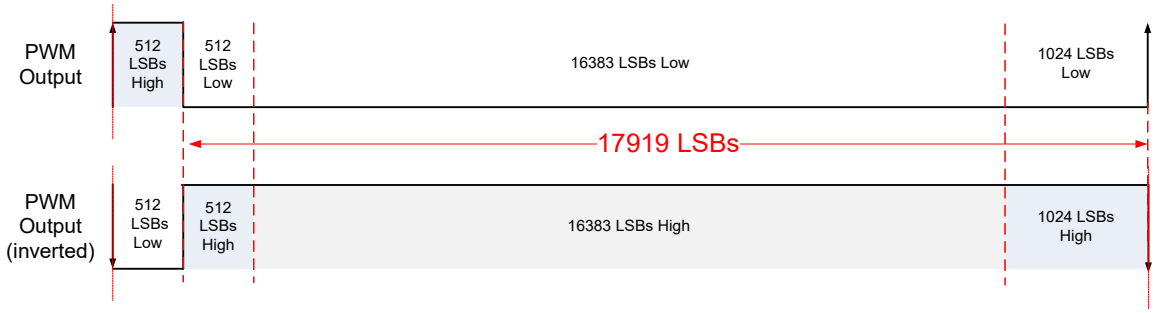


Figure 20. 14-bit PWM Signal in Diagnostics Low Mode

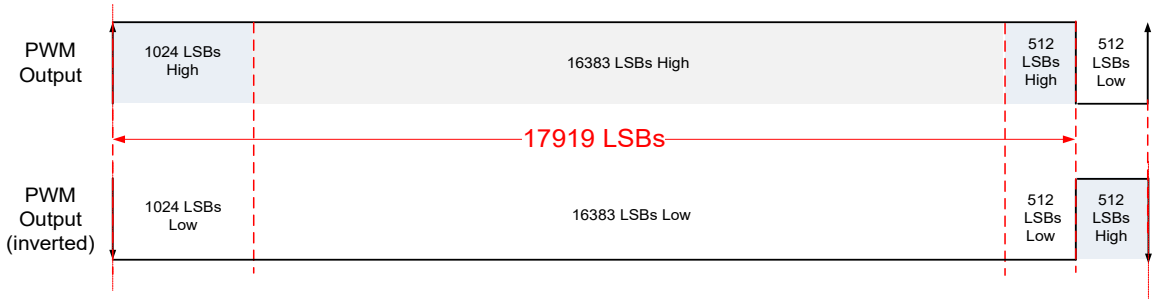


Figure 21. 14-bit PWM Signal in Diagnostics High Mode

5.3 SENT Interface

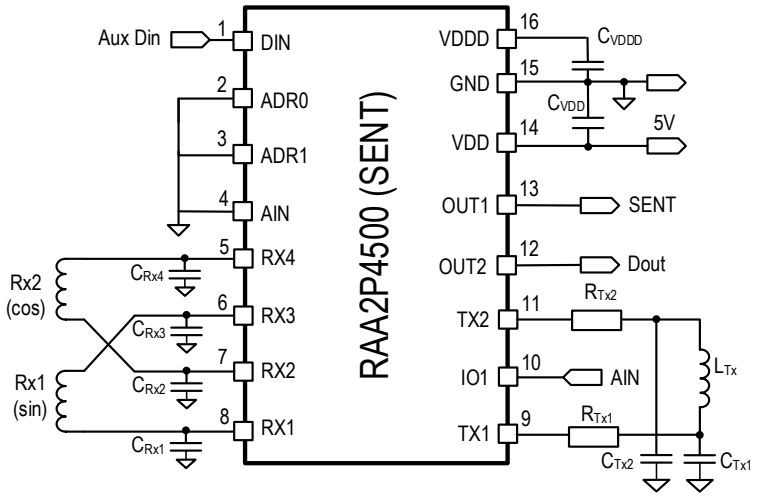


Figure 22. SENT interface Input/Output Pins

The sensor is equipped with a SENT interface compliant with SAE J2716 Standard (Rev. April 2016). The main features are:

- Configurable tick time (1.5µs, 3us, 6us with pulse shaping output, down to 0.1µs with push-pull output).
- Configurable pause pulse.
- Support Enhanced Serial message with 8-bits ID and 12-bits data.
- 8 different fast channel configurations.
- Serial message cycle length is selectable between 16 or 32 messages.
- Signal shaping for reduced EMI.

Table 18. SENT Interface User Programming Options

SENT Programming Parameter	Nr. of Options	Programming Option
SENT tick time	1024	0.02 to 6µs Note: <1.5µs tick time in push-pull mode only
SENT fast channel frame	3	see Table 21
SENT pause pulse	3	No pause, fixed length pauses, Constant frame length, see Table 20
Serial message protocol	3	Disabled, 16 or 32 messages (see Table 22 and Table 23)
CRC calculation method	2	As defined by SENT Standard SAE-J2716, Apr2016: “recommended” or “legacy” calculation method

5.3.1 SENT Protocol Frame

The SENT protocol frame consists of a fixed-length synch pulse (LOW period of 5 ticks followed by a HIGH period of 51 ticks), followed by a status nibble, 6 data nibbles, and a CRC nibble. An optional pause pulse can be programmed to adjust the SENT frame to a fixed length of 270 ticks.

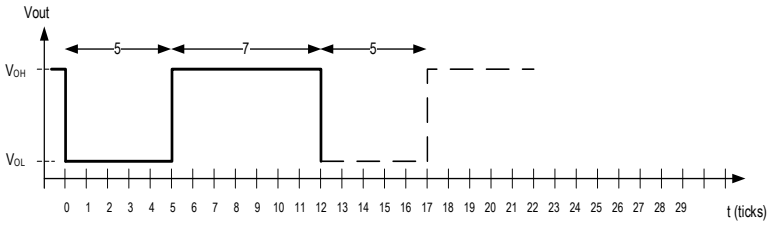


Figure 23. SENT Nibble Output for Value = 0_{DEC}

For transmitting a nibble with the 0 value, 12 clock ticks are required: a fixed LOW period of 5 ticks followed by a HIGH period of 7 ticks.

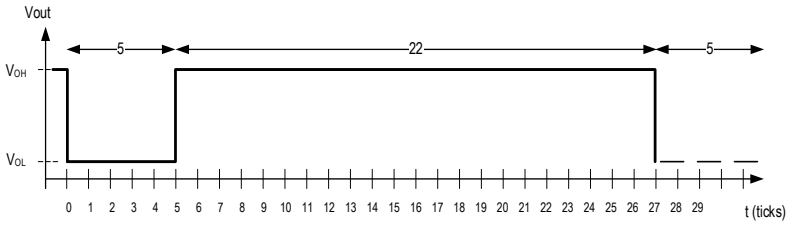


Figure 24. SENT Nibble Output for Value = 15_{DEC}

For transmitting a nibble with the value 15_{DEC} (1111_{BIN}, F_{HEX}), 27 clock ticks are required: a fixed LOW period of 5 ticks followed by a HIGH period of 22 ticks.

The total time for one nibble can be calculated as with the following equation:

$$t_{NIBBLE} = t_{TICK}*(12 + x) \qquad \textbf{Equation 17}$$

Where x = the nibble decimal value = 0 to 15.

t_{TICK} = the length of one tick, which is programmable

Table 19. SENT Tick Counts

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
Number of Ticks	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27

The tick time can be programmed in a wide range from 0.02 to 6µs, see Table 18. Shown in Table 20 are examples for the most common tick times, 1.5µs, 3.0µs and 6.0µs.

Table 20. SENT Tick Time Programming Options

SENT Tick Time t_{TICK}	SENT Frame Length without Pause Pulse		SENT Frame Length with Pause Pulse (Programmable)	
	Total Frame Length (Min 154 Ticks)	**Total Frame Length (Max 270 Ticks)**	**Constant Frame Minimum = 282 Ticks**	**Constant Frame Maximum = 922 Ticks**
1.5µs	231µs	405µs	423µs	1383µs
3.0µs	462µs	810µs	846µs	2766µs
6.0µs	924µs	1620µs	1692µs	5532µs

5.3.1.1 Operation and Frame Format

The SENT transmitter controller supports both fast channel message and serial message formats.

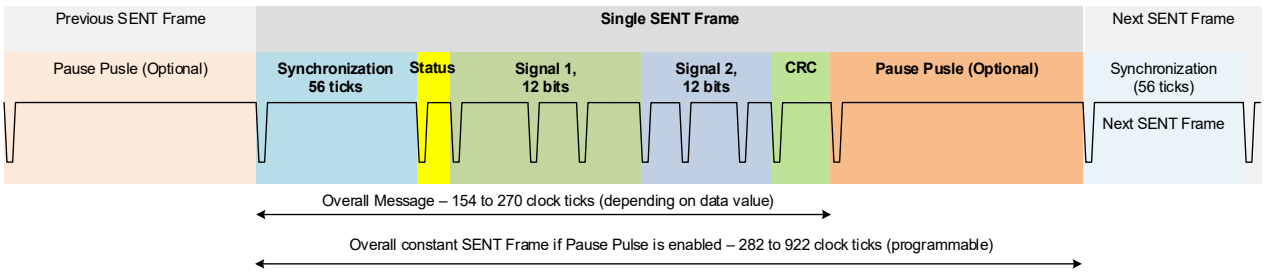


Figure 25. SENT Typical Frame

Several fast channel modes are available, combining primary and analog inputs with turns counter, see Table 21 .

Table 21. SENT Fast Channel Frame Options

SENT Fast Channel Frame									
Nibble #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**SAE J2716 Reference:**
Programming Option:	Status	Signal 1 (12-bit)			Signal 2 (12-bit)			CRC	
Option 0: “Secure Angle Sensor”	Status	12-bit MSB position data (Receiver coils) MSN → LSN			8-bit rolling counter		4-bit inverted MSB	CRC	H.4: 12+8+4 bits
Option 1: "Dual Throttle Sensor": Coil position (12 bit) + Analog input (12 bit)		12-bit MSB position data (Receiver coils) MSN → LSN			12-bit analog input LSN → MSN				H.1: 12+12 bits
Option 2: " Dual Throttle Sensor”: Coil position (14 bit) + Analog input (10 bit)		14-bit MSB position data MSN → LSN			10-bit analog input LSN → MSN				14+10 bits
Option 5: Coil position (14bit) + turns counter (10LSBs)		14-bit position data (Receiver coils) MSN → LSN			10 LSBs turns counter (Receiver coils) LSN → MSN				H.6: 14+10 bits

Notes:

- the internally calculated resolution is always 14bits@360°. For options 0 and 1, where 12-bits position data are selected, the 12 MSBs of the 14-bit position data are transmitted.
- Turns counter functionality counts the number of electrical periods that have been detected on the receiver coils. This information is decoded in a 12-bit register and stored in an internal register also available via I2C interface or provided via SENT. This functionality can also be configured to count pulses on DIN input, more info in section 6.1.1.
- The status nibble bits:
  - S[3:2] contain the enhanced serial message, and they are constat zero if the enhanced serial message is disabled.
  - S[0] contains the temporary diagnostic state of the IC.
  - S[1] is zero.

5.3.1.2 Enhanced Serial Message

The enhanced serial protocol message format consists of an 8-bit ID and 12-bit data with 6-bit CRC per frame. In addition, two sets of serial protocol messages are programmable: 16 frames or 32 frames.

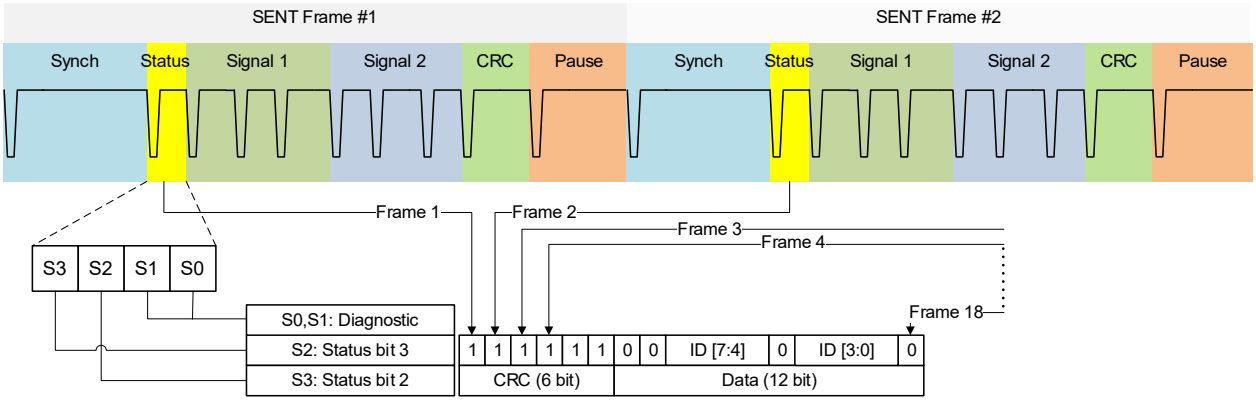


Figure 26. Enhanced Serial Protocol Message Format

Table 22. SENT 12-bit Enhanced Serial Protocol Data (Data Frames 1 - 16)

Frame #	ID (8-bit)	Description	Source Data (12-bit)
1	01 Hex	Diagnostic Status 1	Mapped to internal status registers: irq_sts0[11:0]
2	03 Hex	Ch1, Ch 2 sensor type	Sensor type according to SENT specification: cust_id2[15:8]
3	05 Hex	Manufacturer Code	Manufacturer Code for RENESAS
4	06 Hex	SENT Standard Revision	04 =SENT Revision 4 J2716 APR2016
5	83 Hex	Diagnostic Status 2	Mapped to internal status registers: irq_sts0[15:12], irq_sts1[7:0]
6	23 Hex	Chip temperature	Internal temperature register: chip_temp
7	29 Hex	Sensor ID #1	USER_ID0: cust_id0[11:0]
8	2A Hex	Sensor ID #2	USER_ID1: cust_id1[7:0], USER_ID0: cust_id0[15:12]
9	84 Hex	Diagnostic Status 3	Mapped to internal status registers irq_sts2[3:0], irq_sts1[15:8]
10	90 Hex	OEM ID #1	Product ID [7:0] bits: prod_id
11	88 Hex	ADC raw SIN data	Rx Coil's ADC raw sine data, 11MSBs out of 13-bits and bit denoting inversion adc_raw_sin[13:2]
12	16 Hex	Turns Counter	12-bit Turns counter / Pulse counter angle1_turns
13	85 Hex	Diagnostic Status 4	Mapped to internal status registers: irq_sts2[15:4]
14	80 Hex	Reserved	Reserved
15	81 Hex	Reserved	Reserved
16	89 Hex	ADC raw COS data	Rx Coil's ADC raw cosine data, 11MSBs out of 13-bits and bit denoting inversion adc_raw_cos[13:2]

Table 23. SENT 12-bit Enhanced Serial Protocol Data (Data Frames 17-32)

Frame #	ID (8-bit)	Description	Source Data (12-bit)
17	86 Hex	Diagnostic Status 5	Mapped to internal status registers irq_sts3[11:0]
18	17 Hex	Reserved	Reserved
19	10 Hex	Reserved	Reserved
20	12 Hex	AGC setting	Coil AGC: angle1_gain
21	87 Hex	Diagnostic Status 6	Mapped to internal status registers: irq_sts3[15:12]
22	1C Hex	Analog Input	Analog input, 12 MSBs out of 13-bits: adc_hk_ana_in[12:1]
23	1D Hex	Analog reference voltage (VDDD)	Analog input reference (VDDD) 12 MSBs out of 13-bits: adc_hk_vdda_ref[12:1]
24	18 Hex	Reserved	Reserved
25	01 Hex	Diagnostic Status 1	Mapped to internal status registers: irq_sts0[11:0]
26	91 Hex	OEM ID#2	0x632 (ASCII coded “RA”)
27	2B Hex	Sensor ID #3	cust_id2[3:0], cust_id1[15:8]
28	2C Hex	Sensor ID #4	cust_id2[7:4]
29	82 Hex	Digital Input State	Mapped to internal status registers: reg_flag_din2[0]
30	92 Hex	OEM ID#3 (optional)	0x4A1 (ASCII coded “A2”)
31	93 Hex	OEM ID#4 (optional)	0x430 (ASCII coded “P0”)
32	94 Hex	OEM ID#5 (optional)	0x410 (ASCII coded “00”)

5.4 SENT Load Circuits

Load circuit components are shown in Figure 27 for the legacy SENT interface and Figure 28 for the recommended SENT interface. All components are specified according to specification SAE J2716 – APR2016, see Table 12.

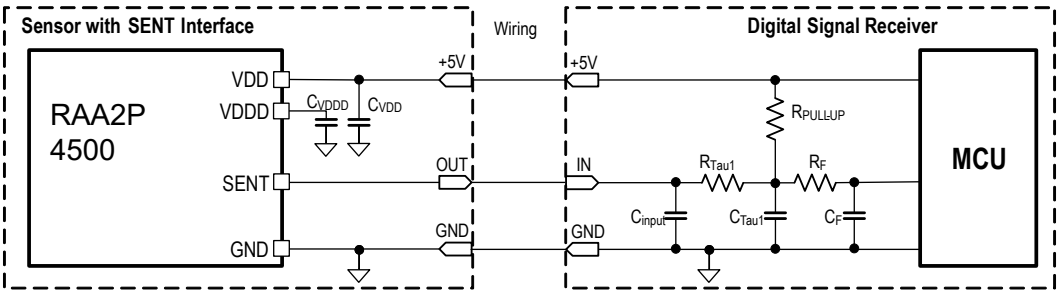


Figure 27. Legacy SENT Interface Load Circuit

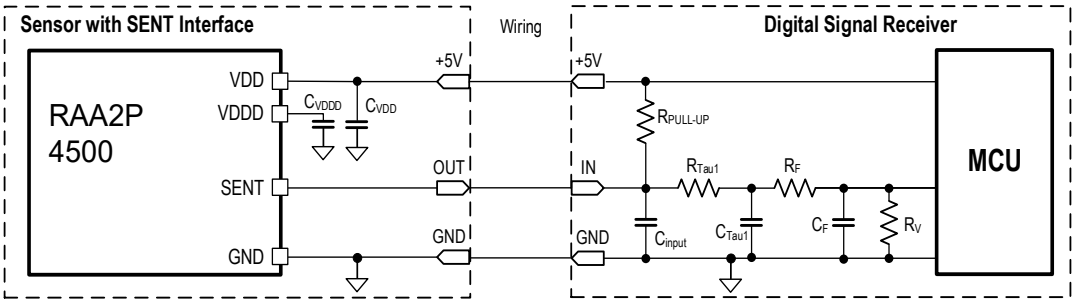


Figure 28. Recommended SENT Interface Load Circuit

5.5 I2C Interface

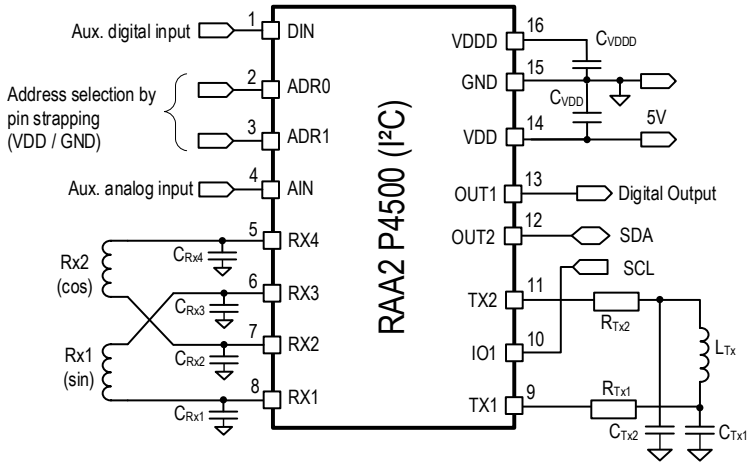


Figure 29. I2C Interface Input/Output Pins

The RAA2P4500 can be programmed for an I2C interface according to the UM10204 I2C-bus specification, utilizing pins 10 (SCL) and 12 (SDA) to address up to 14 slaves over the same 2-wire interface. The interface does not support clock stretching, 10-bit slave address, general call address, software reset, or device ID.

5.5.1 I2C Addressing

The I2C address is programmable in the NVM, and two hardware address select pins, pin 2 (ADR0) and pin 3 (ADR1), provide interface address selection by hardware pin strapping.

Figure 30 shows an example where one device is pin strapped to I2C address 0x72, while the second device is pin strapped to address 0x70. Once each device is separately selected, it can be addressed using its unique NVM I2C address.

Table 24. I2C Interface User Programming Options

I2C Programming Parameter	Number of Options	Programming Option
I2C slave address	14	See Table 25
I2C address select by pin strapping	1	Enable/Disable (2 LSBs)
I2C CRC check for Rx data	1	Enable/Disable
I2C CRC check for command data	1	Enable/Disable
I2C protocol error detection	1	Enable/Disable

Table 25 details the various options for selecting the I2C Address, utilizing combinations of pin addressing and NVM address register setting.

Table 25. I2C Address Selection Options in NVM

Address Selection Mode	A6	A5	A4	A3	A2	A1	A0
Default setting	1	1	1	0	0	Pin 3 = ADR1	Pin 2 = ADR0
User programmable range, with I2C address selection by pins 2 and 3	0x02 to 0x1D					Pin 3 = ADR1	Pin 2 = ADR0
User programmable range, with fixed I2C address	0x08 to 0x77						

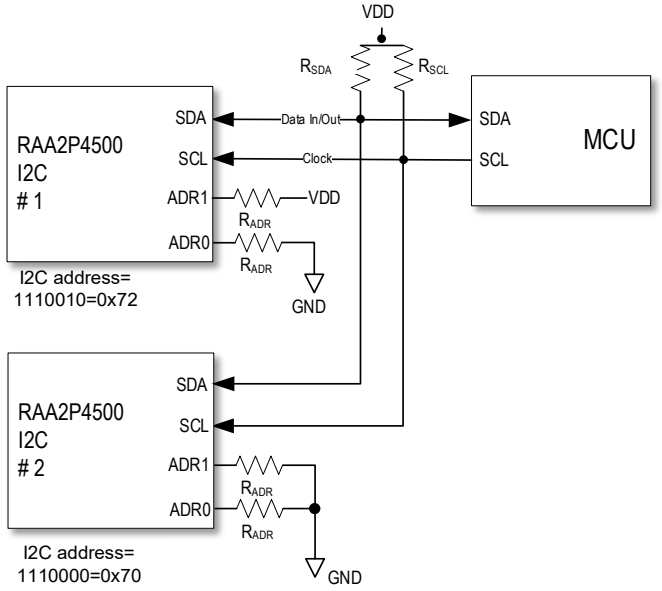


Figure 30. I2C Interface with Address Select

5.5.2 I2C Register Write

To access a register, the slave address must be sent by the master, followed by two bytes of register address (*MemAddr*), one byte of CRC data, and then by the write data *WrData*. If the CRC check is disabled, keep the CRC frame at zero. The write data consists of two bytes of data followed by one byte of CRC data as shown in Figure 31.

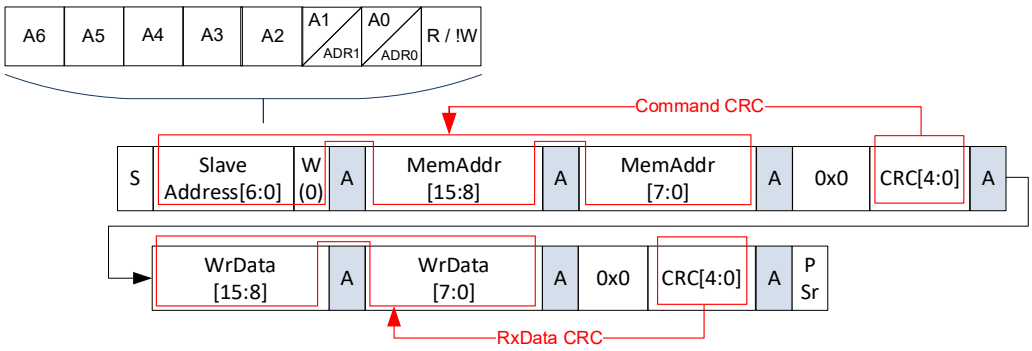


Figure 31. I2C Register Write Access

5.5.3 I2C Register Read

To read a register over the I2C interface, the master sends a write register command frame followed by a repeated start (*PSr*) and slave address with a read bit set. Upon acknowledgement, the device responds with two bytes of data followed by one byte CRC as shown in Figure 32.

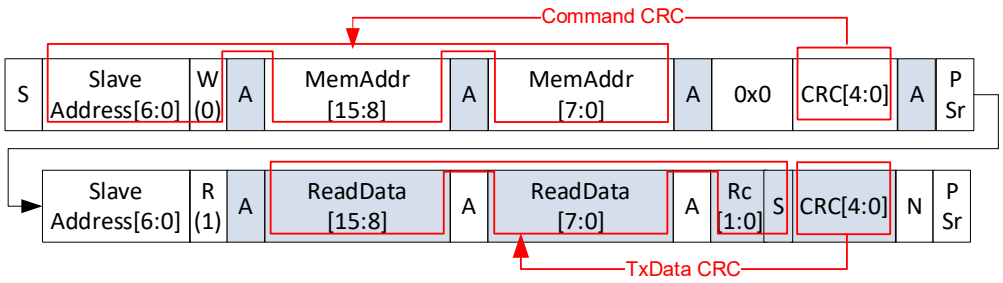


Figure 32. I2C Register Read Access

5.5.4 I2C CRC Check

For optimal communication with the RAA2P4500, it is recommended to enable the CRC check for I2C communication. Enabling it ensures that the device only responds to command frames that include correct CRC data. For more details, please refer to the *RAA2P4500 Programming Manual* document.

5.5.5 UART Single Wire Programming Interface

Any user programmable parameter can be accessed through the single wire programming process, using a half-duplex UART protocol.

Performing an end-of-line calibration or in-line programming of a position sensor module containing the RAA2P4500, requires no additional wires. The chip is programmed through the OUT1 output at the operative supply voltage range (5V ±10%, 3.3V ±10%).

A short programming window is enabled after POR and requires a digital unlock password to enable programming. If no password is sent, the chip resumes its normal operating mode.

For more details, please refer to the *RAA2P4500 Programming Manual* document.

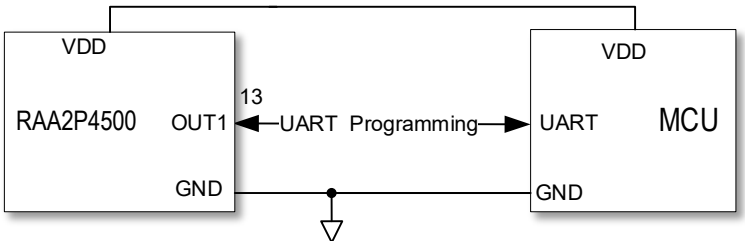


Figure 33. UART Single Wire NVM Programming

5.5.5.1 Lock Feature

The RAA2P4500 includes a user configurable lock bit option, which can be set to restrict write and/or read access. Once the lock bits are enabled, further write or read operations to the RAA2P4500 are prohibited. Note that once a RAA2P4500 part is locked, it cannot be unlocked.

For more details, refer to the *RAA2P4500 Programming Manual* document.

6. Auxiliary Inputs and Outputs

Two auxiliary inputs are available for connecting external devices with analog or digital PWM interface, that can be read through the I2C interface. Further, a digital output pin is available indicating user programmable features. A summary is shown in Table 26.

Table 26. Auxiliary Inputs and Digital Output Options

Interface	Analog Input	Digital Input	Digital Output		
			Register Flag (OD)	Magnitude Alarm (OD)	Magnitude PWM (PP/OD)
Analog	n/a	n/a	n/a	Yes (pin 12)	Yes (pin 12)
PWM	n/a	n/a	n/a	Yes (pin 12)	n/a
Differential PWM	n/a	n/a	n/a	n/a	n/a
SENT	Yes (pin 10)	Yes (pin 1)	n/a	n/a	n/a
I2C	Yes (pin 4)	Yes (pin 1)	Yes (pin 13)	n/a	n/a

6.1.1 Digital Input

The digital input (DIN) available on pin 1 can read static (high/low) signals or to received count pulses. The number of pulses information is available via I2C and SENT (Turns Counter register).

6.1.2 Analog Input

The analog input is available on pin 4 (AIN) for I2C or pin 10 (IO1) for SENT; it can be used to read analog voltages from external sensors. See Table 27 for the key parameters of this input. The analog value must be in relation to VDDD.

Table 27. AIN Analog Input Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IN_AIN}	AIN voltage range		0.1		1.2	V
RES_{AIN}	ADC resolution			12		bits
T_{Smp_AIN}	Sampling rate		4.4			kHz
ACC_{AIN_pin4}	Analog Input Accuracy AIN Pin 4		-1.2		1.2	%VDDD
ACC_{AIN_pin10}	Analog Inout Accuracy IO1 Pin 10	12-bit configuration	-1.5		1.5	%VDDD
		10-bit configuration	-1.55		1.55	%VDDD

Both the analog input and the VDDD reference voltages are internally measured and stored in registers or sent in the SENT enhanced serial message. The external load on VDDD cannot exceed 4 mA as specified in Table 4.

6.1.3 Digital Output

An optional digital output is available and can be configured for various functions, depending on the selected interface, as shown in Table 26.

6.1.3.1 Register Flag

In I2C configuration, the DOUT output can be used to drive external circuits. DOUT is on OUT1 pin for I2C. It is controlled by writing either of the following options to the address 0x029E [0]:

- Register bit 0: FLG output is low
- Register bit 1: FLG output is high

This function can be integrated with a heartbeat feature to provide diagnostic status information alongside the flag value. This status is indicated by a 1.5KHz pulse, see Figure 34 with a duty cycle of 97% when the flag is high and 3% when the flag is low.

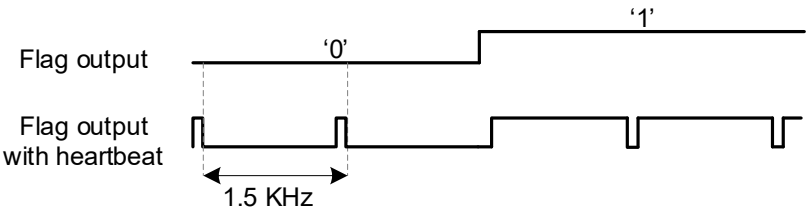


Figure 34. Flag Output Configurations

6.1.3.2 Magnitude Information over PWM

If the analog interface is selected, the magnitude information of the receiver coils is available in PWM format on the digital output with the same 12-14 bit resolution as described in section 5.2.

6.1.3.3 Magnitude Alarm

In analog and PWM interface, the DOUT can be used to trigger an alarm if the amplitude of the receiver signal rises/falls above/below NVM-programmable thresholds.

7. On-Chip Diagnostics (Safety Mechanisms)

The RAA2P4500 includes on-chip diagnostics featuring an extensive number of internal Safety Mechanisms.

It has been developed according to ISO26262 for implementation in safety-relevant systems up to ASIL C. It can also be used in ASIL D system-level requirements according to ASIL Decomposition rules (f.e. ISO 26262:2018, Part 9, Clause 5") or proper risk analysis by the system integrator.

For a more detailed description, see the *RAA2P4500 Programming Manual* and *RAA2P4500 FuSa Manual* documents.

Table 28. Diagnostic Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_{FDTI}	Failure detection time interval (time to detect and internally set a flag describing the error condition)	fdti_cfg=1			2.3	ms
		fdti_cfg=0			20	ms

Table 29. Safety Mechanisms

Category	Safety Mechanisms (SM)	Description
Monitoring of external supply	VDD Monitor	External VDD supply out of range
Monitoring of internal supplies	VDDA Monitor	Internal VDDA (Analog supply) out of range / undervoltage /overvoltage
	VDDD Monitor	▪ Internal VDDD (Digital supply) out of range ▪ Short on VDDD ▪ Overcurrent at VDDD pin
	Internal Supply Monitor	Internal supply out of range
	Internal pre-regulators Monitor	▪ Internal pre-regulator for power management (bandgap, analog parts) out of range ▪ Internal pre-regulator for output stages out of range
	Driver Regulator Monitor	OUT2 regulator driver out of range
	Oscillator Regulator Monitor	LC oscillator regulator out of range
	Bias Current Monitor	Bias current diagnostic out of range

Category	Safety Mechanisms (SM)	Description
Monitoring of RX coils	RX coil Sine Monitor	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX SIN
	RX coil Cosine Monitor	▪ Short of the RX vs GND or VDD ▪ Broken wire detected on RX COS
	RX coil Sine/Cosine neighbor inputs short	Short check between Sine/Cosine coil set detected
Monitoring of TX coils	TX Voltage Monitor	▪ Common mode voltage of TX1/TX2 out of range ▪ Flag for broken pins of LC oscillator
	LC Oscillator Monitor	▪ LC oscillator stuck detected ▪ LC oscillator frequency out of range
Monitoring of system clock	System clock Monitor	▪ Fault in internal system clock: frequency out of range ▪ Fault in internal system clock: stuck detected
Monitoring of the internal communication channel	Internal digital logic failure Monitor	Internal digital logic failure detected such as APB Diagnostic failure, IC internal registers failure, FSM failure, CORDIC failure, other digital failures.
Monitoring the internal memory	Non-Volatile Memory Monitor	▪ CRC mismatch over the NVM or internal shadow register ▪ NVM read timeout fail
Data path diagnostics	Data path WD/OF/UF/DO Monitor	Internal errors, such as overflow, underflow, division by 0, or watchdogs
Signal Path Monitoring	Signal path monitoring from Analog Front End to CORDIC calculation	▪ Reference angle failure ▪ Reference Magnitude failure
Temperature monitoring	Temperature Monitor	▪ Temperature warning detected ▪ Temperature error (shutdown) detected
Magnitude evaluation	Magnitude static Monitor	Magnitude static check error detected on RX coils
Monitoring of analog signal path offset	ADC temperature sensor offset fail Monitor	Compensation of the internal offset not sufficient
Monitoring of the mechanical stress /cracks	Broken chip check Monitor	IC die mechanical failures detected
LPF check for signal path	LPF Monitoring	Failure in internal LPF
AGC monitoring	AGC error Monitoring	▪ Automatic gain control loop not converging ▪ Pre-defined acceptable gains for the AGC not sufficient for RX coil
Monitoring of the output interfaces	Output Interfaces monitors	▪ Failure of the I2C interface ▪ Failure of the SENT interface ▪ Failure of the PWM interface
Analog input	Analog Input Monitoring	Failure on analog input range
OUT2 and IO1 pins monitoring	OUT2/IO1 pins Monitoring	▪ Overvoltage/undervoltage ▪ Short on OUT2/IO1 detection

A fault from a broken or short wire refers to the connection between sensor IC and control unit (MCU, ECU), including the soldering of the IC pins, PCB traces, connectors and cables. In this case, the diagnostic state depends on whether pull-up/pull-down resistors are installed at the receiver side.

7.1 Broken Wires

In analog output mode during normal operation, the analog output can be programmed to operate between VOUT ≥5% VDD and VOUT ≤95% VDD. In case of a diagnostic error, the output is turned off and enters a high-ohmic state. External pull-up/pull-down resistors are pulling the output voltage VOUT outside of its functional operating range thus indicating the error condition.

Most broken supply, broken GND, or analog output signal connection errors can be detected by monitoring the DC voltage levels at the analog output pin AOUT, see the uncritical error cases on Figure 35. If a diagnostic error or broken signal wire occurs, the DC voltage level at the affected pin is pulled into the diagnostic range (diagnostic high: VOUT >95% VDD or diagnostic low: VOUT <5% VDD) through the external pull-up/pull-down resistors.

For the following cases, a parasitic current inside the RAA2P4500 may cause unwanted, too high voltage drops across the pull-up/pull-down resistors. Depending on the value of the external resistor, this may not properly indicate the error condition:

- a broken VDD supply wire with external pull-up resistors at the receiving end, see Figure 35.
- a broken GND wire with external pull-down resistors at the receiving end, see Figure 35.

For these special cases, the maximum resistance value for these resistors must be observed, see Table 30 and Table 31.

Table 30. Diagnostic Levels with Pull-Up Resistors

Diagnostic Level	>96% VDD	Unit
Error indication during normal operation	≤9.1	kΩ
Broken GND line	Not critical, see the uncritical error cases.	kΩ
Broken VDD line, 5V mode	≤2	kΩ
Broken VDD line, 3.3V mode	≤2	kΩ

Table 31. Diagnostic Levels with Pull-Down Resistors

Diagnostic level	<4% VDD	Unit
Error indication during normal operation	≤9.1	kΩ
Broken VDD line	Not critical, see the uncritical error cases.	kΩ
Broken GND line, 5V mode	≤2	kΩ
Broken GND line, 3.3V mode	≤2	kΩ

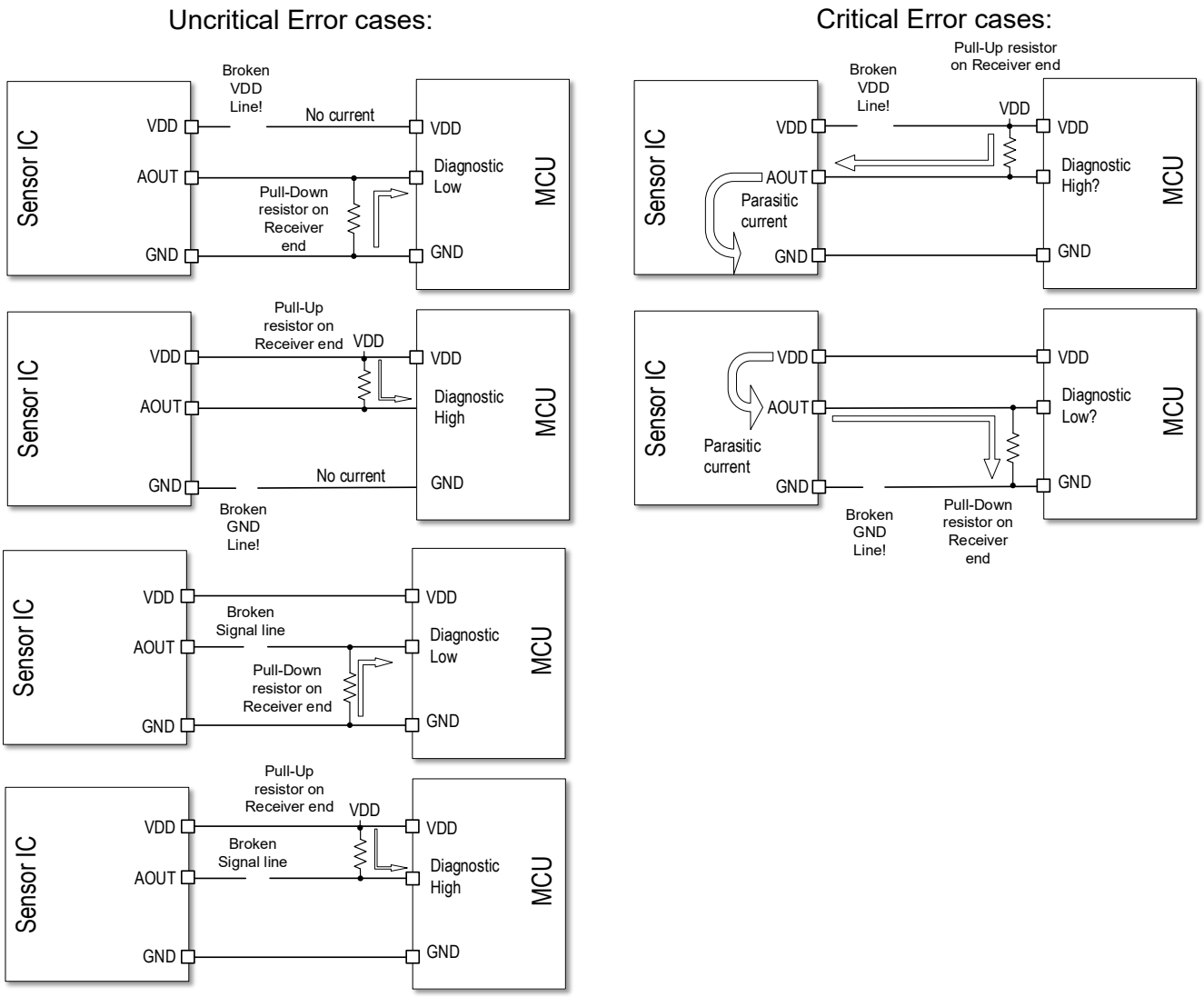


Figure 35. Parasitic Currents on Analog Outputs with Broken VDD or Broken GND Lines

8. User Programming Options

Table 32 shows an extract of the main configuration options. A detailed description is provided in the RAA2P4500 programming manual, available on request from Renesas.

Table 32. Global Programming Options

Programming Option	Number of options	Description
Power supply mode	2	3.3V ±10% or 5.0V ±10%
Interface options	4	Analog, PWM, PWM differential, SENT, I2C
Initial receiver gain coil	28	Initial receiver gain
Automatic gain control AGC	2	Enabled/disabled
Hysteresis	8	0 to 112 LSBs
Number of linearization points	16 points	2/4/6/8/16 linearization points, programmable in x and y
Linearization points resolution	12-bit	Up to 16 linearization points are freely programmable in X (position) and Y (value) with 12-bit resolution
Magnitude alarm reference limits	2 x 14-bit	Upper and Lower limits programmability
Zero (discontinuity) point	12-bit	0° to <360° in 12-bit steps, position output switches from maximum to minimum value (with increasing position movement) or from minimum to maximum value (with decreasing position movement) at this position
Sine and cosine signal offset correction	2 x 8-bit	±127 LSBs for sine and cosine
Sine and cosine amplitude mismatch correction	2 x 15-bit	0% to 199% adjustment range per channel
Digital low pass filter	8	Depth of digital low pass filter for position output
Turns counter option	2	Behavior of 12bit turns counter when overflowing: stop at max/min, wrap around
Customer ID	48-bit	Scratchpad register for customer specific data

9. Related Documents

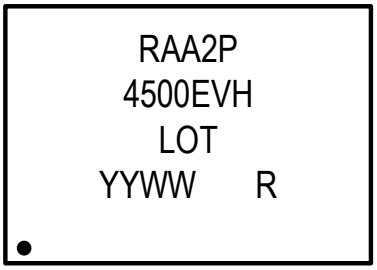
- RAA2P4500 Programming Manual
- RAA2P4500 Functional Safety Manual

10. 16-TSSOP Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

16-TSSOP Package Outline Drawing 4.4mm Body, 0.65mm Pitch PGG16T1

11. Marking Diagram



Line 1: First characters of part code RAA2P

Line 2: Next five characters of the part code:

4500E: Single Coil Low Speed

followed by:

V = Operation temperature range, Extended Automotive

H = Automotive Qualified

Line 3: “LOT” = Lot number

Line 4: “YYWW” = Manufacturing date:

YY = last two digits of manufacturing year

WW = manufacturing week

R = RoHS compliant statement

12. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
RAA2P4500EVHSP#HA0	16-TSSOP, 4.4 ×5.0 mm	1	13” Reel, 4000 parts / reel	-40° to +160°C
For communication and programming, Renesas offers a RAA2P4500 Application Modules with a RAA2P-COMBOARD.A development programmer is available separately.				

13. Glossary

Term	Description
AC	Alternating Current
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
APB	Advanced Peripheral Bus
ASIL	Automotive Safety Integrity Level
CDM	Charged-Device Model
CORDIC	Coordinate Rotation Digital Computer
CRC	Cyclic Redundancy Check
DC	Direct Current
DP	Discontinuity Point
ECU	Electronic Control Unit
EMC	Electromagnetic compatibility
ESD	Electrostatic Discharge
FDM	Failure Detection Mechanisms
FSM	Finite-State Machine
FUSA	Functional Safety
GND	Ground
FSM	Finite State Machine
HK	House Keeping
I/O	Input / Output
I2C	Inter-Integrated Circuit Interface
IC	Integrated Circuit
ID	Identification
LC	Resonant Inductor-Capacitor Circuit

Term	Description
LF	Low Frequency
LPF	Low Pass Filter
LSB	Least Significant Bit
MCU	Micro Controller Unit
MSB	Most Significant Bit
MUX	Multiplexer
NVM	Non Volatile Memory
OD	Open Drain
PCB	Printed Circuit Board
PP	Push-Pull
RF	Radio Frequency
RX	Receiver
SCL	I2C Clock
SDA	I2C Data
TSSP	Thin Shrink Small Outline Package
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

14. Revision History

Revision	Date	Description
1.1	Dec 8, 2025	Reworked Table 11,Table 7
1.0	Aug 7, 2025	Initial release