RAA2P4520

Dual-Angle Inductive Position Sensor with SENT and UART Interfaces

The RAA2P4520 is a magnet-free, inductive position sensor IC that can be used for absolute rotary, linear, or arc position sensing in automotive applications.

It operates on the principle of eddy currents to detect the position of a simple metallic target that is moving above the sensing coil sets.

The device features two sets of receiver coils, providing means for measuring two independent positions or in a high-resolution configuration.

The RAA2P4520 is equipped with:

- High-speed UART interface
- SENT interface
- Additional analog voltage input

The RAA2P4520 was developed according to ISO26262 for implementation in safety-relevant systems up to ASIL C. It can also be used in ASIL D system-level requirements according to ASIL Decomposition rules (ISO 26262:2018, Part 9, Clause 5”) or proper risk analysis by the system integrator. It is available in a 16-pin TSSOP package and qualified for automotive use from −40 °C to +160 °C ambient temperature.

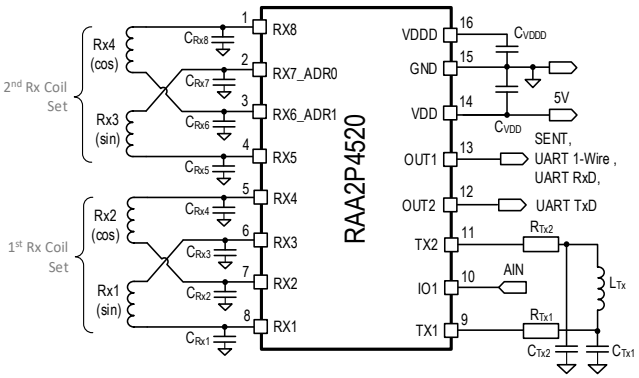

Figure 1. Application circuit example

Features

- Cost-effective; no magnet required
- Immune to magnetic stray fields; no shielding required
- Suitable for harsh environments and extreme temperatures
- Adaptable to any full-scale angle range through Renesas coil design tools
- Dual-coil inputs enabling measurement of:
  - High resolution position up to 19-bit
  - Two independent angles up to 14-bit
  - Angle difference up to 14-bit
- 14-bit SENT SAE J2716/2016-compatible with programmable fast-channel modes and extended serial messages supporting 0.02 µs to 6 µs tick time
- 5.0 V or 3.3 V supply
- High accuracy: ≤ 0.1% full scale (with ideal coils)
- Overvoltage and reverse polarity protection: ±18 V on supply and output pins
- Analog voltage input from external sensors
- Supports low-speed as well as high-speed applications up to 600000 rpm (electrical).
- 48 bits nonvolatile user ID memory space
- Reprogrammable through output pin using 1-wire UART
- Small 16-pin TSSOP package (4.4 mm x 5.0 mm)

Applications

The RAA2P4520 addresses safety relevant automotive sensor applications such as:

- Steering angle
- Pedal position
- Chassis
- Rotor position sensors

Available Support

Renesas provides starter kits that demonstrate RAA2P4520 position sensing applications. A coil design tool is available to generate the sensing coils.

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Terms and Definitions

AC	Alternating Current
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APB	Advanced Peripheral Bus
ASIL	Automotive Safety Integrity Level
CDM	Charged-Device Model
CORDIC	Coordinate Rotation Digital Computer
CRC	Cyclic Redundancy Check
DC	Direct Current
DP	Discontinuity Point
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FDM	Failure Detection Mechanisms
FSM	Finite-State Machine
FUSA	Functional Safety
GND	Ground
HK	Housekeeping
I/O	Input/Output
I2C	Inter-Integrated Circuit Interface
IC	Integrated Circuit
ID	Identification
LC	Resonant Inductor-Capacitor Circuit
LF	Low Frequency
LPF	Low-Pass Filter
LSB	Least Significant Bit
MCU	Microcontroller Unit
MSB	Most Significant Bit
MUX	Multiplexer
NVM	Nonvolatile Memory
OD	Open Drain
PCB	Printed Circuit Board
PP	Push-Pull
RF	Radio Frequency
RX	Receiver
SENT	Single Edge Nibble Transmission
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter

1. Pin Information

1.1 Pin Assignments

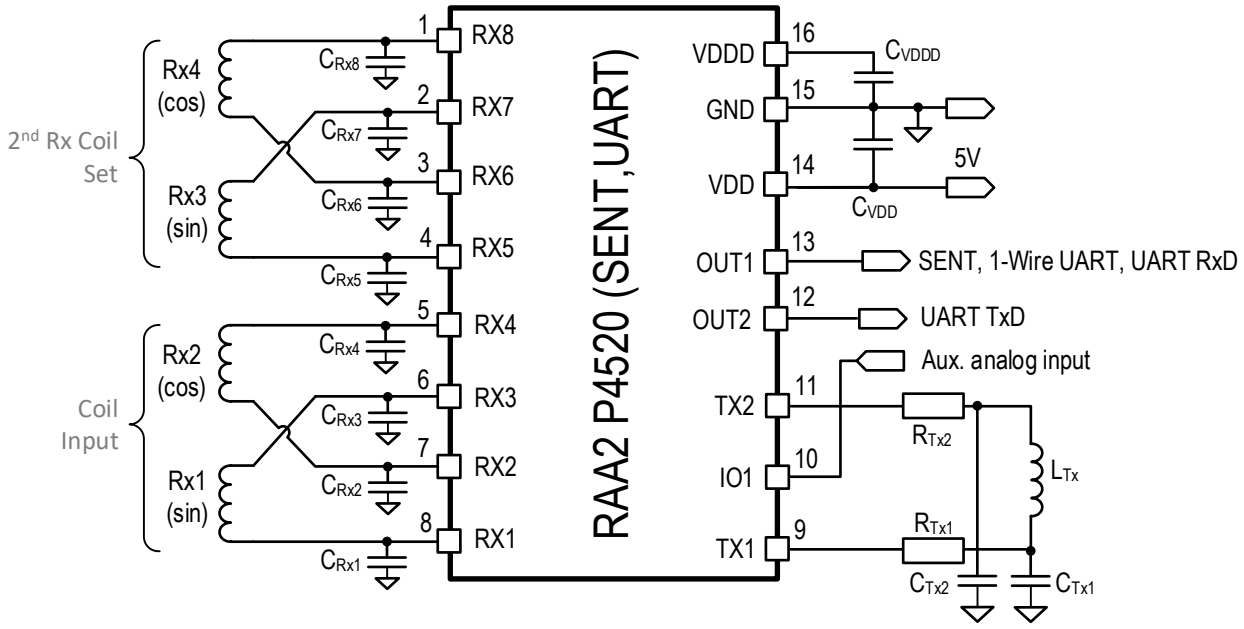


Figure 2. Pin assignments – top view

1.2 Pin Descriptions

Table 1. Pin descriptions

Pin #	Type	RAA2P4520: Dual Coil	
		SENT	UART
1	Analog Inputs	Rx8: COS_P; secondary receiver coil (coil_cfg = DUAL_COIL)	
2		Rx7: SIN_P; secondary receiver coil (coil_cfg = DUAL_COIL)	
3		Rx6: COS_N; secondary receiver coil (coil_cfg = DUAL_COIL)	
4		Rx5: SIN_N; secondary receiver coil (coil_cfg = DUAL_COIL)	
5		Rx4: COS_P; primary receiver coil (coil_cfg = DUAL_COIL)	
6		Rx3: SIN_P; primary receiver coil (coil_cfg = DUAL_COIL)	
7		Rx2: COS_N; primary receiver coil (coil_cfg = DUAL_COIL)	
8		Rx1: SIN_N; primary receiver coil (coil_cfg = DUAL_COIL)	
9	Analog I/O	TX1: Connect the transmitter coil between the TX1 and TX2 pins, using series resistors R_{Tx1} and R_{Tx2}. The resonant frequency is adjusted with capacitors C_{Tx1} and C_{Tx2} from each coil terminal to GND as described in “Specifications”.	
10	Analog Input	IO1: Analog voltage input (AIN)	
11	Analog I/O	TX2: See description of pin 9 (TX1)	
12	Digital Output, Push-Pull (PP) or Open Drain (OD)		OUT2: TxD (2-wire UART)
13	Digital Input/Digital Output, Push-	OUT1: SENT(PP) This pin is used for single wire programming.	OUT1: TxD/RxD (1-wire); RxD input (2-wire). This pin is used for single wire programming.

Pin #	Type	RAA2P4520: Dual Coil	
		SENT	UART
	Pull (PP) or Open Drain (OD)		
14	Supply	VDD: External supply voltage. Connect a capacitor C_{VDD} between VDD and GND.	
15	Supply	GND: Common ground connection.	
16	Supply	VDDD: Internally regulated digital supply voltage. Connect a capacitor C_{VDDD} between VDDD and GND.	
NVM programming and configuration		1-wire UART	1-wire UART

2. Specifications

2.1 Absolute Maximum Ratings

The absolute maximum ratings listed in the following table are stress ratings only. Exceeding these limits can cause permanent damage to the device. The functional operation of the device at these maximum ratings is not guaranteed. Exposure to the absolute maximum rating conditions could impact device's reliability. All voltage levels are referenced to GND.

Table 2. Absolute maximum ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{VDDmax}	External supply voltage: VDD	Continuous	-18	18	V
$V_{OUT1max}$	Digital Output Pin: OUT1				
$V_{OUT2max}$	Digital Output Pin: OUT2				
V_{IN1max}	Analog Input Pin: AIN				
V_{RX1max}	Receiver coil input pin: RX1	Continuous	-12	12	V
V_{RX2max}	Receiver coil input pin: RX2				
V_{RX3max}	Receiver coil input pin: RX3				
V_{RX4max}	Receiver coil input pin: RX4				
V_{RX5max}	Receiver coil input pin: RX5				
V_{RX6max}	Receiver coil input pin: RX6				
V_{RX7max}	Receiver coil input pin: RX7				
V_{RX8max}	Receiver coil input pin: RX8				
V_{Tx1max}	Transmitter pin, TX1	Continuous	-0.3	5.5	V
V_{Tx2max}	Transmitter pin, TX2				
$V_{VDDDmax}$	Internal digital supply voltage, VDDD	VDDD is internally regulated with external capacitor to GND	-0.3	2.0	V

Table 3. Electrostatic discharge

Symbol	Parameter	Condition	Maximum	Unit
V_{ESD_OUT}	ESD tolerance for single wire output pins with potential external cable connection: OUT1 VDD, VSS Human Body Model: 100 pF / 1.5 kΩ	According to AEC-Q100-002 classification 3 A	±4	kV
V_{ESD}	ESD tolerance for all other pins not listed under V_{ESD_OUT} Human Body Model: 100 pF / 1.5 kΩ	According to AEC-Q100-002 classification 2	±2	kV
V_{CDM}	ESD tolerance for all pins: Charged-Device Model (CDM)	According to AEC-Q100-011 classification C2b	±750	V

2.2 Operating Conditions

All minimum/maximum specification limits are guaranteed by design, production testing, and/or statistical characterization. Conditions: T_J = −40 °C to 170 °C unless otherwise specified. C_{VDD} = 470 nF, C_{VDDD} = 100 nF.

Typical values are based on characterization results at default measurement conditions and are informative only.

Table 4. Temperature range

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{AMB}	Ambient temperature (Note 1)		-40	-	160	ºC
T_J	Junction temperature (Note 2)		-40	-	170	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125 °C to prevent pre-aging	-55	-	160	ºC
R_{THJA}	Thermal resistance junction to ambient: 16-TSSOP package	Velocity = 0 m/s with 2s2p PCB test board (JEDEC 51-2, JEDEC 51-7)	-	-	89.5	K/W
R_{THJC}	Thermal resistance junction to case: 16-TSSOP package	Junction to top of package	-	-	38.38	K/W
		Junction to bottom of package	-	-	70.58	

Note 1 The junction temperature must not exceed the specified limits. Maximum ambient temperature depends on the junction temperature, total supply, and thermal resistance.

Note 2 When the maximum junction temperature (T_J) is exceeded, the device enters an overtemperature shutdown state.

2.3 Electrical Characteristics

The following electrical specifications are valid for the operating conditions as specified in Section 2.2. (T_J is −40 °C to 170 °C, Supply voltage V_{VDD} = 3.0 to 5.5 V unless otherwise specified). C_{VDD} = 470 nF, C_{VDDD} = 100 nF.

Table 5. Operating conditions

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{VDD5}	Supply voltage, 5 V mode		4.5	5.0	5.5	V
V_{5UV}	Under-voltage detection level	An under-voltage alarm is created if VDD falls below this limit	3.95	4.1	4.45	V
V_{5OV}	Overvoltage detection level	An overvoltage alarm is created if VDD rises above this limit	5.55	6.15	6.5	V
V_{VDD3}	Supply voltage, 3.3 V mode		3.0	3.3	3.6	V
V_{3UV}	Under-voltage detection level	An under-voltage alarm is created if VDD falls below this limit	2.7	2.8	2.98	V
V_{3OV}	Overvoltage detection level	An overvoltage alarm is created if VDD rises above this limit	3.65	3.85	4.04	V
$V_{VDD_TH_H}$	Power-on reset (POR), high threshold	Power-on reset (POR): the device is activated when VDD increases above this threshold	-	2.61	2.7	V
$V_{VDD_TH_L:}$	Power-on reset, low threshold	The device is deactivated when VDD decreases below this threshold	2.3	2.38	-	V

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DDPOR_HYST}	Power-on reset hysteresis		200	250	300	mV
t_{pup}	Start-up time	Power-on reset (POR) to valid output signal, programming enabled	-	-	5	ms
t_{pupL}		Power-on reset (POR) to valid output signal, programming locked	-	-	3	
t_{ProgEn}	Programming window: enable	Time window after POR, in which a first programming enable command must be sent	1.5	-	5	ms
t_{ProgUL}	Programming window: unlock	Time window after programming enable in which a second unlock command must be sent	-	-	75	ms
V_{VDDD}	Digital supply voltage	Internally regulated. Connect capacitor C_{VDDD} = 100 nF from V_{VDDD} to GND	1.75	1.8	1.85	V
I_{VDDD}	V_{VDDD} external load current	V_{VDDD} must be connected to a capacitor C_{VDDD}.	0	-	1	mA
$I_{VDDDSHORT}$	V_{VDDD} short circuit current limitation		17	-	40	mA
I_{CC}	Current consumption	Without coils, no load	10	15	20	mA
	Programmable transmitter coil drive current (depending on inductance of the transmitter coil)		For values, see Table 7			
C_{VDDD}	Capacitor from V_{VDDD} pin to GND		100	-	-	nF
C_{VDD}	Capacitor from VDD pin to GND	Nominal value	100	470	-	nF

Table 6. Accuracy and resolution

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Res_{SENT}	Resolution of calculated position over SENT interface	Over 1 coil period (360°el.), resolution depending on SENT fast channel mode	12		14	bits
Res_{UART}	Resolution of calculated position over UART interface	Over 1 coil period (360°el.), all modes	-	14	-	bits
ACC_{nom}	Accuracy of the internally calculated position with ideal sinusoidal input signals	At room temperature, 5 V supply mode	-0.1	-	+0.1	% FS (Note 4)
ACC_{temp}		Over temperature and supply voltage range until overvoltage and undervoltage detection.	-0.2	-	+0.2	% FS (Note 4)
t_{POS}	Update rate of internally calculated position	Refresh rate: single coil	2	-	3	µs
		Sampling rate: dual coil	4	-	6	

Note 1 Values are valid for primary channel (angle1) and secondary channel (angle2). Device configuration according to programming manual.

Note 2 For coil difference reading (see Table 20 > options 4) accuracy values are to be multiplied by 2.

Note 3 Accuracy specifications can be further improved with linearization, see Section 3.3.3.

Note 4 "% FS" = percent of full scale = accuracy in % per period, where 100% is the angle range of one electrical period. For rotary multi-period designs, one electrical period = 360° (one full turn) divided by the number of periods per turn.
Examples:
A 4-periodic coil design (4 × 90°) has a typical mechanical accuracy of ±0.1% per 90° = ±0.09°
A 8-periodic coil design (8 × 45°) has a typical mechanical accuracy of ±0.1% per 45° = ±0.045°

Table 7. LC oscillator specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{LC}	Excitation frequency	LC oscillator frequency is determined by external components L and C, see Section 3.2.1	2	-	5.5	MHz
R_{Peq}	Equivalent parallel resistance of the LC resonant circuit		250	-	-	Ω
V_{TX_PP}	LC oscillator amplitude at VDD = 5.0 V ±10%	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. Adjustable by coil current	-	-	8.8	Vpp
	LC oscillator amplitude at VDD = 3.3 V ±10%		-	-	$2*V_{VDD3}$	
I_{LC}	Programmable transmitter coil drive current	Tambient = −40 to +160 °C	0	Note 1	16	mA
R_{Tx1}, R_{Tx2}	LC oscillator series resistors	Depending on coil design and excitation frequency (f_{LC})	-	10	-	Ω

Note 1 The required transmitter coil current is determined by the equivalent parallel resistance of the LC circuit, depending on coil design, see Figure 6.

Table 8. Coil receiver front-end specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{RX}	Receiver coil amplitude	Differential coil input	5	-	200	mVpp
A_{IN_mm}	Maximum amplitude mismatch correction	Programmable gain mismatch correction of Receiver coil signals (SIN and COS)	-	-	15	%
$A_{IN_OFFSET_RANGE\%}$	Input offset correction	Differential input offsets of sine or cosine signal, percentage of transmitter coil amplitude.	-0.2	-	0.2	%
D_{OFFSET}	Coil input offset temperature drift	Over temperature range T_{AMB}	-2.5	-	2.5	%
C_{RX1} to C_{RX8}	Receiver input filter capacitors	For improved EMC immunity	-	220	-	pF
Noise	Signal path noise level	V_{RX}= 50 mV	-	-	0.1	°el., rms
		V_{RX} = 5 mV ; Device configuration according to programming manual.	-	-	0.5	°el., rms

Table 9. UART interface

Symbol	Parameter	Description	Minimum	Typical	Maximum	Unit
V_{OL_UART}	Output low voltage	3mA sink current, VDD = 3.0 to 5.5 V OUT1 pin 13 OUT2 pin 12	0	-	0.4	V
V_{OH_UART}	Output high voltage	3mA source current, VDD = 3.0 to 5.5 V OUT1 pin 13 OUT2 pin 12 (Push-Pull condition)	0.8 × VDD	-	VDD	V
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold	OUT2 pin 12	8	-	-	mA
$I_{OUT2\ sc\ lim}$	OUT2 output short current limitation (Note 1)	OUT2 pin 12 Short to VDD, GND VDD = 3.0 to 5.5 V Open Drain mode	14	-	26	mA
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold	OUT1 pin 13	35	-	-	mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation (Note 2)	OUT1 pin 13 Short to VDD, GND VDD = 3.0 to 5.5 V Push-pull mode	28	-	-	mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation (Note 2)	OUT1 pin 13 Short to VDD, GND VDD = 3.0 to 5.5 V Open Drain mode	28	-	56	mA
V_{IL_UART}	OUT1 low level input voltage	VDD = 5 V	-0.3	-	0.2 × VDD	V
		VDD = 3.3 V	-0.3	-	0.3 × VDD	V
V_{IH_UART}	OUT1 high level input voltage	VDD = 5 V	0.7 × VDD	-	VDD + 0.3	V
		VDD = 3.3 V	0.7 × VDD	-	VDD + 0.3	V

Note 1 With OUT2 drive strength set to "00" and OUT2 drive strength for open drain disabled (out2_io1_drv = "00").

Note 2 With digital mode configuration (out1_drv = "10").

Table 10. SENT interface

Symbol	Parameter	Description	Minimum	Typical	Maximum	Unit
V_{OL_SENT} (Note 2)	Output low voltage	3 mA sink current, VDD = 4.5 to 5.5 V OUT1 pin 13	0	-	0.5	V
V_{OH_SENT} (Note 2)	Output high voltage	3 mA source current, VDD = 4.5 to 5.5 V OUT1 pin 13	4.1	-	5.5	V
$I_{OUT1\ lim\ thr}$	OUT1 current limitation threshold[Note 1]	OUT1 pin 13 in overload condition	55	-		mA
$I_{OUT1\ sc\ lim}$	OUT1 output short current limitation[Note 1]	OUT1 pin 13 Short to VDD, GND VDD = 4.5 to 5.5 V Push-pull mode	40	-	91	mA

Symbol	Parameter	Description	Minimum	Typical	Maximum	Unit
t_{OVL}	Overload shutdown debounce time	Duration of overload condition, before output is shut off	-	2	-	ms
$I_{OUT2\ lim\ thr}$	OUT2 current limitation threshold (Note 1)	OUT2 pin 12 in overload condition	8	-	-	mA
$I_{OUT2\ lim\ thr}$	OUT2 output short current limitation (Note 1)	OUT2 pin 12	33	-	70	mA
C_{input}	Parasitic input capacitance from ESD protection		-	-	0.1	nF
I_{SUP} (Note 2)	Average current consumption from Receiver 5 V supply over one message		-	-	50	mA
I_{GND} (Note 2)	Average current through Ground line over one message		-	-	50	mA
$I_{SUP\ RIPPLE}$ (Note 2)	Peak-to-peak variation in supply current consumption over one message at frequencies up 30 kHz		-	-	9	mA
T_{Fall} (Note 2)	Falling time, tick time = 3 µs From V_{TH} = 3.8 V to V_{TL} = 1.1 V	$I_{SUP} \le 20$ mA	-	-	6.5	µs
		20 mA ≤ I_{SUP} < 50 mA	-	-	5	µs
T_{Rise} (Note 2)	Rising time, tick time = 3 µs From V_{TL} = 1.1 V to V_{TH} = 3.8 V		-	-	18	µs
ΔT_{Fall} (Note 2)	Edge to Edge Jitter with static environment for any pulse period tick time = 3 µs		-	-	0.1	µs
R_{Tau1}	Input filter resistor (first stage)		448	560	672	Ω
C_{Tau1}	Input filter capacitor (first stage)		1.54	2.2	2.86	nF
Tau_1	Input filter time 1st stage time constant defined by RTau1 and CTau1		0.74	-	1.73	µs
$R_{PULL-UP}$	Input Pull-up resistor		10	-	55	kΩ
R_F	Input filter resistor (second stage)		4	-	-	kΩ
C_F	Input filter capacitor (second stage)	Determined by TAU2 requirement	-	-	-	nF
R_V	Voltage divider, adjusting SENT output level to MCU input level	Optional, depends on MCU input level	-	-	-	kΩ
Tau (Note 2)	Input filter time second stage time constant defined by RV, RF, and CF		0.6	-	1.4	µs

Note 1 With SENT mode configuration (out1_drv = 11).

Note 2 With out2_io1_drv = 11.

Note 3 Refer to SENT Standard SAE J2716 Standard (Rev. April 2016).

Table 11. Nonvolatile memory

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Data retention	Qualified according to JEDEC 22-A117	15 at T_J = 100 °C	-	-	Years
	Over product lifetime	-	>100 at T_J = 25 °C	-	
Write temperature	Allowed ambient temperature range for read and write access	-40	-	135	°C
Read temperature		-40	-	160	°C
Endurance (Note 1)	Over product lifetime	-	-	1000	NVM Write Cycles
Read Cycles		5x 10^{11}	1x 10^{12}	-	NVM Read events

Note 1 Verified number of program/erase cycles. Qualified with 2000 cycles.

Note 2 Guaranteed by memory supplier.

3. Functional Description

3.1 Overview

The RAA2P4520 is designed to drive a transmitter coil and receive signals from two pairs of receiver coils, typically created as traces on a printed circuit board. The receiver coils consist of two wire loops connected in anti-serial fashion, with the “sine” and “cosine” coils shifted by 90 electrical degrees. A metal target is placed above this coil arrangement.

The RAA2P4520 supports two sets of independent receiver coils enabling output of one high resolution position, two independent angles, and an angle difference over a single output pin.

When the device drives an AC current into the transmitter coil, it generates an alternating magnetic field. This magnetic field induces secondary voltages in the receiver coils. Without a target, the induced voltages in the loops of the receiver coils cancel each other out, resulting in a net receiver voltage of zero.

When a metal target is placed above the coils, the magnetic field generates eddy currents on its surface. These eddy currents create a counter magnetic field, reducing the total flux density underneath. This leads to a reduction in the voltage induced in the receiver coil areas underneath the target, creating an imbalance in the anti-serial coil segment voltages.

The RAA2P4520 demodulates, offsets, and corrects the amplitude of the signals from the two receiver coils with a 90° electrical phase shift design, which generates sine and cosine shaped voltages as the target is moving.

The RAA2P4520 amplifies, rectifies, and filters the receiver voltages, converting them into digital representation with an ADC. The digital sine and cosine signals are converted into a 0° to 360° absolute position. The signal accuracy can be further enhanced through a 2-dimentional,16-point linearization process.

The absolute position can be read in digital format by UART or SENT interfaces.

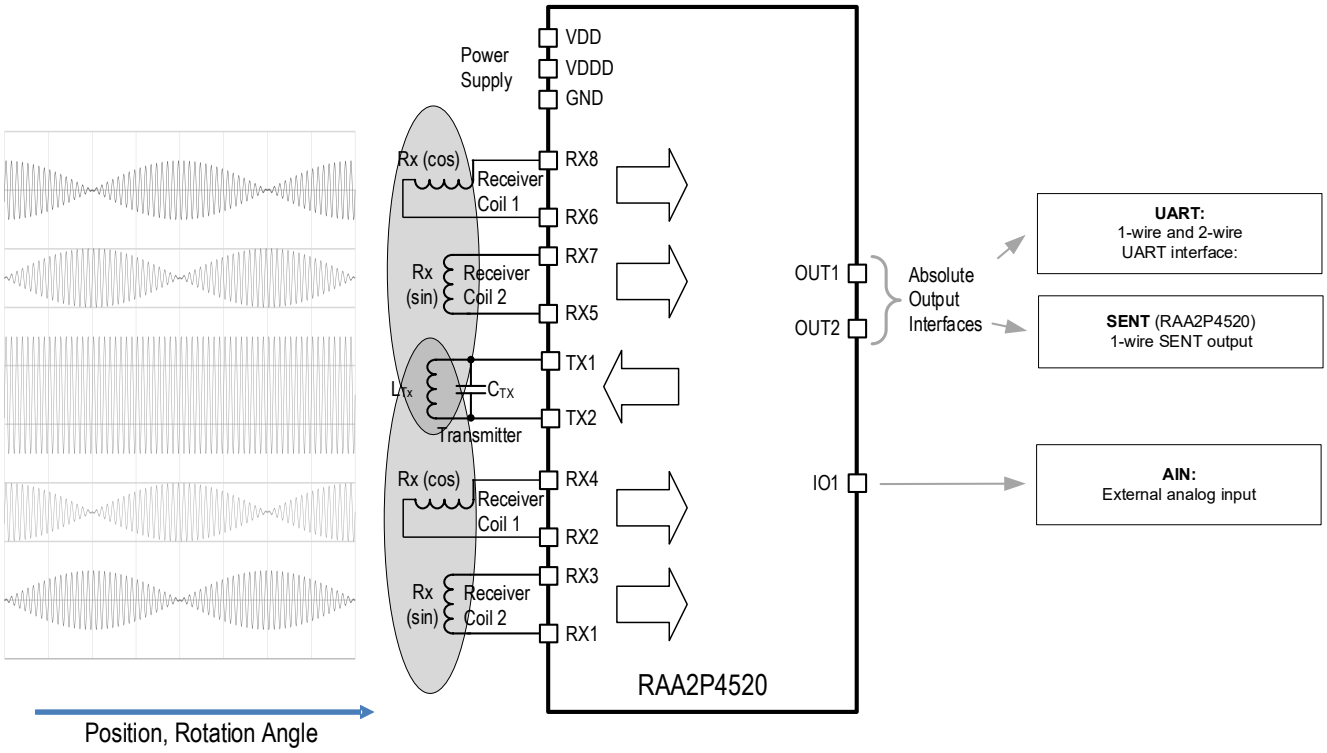


Figure 3. Input and output signals of RAA2P4520

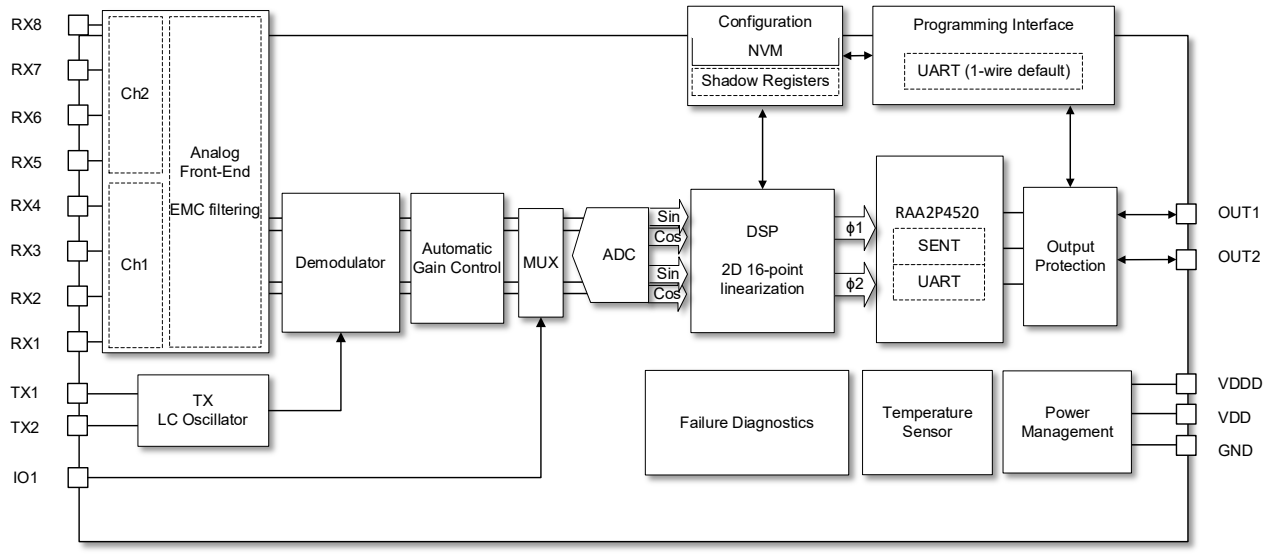


Figure 4. Block diagram

The main building blocks include:

- Analog front-end – Input filter, offset, and gain control for the receiver signals.
- Demodulator: Converts RF modulated position signal to LF demodulated raw sine and cosine signals.
- Automatic Gain Control – Automatically adjusts raw sine and cosine signal levels.
- MUX – Multiplexer for ADC input.
- ADC – Converts raw signals into digital format for further processing in high speed.
- DSP (digital signal processing) – Converts digital sine and cosine raw signals into synchronized absolute position information.
- 2D 16-point linearization – Supports up to 16 two-dimensional linearization points with freely programmable X- and Y- coordinates for each point (X= Position input, Y= Position output).
- UART, SENT: Carries out post processing, Delay correction, speed calculation, clamping, signal integrity checks. Decoding of Channel 1 and Channel 2 information and other diagnostics info into the selected output format.
- TX LC Oscillator – Generates the transmitter coil signal.
- Temperature sensor – Internal temperature sensor used for chip diagnostics.
- Output Protection – All outputs are fully protected against overvoltage, reverse polarity and short circuit, enabling direct cable connection to these outputs and eliminating the need for additional line driver ICs.
- Power Management – Operates with supply voltages ranging from 3.0V to 5.5V. External capacitors are required for the supply voltage VDD, and for the digital power supply, VDDD.
- Programming interface – Accessible via single-wire interface, based on a half-duplex UART protocol.
- Configuration, NVM – Stores non-volatile storage for factory and user-programmable settings. User configuration parameters can be programmed multiple times.
- Failure diagnostics – Performs on-chip, internal diagnosis of critical blocks.
- IO1 – Analog input for external analog signals connected to the multiplexer.

3.2 LC Oscillator

The transmitter circuit of the RAA2P4520 generates the required RF magnetic field for operating the sensor as determined by an external parallel LC circuit, see Figure 2. To ensure low emission of harmonics, the capacitive part of the LC circuit is split into two equal-value capacitors C_{Tx1} and C_{Tx2}. Additionally, two series resistors R_{Tx1} and R_{Tx2} are added as shown in Figure 5.

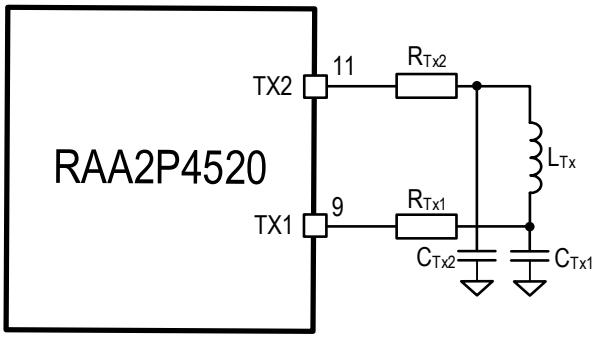


Figure 5. LC oscillator connection with split TX capacitors

3.2.1 Parallel LC Resonator Calculations

A resonator, comprising an inductor (L) and a capacitor (C) in parallel, is essential for generating specific frequencies in RF applications. Accurate calculations of the equivalent parallel resistance (R-Peq) ensure proper resonator function. In the RAA2P4520 transmitter circuit, this resonator minimizes harmonic emissions.

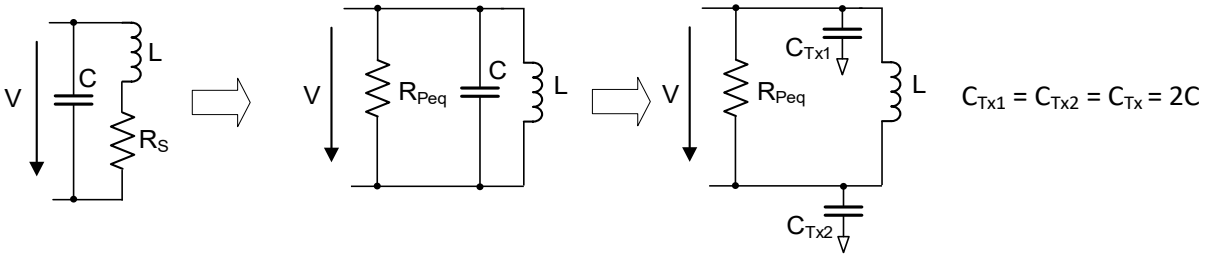


Figure 6. Parallel resonator circuit

Equivalent parallel resistance from Coil series resistance:

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C}$$ Equation 1

For $C_{Tx1} = C_{Tx2} = C_{Tx} = 2C$:

$$R_{Peq} = \frac{1}{R_S} \times \frac{2 \times L}{C_{Tx}}$$ Equation 2

Equivalent parallel resistance from Quality factor Q:

$$R_{Peq} = Q \times \sqrt{\frac{L}{C}} = Q \times \sqrt{\frac{2L}{C_{Tx}}}$$ Equation 3

Ideal LC Oscillator frequency with split Tx capacitors CTx

$$f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{Tx}}{2}}}$$ Equation 4

Oscillator frequency with split T_x capacitor C_{Tx} and coil series resistor R_s

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{R_S}{L}\right)^2}$$ Equation 5

Oscillator frequency with split Tx capacitor C_{Tx} and equivalent parallel resistor R_{Peq}

$$f_{TX} = \frac{1}{2\pi}\sqrt{\frac{2}{LC_{Tx}} - \left(\frac{2}{R_{Peq}C_{Tx}}\right)^2}$$ Equation 6

$$Q = R_{Peq}\sqrt{\frac{C}{L}} = \frac{1}{R_S}\sqrt{\frac{L}{C}}$$ Equation 7

Coil quality factor

$$Q = \omega\frac{L}{R_S} = 2\pi f_{TX}\frac{L}{R_S}$$ Equation 8

Where:

- R_{Peq} Equivalent parallel resistance of the LC circuit at the transmitter frequency in Ohms
- R_S Serial resistance of the transmitter coil at the transmitter frequency in Ohms
- f_{Tx} Resonant circuit frequency in Hertz, 1/s
- L Resonant circuit coil impedance in Henry
- C Resonant circuit capacitance in Farad
- C_{Tx1}, C_{Tx2} Capacitance of the split capacitors in Farad
- Q Resonant circuit quality factor (unitless)
- ω Angular frequency 2*π*f_{Tx} in Hertz, 1/s

3.3 Coil Design

Figure 7 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$$V_{Cos\ Loop1} = -V_{Cos\ Loop2}$$ Equation 9

In the absence of a target, the secondary voltages balance out as follows:

$$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} = 0V$$ Equation 10

With a target placed above the coils, the secondary voltage induced in the covered area decreases compared to the secondary voltage when no target is present above it.

$$V_{Cos\ Loop1} \neq -V_{Cos\ Loop2}$$ Equation 11

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage ≠ 0V is generated, depending on the location of the target

$$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} \neq 0V$$ Equation 12

Figure 7 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

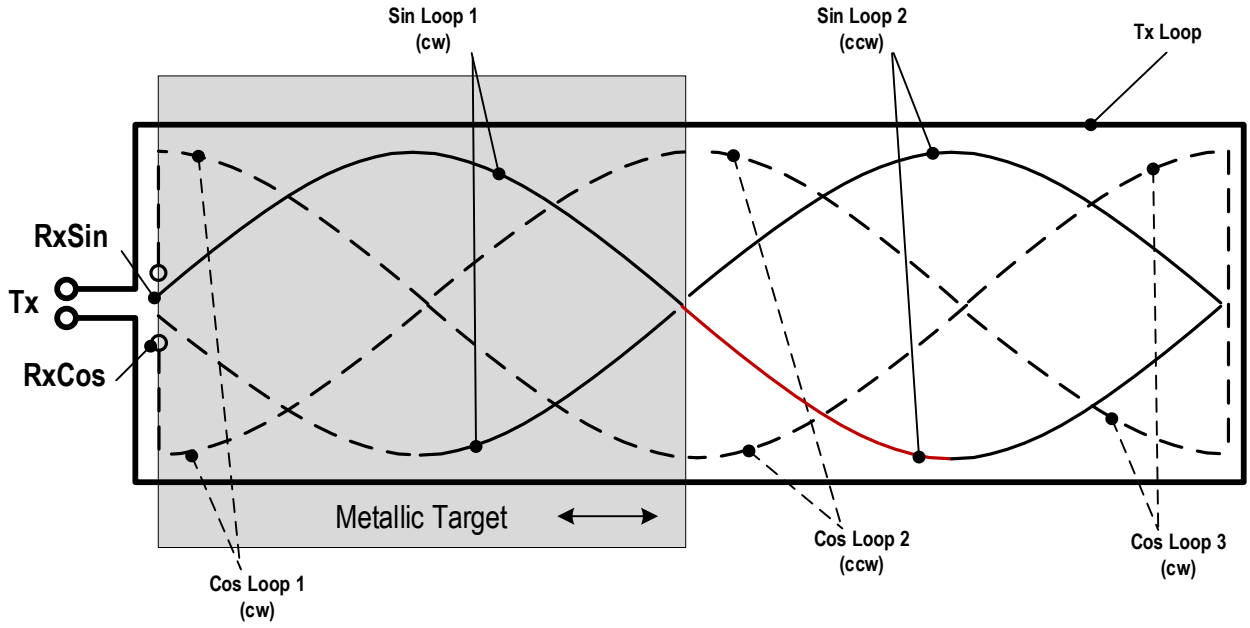


Figure 7. Coil design for a linear motion sensor

The same principles shown for the linear motion sensor in Figure 7 can be applied to a rotary sensor as shown in Figure 8.

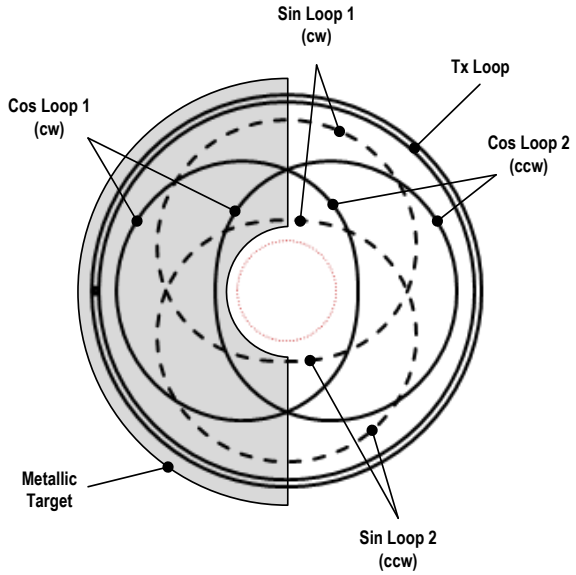


Figure 8. Coil design for a 360° rotary sensor

3.3.1 Multi-Periodic Coil Design Application Examples

Applying the same fundamental design principles, coils with multiple periods per turn can be designed. Multi-periodic designs improve mechanical accuracy compared to single-periodic coil designs. For example, a 4-periodic coil design (4 × 90°) improves mechanical accuracy by a factor of 4. Consequently, for angular designs, requiring < 360° movement range, coil designs with multiple periods are recommended.

3.3.2 Electrical vs. Mechanical Degrees

The RAA2P4520 converts the movement of the target across a single period of the receiver coil into a precise electrical signal. This conversion spans the full angular range from 0° to 360°. As shown in Figure 9, the single-periodic coil design establishes a direct 1:1 relationship between electrical and mechanical domains as the following:

- Coil Period – 360° electrical

- Mechanical Range – 360° mechanical
- Conversion Factor – 1:1 (1°el. = 1° mechanical)

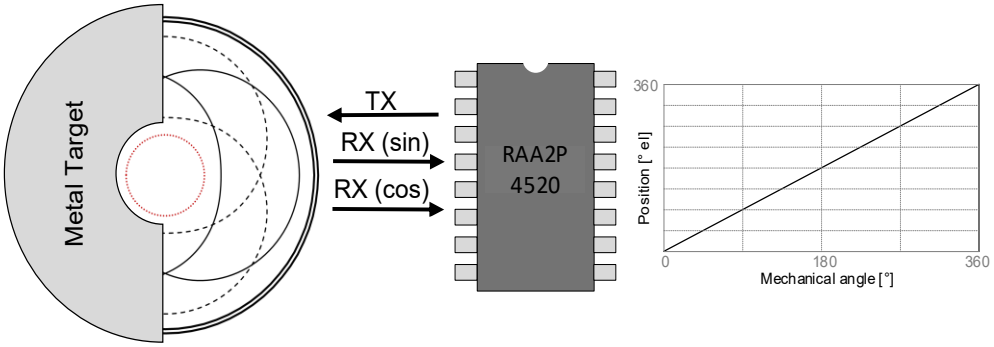


Figure 9. Coil design using single-periodic coil

As displayed in Figure 10, a coil design with four receiver coil periods within a single full mechanical turn, results in four electrical rotations for every complete mechanical turn and provides the following advantages in accuracy and resolution.

Higher resolution: Position output resolution increases proportionally with period count by

$$\text{Mechanical Resolution} = \text{Sensors_Periods} \times \text{Electrical Resolution}$$

In this configuration one electrical degree (°el) equals 0.25 mechanical degrees(°). This provided output resolution is four times higher compared to the single-periodic design.

Improved accuracy: Mechanical error is reduced by the period factor

$$Mechanical\ Error = \frac{Electrical\ Error}{Sensor\ Periods}$$

This configuration is particularly well-suited for:

- Multi-pole motors requiring precise commutation
- Limited-range applications (<180° mechanical travel)
- Systems demanding high-resolution incremental feedback
  Select the number of periods based on application requirements to optimize measurement performance. Proper period selection is critical for achieving maximum system accuracy.

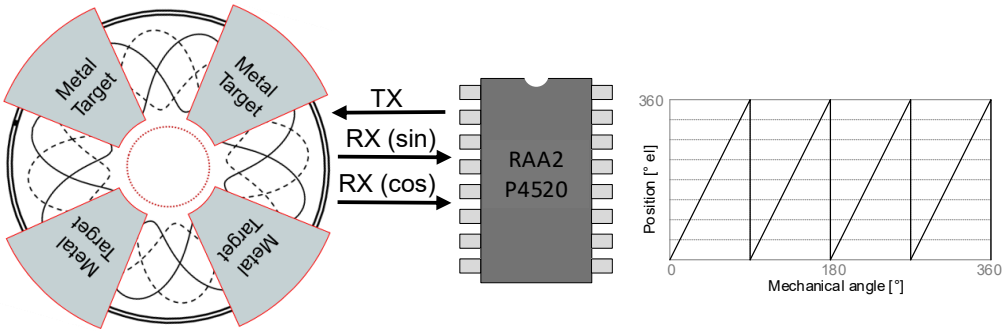


Figure 10. Coil design using 4-periodic coil

3.3.3 Dual Coil High Resolution Mode

The RAA2P4520 supports dual receiver coils inputs and can be configured in high-resolution mode. By defining specific combinations of receiver coils with different numbers of pole pairs on the primary and secondary receivers, the device achieves highly accurate position measurements. In this configuration, the primary coil provides multiple periods, while the secondary coil functions as a reference track, enabling period identification for the primary signal. Two high-resolution modes are available: One track mode or Vernier mode. For available configuration options and the corresponding output resolution, see the following table.

Table 12. High Resolution modes

High Resolution mode	Primary coil [periods]	Secondary coil [periods]	Resolution [bits]
One Track mode	4	1	16
	8		17
	16		18
	32		19
Vernier mode	4	3	16
	8	7	17
	16	15	18
	32	31	19

When the primary coil is configured with 32 pole pairs, the device achieves maximum resolution of 19 bits across the UART and SENT interfaces.

The high-resolution data is stored in two separate registers (hires_lsb 0x028A, hires_msb 0x028C). To ensure data coherency, registers must be accessed in the following order when reading over the UART interface:

1. Read LSB register (0x028A)
2. Read MSB register (0x028C)

Reading the LSB register via digital interfaces (UART) automatically freezes the MSB register content, preventing data corruption during the read sequence and ensuring both register values correspond to the same measurement sample.

3.3.3.1 One Periodic Reference Track Mode

In this mode, the primary coil can be configured with 4, 8, 16, or 32 periods. The secondary coil functions as a reference track, featuring a single pole pair (see Figure 11).

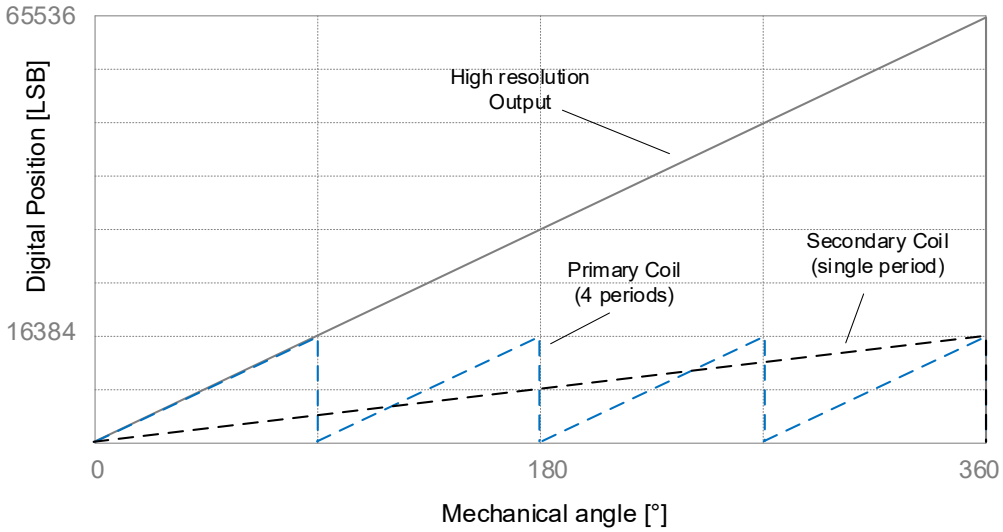


Figure 11. One track mode with single periodic reference track

3.3.3.2 Vernier Reference Track Mode

In Vernier reference track mode, the primary and secondary coils are configured with different period counts to create a vernier measurement system as displayed in the following table.

Table 13. Coil configuration

Primary coil periods	Secondary coil periods
4	3

Primary coil periods	Secondary coil periods
8	7
16	15
32	31

The secondary coil is always configured with one period less than the primary coil (see Figure 12).

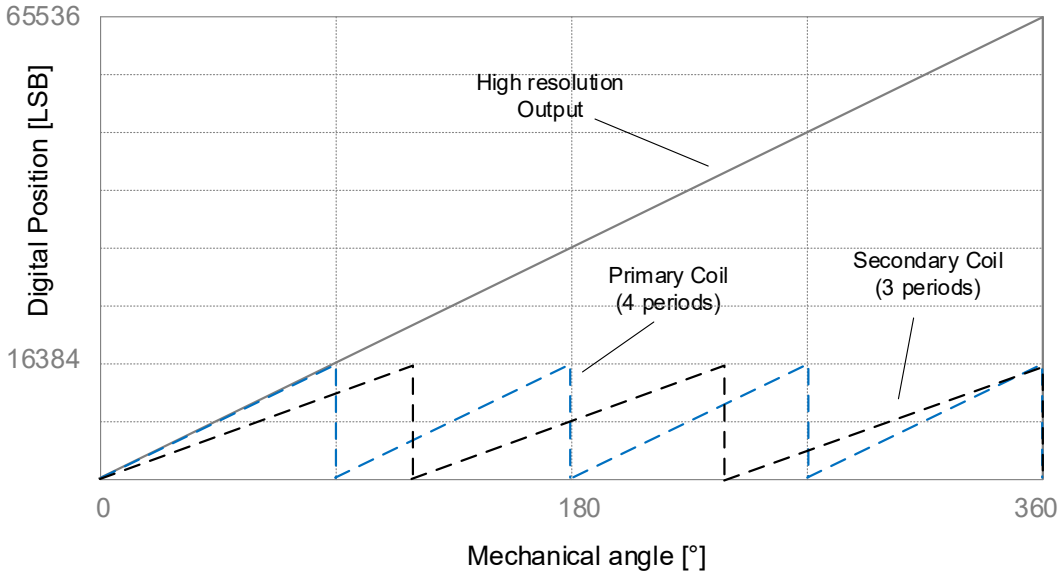


Figure 12. High resolution mode with vernier configuration

3.3.3.3 Coil Synchronization

To prevent sudden jumps in the output position, it is crucial to ensure zero position synchronization between the primary and secondary coils. The maximum allowable shift between their zero positions varies based on the selected primary coil configuration, as detailed in Table 14.

Table 14. High resolution coil synchronization

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Z_{Sync}	Zero position shift between primary and secondary coil.	One periodic reference highres_mode = N, 1	> -180	-	< 180	°electrical of primary coil period
		Vernier reference highres_mode = N, N-1	> -180/(N-1)	-	< 180/(N-1)	°electrical of primary coil

4. Linearization

The RAA2P4520 offers a very flexible linearization feature to enhance sensor accuracy. The linearization algorithm is applied digitally after an angle calculation. The linearization is performed with 16-bits resolution over a 360° electrical range (el.). Up to 16 programmable linearization points can be positioned within a grid of 0.088° in both X (position) and Y (expected output) directions and must be shared between primary and secondary coils.

Figure 13 shows an example of the impact of linearization, showing that the total error is significantly reduced.

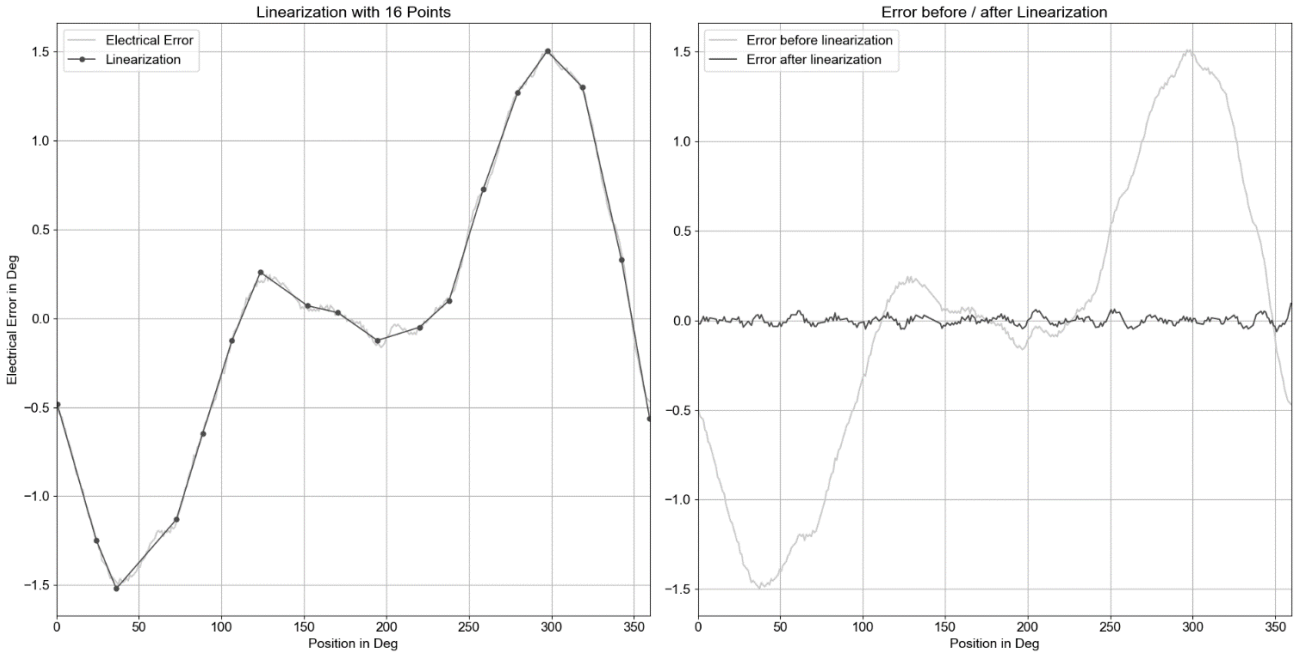


Figure 13. Example of a 16-point linearization

Figure 14. Linearization parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
N_{P_Lin}	Number of linearization points		-	-	16	-
$Grid_{LIN}$	Placement grid of linearization points	In X and Y	0.088			°el
Res_{Lin}	Resolution of linearization transfer function	X and Y coordinates	12			bits

Note 1 The slope of each segment ($\Delta Y/\Delta X$) is automatically calculated from the X and Y parameters of adjacent linearization points. If two adjacent points are positioned with a slope outside the specified range (see Figure 14), the slope is reset to 0 to prevent an overflow of the calculated slope value.

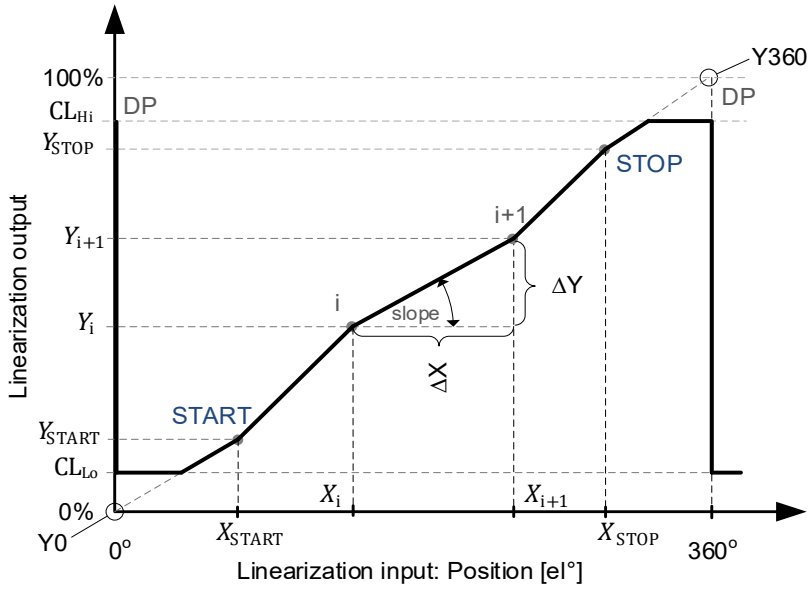


Figure 15. Linearization transfer function parameters

Table 15. Linearization parameter settings

Parameter	Description	Programming options	Resolution
P_{Lin}	Number of total linearization options Note 1	Up to 16 points can be assigned to the primary and secondary coils in multiple combinations	-
D_P	Discontinuity point, Zero position transition from 0/360°	0° to <360°el.	0.088°el./LSB
X_{Start}	Mechanical start position, first linearization point		
Y_{Start}	Expected output at XStart, first linearization point		
X_i	Mechanical position of linearization point (i = 1 to 16, including start and stop)		
Y_i	Expected output at linearization point (i = 1 to 16 including start and stop)		
X_{Stop}	Mechanical end position, last linearization point		
Y_{Stop}	Expected output at XStop, last linearization point		
CL_{Hi}	Output Clamping level, high	0% to 100% VDD	12 bits (VDD/4096)/LSB
CL_{Lo}	Output Clamping level, low		
Y0	Position at DP, start value at X = 0°	0°/360°el.	-
Y360	Position at DP, stop value at X = 360°	0°/360°el.	-

Note 1 Up to 16 Linearization points can be shared between both coil sets. Several options are possible, for example, 8+8 configuration reserves 8 linearization points for the primary coil and 8 points for the secondary. For more information, see *RAA2P4520 Programming Manual*.

5. Interfaces

5.1 SENT Interface

The sensor is equipped with a SENT interface compatible with SAE J2716 Standard, Rev. April 2016. The main features are the following:

- Configurable tick time (1.5 µs, 3 µs, 6 µs with pulse shaping output, down to 0.1 µs with push-pull output)
- Configurable pause pulse
- Support Enhanced Serial message with 8-bits ID and 12-bits Data
- 8 different fast channel configurations
- Serial message cycle length selectable between 16 or 32 messages
- Signal shaping for reduced EMI.

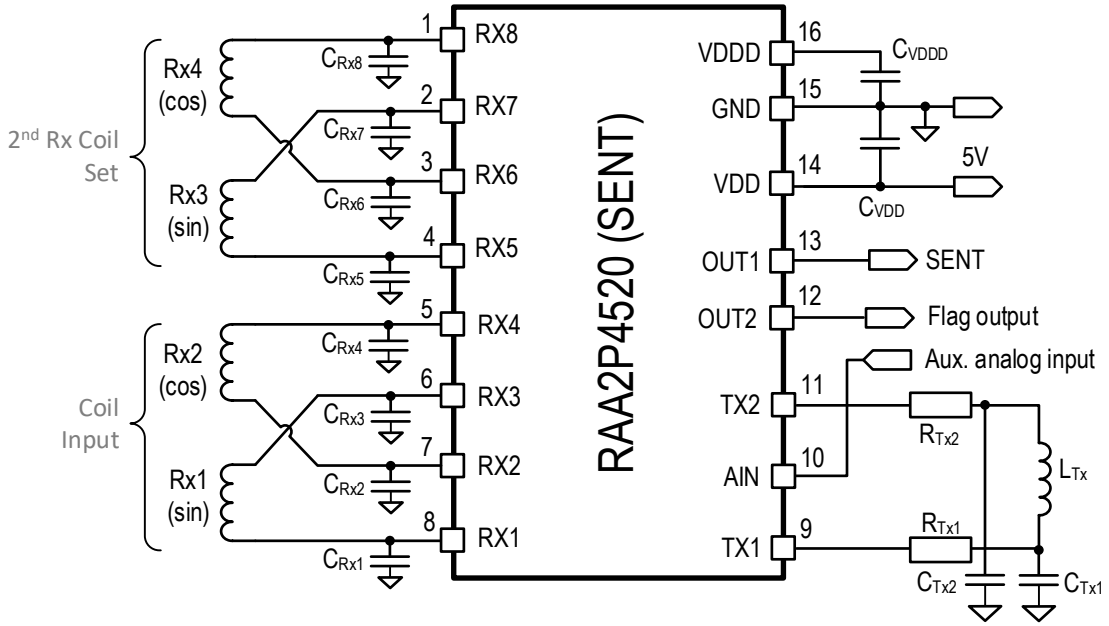


Figure 16. SENT interface with dual coil (RAA2P4520)

Table 16. SENT interface user programming options

SENT programming parameter	Number of options	Programming option
SENT tick time	1024	0.02 to 6 µs Note: < 1.5 µs tick time in push-pull mode only
SENT fast channel frame	8	See Table 19
SENT pause pulse	3	No pause, fixed length pause, Constant frame length, see Table 18
Serial message protocol	3	Disabled, 16 or 32 messages (see Table 20 and Table 21)
CRC calculation method	2	As defined by SENT Standard SAE-J2716, Apr2016: "recommended" or "legacy" calculation method

5.1.1 SENT Protocol Frame

The SENT protocol frame consists of a fixed-length sync pulse (LOW period of 5 ticks followed by a HIGH period of 51 ticks), followed by a status nibble, 6 data nibbles, and a CRC nibble. An optional pause pulse can be programmed to adjust the SENT frame to a fixed length of 282 ticks.

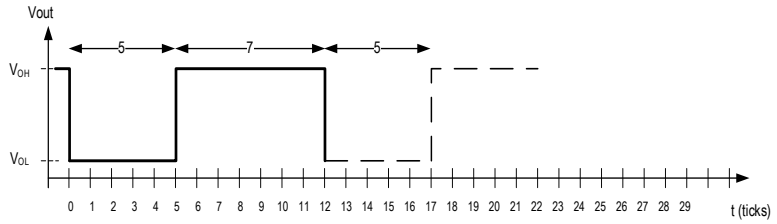


Figure 17. SENT nibble output for value = 0_{DEC}

For transmitting a nibble with the 0 value, 12 clock ticks are required: a fixed LOW period of 5 ticks followed by a HIGH period of 7 ticks.

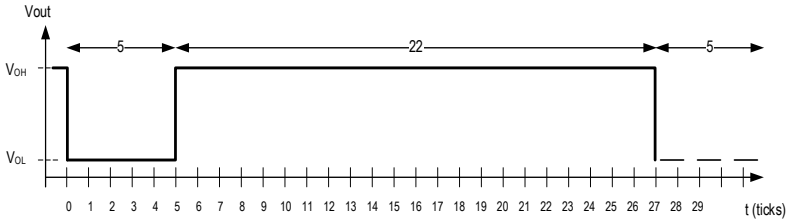


Figure 18. SENT nibble output for value = 15_{DEC}

For transmitting a nibble with the value 15_{DEC} (1111_{BIN}, F_{HEX}), 27 clock ticks are required: a fixed LOW period of 5 ticks followed by a HIGH period of 22 ticks.

The total time for one nibble can be calculated as with the following equation:

$$t_{NIBBLE} = t_{TICK} \times (12 + x) \qquad \text{Equation 13}$$

Where:

- x = the nibble decimal value = 0 to 15.
- t_{TICK} = the length of one tick, which is programmable.

Table 17. SENT tick counts

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Number of Ticks	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27

The tick time can be programmed in a wide range from 0.02 to 6 µs, see Table 16.
Table 18 shows examples for the most common tick times, 1.5 µs, 3.0 µs, and 6.0 µs.

Table 18. SENT tick time programming options

SENT Tick Time	**SENT frame length without pause pulse**		**SENT frame length with pause pulse (programmable)**	
	Total frame length (min 154 ticks)	**Total frame length (max 270 ticks)**	**Constant frame minimum = 282 ticks**	**Constant frame maximum = 922 ticks**
1.5 µs	231 µs	405 µs	423 µs	1383 µs
3.0 µs	462 µs	810 µs	846 µs	2766 µs
6.0 µs	924 µs	1620 µs	1692 µs	5532 µs

5.1.2 Operation and Frame Format

The SENT transmitter controller supports both fast channel message and serial message formats.

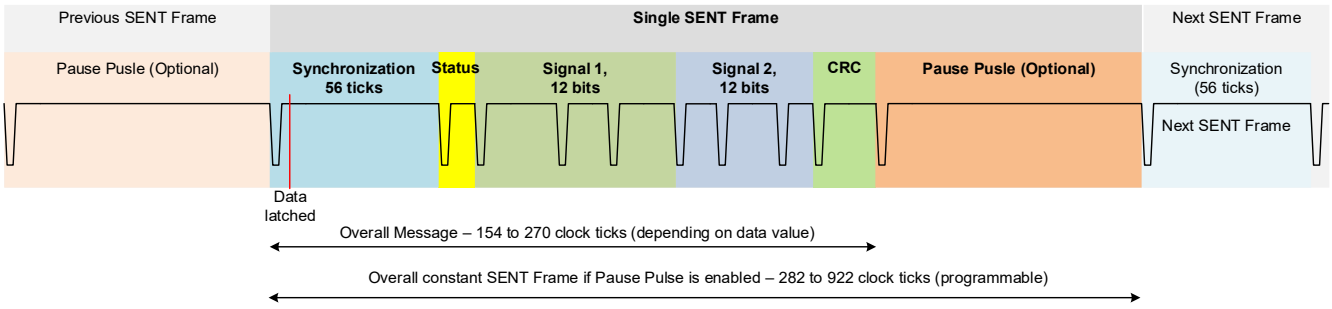


Figure 19. Typical SENT data frame

Several fast channel modes are available, providing combinations of primary and secondary coils (coil set 1 and 2), analog input, and the difference between both coil positions.

Table 19. SENT fast channel frame options

SENT fast channel frame									
Nibble #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**SAE J2716 Reference**
Programming Option	Status	Signal 1 (12-bit)			Signal 2 (12-bit)			CRC	
Option 0: Secure Angle Sensor		12-bit MSB position data (Primary receiver coils) MSN → LSN			8-bit rolling counter		4-bit inverted MSB		H.4: 12+8+4 bits
Option 1: Dual Throttle Sensor		12-bit MSB position data (Primary receiver coils) MSN → LSN			12-bit analog input LSN → MSN				H.1: 12+12 bits
Option 2: Dual Throttle Sensor		14-bit MSB position data MSN → LSN				10-bit analog input LSN → MSN			14+10 bits
Option 3: Dual Throttle Sensor		12-bit MSB position data (Primary receiver coils) MSN → LSN			12-bit MSB position data (Secondary receiver coils) LSN → MSN				H.1: 12+12 bits
Option 4: Torque Sensor		12-bit position data (Primary receiver coils) MSN → LSN			12 LSBs of 14-bit position data difference (Primary - Secondary receiver coils) = ±45°el. LSN → MSN				H.1: 12+12 bits
Option 5: Steering Sensor		14-bit position data (Primary receiver coils) MSN → LSN				10 LSBs turns counter (Primary receiver coils) LSN → MSN			H.6: 14+10 bits
Option 6: High resolution mode		Up to 19-bit high resolution position data. Combination of Primary and secondary receiver coils					4-bit rolling counter		H.6: 14+6+4 bits
		14-bit LSB MSN → LSN				6-bit MSB LSN → MSN			

SENT fast channel frame						
Option 7: Secure Steering Sensor		10-bit position data (Primary receiver coils) MSN → LSN	4-bit rolling counter	10-bit MSB position data (Secondary receiver coils) LSN → MSN		10+4+10 bits

Note 1 The internally calculated resolution is always 14bits at 360°. For options 0, 1, and 3, where 12 bits position data are selected, the 12 MSBs of the 14 bit position data are transmitted.

Note 2 The status nibble bits:

S[3:2] contain the enhanced serial message and they are constant zero if the enhanced serial message is disabled.

S[0] contains the temporary diagnostic state of the IC.

S[1] contains the temporary diagnostic state only in case dual coil configuration is enabled, otherwise it is zero.

5.1.3 Enhanced Serial Message

The enhanced serial protocol message format consists of an 8-bit ID and 12-bit data with 6-bit CRC per frame. In addition, two sets of serial protocol messages are programmable: 16 frames or 32 frames.

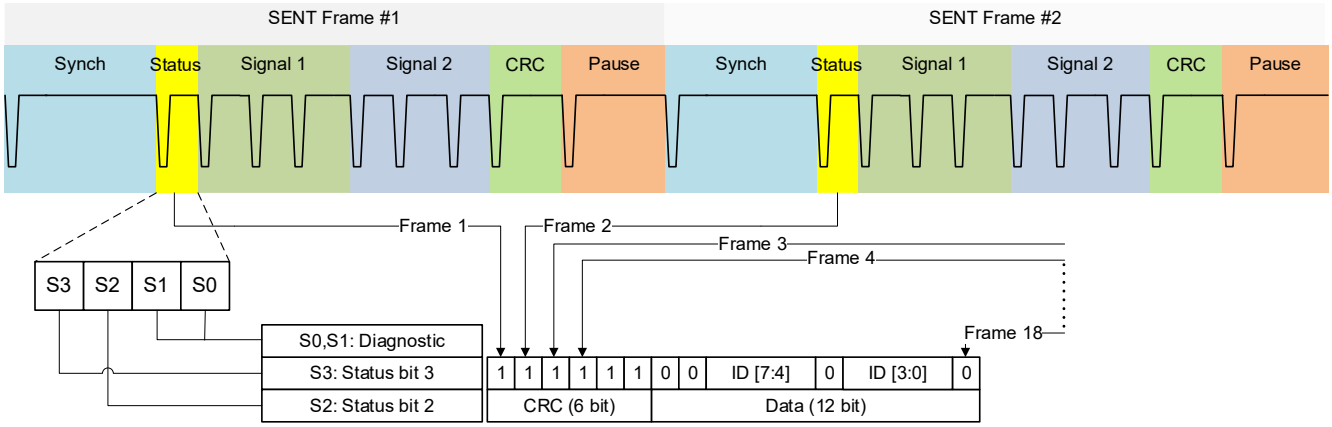


Figure 20. Enhanced serial protocol message format

Table 20. SENT 12-bit enhanced serial protocol data (data frames 1-16)

Frame #	ID (8-bit)	Data (12-bits)	Description
1	01 Hex	Diagnostic Status 1	Mapped to internal status registers: irq_sts0[11:0]
2	03 Hex	Ch1, Ch 2 sensor type	Sensor type according to SENT specification: cust_id2[15:8]
3	05 Hex	Manufacturer Code	Manufacturer Code for RENESAS
4	06 Hex	SENT Standard Revision	04 = SENT Revision 4 J2716 APR2016
5	83 Hex	Diagnostic Status 2	Mapped to internal status registers: irq_sts0[15:12], irq_sts1[7:0]
6	23 Hex	Chip temperature	Internal temperature register: chip_temp
7	29 Hex	Sensor ID 1	USER_ID0: cust_id0[11:0]
8	2A Hex	Sensor ID 2	USER_ID1: cust_id1[7:0], USER_ID0: cust_id0[15:12]
9	84 Hex	Diagnostic Status 3	Mapped to internal status registers irq_sts2[3:0], irq_sts1[15:8]
10	90 Hex	OEM ID 1	Product ID [7:0] bits: prod_id
11	88 Hex	ADC raw SIN data	Primary Coil's ADC raw sine data, 11MSBs out of 13-bits and bit denoting inversion pc_adc_raw_sin[13:2]
12	16 Hex	Turns Counter, Coil 1	Turns counter coil 1 = 12 bit angle1_turns
13	85 Hex	Diagnostic Status 4	Mapped to internal status registers: irq_sts2[15:4]
14	80 Hex	Reserved	Reserved

Frame #	ID (8-bit)	Data (12-bits)	Description
15	81 Hex	Reserved	Reserved
16	89 Hex	ADC raw COS data	Primary Coil's ADC raw cosine data, 11MSBs out of 13-bits and bit denoting inversion pc_adc_raw_cos[13:2]

Table 21. SENT 12-bit enhanced serial protocol data (data frames 17-32)

Frame #	ID (8-bit)	Data (12-bits)	Description
17	86 Hex	Diagnostic Status 5	Mapped to internal status registers irq_sts3[11:0]
18	17 Hex	Turns Counter, Coil 2	Turns counter coil 2 = 12 bit: angle2_turns
19	10 Hex	Coil 2 position	Position of Coil 2: angle2[13:2]
20	12 Hex	Coil 1 AGC setting	Coil 1 AGC: angle1_gain
21	87 Hex	Diagnostic Status 6	Mapped to internal status registers: irq_sts3[15:12]
22	1C Hex	Analog Input	Analog input, 12 MSBs out of 13-bits: adc_hk_ana_in[12:1]
23	1D Hex	Analog reference voltage (VDDD)	Analog input reference (VDDD) 12 MSBs out of 13-bits: adc_hk_vdda_ref[12:1]
24	18 Hex	Coil 2 AGC setting	Coil 2 AGC: angle2_gain
25	01 Hex	Diagnostic Status 1	Mapped to internal status registers: irq_sts0[11:0]
26	91 Hex	OEM ID2	0x632 (ASCII coded "RA")
27	2B Hex	Sensor ID 3	cust_id2[3:0], cust_id1[15:8]
28	2C Hex	Sensor ID 4	cust_id2[7:4]
29	82 Hex	Reserved	Reserved
30	92 Hex	OEM ID3 (optional)	0x4A1 (ASCII coded "A2")
31	93 Hex	OEM ID4 (optional)	0x430 (ASCII coded "P0")
32	94 Hex	OEM ID5 (optional)	0x410 (ASCII coded "00")

5.1.4 SENT Load Circuits

Load circuit components are shown in Figure 21 for the legacy SENT interface and Figure 22 for the recommended SENT interface. All components are specified according to specification SAE J2716 – APR2016.

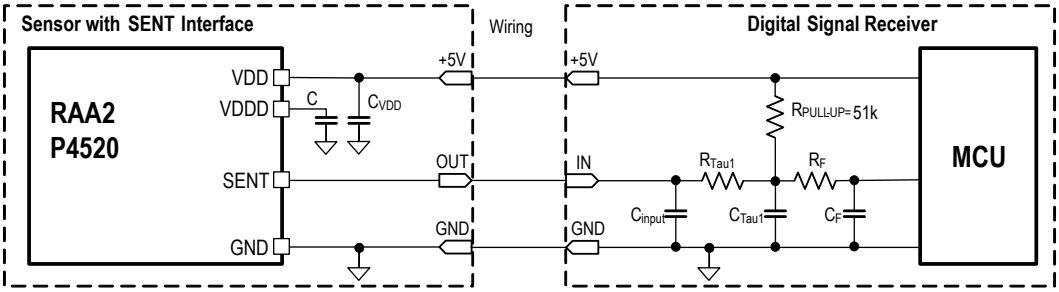


Figure 21. Legacy SENT interface load circuit

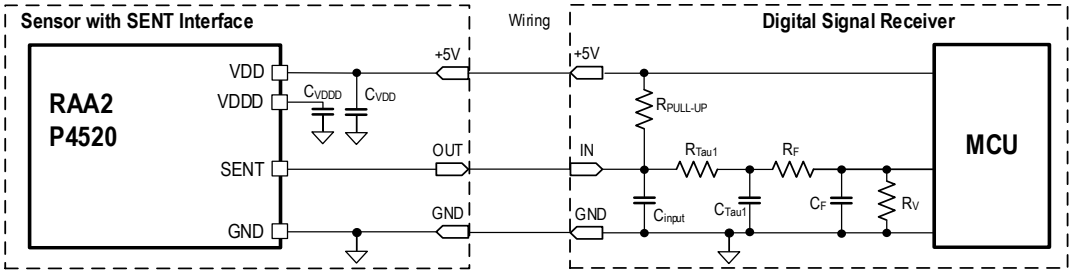


Figure 22. Recommended SENT interface load circuit

Table 22. SENT load circuit components

Component	Function	Minimum	Typical	Maximum	Units
C_{VDD}	VDD external supply buffer capacitor	See Table 5			nF
C_{VDDD}	VDDD internal digital supply buffer capacitor				
C_{input}	Parasitic input capacitance from ESD protection			100	nF
R_{Tau1}	Input filter resistor (first stage)	448	560	672	Ω
C_{Tau1}	Input filter capacitor (first stage)	1.54	2.2	2.86	nF
Tau_1	Input filter time first stage time constant defined by RTau1 and CTau1	0.74		1.73	µs
$R_{PULL-UP}$	Input Pull-up resistor	10		55	kΩ
R_F	Input filter resistor (second stage)	4			kΩ
C_F	Input filter capacitor (second stage)	Determined by TAU2 requirement			nF
R_V	Voltage divider, adjusting SENT output level to MCU input level	Optional, depends on MCU input			kΩ
Tau_2	Input filter time 2nd stage time constant defined by RV, RF, and CF	0.6		1.4	µs

5.2 High-Speed UART Interface

Performing an end-of-line calibration or in-line programming of a position sensor module containing the RAA2P4520, requires no additional wires. The chip is programmed through the OUT1 output at the operative supply voltage range (5V ±10%).

A short programming window is enabled after POR and requires a digital unlock password to enable programming. If no password is sent, the chip resumes its normal operating mode.

For more details, see *RAA2P4520 Programming Manual*.

Additionally, when the UART interface is enabled as the primary back-end interface, additional modes are available as described in Table 23.

Table 23. UART operation modes

Operation mode	Single wire	Dual wire differential	Dual wire
Direction	Bi-directional	Bi-directional	Uni-Directional
Pin 13: OUT1	RxD/TxD	RxD/TxD	RxD
Pin 12: OUT2	Not used	TxD complementary open drain	TxD open drain or push-pull

Note 1 All modes are half duplex data transmission.

Table 24. UART interface user programming options

Incremental interface programming parameter	# of options	Programming option
UART output drive	2	Open drain or push-pull
UART Slave Address	4	2 LSBs of general slave address
UART Baud rate	6	{9600, 57600, 115200, 230400,1M,2M} bit/s
UART operation mode	3	See Table 23
UART Error warnings	7	Baud rate, framing, CRC errors

Note 1 Maximum data rate may be reduced by external capacitive and resistive loads when open drain configuration is used.

5.2.1 Single Wire Bidirectional UART (Default)

In single wire UART mode, the device communicates with the ECU using only OUT1 pin, which can be configured in either push-pull or open drain mode. This mode is suitable for point-to-point connections where one device interfaces directly with an ECU or for implementing a multi-slave single bidirectional wire connection. (Figure 23). Single wire UART is the default programming interface.

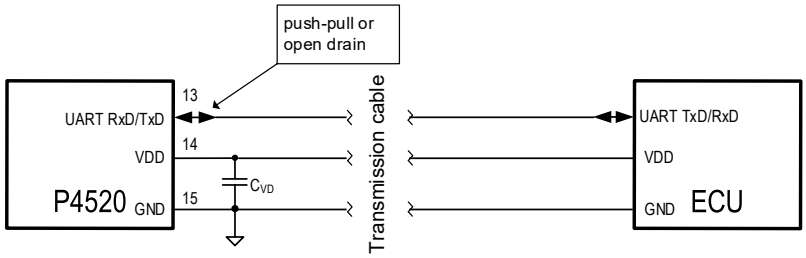


Figure 23. UART 1-wire point-to-point single wire bi-directional connection

In open drain mode, a single master can address up to four sensors over a single wire, communicating with one sensor at a time. Each sensor is identified by its slave address, stored in the NVM.

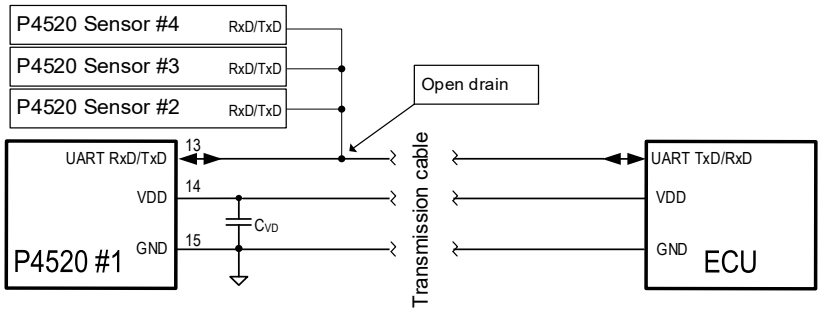


Figure 24. UART 1-wire multi-slave single wire bi-directional connection

5.2.2 Dual Wire Bidirectional UART with Pseudo-Differential TX

In dual wire UART mode, the device uses both OUT1 and OUT2 pins for communication. A point-to-point connection can be implemented as shown in Figure 25. This communication mode employs OUT1 as a single wire transceiver, Figure 26.

In addition, OUT2 (pin 12) is used as the transmitter and OUT1 (pin 13) is used for both transmitting and receiving. OUT1 carries inverted information of the transmitted data, creating a pseudo differential signal for more reliable data transmission. During reception, OUT1 is kept in high state.

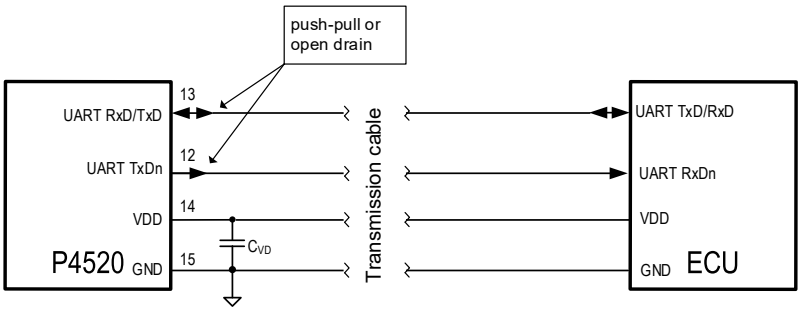


Figure 25. UART 2-wire connection with pseudo-differential transmitter

In pseudo-differential mode, with open drain configuration, a single Master can address up to four sensors, communicating with one sensor at a time. Each sensor is identified by its slave address, stored in the NVM.

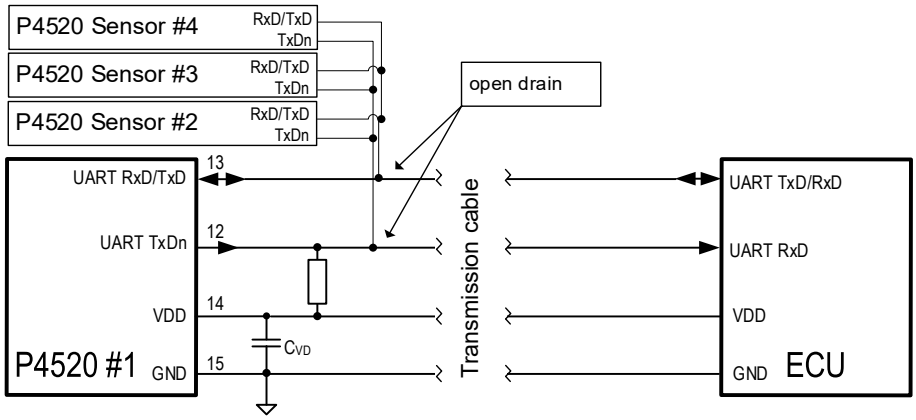


Figure 26. UART 2-wire connection with pseudo-differential transmitter and multiple slaves

5.2.3 Dual Wire Unidirectional UART

In this dual wire mode, separate unidirectional lines are used for transmitting and receiving data. The transmitter can be configured either for push-pull or open-drain output. Push-pull mode is recommended for achieving data rates up to 2Mbit/s. In open-drain mode, data rates may be limited, depending on the capacitive load on the transmission cable and the resistance of the pull-up resistor.

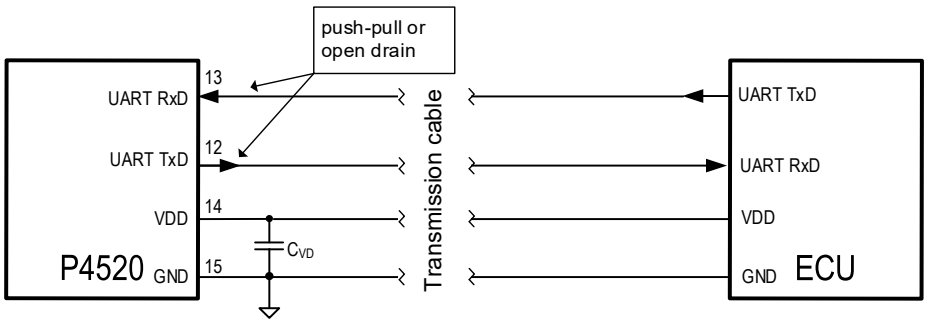


Figure 27. UART 2-wire uni-directional connection

In dual wire unidirectional mode, a single Master can address up to four sensors, communicating with one sensor at a time. Each sensor is identified by its slave address in the NVM. When connecting multiple sensors in parallel on the same line, the transmitter output (TxD) must be configured for open drain output.

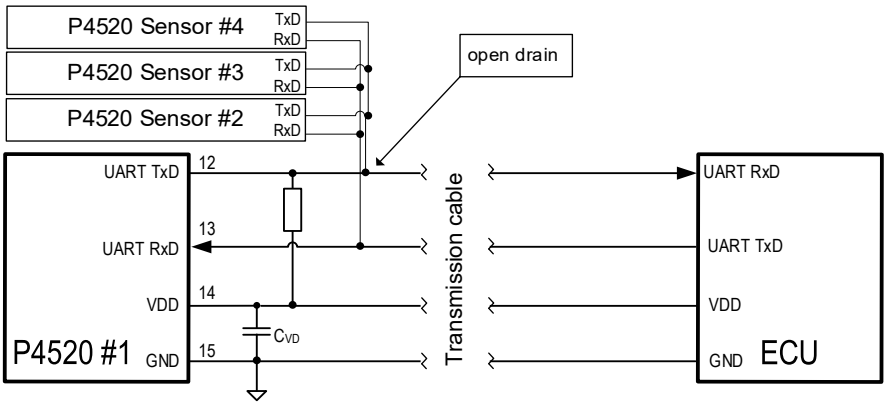


Figure 28. UART 2-wire uni-directional connection with multiple slaves

The transmission cable can be extended with external bus transceiver circuits as shown in Figure 29, providing extra robustness and low capacitive load for the UART TxD output pin, enabling high data rates.

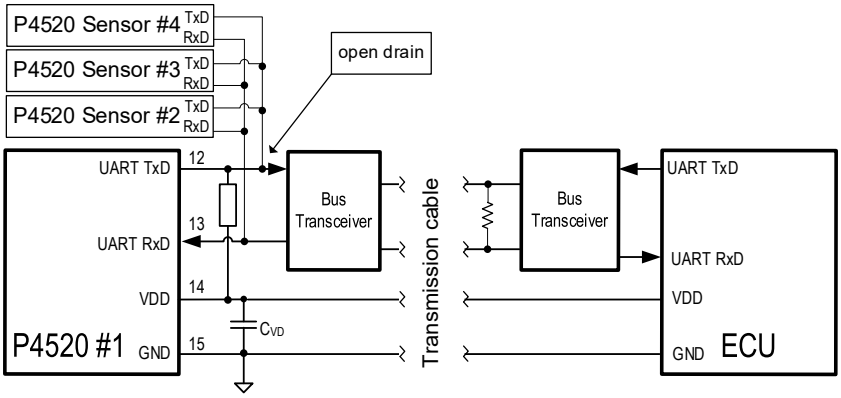


Figure 29. UART 2-wire uni-directional connection with multiple slaves and bus transceivers

5.2.4 UART Operating Modes

The RAA2P4520 provides the following operating modes:

- 16-bit register read (Table 27)
- 16-bit register write (Table 28)

Fast read mode of two registers within one frame with 12,14 or 16 bits of data per register (Table 29, Table 30).

5.2.4.1 1-Wire Bi-Directional and 2-Wire Uni-Directional Configuration

Each frame consists of 8 bytes, with each byte including a start and stop bit, resulting in a total of 8 × 10bits per frame. A brief wait time, referred to as GAP, is required between frames, see Table 26. In total, each frame contains either 90 bits for data rates up to 230.4 kbit/s or 92 bits for 1 Mbit and 2 Mbit data rates. In all modes, the bit order is from MSB to LSB.

5.2.4.2 2-Wire Pseudo-Differential Configuration

Each frame is composed of 8 bytes, with each byte including a start and stop bit, totaling 8 × 10bits. For data read operation , an additional wait bit is required by the master when switching from sending to receiving due to the generation of differential start and stop bits. A short wait time, or GAP, is necessary between frames, see Table 26. In total, each frame contains either 91 bits for data rates up to 230.4 kbit/s or 93 bits for 1Mbit and 2 Mbit data rates.

In data write operation, the wait bit is optional without it, the frame size is as specified in Section 5.2.4.1. In all modes, the bit order is from MSB to LSB.

5.2.4.3 Pause/Gap Time between Messages

Minimum pause (GAP) is required between messages to ensure the controller returns to idle state before subsequent communications. The minimum gap time varies with UART baud rate configuration as shown in Table 25.

Table 25. UART wait time between measurements

UART baud rate [bits/s]	Min gap time [bits]
9600, 57600, 115200, 230400	10
1M, 2M	12

5.2.4.4 UART Register Write

This mode writes one register per frame. Each frame consists of 8 bytes, each accompanied by a start and stop bit, resulting in 8x10bits. A short wait (gap) time is required between each frame to ensure proper data transmission. The frame structure permits write access for all bytes, with the data being transmitted from the master to the chip.

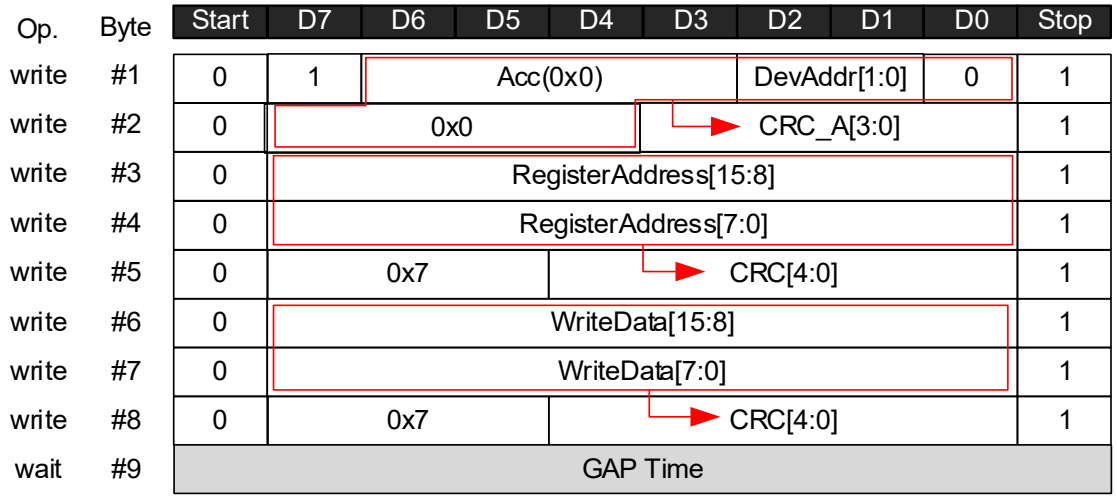


Figure 30. UART register write mode

Fields have the following information:

- Acc = Access type: must be 0x0 for register write.
- DevAddr = Device address: default = 0x0. If several sensors are connected in parallel, it defines their slave address (0x1..0x3).
- Register Address = The register to be written to
- Write Data = The data to be written to Register address
- CRC = Cyclic redundancy check

5.2.4.5 UART Register Read

In read mode, the device reads one register per frame. The first 5 bytes are sent from master to the chip, while on bytes 6 to 8 are read from the chip. In all modes, the bit order is MSB to LSB. Each read frame contains 8 bytes, each with a start and stop bit, resulting in 8x10 bits. A short wait (gap) time is required between each frame.

For performing a data read operation, due to the generation of the differential start and stop bits, an additional wait bit must be added by the master when switching from sending data to receiving data. This results in each frame containing either 91 bits (for data rates up to 230.4 kbit/s) or 93 bits (for 1 Mbit and 2 Mbit data rates).

In register read mode, an additional wait bit must be added at the end of byte 5 before the chip can start transmitting data (start bit of byte 6). The ReadData content is latched at the stop bit of byte 5.

To ensure the accurate reading of high-resolution data, it is essential to begin by reading hires_lsb register first. This operation locks hires_msb that needs to be read subsequently.

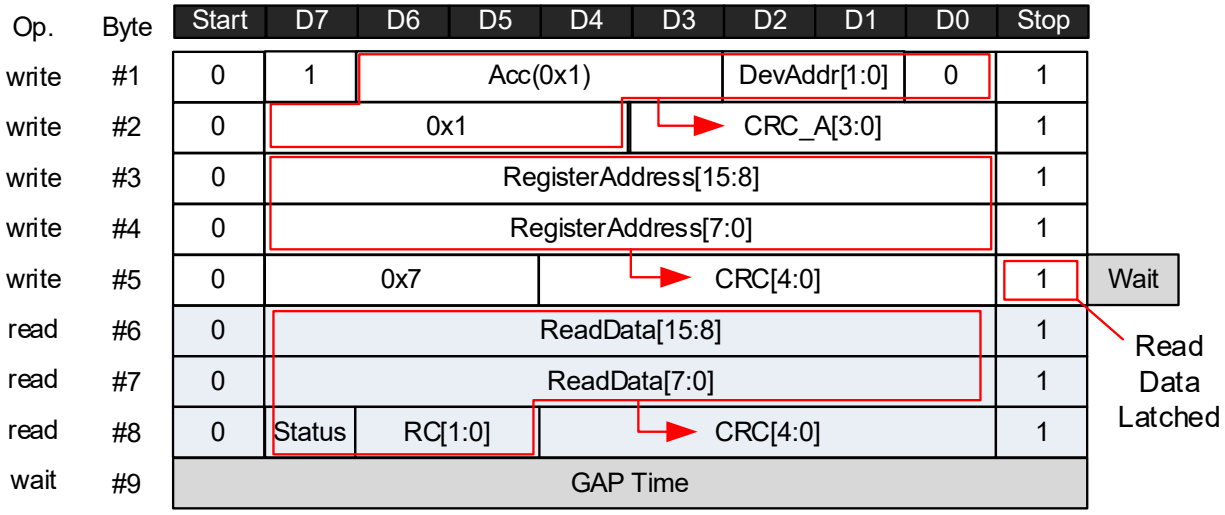


Figure 31. Register read mode

Fields have the following information:

- Acc = Access type: must be 0x1 for register read.
- DevAddr = Device address: default = If several sensors are connected in parallel, it defines their slave address (0x1..0x3).
- Register Address = The register to be read from
- Write Data = The contents of the data read from Register address
- CRC = Cyclic redundancy check.
- Status = 1 bit status information of the sensor (0 = normal operation , 1 = error)
- RC = Rolling counter, a counter that increments with each frame and wraps around 0 when overflowing
- Wait = 1 bit wait time for master before receiving data (in pseudo-differential mode only)

NOTE
To read high resolution data using register read mode, first access hires_lsb, which lockshires_msb gets, and then proceed to read hires_msb.

5.2.4.6 UART Fast Two-Register Read

This mode reads two predefined registers per frame using 4-bit access code to specify the target registers.

Table 26. UART access types for fast read mode

Acc Type1/2	Byte3/Byte 6		Byte 4/Byte 7		Byte 5/Byte 8		
2	PC Sensor Data[11:4]		PC Sensor Data[3:0]	RC[5:2]	S	RC[1:0]	CRC[4:0]
3	SC Sensor Data[11:4]		SC Sensor Data[3:0]	RC[5:2]	S	RC[1:0]	CRC[4:0]
4	PC Sensor Data[13:6]		PC Sensor Data[5:0]	RC[3:2]	S	RC[1:0]	CRC[4:0]
5	SC Sensor Data[13:6]		SC Sensor Data[5:0]	RC[3:2]	S	RC[1:0]	CRC[4:0]
6 (ACC1)	HiRes LSB [13:6]		HiRes LSB [5:0]	RC[3:2]	S	RC[1:0]	CRC[4:0]
6 (ACC2)	HiRes MSB[4:0]	0x0	0x0	RC[3:2]	S	RC[1:0]	CRC[4:0]
7	Chip Temperature		0x0	RC[5:2]	S	RC[1:0]	CRC[4:0]

Acc Type1/2	Byte3/Byte 6	Byte 4/Byte 7			Byte 5/Byte 8		
8	Analog input [12:5]	Analog input [4:0]	0	RC[3:2]	S	RC[1:0]	CRC[4:0]
9	PWM Input Data High [15:8]	PWM Input Data High [7:0]			S	RC[1:0]	CRC[4:0]
10 = 0xA	PWM Input Data Low [15:8]	PWM Input Data Low [7:0]			S	RC[1:0]	CRC[4:0]
11 = 0xB	IRQ Status 0 [15:8]	IRQ Status 0 [7:0]			S	RC[1:0]	CRC[4:0]
12 = 0xC	IRQ Status 1 [15:8]	IRQ Status 1 [7:0]			S	RC[1:0]	CRC[4:0]
13 = 0xD	IRQ Status 2 [15:8]	IRQ Status 2 [7:0]			S	RC[1:0]	CRC[4:0]
14 = 0xE	IRQ Status 3 [15:8]	IRQ Status 3 [7:0]			S	RC[1:0]	CRC[4:0]
15 = 0xF	IRQ Status 4 [15:8]	IRQ Status 4 [7:0]			S	RC[1:0]	CRC[4:0]

Note 1 Legend:

PC: Primary coil (coil set 1)

SC: Secondary coil (coil set 2)

RC: Rolling counter

HiRes: High resolution mode (combination of coil sets 1 and 2) position result: up to 19 bit

The first two bytes of the frame allow the user to specify which subset of the two pre-defined registers to read, using a 4-bit access code. This is achieved by setting the access type on the *Acc1* and *Acc2* bitfields (see the following figure. The readout data for the first register is contained in bytes 3 to 5 while bytes 6 to 8 contain the data for the second register.

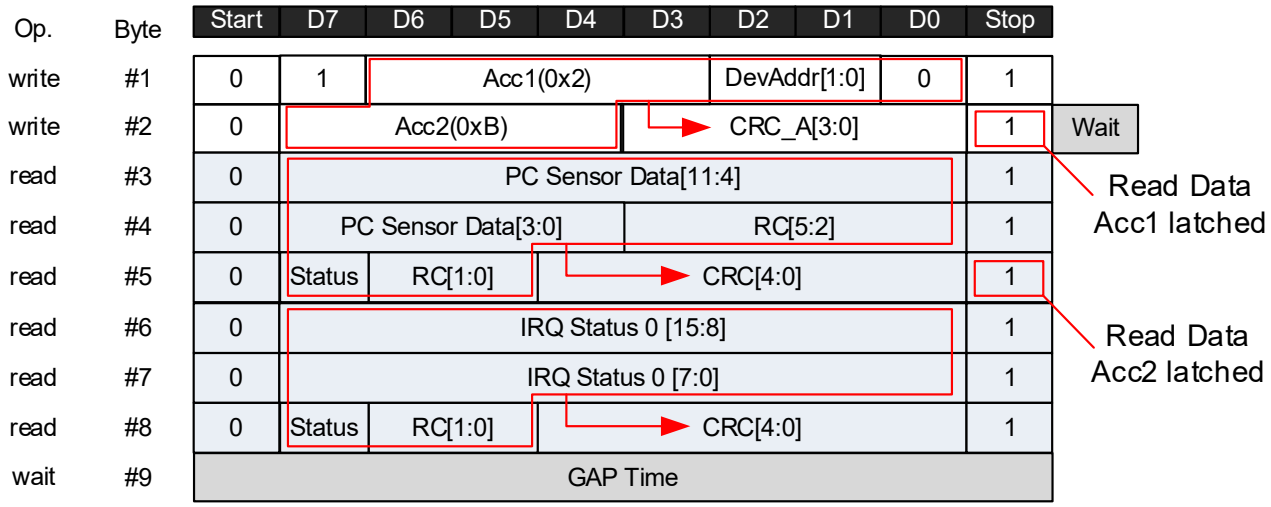


Figure 32. UART fast read mode with different access codes

See the frame structure on Table 20 with an example of reading 12-bit primary coil sensor data (Acc1 = 0x2) and 16-bit IRQ status 0 (Acc2 = 0xB), the frame bitfields are the following:

- Acc1, Acc2 = Access type: 0x2 to 0xF
- DevAddr = Device address: default = 0x0. If several sensors are connected in parallel, it defines their slave address (0x1..0x3).
- CRC = Cyclic redundancy check.
- Status = 1 bit status information of the sensor (0 = normal operation , 1 = error)
- RC = Rolling counter, a counter that increments with each frame and wraps around 0 when overflowing
- Wait = 1 bit wait time for master before receiving data (in pseudo-differential mode only)

In fast read mode, an additional wait bit must be added at the end of byte 2 before the device can start transmitting data.

5.2.4.7 UART Fast Read Mode with Same Access Code

Reading the same register twice provides two results from the same input but at different sampling time stamps. For example, in the configuration shown in Figure 33, the primary coil sensor data is read twice. The first reading (Acc1 = 0x2) is sampled at the end of Byte 2, while the second reading (Acc2 = 0x2) is sampled at the end of Byte 5. The interval between these two results is 30 bits of the UART clock (3 bytes, including start and stop bits).

By repeating this sequence, the user can obtain two samples within a 92-bit frame. The timeframe between each consecutive sample is 30 UART clock cycles resulting in 15 µs at 2 M/s Baud rate. However, the time between each frame is 46 µs at the same Baud-rate.

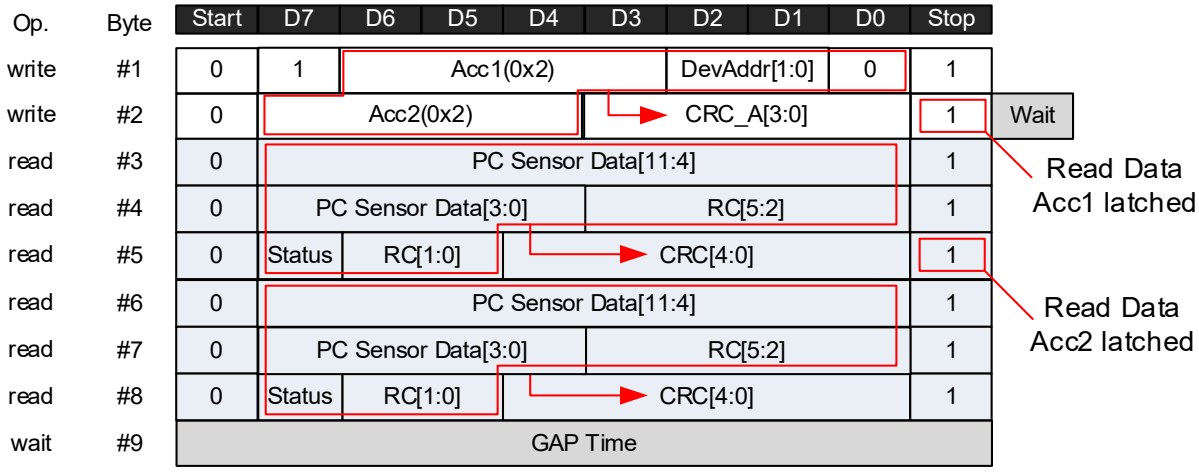


Figure 33. UART fast read mode of the same register

5.2.4.8 High Resolution Mode Data

The device can provide high-resolution position information up to 19 bit. This requires two readings from the same access type (*Acc* = 0x6), split into the 14 LSBs and the 5 MSBs of the 19-bit data. In this mode, Bit D0 in byte 1 must be set to 0. The position is latched at the stop bit of Byte 2.

Both *Acc1* and *Acc2* must be set for access type 0x6. Bytes 3 to 8 transmit the full high resolution information including CRC and status bits.

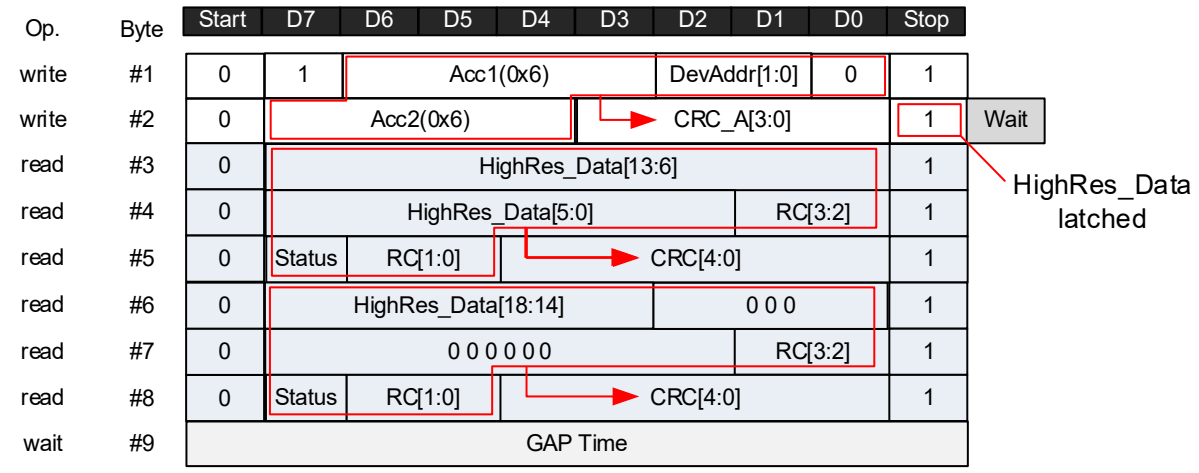


Figure 34. UART fast mode: high resolution position information

See Table 27 for a summary of the UART interface speed, based on the selected Baud rate and mode. Note that one frame can perform various operations such as register read, register write, or two consecutive register read (fast read).

See Table 20 for a summary of the UART interface speed, based on the selected Baud rate and mode. Note that each frame can perform various operations such as register read, register write, or two consecutive register reads (fast read).

Table 27. UART data access speed with uart_start_bit_cfg = 0

UART baud rate [bits/s]	Bits per frame (incl. gap time)	Time per frame [µs]	Frame rate [frames/s]
9600	91	9479.4	105.5
57600	91	1580	633
115200	91	789.9	1265
230400	91	395	2532
1M	93	93	10.75 k
2M	93	46.5	21.5 k

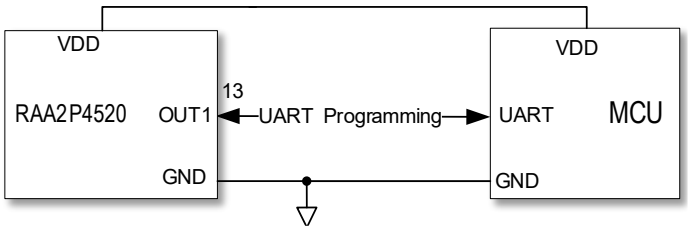


Figure 35. UART single wire NVM programming

5.2.4.9 Memory Lock Feature

The RAA2P4520 includes a user configurable lock bit option, which can be set to restrict write and/or read access. Once the lock bits are enabled, further write or read operations to the RAA2P4520 are prohibited. Following options are available:

- Read/Write allowed: Programming window enabled, start-up time 5ms
- Read only: Reading the memory is allowed
- Locked: Programming window disabled, start-up time 3 ms

NOTE
When a RAA2P4520 part is locked, it cannot be unlocked.

For more information, see *RAA2P4520 Programming Manual*.

6. Auxiliary Input

An auxiliary input pin is available for connecting external devices with an analog interface. This input can be accessed through the SENT interface via the enhanced serial message or by using register read commands over the UART interface.

6.1 Analog Input

The analog input is designed to read an external voltage source like a sensor with analog output. The relevant parameters and specifications are detailed in Table 28. The analog value must be calculated in relation to VDDD.

Table 28. AIN analog input parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IN_AIN}	AIN voltage range		0.2	-	1.2	V
RES_{AIN}	AIN resolution		-	11	-	bits
T_{Smp_AIN}	Sampling rate		1	-	-	kHz
ACC_{AIN10}	Analog Input Accuracy IO1 in relation to VDDD	10-bit output	-1.55	-	1.55	%VDDD
ACC_{AIN12}		12-bit output	-1.5	-	1.5	%VDDD

Internally, both the analog input voltage and the VDDD reference voltage are measured and made available in registers and through the SENT enhanced serial message (see Table 21).

NOTE
The external load on VDDD cannot exceed 1 mA (see Table 5). The maximum value for a 12-bit AIN voltage reading being 7FF h.

7. Diagnostic State, Functional Safety

The RAA2P4520 includes on-chip diagnostics featuring an extensive number of internal Safety Mechanisms.

It has been developed according to ISO26262 for implementation in safety-relevant systems up to ASIL C. It can also be used in ASIL D system-level requirements according to ASIL Decomposition rules (ISO 26262:2018, Part 9, Clause 5”) or proper risk analysis by the system integrator.

For a more detailed description, see *RAA2P4520 Programming Manual* and *RAA2P4520 FuSa Manual*.

Table 29. Diagnostic parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T_{FDTI}	Failure detection time interval (time to detect and internally set a flag describing the error condition)	fdti_cfg=0	-	-	20	ms
		fdti_cfg=1	-	-	2.3	ms

7.1 Diagnostic Checks

An extract of the diagnostic checks is the following:

- VDD pin over- or undervoltage
- Internally regulated VDDD pin over- or undervoltage, short to GND
- Receiver coils open, short to GND, short to VDD, short between coils
- Signal magnitude out of range
- Transmitter coil frequency out of range, coil open, short to VDD, short to GND

- Internal temperature sensor fault, warning or shutdown temperature detected
- Shorted output pin
- Other internally regulated supplies fault
- Internal memory fault
- AGC fault
- Signal non-linearity exceeds pre-programmed limits
- Mechanically broken chip
- Internal power-on self test error

Detailed Functional Safety information is available upon request from Renesas.

8. User Programming Options

Table 30 shows the main configuration options. A detailed description is provided in RAA2P4520 *Programming Manual*, available on request from Renesas.

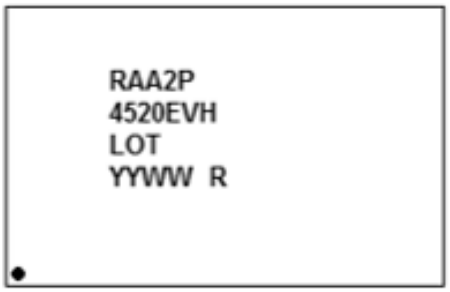
Table 30. Global programming options

Programming Parameter Option	Programming Options, RAA2P4520
Output interface mode	SENT, UART interface
High resolution mode	Disabled, Absolute high resolution mode
Power supply mode	3.3 V ±10% or 5.0 V ±10%
Automatic gain control AGC	Enabled/Disabled
Magnitude upper and lower limit alarm	Static upper and lower magnitude (Sine, Cosine signal strength)
Linearization, X and Y positions	Up to 16 linearization points programmable in X (position) and Y (value)
Zero (discontinuity) points	12-bit discontinuity point
Sine and Cosine signal offset correction	±127 LSBs
Sine and Cosine amplitude mismatch correction	0% to 199% adjustment range per channel
Digital low pass filter	Depth of digital low pass filter for primary and secondary coil position output
Alarm Flags	Enable/Disable internal alarm flags for diagnostic indication, See chapter 0
Customer ID	48-bit scratchpad register for customer specific data
Dynamic amplitude and offset correction	Enable / disable dynamic amplitude mismatch correction (Note: dynamic correction requires full electrical rotation 0° to <360°)
High resolution absolute mode	4/8/16/32 periods on secondary coil

9. Package Outline Drawings

The latest version of the package dimensions is accessible through the Renesas website: TSSOP-16.

10. Marking Diagram



Line 1: First characters of part code RAA2P

Line 2: Next four characters of the part code:
4520: SENT or UART

followed by

E = Design revision

V = Operation temperature range, Extended automotive

H = Automotive Qualified

Line 3: “LOT” = Lot number

Line 4: “YYWW” = Manufacturing date:

YY = last two digits of manufacturing year

WW = manufacturing week

R = RoHS compliant statement

11. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
RAA2P4520EVHSP#HA0	16-TSSOP, 4.4 ×5.0 mm	1	13” Reel, 4000 parts/reel	−40° to +160°C
The following evaluation kits are available:				
RAA2P-COMBOARD	USB communication and programming board for lab evaluation.			
RTKA2P4500S00MC0BE	RAA2P4520MCSTKIT – Starter kit for High-speed motor control applications. It includes one RAA2P-COMBOARD and sensor reference designs.			
RTKA2P4500S00PS0BE	RAA2P4520PSSTKIT– Starter kit for pedal and steering applications. It includes one RAA2P-COMBOARD and sensor reference designs.			

12. Revision History

Revision	Date	Description
1.11	Sep 20, 2026	Updated the ambient temperature range
1.10	Jul 1, 2026	Updated "Noise, Parameter, Conditions" description in Table 8 Updated "ACC conditions, Notes" description in Table 6 Updated "T_{FDTI} conditions" description in Table 29 Updated description in Table 14 Updated "OUT2" description in Table 2 Added Notes in Table 4 Updated typos in Table 20 and in Figure 20 Updated "RX coil pin description" description in Table 1 Updated description in Table 21 Updated description in Table 28
1.00	Nov 26, 2025	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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