RAA489300

3-Level Buck Controller with Pass-Through Mode

Description

The RAA489300 is a high-performance buck controller designed for a 3-level buck topology. This topology delivers exceptional efficiency and significantly reduces the required inductance for regulating the output voltage. Its innovative design minimizes power loss and reduces system size, making it ideal for compact, high-performance applications. In addition, the controller ensures a seamless switching mode transition across the entire output voltage range.

The advanced Renesas R3™ Technology enhances performance by enabling highly efficient light-load operation, fast transient response, and seamless transitions between discontinuous conduction mode (DCM) and continuous conduction mode (CCM).

The RAA489300 is an ideal choice for applications requiring versatile input sources, such as high-power barrel adapters and USB Power Delivery (USB PD) adapters. For USB PD applications, it complies with PD specifications and supports Programmable Power Supply (PPS) and Adjustable Voltage Supply (AVS) operation. Independent control loops for input and output voltages and currents ensure precision, safety, and flexibility.

The device features pass-through mode (PTM) in both forward and reverse directions, maximizing efficiency when the input and output voltages are identical. This makes it especially suitable for applications demanding high efficiency and low power loss.

Beyond its core functionality, the RAA489300 incorporates system-level features such as isolation MOSFET control and an adjustable output voltage. Its robust protection mechanisms, including overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), and over-temperature protection (OTP), ensure reliable and safe operation under all conditions.

The controller also supports serial communication through SMBus/I^{2}C to allow the programing of critical parameters for tailored performance. Customizable parameters include minimum input voltage, maximum output voltage, input current limits, and output current limits, offering flexibility and adaptability for diverse applications.

Features

- Single inductor 3-level buck controller
- Patented modulator for flying capacitor balancing and smooth mode transition
- Wide input voltage range: 4.5V to 57.6V
- Wide output voltage range: 3V to 54.912V
- Programmable switching frequency: up to 400kHz (800kHz at switching node effectively)
- EXT5V pin to generate 5V or 10V gate drive voltage through internal charge pump
- Low shutdown current: 25µA
- Pass through mode (PTM) in both directions
- Support pre-biased output with soft-start
- Input and output current monitor
- Protection features: OCP, OVP, UVP, and OTP
- SMBus and I^{2}C compatible
- 32 Ld 4x4 TQFN package

Applications

- USB PD 3.0/3.1 systems
- Docking stations
- Battery powered mobile devices
- Renewable energy systems
- Robots and drones
- Security surveillance
- Medical equipment

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Contents

1. Overview

1.1 Block Diagram

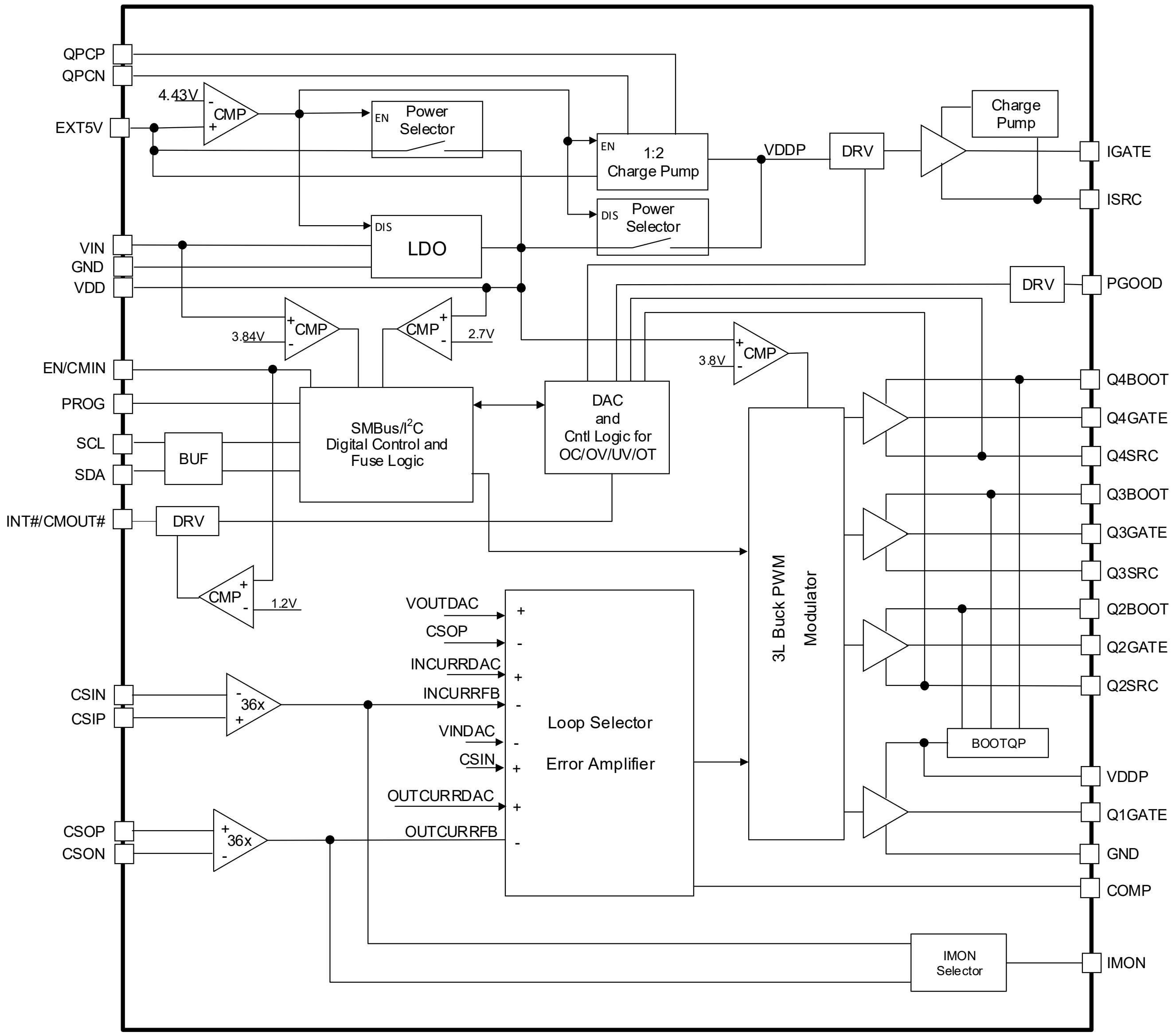


Figure 1. Block Diagram

1.2 Typical Applications

1.2.1 3-Level Configurations

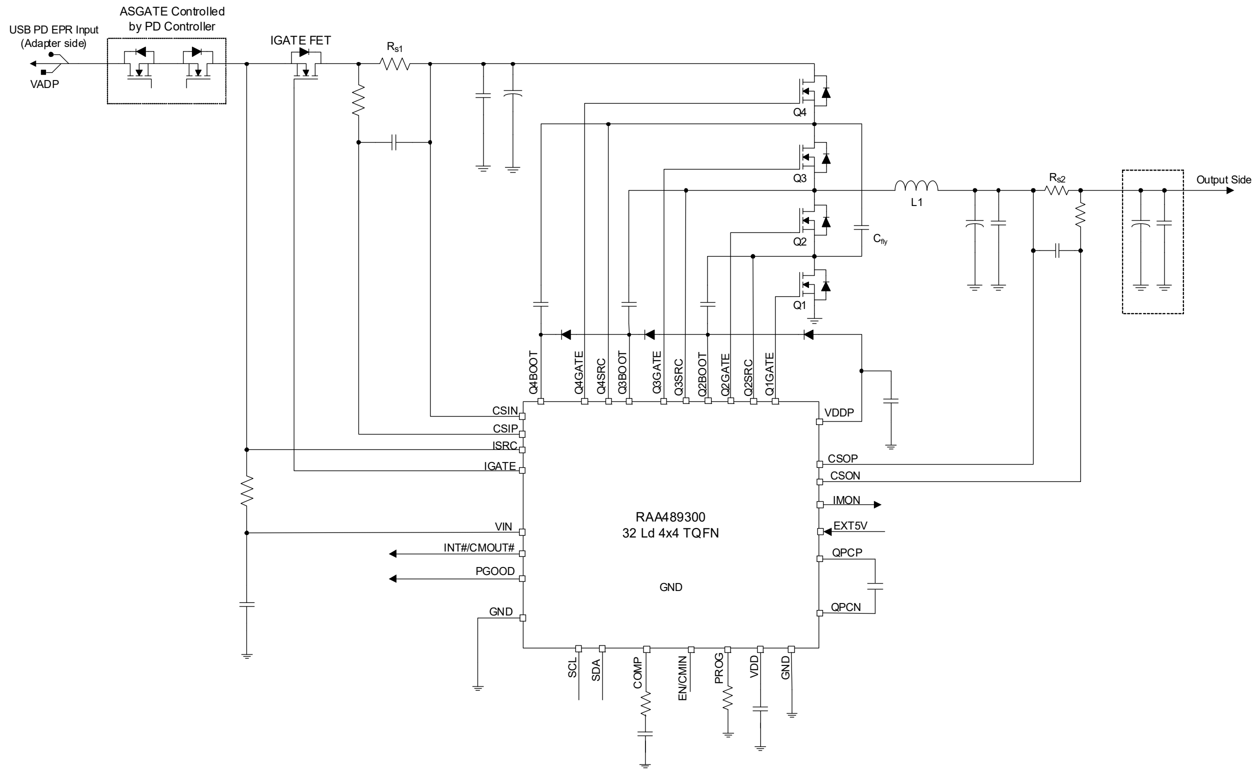


Figure 2. Typical 3-Level Application Circuit – With Isolation FET at Input

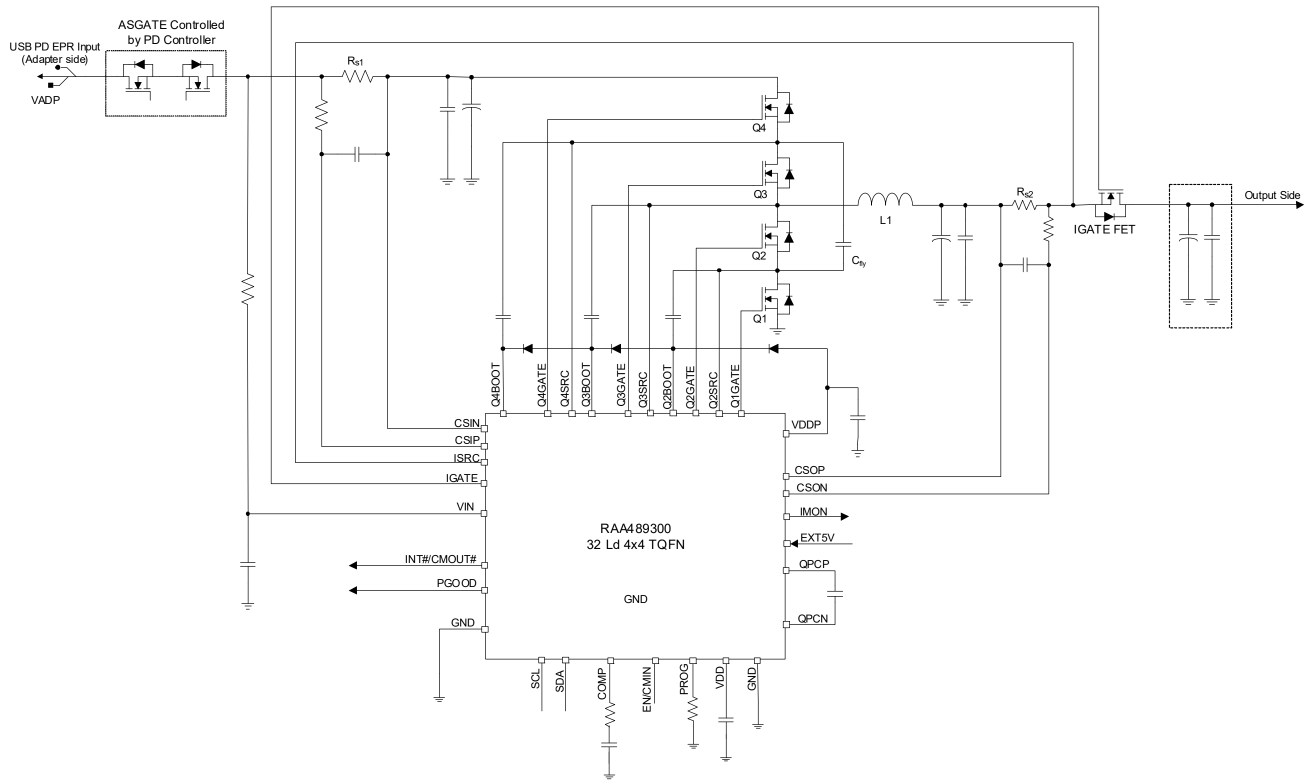


Figure 3. Typical 3-Level Application Circuit – With Isolation FET at Output

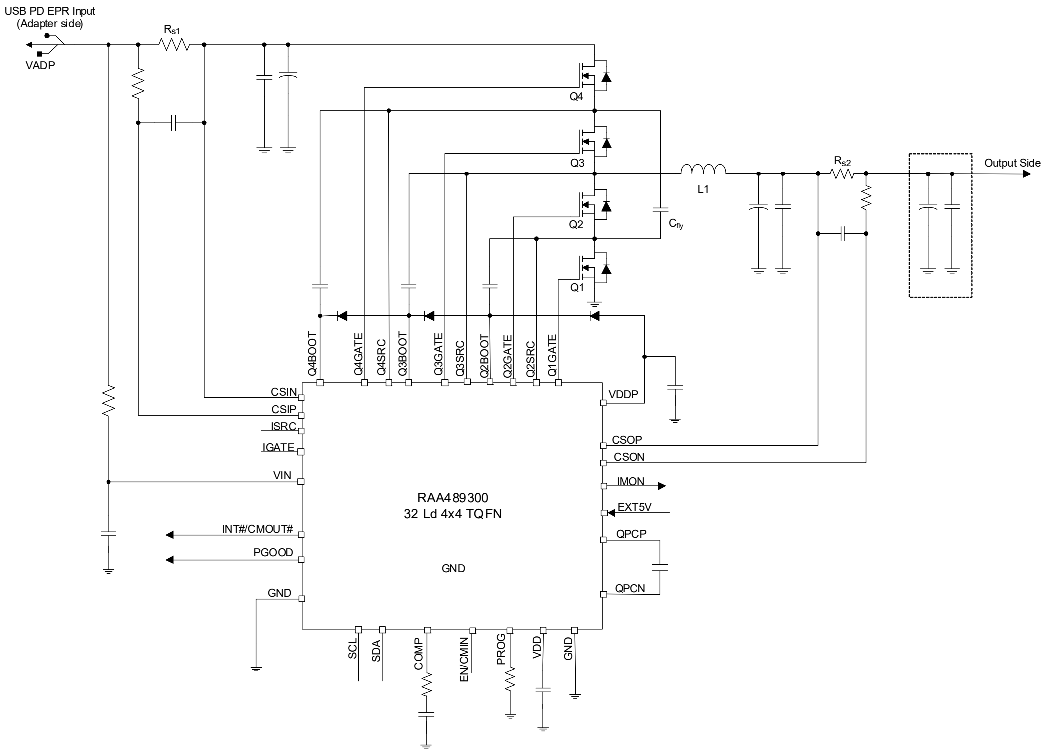


Figure 4. Typical 3-Level Application Circuit – Without Isolation FET

2. Pin Information

2.1 Pin Assignments

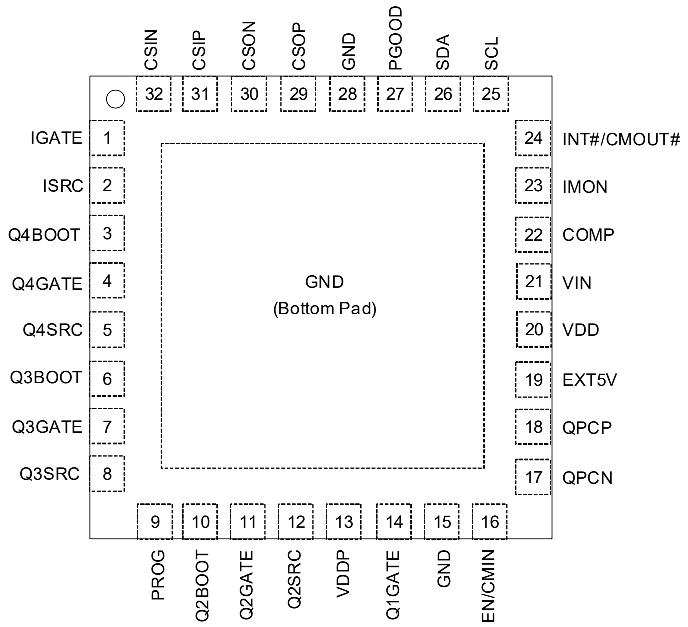


Figure 5. Pin Assignments – Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1	IGATE	Output of the gate driver for an isolation FET (N-Channel). The use of an isolation FET is optional. Leave this pin floating if there is no isolation FET.
2	ISRC	Source terminal of the IGATE FET.
3	Q4BOOT	Q4 MOSFET gate driver supply. Between Q4BOOT and Q4SRC, connect an MLCC that has an effective capacitance of at least 50 times the Cg of the Q4 MOSFET and is not less than 200nF at 10V.
4	Q4GATE	Q4 MOSFET gate driver output.
5	Q4SRC	Current return path for the Q4 MOSFET gate drive. Connect this pin to the node consisting of the Q4 MOSFET source, the Q3 MOSFET drain, and the positive input terminal of flying capacitor.
6	Q3BOOT	Q3 MOSFET gate driver supply. Between Q3BOOT and Q3SRC, connect an MLCC that has an effective capacitance of at least 50 times the Cg of the Q3 MOSFET and is no less than 200nF at 10V.
7	Q3GATE	Q3 MOSFET gate driver output.
8	Q3SRC	Current return path for Q3 MOSFET gate drive. Connect this pin to the node consisting of the Q3 MOSFET source, the Q2 MOSFET drain, and the input terminal of the inductor.
9	PROG	Connect a resistor to GND. Configures default address, default operation, and default input current limit.
10	Q2BOOT	Q2 MOSFET gate driver supply. Between Q2BOOT and Q2SRC, connect an MLCC that has an effective capacitance of at least 50 times the Cg of the Q2 MOSFET, and that is no less than 200nF at 10V.
11	Q2GATE	Q2 MOSFET gate driver output.
12	Q2SRC	Current return path for the Q2 MOSFET gate drive. Connect this pin to the node consisting of the Q2 MOSFET source, the Q1 MOSFET drain, and the negative input terminal of flying capacitor.
13	VDDP	Power supply for the gate drivers. Between VDDP and GND, connect an MLCC that has an effective capacitance of at least 50 times the Cg of the Q1 MOSFET and is no less than 200nF at 10V.
14	Q1GATE	Q1 MOSFET gate driver output.

Pin Number	Pin Name	Description
15	GND	Connect to GND.
16	EN/CMIN	Input pin. It can be configured as enable switching or general-purpose comparator input based on Control0 register Bit[3].
17	QPCN	Internal charge pump capacitor negative input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
18	QPCP	Internal charge pump capacitor positive input. Connect an MLCC capacitor across the QPCP pin and the QPCN pin.
19	EXT5V	Input from external 5V supply or external 5V rail.
20	VDD	Internal LDO output that provides the bias power for the internal analog and digital circuit. Connect an MLCC between VDD and GND. MLCC should have an effective capacitance of 1µF at 5V.
21	VIN	Input voltage sense. The input voltage is valid if the VIN pin voltage is greater than 3.84V when the VIN voltage is rising. The VIN pin can be one of the internal LDO inputs. The LDO provides power to the IC. Connect an MLCC having an effective capacitance of at least 200nF at 48V.
22	COMP	Error amplifier output. Connect a compensation network externally from COMP to GND.
23	IMON	Input or output current monitor output. The default is output current monitor.
24	INT#/CMOUT#	Open-drain output. This output is driven from the active-low interrupt function or the general-purpose comparator. When configured as an interrupt, this pin indicates abnormal events such as WOC, OV, UV, OTP, CFLY UV OV, and others. The interrupt status register must be read to clear the latch.
25	SCL	SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
26	SDA	SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification.
27	PGOOD	Open-drain output. This indicates if the output voltage is within the value set by PGOOD register.
28	GND	Connect to GND.
29	CSOP	Output current sense positive input. Place a 4.7µF MLCC between CSOP and CSON to provide differential mode filtering.
30	CSON	Output current sense negative input. Place a 4.7µF MLCC between CSOP and CSON to provide differential mode filtering.
31	CSIP	Input current sense positive input. Place a 10µF MLCC between CSIP and CSIN to provide differential mode filtering.
32	CSIN	Input current sense negative input. Place a 10µF MLCC between CSIP and CSIN to provide differential mode filtering.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Q4BOOT, Q3BOOT	-0.3	73	V
CSIP, CSIN, CSOP, CSON, ISRC, VIN, Q2BOOT, Q4SRC	-0.3	63	V
Q2SRC, Q3SRC	-1, -3.5 (<10ns)	63	V
CSIP-CSIN, CSOP-CSON	-0.3	0.3	V
VDDP	-0.3	12	V
Q2BOOT-Q2SRC, Q3BOOT-Q3SRC, Q4BOOT-Q4SRC	-0.3	14	V
Q1GATE	GND - 0.3	VDDP + 0.3	V
Q2GATE	Q2SRC - 0.3	Q2BOOT + 0.3	V
Q3GATE	Q3SRC - 0.3	Q3BOOT + 0.3	V
Q4GATE	Q4SRC - 0.3	Q4BOOT + 0.3	V
IGATE-ISRC, VDDP-EXT5V, VDDP-VDD, QPCP-QPCN, VDD, VDD-EXT5V, EXT5V, EN/CMIN, VINOK, INT#/CMOUT#, SCL, SDA, PGOOD	-0.3	6.5	V
QPCP	EXT5V-0.3	VDDP + 0.3	V
QPCN	-0.3	EXT5V + 0.3	V
IMON, COMP, PROG	-0.3	VDD + 0.3	V
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter		Minimum	Maximum	Unit
Ambient Temperature	ARGNP	-10	+100	°C
	A3GNP	-40	+105	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	32 Ld 4x4 TQFN Package	θ_{JA}[1]	Junction to air.	38	°C/W
		θ_{JC}[2]	Junction to case.	2	°C/W

1. θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
UVLO/ACOK						
VIN UVLO Rising	VIN_UVLO_r	-	3.50	3.84	4.20	V
VIN UVLO Hysteresis	VIN_UVLO_h	-	-	240	-	mV
VDD 3P8 Rising	VDD_3P8_r	-	3.45	3.8	4.25	V
VDD 3P8 Hysteresis	VDD_3P8_h	-	-	150	-	mV
EXT5V Rising	EXT5V_r	-	4.30	4.7	4.95	V
EXT5V Hysteresis	EXT5V_h	-	-	400	-	mV
EN Threshold	EN_r	-	0.50	0.7	1.10	V
Bias Current						
VIN Supply Current	I_VIN_SLEEP	EXT5V = 0V, VIN = 5V, SLEEP state	-	25	-	µA
EXT5V Supply Current	I_EXT5V_READY	VIN ≥ 5V, EXT5V = 5V, READY state	-	2.6	-	mA
Forward Supply Current, Enable State	I_EXT5V_ SWITCH	VIN ≥ 5V, EXT5V = 5V, SWITCHING state	-	2.9	-	mA
Linear Regulator						
VDD Output Voltage	VDD	VIN = 6V to 57.6V, EXT5V = 0V	4.7	5	5.6	V
VDD Dropout Voltage	VDD_dp	VIN = 4.5V, I_{VDD} = 10mA	75	130	170	mV
VDD Overcurrent Threshold	VDD_OC_ READY	VIN = 6V, V_{VDD} = 4.0V, READY state	40	100	150	mA
	VDD_OC_ SLEEP	VIN = 6V, V_{VDD} = 4.0V, SLEEP state	18	33	50	mA
Input Current Regulation, Rs1 = 10mΩ						
Input Current Accuracy	CSIx_acc	VCSIP - VCSIN = 60mV (6A), CSIP = 4.5V to 57.6V	-3	-	3	%
		VCSIP - VCSIN = 25mV (2.5A), CSIP = 4.5V to 57.6V	-4	-	4	
		VCSIP - VCSIN = 15mV (1.5A), CSIP = 4.5V to 57.6V	-6	-	6	
		VCSIP - VCSIN = 10mV (1A), CSIP = 4.5V to 57.6V	-9	-	9	
		VCSIP - VCSIN = 5mV (0.5A), CSIP = 4.5V to 57.6V	-15	-	15	
Voltage Regulation						
Output Voltage Accuracy, Forward Mode	VCSOP_acc	20V output case	-1	-	1	%
Input Voltage Regulation Accuracy	VCSIN_acc	Min VIN DAC = 10.034V	-3	-	3	
Output Current Regulation, Rs2 = 5mΩ						
Output Current Accuracy	CSOx_acc	VCSOP- VCSON = 60mV (12A)	-3	-	3	%
		VCSOP- VCSON = 25mV (5A)	-4	-	4	
		VCSOP- VCSON = 15mV (3A)	-9	-	9	
		VCSOP- VCSON = 10mV (2A)	-16	-	16	
		VCSOP- VCSON = 5mV (1A)	-25	-	25	

Limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.

IMON						
Input Current Sense Amplifier, Rs1 = 10mΩ						
Forward IMON_IN Gain	IMON_IN_gain	-	-	36	-	V/V
Forward IMON_IN Accuracy VIMON_IN = IMON_IN gain x (CSIP - CSIN)	IMON_IN_acc	VCSIP - VCSIN = 60mV (6A), CSIP = 5V to 57.6V	-3	-	3	%
		VCSIP - VCSIN = 25mV (2.5A), CSIP = 5V to 57.6V	-6	-	6	
		VCSIP - VCSIN = 15mV (1.5A), CSIP = 5V to 57.6V	-12	-	12	
		VCSIP - VCSIN = 10mV (1A), CSIP = 5V to 57.6V	-20	-	20	
		VCSIP - VCSIN = 5mV (0.5A), CSIP = 5V to 57.6V	-40	-	40	
Output Current Sense Amplifier, Rs2 = 5mΩ						
Forward IMON_OUT Gain	IMON_OUT_gain	-	-	36	-	V/V
IMON_OUT Accuracy VIMON_OUT = IMON_OUT Gain x (VCSOP - VCSON)	IMON_OUT_acc	VCSOP - VCSON = 60mV (12A), VCSON = 20V	-3	-	3	%
		VCSOP - VCSON = 25mV (5A), VCSON = 20V	-6	-	6	
		VCSOP - VCSON = 15mV (3A), VCSON = 20V	-12	-	12	
		VCSOP - VCSON = 10mV (2A), VCSON = 20V	-20	-	20	
		VCSOP - VCSON = 5mV (1A), VCSON = 20V	-40	-	40	
INT#/CMOUT#						
INT#, Input Leakage Current	-	-	-	-	1	µA
INT#, Output Current Sink		VINT# = 0.4V	4	-	-	mA
General-Purpose Comparator						
General-Purpose Comparator Rising Threshold	GPCOMP_r	Reference = 1.2V	1.14	1.2	1.32	V
		Reference = 2V	1.98	2	2.02	V
General-Purpose Comparator Hysteresis	GPCOMP_h	Reference = 1.2V	-	45	-	mV
		Reference = 2V	-	45	-	mV
Protection						
V_{IN} Absolute Overvoltage Rising Threshold	VIN_ABS_OV_r	-	57.1	57.8	58.5	V
V_{IN} Absolute Overvoltage Hysteresis	VIN_ABS_OV_h	-	-	730	-	mV
V_{OUT} Absolute Overvoltage Rising Threshold	VOUT_ABS_OV_r	Control1 register Bit[3:2] = 00	23.4	24	24.6	V
		Control1 register Bit[3:2] = 01	32.9	33.6	34.3	
		Control1 register Bit[3:2] = 10	44.8	45.6	44.4	
		Control1 register Bit[3:2] = 11	56.7	57.6	58.5	
V_{OUT} Absolute Overvoltage Hysteresis	VOUT_ABS_OV_h	-	-	800	-	mV

Limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.

PGOOD Window	FPGOOD_WIN	Control2 register Bit[9:8] = 00 from V_{OUT} DAC	-	5	-	%
		Control2 register Bit[9:8] = 01 from V_{OUT} DAC	-	10	-	
		Control2 register Bit[9:8] = 10 from V_{OUT} DAC	-	15	-	
		Control2 register Bit[9:8] = 11 from V_{OUT} DAC	-	20	-	
PGOOD Window Hysteresis	FPGOOD_ WIN_h	Control2 register Bit[9:8] = 00 from V_{OUT} DAC	-	2.5	-	%
		Control2 register Bit[9:8] = 01 from V_{OUT} DAC	-	5	-	
		Control2 register Bit[9:8] = 10 from V_{OUT} DAC	-	5	-	
		Control2 register Bit[9:8] = 11 from V_{OUT} DAC	-	5	-	
V_{OUT} OK Threshold	VOUT_OK_th	-	-	0.6	-	V
V_{OUT} OK Source Current	VOUT_OK_Isr	-	-	10	-	mA
Input Way Overcurrent Rising Threshold	WOCP_IN_r	Rs1 = 10mΩ, Control1 register Bit[7] = 0	15.6	16.8	18	A
Output Way Overcurrent Rising Threshold	WOCP_OUT_r	Rs2 = 5mΩ. Control1 register Bit[7] = 0	31.2	33.6	36	A
Reverse PTM PGOOD Window[1]	RPGOOD_WIN	Control2 register Bit[9:8] = 00 from Reverse PTM Voltage DAC	-	5	-	%
		Control2 register Bit[9:8] = 01 from Reverse PTM Voltage DAC	-	10	-	
		Control2 register Bit[9:8] = 10 from Reverse PTM Voltage DAC	-	15	-	
		Control2 register Bit[9:8] = 11 from Reverse PTM Voltage DAC	-	20	-	
Reverse PTM PGOOD Hysteresis[1]	RPGOOD_ WIN_h	Control2 register Bit[9:8] = 00 from Reverse PTM Voltage DAC	-	2.5	-	V
		Control2 register Bit[9:8] = 01 from Reverse PTM Voltage DAC	-	5	-	
		Control2 register Bit[9:8] = 10 from Reverse PTM Voltage DAC	-	5	-	
		Control2 register Bit[9:8] = 11 from Reverse PTM Voltage DAC	-	5	-	
CFLY Switching Overvoltage Ratio[1]	VCFLY_OV_ ratio	Control3 Bit[10:9] = 00, VCFLY_OV_ratio = V_{CFLY} / V_{IN} / 2	-	1.5	-	N/A
		Control3 Bit[10:9] = 01 or 11, VCFLY_OV_ratio = V_{CFLY} / V_{IN} / 2	-	1.25	-	
		Control3 Bit[10:9] = 10, VCFLY_OV_ratio = V_{CFLY} / V_{IN} / 2	-	1.125	-	
CFLY Switching Undervoltage Ratio[1]	VCFLY_UV_ ratio	Control3 Bit[10:9] = 00, VCFLY_UV_ratio = V_{CFLY} / V_{IN} / 2	-	0.5	-	N/A
		Control3 Bit[10:9] = 01 or 11, VCFLY_UV_ratio = V_{CFLY} / V_{IN} / 2	-	0.25	-	
		Control3 Bit[10:9] = 10, VCFLY_UV_ratio = V_{CFLY} / V_{IN} / 2	-	0.125	-	
Over-Temperature Threshold	OT_th	-	140	150	160	°C

Limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.

Oscillator						
Oscillator Frequency, Digital Core Only	-	-	0.85	1	1.15	MHz
Digital Debounce Time Accuracy	-	-	-15	-	15	%
Miscellaneous						
Switching Frequency Accuracy	SW_Freq_acc	VCOMP > 1.7V and not in period stretching	-15	-	15	%
CSIN Discharge Current	CSIN_I_dc	Control2 register Bit[13] = 0	-	20	-	mA
CSOP Discharge Current	CSOP_I_dc	Control2 register Bit[12] = 0	-	20	-	mA
Gate Driver						
Q1GATE Pull-Up Resistance	Q1GRPU	10V gate drive at 100mA source current	-	1.275	2.50	Ω
Q1GATE Source Current	Q1GSRC	VQ1BOOT – VQ1GATE = 2.5V	-	2.346	-	A
Q1GATE Pull-Down Resistance	Q1GRPD	10V gate drive at 100mA source current	-	1.029	1.50	Ω
Q1GATE Sink Current	Q1GSNK	VQ1BOOT - VQ1SRC = 2.5V	-	1.692	-	A
Q2GATE Pull-Up Resistance	Q2GRPU	10V gate drive at 100mA source current	-	1.275	2.50	Ω
Q2GATE Source Current	Q2GSRC	VQ2BOOT – VQ2GATE = 2.5V	-	2.346	-	A
Q2GATE Pull-Down Resistance	Q2GRPD	10V gate drive at 100mA source current	-	1.029	1.50	Ω
Q2GATE Sink Current	Q2GSNK	VQ2BOOT – VQ2SRC = 2.5V	-	1.692	-	A
Q3GATE Pull-Up Resistance	Q3GRPU	10V gate drive at 100mA source current	-	1.275	2.50	Ω
Q3GATE Source Current	Q3GSRC	VQ3BOOT – VQ3GATE = 2.5V	-	2.346	-	A
Q3GATE Pull-Down Resistance	Q3GRPD	10V gate drive at 100mA source current	-	1.029	1.50	Ω
Q3GATE Sink Current	Q3GSNK	VQ3BOOT – VQ3SRC = 2.5V	-	1.692	-	A
Q4GATE Pull-Up Resistance	Q4GRPU	10V gate drive at 100mA source current	-	1.275	2.50	Ω
Q4GATE Source Current	Q4GSRC	VQ3BOOT – VQ3GATE = 2.5V	-	2.346	-	A
Q4GATE Pull-Down Resistance	Q4GRPD	10V gate drive at 100mA source current	-	1.029	1.50	Ω
Q4GATE Sink Current	Q4GSNK	VQ3BOOT – VQ3SRC = 2.5V	-	1.692	-	A
Q1GATE1 to Q4GATE1 Dead Time	$t_{Q1GQ4GDEAD}$	-	-	20	-	ns
Q4GATE1 to Q1GATE1 Dead Time	$t_{Q4GQ1GDEAD}$	-	-	20	-	ns
Q2GATE1 to Q3GATE1 Dead Time	$t_{Q2GQ3GDEAD}$	-	-	20	-	ns
Q3GATE1 to Q2GATE1 Dead Time	$t_{Q3GQ2GDEAD}$	-	-	20	-	ns
Charge Pump Gate Drivers						
IGATE Gate Drive Current (Sink)	IG_GD_I_sink	V_{IGATE} - V_{ISRC} = 2V	-	190	-	µA
IGATE Gate Drive Current (Source)	IG_GD_I_src	V_{IGATE} - V_{ISRC} = 2V	-	50	-	µA
SMBus						
SDA/SC Input Low Voltage	-	-	-	-	0.6	V
SDA/SCL Input High Voltage	-	-	1.3	-	-	V
SDA/SCL Input Bias Current	-	-	-	-	1	µA

Limits apply across the junction temperature range, -40°C to +125°C unless otherwise specified.

SDA, Output Sink Current	-	VSDA_B = 0.4V, on	4	-	-	mA
SMBus Frequency	f_{SMB}	-	10	-	400	kHz

1. Limits established by characterization and are not production tested.

3.5 SMBus Timing Specifications

Parameters	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
SMBus Frequency	f_{SMB}	(Supports Standard-Mode and Fast-mode)	10	-	-	kHz
Bus Free Time	t_{BUF}	-	4.7	-	-	µs
Start Condition Hold Time from SCL	$t_{HD:STA}$	-	4	-	-	µs
Start Condition Set-Up Time from SCL	$t_{SU:STA}$	-	4.7	-	-	µs
Stop Condition Set-Up Time from SCL	$t_{SU:STO}$	-	4	-	-	µs
SDA Hold Time from SCL	$t_{HD:DAT}$	-	300	-	-	µs
SDA Set-Up Time from SCL	$t_{SU:DAT}$	-	250	-	-	µs
SCL Low Period	t_{LOW}	For SMBus Standard-mode	4.7	-	-	µs
SCL High Period	t_{HIGH}	For SMBus Standard-mode	4	-	-	µs

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Graphs

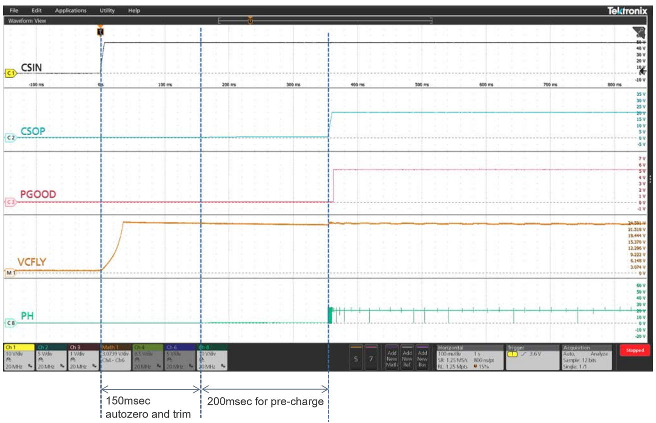


Figure 6. Startup without EXT5V, V_{IN} = 48V, V_{OUT} = 20V, No Load

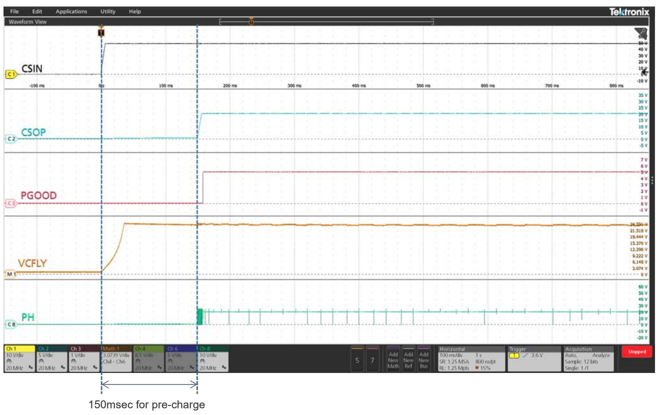


Figure 7. Startup with EXT5V, V_{IN} = 48V, V_{OUT} = 20V, No Load, Control0 Bits[14:13] = 0b01 (Pre-Charge Wait Time = 150ms)

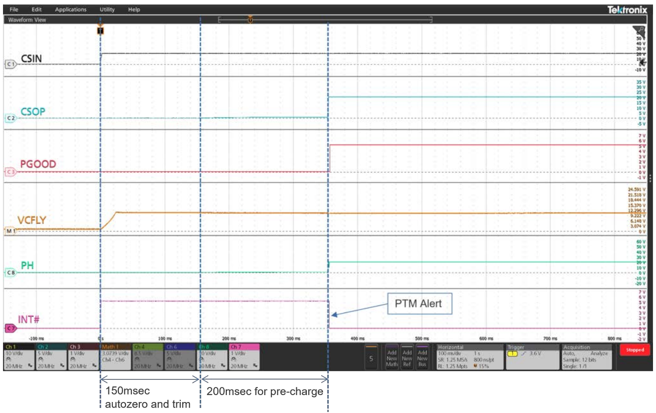


Figure 8. PTM Startup without EXT5V, V_{IN} = 20V, V_{OUT} = 20V, No Load (PROG Pin Resistance = 7.5kΩ)

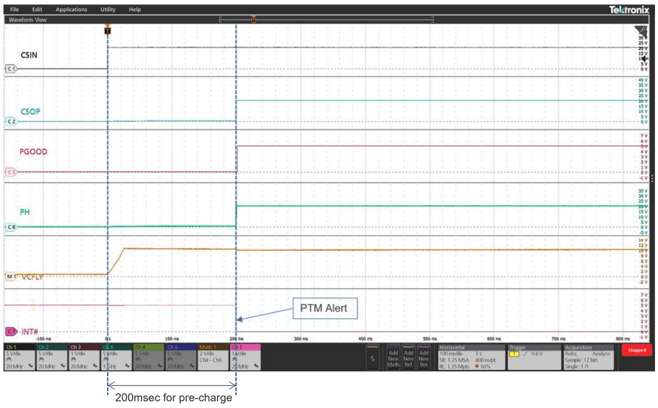


Figure 9. PTM Startup with EXT5V, V_{IN} = 20V, V_{OUT} = 20V, No Load

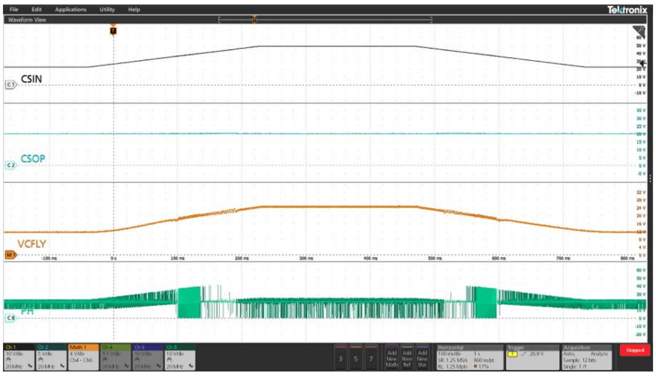


Figure 10. Flying Cap Voltage Regulation During V_{IN} Transition, V_{IN} = 22V to 48V, V_{OUT} = 20V, I_{OUT} = 10mA, V_{IN} slew rate = 0.1mV/µs

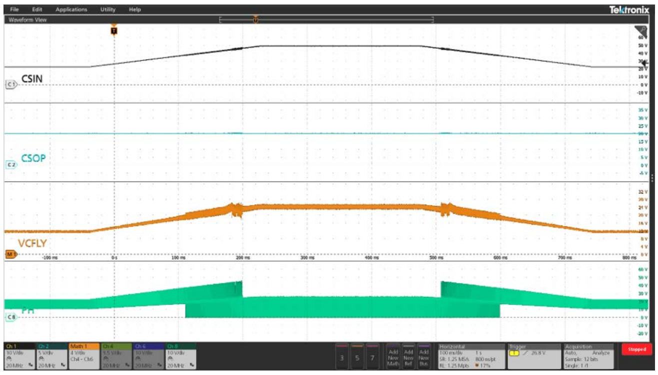


Figure 11. Flying Cap Voltage Regulation During V_{IN} Transition, V_{IN} = 22V to 48V, V_{OUT} = 20V, I_{OUT} = 12A, V_{IN} slew rate = 0.1mV/µs

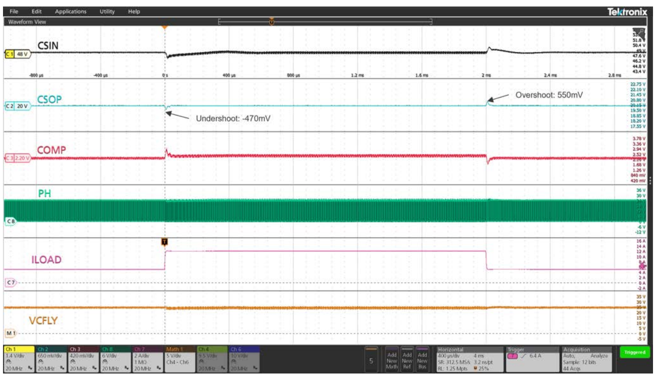


Figure 12. Voltage Regulation During Load Transients, V_{IN} = 48V, V_{OUT} = 20V, I_{OUT} = 5A to 12A (Load Slew = 2.5A/µs, 5A_Time = 12A_Time = 2ms)

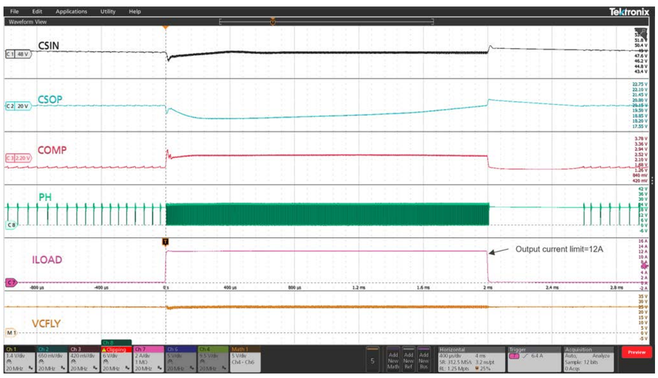


Figure 13. Output Current Regulation During Load Transients, V_{IN} = 48V, V_{OUT} = 20V, I_{OUT} = 0.1A to 12A (Load Slew = 2.5A/µs, 5A_Time = 12A_Time = 2ms, Output Current Limit = 12A)

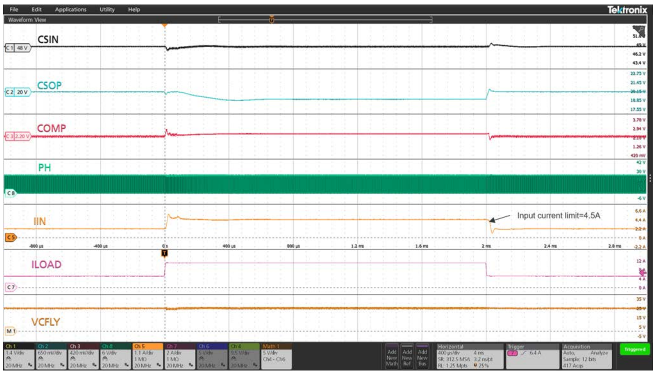


Figure 14. Input Current Regulation During Load Transients, V_{IN} = 48V, V_{OUT} = 20V, I_{OUT} = 5A to 11A (Load Slew = 2.5A/µs, 11A time = 5A time = 2ms, Input Current Limit = 4.5A)

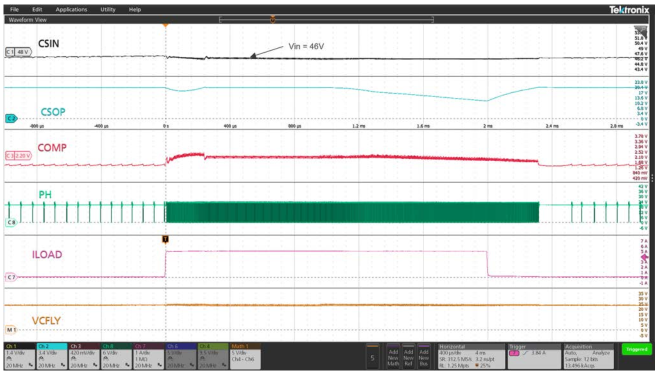


Figure 15. Input Voltage Regulation, V_{IN} = 48V, V_{OUT} = 20V, I_{OUT} = 0.1A to 5A (Load Slew = 2.5A/µs, 0.1A time = 5A time = 2ms, Min Input Voltage Limit = 46.053V, Input Power Supply Current Limit = 1A)

5. General SMBus Architecture

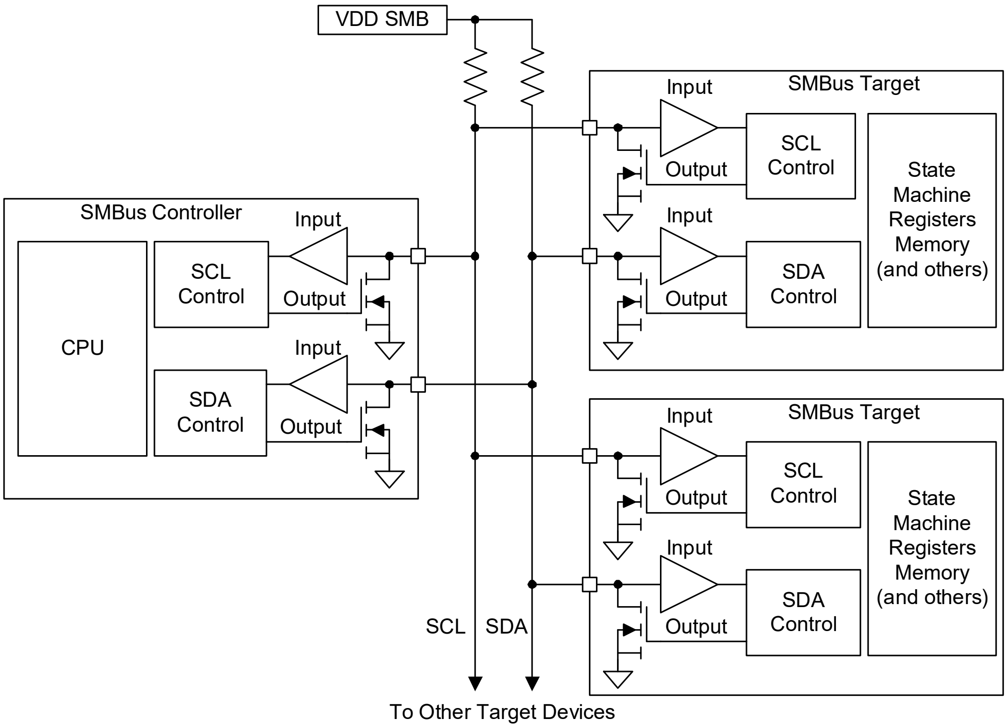


Figure 16. General SMBus

5.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 17.

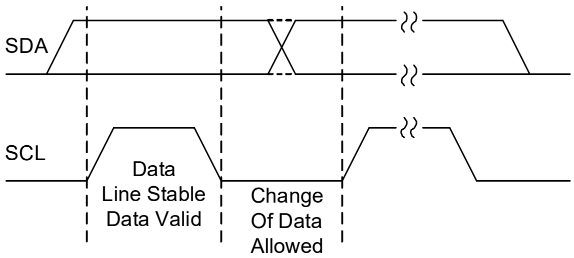


Figure 17. Data Validity

5.2 START and STOP Conditions

Figure 18 shows that the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH.

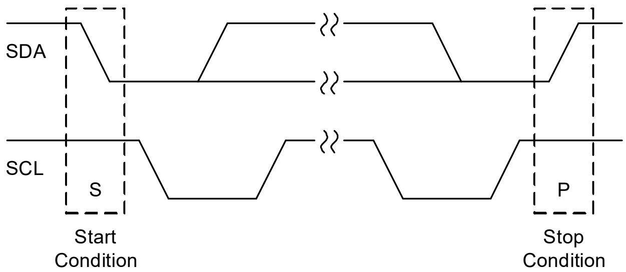


Figure 18. Start and Stop Waveforms

5.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the controller sends seven target address bits and a R/$\overline{\text{W}}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge (see Figure 19). Both the controller and the target use the ACK bit to acknowledge receipt of register addresses and data.

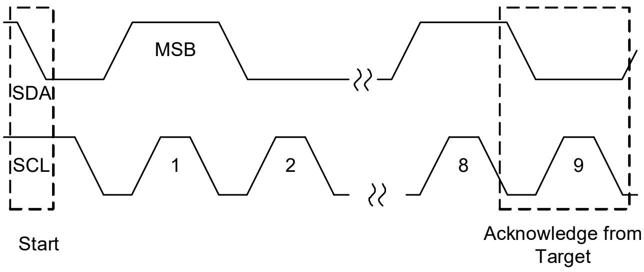


Figure 19. Acknowledge on the SMBus

5.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus controller device. The control byte begins with a Start condition followed by seven bits of target address (0001001) and the R/$\overline{\text{W}}$ bit. The R/$\overline{\text{W}}$ bit is 0 for a WRITE or 1 for a READ. If any target device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no target exists at that address or it is not ready to communicate, the data line is 1 indicating a not acknowledge condition.

After the control byte is sent and the RAA489300 acknowledges it, the second byte sent by the controller must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the RAA489300 which register the controller writes or reads. When the RAA489300 receives a register address byte, it responds with an acknowledge.

5.5 Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO Byte data is transferred before the HI Byte data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

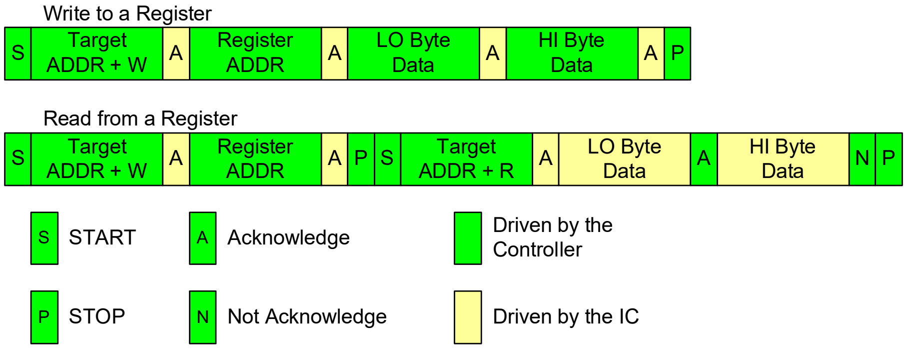


Figure 20. SMBus Read and Write Protocol

5.6 SMBus and I^{2}C Compatibility

The RAA489300 SMBus minimum input logic high voltage is 1.3V, so it is compatible with I^{2}C with pull-up power supplies higher than 1.3V.

The RAA489300 SMBus registers are 16 bits, so it is compatible with 16-bit I^{2}C or 8-bit I^{2}C with auto-increment capability.

6. RAA489300 SMBus Commands

The RAA489300 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification. The RAA489300 uses the SMBus Read-word and Write-word protocols, as shown in Figure 20, to communicate with the host system The RAA489300 is an SMBus target device and does not initiate communication on the bus. The RAA489300 offers two device address options, and the address is selected by programming through the PROG pin resistor. The two 7-bit device addresses are as follows:

Read addresses = 0b10010101(0x95)

Write addresses = 0b10010100(0x94)

Read addresses = 0b10010111(0x97)

Write addresses = 0b10010110(0x96)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The information in this datasheet is based on current sensing resistors Rs1 = 10mΩ and Rs2 = 5mΩ, unless otherwise specified.

The control inputs and control information of the RAA489300 received or provided can be done by writing or reading registers in Table 1 using the Write-word protocol shown in Figure 20.

Table 1. Register Summary

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
Output Current Limit	0x14	R/W	11	[13:3] 11-bit, LSB size 8mA, total range 12156mA with Rs2 = 10mΩ	0x00BC 1500mA
Output Voltage	0x15	R/W	13	[15:3] 13-bit, LSB size 12mV for PPS and 24mV for AVS, total range 24564mV for PPS and 54912mV for AVS	Set by PROG
Control0	0x39	R/W	16	Configures various options. See Table 11.	0x0000
Information1	0x3A	R	16	Indicates various options. See Table 18.	0x0000
Control1	0x3C	R/W	16	Configures various options. See Table 12.	0x0000
Control2	0x3D	R/W	16	Configures various options. See Table 13.	0x0000
Input Current Limit	0x3F	R/W	11	[12:2] 11-bit, LSB size 4mA (default) or 8mA, total range 6078mA (default) or 12156mA	Set by PROG
VINOK Reference	0x40	R/W	8	[15:8] 8-bit, LSB size 257.28mV, total range 46310.4mV	0mV
Control6	0x43	R/W	16	Configures various options. See Table 17.	0x0000
Reverse PTM Voltage[1]	0x49	R/W	12	[15:4] 12-bit, LSB size 12mV, total range 32784mV	0mV
Minimum Input Voltage[2]	0x4B	R/W	8	[15:8] 8-bit, LSB size 257.28mV, total range 46310.4mV	0mV
Control3	0x4C	R/W	16	Configures various options. See Table 14.	0x0000
Information2	0x4D	R	5	Indicates various options. See Table 19.	0x0000
Control4	0x4E	R/W	2	Configures various options. See Table 15.	0x0000
Control5	0x4F	R/W	16	Configures various options. See Table 16.	0x0000
Information3	0x90	R	16	Indicates various options. See Table 20.	0x0000
Information4	0x91	R	16	Indicates various options. See Table 21.	0x0000
Manufacturer ID	0xFE	R	8	Manufacturer ID register – 0x49. Read only	0x0049
Device ID	0xFF	R	8	Device ID register. Read only	0x0017

1. Although the register accepts values up to 32784mV, values should be lower than Absolute Input Overvoltage Threshold.
2. Although the register accepts values up to 46310mV, values should be lower than Absolute Input Overvoltage Threshold.

6.1 Setting Input Current Limit

To set the input current limit, write the 16-bit Input Current Limit register (0x3F) using the Write-word protocol shown in Figure 20.

The RAA489300 limits the input current based on the differential voltage across the CSIP and CSIN pins. The gain of the input current feedback signal can be set by Control1 Bit[7]. With the recommended current sense resistor value Rs1 = 10 mΩ, the LSB of the Input Current Limit register according to Control1 Bit[7] is:

- Control1 Bit[7] = 0 (default): LSB of the Input Current Limit register is 4mA
- Control1 Bit[7] = 1: LSB of the Input Current Limit register is 8mA

The Input Current Limit register accepts any value, but only the valid bits are written to the register. The maximum input current limit, with Rs1 = 10mΩ, is clamped at 6078mA for Control1 Bit[7] = 0 or 12156mA for Control1 Bit[7] = 1.

After POR, the Input Current Limit register is reset to the value programmed through the PROG pin resistor. The Input Current Limit register can be read back to verify its value.

RAA489300 can limit the slew rate of the input current limit by setting Control3 Bit[15]. If Control3 Bit[15] is enabled, the input current limit DAC reference increases by 1LSB per 1µsec.

Table 2 and Table 3 show the data format of the input current limit with Rs1 =10mΩ when Control1 Bit[7] = 0 and Control1 Bit[7] = 1, respectively.

Table 2. Input Current Limit Register 0x3F (11-bit, 4mA Step, 10mΩ Sense Resistor, Control1 Bit[7] = 0)

Bit	Description
[1:0]	Not used
[2]	0 = Add 0mA of input current limit. 1 = Add 4mA of input current limit.
[3]	0 = Add 0mA of input current limit. 1 = Add 8mA of input current limit.
[4]	0 = Add 0mA of input current limit. 1 = Add 16mA of input current limit.
[5]	0 = Add 0mA of input current limit. 1 = Add 32mA of input current limit.
[6]	0 = Add 0mA of input current limit. 1 = Add 64mA of input current limit.
[7]	0 = Add 0mA of input current limit. 1 = Add 128mA of input current limit.
[8]	0 = Add 0mA of input current limit. 1 = Add 256mA of input current limit.
[9]	0 = Add 0mA of input current limit. 1 = Add 512mA of input current limit.
[10]	0 = Add 0mA of input current limit. 1 = Add 1024mA of input current limit.
[11]	0 = Add 0mA of input current limit. 1 = Add 2048mA of input current limit.
[12]	0 = Add 0mA of input current limit. 1 = Add 4096mA of input current limit.
[13:15]	Not used
Maximum	[12:2] = 101 1111 0000: 6078mA

Table 3. Input Current Limit Register 0x3F (11-bit, 8mA Step, 10mΩ Sense Resistor, Control1 Bit[7] = 1)

Bit	Description
[1:0]	Not used
[2]	0 = Add 0mA of input current limit. 1 = Add 8mA of input current limit.
[3]	0 = Add 0mA of input current limit. 1 = Add 16mA of input current limit.
[4]	0 = Add 0mA of input current limit. 1 = Add 32mA of input current limit.
[5]	0 = Add 0mA of input current limit. 1 = Add 64mA of input current limit.
[6]	0 = Add 0mA of input current limit. 1 = Add 128mA of input current limit.
[7]	0 = Add 0mA of input current limit. 1 = Add 256mA of input current limit.
[8]	0 = Add 0mA of input current limit. 1 = Add 512mA of input current limit.
[9]	0 = Add 0mA of input current limit. 1 = Add 1024mA of input current limit.
[10]	0 = Add 0mA of input current limit. 1 = Add 2048mA of input current limit.
[11]	0 = Add 0mA of input current limit. 1 = Add 4096mA of input current limit.
[12]	0 = Add 0mA of input current limit. 1 = Add 8192mA of input current limit.
[13:15]	Not used
Maximum	[13:3] = 10111110000: 12160mA

6.2 Setting Output Current Limit

To set the output current limit, write the 16-bit Output Current Limit register (0x14) using the Write-word protocol shown in Figure 20.

The RAA489300 limits the output current based on the differential voltage across the CSOP and CSON pins. The gain of the output current feedback signal can be set by Control1 Bit[7]. With the recommended current sense resistor value Rs2 = 5 mΩ, the LSB of the Output Current Limit register according to Control1 Bit[7] is:

- Control1 Bit[7] = 0 (default): LSB of the Output Current Limit register = 8mA
- Control1 Bit[7] = 1: LSB of the Output Current Limit register = 16mA

The Output Current Limit register accepts any value, but only the valid bits are written to the register. The maximum output current limit, with Rs2 = 5mΩ, is clamped at 12156mA for Control Bit[7] = 0 or 24311mA for Control Bit[7] = 1.

After POR, the Output Current Limit register is reset to 0x00BC (1.5A). The Output Current Limit register can be read back to verify its value.

Table 4 and Table 5 show the data format of the output current limit, with Rs2 =5mΩ, when Control1 Bit[7] = 0 and 1, respectively.

Table 4. Output Current Limit Register 0x14 (11-bit, 8mA Step, 5mΩ Sense Resistor, Control1 Bit[7] = 0)

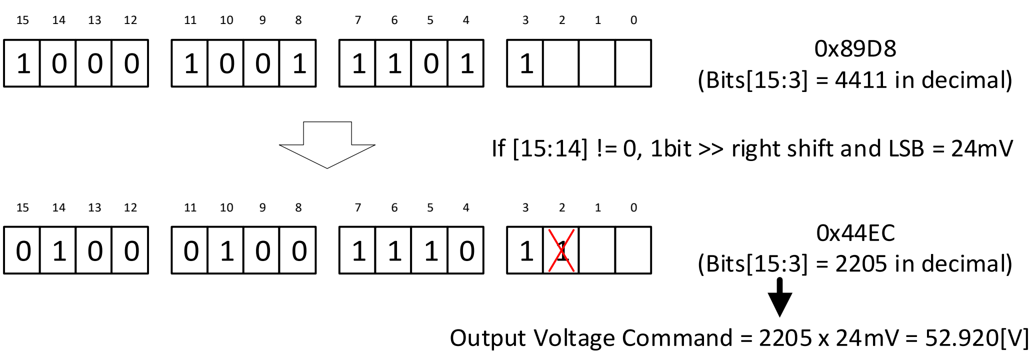
Bit	Description
[2:0]	Not used
[3]	0 = Add 0mA of output current limit. 1 = Add 8mA of output current limit.
[4]	0 = Add 0mA of output current limit. 1 = Add 16mA of output current limit.
[5]	0 = Add 0mA of output current limit. 1 = Add 32mA of output current limit.
[6]	0 = Add 0mA of output current limit. 1 = Add 64mA of output current limit.
[7]	0 = Add 0mA of output current limit. 1 = Add 128mA of output current limit.
[8]	0 = Add 0mA of output current limit. 1 = Add 256mA of charge current limit.
[9]	0 = Add 0mA of output current limit. 1 = Add 512mA of output current limit.
[10]	0 = Add 0mA of output current limit. 1 = Add 1024mA of output current limit.
[11]	0 = Add 0mA of output current limit. 1 = Add 2048mA of output current limit.
[12]	0 = Add 0mA of output current limit. 1 = Add 4096mA of output current limit.
[13]	0 = Add 0mA of output current limit. 1 = Add 8192mA of output current limit.
[14:15]	Not used
Maximum	[13:3] = 10111110000: 12156mA

Table 5. Output Current Limit Register 0x14 (11-bit, 6mA Step, 5mΩ Sense Resistor, Control1 Bit[7] = 1)

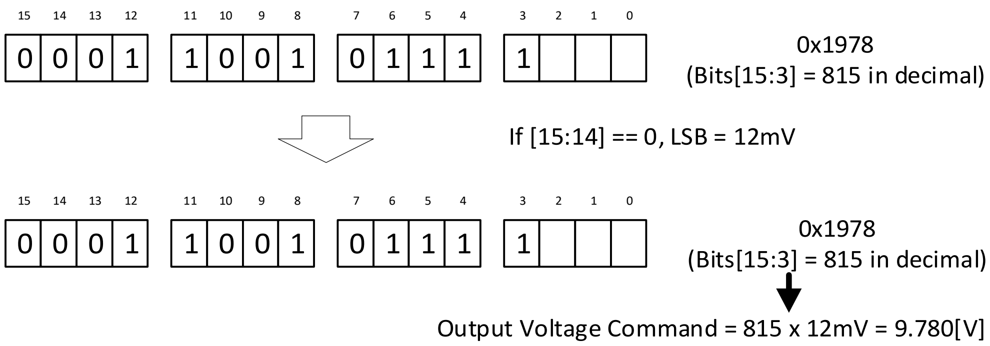
Bit	Description
[2:0]	Not used
[3]	0 = Add 0mA of output current limit. 1 = Add 16mA of output current limit.
[4]	0 = Add 0mA of output current limit. 1 = Add 32mA of output current limit.
[5]	0 = Add 0mA of output current limit. 1 = Add 64mA of output current limit.
[6]	0 = Add 0mA of output current limit. 1 = Add 128mA of output current limit.
[7]	0 = Add 0mA of output current limit. 1 = Add 256mA of output current limit.
[8]	0 = Add 0mA of output current limit. 1 = Add 512mA of output current limit.
[9]	0 = Add 0mA of output current limit. 1 = Add 1024mA of output current limit.
[10]	0 = Add 0mA of output current limit. 1 = Add 2048mA of output current limit.
[11]	0 = Add 0mA of output current limit. 1 = Add 4096mA of output current limit.
[12]	0 = Add 0mA of output current limit. 1 = Add 8192mA of output current limit.
[13]	0 = Add 0mA of output current limit. 1 = Add 16384mA of output current limit.
[14:15]	Not used
Maximum	[13:3] = 10111110000: 24320mA

6.3 Setting Output Voltage

To set the regulated output voltage, write a 16-bit value to the Output Voltage register (0x15) using the Write-word protocol shown in Figure 20. Thirteen bits, [15:3], are allocated for the Output Voltage register. The RAA489300 supports Programmable Power Supply (PPS) and Adjustable Voltage Supply (AVS) modes. The RAA489300 can be configured to regulate the output voltage in PPS mode or AVS mode based on Bits[15:14] of the Output Voltage register. If those bits are 0, PPS mode is engaged and, otherwise, AVS mode is engaged. When supporting PPS mode, 11 bits are used and the LSB is 12mV. When AVS is supported, 12 bits are used and the LSB is 24mV. For example, when a user writes 0x89D8 (4411 in decimal) to the Output Voltage register, the Output Voltage register value is expressed as follows and AVS is supported:



However, when a user writes 0x1978 (815 in decimal) to the Output Voltage register, the Output Voltage register value is expressed as follows and PPS is supported:



RAA489300 can apply the slew rate to the output voltage DAC reference by setting Control3 Bit[14]. When Control3 Bit[14] is enabled, the slew rate is limited to 3mV/µs or 0.75mV/µs, as selected according to the Control3 Bit[13] value (see Table 14).

Table 6 and Table 7 show the data format of the Output Voltage register in PPS mode and AVS mode, respectively.

Table 6. Output Voltage Command Register 0x15 in PPS mode (13-bit, 12mV Step) – Bits[15:14] = 0

Bit	Description
[2:0]	Not used
[3]	0 = Add 0mV of output voltage. 1 = Add 12mV of output voltage.
[4]	0 = Add 0mV of output voltage. 1 = Add 24mV of output voltage.
[5]	0 = Add 0mV of output voltage. 1 = Add 48mV of output voltage.
[6]	0 = Add 0mV of output voltage. 1 = Add 96mV of output voltage.
[7]	0 = Add 0mV of output voltage. 1 = Add 192mV of output voltage.
[8]	0 = Add 0mV of output voltage. 1 = Add 384mV of output voltage.
[9]	0 = Add 0mV of output voltage. 1 = Add 768mV of output voltage.
[10]	0 = Add 0mV of output voltage. 1 = Add 1536mV of output voltage.
[11]	0 = Add 0mV of output voltage. 1 = Add 3072mV of output voltage.
[12]	0 = Add 0mV of output voltage. 1 = Add 6144mV of output voltage.
[13]	0 = Add 0mV of output voltage. 1 = Add 12288mV of output voltage.
[14]	0 = Add 0mV of output voltage.
[15]	0 = Add 0mV of output voltage.
Maximum	[15:3] = 0011111111111: 24564mV

Table 7. Output Voltage Command Register 0x15 in AVS mode (13-Bit, 24mV Step) – Bits[15:14] = nonzero

Bit	Description
[2:0]	Not used
[3]	0 = Add 0mV of output voltage. (no impact)
[4]	0 = Add 0mV of output voltage. 1 = Add 24mV of output voltage.
[5]	0 = Add 0mV of output voltage. 1 = Add 48mV of output voltage.
[6]	0 = Add 0mV of output voltage. 1 = Add 96mV of output voltage.
[7]	0 = Add 0mV of output voltage. 1 = Add 192mV of output voltage.
[8]	0 = Add 0mV of output voltage. 1 = Add 384mV of output voltage.
[9]	0 = Add 0mV of output voltage. 1 = Add 768mV of output voltage.
[10]	0 = Add 0mV of output voltage. 1 = Add 1536mV of output voltage.
[11]	0 = Add 0mV of output voltage. 1 = Add 3072mV of output voltage.
[12]	0 = Add 0mV of output voltage. 1 = Add 6144mV of output voltage.
[13]	0 = Add 0mV of output voltage. 1 = Add 12288mV of output voltage.
[14]	0 = Add 0mV of output voltage. 1 = Add 24576mV of output voltage.
[15]	0 = Add 0mV of output voltage. 1 = Add 49152mV of output voltage.
Maximum	[15:3] = 1000111100000: 54912mV

6.4 Setting VINOK Reference

RAA489300 starts switching when the input voltage is higher than the voltage setting of the VINOK Reference register. To set the VINOK reference, write a 16-bit value to the VINOK Reference register (0x40) using the Write-word protocol shown in Figure 20.

Table 8. VINOK Reference Register 0x40 (8-bit, 257.28mV Step)

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mV of VINOK reference. 1 = Add 257.28mV of VINOK reference.
[9]	0 = Add 0mV of VINOK reference. 1 = Add 514.56mV of VINOK reference.
[10]	0 = Add 0mV of VINOK reference. 1 = Add 1029.12mV of VINOK reference.
[11]	0 = Add 0mV of VINOK reference. 1 = Add 2058.24mV of VINOK reference.
[12]	0 = Add 0mV of VINOK reference. 1 = Add 4116.48mV of VINOK reference.
[13]	0 = Add 0mV of VINOK reference. 1 = Add 8232.96mV of VINOK reference.
[14]	0 = Add 0mV of VINOK reference. 1 = Add 16465.92mV of VINOK reference.
[15]	0 = Add 0mV of VINOK reference. 1 = Add 32931.84mV of VINOK reference.
Maximum	[15:8] = 10110100: 46310.4 mV

6.5 Setting Minimum Input Voltage

The Minimum Input Voltage register (0x4B) contains an SMBus readable and writable minimum input voltage. The default is 3.8592V. This register accepts any value, but only the valid register bits are written. The maximum value is clamped at 46.3104V.

Table 9. Minimum Input Voltage Register 0x4B (11-bit, 257.29mV Step)

Bit	Description
[7:0]	Not used
[8]	0 = Add 0mV of minimum input voltage. 1 = Add 257.28mV of minimum input voltage.
[9]	0 = Add 0mv of minimum input voltage. 1 = Add 514.56mV of minimum input voltage.
[10]	0 = Add 0mV of minimum input voltage. 1 = Add 1029.12mV of minimum input voltage.
[11]	0 = Add 0mV of minimum input voltage. 1 = Add 2058.24mV of minimum input voltage.
[12]	0 = Add 0mV of minimum input voltage. 1 = Add 4116.48mV of minimum input voltage.
[13]	0 = Add 0mV of minimum input voltage. 1 = Add 8232.96mV of minimum input voltage.
[14]	0 = Add 0mV of minimum input voltage. 1 = Add 16465.92mV of minimum input voltage.
[15]	0 = Add 0mV of minimum input voltage. 1 = Add 32931.84mV of minimum input voltage.
Maximum	[15:8] = 10110100: 46310.4mV

6.6 Setting Reverse PTM Voltage

RAA489300 provides Reverse Pass-Through Mode (PTM). To switch to Reverse PTM, the CSOP voltage must be matched with the reverse PTM voltage reference. To set the reverse PTM voltage reference, write a 16-bit value to the Reverse PTM Voltage register (0x49) using the Write-word protocol shown in Figure 20.

Table 10. Reverse PTM Voltage Register 0x49 (12-bit, 12mA Step)

Bit	Description
[3:0]	Not used
[4]	0 = Add 0mV of reverse PTM voltage. 1 = Add 12mV of reverse PTM voltage.
[5]	0 = Add 0mV of reverse PTM voltage. 1 = Add 24mV of reverse PTM voltage.
[6]	0 = Add 0mV of reverse PTM voltage. 1 = Add 48mV of reverse PTM voltage.
[7]	0 = Add 0mV of reverse PTM voltage. 1 = Add 96mV of reverse PTM voltage.
[8]	0 = Add 0mV of reverse PTM voltage. 1 = Add 192mV of reverse PTM voltage.
[9]	0 = Add 0mV of reverse PTM voltage. 1 = Add 384mV of reverse PTM voltage.
[10]	0 = Add 0mV of reverse PTM voltage. 1 = Add 768mV of reverse PTM voltage.
[11]	0 = Add 0mV of reverse PTM voltage. 1 = Add 1536mV of reverse PTM voltage.
[12]	0 = Add 0mV of reverse PTM voltage. 1 = Add 3072mV of reverse PTM voltage.
[13]	0 = Add 0mV of reverse PTM voltage. 1 = Add 6144mV of reverse PTM voltage.
[14]	0 = Add 0mV of reverse PTM voltage. 1 = Add 12288mV of reverse PTM voltage.
[15]	0 = Add 0mV of reverse PTM voltage. 1 = Add 24576mV of reverse PTM voltage.
Maximum	[15:4] = 101010101100: 32784mV

6.7 Control Registers

The Control0, Control1, Control2, Control3, Control4, Control5 and Control6 registers configure the RAA489300 operation. To change certain functions or options after VDD 2.7V POR, write a 16-bit control command to the Control0 register (0x39), Control1 register (0x3C), Control2 register (0x3D), Control3 register (0x4C), Control4 register (0x4E), Control5 register (0x4F) and/or Control6 register (0x43) using the Write-word protocol shown in Figure 20 and the data format shown in the tables from Table 11 to Table 15, respectively.

Table 11. Control0 Register 0x39

Bit	Bit Name	Description
[15]	Digital Reset	Bit[15] resets all SMBus register values to the POR default value. 0 = Idle (default) 1 = Reset
[14:13]	Pre-Charge Wait	Bits[14:13] configure the Pre-charging state waiting time. 00 = 200ms (default) 01 = 150ms 10 = 100ms 11 = 50ms
[12:11]	Alert Debounce	Bits[12:11] configure the debounce time for ALERT# assertion. 00 = 2µs (default) 01 = 12µs 10 = 720µs 11 = 2ms
[10:9]	Output Current Alert Threshold	Bits[10:9] configure the Output Current alert threshold. 00 = 97.5% (default) 01 = 95% 10 = 92.5% 11 = 100%
[8]	Current Alert Integration Time	Bit[8] configures Current Alert Integration time. 0 = 250ms (default) 1 = 500ms
[7]	PTM Entry Timeout	Bit[7] configures PTM Entry Timeout. 0 = Disable (default) 1 = Enable
[6]	General-Purpose Comparator output (CMOUT) Latch	Bit[6] enables or disables the latch of the General-Purpose Comparator. 0 = Enable (default) 1 = Disable
[5]	General-Purpose Comparator Input (CMIN) Reference	Bit[5] configures CMIN pin Reference of the General-Purpose Comparator. 0 = 1.2V (default) 1 = 2.0V
[4]	General-Purpose Comparator output CMOUT polarity	Bit[4] configures CMOUT pin polarity for the General-Purpose Comparator. 0 = Non-inverted (default) 1 = Inverted
[3]	General-Purpose Comparator	Bit[3] enables or disables the General-Purpose Comparator output. 0 = Disable (default) 1 = Enable
[2]	Forward/Reverse PTM Operation	Bit[2] configures Forward/Reverse PTM Operation. 0 = Forward (default) 1 = Reverse
[1]	Pass-Through Mode	Bit[1] enables or disables the Pass-Through Mode. 0 = Disable (default) 1 = Enable
[0]	Enable Bit	Bit[0] enables or disables the 3L buck converter switching. 0 = Sleep/Switching following EN pin status (default) 1 = Enable Switching

Table 12. Control1 Register 0x3C

Bit	Bit Name	Description
[15:12]	High-Side Phase Comparator Offset	Bits[15:12] adjust the High side phase comparator threshold offset. 0000 = 0mV (default) 0001 = -1mV 1000 = +8mV 0010 = -2mV 1001 = +7mV 0011 = -3mV 1010 = +6mV 0100 = -4mV 1011 = +5mV 0101 = -5mV 1100 = +4mV 0110 = -6mV 1101 = +3mV 0111 = -7mV 1110 = +2mV 1110 = +2mV 1111 = +1mV
[11:10]	Boot QP Frequency	Bits[11:10] configure Boot Charge Pump (QP) clock frequency. 00 = 20MHz (default) 01 = 10MHz 10 = 5MHz 11: Force Disable Boot QP independent of Power State Machine
[9:8]	Relative Output Overvoltage Interrupt Debounce Time	Bits[9:8] configure debounce time only for output overvoltage. 00 = 12µs (default) 01 = 2µs 10 = 720µs 11 = 2ms
[7]	Current Feedback Gain	Bit[7] configures current feedback gain of the input current sensing and output current sensing. 0 = 1x (default) 1 = 0.5x
[6]	IMON Gain	Bit[6] configures IMON gain. 0 = 1x (default) 1 = 4x
[5]	IMON Select	Bit[5] selects IMON sensing point. 0 = Output current (default) 1 = Input current
[4]	V_{OUT}/Reverse PTM Absolute Undervoltage Threshold	Bit[4] configures Absolute Undervoltage threshold of V_{OUT} or Reverse Pass-Through Mode voltage. 0 = 1.6V (default) 1 = 3.2V
[3:2]	V_{OUT} Absolute Overvoltage Threshold	Bits[3:2] configure Vout absolute overvoltage threshold. 00 = 24V (default) 01 = 33.6V 10 = 45.6V 11 = 57.6V
[1:0]	Dither	Bits[1:0] configure the dither function. 00 = Disable (default) 01 = 102% 10 = 104% 11 = 106%

Table 13. Control2 Register 0x3D

Bit	Bit Name	Description
[15]	CSIN Discharge	Bit[15] enables or disables the forced CSIN Discharge. 0 = Disable (default) 1 = Enable
[14]	CSOP Discharge	Bit[14] enables or disables the forced CSOP Discharge. 0 = Disable (default) 1 = Enable
[13]	CSIN and CSOP Discharge Current	Bit[13] configures the CSIN and CSOP Discharge current. 0 = 20mA (default) 1 = 30mA
[12]	Low Power PTM mode	Bit[12] enables or disables the Low Power PTM mode. 0 = Disable (default) 1 = Enable
[11]	CSIN and CSOP Auto Discharge	Bit[11] enables or disables the CSIN and CSOP Auto Discharge. 0 = Disable (default) 1 = Enable
[10]	CSOP Auto Discharge with V_{OUT} DAC Change	Bit[10] enables or disables CSOP Auto Discharge when DAC value is changed. 0 = Enable (default) 1 = Disable
[9:8]	PGOOD Window	Bits[9:8] configure the PGOOD window. Relative Undervoltage and Overvoltage follow the PGOOD window thresholds. 00 = 5% 01 = 10% 10 = 15% 11 = 20% (default)
[7]	CFLY Pre-Charge Function	Bit[7] enables or disables the CFLY Pre-Charge function. 0 = Disable (default) 1 = Enable
[6]	CFLY Startup Power Mode	Bit[6] configures the CFLY Startup power mode. 0 = CFLY Startup in high power mode (default). 1 = CFLY Startup in low power mode.
[5]	Idle Period in CFLY Low Power Mode	Bit[5] configures the Idle Period in CFLY low power mode. 0 = 1950us (default) 1= 7710us
[4]	Fault Retry Timer	Bit[4] configures the Fault Retry Timer. 0 = 1.3s (default) 1 = 150ms
[3]	Forced Latch-off on Fault	Bit[3] configures the Forced Latch-off on Fault. 0 = Follow Individual Fault Retry/Latch-Off Settings (default) 1 = Enable Force Latch-off on Fault
[2:1]	VDDP Charge Pump Ratio with EXT5V	Bits[2:1] configure the VDDP Charge Pump Ratio with EXT5V. 00 = 1:2 (default) 01 = 1:1 10 = Auto mode 11 = Auto mode
[0]	Reload Input Current Limit on Fault Retry	Bit[0] configures reloading the Input Current Limit on Fault Retry 0 = Enable (default) 1 = Disable

Table 14. Control3 Register 0x4C

Bit	Bit Name	Description
[15]	Current Slew Rate Control	Bit[15] enables or disables the input current limit slew rate control. 0 = Disable (default) 1 = Enable
[14]	Voltage Slew Rate Control	Bit[14] enables or disables the output voltage slew rate control. 0 = Enable (default) 1 = Disable
[13]	Voltage Slew Rate Select	Bit[13] configures voltage slew rate ratio. 0 = 1x (default) 1 = 0.25x
[12]	USB Arcing Prevention	Bit[12] enables or disables the USB arcing prevention. 0 = Disable (default) 1 = Enable
[11]	Enable IGATE Charge Pump to 100%	Bit[11] enables or disables the IGATE charge pump to 100%. 0 = Disable (default) 1 = Enable the IGATE charge pump 100% of the time
[10:9]	Modulator CFLY OV UV Thresholds	Bit[10:9] configures the Modulator CFLY OV UV thresholds. 00 = ±50% (default) 01 = ±25% 10 = ±12.5% 11 = ±25% (disable Nonlinear CFLY OV UV balancer)
[8]	ADC Voltage Measurement Range	Bit[8] configures ADC voltage measurement range. 0 = Normal (default) 1 = High Range
[7:6]	IGATE Control	Bits[7:6] configure the IGATE behavior. 00 = Auto (default) 01 = IGATE Force ON 10 = IGATE Force OFF 11 = Tri-State IGATE
[5]	IGATE Turn ON Timing in Auto mode	Bit[5] configures the IGATE turn ON timing in auto mode. 0 = Within PGOOD Window (default) 1 = When switching starts / Entering the Pass-Through Mode
[4]	PGOOD control	Bit[4] enables or disables the PGOOD pin. 0 = Enable (default) 1 = Disable
[3:2]	Switching Frequency	Bits[3:2] configure switching frequency. 00 = 300 kHz (default) 01 = 400 kHz 10 = 200 kHz 11 = 250 kHz
[1]	Exit Pass-Through Mode with Current Alert	Bit[1] enables or disables the Pass-Through Mode with Current Alert. 0 = Disable (default) 1 = Enable
[0]	Enable ADC	Bit[0] enables or disables the ADC. 0 = ADC OFF (default) 1 = ADC ON

Table 15. Control4 Register 0x4E

Bit	Bit Name	Description
[15]	Reserved	Reserved
[14]	CFLY Balance Gain	Bit[14] configures CFLY balancer gain. 0 = 1X gain (default) 1 = 4X gain
[13:12]	High-Side Phase Comparator Blanking Time	Bits[13:12] configure High-side Phase Comparator Blanking time. 00 = 128ns (default) 01 = 72ns 10 = 53ns 11 = 43ns
[11]	High-Side Phase Comparator Filter	Bit[11] configures High-side Phase Comparator Filter. 00 = High filtering (default) 10 = Low filtering
[10]	Output Short-Circuit Check	Bit[10] enables or disables the output short-circuit check before moving to SWITCHING state. 0 = Enable (default) 1 = Disable
[9:8]	Low-Side Phase Comparator Blanking Time	Bits[9:8] configure Low-side Phase Comparator Blanking time. 00 = 40ns (default) 01 = 80ns 10 = 120ns 11 = 160ns
[7:6]	Low-Side Phase Comparator Filter Bandwidth	Bits[7:6] configure Low-side Phase Comparator Filter Bandwidth. 00 = 15.4MHz (default) 01 = 7.3MHz 10 = 4.3MHz 11 = 3.2MHz
[5]	Disable Boot QP in Modulator OFF state	Bit[5] enables or disables Boot QP in Modulator OFF state when the part is in SWITCHING state. 0 = Enable Boot QP in Modulator OFF state (default) 1 = Disable Boot QP in Modulator OFF state
[4:2]	Low-Side Phase Comparator Offset Control	Bits[4:2] configure Low-side Phase Comparator offset. 000 = 0mV (default) 001 = +1.1mV 010 = +2.2mV 011 = +3.3mV 100 = -4.3mV 101 = -3.3mV 110 = -2.2mV 111 = -1.1mV
[1]	VINOK Interrupt Trigger Polarity	Bit[1] configures the INT#/CMOUT# pin trigger polarity for the VINOK Interrupt. 0 = VIN falling (default) 1 = VIN rising
[0]	PGOOD Status in SLEEP State	Bit[0] configures the PGOOD status in SLEEP state. 0 = PGOOD is low in SLEEP state (default) 1 = PGOOD is high in SLEEP state

Table 16. Control5 Register 0x4F

Bit	Bit Name	Description
[15]	Over-Temperature Fault	Bit[15] enables or disables the Over-temperature Fault. 0 = Enable Over-temperature Fault (default) 1 = Disable Over-temperature Fault (Alert# pin assertion only)
[14]	Way Overcurrent Fault	Bit[14] enables or disables the Way Overcurrent Fault. 0 = Enable Way Overcurrent Fault (default) 1 = Disable Way Overcurrent Fault
[13]	Absolute Output Undervoltage Fault	Bit[13] enables or disables the Absolute Output Undervoltage Fault. 0 = Enable Absolute Output UV Fault (default) 1 = Disable Absolute Output UV Fault
[12]	Reverse PTM UV OV Fault	Bit[12] enables or disables the reverse Pass-Through Mode Undervoltage and Overvoltage Fault. 0 = Enable Reverse Pass-Through Mode UV OV Fault (default) 1 = Disable Reverse Pass-Through Mode UV OV Fault
[11]	CFLY UV OV Fault	Bit[11] enables or disables CFLY Undervoltage and Overvoltage Fault. 0 = Enable CFLY undervoltage and overvoltage Fault (default) 1 = Disable CFLY undervoltage and overvoltage Fault
[10]	Absolute Output OV Interrupt	Bit[10] enables or disables the Absolute Output Overvoltage Interrupt. 0 = Enable Absolute Output OV protection (default) 1 = Disable Absolute Output OV protection
[9]	Absolute Input OV Interrupt	Bit[9] enables or disables the Absolute Input Overvoltage Interrupt. 0 = Enable Absolute Input OV protection (default) 1 = Disable Absolute Input OV protection
[8]	Relative Output OV Interrupt	Bit[8] enables or disables the Relative Output Overvoltage Interrupt. 0 = Enable Relative Output OV protection (default) 1 = Disable Relative Output OV protection
[7]	VINOK Interrupt	Bit[7] enables or disables the VINOK Reference Interrupt. 0 = Enable VINOK Reference Check (default) 1 = Disable VINOK Reference Check
[6]	Output Current Alert	Bit[6] enables or disables the Output Current Alert. 0 = Enable Output current Alert (default) 1 = Disable Output current Alert
[5]	Input Current Alert	Bit[5] enables or disables the Input Current Alert. 0 = Enable Input current Alert (default) 1 = Disable Input current Alert
[4]	Minimum Input Voltage Loop Alert	Bit[4] enables or disables the Minimum Input Voltage Loop Alert. 0 = Enable Minimum Input Voltage Loop Alert (default) 1 = Disable Minimum Input Voltage Loop Alert
[3]	Ready Alert	Bit[3] enables or disables the Ready Alert. 0 = Enable READY state enter Alert (default) 1 = Disable READY state enter Alert
[2]	Relative Output Undervoltage Alert	Bit[2] enables or disables the Relative Output Undervoltage Alert. 0 = Enable Relative Output UV Alert (default) 1 = Disable Relative Output UV Alert
[1]	Pass-Through Mode Alert	Bit[1] enables or disables the Pass-Through Mode Alert. 0 = Enable PTM Alert (default) 1 = Disable PTM Alert
[0]	General-Purpose Comparator Alert	Bit[0] enables or disables the General-Purpose Comparator Alert. 0 = Enable GP Comparator Alert (default) 1 = Disable GP Comparator Alert

Table 17. Control6 Register 0x43

Bit	Bit Name	Description
[15]	Over-Temperature Fault	Bit[15] configures the Over-temperature Fault latch. 0 = Retry on fault (default) 1 = Latch-off on fault
[14]	Way Overcurrent Fault	Bit[14] configures the Way Overcurrent Fault latch. 0 = Retry on fault (default) 1 = Latch-off on fault
[13]	Absolute Output Undervoltage Fault	Bit[13] configures the Absolute Output Undervoltage Fault latch. 0 = Retry on fault (default) 1 = Latch-off on fault
[12]	Reverse PTM UV OV Fault	Bit[12] configure the reverse Pass-Through Mode Undervoltage and Overvoltage Fault latch. 0 = Wait on fault (default) 1 = Latch-off on fault
[11]	CFLY UV OV Fault	Bit[11] configures the CFLY UV OV Fault latch. 0 = Retry on fault (default) 1 = Latch-off on fault
[10]	Absolute Output OV Interrupt	Bit[10] enables or disables INT# pin assertion for the Absolute Output OV Interrupt. 0 = Enable Absolute Output OV INT# (default) 1 = Disable Absolute Output OV INT#
[9]	Absolute Input OV Interrupt	Bit[9] enables or disables INT# pin assertion for the Absolute Input OV Interrupt. 0 = Enable Absolute Input OV INT# (default) 1 = Disable Absolute Input OV INT#
[8]	Relative Output OV Interrupt	Bit[8] enables or disables INT# pin assertion for the Relative Output OV Interrupt. 0 = Enable Relative Output OV INT# (default) 1 = Disable Relative Output OV INT#
[7]	VINOK Interrupt	Bit[7] enables or disables INT# pin assertion for the VINOK Interrupt. 0 = Enable VINOK INT# (default) 1 = Disable VINOK INT#
[6]	Output Current Alert	Bit[6] configures the Output Current Alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge
[5]	Input Current Alert	Bit[5] configures the Input Current Alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge
[4]	Minimum Input Voltage Loop Alert	Bit[4] configures the Minimum Input Voltage Loop Alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge
[3]	Ready Alert	Bit[3] configures the Ready Alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge
[2]	Relative Output Undervoltage Alert	Bit[2] configures the Relative Output Undervoltage Alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge
[1]	Pass-Through Mode Alert	Bit[1] configures the Pass-Through Mode alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge
[0]	General Comparator Alert	Bit[0] configures the General Comparator Alert trigger polarity. 0 = Trigger on rising edge (default) 1 = Trigger on falling edge

6.8 Information Register

The information registers contain SMBus readable information about manufacture and operating modes. Table 18, Table 19, Table 20, and Table 21 identify the bit locations of the available information.

Table 18. Information1 Register 0x3A

Bit	Name	Description
[15]	Forward PGOOD	Bit[15] indicates Forward PGOOD status. 0 = Not Good 1 = Good
[14]	Reverse PGOOD	Bit[14] indicates Reverse PGOOD status. 0 = Not Good 1 = Good
[13:12]	Operating Mode	Bits[13:12] indicate the operating mode. 00 = Off 01 = Reverse PTM 10 = Forward PTM 11= Forward Buck
[11:8]	Power State Machine	Bits[11:8] indicate the Power State Machine status. 0000 = RESET state. 0001 = SLEEP state. 0010 = PRE-CHARGE state. 0011 = READY state. 0100 = REVERSE_PTM state. 0101 = SWITCHING state. 0110 = FORWARD_PTM state. 0111 = FAULT_LATCHOFF state. 1000 = FAULT_RETRY state. 1001 = AUTO_DISCHARGE state.
[7]	Operating Buck Level	Bit[7] indicates the 3-Level Buck operation status. 0 = Not active 1 = Active
[6]	High Range Request	Bit[7] indicates high range/low range. 0 = Low range 1 = High range
[5]	Modulator in OFF State	Bit[5] indicates the modulator state. 0 = Not in OFF state 1 = In OFF state
[4]	EXT5V State	Bit[4] indicates EXT5V status. 0 = EXT5V not active 1 = EXT5V active
[3:2]	Active Control Loop	Bits[3:2] indicate active control loop. 00 = Output Voltage Loop 01 = Output Current Loop 10 = Input Current Loop 11 = Minimum Input Voltage Loop
[1]	IGATE Charge Pump Status	Bit[1] indicates IGATE charge pump status. 0 = IGATE charge pump is not good 1 = IGATE charge pump is good
[0]	VINOK status	Bit[0] indicates VINOK status. 0 = VINOK is low 1 = VINOK is high

Table 19. Information2 Register 0x4D

Bit	Name	Description
[15:7]	Reserved	-
[6]	PTM Timeout Status	Bit[6] indicates PTM Timeout status 0 = PTM Entry timeout has not occurred 1 = PTM Entry timeout has occurred
[5]	Internal Reference	Bit[5] indicates internal reference 0 = Internal reference is not active 1 = Internal reference is active
[4:0]	PROG Pin Readout	Bits[4:0] indicates PROG pin readout. See below for details (I^2C Target Address/Default Operation/Output /Voltage, and Default Input Current Limit respectively). 01011 = 0x96, Sleep, 0.476A 01100 = 0x96, PTM, 1.5A 01101 = 0x96, PTM, 0.476A 01110 = 0x96, 5V, 1.5A 01111 = 0x96, 5V, 0.476A 10000 = 0x96, 20V, 1.5A 10001 = 0x96, 20V, 0.476A 10010 = 0x94, Sleep, 0.476A 10011 = 0x94, PTM, 1.5A 10100 = 0x94, PTM, 0.476A 10101 = 0x94, 5V, 1.5A 10110 = 0x94, 5V, 0.476A 10111 = 0x94, 20V, 1.5A 11xxx = 0x94, 20V, 0.476A

Table 20. Information3 Register 0x90

Bit	Bit Name	Description
[15]	Over-Temperature Fault	1 = Over-temperature Fault occurred. Cleared by reading Information3 register
[14]	Way Overcurrent Fault	1 = Way Overcurrent Fault occurred. Cleared by reading Information3 register
[13]	Absolute Output UV Fault	1 = Absolute Output UV Fault occurred. Cleared by reading Information3 register
[12]	Reverse PTM UV and OV Fault	1 = Reverse PTM UV OV Fault occurred. Cleared by reading Information3 register
[11]	CFLY UV OV Fault	1 = Cfly UV OV Fault occurred. Cleared by reading Information3 register
[10]	Absolute Output OV Interrupt	1 = Absolute Output OV Interrupt triggered. Cleared by reading Information3 register
[9]	Absolute Input Overvoltage Interrupt	1 = Absolute Input Overvoltage Interrupt triggered. Cleared by reading Information3 register
[8]	Relative Output OV Interrupt	1 = Relative Output OV Interrupt triggered. Cleared by reading Information3 register
[7]	VINOK interrupt	1 = VINOK Interrupt triggered. Cleared by reading Information3 register
[6]	Output Current Alert	1 = Output Current Alert triggered. Cleared by reading Information3 register
[5]	Input Current Alert	1 = Input Current Alert triggered. Cleared by reading Information3 register
[4]	Minimum Input Voltage Loop Alert	1 = Minimum Input Voltage Loop Alert triggered. Cleared by reading Information3 register
[3]	Ready Alert	1 = Entered READY state. Cleared by reading Information3 register
[2]	Relative Output UV Alert	1 = Relative Output UV Alert triggered. Cleared by reading Information3 register
[1]	Pass-Through Mode Alert	1 = PTM was entered or exited. Cleared by reading Information3 register
[0]	GP Comparator Alert	1 = GP comparator triggered. Cleared by reading Information3 register

Table 21. Information4 Register 0x91

Bit	Name	Description
[15]	Over-Temperature Fault	0 = Not active 1 = Active
[14]	Way Overcurrent Fault	0 = Not active 1 = Active
[13]	Absolute Output UV	0 = Not active 1 = Active
[12]	Reverse Pass-Through Mode UV OV fault	0 = Not active 1 = Active
[11]	CFLY UV OV fault	0 = Not active 1 = Active
[10]	Absolute Output OV Interrupt	0 = Not active 1 = Active
[9]	Absolute Input OV Interrupt	0 = Not active 1 = Active
[8]	Relative Output OV Interrupt	0 = Not active 1 = Active
[7]	VINOK Interrupt	0 = Not active 1 = Active
[6]	Output Current Alert	0 = Not active 1 = Active
[5]	Input Current Alert	0 = Not active 1 = Active
[4]	Minimum Input Voltage Loop Alert	0 = Not active 1 = Active
[3]	Ready Alert	0 = Not active 1 = Active
[2]	Relative Output UV Alert	0 = Not active 1 = Active
[1]	Pass-Through Mode Alert	0 = Not active 1 = Active
[0]	General-Purpose Comparator Alert	0 = Not active 1 = Active

6.9 ADC register

RAA489300 provides four ADC registers. The ADC registers can be enabled or disabled by Control3 Bit[0]. The data format of ADC registers is shown in Table 22.

Table 22. ADC Output

ADDR	Description	LSB	Sample Window Time	Polling Time
0x83	Input Current [7:0]	22.2mA	80µs	320µsec
0x85	Output Current [7:0]	22.2mA	80µs	320µsec
0x86	Output Voltage [7:0]	192mV	80µs	320µsec
0x87	Input Voltage [7:0]	192mV	80µs	320µsec

7. Modulator Information

7.1 3-Level Buck Converter Operation

As shown in Figure 21, the topology of the 3-level buck converter includes a flying capacitor, an inductor and FETs. The switching scheme of the 3-level buck has that complementary gate signals drive the Q4 and Q1 with a duty cycle.The gate signals of Q3 and Q2 have a phase difference of 180 degrees from the gate signals of Q4 and Q1, respectively.

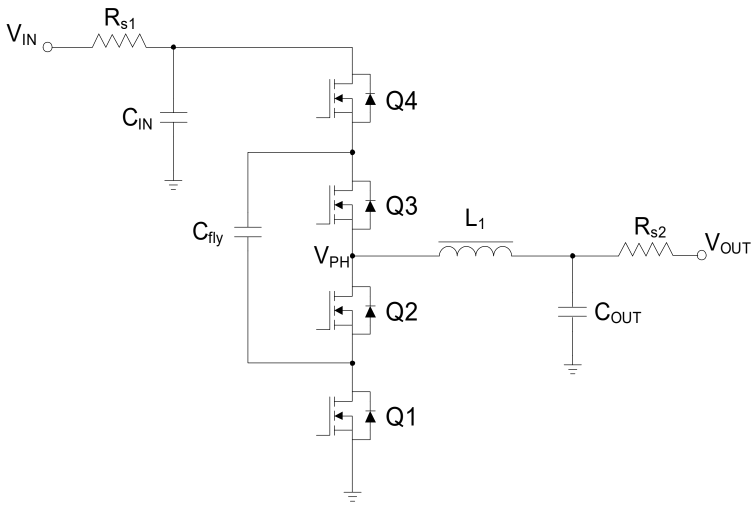


Figure 21. 3-level Buck Converter

If V_{CFLY} is charged with $V_{IN}/2$, the operation of the 3-level buck converter can be considered as a 2-level buck converter. However, V_{PH} does not alternate between V_{IN} and ground. Instead, V_{PH} alternates between $V_{IN}/2$ and ground in low duty operation, or between V_{IN} and $V_{IN}/2$ in high duty operation. Figure 22 shows the inductor current, V_{PH} and the gate signal of each FET when the duty is less than 0.5. The waveforms of the V_{PH} and inductor current shown in Figure 2 are identical to those of the 2-level buck converter. That is, V_{PH} becomes $V_{IN}/2$ or ground and the inductor current appears as a triangle wave that increases when V_{PH} is $V_{IN}/2$ and decreases when V_{PH} is ground. However, the inductor current or phase voltage has twice the frequency compared to the gate signal of the switching devices.

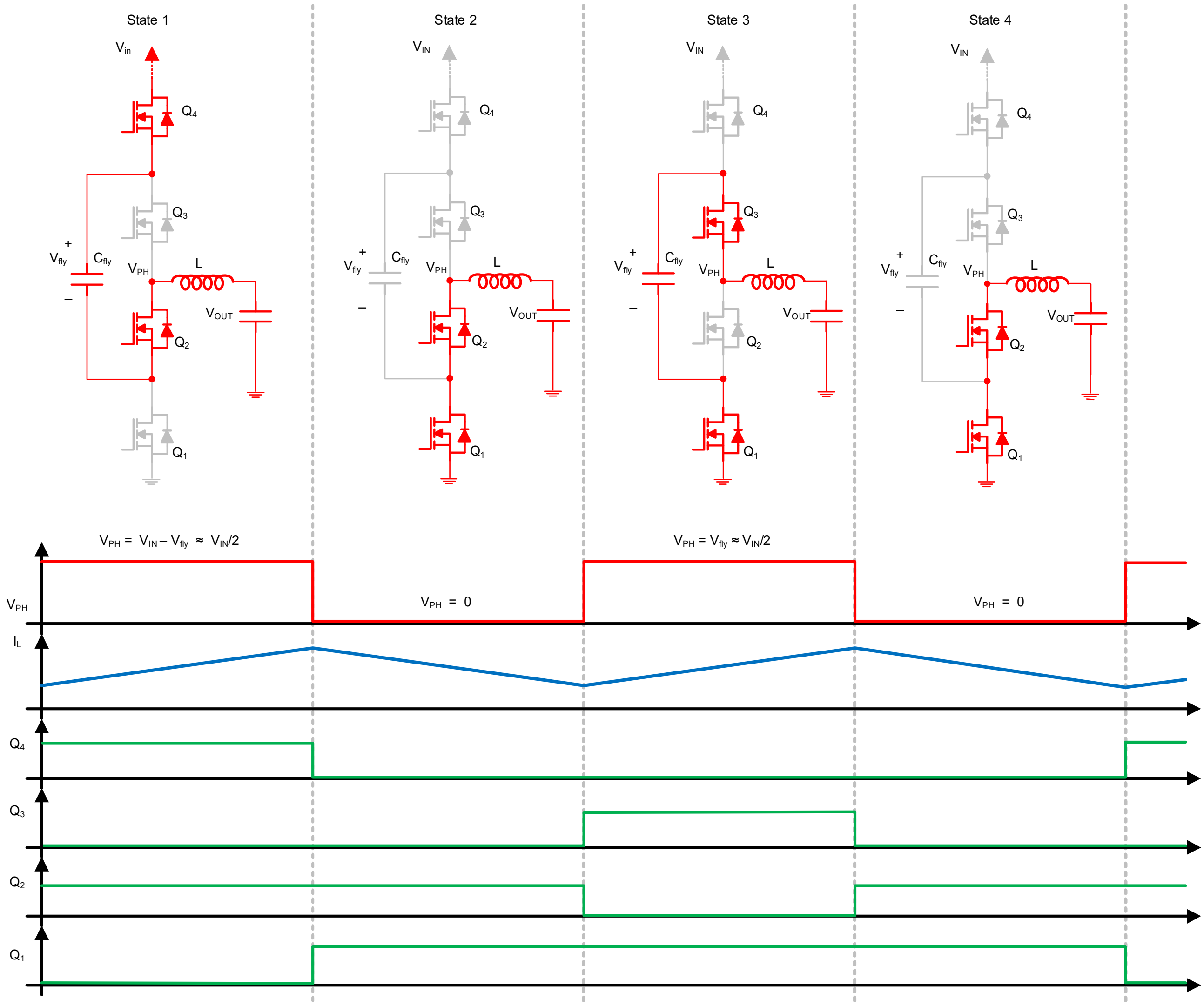


Figure 22. 3-Level Buck Converter Switching Scheme with Low Voltage Range (Duty = 0.25)

Figure 23 shows the operation of the 3-level buck converter when the duty is greater than 0.5. The waveforms of the inductor current shown in Figure 23 are identical to that of the 2-level buck converter. However, as the duty becomes greater than 0.5, V_{PH} becomes V_{IN} or $V_{IN}/2$. It operates similarly with the conventional 2-level buck converter except that V_{PH} is $V_{IN}/2$ when the inductor current is decreasing, and the inductor current or phase voltage has twice the frequency compared to the gate signal of the switching devices. Therefore, a 3-level buck converter can be expressed as a combination of a buck converter in which V_{PH} is alternately connected to $V_{IN}/2$ and ground, and a buck converter in which V_{PH} is alternately connected to V_{IN} and $V_{IN}/2$. Considering all cases where the duty value changes from 0 to 1, by keeping VCFLY at half of V_{IN}, V_{PH} is alternately switched to 3 levels: V_{IN}, $V_{IN}/2$, and ground.

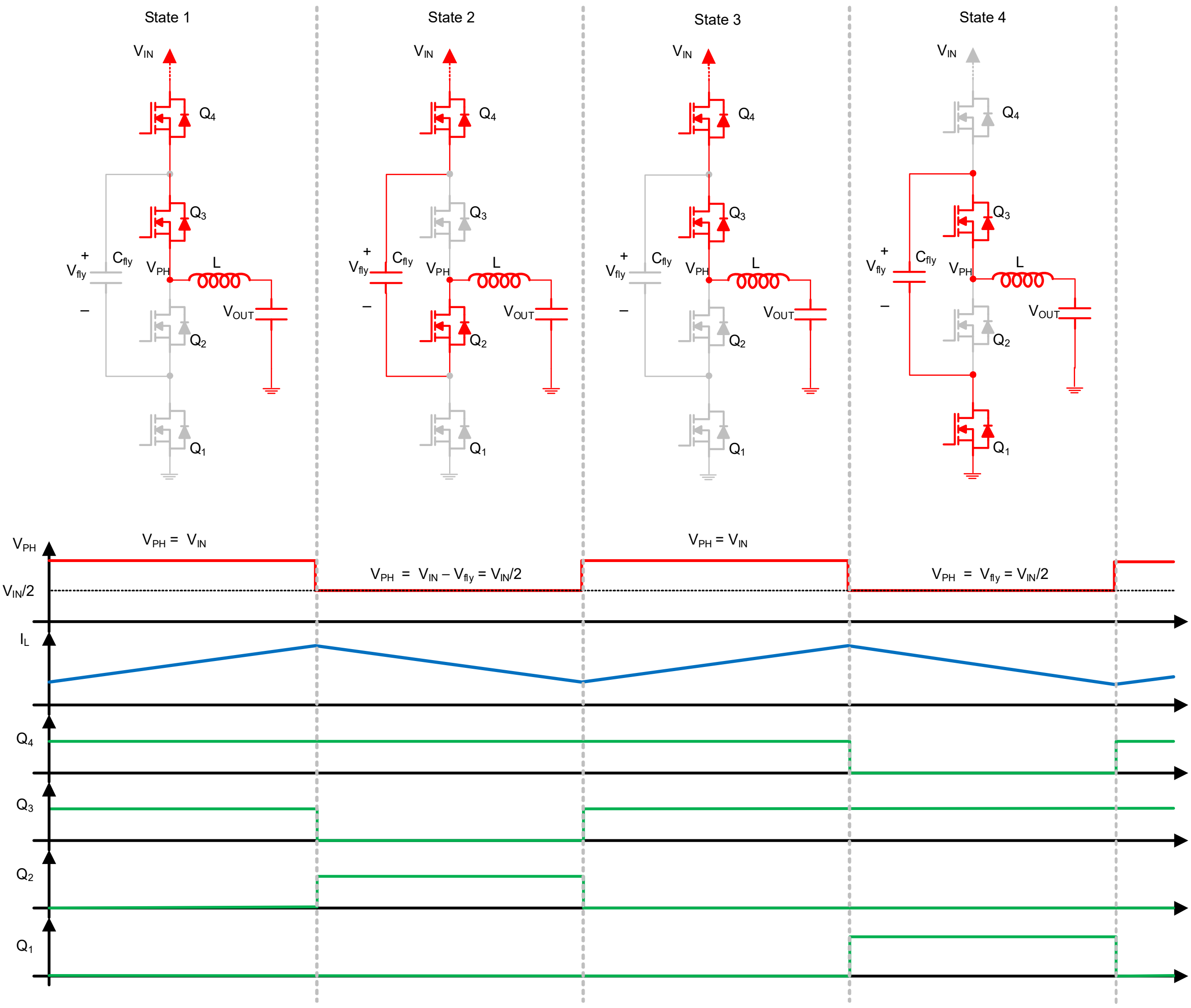


Figure 23. 3-Level Buck Converter Switching Scheme with High Voltage Range (Duty = 0.75)

In the ideal operation of the 3-level buck converter, the Vds of each of the 4 FETs can be half of the input voltage. As shown in Figure 24, since the ripple current of the inductor is 1/4 that of the conventional 2-level buck converter, the size of the ripple current is half of the conventional 2-level buck converter, even if half the size inductor applied to the 3-level converter half the size.

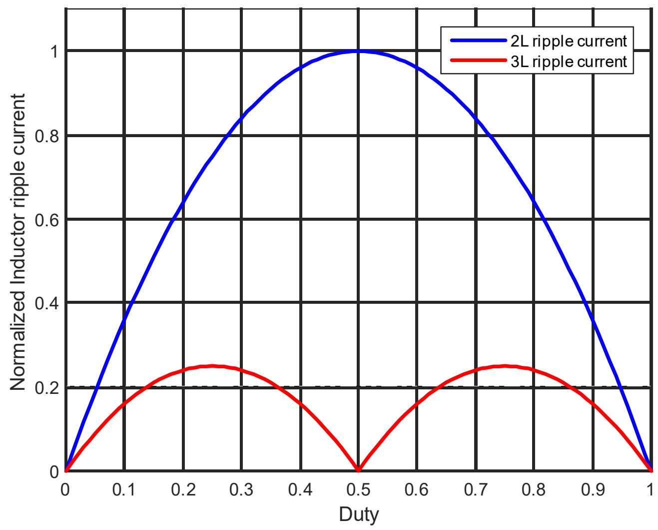


Figure 24. Inductor Ripple Current Comparison of 2-Level and 3-Level Converter

7.2 Modulator

7.2.1 R3 Modulator

The RAA489300 uses the Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 25 and Figure 26 conceptually show the control block diagram of the RAA489300 and R3 modulator circuit, and Figure 27 shows the operation principles in steady state.

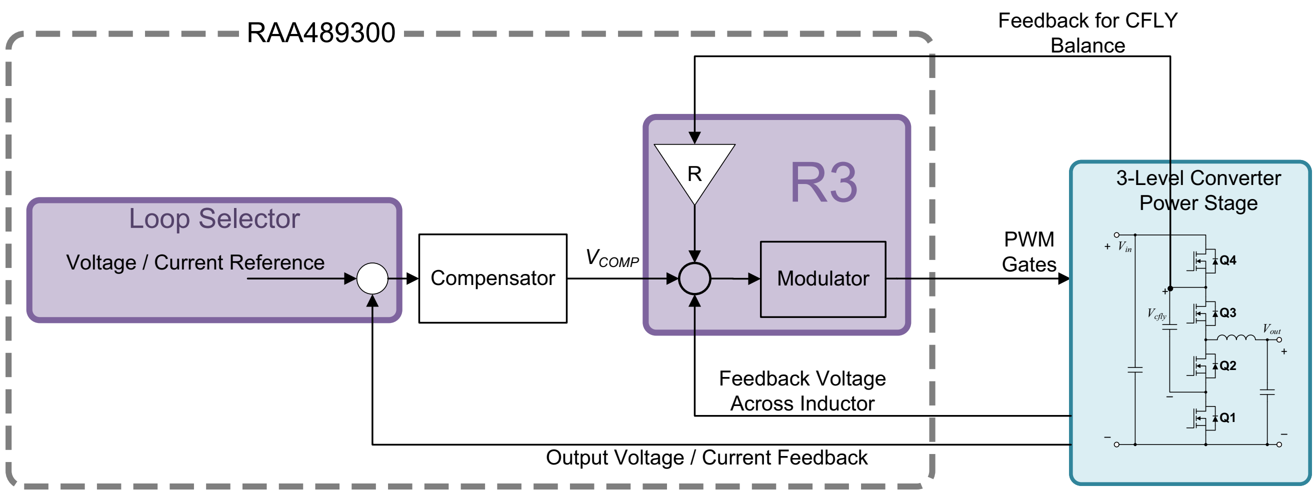


Figure 25. Control Block Diagram of the RAA489300

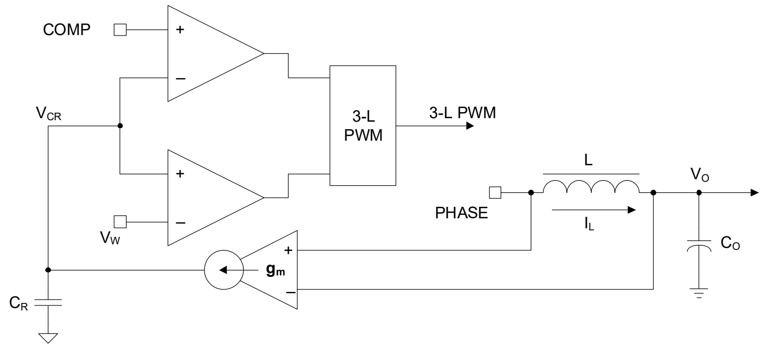


Figure 26. R3 Modulator

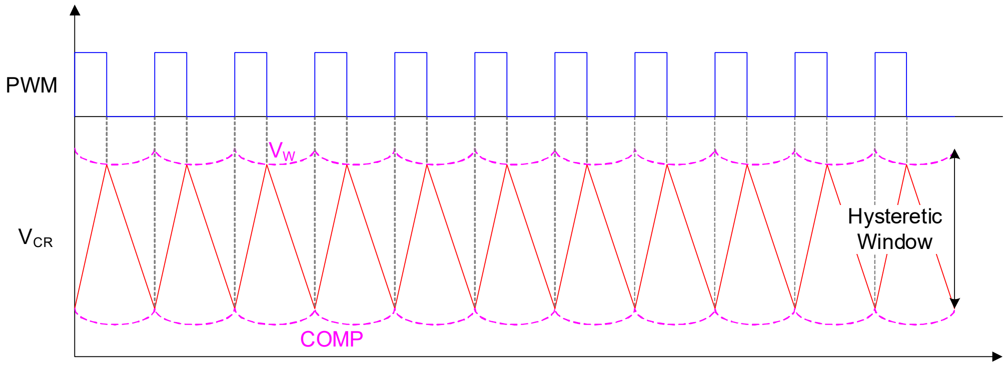


Figure 27. R3 Modulator Operation Principles in Steady State

A fixed voltage window (VW window) is between VW and COMP. The modulator charges the ripple capacitor CR with a current source equal to gm(VIN - VO) during PWM on-time, and it discharges the ripple capacitor CR with a current source equal to gmVO during PWM off-time, where gm is a gain factor. The CR voltage VCR therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when VCR reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with VCR, which is a large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulators.

Figure 28 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, temporarily turning on PWM pulses earlier and more frequently, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

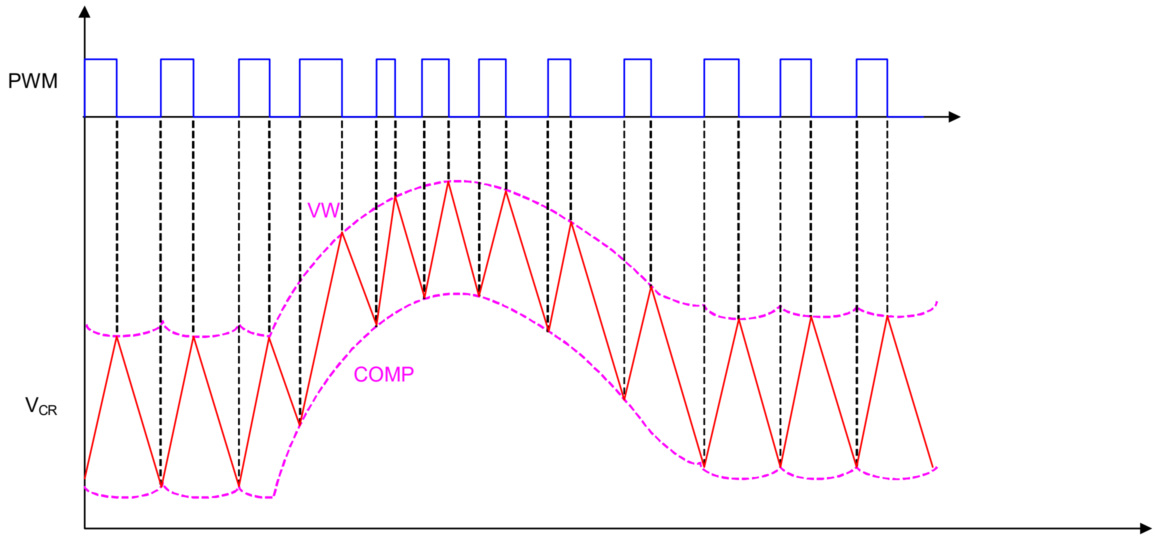


Figure 28. R3 Modulator Operation Principles in Dynamic Response

8. Application Information

8.1 Soft-Start

The RAA489300 includes a high-power LDO with 5V output, with an input from the VIN pin. The RAA489300 also has an EXT5V pin that can accept a 5V input. The LDO output or EXT5V input are tied to the VDD pin to provide bias power and gate drive power for the RAA489300. However, LDO output and EXT5V input are not used at the same time, and only EXT5V input is used when there is an EXT5V input. The VDDP pin is the RAA489300 gate drive power supply input. Only when powering the gate driver from EXT5V, the RAA489300 can select a gate voltage of 5V or 10V, and the gate voltage of 10V is supplied through the gate driver charge pump. The VDD pin and VDDP pin are separately connected to a decoupling capacitor for stable power supply.

When VDD > 2.7V, the RAA489300 digital block is activated by low power LDO and the SMBus register is ready to communicate with the main controller. Although the default value of VINOK reference is 0, the VINOK threshold is 3.8V after VDD POR. When VIN > 3.8V after VDD POR, the RAA489300 initializes with a debounce time of 150ms. For initialization, it reads trim settings and PROG pin programming options, and performs autozero of the internal circuitry. To read PROG pin programming options on RAA489300, it sources a current out of the PROG pin and reads the pin voltage to determine the PROG resistor value. Table 23 shows the register values set by the PROG resistor.

After initialization, the RAA489300 charges the boot capacitors for the switching FETs and precharges Cfly for 200ms before starting switching. The Cfly precharge time can be set in Control0 Bits[14:13]. When Cfly precharging begins, the RAA489300 uses proprietary technology to check if the VSYS output is shorted (see section Faults, Interrupts, and Alerts).

After Cfly's precharge is finished, the RAA489300 starts switching. When the output voltage crosses the PGOOD window for the DAC value of Output Voltage register, IGATE turns on and 1ms later, the PGOOD goes high. More details about PGOOD are in the section PGOOD, and details on IGATE are in section IGATE Control.

8.2 PROG Pin Option

The resistor from the PROG pin to GND programs the configuration of the RAA489300 for the default device address, the default operation mode/output voltage, and input current limit.

After POR, the RAA489300 supplies 130µA current to the PROG pin and reads the PROG pin voltage to determine the programming option. Therefore, a PROG resistor must have a tolerance of less than 1%. However, if an application requires higher noise immunity on the pin, a capacitor from the PROG pin to GND can be added to provide filtering. The resistor and the capacitor R-C time constant should be less than 40µs so the PROG pin voltage can rise to a steady state before the RAA489300 reads it. Table 23 shows the programming options.

Table 23. PROG Pin Programming Options

PROG - GND Resistance [Ω]			Topology	Device Address	Default Operation / Output Voltage	Default Input Current Limit [A]
Min	Typ 1%	Max				
	1870		3-L buck	96H	Sleep	0.476
	2210				Pass-Through Mode	1.5
	2740				Pass-Through Mode	0.476
	3240				5V	1.5
	3740				5V	0.476
	4420				20V	1.5
	5490				20V	0.476
	6490			94H	Sleep	0.476
	7500				Pass-Through Mode	1.5
	8450				Pass-Through Mode	0.476
	9310				5V	1.5
	11000				5V	0.476
	12700				20V	1.5
	14700				20V	0.476

8.3 EXT5V and Gate Voltage

The RAA489300 has built-in gate drivers for switching devices, and the gate voltage can be set to either 5V or 10V using Control2 Bits[2:1]. Table 24 shows the corresponding gate voltages based on the settings of Control2 Bits[2:1].

Table 24. Gate Voltage According to Control2 Bits[2:1]

Presence of EXT5V	Control2 Bits[2:1]	Gate Voltage (VDDP)
No (VDD Generated by Internal LDO)	0b00	5V
	0b01	
	0b10 or 0b11	
Yes (VDD Generated by EXT5)	0b00	10V
	0b01	5V
	0b10 or 0b11	Auto Mode

As shown in Table 24, if there is no 5V voltage source supplied to the EXT5V pin, the RAA489300 provides a 5V gate voltage regardless of the Control2 Bits[2:1] settings. The gate voltage can be configured through Control2 Bits[2:1] when power is supplied to the EXT5V pin. When a 5V external voltage source is supplied to the EXT5V pin and Control2 Bits[2:1] are set to 0b10 or 0b11, the RAA489300 automatically adjusts the gate voltage, switching between 5V in Discontinuous Conduction Mode (DCM) and 10V in Continuous Conduction Mode (CCM).

VDDP pin serves as the gate drive power supply input for the RAA489300, with the voltage set to either 5V or 10V depending on the Control2 Bits[2:1] settings. When the gate voltage is set to 5V, the VDD pin and VDDP pin are internally connected. When the gate voltage is set to 10V, the voltage from the VDD pin is stepped up to 10V using a 1:2 charge pump and supplied to the VDDP pin. Therefore, the VDD pin and VDDP pin should not be externally connected. For proper operation, the VDDP pin requires a decoupling capacitor with an effective capacitance of at least 200nF at 10V, while the VDD pin requires a decoupling capacitor with an effective capacitance of at least 1µF at 5V.

Figure 2, Figure 3, and Figure 4 show that the RAA489300 requires bootstrap capacitors and diodes. However, to ensure that Q4 and Q3 remain turned on in Pass-Through Mode (PTM) and to maintain a stable gate voltage during deep Discontinuous Conduction Mode (DCM), the RAA489300 integrates a built-in boot charge pump. During the deep Discontinuous Mode of operation, as the controller operates in the Pulse Frequency Modulation (PFM) mode, the boot charge pump automatically turns on to maintain the boot voltage during the long periods of non-switching, and this functionality can be disabled or enabled 0 by configuring Control4 Bit[5]. Regardless of the operating state, the frequency and forced shutdown of the boot charge pump can be configured using Control1 Bits[11:10].

8.4 Pass-Through Mode

The Pass-through mode (PTM) is a feature of the RAA489300 that enables direct connection between the input and output, ensuring that the output voltage (CSOP) is maintained the same as the input voltage (CSIN). This feature enhances efficiency, particularly during light load conditions. When the PTM is entered, Q4 and Q3 are continuously turned on. The RAA489300 provides 3 types of PTMs. The first is Forward PTM, the second is Low Power PTM, and the third is Reverse PTM. More details about each PTM can be found in subsections 8.4.1, 8.4.1 and 8.4.1.

8.4.1 Forward PTM

Prior to entering Forward PTM, configure the registers as follows:

1. Set the Forward/Reverse Operation bit to Forward (Control0 Bit[2] = 0).
2. Set the Low Power PTM mode bit to disable (Control2 Bit[12] = 0).
3. Set the PGOOD Window bit to 20% (Control2 Bits[9:8] = 0b11).
4. Set the Output Voltage register (0x15) to the value obtained from Equation 1.

(EQ. 1)
$$\text{Output Voltage} = \text{Input Voltage} \times \text{Input Voltage Tolerance Ratio} - 0.5\text{V}$$

5. Set the Enable PTM bit to enable (Control1 Bit[1] = 1) to enter the Forward PTM mode.

When the RAA489300 successfully enters the Forward PTM, the Q4 and Q3 are continuously turned on, the Operating Mode bits are set to Forward PTM (Information1 bits [13:12] = 0b10), and the Power State Machine bits are set to the Forward PTM state (Information1 bits [11:8] = 0b0110).

The RAA489300 provides the PTM Entry Timeout bit (Control0 Bit[7]) to control the behavior when the PTM entry is unsuccessful. When the PTM Entry Timeout bit is set to disable (Control0 Bit[7] = 0), the RAA489300 maintains SWITCHING state with the output voltage DAC if the CSOP pin voltage does not reach within 300mV from the CSIN pin voltage. When the PTM Entry Timeout bit is set to enable (Control0 Bit[7] = 1), the RAA489300 aborts the PTM entry if the CSOP pin voltage is not within 300mV from the CSIN pin voltage within 100ms, and the RAA489300 enters the SLEEP state.

By setting the PROG pin, the RAA489300 can be programmed to enter the Forward PTM automatically when startup occurs. The Forward PTM configuration using the PROG pin can be found in Table 23. The default value of the Absolute Output OV threshold of the RAA489300 is 24V; therefore, the input voltage should be less than the Absolute Output OV threshold when entering Forward PTM using the PROG options.

After entering PTM, the RAA489300 exits PTM if any of the following criteria are met:

- When the PTM control bit (Control0 Bit[1]) is disabled.
- When the VINOK Interrupt (Control5 Bit[7]) is enabled and the input voltage falls below the set value of the VINOK Reference register or 3.8V.
- When the output current exceeds the Output Current Alert Threshold (Control0 Bits[10:9]) while the Exit PTM with Current Alert (Control3 Bit[1]) is enabled.
- When Absolute Output OV Interrupt, Absolute Input OV Interrupt, Relative Output OV Interrupt, or Relative Output UV Interrupt occurs.

To exit the Forward PTM, configure the registers as follows:

1. Set the Relative Output OV Protection to disable (Control5 Bit[8] = 1).
2. Set the CFLY OV UV Fault to disable (Contrl5 Bit[11] = 1).
3. Set the CFLY Pre-Charge Function to enable (Control2 Bit[7] = 1).
4. Set the CSOP Discharge bit to enable (Control2 Bit[14] = 1).
5. Set the Enable PTM bit to disable (Control1 Bit[1] = 0) to exit the Forward PTM mode.

Depending on the setting for Control0 Bit[0], the RAA489300 can exit from PTM to resume switching or can directly enter the SLEEP state.

After the RAA489300 exits the Forward PTM, configure the registers as follows:

1. Set the CSOP Discharge bit to disable (Control2[14] = 0).
2. Set the CFLY Pre-Charge Function to disable (Control2 Bit[7] = 0).
3. Set the CFLY OV UV Fault to enable (Control5 Bit[11] = 0).
4. Set the Relative Output OV Protection to enable (Control5[8] = 0).

8.4.2 Reverse PTM

To enter the Reverse PTM, configure the registers as follows:

1. Set the CFLY Pre-Charge Function to disable (Control2 Bit[7] = 0).
2. Set the PGOOD Window to 20% (Control2 Bits[9:8] = 0b11).
3. Set the Reverse PTM voltage (0x49) according to the CSON side voltage.
4. If the IGATE is used, set the IGATE Control to IGATE Force ON (Control3 Bit[7:6] = 0b01). To prevent an excessive inrush current, Renesas recommends the CSIP side terminal is open or is not heavily loaded before turning on the IGATE.
5. Set the Enable bit to enable (Control0 Bit[0] = 1), set the FWD/REV Operation bit to Reverse (Control0 Bit[2] = 1), and set the Pass-Through Mode bit to enable (Control0 Bit[1] = 1). In other words, set the Control0 Bits[2:0] to 0b111.

Note: If the IGATE is located on the CSON side, the internal LDO cannot be powered through the VIN pin when the power source is located the CSON side and the IGATE is turned off. For such configuration, the RAA489300 must be powered through the EXT5V pin to enter Reverse PTM.

After entering the Reverse PTM, the RAA489300 exits the Reverse PTM if any of the following criteria is met:

- The Reverse PTM OV UV fault is triggered, which is based on the Reverse PTM Voltage (0x49) and PGOOD Window (Control2 bits [9:8]).

To exit the Reverse PTM, configure the registers as follows:

1. Set the Pass-Through Mode bit to disable (Control0 Bit[1] = 0).

When the RAA489300 exits the Reverse PTM, it enters the SLEEP state.

8.4.3 Low Power PTM

Low Power PTM significantly reduces the RAA489300 bias current compared to regular Forward PTM. However, in Low Power PTM, not all monitoring functions and protection features are operational.

Low Power PTM can be entered either from SWITCHING state or SLEEP state. To enter the Low Power PTM, configure the registers in steps as follows:

1. Set the Output Voltage register (0x15) to the value obtained from Equation 1. Ensure that the output voltage setting is lower than the VOUT Absolute Overvoltage threshold.
2. Set PGOOD window to 20% by Control2[9:8] = 0b11.
3. Enable Low Power PTM mode by setting Control2 Bit[12] = 1.
4. Ensure the Forward/Reverse Operation is set to Forward by Control0 Bit[2] = 0.
5. Enable switching by Control0 Bit[0] = 1 and Enable PTM by Control0 Bit[1] = 1.

When the RAA489300 successfully enters LP PTM, the operating mode bits are set to Forward PTM (Information1 Bits[13:12] = 0b10), and the Power State Machine bits is set to the Forward PTM state (Information1 Bits[11:8] = 0b0110) (see Table 18). Similar to Forward PTM, the PTM entry timeout bit (Control0 Bit[7]) controls the behavior in case of a failure to enter LP PTM (see Forward PTM).

After entering LP PTM, RAA489300 exits LP PTM if any of the following criteria is met:

- When the PTM control bit is disabled (Control0 Bit[1] = 0). the RAA489300 transitions to Switching mode. However, when transitioning to Switching mode, the previously deactivated protection functions are simultaneously activated, which can cause faults, interrupts, or alerts. Therefore, this method of exiting LP PTM is not recommended.
- When the Low Power PTM mode is set to Regular PTM mode (Control2 Bit[12] = 0), the RAA489300 transitions to SLEEP state, which prevents faults, interrupts, or alerts occurring. This method is recommended for exiting LP PTM.

8.5 Cfly Balance

To operate a 3-level buck converter, the flying capacitor (Cfly) voltage must be regulated to half of the input voltage. The RAA489300 offers two methods to achieve this. The first method is the Cfly pre-charging function, which uses an internal current source to regulate the Cfly voltage. The second method is through the Cfly balancer within the enhanced 3-level R3 modulator, which controls the Cfly voltage during the SWITCHING state.

The Cfly pre-charging function can be enabled or disabled in Control2 Bit[7]. However, after a Power-On Reset (POR) at startup or when a fault occurs, the Cfly pre-charging function operates automatically, regardless of the setting of Control2 Bit[7]. This function also operates in PTM and deep Discontinuous Conduction Mode (DCM), provided that pre-charging is enabled in Control2[7].

When the RAA489300 enters the SLEEP state, the Cfly pre-charging function is automatically turned off, regardless of the control register settings. When the state switches from SLEEP to SWITCHING, the Cfly pre-charging function is enabled by default for 200ms to regulate the Cfly voltage to half of the input voltage. This 200ms duration can be adjusted in Control0 Bits[14:13] (see Table 11).

By default, the pre-charging circuitry works in high-power mode, continuously regulating the Cfly voltage to $V_{IN}/2$. It can be configured to low-power mode for saving power, where the Cfly voltage is regulated periodically (either 1950µs or 7710µs intervals). The pre-charge mode can be selected using Control2 Bit[6], while Control2 Bit[5] controls the activation duration of the pre-charge circuitry (see Table 13).

The Cfly balancer within the R3 modulator operates only in the SWITCHING state. The gain of the Cfly balancer within the R3 modulator can be increased by four times through Control4 Bit[14] (see Table 15). When the gain of the Cfly balancer is increased, the Cfly voltage is more aggressively regulated in the SWITCHING state. However, depending on the system configuration, there might be conditions where system operation is unstable, so system stability should be checked when changing the gain.

8.6 PGOOD

The RAA489300 provides a PGOOD pin to indicate if the output voltage is out of the PGOOD window based on the DAC value of Output Voltage register. The PGOOD window is enabled by default, and Control3 Bit[4] = 1 disables the PGOOD pin function. Setting Control3 Bit[4] = 1 does not disable PGOOD window (see Table 14). The size of the PGOOD window can be set in the Control2 Bits[9:8] (see Table 13). For example, if the Control2 Bits[9:8] is set to 20% (0b11), the upper boundary of the PGOOD window is 20% larger than the Output Voltage register DAC value, and the lower boundary is 20% smaller.

When the output voltage goes out of the PGOOD window, the PGOOD pin is pulled low. PGOOD window also can trigger the Relative Output Overvoltage (OV) interrupt and Relative Output Undervoltage (UV) Alert depending on whether an output overvoltage or undervoltage event occurs (see Table 20). More details about the Relative Output OV interrupt are in section Relative Output Overvoltage Interrupt and details on Relative Output UV Alert are in section Relative Output Under Voltage Alert. Figure 29 shows how the PGOOD pin is asserted depending on the output voltage and the PGOOD window. Table 25 describes the PGOOD window and PGOOD hysteresis window size according to Control2 Bits[9:8].

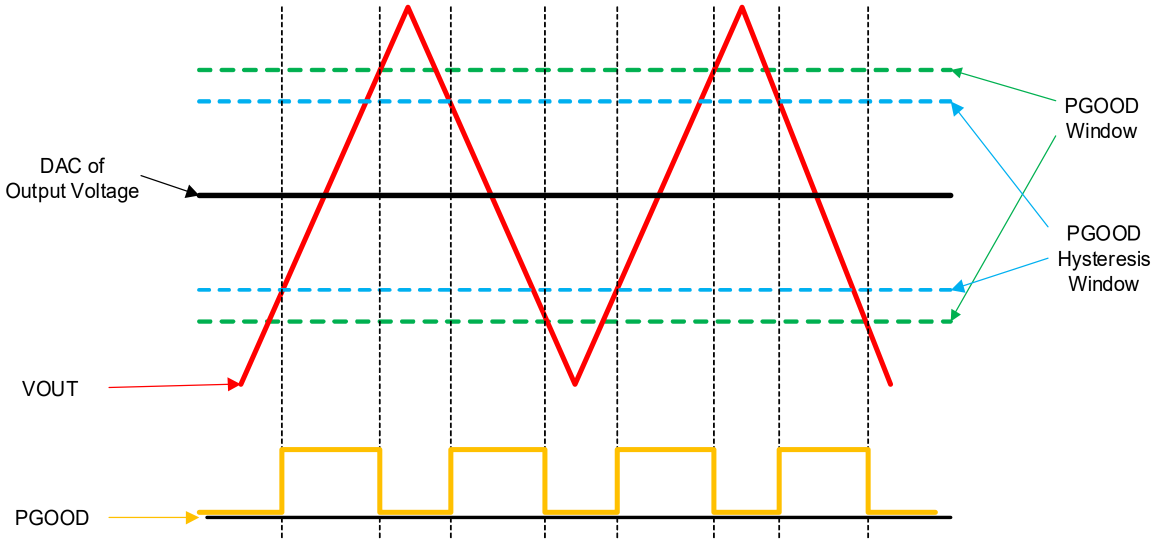


Figure 29. PGOOD Window Behavior

Table 25. PGOOD Window According to Control2 Bits[9:8]

Control2 Bits[9:8]	PGOOD Window	PGOOD Hysteresis
00	5%	2.5%
01	10%	5%
10	15%	5%
11	20%	5%

When Output Voltage DAC is changed in SWITCHING state, the PGOOD status is masked during a V_{OUT} transition. Figure 30 shows the PGOOD signal remains high when Output Voltage DAC is changed in SWITCHING state, even if the V_{OUT} is below PGOOD window UV threshold during the V_{OUT} transition.

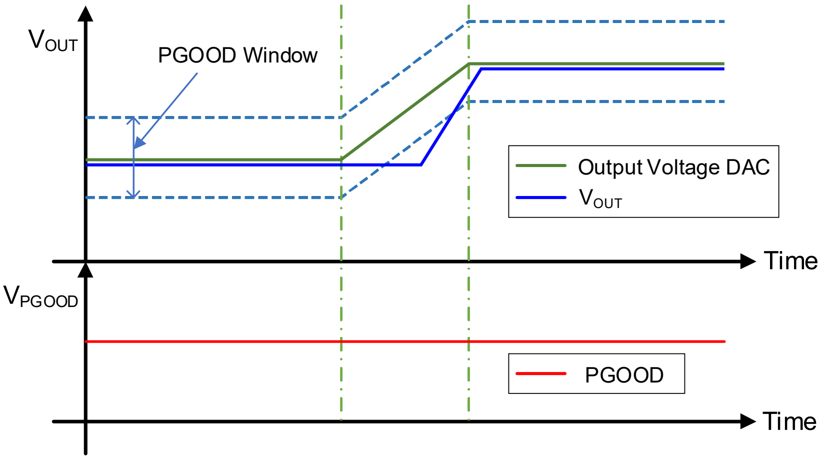


Figure 30. PGOOD and Output Voltage DAC Transition

8.7 IGATE Control

To isolate the power stage driven by the RAA489300 from inputs or outputs, the RAA489300 provides an IGATE driver. As seen in the typical application circuit (Figure 2), IGATE can be configured on either an input or an output or can be omitted. The Control3 Bits[7:6] can control how the IGATE driver operates. The IGATE driver can be configured to operate in the following modes using the Control3 Bits[7:6]:

- 00 = Auto
- 01 = IGATE Force ON
- 10 = IGATE Force OFF
- 11 = Tri-State IGATE

After POR, the IGATE control (Control3 Bits[7:6]) is set to AUTO by default, IGATE remains turned off while in the READY state and automatically turns on 1ms after the output voltage reaches the PGOOD window. After IGATE turns on, the PGOOD pin becomes High. ***Important:*** If PGOOD is disabled (Control3 Bit[4] = 1), the turn-on of IGATE is still determined by whether the output voltage is within the PGOOD window. After IGATE is turned on with IGATE control set to AUTO, IGATE turns off only when RAA489300 transitions out of the SWITCHING state. For example, IGATE turns off when the SWITCHING state exits due to a fault such as Over-temperature Fault or Absolute UV Fault.

The turn-on timing of IGATE in auto mode can be adjusted using Control3 Bit[5]. If Control3 Bit[5] is set to 1, IGATE turns on as switching starts or enters PTM. IGATE Control (Control3 Bits[7:6]) can force the output of the IGATE driver ON OFF.

If the gate pin of the IGATE MOSFET is shared with a controller other than the RAA489300, control of the gate pin of the IGATE MOSFET can be relinquished to another controller by setting the IGATE control (Bits[7:6] in the Control3 register) to Tri-State IGATE. When the IGATE control (Control3 Bits[7:6]) is set to Tri-State IGATE, the IGATE pin of the RAA489300 becomes a high impedance state.

The IGATE driver uses the internal charge pump. The charge pump refresh cycle for the IGATE driver can be set in Enable IGATE Charge Pump to 100% (Control3 Bit[11]). When Enable IGATE Charge Pump to 100% (Control3 Bit[11]) is disabled, the charge pump refresh cycle is 8ms. If the Control3 Bit[11] (Enable IGATE Charge Pump to 100%) is enabled, the charge pump for the IGATE driver is continuously charged. The Control3 Bit[11] (Enable IGATE Charge Pump to 100%) is disabled by default (see Table 14).

8.8 General-Purpose Comparator

The RAA489300 includes a general-purpose stand-alone comparator. The EN/CMIN pin is the non-inverting comparator input. The internal comparator reference is connected to the inverting input of the comparator and is configured by the Control0 Bit[5] (GP Comparator Input Reference) as 1.2V or 2V. The comparator output is the

INT#/ CMOUT pin, and the output polarity can be configured through Bit[4] of Control0 register (GP Comparator Output Polarity).

By default, the general-purpose comparator is disabled. This comparator can be enabled/disabled using Bit[3] of Control0 register (GP Comparator). The reference is set to 1.2V by default. For example,

- When Control0 Bit[4] = 0 for normal comparator output polarity and if CMIN > Reference, CMOUT = Low; if CMIN < Reference, CMOUT = High.
- When Control0 Bit[4] = 1 for inversed comparator output polarity and if CMIN > Reference, CMOUT = High; if CMIN < Reference, CMOUT = Low.

The general-purpose comparator output and the active-low interrupt function output (INT#) share the same pin, so either of them can pull the pin low if interrupts or the general comparator is enabled. If all interrupts are disabled, the CMOUT/INT# pin only shows the output of the general comparator. If general comparator is disabled, the pin indicates an interrupt status only.

Whether to latch the output of the general-purpose comparator can be configured in Bit[6] of Control0 register. The output of the general-purpose comparator is latched by default. To clear the latched output of the general-purpose comparator, read the 16-bit Info3 register (0x90) using the word read protocol shown in Figure 20. If Control0 Bit[6] is set to 1 (Disabled), the output of the general-purpose comparator follows the comparator result according to its input.

8.9 Current Alert

If the input or output current is higher than the current limit set by the user for 10 consecutive cycles of the RAA489300's internal counter, the input or Output Current Alert is triggered, and the INT# pin is asserted low. The Output Current Alert and Input Current Alerts are enabled by default. The Output Current Alert can be disabled by setting Control5 Bit[6], and the Input Current Alert may be disabled by setting Control5 Bit[5]. Set control5 Bit[6] to 1 to disable the Output Current Alert, and set control5 Bit[5] to 1 to disable the Input Current Alert. The Output Current Alert threshold is determined from the Output Current Limit register and Control0 Bits[10:9]. Control0 Bits[10:9] can set a percentage that is applied to the value of the Output Current Limit register that determines the threshold for the Output Current Alert. The percentages that can be set with Control0 Bits[10:9] are as follows:

- 00 = 97.5%
- 01 = 95%
- 10 = 92.5%
- 11 = 100%

For example, if the DAC value of the Output Current Limit register is set to 8192mA and the Control0 Bits[10:9] are set to 95%, the Output Current Alert threshold is 8192mA * 0.95 = 7782mA. Regardless of the settings of Control0 Bits[10:9], the DAC value of the Input Current Limit register alone determines the threshold for the Input Current Alert. Control0 Bit[8] sets the time period of the counter used for the current alert. Table 26 shows the current alert counter interval and current alert integration time according to the setting value of Control0 Bit[8] (see Table 11).

Table 26. Current Alert Integration Time, Control0 Bit[8]

Control0 Bit[8]	Current Alert Counter Interval	Current Alert Integration Time
0	25ms	250ms
1	50ms	500ms

For example, if Control0 Bit[8] is 0, the counter's cycle time interval is 25ms, and the current alert is triggered if the input or output current exceeds the input or Output Current Alert threshold for 10 consecutive cycles (250ms). To clear the current alert, read a 16-bit information3 register (0x90) using the Read-word protocol shown in Figure 20.

8.10 Current Monitoring (IMON)

The RAA489300 provides the functionality to monitor either the input or output current through the IMON pin. The specific current being monitored by the IMON pin's output voltage can be configured using Control1 Bit[5]. By default, the RAA489300 monitors the output current (see Table 12).

To monitor the input or output current, the voltage across the sensing resistor on the respective side (input or output) is used as a feedback signal. The relationship between the IMON output voltage and the voltage across the sensing resistor is defined by the following equations:

- Input current monitoring case: IMON = IMON_gain x (CSIP - CSIN)
- Output current monitoring case: IMON = IMON_gain x (CSOP - CSON)

In the equations above, IMON_gain can be set to 1x or 4x in Control1 Bit[6], and the default is 1x (see Table 12). The Current Feedback Gain is 36V/V by default, and it can be halved (18V/V) by Control Bit[7] = 1.

8.11 Analog-to-Digital Converter

The RAA489300 delivers 8-bit analog-to-digital converter (ADC) results for input voltage, output voltage, input current, and output current. The digitally converted values are stored in the ADC registers (see Table 22). The stored ADC values can be accessed using the Read-word protocol illustrated in Figure 20. The activation or deactivation of the ADC can be configured by setting the Control3 Bit[0]. If the ADC is enabled during the SLEEP state, the RAA489300 transitions to the READY state.

8.12 Auto Discharge

8.12.1 Auto-Discharge at Input Disconnection

The RAA489300 provides an auto-discharge function to discharge the input and output terminals and to discharge the Cfly, when the input is disconnected. By default, this auto-discharge is disabled. This auto-discharge can be enabled by setting Control2 register Bit[11] = 1. When the input voltage drops below the Minimum Input Voltage value (0x4B) while auto-discharge is enabled, the Minimum Input Voltage Loop Alert is triggered, auto-discharge is initiated, and the discharge is maintained for 670ms. More details about the Minimum Input Voltage Loop Alert can be found in Minimum Input Voltage Loop Alert. The discharge current of the CSIN pin and CSOP pin is 20mA by default. The discharge current can be set to 30mA by Control2 Bit[13] = 1.

The RAA489300 provides USB arcing prevention when Control3 Bit[12] = 1. When USB arc prevention is enabled and the input is disconnected, auto-discharge on CSIN and CSOP pins starts after 250µsec from the point where the input voltage drops below the Minimum Input Voltage value (0x4B).

8.12.2 Auto-Discharge at V_{OUT} DAC Change

In the case of a light load or no-load, changing the V_{OUT} DAC (0x15) might delay the output voltage response. To compensate for this, the RAA489300 provides an Auto-discharge function that discharges the output terminal (CSOP pin) when the V_{OUT} DAC is changed. This Auto-discharge function is enabled by default and can be disabled with Control2 Bit[10] = 1. If V_{OUT} DAC Slew Rate Control (Control3 Bit[15]) is enabled, the RAA489300 discharges CSOP while the VOUT DAC slews the voltage; afterwards, it continues to discharge for an additional 100µsec. A more detailed explanation of the slew rate of the output voltage DAC is in Setting Output Voltage. As described in Auto-Discharge at Input Disconnection, the discharge current can be set to 20mA or 30mA in Control2 Bit[3].

8.13 Output Short-Circuit Protection

The RAA489300 has an output short-circuit protection to prevent powering on the output into a short-circuit before moving to SWITCHING state. When the output (CSOP pin) voltage is below 0.6V, the RAA489300 sources a small current to CSOP pin to check the output short circuit. When the CSOP pin is charged above 0.6V, an internal timer starts to count. After a 10µsec debounce time of the CSOP pin voltage being above 0.6V, the RAA489300 stops sourcing small current and allows the RAA489300 to move SWITCHING state. Any time a transition occurs from the READY state back to the SWITCHING state, the small current charges the CSOP pin voltage again, and the CSOP voltage has to be charged above 0.6V to allow entering SWITCHING state again. If the CSOP pin voltage does not reach 0.6V, the RAA489300 remains in the READY state. This function is disabled by Control4 Bit[10] = 1 and is enabled by default (see Table 15).

8.14 Phase Comparator

For DCM operation, the RAA489300 detects the direction of the inductor current using a High-Side Phase Comparator (HPC) and a Low-Side Phase Comparator (LPC), which are included in the patented R3 modulator. When the output voltage is less than half the input voltage, the RAA489300 uses the LPC, and when the output voltage is half or higher than half the input voltage, it uses both the HPC and LPC. The performance of each phase comparator can be fine-tuned by adjusting parameters such as the Blanking Time, Filter Bandwidth, and Offset, which are available with the control registers. Blanking Time sets the time to ignore the voltage ringing that occurs during switching, Filter Bandwidth is a setting used to reduce the phase voltage distortion, and Offset sets the offset of the Phase Comparator. Table 27 shows the Control registers that set the LPC and HPC.

Table 27. Control Registers for Phase Comparator

Low-Side Phase Comparator	Blanking Time	Control4 Bits[9:8]
	Filter Bandwidth	Control4 Bits[7:6]
	Offset	Control4 Bits[4:2]
High-Side Phase Comparator	Blanking Time	Control4 Bits[13:12]
	Filter Bandwidth	Control4 Bit[11]
	Offset	Control1 Bits[15:12]

8.15 Faults, Interrupts, and Alerts

8.15.1 Overview

RAA489300 provides three types of error handling methods for system protection, and the three types of error handling methods are as follows:

- Fault – When a fault is triggered, the RAA489300 stops switching, the INT# pin latches low, and the Power State Machine latches the FAULT state. The Information3 register may be read to identify the specific cause of the fault. With the cause of the fault removed, reading the Information3 register clears the latched FAULT state and the INT# pin, and it restores normal functionality. Additionally, the RAA489300 provides an option to automatically clear the latched FAULT state a specified period of time after the fault trigger. By disabling the Forced Latch-off on Fault (Control2 Bit[3] = 0), the RAA489300 attempts switching operations again after maintaining the fault state for the duration specified in Control2 Bit[4]. To set a separate latch-off rule for each fault, the latch-off setting bits for each fault in Control6 must be configured while Control2 Bit[3] is set to 0 (see Table 17).
- Interrupt – When an interrupt is triggered, the RAA489300 stops switching, latches the INT# pin low, and sets the Power State Machine to the READY state. When the cause of the interrupt is removed, the power state machine returns to the SWITCHING state. However, the INT# pin remains low, and the Information3 register retains the cause of the interrupt. Read the Information3 register to determine the specific cause of the interrupt. When reading the information3 register, the latched INT# pin is cleared, and the information in the Information3 register is reset. Unlike the normal interrupts, the VINOK interrupt and Relative Output OV interrupt have exceptional behavior, and detailed descriptions thereof can be found in sections Relative Output Overvoltage Interrupt and VINOK Interrupt, respectively.
- Alert – When an Alert is triggered, unlike Fault or Interrupt scenarios, switching continues, and the state of the Power State Machine is unchanged. However, the INT# pin is latched low, and the specific cause of the alert are stored in the Information3 register. Users can ascertain the specific alert that has occurred by reading the Information3 register, and simultaneously, the latched INT# pin is cleared.

A comparison between Fault, Interrupt and Alert can be found in Table 28.

Table 28. Comparison between Fault, Interrupt and Alert[1]

	Fault	Interrupt	Alert
Switching Operation	Stop	Stop	No change
Power State Machine	FAULT state	READY state	No change
INT# Pin	Latched low	Latched low	Latched low
Recovery Option	Configurable retry timer (see Table 14)	Cause of the interrupt is removed	N/A

1. The VINOK interrupt and Relative Output OV interrupt have exceptional behavior

8.15.2 Faults

8.15.2.1 Over-Temperature Fault

The RAA489300 triggers an Over-temperature Fault when the junction temperature exceeds +150°C. When the Over-temperature Fault is triggered, the RAA489300 stops switching, the INT# pin latches low, the Power State Machine latches the FAULT state, and the Over-temperature Fault bit (Information3 Bit[15]) is set to 1. If the junction temperature remains below +120°C for 100µs after the Over-temperature Fault is triggered, the RAA489300 attempts switching operations again after maintaining the FAULT state for the duration specified in the Fault Retry Timer (Control2 Bit[4]). The latch-off only for Over-temperature Fault is set by Control6 Bit[15] = 1, and the Over-temperature Fault is disabled by Control5 Bit[15] = 1.

8.15.2.2 Way Overcurrent Fault

The RAA489300 provides Way Overcurrent Protection (WOCP) for both input and output. The voltage across the input current sensing resistor (CSIP-CSIN voltage) and the voltage across the output current sensing resistor (CSON-CSOP voltage) are monitored and compared to the WOCP threshold, and if the value is higher than the WOCP threshold, the Way Overcurrent Fault is triggered. Table 29 shows the variation of the WOCP threshold depending on the sense resistor and Current Feedback Gain settings. When the WOCP fault is triggered, the RAA489300 stops switching, the INT# pin latches low, the Power State Machine latches to the FAULT state, and the WOCP Fault bit (Information3 Bit[14]) is set to 1. The latch-off only for the WOCP Fault is set by Control6 Bit[14] = The WOCP Fault can be disabled by Control5 Bit[14] = 1.

Table 29. WOCP Threshold

WOCP	Current Feedback Gain Control1 Bit[7] (See Table 12)	Threshold [A]
Input WOCP (10mΩ Sensing Resistor)	1x (default)	16.8A
	0.5x	33.6A
Output WOCP (5mΩ Sensing Resistor)	1x (default)	33.6A
	0.5x	67.2A

8.15.2.3 Absolute Output Undervoltage Fault

The RAA489300 triggers an Absolute Output UV Fault if the output voltage drops below a VOUT Absolute Undervoltage threshold. This threshold is 1.6V by default, and it can be changed to 3.2V by setting Control1 Bit[4] = 1. *Note*: The Absolute Output UV fault is disabled until PGOOD first becomes high after POR. When the Absolute Output UV fault is triggered, the RAA489300 stops switching, the INT# pin latches low, the Power State Machine latches to the FAULT state, and the Absolute Output UV Fault bit (Information3 bit [13]) is set to 1. The latch-off only for Absolute Output UV Fault can be set by Control6 Bit[14] = 1 and the Absolute Output UV Fault can be disabled by Control5 Bit[13] = 1.

8.15.2.4 Reverse PTM Overvoltage and Undervoltage Fault

When the RAA489300 is operating as Reverse PTM, a Reverse PTM OV Fault is triggered if the voltage at the CSOP pin exceeds the upper limit of the PGOOD window, and a reverse PTM UV fault is triggered if this voltage decreases below the lower limit of the PGOOD window. The PGOOD window is based on the voltage set by the Reverse PTM voltage register (0x49). See PGOOD for details about the PGOOD window. Regardless of the Forced Latch-off on Fault bit (Control2 Bit[3]) status, when a Reverse PTM OV or UV Fault occurs, the RAA489300 turns the IGATE off, the RAA489300 enters the SLEEP state, the PTM is disabled, the Reverse OV or UV Fault bit (Information3 Bit[12]) is set to 1, and the Pass-Through Mode bit is disabled (Control0 Bit[1] = 0). The latch-off only for the Reverse PTM OV and UV Fault can be set by Control6 Bit[12] = 1. The Reverse PTM OV and UV Fault can be disabled by Control5 Bit[12] = 1.

8.15.2.5 CFLY Overvoltage and Undervoltage Fault

The RAA489300 balances the CFLY voltage using the CFLY balancer within the enhanced 3-level R3 modulator and the CFLY pre-charge function. Each of these balancers includes a CFLY OV and UV fault detector. The results from these two precursor CFLY OV and UV fault detectors are Ored together to generate a combined CFLY OV and UV fault signal.

When the CFLY voltage falls outside of a CFLY voltage window, the RAA489300 triggers a CFLY OV or UV fault. The two CFLY OV or UV fault detectors can have different CFLY OV and UV window sizes. The CFLY OV and UV window for the CFLY pre-charge function has a fixed setting of ±25%. For example, when the input is 48V and the target CFLY voltage is 24V, the OV threshold of the CFLY voltage window is 24V × (125%) = 30V and the UV threshold is 24V × (75%) = 18V. On the other hand, the CFLY OV and UV window sizes of the CFLY balancer within the enhanced 3-level R3 modulator are configured by the Control3 Bits[10:9]. For example, when Control3 Bits[10:9] = 00 (x1.5) and the input voltage is 48V, the OV threshold of the CFLY voltage window is 24V × (150%) = 36V and the UV threshold is 24V × (50%) = 12V.

Unlike other faults, the CFLY OV or UV fault has a 1msec debounce time, during which a nonlinear CFLY balancer attempts to correct the CFLY voltage imbalance. If the nonlinear CFLY balancer successfully balances the CFLY voltage to be within the CFLY window, the RAA489300 maintains the SWITCHING state and does not trigger a FAULT state. However, if the CFLY voltage is not recovered to within the CFLY voltage window despite the 1ms intervention of the nonlinear CFLY balancer, the RAA489300 triggers a CFLY OV or UV fault, stops switching, latches the INT# pin low, latches Power State Machine in the FAULT state, and sets the Information3 Bit[11] to 1. The nonlinear CFLY balancer is disabled by Control3 Bits[10:9] = 3. The latch-off only for the CFLY OV and UV Fault is set by Control6 Bit[11] = 1. The CFLY OV and UV Fault is disabled by Control5 Bit[11] = 1.

RAA489300 CFLY balancing prevents damage to the FETs by avoiding excessive voltage across the FETs. This protection is primarily applicable for USB EPR (Extended Power Range), wherein input voltages are ≥ 28V. When the input voltage is below 20V, the CFLY OV or UV faults should be disabled to prevent undesired faulting that can cause startup issues. Notably, the CFLY OV or UV fault detection should be disabled when operating in PTM mode with input voltages below 20V to prevent undesired CFLY OV or UV faults.

8.15.3 Interrupts

8.15.3.1 Absolute Output Overvoltage Interrupt

When the output voltage (CSOP pin) exceeds the V_{OUT} Absolute Overvoltage Threshold, the RAA489300 triggers an Absolute Output OV Interrupt, stops switching operations, sets the INT# pin to a low state, latches the Power State Machine to the READY state, and sets the Information3 Bit[10] to 1. The V_{OUT} Absolute Overvoltage Threshold is configured by setting Control1 Bits[3:2] as follows:

- 00 = 24V
- 01 = 33.6V
- 10 = 45.6V
- 11 = 57.6V

The Absolute Output OV Interrupt is enabled by default and can be disabled in Control5 Bit[10]. Reading the Information3 register clears the latched FAULT state and the INT# pin and restores normal functionality from the READY state.

8.15.3.2 Absolute Input Overvoltage Interrupt

When the input voltage exceeds the V_{IN} Absolute Overvoltage Threshold, 57.6V, the RAA489300 triggers an Absolute Input Overvoltage Interrupt, stops switching operations, sets the INT# pin to a low state, latches the Power State Machine to the READY state, and sets the Information3 Bit[9] to 1. The absolute Input Overvoltage Interrupt is enabled by default and can be disabled in Control5 Bit[9] = 1. Reading the Information3 register clears the latched FAULT state, clears the INT# pin, and restores normal functionality from the READY state.

8.15.3.3 Relative Output Overvoltage Interrupt

When the output voltage is higher than the upper boundary of the PGOOD window, the RAA489300 triggers a Relative Output Overvoltage Interrupt, sets the INT# pin to a low, and sets the Information3 Bit[8] to 1, but the Power State Machine keeps the SWITCHING state. The Relative Output Overvoltage Interrupt is not triggered immediately when the output voltage exceeds the PGOOD window. It is triggered after the debounce time, which can be configured by Control1 Bits[9:8]. The default debounce time is 12µsec. The Relative Output Overvoltage Interrupt is enabled by default, and it is disabled by Control5 Bit[8]. Reading the information3 register clears the INT# pin to high.

8.15.3.4 VINOK Interrupt

When the input voltage drops below the VINOK reference level, the RAA489300 triggers the VINOK Interrupt. However, unlike other interrupts, depending on the V_{IN} voltage, the Power State Machine can enter the SLEEP state instead of the READY state. Figure 31 shows which Power State Machine RAA489300 enters when the VINOK Interrupt occurs depending on the V_{IN} voltage level. If the V_{IN} voltage level is between 3.8V and VINOK reference level, the RAA489300 stops switching and enters READY state. When the V_{IN} voltage level is below 3.8V, the RAA489300 enters SLEEP state. Table 30 shows the behavior of IGATE according to V_{IN} voltage level when the IGATE Control (Control3 Bits[7:6]) is set to Auto and the VINOK interrupt occurs. When the V_{IN} voltage level is higher than 3.8V, IGATE is not turned off although the VINOK Interrupt occurs. When the VINOK Interrupt is triggered, the INT# pin is pulled low. Reading the Information3 register clears both the INT# pin to high and the Information3 register. The VINOK Interrupt is enabled by default, and it is disabled in Control5 Bit[7].

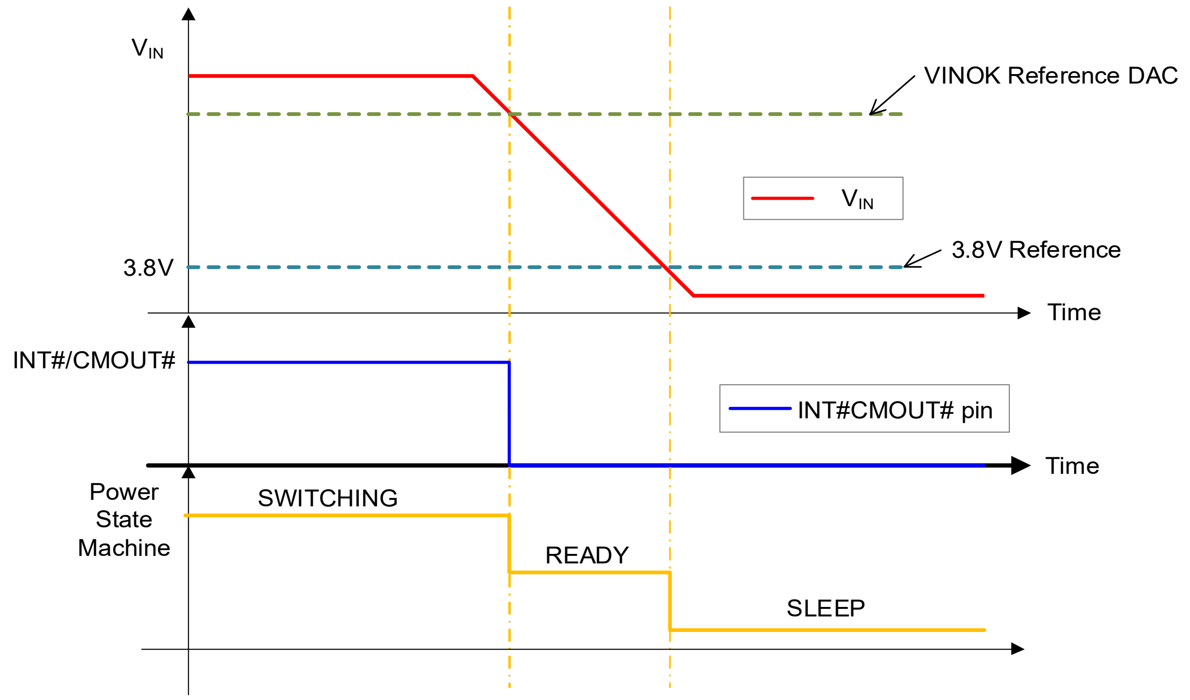


Figure 31. VINOK Interrupt Behavior

Table 30. Behavior of IGATE (According to the VIN Voltage When the VINOK Interrupt Occurs)

VINOK interrupt happens when	IGATE	
	When VINOK interrupt triggers	When the VINOK interrupt condition is cleared
3.8V < V_{IN} < VINOK Reference	Turn On	Turn On
V_{IN} < 3.8V	Turn Off	Turn On

8.15.4 Alerts

8.15.4.1 Input and Output Current Alert

If the input or output current is higher than the current limit set by the user for 10 consecutive cycles of the RAA489300's internal counter, the input or Output Current Alert is triggered and the INT# pin is asserted low. The Output Current Alert and Input Current Alerts are enabled by default. The Output Current Alert is disabled by setting Control5 Bit[6], whereas the Input Current Alert is disabled by setting Control5 Bit[5]. Set Control5 Bit[6] = 1, to disable the Output Current Alert. Set Control5 Bit[5] = 1 to disable the Input Current Alert. The Output Current Alert threshold is determined from the Output Current Limit register and Control0 Bits[10:9]. Control0 Bits[10:9] can set a percentage that is applied to the value of the Output Current Limit register that determines the threshold for the Output Current Alert. The following are percentages used with Control0 Bits[10:9]:

- 00 = 97.5%
- 01 = 95%
- 10 = 92.5%
- 11 = 100%

For example, if the DAC value of the Output Current Limit register is set to 8192mA and the Control0 Bits[10:9] are set to 95%, the Output Current Alert threshold is 8192mA × 0.95 = 7782mA. Regardless of the settings of Control0 Bits[10:9], the DAC value of the Input Current Limit register alone determines the threshold for the Input Current

Alert. Control0 Bit[8] sets the time period of the counter used for the current alert. Table 31 shows the current alert counter interval and current alert integration time according to the setting value of Control0 Bit[8] (see Table 11).

Table 31. Current Alert Integration Time, Control0 Bit[8]

Control0 Bit[8]	Current Alert Counter Interval	Current Alert Integration Time
0	25ms	250ms
1	50ms	500ms

For example, if Control0 Bit[8] is 0, the counter's cycle time interval is 25ms, and the current alert is triggered if the input or output current exceeds the input or Output Current Alert threshold for 10 consecutive cycles (250ms). To clear the current alert, read the Information3 register.

8.15.4.2 Minimum Input Voltage Loop Alert

When the input voltage drops to the Minimum Input Voltage register (0x4B) setting, the RAA489300 operates in the Minimum Input Voltage control loop to regulate the input voltage to the Minimum Input Voltage register setting. The RAA489300 informs the host controller of the Minimum Input Voltage control loop operation by pulling the INT# pin low and setting the Information3 Bit[4] to 1. This alert can be masked by Control5 Bit[4] = 1. The polarity of this alert is changed by Control6 Bit[4] = 1. When this bit sets to 1, the alert is notified only when RAA489300 exits the Minimum Input Voltage control loop.

8.15.4.3 Ready Alert

The RAA489300 can notify the host controller whenever it enters the READY state (refer to Information1 bits [11:8] for the different states) by means of pulling the INT# pin low and setting Information3 Bit[3] to 1. In this state, the RAA489300 is ready to start switching whenever the Output Voltage Register (0x15) is a non-zero value. When RAA489300 is configured to startup to the SLEEP state and the enable bit is set (Control0 Bit[0] = 1) or the EN pin is pulled high, the RAA489300 can directly go to SWITCHING state through the READY state when the output voltage register has a non-zero value in it. This alert can be masked when Control5 Bit[3] is set to 1. The polarity of this alert can be changed when Control6 Bit[3] is set to 1 so that the alert is notified only when RAA489300 exits this state.

8.15.4.4 Relative Output Under Voltage Alert

When the output voltage is lower than the lower boundary of the PGOOD window, the RAA489300 triggers a Relative Output UV Alert and the INT# pin is pulled low. In this case, the RAA489300 does not stop switching, and the Information3 Bit[2] is set to 1. Reading the Information3 register clears the Relative Output UV Alert and makes INT# high. If the Relative Output UV Alert is triggered while the GP comparator output latch is disabled (Control0 Bit[6] = 1), the INT# pin remains high.

9. Application Design Guidelines

Table 32 describes principles and rules for selecting component values to use with the RAA489300 for various applications. For the recommended component part numbers, refer to the evaluation board manual for the RAA489300. Contact local support if constraints exist that require the usage of components outside the range provided in Table 32.

Table 32. Application Design Guidelines

Number	Component	Recommended Value	Selection Criteria
1	Power Inductor	1µH	The inductor must be selected to avoid current saturation in the default operating frequency and to minimize the ripple current. A range of 680nH to 1.5µH inductors can be used if the recommended option is not available.
2	Flying Capacitor	≥20µF (Effective at $V_{IN}/2$)	The flying capacitor must be chosen to avoid its voltage ripple exceeding the CFLY OV or UV thresholds for the maximum application load current. Renesas recommends using same values MLCC capacitors to minimize the effective ESR and ESL and to help facilitate even distribution of inductor current. Because of larger ESR and ESL, polymer capacitors are not recommended for this purpose
3	Output Capacitor	≥60µF (Effective at VOUT) A	A combination of MLCC and polymer capacitors are recommended for the output capacitors. The overall ESR and ESL must be low to minimize the output ripple. The capacitor is chosen to account for optimal performance to minimize the voltage undershoot and overshoot.
4	Input Capacitor	≥15µF (Effective at Max VIN)	Renesas recommends using MLCC capacitors for the input side, while the use of a polymer capacitor is optional. When the input current control loop is used in the application, Renesas recommends splitting the total capacitance between the CSIN and CSIP nodes for optimal input current loop performance.
5	Boot Diode	-	Renesas recommends using a Schottky diode with a voltage drop lower than 0.6V. It is because the boot voltage for the Q4 MOSFET is three diode drops lower than the VDDP voltage. Renesas also recommends choosing the Schottky diodes that have a reverse leakage current lower than 10uA in the maximum ambient temperature, which avoids overloading the internal charge pumps that charge the boot voltages during startup and PTM.
6	Boot Capacitor	330nF (Effective at 10V)	Renesas recommends using a boot capacitor whose capacitance is ~ 50x the gate capacitance of the MOSFET. Use low ESR and ESL MLCC capacitors to avoid any ringing in the gate voltage during switching.
7	Power MOSFETs	-	Renesas recommends using MOSFETs that have a peak current rating of 1.5x the application RMS current. Because of the three-level topology, the low-side MOSFETs blocking voltage can be selected to block 0.85x of the maximum input voltage, while the High-side FETs must block 1x of the maximum input voltage. The Rds(on) of the MOSFETs must not be below 1.2mΩ for optimal performance of the IC's Zero Cross Detector. Renesas also recommends choosing the four FETs each with a total gate charge lower than 55nC.

10. Layout Guidelines

See Figure 32 for a layout example of RAA489300 and the power stage.

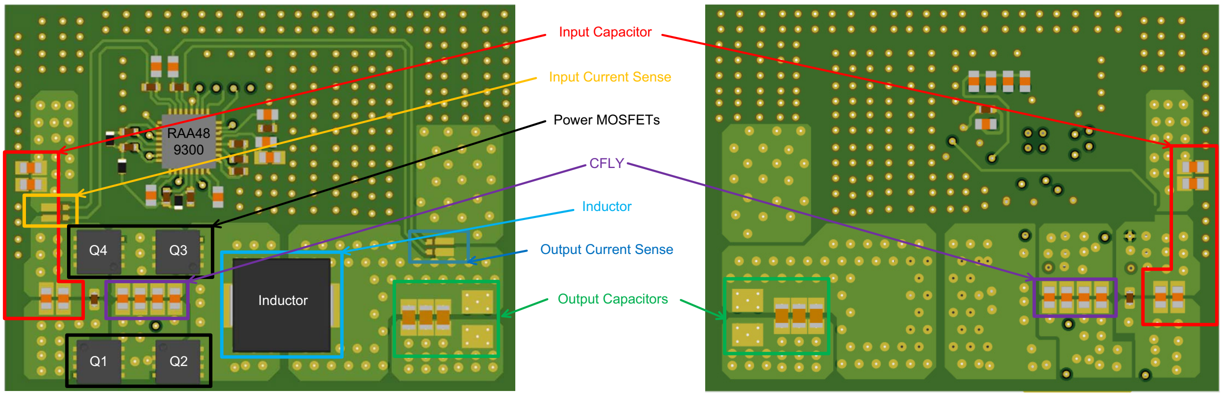


Figure 32. Example Layout of the RAA489300

An an example layout of the power stage components along with the IC is shown in Figure 32. The input, flying, and the output capacitors are split on both layers and are placed in a super-imposed fashion. The example layout shows a 6-layer PCB design with the following stack-up as shown in Table 33.

Table 33. Layer Stack-up of the Example PCB Layout

Layer	Stack
Top Layer	Components + Power planes + Signal Routing
Layer 2	Gnd Planes only
Layer 3	Signal Routing
Layer 4	Power Planes
Layer 5	GND Planes only
Bottom Layer	Components + Power planes + Signal Routing

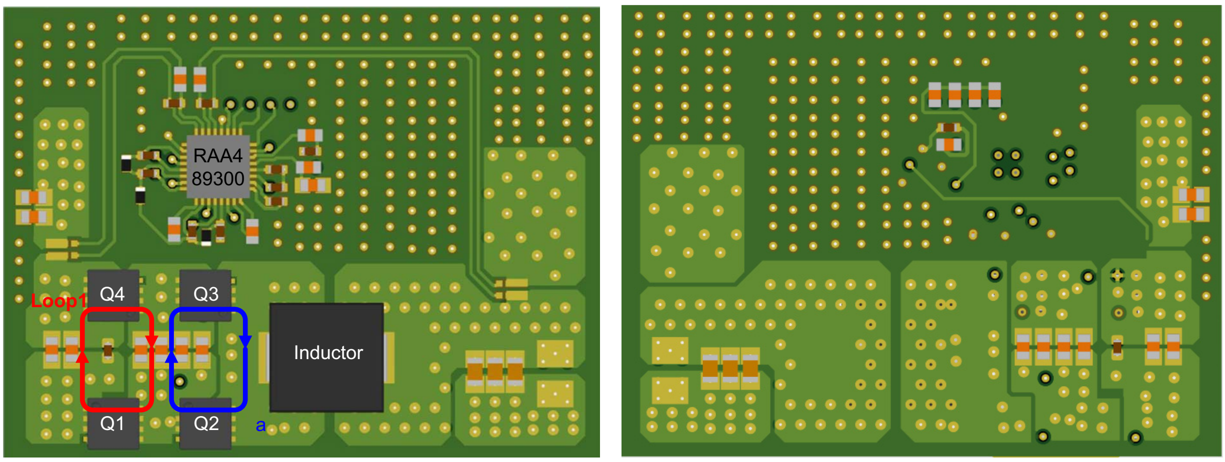


Figure 33. Top Side (left) and Bottom Side (right) of the Example Layout

The two main commutation loops that must be minimized are highlighted in the example power stage layout in Figure 33.

- Loop 1 encompasses the input capacitors, the highest side MOSFET (Q4), the flying capacitor, and the lowest side MOSFET (Q1). The impedance on this loop can be minimized by arranging the components as seen in Figure 33. The impedance can further be lowered by placing low ESR and ESL capacitors close to the drain terminal of Q4 and the source terminal of Q1.
- Loop 2 consists of the flying capacitors, Q3 MOSFET, and Q2 MOSFET. This loop can be minimized when arranged as shown in Figure 33. Generous use of stitching vias is recommended along with power planes when connecting the flying capacitors to the MOSFETs.

Renesas recommends routing the corresponding gate and source traces from the IC to the MOSFETs close to each other and in the same layer as shown in Figure 34 from the example layout. In this example, the gate and source traces are routed in Layer 4 of the PCB.

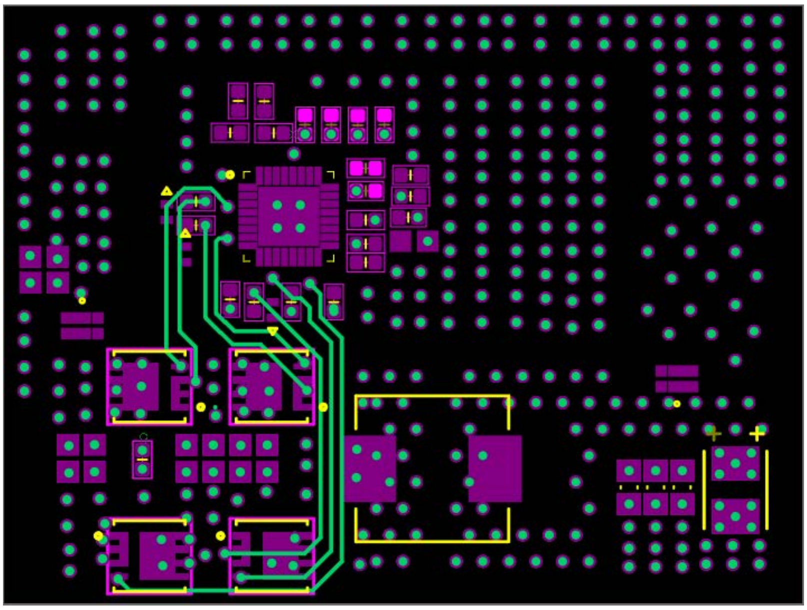


Figure 34. Gate and Source Traces from the IC to the FETs

10.1 General Guidelines for Routing the Traces to Current-Sense Resistors:

The CSIP and CSIN pins connect to the input current sense resistor along with the CSOP and CSON pins connecting to the output current sense resistor. The traces from the pins to the respective resistors must be routed in a parallel fashion to minimize any offset voltage resulting from input bias currents to the current sense amplifiers.

It is best to route the current-sensing traces through vias to connect the center of the pads, or route the traces into the pads from the inside of the current-sensing resistor. Figure 35 shows the two preferred ways of routing current-sensing traces.

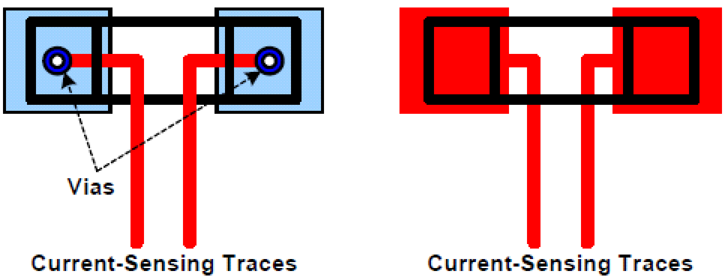


Figure 35. Recommended Routing Style for the Current Sense Traces from the Resistor Placed On: The Other Side as Controller (Left), the Same Side as Controller (Right)

Table 34. Pin-wise Layout Recommendations

Pin Number	Pin Name	Guidelines
1	IGATE	When an isolation FET is used in the application, the trace connecting the IGATE pin to the gate terminal of the isolation FET must be routed parallel to the trace connecting the ISRC pin to the source of the isolation FET. When the Isolation FET is not used, leave this pin floating.
2	ISRC	When an isolation FET is used in the application, the trace connecting the IGATE pin to the gate terminal of the isolation FET must be routed parallel to the trace connecting the ISRC pin to the source of the isolation FET. When the Isolation FET is not used, connect ISRC to GND or VDD.
3	Q4BOOT	Connect the bootstrap supply capacitor as close as possible to the Q4Boot and Q4Source pins. Avoid routing any analog signals near this trace and use sufficiently wide traces to make connections from this pin.
4	Q4GATE	The trace connecting this pin to the gate terminal of the Q4 MOSFET must be routed in parallel to the trace connecting the Q4SRC pin to the source terminal of the Q4 MOSFET. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin.
5	Q4SRC	The trace connecting the Q4SRC pin to the source terminal of the Q4 MOSFET must be routed in parallel to the trace connecting the Q4Gate pin to the gate terminal. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. This trace must also be routed in parallel to the trace connecting the CSIN pin and the current sense resistor as they form the inputs to the high-side phase comparator. It must also be ensured that this pin is directly connected to the Source pin of the MOSFET and not through a copper plane.
6	Q3BOOT	Connect the bootstrap supply capacitor as close as possible to the Q3BOOT and Q3SOURCE pins. Avoid routing any analog signals near this trace and use sufficiently wide traces to make connections from this pin.
7	Q3GATE	The trace connecting this pin to the gate terminal of the Q3 MOSFET must be routed in parallel to the trace connecting the Q3SRC pin to the source terminal of the Q3 MOSFET. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin.
8	Q3SOURCE	The trace connecting the Q3SRC pin to the source terminal of the Q3 MOSFET must be routed in parallel to the trace connecting the Q3Gate pin to its gate terminal. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. It must also be ensured that this pin is directly connected to the Source pin of the MOSFET and not through a copper plane.
9	PROG	This pin must be connected to a resistor based on the desired programming option. The resistor can be placed in general proximity to the IC.
10	Q2BOOT	Connect the bootstrap supply capacitor as close as possible to the Q2BOOT and Q2SOURCE pins. Avoid routing any analog signals near this trace and use sufficiently wide traces to make connections from this pin.
11	Q2GATE	The trace connecting this pin to the gate terminal of the Q2 MOSFET must be routed in parallel to the trace connecting the Q2SRC pin to the source terminal of the Q2 MOSFET. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin.
12	Q2SOURCE	The trace connecting the Q2SRC pin to the source terminal of the Q2 MOSFET must be routed in parallel to the trace connecting the Q2GATE pin to its gate terminal. The traces must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. It must also be ensured that this pin is directly connected to the source pin of the MOSFET and not through a copper plane.
13	VDDP	This pin must be connected to a decoupling capacitor placed close to the IC. The capacitor must have a seamless and low-impedance connection in the form of a PCB via to the GND exposed pad of the IC.
14	Q1GATE	The trace connecting this pin to the gate terminal of the Q1 MOSFET. The trace must be sufficiently wide and as short as possible. Avoid routing any analog signals near this pin. Ensure a continuous connection to GND parallel to this trace that connects to the source terminal of Q1 MOSFET.
15	GND	This pin must be connected to the ground copper plane with low impedance. Renesas recommends using four to five vias to connect to ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
16	EN/CMIN	This pin is an input signal and is recommended to be connected to a pull-down resistor placed close to the IC.
17	QPCN	The pins interface an external capacitor to the internal charge pump (QP). QPCN and QPCP are to be connected to an external capacitor which is placed close to the IC. The traces must be routed parallel to each other as the currents flowing through them are differential in nature.
18	QPCP	
19	EXT5V	Connect a decoupling capacitor to this pin. The decoupling capacitor must be placed close to the IC. The capacitor must have a seamless and low-impedance connection in the form of a PCB via to the GND exposed pad of the IC.
20	VDD	

Table 34. Pin-wise Layout Recommendations (Cont.)

Pin Number	Pin Name	Guidelines
21	VIN	Connect an RC filter to this pin from the applied input voltage source terminal. The VIN pin must be connected to the DRAIN terminal of the Isolation MOSFET when used on the input side. The decoupling capacitor must be placed close to the IC. The capacitor must have a seamless and low-impedance connection in the form of a PCB via to the GND exposed pad of the IC.
22	VCOMP	Connect the compensation components in general proximity to the IC. Ensure no digital or switching signals are routed close to these components or traces connecting them.
23	IMON	Connect an RC filter to this pin. The filter components must be placed in close proximity to the IC. This pin can be left floating when not used.
24	INT#/CMOUT#	Connect a pull-up resistor placed in general proximity to the IC. This pin can be left floating when not used.
25	SCL	Connect a pull-up resistor placed in general proximity to the IC.
26	SDA	
27	PGOOD	
28	GND	This pin must be connected to the ground copper plane with low impedance. Renesas recommends using four to five vias to connect to ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
29	CSOP	The trace connecting the CSOP pin to the current sense resistor must be routed differentially to the trace connecting the CSON pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC.
30	CSON	The trace connecting the CSOP pin to the current sense resistor must be routed differentially to the trace connecting the CSON pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC. Additionally, connect a RC filter between this pin and the current sense resistor that in placed in close proximity to the IC.
31	CSIP	The trace connecting the CSIP pin to the current sense resistor must be routed differentially to the trace connecting the CSIN pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC. Additionally, connect a RC filter between this pin and the current sense resistor that in placed in close proximity to the IC.
32	CSIN	The trace connecting the CSIP pin to the current sense resistor must be routed differentially to the trace connecting the CSIN pin to the resistor. Connect a differential capacitor between the pins in close proximity to the IC.

11. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

12. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg #	Carrier Type [4]	Temp. Range
RAA489300ARGNP#AA0	489300 ARGNPA	32 Ld 4x4 TQFN	L32.4x4D	Tray	-10 to +100°C
RAA489300ARGNP#HA0				Reel, 6k	
RAA489300A3GNP#AA0	489300 A3GNPA			Tray	-40 to +105°C
RAA489300A3GNP#HA0				Reel, 6k	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL) rating see the RAA489300 product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

13. Revision History

Revision	Date	Description
2.00	Oct 28, 2025	Updated the Device ID default in Table 1. In Thermal Specifications, updated θ_{JA} from 37 to 38.
1.02	Aug 13, 2025	Updated section 8.6 PGOOD in the first and second paragraph. Updated section 8.15.2.5 CFLY Overvoltage and Undervoltage Fault by adding the last paragraph. Updated POD to the latest revision.
1.01	Apr 17, 2025	Updated the Absolute Maximum Ratings for Q2BOOT-Q2SRC, Q3BOOT-Q3SRC, Q4BOOT-Q4SRC, and VDDP. Added ECAD Information.
1.00	Feb 18, 2025	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RAA489300ARGNP#AA0	32	TQFN	L32.4x4D
RAA489300ARGNP#HA0	32	TQFN	L32.4x4D
RAA489300A3GNP#AA0	32	TQFN	L32.4x4D
RAA489300A3GNP#HA0	32	TQFN	L32.4x4D

A.2 Symbol Pin Information

A.2.1 32-TQFN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	IGATE	Output	-
2	ISRC	Power	-
3	Q4BOOT	Power	-
4	Q4GATE	Output	-
5	Q4SRC	Power	-
6	Q3BOOT	Power	-
7	Q3GATE	Output	-
8	Q3SRC	Power	-
9	PROG	Input	-
10	Q2BOOT	Power	-
11	Q2GATE	Output	-
12	Q2SRC	Power	-
13	VDDP	Power	-
14	Q1GATE	Output	-
15	GND	Power	-
16	EN	Input	CMIN
17	QPCN	Power	-
18	QPCP	Power	-
19	EXT5V	Input	-
20	VDD	Power	-
21	VIN	Input	-
22	COMP	Output	-
23	IMON	Output	-
24	INT#	Output	CMOUT#
25	SCL	I/O	-
26	SDA	I/O	-
27	PGOOD	Output	-
28	GND	Power	-
28	CSOP	Input	-
30	CSON	Input	-
31	CSIP	Input	-
32	CSIN	Input	-
EPAD33	GND	Power	-

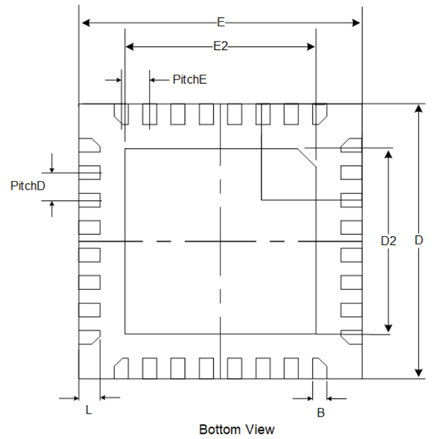
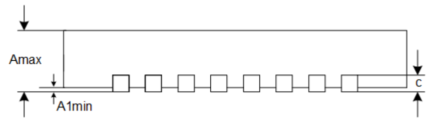
A.3 Symbol Parameters

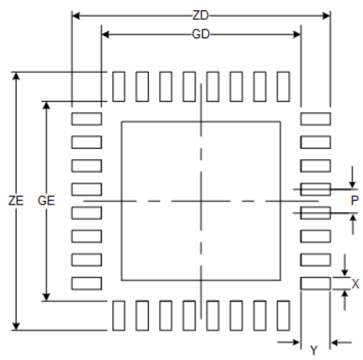
Orderable Part Number	Qualification	Mounting Type	Min Input Voltage	Max Input Voltage	Min Output Voltage	Max Output Voltage	Min Operating Temperature	Max Operating Temperature	Max Junction Temperature (Tj)	RoHS	Typ Switching Frequency	Switcher Configuration
RAA489300ARGNP#AA0	Consumer	SMD	4.5 V	57.6 V	3 V	54.912 V	-10 °C	+100 °C	+125 °C	Compliant	300 kHz	3-level buck
RAA489300ARGNP#HA0	Consumer	SMD	4.5 V	57.6 V	3 V	54.912 V	-10 °C	+100 °C	+125 °C	Compliant	300 kHz	3-level buck
RAA489300A3GNP#AA0	Industrial	SMD	4.5 V	57.6 V	3 V	54.912 V	-40 °C	+105 °C	+125 °C	Compliant	300 kHz	3-level buck
RAA489300A3GNP#HA0	Industrial	SMD	4.5 V	57.6 V	3 V	54.912 V	-40 °C	+105 °C	+125 °C	Compliant	300 kHz	3-level buck

A.4 Footprint Design Information

A.4.1 32-TQFN

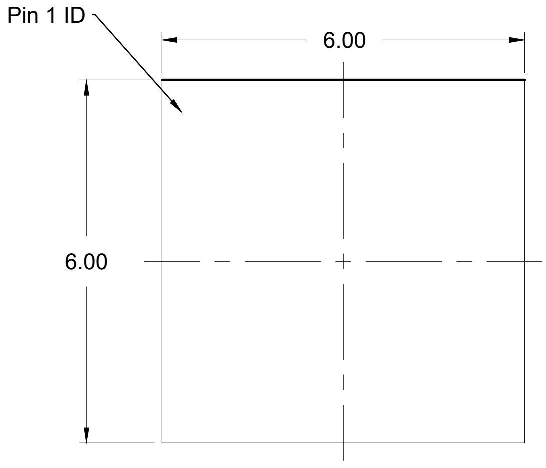
IPC Footprint Type	Package Code/ POD Number	Number of Pins
QFN	L32.4x4D	32

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	3.90	 Bottom View
Maximum body span (vertical side)	Dmax	4.10	
Minimum body span (horizontal side)	Emin	3.90	
Maximum body span (horizontal side)	Emax	4.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.25	
Maximum Lead Length	Lmax	0.35	
Number of pins (vertical side)	PinCountD	8	
Number of pins (horizontal side)	PinCountE	8	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.4	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.4	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	2.6	
Maximum thermal pad size (vertical side)	D2max	2.8	
Minimum thermal pad size (horizontal side)	E2min	2.6	
Maximum thermal pad size (horizontal side)	E2max	2.8	 Side View
Maximum Height	Amax	0.8	
Minimum Standoff Height	A1min	0	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

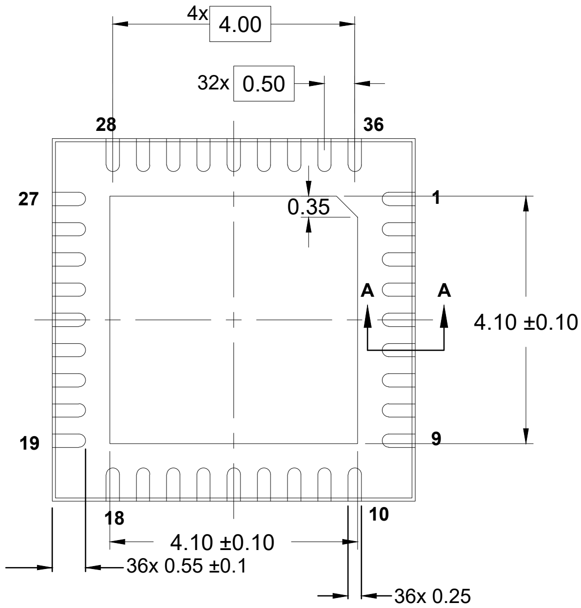
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	4.4	 PCB Top View
Distance between top pad toe to bottom pad toe (vertical side)	ZD	4.4	
Distance between left pad heel to right pad heel (horizontal side)	GE	3.4	
Distance between top pad heel to bottom pad heel (vertical side)	GD	3.4	
Pad Width	X	0.2	
Pad Length	Y	0.5	

Package Outline Drawing

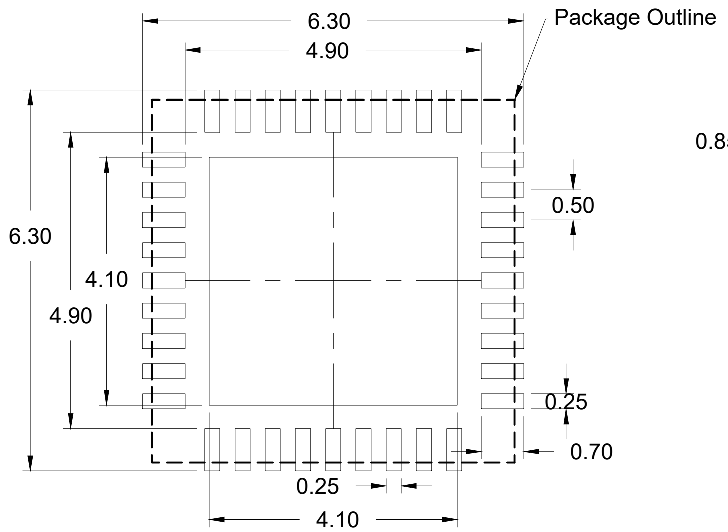
L36.6x6D
SQ0036AA
36 Lead Step Cut Quad Flat N0-Lead Plastic Package (SCQFN)
Rev.01, Aug 29, 2025



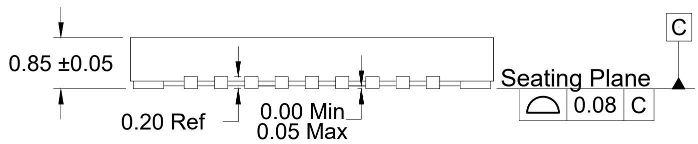
Top View



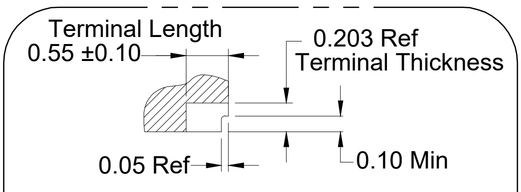
Bottom View



Recommended Land Pattern



Side View



Section: A-A
Scale: NTS

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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