RAA489800

Bidirectional Buck-Boost Voltage Regulator

The RAA489800 is a bidirectional, buck-boost voltage regulator that provides buck-boost voltage regulation and protection features. The advanced Renesas R3™ Technology provides high light-load efficiency, fast transient response, and seamless DCM/CCM transitions.

The RAA489800 takes input power from a wide range of DC power sources up to 23V (such as conventional AC/DC adapters (ADP), USB PD ports, travel ADP) and safely converts it to a regulated voltage up to 21V. The RAA489800 can also convert a wide range DC power source connected at its output (system side) to a regulated voltage to its input (ADP side). This bidirectional buck-boost regulation feature makes the RAA489800's application very flexible. In addition to 4-switch buck-boost configuration, it can also support 2-switch Buck mode operation.

The RAA489800 includes various system operation functions such as the Forward mode enable pin, Reverse mode enable pin, programmable soft-start time, and adjustable forward and reverse V_{OUT}. It also has forward and reverse power-good indicators. The protection functionalities include OCP, OVP, UVP, and OTP.

The RAA489800 has serial communication through SMBus/I^2C that allows programming of many critical parameters to deliver a customized solution. These programming parameters include, but are not limited to: output current limit, input current limit, and output voltage setting.

Features

- Bidirectional buck, boost, and buck-boost operation
- Configurable for 4-switch buck-boost or 2-switch buck operation
- Input voltage range: 3.8V to 23V (no dead zone)
- Output voltage: up to 21V
- Up to 1MHz switching frequency
- Pin programmable soft-start time
- LDO output for VDD and VDDP
- System FAULT status ALERT function
- Input/output internal discharge function
- Active switching for negative voltage transitions
- Pass Through mode in both directions
- Forward and Reverse mode enable pins
- OCP, OVP, UVP, and OTP protection
- Absolute overvoltage protection
- SMBus and auto-increment I^2C compatible
- Pb-free (RoHS compliant)
- 32 Ld 4x4 TQFN package
- UL 2367, IEC 62368-1: File No. E520109

Applications

- Tablets, Ultrabooks, power banks, mobile devices, and USB-C

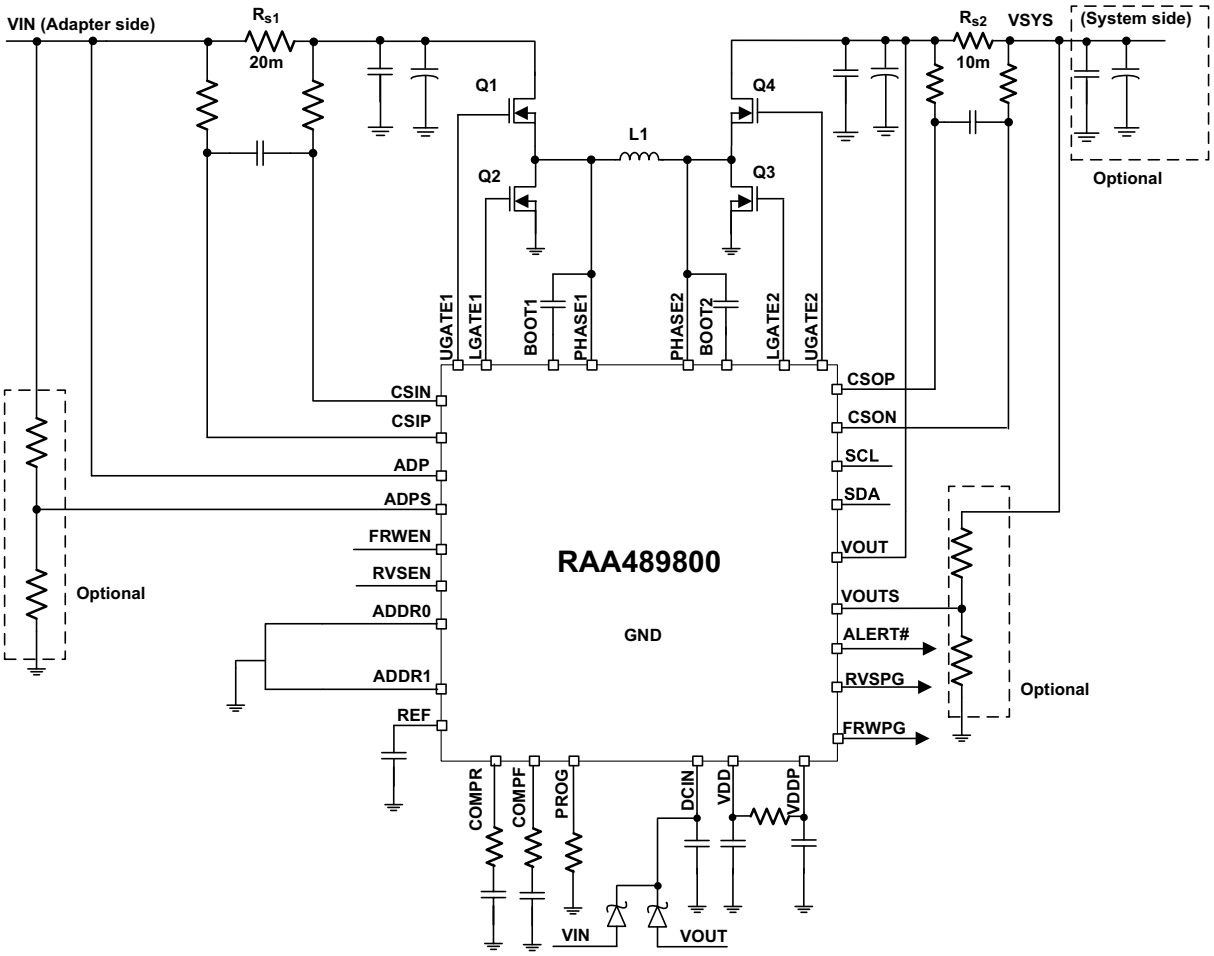


Figure 1. Typical Application Circuit in 4-Switch Buck-Boost Configuration

Contents

1. Overview

1.1 Simplified Application Circuit

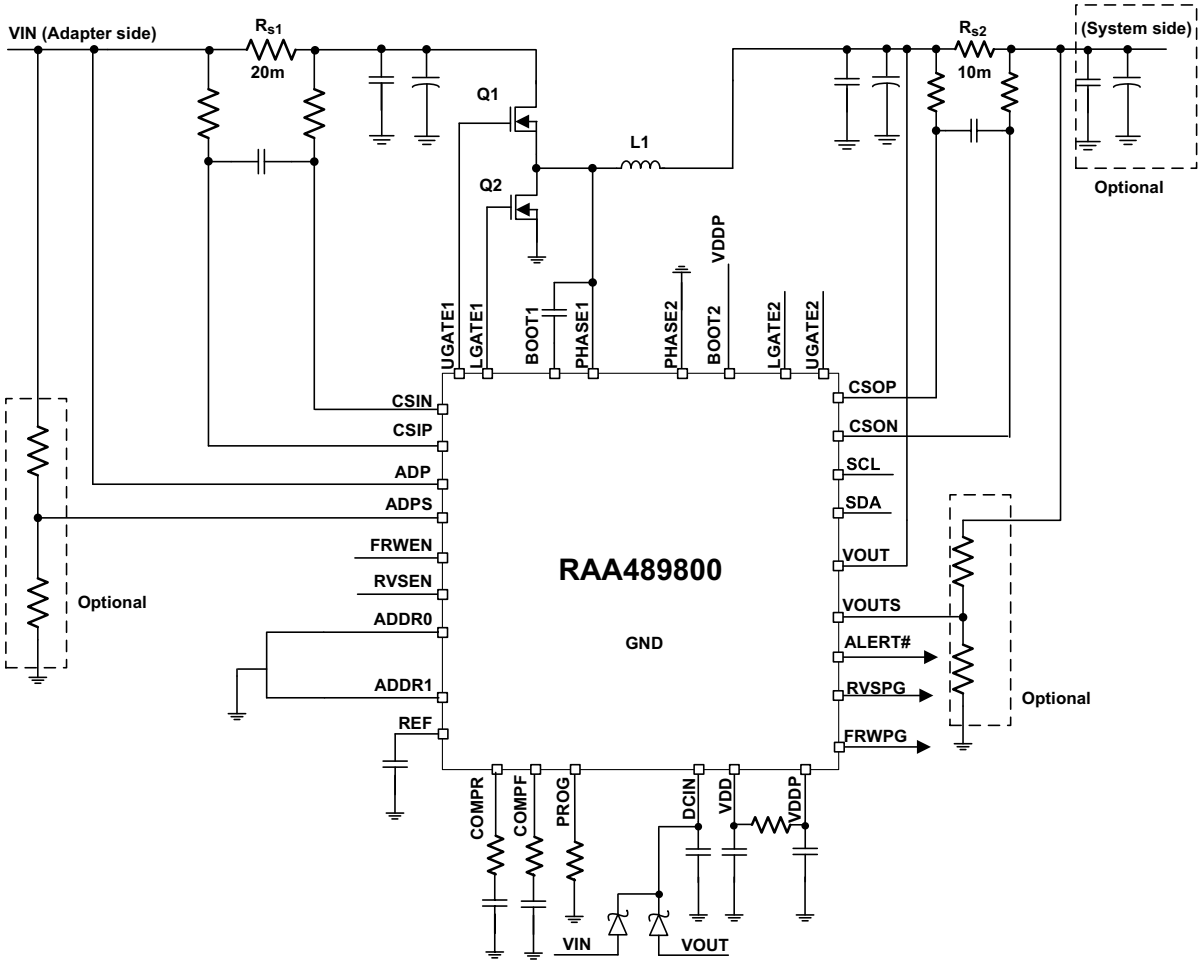


Figure 2. Typical Application Diagram in 2-Switch Buck Configuration

1.2 Block Diagram

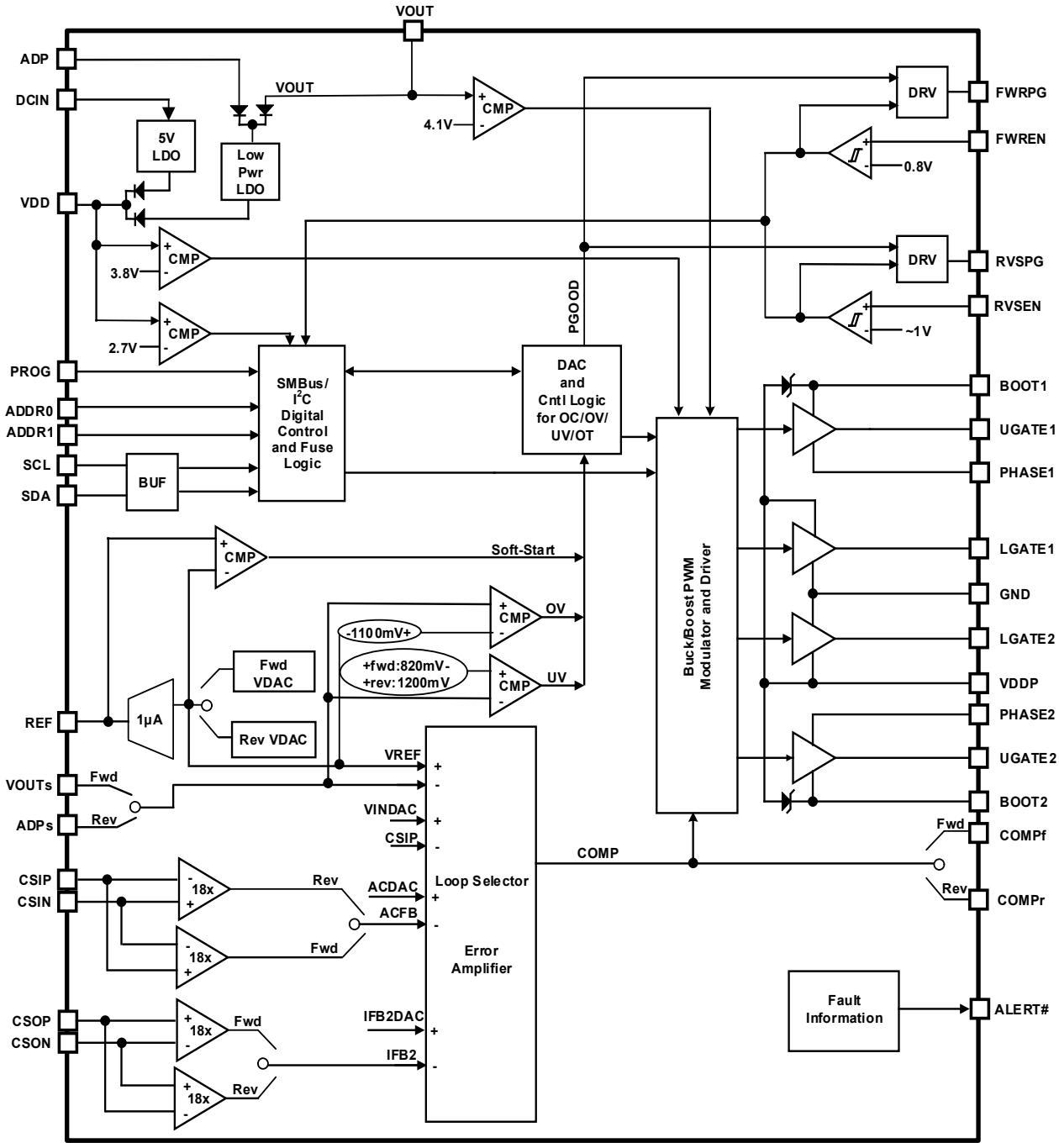


Figure 3. Block Diagram

1.3 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type (Note 1)	Temp. Range
RAA489800ARGNP#AA0	489800 ARGNPA	32 Ld 4x4 TQFN	L32.4x4D	Tube	-10 to +100°C
RAA489800ARGNP#HA0				Reel, 6k	
RAA489800A2GNP#AA0	489800 A2GNPA			Tube	-40 to +85°C
RAA489800A2GNP#HA0				Reel, 6k	
RTKA489800DE0000BU	Evaluation board				

Notes:

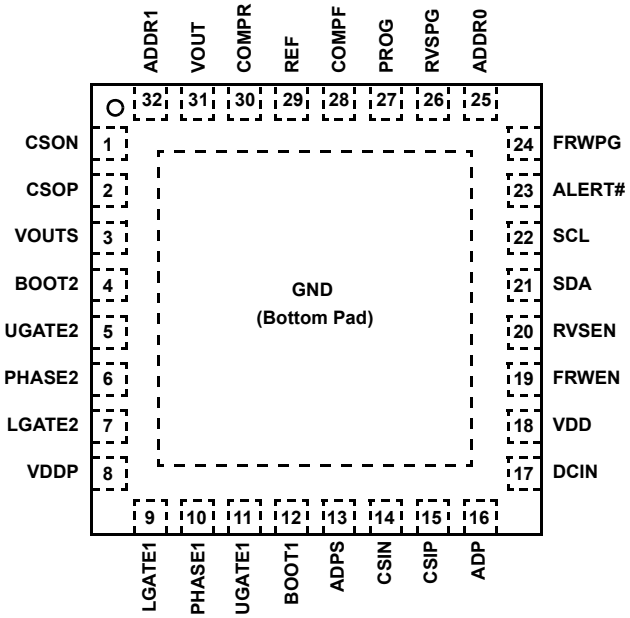
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. The Moisture Sensitivity Level (MSL) rating is 3. For more information about MSL, see TB363.

Table 1. Key Differences Between Family of Parts

Part Number	Absolute Overvoltage Protection	Buck-Boost Efficiency Improvement	Pin #23 Function	Input/ Output Current PROCHOT#	CC/CV Loop ALERT#	2-FET Buck Only Mode	Forced Buck-Boost and Boost Mode	VSYS Low Shutdown Feature	Default Input Current Limit Setting Trough PROG pin
RAA489800	Yes	5%	ALERT#	No	Yes	Yes	No	Yes	Yes
RAA489801	Yes	5%	PROCHOT#	Yes	No	Yes	Yes	No	Yes
ISL95338	No	N/A	PROCHOT#	Yes	No	No	Yes	No	No

1.4 Pin Configuration

32 Ld 4x4 TQFN
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Description
Bottom Pad	GND	Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. GND should also be used as the thermal pad for heat dissipation.
1	CSON	Forward V_{OUT} current sense negative input. Connect to the VOUT current resistor negative input. Place a 0.1µF ceramic capacitor between CSOP and CSON to provide differential mode filtering.
2	CSOP	Forward V_{OUT} current sense positive input. Connect to the VOUT current resistor positive input. Place a 0.1µF ceramic capacitor between CSOP and CSON to provide differential mode filtering.
3	VOUTS	Forward VSYS feedback voltage. Use an optional resistor divider externally to configure forward VSYS voltage.
4	BOOT2	High-side MOSFET Q4 gate driver supply. Connect an MLCC capacitor across the BOOT2 pin and the PHASE2 pin. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT2 pin when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode.
5	UGATE2	High-side MOSFET Q4 gate drive.
6	PHASE2	Current return path for the high-side MOSFET Q4 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q4 source, the low-side MOSFET Q3 drain, and the inductor output terminal.
7	LGATE2	Low-side MOSFET Q3 gate drive.
8	VDDP	Power supply to the gate drivers. Connect to the VDD pin through a 4.7Ω resistor and connect a 2.2µF ceramic capacitor to GND. The effective capacitance at 5V must be at least 0.4µF after derating.
9	LGATE1	Low-side MOSFET Q2 gate drive.
10	PHASE1	Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and the input terminal of the inductor.
11	UGATE1	High-side MOSFET Q1 gate drive.
12	BOOT1	High-side MOSFET Q1 gate driver supply. Connect an MLCC capacitor across the BOOT1 pin and the PHASE1 pin. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT1 pin when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode.
13	ADPS	Reverse output voltage feedback. Use a resistor divider externally to configure the reverse output voltage.
14	CSIN	ADP current sense negative input.
15	CSIP	ADP current sense positive input. The modulator also uses this for sensing input voltage in Forward mode and output voltage in Reverse mode.
16	ADP	Senses ADP voltage. Forward mode can be enabled when the ADP voltage is higher than 4.1V. The ADP pin is also one of the two internal low power LDO inputs.
17	DCIN	Internal LDO input providing power to the IC. Connect a diode OR from the ADP and system outputs. Connect a 4.7µF ceramic capacitor to GND. The effective capacitance at 20V must be at least 0.4µF after derating.
18	VDD	Internal LDO output that provides the bias power for the internal analog and digital circuit. Connect a 2.2µF ceramic capacitor to GND. The effective capacitance at 5V must be at least 0.4µF after derating. If V_{DD} is pulled below 2.7V, the RAA489800 resets all the SMBus registers to their default values.
19	FRWEN	Forward mode enable, analog signal input. Forward mode is valid if the FRWEN pin voltage is greater than 0.6V.
20	RVSEN	Reverse mode enable, digital signal input. Reverse mode is valid if the signal is “1” (logic high), otherwise, Reverse mode is disabled.
21	SDA	SMBus data I/O. Connect to the data line from the host controller. Connect a 10k pull-up resistor according to the SMBus specification.
22	SCL	SMBus clock I/O. Connect to the clock line from the host controller. Connect a 10k pull-up resistor according to the SMBus specification.
23	ALERT#	Open-drain output. If WOC, OV, UV, OTP, or ADPOV faults are detected, ALERT# is pulled low. Clear ALERT# with Control4<1>. If ALERT# is asserted, Table 9 on page 26 shows which fault information bits are set. Configure ALERT# behavior with Control2<10:9>, Control4<7>, and Control4<1>.
24	FRWPG	Open-drain output. Indicator output to indicate the forward modulator is enabled and in regulation.

Pin Number	Pin Name	Description
25	ADDR0	Address setting pin for the IC. The IC address is set by the ADDR0 and ADDR1 logic voltage levels.
26	RVSPG	Open-drain output. Indicator output to indicate the reverse modulator is enabled and in regulation.
27	PROG	A resistor from the PROG pin to GND sets the default forward system output voltage.
28	COMPF	Forward mode error amplifier output. Connect a compensation network externally from COMPF to GND.
29	REF	Output voltage soft-start reference. It also sets the slew rate for output voltage changes. A ceramic capacitor from REF to GND is set to the desired soft-start time. The forward output voltage (VOUTS) reference soft-start time is set in Forward mode. The reverse output voltage (ADPS) reference soft-start time is set in Reverse mode.
30	COMPR	Reverse mode error amplifier output. Connect a compensation network externally from COMPR to GND.
31	VOUT	Forward V_{OUT} sense voltage for modulator and PHASE 2 zero-current comparator.
32	ADDR1	Address setting pin for the IC. The IC address is set by the ADDR0 and ADDR1 logic voltage levels.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
CSIP, CSIN, ADPS, ADP, DCIN	-0.3	+28	V
CSIP	-0.3	ADP + 2	V
PHASE1	GND - 0.3	+28	V
PHASE1	GND - 2 (<20ns)	+28	V
UGATE1	PHASE1 - 0.3	BOOT1 + 0.3	V
PHASE2	GND - 0.3	+28	V
PHASE2	GND - 2 (<20ns)	+28	V
UGATE2	PHASE2 - 0.3	BOOT2 + 0.3	V
LGATE1, LGATE2	GND - 0.3	VDDP + 0.3	V
LGATE1, LGATE2	GND - 2 (<20ns)	VDDP + 0.3	V
VOUT, VOUTS, CSOP, CSON	-0.3	+24	V
VDD, VDDP	-0.3	+6.5	V
BOOT1	GND - 0.3	PHASE1 + 6.5	V
BOOT2	GND - 0.3	PHASE2 + 6.5	V
BOOT1 - PHASE1, BOOT2 - PHASE2	-0.3	+6.5	V
COMPR, COMPF, REF, PROG	-0.3	VDD + 0.3	V
RVSEN, FRWEN, ADDR0, ADDR1	-0.3	+6.5	V
FRWPG, ALERT#, RVSPG	-0.3	+6.5	V
SCL, SDA	-0.3	+6.5	V
CSIP-CSIN, CSOP-CSON	-0.3	+0.3	V
RVSEN, FRWEN, SDA, SCL, FRWPG, RVSPG, ALERT#		2	mA
ESD Rating	**Rating**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld TQFN Package (Notes 4, 5)	37	2

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the ceramic on the package underside.

Parameter	Minimum	Maximum	Unit
Junction Temperature Range (T_J)	-10	+125	°C
Storage Temperature Range (T_S)	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
ADP Input Voltage	4	23	V
V_{OUT} Input Voltage	4	21	V

2.4 Electrical Specifications

Operating conditions: ADP = CSIP = CSIN = 20V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the ambient temperature range, -40°C to +100°C unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
UVLO/ACOK						
VADP UVLO Rising	VADP_UVLO_r		**3.9**	4.2	**4.55**	V
VADP UVLO Hysteresis	VADP_UVLO_h			530		mV
V_{OUT} UVLO Rising	VOUT_UVLO_r		**3.9**	4.2	**4.55**	V
V_{OUT} UVLO Hysteresis	VOUT_UVLO_h			300		mV
VDDA 2P7 Rising, SMBus Active (Note 7)	VDD_2P7_r		**2.5**	2.7	**2.9**	V
VDDA 2P7 POR Hysteresis (Note 7)	VDD_2P7_h			150		mV
VDDA 3P8 POR Rising, Modulator, and Gate Driver Active	VDD_3P8_r		**3.6**	3.8	**3.9**	V
V_{DD} 3P8 Hysteresis	VDD_3P8_h			150		mV
FRWEN Rising	FRWEN_r		**0.48**	0.625	**0.77**	V
FRWEN Hysteresis	FRWEN_h			20		mV
Bias Current						
Forward Supply Current, Disable State		ADP, ADPS CSIN, CSIP, VDDP, DCIN = 5V, FWREN = High, Control4<6> = High		120	**200**	µA
Reverse Supply Current, Disable State		V_{OUT}, VOUTS CSON, CSOP, VDDP, DCIN = 5V, RVSEN = Low		70	**120**	µA
Forward Supply Current, Enable State		ADP, ADPS CSIN, CSIP, DCIN = 20V, FWREN = High		3000	**3350**	µA
Reverse Supply Current, Enable State		VOUT, VOUTS CSON, CSOP, DCIN = 20V, RVSEN = High		3000	**3350**	µA
Forward Supply Current, Enable State		DCIN only (does not include gate driver current)		1600	**1900**	µA
Reverse Supply Current, Enable State		DCIN only (does not include gate driver current)		1500	**1700**	µA
Linear Regulator						
VDDA Output Voltage	V_{DD}	6V < V_{ADP} < 23V, no load	**4.5**	5.1	**5.5**	V
VDDA Dropout Voltage	VDD_dp	30mA, V_{DCIN} = 4V		100		mV
VDD Overcurrent Threshold	VDD_OC		**90**	135	**175**	mA

Operating conditions: ADP = CSIP = CSIN = 20V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the ambient temperature range, -40°C to +100°C unless otherwise specified. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
ADP Current Regulation, R_{ADP} = 20mΩ						
Input Current Accuracy		|CSIP - CSIN| = 80mV		4		A
			-3		**+3**	%
		|CSIP - CSIN| = 40mV		2		A
			-4		**+4**	%
		|CSIP - CSIN| = 10mV		0.5		A
			-10		**+10**	%
Voltage Regulation						
Output Voltage Accuracy Forward (-10°C to +100°C)		Measured at VOUTS, 5V and up	**-1**		**+1**	%
		Measured at VOUTS, 4V to 5V	**-1.5**		**+1.5**	%
Output Voltage Accuracy Reverse (-10°C to +100°C)		Measured at ADPS, 5V and up	**-2**		**+2**	%
		Measured at ADPS, 4V to 5V	**-2.5**		**+2.5**	%
Output Voltage Accuracy Forward (-40°C to +85°C)		Measured at VOUTS, 5V and up	**-1.5**		**+1.5**	%
		Measured at VOUTS, 4V to 5V	**-2**		**+2**	%
Output Voltage Accuracy Reverse (-40°C to +85°C)		Measured at ADPS, 5V and up	**-2.5**		**+2.5**	%
		Measured at ADPS, 4V to 5V	**-3.5**		**+3.5**	%
Minimum Input Voltage Accuracy		Measured at ADPS	**-3**		**+3**	V
VOUT Current Regulation, Rs2 = 10mΩ						
V_{OUT} Current Accuracy		|CSOP - CSON| = 60mV		6		A
			-3		**+3**	%
		|CSOP - CSON| = 20mV		2		A
			-5		**+5**	%
		|CSOP - CSON| = 10mV		1		A
			-10		**+10**	%
		|CSOP - CSON| = 5mV		0.5		A
			-20		**+20**	%
ADP Current-Sense Amplifier, R_{ADP} = 20mΩ						
CSIP/CSIN Input Voltage Range	$V_{CSIP/N}$		**0**		**27**	V
RVSEN						
High-Level Input Voltage			**0.9**			V
Low-Level Input Voltage					**0.35**	V
ALERT#, RVSPG, FWRPG						
Output Sinking Current		Pin at 0.4V	**15**	40	**65**	mA
Leakage Current					**1**	µA
ALERT#						
ALERT# Debounce Time (Note 7)		ALERT# Debounce register	**-15**		**15**	%

Operating conditions: ADP = CSIP = CSIN = 20V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the ambient temperature range, -40°C to +100°C unless otherwise specified. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Protection						
ADP Overvoltage Rising Threshold		Forward mode	**25.5**	26.4	**27.5**	V
VSYS Absolute Overvoltage Rising Threshold			**22.5**	23.5	**24**	V
VSYS Absolute Overvoltage Hysteresis				0.65		V
VOUTS Overvoltage Rising Threshold		Forward mode VOUTS - 12xREF	**0.85**	1.1	**1.45**	V
VOUTS Overvoltage Hysteresis				0.55		V
ADPS Overvoltage Rising Threshold		Reverse mode ADPS - 12xREF	**0.9**	1.2	**1.5**	V
ADPS Overvoltage Hysteresis				0.6		V
Over Current Warning Threshold		Forward Mode at 4A	**90**		**110**	%
VSYS Low Voltage Shutdown Threshold		Control0<4> = 1, Control0<3> = 0	**2.8**	3	**3.3**	V
		Control0<4> = 1, Control0<3> = 1	**3.1**	3.3	**3.6**	V
VOUTS Undervoltage Falling Threshold		Forward mode VOUTS - 12xREF	**-1.15**	-0.85	**-0.55**	V
VOUTS Undervoltage Hysteresis				0.6		V
ADPS Undervoltage Falling Threshold		Reverse mode ADPS - 12xREF	**-1.55**	-1.2	**-0.85**	V
ADPS Undervoltage Hysteresis				0.4		V
Over-Temperature Threshold (Note 7)			**140**	150	**160**	°C
Oscillator						
Oscillator Frequency, Digital Core Only			**0.85**	1	**1.15**	MHz
Digital Debounce Time Accuracy		PV Debounce and UV Debounce for FWRPG and RVSPG delay	**-15**		**15**	%
Miscellaneous						
Switching Frequency Accuracy		All programmed f_{SW} settings, CCM, and no period stretching	**-15**		**15**	%
ADP Discharge Current		ADP = 5V		22		mA
V_{OUT} Discharge Current		V_{OUT} = 5V		22		mA
REF Pin Source Current		Control1 <3> = 0	**1**	1.8	**2.9**	µA
REF Pin Sink Current		Control1 <3> = 0	**1.2**	2	**3**	µA
REF Pin Fast Sink Current		Control1 <3> = 1		2		µA
REF Pin Fast Source Current		Control1 <3> = 1		20		µA
SMBus						
SDA/SCL Input Low Voltage					**0.7**	V
SDA/SCL Input High Voltage			**1.5**			V
SDA/SCL Input Bias Current					**1**	µA
SDA, Output Sink Current (Note 7)		SDA = 0.4V	**4**			mA
SMBus Frequency	f_{SMB}		**10**		**400**	kHz

Operating conditions: ADP = CSIP = CSIN = 20V, VOUTS = VOUT = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the ambient temperature range, -40°C to +100°C unless otherwise specified. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Gate Driver						
UGATE1 Pull-Up Resistance	$UG1_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE1 Source Current	$UG1_{SRC}$	UGATE1 - PHASE1 = 2.5V	**1.3**	2		A
UGATE1 Pull-Down Resistance	$UG1_{RPD}$	100mA sink current		350	**475**	mΩ
UGATE1 Sink Current	$UG1_{SNK}$	UGATE1 - PHASE1 = 2.5V	**1.9**	2.8		A
LGATE1 Pull-Up Resistance	$LG1_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE1 Source Current	$LG1_{SRC}$	LGATE1 - GND = 2.5V	**1.3**	2		A
LGATE1 Pull-Down Resistance	$LG1_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE1 Sink Current	$LG1_{SNK}$	LGATE1 - GND = 2.5V	**2.3**	3.5		A
LGATE2 Pull-Up Resistance	$LG2_{RPU}$	100mA source current		800	**1200**	mΩ
LGATE2 Source Current	$LG2_{SRC}$	LGATE2 - GND = 2.5V	**1.3**	2		A
LGATE2 Pull-Down Resistance	$LG2_{RPD}$	100mA sink current		300	**450**	mΩ
LGATE2 Sink Current	$LG2_{SNK}$	LGATE2 - GND = 2.5V	**2.3**	3.5		A
UGATE2 Pull-Up Resistance	$UG2_{RPU}$	100mA source current		800	**1200**	mΩ
UGATE2 Source Current	$UG2_{SRC}$	UGATE2 - PHASE2 = 2.5V	**1.3**	2		A
UGATE2 Pull-Down Resistance	$UG2_{RPD}$	100mA sink current		300	**450**	mΩ
UGATE2 Sink Current	$UG2_{SNK}$	UGATE2 - PHASE2 = 2.5V	**2.3**	3.5		A
UGATE1 to LGATE1 Dead Time	$t_{UG1LG1DEAD}$		**10**	20	**40**	ns
LGATE1 to UGATE1 Dead Time	$t_{LG1UG1DEAD}$		**10**	20	**40**	ns
LGATE2 to UGATE2 Dead Time	$t_{LG2UG2DEAD}$		**10**	20	**40**	ns
UGATE2 to LGATE2 Dead Time	$t_{UG2LG2DEAD}$		**10**	20	**40**	ns

Notes:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

2.5 SMBus Timing Specification

Parameters	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
SMBus Frequency	f_{SMB}		10		400	kHz
Bus-Free Time	t_{BUF}		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
Stop Condition Setup Time from SCL	$t_{SU:STO}$		4			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SCL Low Period	t_{LOW}		4.7			µs
SCL High Period	t_{HIGH}		4			µs
SMBus Inactivity Timeout		Maximum charging period without an SMBus Write to MaxSystemVoltage or ADPCurrent register		175		s

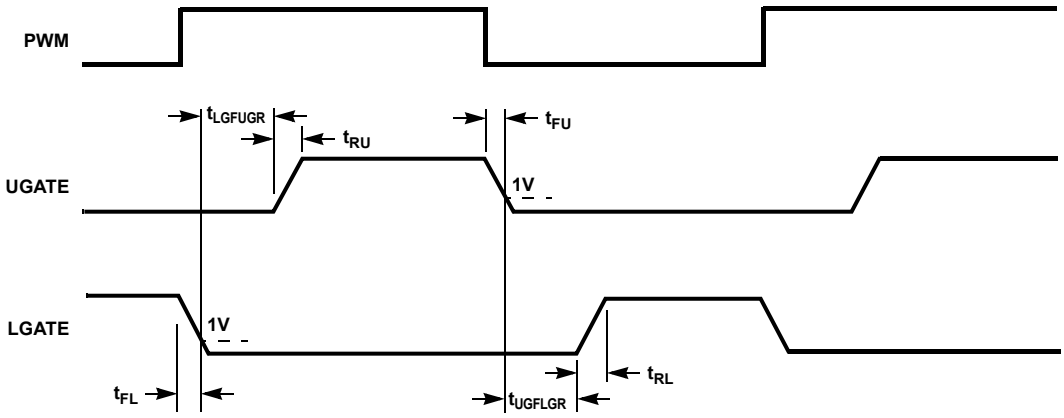


Figure 4. Gate Driver Timing Diagram

3. Typical Performance Curves

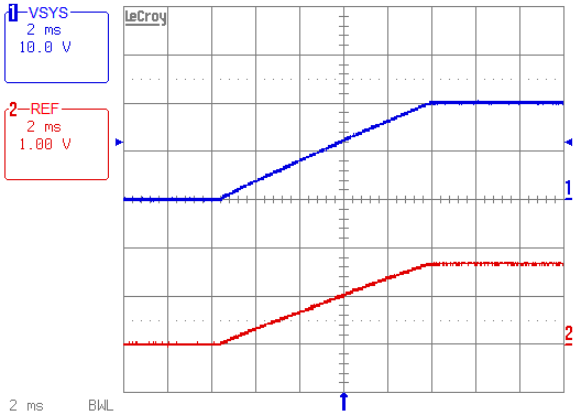


Figure 5. Forward Mode Soft-Start, $12V_{ADP}$, $20V_{SYS}$

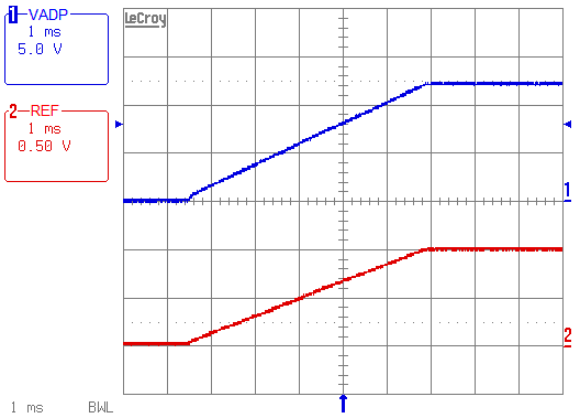


Figure 6. Reverse Mode, Soft-Start, $12V_{ADP}$, $5V_{SYS}$

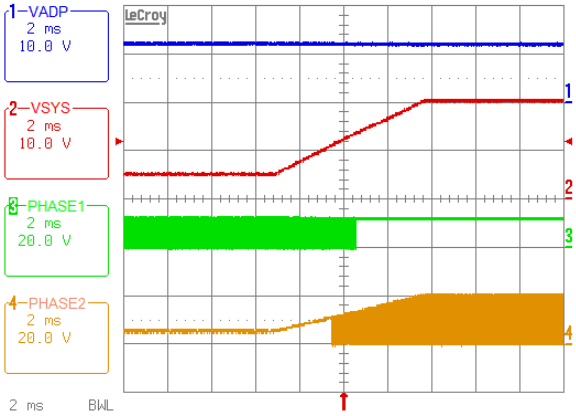


Figure 7. V_{SYS} Voltage Ramps Up in Forward Mode, Buck -> Buck-Boost -> Boost Operation Mode Transition

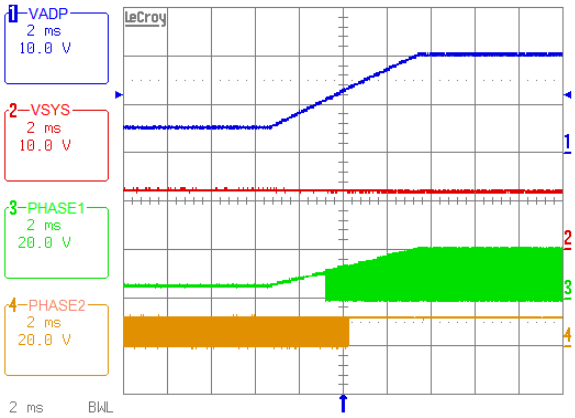


Figure 8. ADP Voltage Ramps Up in Reverse Mode, Buck -> Buck-Boost -> Boost Operation Mode Transition

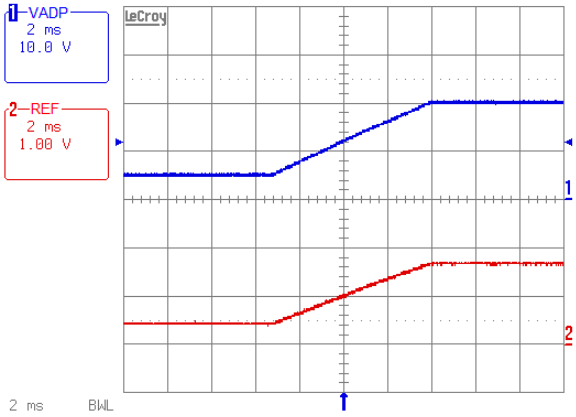


Figure 9. Reverse Mode, $5V_{ADP}$ to $20V_{ADP}$

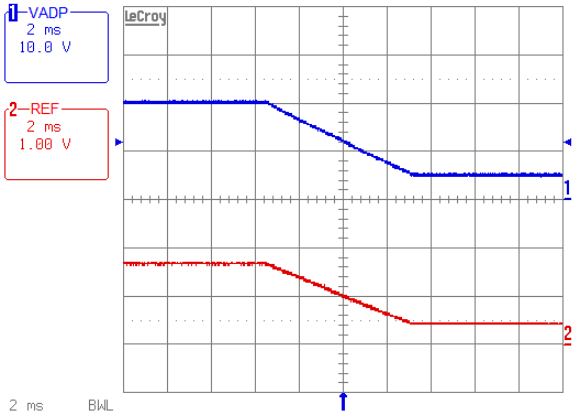


Figure 10. Reverse Mode, $20V_{ADP}$ to $5V_{ADP}$

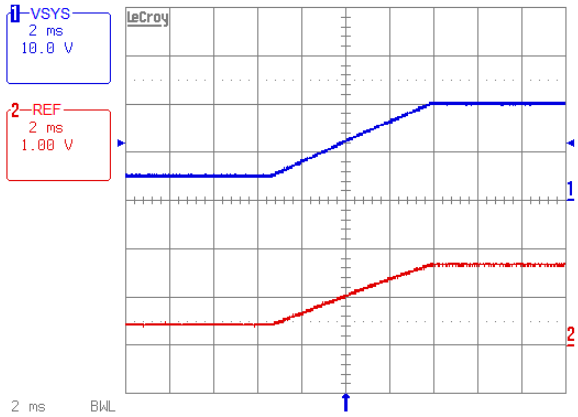


Figure 11. Forward Mode, $5V_{SYS}$ to $20V_{SYS}$

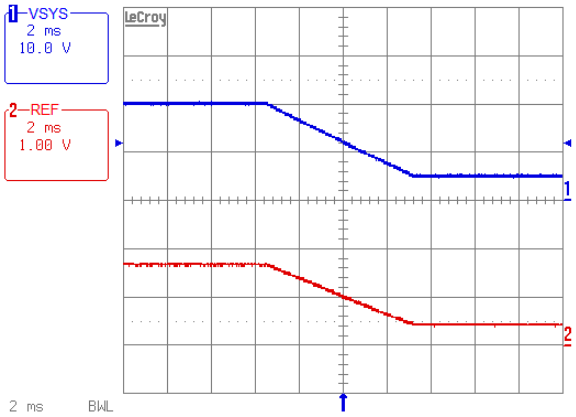


Figure 12. Forward Mode, $20V_{SYS}$ to $5V_{SYS}$

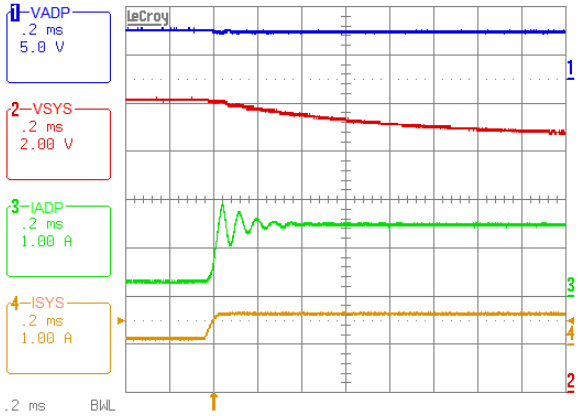


Figure 13. Forward Mode, Output Voltage Loop to ADP Current Loop Transition. $5V_{ADP}$, $12V_{SYS}$, System Load 0A to 0.65A Step, ADP Current Limit = 1.5A

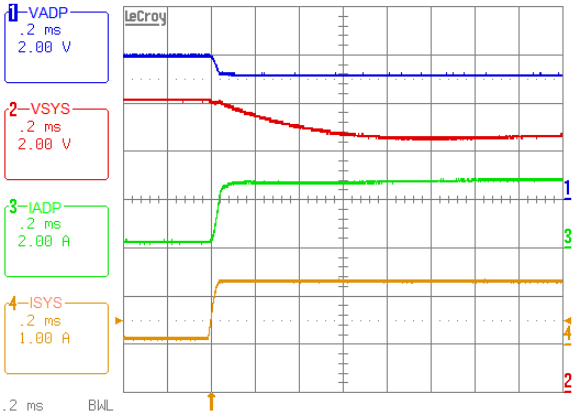


Figure 14. Forward Mode, Output Voltage Loop to Adapter Voltage Loop Transition. $6V_{ADP}$, Input Voltage Limit = 5.12V, $12V_{SYS}$, System Load 0A to 1.3A Step, System Current Limit = 5A, Input Current Limit = 5A

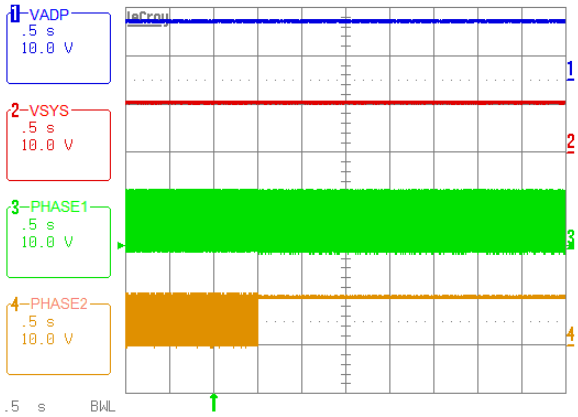


Figure 15. Forward Mode, Force Buck-Boost Mode to Buck Mode. $12V_{ADP}$, $10.1V_{SYS}$

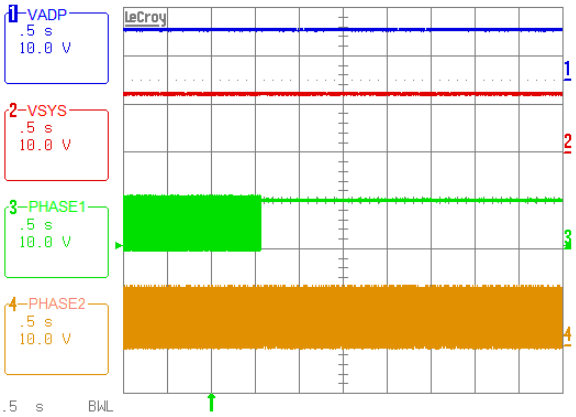


Figure 16. Reverse Mode, Force Buck-Boost Mode to Buck Mode. $10.1V_{ADP}$, $12V_{SYS}$

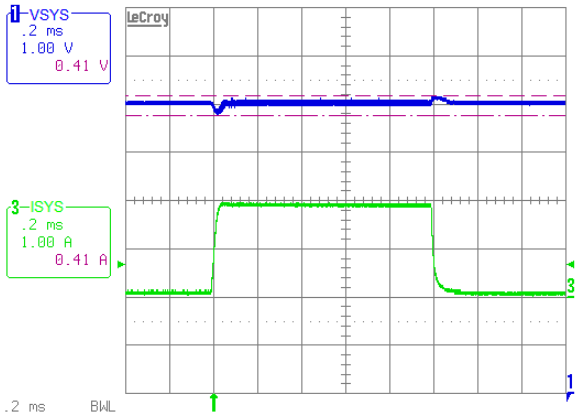


Figure 17. Forward Mode, $5V_{ADP}$, $12V_{SYS}$, 0-2A Transient Load

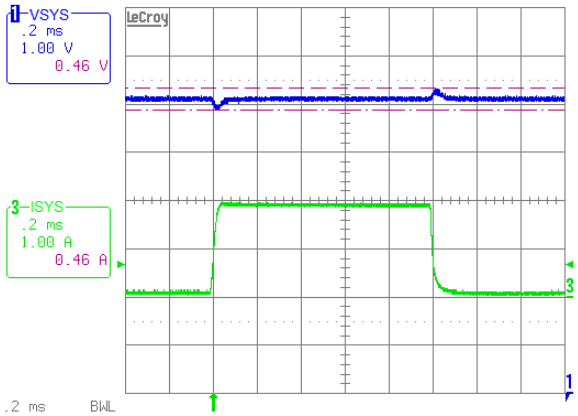


Figure 18. Reverse Mode, $20V_{ADP}$, $12V_{SYS}$, 0-2A Transient Load

4. General SMBus Architecture

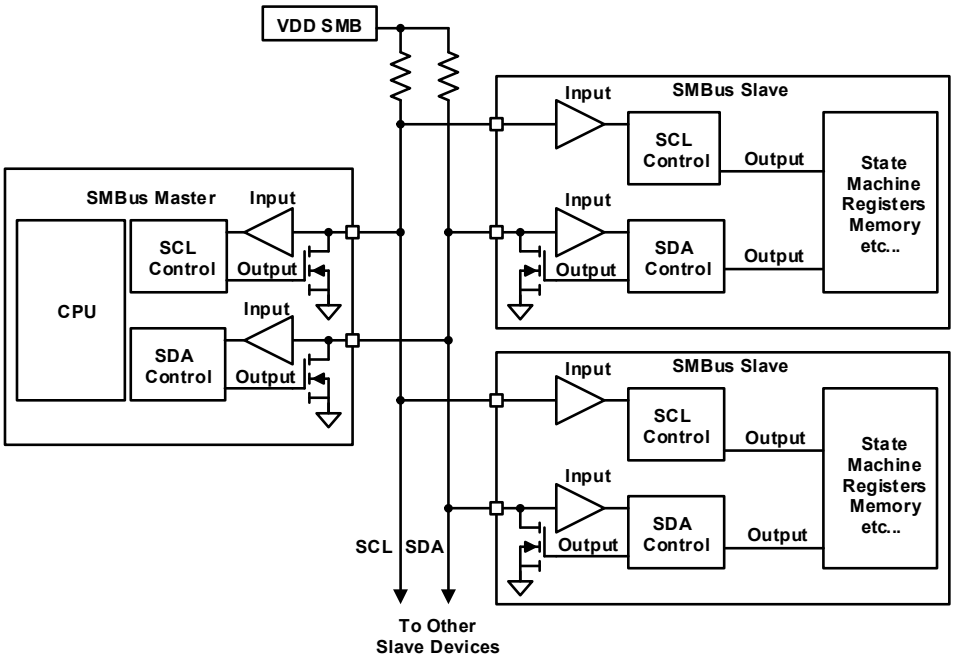


Figure 19. General SMBus Architecture

4.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 20.

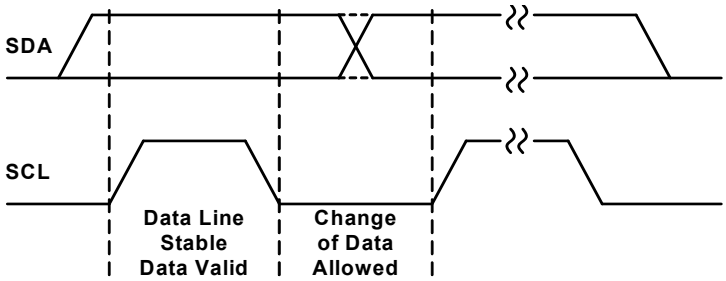


Figure 20. Data Validity

4.2 START and STOP Conditions

As Figure 21 shows, the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

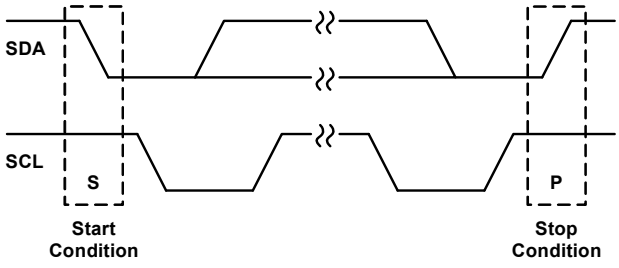


Figure 21. Start and Stop Waveforms

4.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and an R/W bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge (see Figure 22). Both the master and the slave use the ACK bit to acknowledge receipt of register addresses and data.

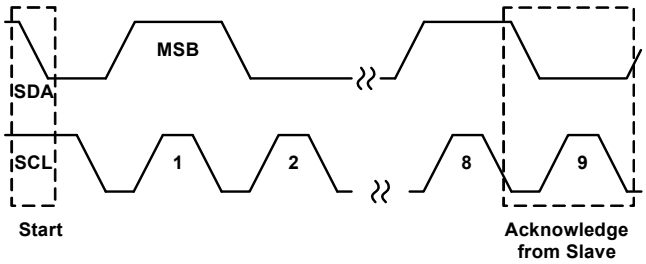


Figure 22. Acknowledge on the SMBus

4.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a START condition, followed by seven bits of slave address (see Table 2), and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is “0” for a WRITE or “1” for a READ. If any slave device on the SMBus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is “1”, indicating a Not Acknowledge condition.

After the control byte is sent and the RAA489800 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the SystemCurrentLimit register. The register address byte tells the RAA489800 which register the master writes or reads. See Tables 3 for more information about the registers. After the RAA489800 receives a register address byte, it responds with an ACK.

4.5 Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO BYTE data is transferred before the HI BYTE data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

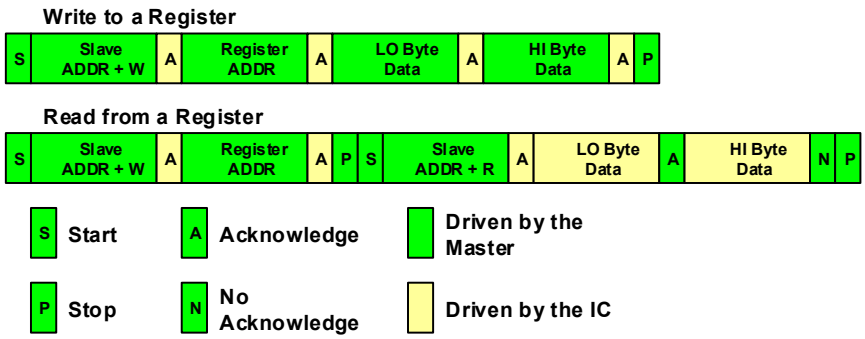


Figure 23. SMBus Read and Write Protocol

4.6 SMBus and I²C Compatibility

The RAA489800 SMBus minimum input logic high voltage is 1.5V, so it is compatible with I²C with pull-up power supplies higher than 1.5V.

The RAA489800 SMBus registers are 16 bits, so it is compatible with 16 bits I²C or 8 bits I²C with auto-increment capability. The chip does not acknowledge SMBus communication unless either ADP or VOUT is higher than 4.1V.

5. RAA489800 SMBus Commands

The RAA489800 receives control inputs from the SMBus interface after V_{DD} 2.7V Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The RAA489800 uses the SMBus Read-word and Write-word protocols (see Figure 23) to communicate with the host system. The RAA489800 is an SMBus slave device and does not initiate communication on the bus. The RAA489800 address is programmable through the ADDR0 and ADDR1 voltage levels (see Table 2) to support multiple RAA489800s sharing a common SMBus. Connect the ADDR0 and ADDR1 pins to either ground or VDD.

Bits 1 and 2 are for the ADDR0 and ADDR1 pins, respectively. A “1” means the pin voltage is high, while a “0” means the pin voltage is low. From Bits 3 to 7, the value is fixed as 10010. The address is latched at the rising V_{DD} 2.7V POR threshold.

Table 2. Address Table

ADDR0	ADDR1	Read/Write	Binary Address	Hex Address
0	0	1	1001,0001	0x91H
0	0	0	1001,0000	0x90H
0	1	1	1001,0101	0x95H
0	1	0	1001,0100	0x94H
1	0	1	1001,0011	0x93H
1	0	0	1001,0010	0x92H
1	1	1	1001,0111	0x97H
1	1	0	1001,0110	0x96H

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

The information in this datasheet is based on current-sensing resistors Rs1 = 20mΩ and Rs2 = 10mΩ, unless otherwise specified.

Table 3. Register Summary

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
SystemCurrentLimit	0x14	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA, with 10mΩ Rs1. This is output current in Forward mode and input current in Reverse mode. Gain is 0.5x in reverse direction. See Table 4.	1.5A
ForwardRegulatingVoltage	0x15	R/W	12	[14:3]12-bit, LSB size 12mV. See PROG Table 21.	5.004V
					9.000V
					12.000V
					15.000V
					20.004V
Control0	0x39	R/W	16	Configures various options. See Table 10.	0x0000h
Information1	0x3A	R	16	Indicates various status. See Table 18.	0x0000h
Control1	0x3C	R/W	16	Configures various options. See Table 11.	0x0000h
Control2	0x3D	R/W	16	Configures various options. See Table 12.	0x0000h
ForwardInputCurrent	0x3F	R/W	11	[12:2]11-bit, LSB size 4mA, total range 6080mA, with 20mΩ Rs1. See Table 6.	Set by PROG pin
ReverseRegulatingVoltage	0x49	R/W	12	[14:3] 12-bit, LSB size 12mV Reverse mode regulating voltage reference. See Table 15.	5.004V
ReverseOutputCurrent	0x4A	R/W	6	[12:7] 6-bit, LSB size 128mA, total range 4.096A Reverse mode maximum current limit. See Table 16.	0.512A

Table 3. Register Summary (Continued)

Register Names	Register Address	Read/ Write	Number of Bits	Description	Default
InputVoltageLimit	0x4B	R/W	6	[13:8] 6-bit, LSB size 512mV Forward low V_{IN} loop voltage reference. See Table 17.	4.096V
Control3	0x4C	R/W	16	Configures various options. See Table 13.	0x0000h
Information2	0x4D	R	16	Indicates various statuses. See Table 19.	0x0000h
Control4	0x4E	R/W	8	[7:0] 8-bit, configures various options. See Tables 14.	0x00h
ManufacturerID	0xFE	R	8	Manufacturer's ID register.	0x49h
DeviceID	0xFF	R	8	Device ID register - 0x0F.	0x0Fh

5.1 Setting System Side Current Limit

To set the system side current limit, which is the output current in Forward mode or the input current in Reverse mode, write a 16-bit SystemCurrentLimit command (0x14H or 0b00010100) using the Write-word protocol shown in Figure 23 and the data format shown in Table 4 for a 10mΩ Rs2 or Table 5 for a 5mΩ Rs2.

The RAA489800 limits the system current by limiting the CSOP-CSON voltage. By using the recommended current-sense resistor value Rs2 = 10mΩ, the register's LSB always translates to 4mA of output current. The SystemCurrentLimit register accepts any output current command but only the valid register bits are written to the register and the maximum value is clamped at 6080mA for Rs2 = 10mΩ.

After POR, the SystemCurrentLimit register is reset to 0x05DCH (1.5A). The SystemCurrentLimit register can be read back to verify its content.

The gain for the system side current-sensing amplifiers is different for Forward mode and Reverse mode. The gain in Reverse mode is half of that in Forward mode. Therefore, in Reverse mode, the sensing current value needs to be doubled compared to the value set in the SystemCurrentLimit register.

Table 4. SystemCurrentLimit Register 0x14H (11-Bit, 4mA Step, 10mΩ Sense Resistor)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of system current limit 1 = Add 4mA of system current limit
<3>	0 = Add 0mA of system current limit 1 = Add 8mA of system current limit
<4>	0 = Add 0mA of system current limit 1 = Add 16mA of system current limit
<5>	0 = Add 0mA of system current limit 1 = Add 32mA of system current limit
<6>	0 = Add 0mA of system current limit 1 = Add 64mA of system current limit
<7>	0 = Add 0mA of system current limit 1 = Add 128mA of system current limit
<8>	0 = Add 0mA of system current limit 1 = Add 256mA of system current limit
<9>	0 = Add 0mA of system current limit 1 = Add 512mA of system current limit
<10>	0 = Add 0mA of system current limit 1 = Add 1024mA of system current limit
<11>	0 = Add 0mA of system current limit 1 = Add 2048mA of system current limit
<12>	0 = Add 0mA of system current limit 1 = Add 4096mA of system current limit

Table 4. SystemCurrentLimit Register 0x14H (11-Bit, 4mA Step, 10mΩ Sense Resistor) (Continued)

Bit	Description
<13:15>	Not used
Maximum	<12:2> = 10111110000 6080mA

Table 5. SystemCurrentLimit Register 0x14H (11-Bit, 8mA Step, 5mΩ Sense Resistor)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of system current limit 1 = Add 8mA of system current limit
<3>	0 = Add 0mA of system current limit 1 = Add 16mA of system current limit
<4>	0 = Add 0mA of system current limit 1 = Add 32mA of system current limit
<5>	0 = Add 0mA of system current limit 1 = Add 64mA of system current limit
<6>	0 = Add 0mA of system current limit 1 = Add 128mA of system current limit
<7>	0 = Add 0mA of system current limit 1 = Add 256mA of system current limit
<8>	0 = Add 0mA of system current limit 1 = Add 512mA of system current limit
<9>	0 = Add 0mA of system current limit 1 = Add 1024mA of system current limit
<10>	0 = Add 0mA of system current limit 1 = Add 2048mA of system current limit
<11>	0 = Add 0mA of system current limit 1 = Add 4096mA of system current limit
<12>	0 = Add 0mA of system current limit 1 = Add 8192mA of system current limit
<13:15>	Not used
Maximum	<12:2> = 10111110000 12160mA

5.2 Setting Input Current Limit in Forward Mode

To set the input current limit in Forward mode, write a 16-bit ForwardInputCurrent command (0x3FH or 0b00111111) using the Write-word protocol shown in Figure 23 and the data format shown in Table 6 for a 20mΩ Rs1 or Table 7 for a 10mΩ Rs1.

The RAA489800 limits the input current in Forward mode by limiting the CSIP - CSIN voltage. By using the recommended current-sense resistor values, the register's LSB always translates to 4mA of input current. Any input current limit command is accepted, but only the valid register bits are written to the ForwardInputCurrent register and the maximum values are clamped at 6080mA for Rs1 = 20mΩ.

Table 6. ForwardInputCurrent Register 0x3FH (11-Bit, 4mA Step, 20mΩ Sense Resistor, x18)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of input current limit in Forward mode 1 = Add 4mA of input current limit in Forward mode
<3>	0 = Add 0mA of input current limit in Forward mode 1 = Add 8mA of input current limit in Forward mode

Table 6. ForwardInputCurrent Register 0x3FH (11-Bit, 4mA Step, 20mΩ Sense Resistor, x18) (Continued)

Bit	Description
<4>	0 = Add 0mA of input current limit in Forward mode 1 = Add 16mA of input current limit in Forward mode
<5>	0 = Add 0mA of input current limit in Forward mode 1 = Add 32mA of input current limit in Forward mode
<6>	0 = Add 0mA of input current limit in Forward mode 1 = Add 64mA of input current limit in Forward mode
<7>	0 = Add 0mA of input current limit in Forward mode 1 = Add 128mA of input current limit in Forward mode
<8>	0 = Add 0mA of input current limit in Forward mode 1 = Add 256mA of input current limit in Forward mode
<9>	0 = Add 0mA of input current limit in Forward mode 1 = Add 512mA of input current limit in Forward mode
<10>	0 = Add 0mA of input current limit in Forward mode 1 = Add 1024mA of input current limit in Forward mode
<11>	0 = Add 0mA of input current limit in Forward mode 1 = Add 2048mA of input current limit in Forward mode
<12>	0 = Add 0mA of input current limit in Forward mode 1 = Add 4096mA of input current limit in Forward mode
<13:15>	Not used
Maximum	<12:2> = 10111110000 6080mA.

Table 7. ForwardInputCurrent Register 0x3FH (11-Bit, 8mA Step, 10mΩ Sense Resistor, x18)

Bit	Description
<1:0>	Not used
<2>	0 = Add 0mA of input current limit in Forward mode 1 = Add 8mA of input current limit in Forward mode
<3>	0 = Add 0mA of input current limit in Forward mode 1 = Add 16mA of input current limit in Forward mode
<4>	0 = Add 0mA of input current limit in Forward mode 1 = Add 32mA of input current limit in Forward mode
<5>	0 = Add 0mA of input current limit in Forward mode 1 = Add 64mA of input current limit in Forward mode
<6>	0 = Add 0mA of input current limit in Forward mode 1 = Add 128mA of input current limit in Forward mode
<7>	0 = Add 0mA of input current limit in Forward mode 1 = Add 256mA of input current limit in Forward mode
<8>	0 = Add 0mA of input current limit in Forward mode 1 = Add 512mA of input current limit in Forward mode
<9>	0 = Add 0mA of input current limit in Forward mode 1 = Add 1024mA of input current limit in Forward mode
<10>	0 = Add 0mA of input current limit in Forward mode 1 = Add 2048mA of input current limit in Forward mode
<11>	0 = Add 0mA of input current limit in Forward mode 1 = Add 4096mA of input current limit in Forward mode
<12>	0 = Add 0mA of input current limit in Forward mode 1 = Add 8192mA of input current limit in Forward mode
<13:15>	Not used
Maximum	<12:2> = 10111110000 12160mA

5.3 Setting System Regulating Voltage in Forward Mode

To set the regulating voltage in Forward mode, write a 16-bit ForwardRegulatingVoltage command (0x15H or 0b00010101) using the Write-word protocol shown in Figure 23 and the data format shown in Table 8.

The output regulating voltage range in Forward mode is 2V to 21V. The ForwardRegulatingVoltage register accepts any voltage command, but only the valid register bits are written to the register. The maximum value is clamped at 21V. The RAA489800 accepts a 0V command, but the register value does not change. The VOUTS pin is the output voltage regulation sense point in Forward mode.

In Forward mode, you can also configure the regulating output voltage by setting the external voltage divider on the VOUTS pin without changing the ForwardRegulatingVoltage register value.

Table 8. ForwardRegulatingVoltage Register 0x15H (12mV Step)

Bit	Description
<2:0>	Not used
<3>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 12mV of regulating voltage in Forward mode
<4>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 24mV of regulating voltage in Forward mode
<5>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 48mV of regulating voltage in Forward mode
<6>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 96mV of regulating voltage in Forward mode
<7>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 192mV of regulating voltage in Forward mode
<8>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 384mV of regulating voltage in Forward mode
<9>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 768mV of regulating voltage in Forward mode
<10>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 1536mV of regulating voltage in Forward mode
<11>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 3072mV of regulating voltage in Forward mode
<12>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 6144mV of regulating voltage in Forward mode
<13>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 12288mV of regulating voltage in Forward mode
<14>	0 = Add 0mV of regulating voltage in Forward mode 1 = Add 24576mV of regulating voltage in Forward mode
<15>	Not used
Maximum	21000mV

Note: The default reading value of this register is 5.004V when the chip is powering up without writing any values because of the DAC initial value. Thus, write the required value in this register before enabling forward output voltage.

5.4 ALERT# FAULT Interrupt Behavior

The ALERT# pin is an open-drain fault indicator. When the controller detects a WOC, OV, UV, OTP, or ADPOV, fault the ALERT# pin is actively pulled low to alert the system that a fault has occurred. Additionally, the ALERT# pin is pulled low when the controller enters or exits output current limit mode.

In addition to setting the ALERT# pin low, information bits are set to indicate to the system which fault has occurred. See Table 9 for details about the information bits associated with the ALERT# signal.

Both the information bits and the ALERT# signal are cleared by writing a 1 to Control4<1>. Clearing the ALERT# signal also clears the information bits listed in Table 9.

Table 9. Information1 Register Bits Associated with ALERT# Indicator

Bit	Description
INFORMATION1<12>	A WOC fault has occurred
INFORMATION1<11>	An output OV fault has occurred
INFORMATION1<10>	An output UV fault has occurred
INFORMATION1<9>	A controller OTP (over-temperature) fault has occurred
INFORMATION1<8>	An adapter side OV fault has occurred
INFORMATION1<7>	The controller has entered or exited output current limit mode

5.5 Setting ALERT# Debounce Time

Control2 register Bit<10:9> configures the ALERT# signal debounce time before its assertion for the fault indicator response.

5.6 Control Registers

The Control0, Control1, Control2, Control3, and Control4 registers configure the RAA489800 operation. To change certain functions or options after V_{DD} 2.7V POR, write a 16-bit control command to the Control0 register (0x39H or 0b00111001), and a 16-bit control command to the Control1 register (0x3CH or 0b00111100), Control2 register (0x3DH or 0b00111101), Control3 register (0x4CH or 0b00111100), or an 8-bit control command to the Control4 register (0x4EH or 0b00111101) using the Write-word protocol shown in Figure 23 and the data format shown in Tables 10, 11, 12, 13, and 14, respectively.

Table 10. Control0 Register 0x39H

Bit	Bit Name	Description
<15:13>	Forward Buck and Buck-Boost Phase Comparator Threshold Offset	Bit<15:13> adjusts the phase comparator threshold offset for forward buck and buck-boost. 000 = 0mV 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
<12:10>	Forward and Reverse Boost Phase Comparator Threshold Offset	Bit<12:10> adjusts the phase comparator threshold offset for forward and reverse boost. 000 = 0mV 001 = 0.5mV 010 = 1mV 011 = 1.5mV 100 = -2mV 101 = -1.5mV 110 = -1mV 111 = -0.5mV
<9:7>	Reverse Buck and Buck-Boost Phase Comparator Threshold Offset	Bit<9:7> adjusts the phase comparator threshold offset for reverse buck and buck-boost. 000 = 0mV 001 = 1mV 010 = 2mV 011 = 3mV 100 = -4mV 101 = -3mV 110 = -2mV 111 = -1mV
<6:5>	High-Side FET Short Detection Threshold	Bit<6:5> configures the high-side FET short detection PHASE1 and PHASE 2 node voltage threshold during low-side FET turn-on. 00 = 500mV (default) 01 = 400mV 10 = 600mV 11 = 800mV

Table 10. Control0 Register 0x39H (Continued)

Bit	Bit Name	Description
<4>	Low Voltage Shutdown	Bit<4> enables or disables the system shutdown option when the output voltage falls below 3V/3.3V depending on the Bit<3> setting. 0 = Disable low voltage shutdown when the output voltage is lower than 3V/3.3V (default). 1 = Enable low voltage shutdown when the output voltage is lower than 3V/3.3V.
<3>	Low Voltage Shutdown Threshold	Bit<3> configures the output voltage threshold for low voltage shutdown function 0 = Low voltage shutdown threshold is 3V (default) 1 = Low voltage shutdown threshold is 3.3V
<2>	Disable Input Voltage Regulation Loop	Bit<2> disables or enables the input voltage regulation loop. 0 = Enable input voltage regulation loop (default) 1 = Disable input voltage regulation loop
<1>	ADP Side Discharge	Bit<1> enables or disables the ADP side charger function. Typical 22mA. 0 = Disable (default) 1 = Enable
<0>	System Side Discharge	Bit<0> enables or disables the system side charger function. Typical 22mA. 0 = Disable (default) 1 = Enable

Note:
8. The ADP side discharge is automatically enabled in Reverse mode when $V_{OUT} > V_{REF}$. The system side discharge is automatically enabled in Forward mode when $V_{OUT} > V_{REF}$.

Table 11. Control1 Register 0x3CH

Bit	Bit Name	Description
<15>	Disable Diode-Emulation Comparator	Bit<15> enables or disables the diode-emulation comparator. 0 = Diode-emulation comparator enabled (default) 1 = Diode-emulation comparator disabled
<14>	Allow Sinking Current During Negative DAC Transition	Bit<14> enables or disables sinking current during the negative DAC transition. 0 = Sinking current during negative DAC transition disabled (default) 1 = Sinking current during negative DAC transition enabled
<13>	Skip Trim During Restart	Bit<13> enables or disables trim read during restart. Program this bit when PGOOD is high. 0 = Read trim during restart (default) 1 = Skip trim during restart
<12>	Skip Autozero During Restart	Bit<12> enables or disables autozero during restart. Program this bit when PGOOD is high. 0 = Autozero during restart (default) 1 = Skip autozero during restart
<11>	Reverse Mode Function	Bit<11> enables or disables the Force Reverse mode function. 0 = Disable Force Reverse mode function (default) 1 = Enable Force Reverse mode function
<10>	Audio Filter	Bit<10> enables or disables the audio filter function. The audio filter function is not available in Buck-Boost mode. 0 = Disable (default) 1 = Enable
<9:7>	Switching Frequency	Bit<9:7> configures the switching frequency. 000 = 1000kHz (default) 001 = 910kHz 010 = 850kHz 011 = 787kHz 100 = 744kHz 101 = 695kHz 110 = 660kHz 111 = 620kHz
<6>	Output Current Limit ALERT#	ALERT# is asserted by default if the controller enters or exits output current limit mode. 0 = controller asserts ALERT# when entering or exiting output current limit mode 1 = ALERT# is not asserted when entering or exiting output current limit mode

Table 11. Control1 Register 0x3CH (Continued)

Bit	Bit Name	Description
<5>	Disable System Side Current-Amp When in FWD Mode without ADP	Bit<5> enables or disables the system side current amplifier when in FWD mode without ADP. 0 = Enable system side current amplifier (default) 1 = Disable system side current amplifier
<4>	Pass Through Mode	Bit<4> enables or disables Pass Through mode. 0 = Disable (default) 1 = Enable
<3>	Fast REF mode	Bit<3> enables or disables fast REF mode. 5kΩ impedance to the REF pin. 0 = Disable (default) 1 = Enable
<2>	Stop Switching in FWD Mode	Bit<2> enables or disables the buck-boost switching V_{OUT} output. When disabled, the RAA489800 stops switching and REF drops to 0V. Valid in Forward mode only. 0 = Enable switching (default) 1 = Disable switching
<1>	OV Enable or Disable During Slew-Down	Bit<1> enables or disables the OV fault when the VDAC slew rate is down in Forward and Reverse mode. 0 = Enable OV (default) 1 = Disable OV
<0>	Force 5.04V VDAC	Bit<0> enables or disables force 5.04V VDAC in Forward and Reverse mode. 0 = Disable force 5.04V VDAC (default) 1 = Enable force 5.04V VDAC

Table 12. Control2 Register 0x3DH

Bit	Bit Name	Description
<15>	OV Control	Bit<15> enables or disables OV. 0 = Enable OV (default) 1 = Disable OV
<14>	UV Control	Bit<14> enables or disables UV. 0 = Enable UV (default) 1 = Disable UV
<13>	Fault Restart Debounce for Reverse Enable	Bit<13> configures fault restart debounce for reverse enable mode. 0 = Debounce time is 1.3s (default) 1 = Debounce time is 150ms
<12>	Fault Restart Debounce	Bit<12> configures fast fault restart debounce. 0 = Debounce time is 1.3s or 150ms, depending on Bit<11> or Bit<13> setting (default) 1 = Debounce time is 80µs
<11>	Fault Restart Debounce for Forward Enable	Bit<11> configures fault restart debounce for forward enable mode. 0 = Debounce time is 1.3s (default) 1 = Debounce time is 150ms
<10:9>	ALERT# Debounce	Bit<10:9> configures the ALERT# debounce time before its assertion for ADPsideALERT# and SystemsideALERT#. 00: 7µs (default) 01: 100µs 10: 500µs 11: 1ms
<8:5>	Not used	Not used
<4>	Reverse Fast Swap	Bit<4> configures reverse fast swap. 0 = Disable reverse fast swap (default) 1 = Enable reverse fast swap
<3>	Forward Fast Swap	Bit<3> configures forward fast swap. 0 = Disable forward fast swap (default) 1 = Enable forward fast swap
<2>	Output Current Limit Control	Bit<2> configures the output current limit control loop during an output overcurrent event. ALERT# is asserted regardless of this bit setting. 0 = Enable output current limit control during overcurrent (default) 1 = Disable output current limit control during overcurrent

Table 12. Control2 Register 0x3DH (Continued)

Bit	Bit Name	Description
<1>	Disable WOC Fault	Bit<1> enables and disables WOC fault. 0 = Enable WOC (default) 1 = Disable WOC
<0>	Not Used	Not used

Table 13. Control3 Register 0x4CH

Bit	Bit Name	Description
<15>	Reread PROG Pin Resistor	Bit<15> specifies whether to reread the PROG pin resistor before switching. 0 = Reread the PROG pin resistor (default) 1 = Do not reread the PROG pin resistor
<14>	Not used	Not used
<13>	Not used	Not used
<12>	Reverse Startup Debounce Time	Bit<12> configures the startup debounce time for reverse mode (Control1<13> = 1 and Control1<12> = 1). 0 = Debounce time is 50µs (default) 1 = Debounce time is 250µs
<11>	Not Used	Not used
<10>	Force Operating Mode	Bit<10:8> enables or disables Force Operating mode. 0 = Disable Forced Operating mode (default) 1 = Enable Forced Operating mode
<9>	Automatic Discharge Path	Bit<9> enables or disables the ADP and System side automatic discharge paths when $V_{DAC} > V_{REF}$. 0 = Enable all automatic discharge paths (default) 1 = Disable all automatic discharge paths
<8>	Forced Buck Mode	Bit<8> configures Forced Operating mode when enabled by Bit<10>. 0 = No switching, do not use 1 = Forced buck mode
<7>	Not used	Not used
<6>	Current Loop Feedback Gain	Bit<6> configures current loop feedback gain for high current. 0 = Gain x 1 (default) 1 = Gain x 0.5
<5>	Input Current Limit Loop in Forward Mode	Bit<5> disables input current limit loop in Forward mode. 0 = Enable input current limit loop in Forward mode (default) 1 = Disable input current limit loop in Forward mode
<4>	PGOOD Window Control	Bit<4> configures the PGOOD window control. 0 = PGOOD is controlled by a window around REF (default) 1 = PGOOD is controlled by a window around DAC
<3>	Disable Internal REF Amplifier for Use with External Reference	Bit<3> disables the internal REF amplifier. 0 = Enable internal REF amplifier (default) 1 = Disable internal REF amplifier
<2>	Digital Reset	Bit<2> resets all SMBus register values to the POR default value and restarts switching. 0 = Idle (default) 1 = Reset
<1>	Conduction Time in Buck-Boost Light-Load Discontinuous Conduction Mode	Bit<1> configures the conduction time in Buck-Boost Discontinuous Conduction mode. 0 = Shorter conduction time to reduce ripple 1 = Longer conduction time, which improves efficiency but increases ripple
<0>	PGOOD Setting	Bit<0> configures the PGOOD assert condition. 0 = PGOOD suppressed until V_{REF} equals to V_{DAC} (default) 1 = PGOOD asserts when switching starts

Table 14. Control4 Register 0x4EH

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td><7></td><td>Disable ALERT#</td><td>Bit<7> enables or disables the ALERT# function.
0 = Enable ALERT# (default)
1 = Disable ALERT#</td></tr>
<tr><td><6></td><td>Forward Sleep Mode</td><td>Bit<6> enables or disables Chip Sleep mode in Forward mode regardless of ADP voltage. The RVSEN pin or Control1 Bit <11> can override this function.
0: The controller is enabled if FWREN = 1. The controller is disabled if FWREN = 0 (default)
1: The controller is disabled if FWREN = 1. The controller is enabled if FWREN = 0
<table>
<tr><th>FRWEN</th><th>Control4 <6></th><th>Forward Sleep</th><th>Forward Enable</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table>
</td></tr>
<tr><td><5:2></td><td>Not used</td><td>Not used</td></tr>
<tr><td><1></td><td>ALERT# Clear</td><td>Bit<1> clears ALERT#.
0 = Idle (default)
1 = Clear ALERT#</td></tr>
<tr><td><0></td><td>Not Used</td><td>Not used</td></tr>
</table>

5.7 Regulating Voltage Register in Reverse Mode

The ReverseRegulatingVoltage register contains the SMBus readable and writable Reverse mode output regulation voltage reference. The output regulating voltage range in Reverse mode is 2V to 21V. The default value is 5.004V. This register accepts any voltage command, but only the valid register bits are written to the register. However, do not program the register higher than the recommended operating voltage.

In Reverse mode, you also can configure the regulating output voltage on the ADP side by setting the external voltage divider on the ADP pin without changing the ReverseRegulatingVoltage register value.

Table 15. ReverseRegulatingVoltage Register 0x49H

Bit	Description
<2:0>	Not used
<3>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 12mV of regulating voltage in Reverse mode
<4>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 24mV of regulating voltage in Reverse mode
<5>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 48mV of regulating voltage in Reverse mode
<6>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 96mV of regulating voltage in Reverse mode
<7>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 192mV of regulating voltage in Reverse mode
<8>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 384mV of regulating voltage in Reverse mode
<9>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 768mV of regulating voltage in Reverse mode
<10>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 1536mV of regulating voltage in Reverse mode
<11>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 3072mV of regulating voltage in Reverse mode

Table 15. ReverseRegulatingVoltage Register 0x49H (Continued)

Bit	Description
<12>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 6144mV of regulating voltage in Reverse mode
<13>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 12288mV of regulating voltage in Reverse mode
<14>	0 = Add 0mV of regulating voltage in Reverse mode 1 = Add 24576mV of regulating voltage in Reverse mode
<15>	Not used
Maximum	21000mV

5.8 Output Current Limit Register in Reverse Mode

The ReverseCurrentLimit register contains SMBus readable and writable reverse current limit. The default is 512mA. This register accepts any current command, but only the valid register bits are written to the register. The maximum values are clamped at 4096mA for Rs1 = 20mΩ.

Table 16. ReverseCurrentLimit Register 0x4AH

Bit	Description
<6:0>	Not used
<7>	0 = Add 0mA of output current limit in Reverse mode 1 = Add 128mA of output current limit in Reverse mode
<8>	0 = Add 0mA of output current limit in Reverse mode 1 = Add 256mA of output current limit in Reverse mode
<9>	0 = Add 0mV of output current limit in Reverse mode 1 = Add 512mA of output current limit in Reverse mode
<10>	0 = Add 0mV of output current limit in Reverse mode 1 = Add 1024mA of output current limit in Reverse mode
<11>	0 = Add 0mV of output current limit in Reverse mode 1 = Add 2048mA of output current limit in Reverse mode
<12>	0 = Add 0mV of output current limit in Reverse mode 1 = Add 4096mA of output current limit in Reverse mode
<15:13>	Not used
Maximum	4096mA

5.9 Input Voltage Limit Register

The InputVoltageLimit register contains SMBus readable and writable input voltage limits. The default is 4.096V. This register accepts any command, but only the valid register bits are written to the register. The maximum values are clamped at 18V. The recommended minimum setting for this register is 4.096V.

Table 17. InputVoltageLimit Register 0x4BH

Bit	Description
<7:0>	Not used
<8>	0 = Add 0mV of input voltage limit 1 = Add 512mV of input voltage limit
<9>	0 = Add 0mA of input voltage limit 1 = Add 1024mV of input voltage limit
<10>	0 = Add 0mV of input voltage limit 1 = Add 2048mV of input voltage limit
<11>	0 = Add 0mV of input voltage limit 1 = Add 4096mV of input voltage limit

Table 17. InputVoltageLimit Register 0x4BH (Continued)

Bit	Description
<12>	0 = Add 0mV of input voltage limit 1 = Add 8192mV of input voltage limit
<13>	0 = Add 0mV of input voltage limit 1 = Add 16384mV of input voltage limit
<15:14>	Not used
Maximum	18000mV

5.10 Information Register

The Information Register contains SMBus readable information about manufacture and operating modes. Tables 18 and 19 identify the bit locations of the information available.

Table 18. Information1 Register 0x3AH

Bit	Description
<6:0>	Not used
<7>	Bit<7> indicates that the controller has entered or exited output current limit mode. 0 = The controller has not entered or exited output current limit mode 1 = The controller has entered or exited output current limit mode
<8>	Bit<8> indicates that an adapter side overvoltage (ADPOV) fault has occurred. 0 = An ADPOV fault has not occurred 1 = An ADPOV fault has occurred
<9>	Bit<9> indicates that a controller over-temperature (OTP) fault has occurred. 0 = An OTP fault has not occurred 1 = An OTP fault has occurred
<10>	Bit<10> indicates that an output undervoltage (UV) fault has occurred. 0 = An UV fault has not occurred 1 = An UV fault has occurred
<11>	Bit<11> indicates that an output overvoltage (OV) fault has occurred. 0 = An OV fault has not occurred 1 = An OV fault has occurred
<12>	Bit<12> indicates that a way overcurrent (WOC) fault has occurred. 0 = A WOC fault has not occurred 1 = A WOC fault has occurred
<14:13>	Bit<14:13> indicates the active control loop. 00 = Voltage control loop is active 01 = System current loop is active 10 = ADP current limit loop is active 11 = Input voltage loop is active
<15>	Bit<15> indicates whether the internal reference circuit is active. Bit<15> = 0 indicates that the RAA489800 is in low power mode. 0 = Reference is not active 1 = Reference is active

Table 19. Information2 Register 0x4DH

Bit	Description
<4:0>	Program Resister read out
<7:5>	Bit<7:5> indicates the RAA489800 operation mode. 001: Forward Boost 010: Forward Buck 011: Forward Buck-Boost 101: Reverse Boost 110: Reverse Buck 111: Reverse Buck-Boost

Table 19. Information2 Register 0x4DH (Continued)

Bit	Description
<11:8>	Bit<11:8> indicates the RAA489800 state machine status. 0000 = RESET 0001 = OTG Ready 0101 = FWD Mode 0111 = OTG Mode 1010 = FWD Ready
<12>	Not used
<13>	Not used
<14>	Bit<14> indicates whether forward switching is enabled. 0 = Not enabled 1 = Enabled
<15>	Not used

6. Application Information

6.1 R3 Modulator

The RAA489800 uses the Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM, while eliminating many of their shortcomings. Figure 24 conceptually shows the R3 modulator circuit and Figure 25 shows the operation principles in steady state.

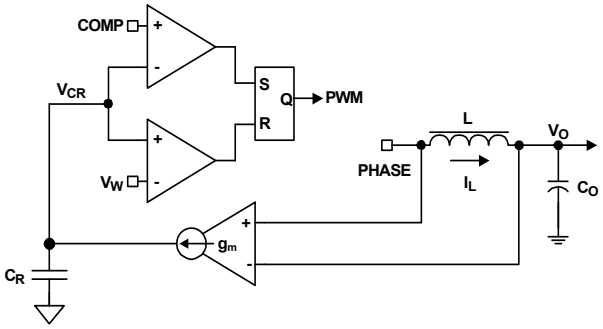


Figure 24. R3 Modulator

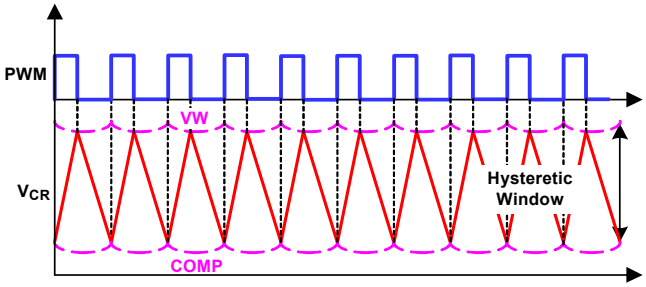


Figure 25. R3 Modulator Operation Principles in Steady State

The fixed voltage window between VW and COMP is called the VW window in the following discussion. Using Buck mode as an example, the modulator charges the ripple capacitor C_R with a current source equal to g_m (V_{IN} - V_O) during PWM on-time and discharges the ripple capacitor C_R with a current source equal to $g_m V_O$ during PWM off-time, where g_m is a gain factor. Therefore, the C_R voltage V_{CR} emulates the inductor current waveform. The modulator turns off the PWM pulse when V_{CR} reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with V_{CR}, which is a large amplitude and noise-free synthesized signal, it achieves lower phase jitter than a conventional hysteretic mode modulator.

Figure 26 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, temporarily turning on PWM pulses earlier and more frequently, which allows for higher control loop bandwidth than a conventional fixed frequency PWM modulator at the same steady-state switching frequency.

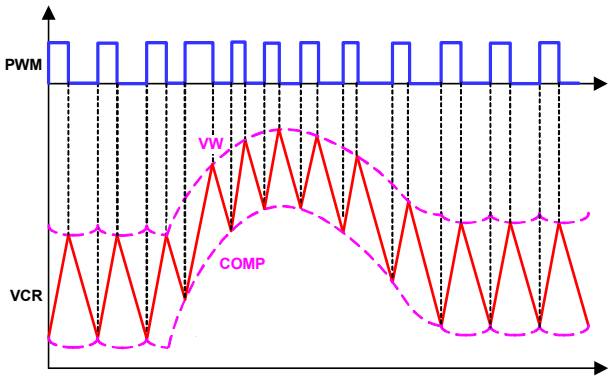


Figure 26. R3 Modulator Operation Principles in Dynamic Response

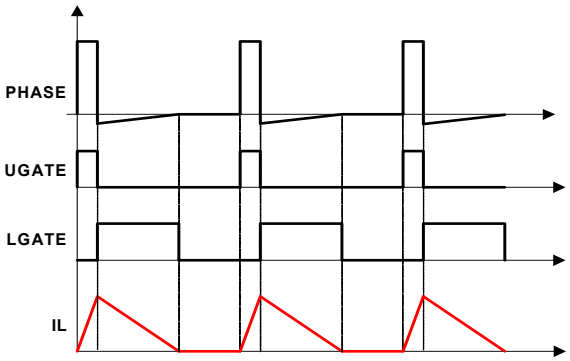


Figure 27. Diode Emulation

The R3 modulator can operate in Diode Emulation (DE) mode to increase light-load efficiency. For example, in Buck DE mode the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow reverse current, emulating a diode. As shown in Figure 27, the low-side MOSFET carries current when LGATE is on, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. The RAA489800 turns off LGATE when the phase

node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss. Similar operations apply for other modes, such as Boost mode and Buck-Boost mode.

If the load current is light enough, as Figure 27 shows, the inductor current reaches and stays at zero before the next phase node pulse. At this stage, the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in Continuous Conduction Mode (CCM), although the controller is in DE mode.

Figure 28 shows the operation principle in DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage V_{CR} in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach V_{CR}, naturally stretching the switching period. The inductor current triangles move farther apart from each other, so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

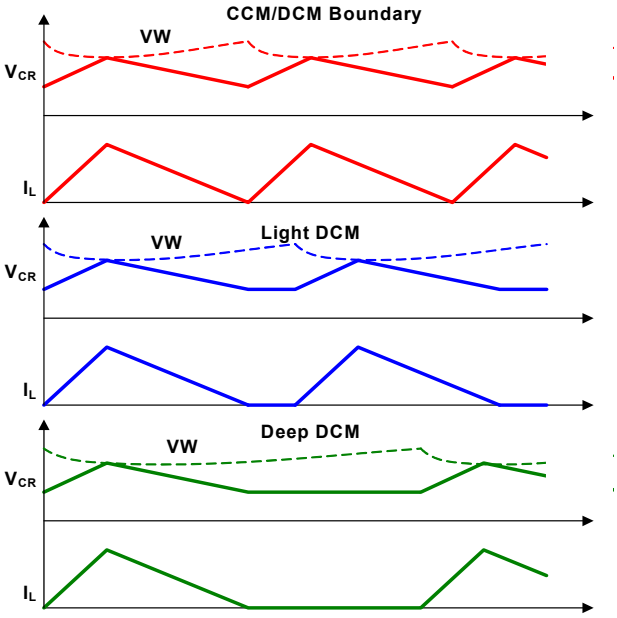


Figure 28. Period Stretching

6.2 4-Switch Bidirectional Buck-Boost Voltage Regulator and 2-Switch Buck Regulator Configurations

The RAA489800 bidirectional buck-boost voltage regulator drives an external N-channel MOSFET bridge comprised of two transistor pairs as shown in Figure 3. The first pair, Q1 and Q2, is a buck arrangement with the transistor center tap connected to an inductor “input”, as is the case with a buck converter in Forward mode. The second transistor pair, Q3 and Q4, is a boost arrangement with the transistor center tap connected to the same inductor’s “output”, as is the case with a boost converter in Forward mode. This arrangement supports the same operation mode in reverse direction.

Table 20 describes how the transistors operate in different operation modes.

Table 20. 4-Switch Buck-Boost Modes of Operation

Mode	Q1	Q2	Q3	Q4
Forward Buck	Control FET	Sync. FET	Off	On
Forward Boost	On	Off	Control FET	Sync. FET
Forward Buck-Boost	Control FET	Sync. FET	Control FET	Sync. FET

Table 20. 4-Switch Buck-Boost Modes of Operation (Continued)

Mode	Q1	Q2	Q3	Q4
Forward Pass Through	On	Off	Off	On
Reverse Buck	On	Off	Sync. FET	Control FET
Reverse Boost	Sync. FET	Control FET	Off	On
Reverse Buck-Boost	Sync. FET	Control FET	Sync. FET	Control FET
Reverse Pass Through	On	Off	Off	On

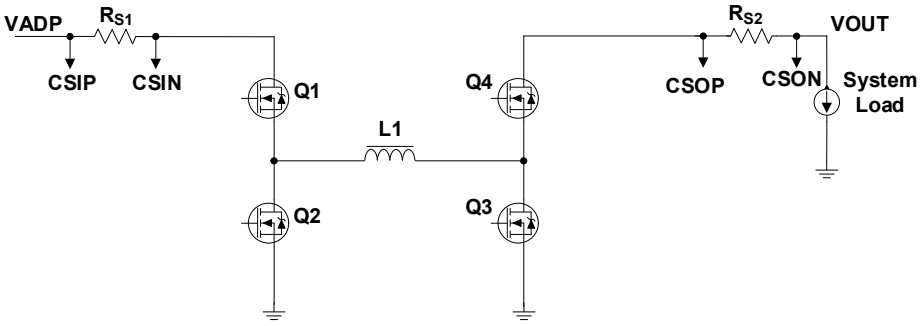


Figure 29. 4-Switch Buck-Boost Regulator Topology

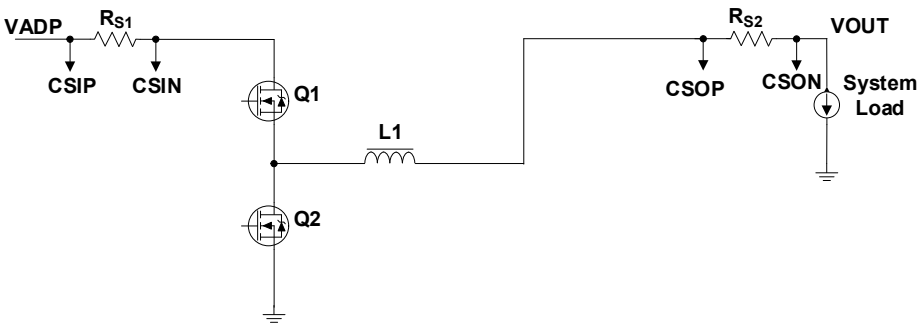


Figure 30. 2-Switch Buck Regulator Topology

The RAA489800 optimizes the operation mode transition algorithm by considering the input and output voltage ratio. When the ADP voltage V_{ADP} is rising and is higher than 88% of the system bus voltage VSYS, the RAA489800 transitions from Boost mode to Buck-Boost mode. If V_{ADP} is higher than 120% of VSYS, the RAA489800 transitions from Buck-Boost mode to Buck mode under any circumstance. At a heavier load, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the voltage regulator circuit.

When the ADP voltage V_{ADP} is falling and is lower than 112% of the system bus voltage VSYS, the RAA489800 transitions from Buck mode to Buck-Boost mode. If V_{ADP} is lower than 80% of VSYS, the RAA489800 transitions from Buck-Boost mode to Boost mode.

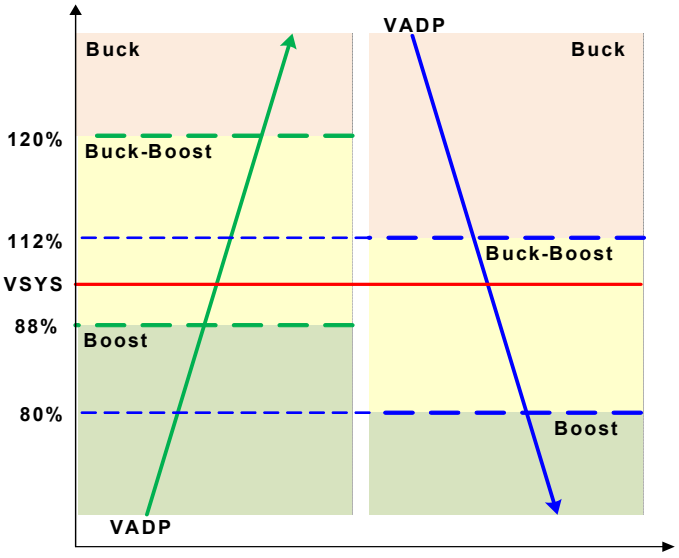


Figure 31. Operation Mode

When the reverse function is enabled with the SMBus command or RVSEN pin, and if the reverse voltage VSYS is higher than 4.1V, the RAA489800 operates in Reverse mode.

The RAA489800 can be configured to operate in 2-Switch Buck mode as shown in Figure 3. 2-Switch Buck mode can be selected based on the PROG pin resistor shown in Table 21. When selecting 2-Switch Buck mode, configure the UGATE2, PHASE2, and BOOT2 pins as shown in Figure 2. The controller operates in Buck mode only, disabling boost and buck-boost control loops.

6.3 Pass Through Mode

The RAA489800 has a Pass Through Mode (PTM) for improved light load efficiency. You can enable PTM with Control1 register Bit 4. When the PTM control bit is enabled, the REF ramps to the input voltage and the switcher continues switching until the output voltage is in the 300mV window to the input. When the regulating voltage is within the 300mV window to the input voltage, the latch is set to stop switching, Q1 and Q4 are always on while Q2 and Q3 are always off (except during BOOT capacitor refresh time), and UV and OV are disabled. To exit PTM, set Control1 register Bit 4 to zero. The REF ramps to the DAC value and switching resumes.

6.4 Soft-Start

The RAA489800 includes a low power LDO with a nominal 5V output, with an input that is OR-ed from the VOUT pin and ADP pin. The RAA489800 also includes a high power LDO with a nominal 5V output, with an input from the DCIN pin connected to the ADP and the system bus through an external OR-ing diode circuit. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for the RAA489800. The VDDP pin is the RAA489800 gate drive power supply input. Use an RC filter to generate the VDDP pin voltage from the VDD pin voltage.

The RAA489800 digital block is activated when V_{DD} > 2.7V. The soft-start time can be set by the external capacitor on the REF pin. The RAA489800 sources 2µA current out of the REF pin to charge this external capacitor. Its voltage is used as the output voltage reference in the soft-start procedure.

6.5 Programming Options

The resistor from the PROG pin to GND programs the forward output voltage configuration of the RAA489800. Table 21 shows the programing options.

Table 21. PROG Pin Programming Options

PROG-GND Resistance (kΩ)			Force 2-FET	Default Forward Regulating Output (V)	Default Forward Input Current Limit (A)
Min	Typ	Max			
0	7.5	14.9	0	5	0.476
20.7	21.0	21.3	0	5	2.848
27.7	28.0	28.3	0	9	0.476
35.3	35.7	36.1	0	9	2.848
42.7	43.2	43.7	0	12	0.476
51.7	52.3	52.9	0	12	2.848
61.2	61.9	62.6	0	15	0.476
70.6	71.5	72.4	0	15	2.848
81.5	82.5	83.5	0	20	0.476
92.0	99.0	106.0	1	20	2.848
116.0	118.0	120.0	1	20	0.476
131.0	133.0	135.0	1	15	2.848
145.0	147.0	149.0	1	15	0.476
160.0	162.0	164.0	1	12	2.848
176.0	178.0	180.0	1	12	0.476
194.0	196.0	198.0	1	9	2.848
212.0	215.0	218.0	1	9	0.476
234.0	237.0	240.0	1	5	2.848
258.0	261.0	264.0	1	5	0.476

The switching frequency can be changed through SMBus Control1 register Bit<9:7> after POR. See Table 11 for a detailed description.

After POR, the RAA489800 sources 10µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. If the RAA489800 is powered up from reverse side, it does not read the PROG resistor. When FRWEN is enabled, the RAA489800 resets the forward regulating voltage register to its default value according to the PROG pin setting.

By default, the ADP current-sensing resistor Rs1 is 20mΩ and the VSYS current-sensing resistor Rs2 is 10mΩ. Using these Rs1 = 20mΩ and Rs2 = 10mΩ options results in a 4mA/LSB correlation in the SMBus current commands.

If the Rs1 and Rs2 values are different from these Rs1 = 20mΩ and Rs2 = 10mΩ options, the SMBus command needs to be scaled accordingly to obtain the correct current. Smaller current-sense resistor values reduce the power loss whereas larger current-sense resistor values give better accuracy.

The information in this datasheet is based on current-sensing resistors Rs1 = 20mΩ and Rs2 = 10mΩ unless specified otherwise.

6.6 DE Operation

In DE operation mode, the RAA489800 uses a phase comparator to monitor the PHASE node voltage to the ground or VOUT or ADP voltage during the low-side switching FET on-time to detect the inductor current zero crossing, depending on the operation mode (Buck, Buck-Boost, or Boost) and power delivery direction (forward or reverse direction). See Table 22 for more information. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the RAA489800 may lose diode emulation ability. To prevent this, the RAA489800 uses a minimum low-side switching FET on-time. When

the intended low-side switching FET on-time is shorter than the minimum value, the RAA489800 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

Table 22. Voltage Comparator for DE Operation

Mode	Direction	Voltage Comparator
Buck	Forward	PHASE1 to GND
Boost	Forward	PHASE2 to VOUT
Buck-Boost	Forward	PHASE2 to VOUT
Buck	Reverse	PHASE2 to GND
Boost	Reverse	PHASE2 to VOUT
Buck-Boost	Reverse	PHASE2 to VOUT or PHASE2 to GND

6.7 Forward Mode

When the forward function is enabled with the SMBus command or the FRWEN pin (voltage is higher than 0.8V) and DCIN is powered by ADP, and if ADP is plugged in and its value is higher than 4.1V, the RAA489800 can operate in Forward Buck mode, Forward Boost mode, Forward Buck-Boost mode, or Forward Pass Through mode. After the forward output voltage reaches the regulating output voltage range set by register 0x15H Bit<14:3>, forward power-good FWGPG asserts to High.

6.8 Reverse Mode for USB OTG (On-The-Go)

When the reverse function is enabled with the SMBus command (Control1 Bit<11>) or the RVSEN pin, and if an external voltage is on the system side and its value is higher than 4.1V, the RAA489800 can operate in Reverse Buck mode, Reverse Boost mode, Reverse Buck-Boost mode, or Reverse Pass Through mode. RVSEN is the digital input pin. The 1.3s or 150ms debounce time can be set by Control2 register Bit<13>. After the reverse output voltage reaches the output voltage set by register 0x49H Bit<14:3>, reverse power-good RVSPG asserts to High.

Before Reverse mode starts switching, the CSIP pin voltage must first drop below the reverse output overvoltage protection threshold (ReverseRegulatingVoltage + 1177mV).

The default reverse output voltage is 5V and programmable up to 21V in Reverse Buck, Reverse Buck-Boost, and Reverse Boost mode. In Reverse Pass Through mode, the maximum value of the reverse output voltage is programmable up to 21V. The reverse voltage register 0x49H can configure the reverse output voltage.

6.9 Overcurrent Warning

The RAA489800 provides an Overcurrent Warning feature. The overcurrent warning option can be set by Control2<2>. When Control2<2> is set to 0, if the system output current is higher than the SystemCurrentLimit register set value, the RAA489800 enters the output current limit mode and ALERT# is asserted. The output current is regulated at the SystemCurrentLimit set value and system output voltage drops.

When Control2<2> is set to 1, if the system output current is higher than the SystemCurrentLimit register set value, the RAA489800 declares an overcurrent warning and ALERT# is asserted. The output current is not regulated at the SystemCurrentLimit set value and the system output voltage is regulated normally.

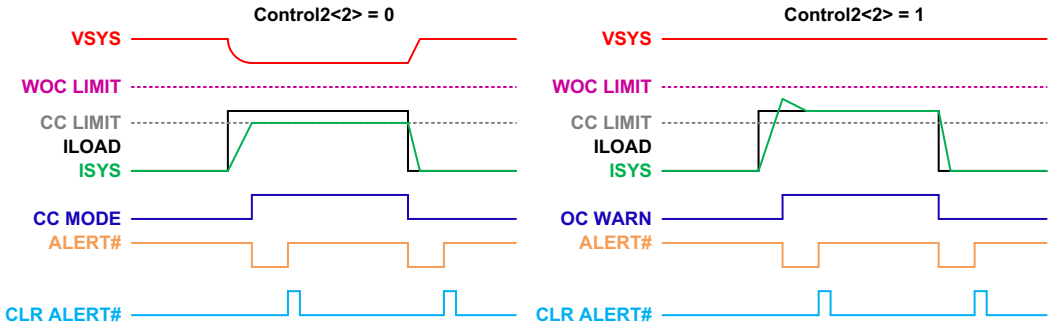


Figure 32. Overcurrent Warning

6.10 VSYS Low Voltage Shutdown

The RAA489800 has a VSYS low voltage shutdown feature if UVP is disabled. The low voltage shutdown option can be controlled by Control0<4> and Control0<3>. The low voltage shutdown is enabled when Control0<4> is set to 1. While enabled, if VSYS drops below 3V, the system triggers a shutdown. The threshold for the low voltage shutdown option can be configured to either 3V or 3.3V by setting Control0<3>.

Figure 33. VSYS Low Voltage Shutdown

6.11 PGOOD Window Control

The RAA489800 has an option to configure the PGOOD window to control when PGOOD is asserted in case of a voltage transition by setting the DAC. By default, the PGOOD is defined by a window around REF. When a new output voltage reference is set by the DAC, REF ramps to the new set-point and the PGOOD window follows the REF. The output voltage follows the REF transition but the slew rate can be different than the REF. PGOOD goes Low when output voltage falls out of the window and goes High again when the output voltage is back inside the window.

The PGOOD window can be reconfigured around the DAC by setting Control3<4> to 1. In this case, the PGOOD window is defined around the value set by the DAC. When the output voltage reference is set by the DAC, the window is shifted to the new set point. PGOOD goes Low immediately and goes High again when the output voltage is back inside the window. Figure 34 explains the PGOOD behavior in detail.

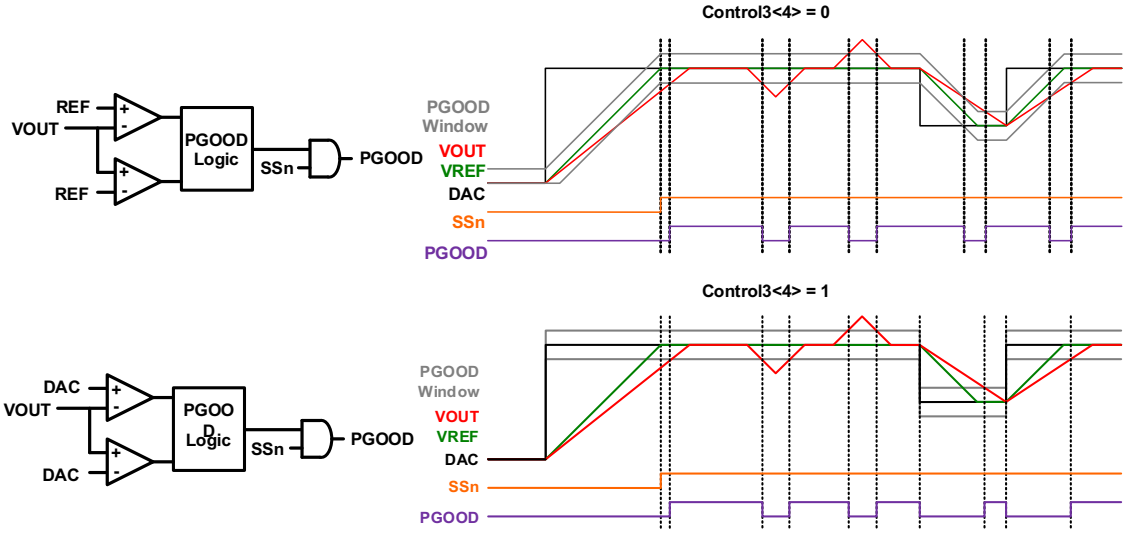


Figure 34. PGOOD Window Control

6.12 Fast REF

To achieve fast REF in some applications, the fast REF function can be programmed by Control1 Bit<3>. If this bit is programmed, the 1µA current source for REF pin is replaced with 5k impedance to get faster transitions for REF voltage.

6.13 Fast Swap

The RAA489800 provides a fast swap function in Forward mode and Reverse mode. Implement the fast swap function in Forward mode using either pin reverse or software reverse by completing the following steps:

- **Pin reverse fast swap enable:**

1. Program Control2 Bit<4> (Reverse Fast Swap).
2. Skip trim during restart by programming Control1 Bit<13>.
3. Skip autozero during restart by programming Control1 Bit<12>.
4. Enable the RVSEN pin.

- **Software reverse fast swap enable:**

1. Program Control1 Bit<0> (Force 5.04V VDAC).
2. Program Control1 Bit<3> (Fast REF).
3. Skip trim during restart by programming Control1 Bit<13>.
4. Skip autozero during restart by programming Control1 Bit<12>.
5. Program Control1 Bit<11> (Force Reverse mode).

Similarly, you can implement the fast swap function in Reverse mode using either pin forward or software forward by completing the following steps:

- **Pin forward fast swap enable:**

1. Program Control2 Bit<3> (Forward Fast Swap).
2. Skip trim during restart by programming Control1 Bit<13>.
3. Skip autozero during restart by programming Control1 Bit<12>.
4. Disable the RVSEN pin.
5. Enable the FWREN pin.

- **Software forward fast swap enable:**

1. Program Control1 Bit<0> (Force 5.04V VDAC).
2. Program Control1 Bit<3> (Fast REF).
3. Skip trim during restart by programming Control1 Bit<13>.
4. Skip autozero during restart by programming Control1 Bit<12>.
5. Un-program Control1 Bit<1> (Force Reverse mode).

6.14 Way Overcurrent Protection (WOCP)

The RAA489800 provides Way Overcurrent Protection (WOCP) against MOSFET shorts, system side and ADP side shorts, and inductor shorts. The RAA489800 monitors the CSIP - CSIN voltage and VOUT - CSON voltage and compares them to the WOCP threshold (12A for ADP current and 20A for system side current in Forward mode).

When the WOC comparator is tripped, the RAA489800 counts one time within each 10µs window. If the RAA489800 counts WOC to seven times in 50ms, it stops switching immediately. After the 1.3s or 150ms debounce time is set by Control2 register Bit<12>, the RAA489800 goes through the startup sequence to retry.

The WOCP function can be disabled through Control2 register Bit<1>.

6.15 ADP Input Overvoltage Protection

If the ADP pin input voltage exceeds 26.4V for more than 10µs, the RAA489800 declares an ADP overvoltage condition and stops switching. When the ADP voltage drops below 26.4V for more than 100µs, the RAA489800 starts to switch.

6.16 System Output Overvoltage Protection

The RAA489800 provides system rail output overvoltage protection. If the system voltage VOUTS is 1095mV higher than the ForwardRegulatingVoltage register set value for more than 100µs, it declares the system overvoltage, deasserts FWRPG, and stops switching. It resumes switching with the 100µs debounce time when VOUTS is less than 542mV plus the setting reference voltage for forward.

The RAA489800 system output voltage also has an absolute overvoltage protection. If the system output voltage is higher than 23.5V for more than 10µs, the RAA489800 declares an absolute system overvoltage condition and stops switching. The device resumes switching as soon as this voltage falls by 650mV for more than 100µs.

6.17 System Output Undervoltage Protection

The RAA489800 provides system rail output undervoltage protection. If the system voltage VOUTS is 818mV lower than the ForwardRegulatingVoltage register set value for more than 1ms, it declares the system undervoltage, de-asserts FWRPG, and restarts.

6.18 ADP Output Overvoltage Protection

The RAA489800 provides ADP rail output overvoltage protection. If the ADP voltage ADPS is 1177mV higher than the ReverseRegulatingVoltage register set value for more than 100µs, it declares the ADP overvoltage, de-asserts RVSPG, and stops switching. The RAA489800 resumes switching with the 100µs debounce when ADPS is less than 583mV plus the setting reference voltage for reverse.

6.19 ADP Output Undervoltage Protection

The RAA489800 provides ADP rail output undervoltage protection. If the ADP voltage VADPS is 1177mV lower than the ReverseRegulatingVoltage register set value for more than 1ms, it declares the ADP undervoltage, de-asserts RVSPG, and stops switching.

6.20 Over-Temperature Protection

The RAA489800 stops switching for self protection when the junction temperature exceeds +140°C.

The RAA489800 starts switching when the temperature falls below +120°C and after a 100µs delay.

6.21 Switching Power MOSFET Gate Capacitance

The RAA489800 includes an internal 5V LDO output at the VDD pin, which can provide the switching MOSFET gate driver power through the VDDP pin with an RC filter. The 5V LDO output overcurrent protection threshold is 115mA, nominal. When selecting the switching power MOSFET, carefully consider the MOSFET gate capacitance to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 1:

(EQ. 1) $$I_{driver} = Q_g \bullet f_{SW}$$

where:

- Q_g is the total gate ADP which can be found in the MOSFET datasheet
- f_{SW} is the switching frequency

Renesas recommends connecting a 2.2µF ceramic capacitor from the VDD and VDDP pins to GND. The effective capacitance of the MLCC at 5V must be at least 0.4µF after derating and at least 1.6 times the effective capacitance at the BOOT pin. Use a X7R or X5R ceramic capacitor.

6.22 ADP Side Input Filter

The ADP cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the ADP connector node when the ADP is hot plugged in. This voltage spike can damage the RAA489800 pins connecting to the ADP connector node. One low cost solution is to add an RC snubber circuit at the ADP connector node to clamp the voltage spike as shown in Figure 35. A practical value of the RC snubber is 2.2Ω to 2.2µF; however, the appropriate values and power rating should be carefully characterized based on the actual design. Additionally, it is not recommended to add a pure capacitor at the ADP connector node, which can cause an even larger voltage spike due to the ADP cable or the ADP current path parasitic inductance.

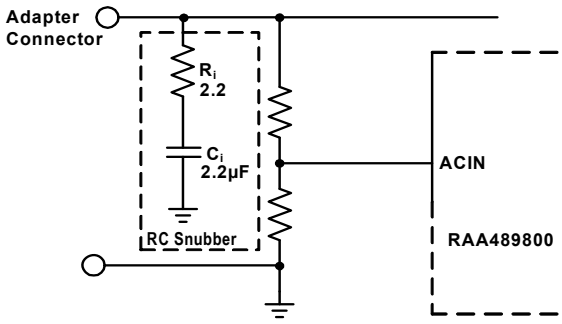


Figure 35. Adapter Input RC Snubber Circuit

7. General Application Information

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Renesas provides complete reference designs that include schematics, bills of materials, and example board layouts.

7.1 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. This relationship is written by Equation 2:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 2)}$$

The output inductor peak-to-peak ripple current is written by Equation 3:

$$I_{P\text{-}P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L} \quad \text{(EQ. 3)}$$

A typical step-down DC/DC converter has an $I_{P\text{-}P}$ of 20% to 40% of the maximum DC output load current for a practical design. The value of $I_{P\text{-}P}$ is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 4:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 4)}$$

where I_{LOAD} is the converter output DC current.

The copper loss can be significant, so select the DCR carefully. Consider the inductor's saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance C_O, into which ripple current $I_{P\text{-}P}$ can flow. Current $I_{P\text{-}P}$ develops a corresponding ripple voltage $V_{P\text{-}P}$ across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from ADP moved in and out of the capacitor. These two voltages are written by Equations 5 and 6:

$$\Delta V_{ESR} = I_{P\text{-}P} \cdot ESR \quad \text{(EQ. 5)}$$

$$\Delta V_C = \frac{I_{P\text{-}P}}{8 \cdot C_O \cdot f_{SW}} \quad \text{(EQ. 6)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required $V_{P\text{-}P}$ is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Consider low inductance capacitors in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that $I_{P\text{-}P}$ is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at f_{SW}. The rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

7.2 Selecting the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. The Typical Application Circuit in 4-Switch Buck-Boost Configuration is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 7:

(EQ. 7)
$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1 - D) + \frac{D \cdot k^2}{12}}}{I_{MAX}}$$

where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a ratio of I_{MAX} (0 to 1)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 8:

(EQ. 8)
$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

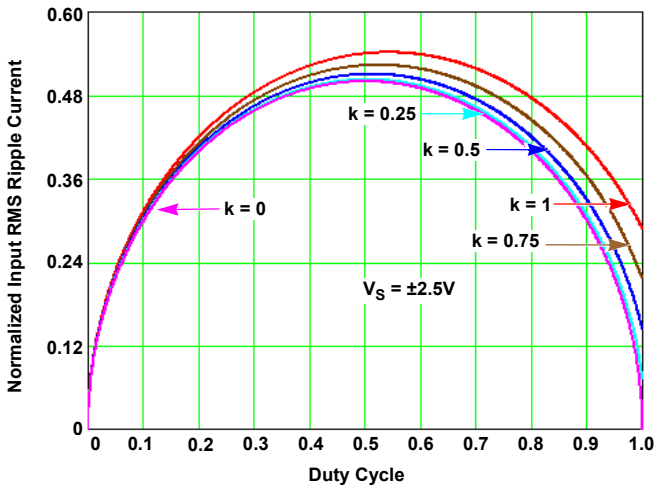


Figure 36. Normalized RMS Input Current at EFF = 1

7.3 Selecting the Switching Power MOSFET

Typically, MOSFETs cannot tolerate even brief excursions beyond their maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs are readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate ADP so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its

body diode during turn-off, the high-side MOSFET turns off with a VDS of approximately V_{IN} - V_{OUT}, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. Note: This is an optimal MOSFET selection configuration for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high- and low-side devices may be warranted.

For the low-side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as Equation 9:

$$P_{CON\_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)\_LS} \cdot (1 - D) \quad \text{(EQ. 9)}$$

For the high-side (HS) MOSFET, the conduction loss is written as Equation 10:

$$P_{CON\_HS} = I_{LOAD}^{2} \cdot r_{DS(ON)\_HS} \cdot D \quad \text{(EQ. 10)}$$

For the high-side MOSFET, the switching loss is written as Equation 11:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{SW(ON)} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{SW(OFF)} \cdot f_{SW}}{2} \quad \text{(EQ. 11)}$$

where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{SW(ON)}$ is the time required to drive the device into saturation
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off

7.4 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 12.

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 12)}$$

where:

- Q_g is the total gate ADP required to turn on the high-side MOSFET
- ΔV_{BOOT} is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate ADP Q_g of 25nC at V_{GS} = 5V and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF will suffice.

Renesas recommends using a 0.47µF ceramic capacitor at the BOOT pin. The effective capacitance of the MLCC at 5V must be at least 0.25µF after derating and at least 50 times the effective high side MOSFET gate capacitance. Use a X7R or X5R ceramic capacitor.

7.5 Selecting the Resistor Divider for VOUTS and ADPS

ADPS and VOUTS are output voltage feedback pins, in Reverse mode and Forward mode, respectively, that allow you to change the output voltage by the resistor divider (R_1, R_2, and R_3, R_4), as shown in Figure 37. There is an equivalent resistance of 600kΩ inside from VOUTS and ADPS to ground. For example, in Forward mode, the VSYS voltage magnitude can be revised by tuning the R_1 and R_2 values, written by Equation 13. Thus, there is no need to change the Forward Regulating Voltage register (0x15H) through the GUI. The same process can be applied at the ADPS pin. The external resistances for R_1, R_2, R_3, and R_4 must be selected carefully to avoid overloading the internal equivalent resistances. Renesas recommends using external resistors with less than 100kΩ value.

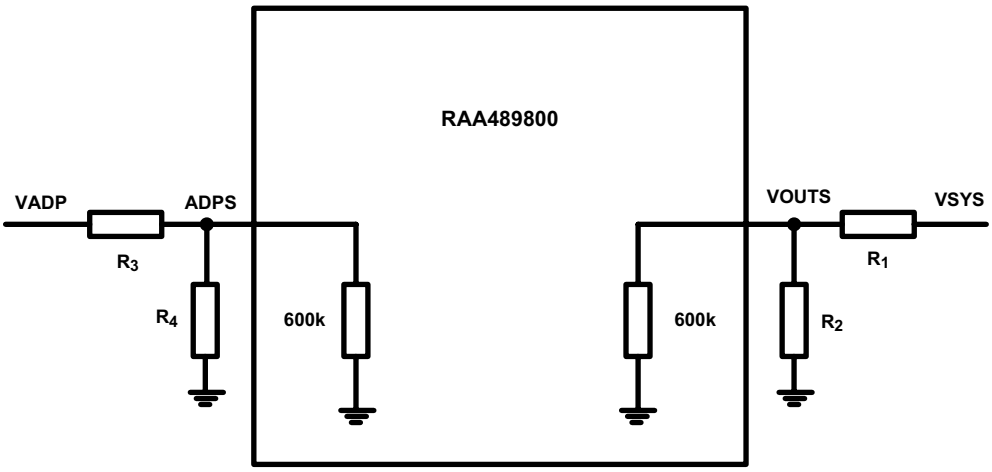


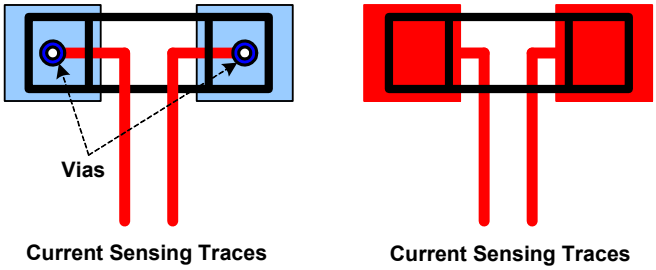
Figure 37. Resistor Divider for VOUTS and ADPS

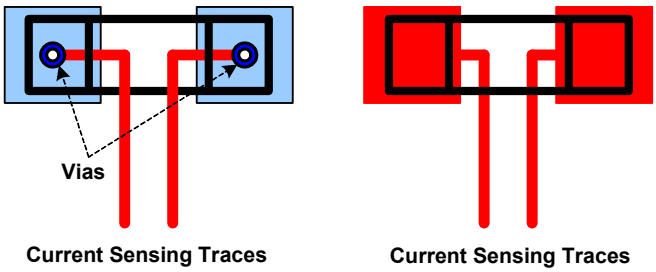
(EQ. 13) $$V_{OUTS} = V_{SYS}\frac{(600k\Omega \backslash\backslash R_2)}{(600k\Omega \backslash\backslash R_2) + R_1}$$

7.6 Selecting the DCIN Filter

When the ADP is plugged in, it can cause some voltage spike at the DCIN node. This voltage spike can cause damage to the associated pins and the internal LDO of the RAA489800. Therefore, a simple RC filter must be connected at the DCIN pin to minimize the effect of the voltage spike. Renesas recommends using a 4.7Ω resistor and a 4.7µF ceramic capacitor as the RC filter at the DCIN pin. The effective capacitance of the MLCC at 20V must be at least 0.4µF after derating. Use a X7R or X5R ceramic capacitor.

8. Layout

Pin Number	Pin Name	Layout Guidelines
Bottom Pad	GND	Connect this ground pad to the ground plane through a low impedance path. Renesas recommends using at least five vias to connect to the ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC.
1	CSON	Run two dedicated trace with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
2	CSOP	
3	VOUTS	Signal pin that provides feedback for the forward system bus voltage. Run a dedicated trace from system bus to the pin and do not route near the switching traces. Do not share the same trace with the signal routing to the DCIN pin OR diodes.
4	BOOT2	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use decent wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
5	UGATE2	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing the PHASE2 trace to high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation, but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
6	PHASE2	
7	LGATE2	Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
8	VDDP	Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to VDD pin with sufficient width.
9	LGATE1	Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close.
10	PHASE1	Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing the PHASE1 trace to high-side MOSFET source pin instead of general copper. Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs. Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection. Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB.
11	UGATE1	

Pin Number	Pin Name	Layout Guidelines
12	BOOT1	Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use decent wide trace. Avoid any sensitive analog signal trace from crossing over or getting close.
13	ADPS	Run this trace with sufficient width parallel to the ADP pin trace.
14	CSIN	Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the Differential mode and common-mode RC filter components in the general proximity of the controller. Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces. 
15	CSIP	
16	ADP	Run this trace with sufficient width parallel to the ADPS pin trace.
17	DCIN	Place the OR diodes and the RC filter in the general proximity of the controller. Run the VADP trace and VSYS trace to the OR diodes with sufficient width.
18	VDD	Place the RC filter connecting with VDDP pin in the general proximity of the controller. Run the trace connecting to VDDP pin with sufficient width.
19	FRWEN	No special consideration.
20	RVSEN	No special consideration.
21	SDA	Digital pins. No special consideration. Run the SDA and SCL traces in parallel.
22	SCL	
23	ALERT#	Digital pin, open-drain output. No special consideration.
24	FRWPG	Digital pin, open-drain output. No special consideration.
25	ADDR0	No special consideration.
26	RVSPG	Digital pin, open-drain output. No special consideration.
27	PROG	Signal pin. Place the PROG programming resistor in the general proximity of the controller.
28	COMPF	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
29	REF	Place the reference capacitor in the general proximity of the controller.
30	COMPR	Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close.
31	VOUT	Run a dedicated trace from system bus to the pin and do not route near the switching traces.
32	ADDR1	No special consideration.

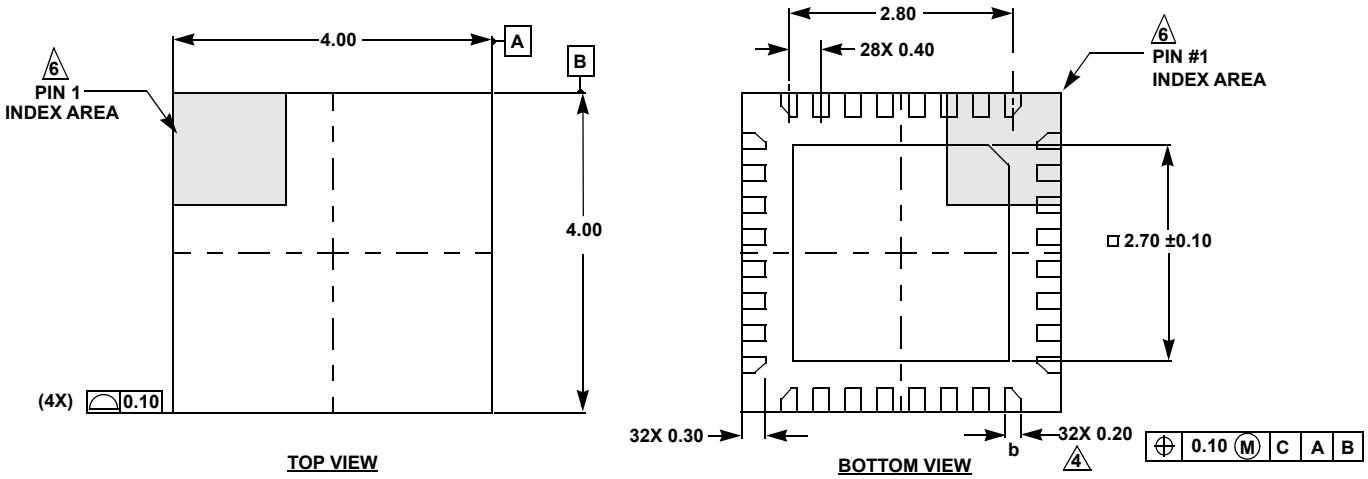
9. Revision History

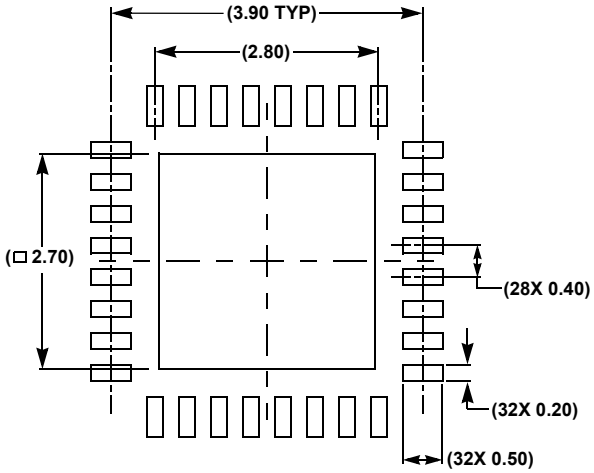
Rev.	Date	Description
1.02	Oct 21, 2021	Added Features bullet. Updated System Output Overvoltage Protection section. Updated Ordering Information table formatting.
1,01	Sep 25, 2020	Update Figure 23. SMBus Read and Write Protocol
1.00	May 28, 2020	Corrected evaluation board part number. Updated Table 10 Bit<6:5> description.
0.00	Jul 15, 2019	Initial release

10. Package Outline Drawing

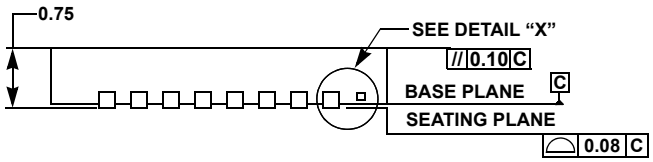
For the most recent package outline drawing, see L32.4x4D.

L32.4x4D
32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/16

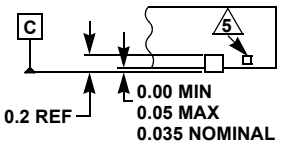




TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
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