RAA788170, RAA788172, RAA788173, RAA788175, RAA788176, RAA788178

3.3V, Full Fail-Safe, Low-Power, RS-485 Transceivers with 3kV EFT Immunity and 15kV ESD Protection

The RAA78817x family (RAA788170, RAA788172, RAA788173, RAA788175, RAA788176, RAA788178) of 3.3V powered single transceivers feature high output drive and high EFT and ESD protection. The devices are immune to ±3kV IEC61000-4-4 EFT transients and withstand ±15kV IEC61000-4-2 ESD strikes without latch-up. These devices have low bus currents (+125µA/-100µA), so they present a true 1/8 unit load to the RS-485 bus. This allows up to 256 transceivers on the network without violating the RS-485 specification 32 unit load maximum, and without using repeaters. For example, in a remote utility meter reading system, individual meter readings are routed to a concentrator using an RS-485 network, so the high allowed node count minimizes the number of repeaters required.

Receiver (Rx) inputs feature a Full Fail-Safe design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

Hot Plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state while the power supply stabilizes.

The RAA788170 through RAA788175 use slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications. Slew rate limited versions also include receiver input filtering to enhance noise immunity in the presence of slow input signals.

The RAA788170, RAA788173, and RAA788176 are configured for full duplex (separate Rx input and Tx output pins) applications. The half duplex versions multiplex the Rx inputs and Tx outputs to allow transceivers with output disable functions in 8 Ld packages.

Features

- IEC61000 ESD protection on RS-485 I/O pins: ±15kV
  - Class 3 ESD level on all other pins: >7kV HBM
- ±3kV EFT immunity of bus I/O pins
- Full fail-safe (open, short, terminated/floating) receivers
- Hot plug - Tx and Rx outputs remain three-state during power-up
- True 1/8 unit load allows up to 256 devices on the bus
- Single 3.3V supply
- High data rates: up to 20Mbps
- Low quiescent supply current: 800µA (Max)
  - Ultra low shutdown supply current: 10nA
- -7V to +12V common-mode input/output voltage range
- Half and full duplex pinouts
- Three state Rx and Tx outputs available
- Current limiting and thermal shutdown for driver overload protection
- Tiny MSOP packages consume 50% less board space
- Pb-free (RoHS compliant)

Applications

- Automated utility meter reading systems
- High node count systems
- Field bus networks
- Security camera networks
- Building environmental control/lighting systems
- Industrial/process control networks

Table 1. Summary of Features

Part Number	Duplex	Data Rate (Mbps)	Slew-Rate Limited?	Hot Plug?	# Devices on Bus	RX/TX Enable?	Quiescent I_{CC} (µA)	Low Power Shutdown?	Pin Count
RAA788170	Full	0.25	Yes	Yes	256	Yes	510	Yes	10, 14
RAA788172	Half	0.25	Yes	Yes	256	Yes	510	Yes	8
RAA788173	Full	0.5	Yes	Yes	256	Yes	510	Yes	10, 14
RAA788175	Half	0.5	Yes	Yes	256	Yes	510	Yes	8
RAA788176	Full	20	No	Yes	256	Yes	510	Yes	10, 14
RAA788178	Half	20	No	Yes	256	Yes	510	Yes	8

Contents

1. Overview

1.1 Typical Operating Circuits

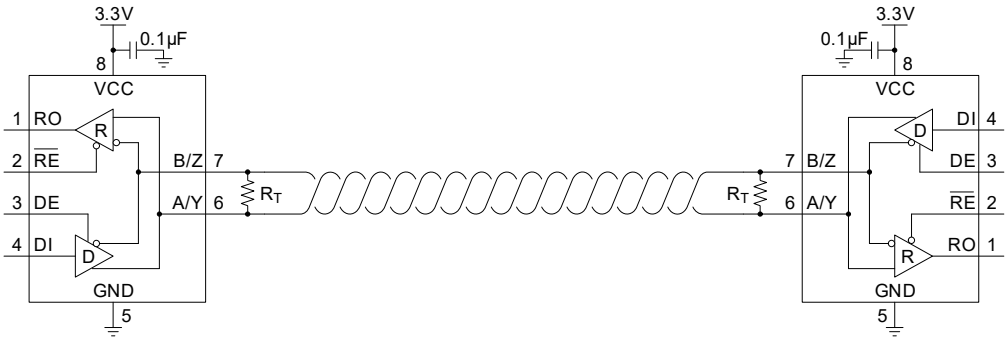


Figure 1. RAA788172, RAA788175, RAA788178

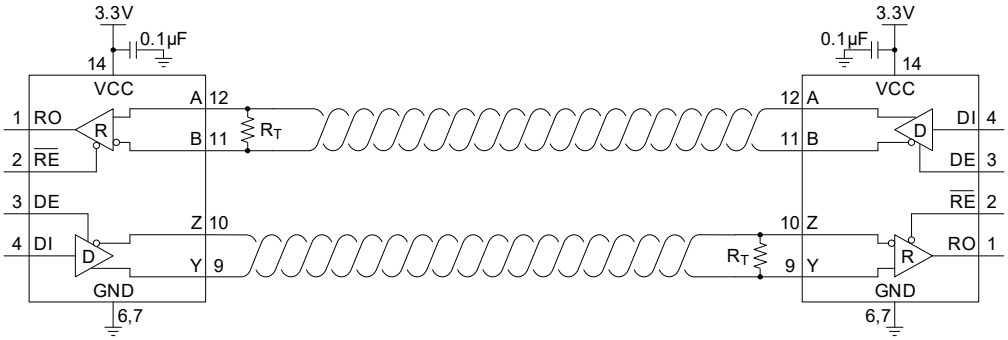
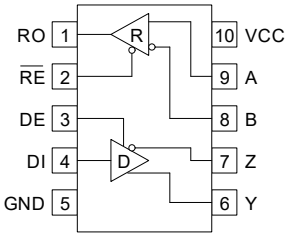


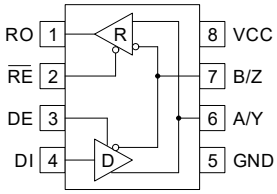
Figure 2. RAA788170, RAA788173, RAA788176

2. Pin Information

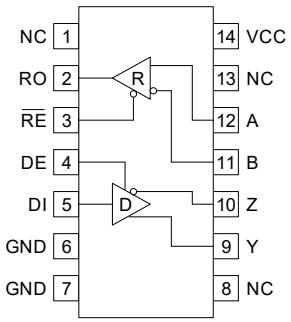
2.1 Pin Assignments



10 Ld MSOP
Top View



8 Ld SOIC, MSOP
Top View



14 Ld SOIC
Top View

2.2 Truth Tables

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z[1]	High-Z[1]

1. Shutdown Mode

Receiving				
Inputs				Output
$\overline{RE}$	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	$V_{AB} \geq -0.05V$	1
0	0	X	$-0.05V > V_{AB} > -0.2V$	Undetermined
0	0	X	$V_{AB} \leq -0.2V$	0
0	0	X	Inputs Open/Shorted	1
1	0	X	X	High-Z[1]
1	1	X	X	High-Z

1. Shutdown Mode

2.3 Pin Descriptions

Pin	Function
RO	Receiver output: If A-B ≥ -50mV, RO is high; If A-B ≤ -200mV, RO is low; if A and B are unconnected (floating) or shorted, RO = High.
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND or through a 1kΩ to 3kΩ resistor to GND.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the Tx enable function is not required, connect DE to VCC through a 1kΩ to 3kΩ resistor.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection.
A/Y	±15kV IEC61000 ESD Protected RS-485/422 level, non-inverting receiver input and non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	±15kV IEC61000 ESD Protected RS-485/422 level, Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	±15kV IEC61000 ESD Protected RS-485/422 level, non-inverting receiver input.
B	±15kV IEC61000 ESD Protected RS-485/422 level, inverting receiver input.
Y	±15kV IEC61000 ESD Protected RS-485/422 level, non-inverting driver output.
Z	±15kV IEC61000 ESD Protected RS-485/422 level, inverting driver output.
VCC	System power supply input (3.0V to 3.6V).
NC	No Connection.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC to GND		7	V
Input Voltages			
DI	-0.3	7	V
DE, $\overline{RE}$[1]	-0.3	7	V
Input/Output Voltages			
A, B, Y, Z	-8	13	V
RO	-0.3	V_{CC} + 0.3	
Short-Circuit Duration			
Y, Z		Continuous	

1. If the DE or $\overline{RE}$ input voltage exceeds the V_{CC} voltage by more than 500mV, current flows into the logic pin. The current is limited by a 340Ω resistor (so ≈ 13mA with V_{IN} = 5V and V_{CC} = 0V) so no damage occurs if $V_{CC} \leq V_{IN} \leq 7V$ for short periods of time.

3.2 ESD Ratings

ESD Model/Test/Condition	Rating	Unit
IEC61000-4-2, Air-Gap Discharge Method - RS-485 Pins (A, Y, B, Z, A/Y, B/Z)	±15	kV
IEC61000-4-2, Contact Discharge Method - RS-485 Pins (A, Y, B, Z, A/Y, B/Z)	±8	kV
Human Body Model (Tested per JS-001-2017) - RS-485 Pins (A, Y, B, Z, A/Y, B/Z) from Bus pins to GND	±15	kV
Human Body Model (Tested per JS-001-2017) - All pins	±7	kV
Machine Model	200	V

3.3 EFT Performance

EFT Test/Condition		Rating	Unit
IEC61000-4-4 Electrical Fast Transient Immunity - RS-485 Pins (A, Y, B, Z, A/Y, B/Z)	5kHz	±3	kV
	100kHZ		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-40	+85	°C

3.5 Thermal Specifications

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]
8 Ld SOIC Package	110
8 Ld MSOP Package	148
10 Ld MSOP Package	160
14 Ld SOIC Package	85

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.6 Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 3.6V; unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C[1]

Parameter	Symbol	Test Conditions		Temp (°C)	Min[2]	Typ	Max[2]	Unit
DC Characteristics								
Driver Differential V_{OUT}	V_{OD}	R_L = 100Ω (RS-422)[3] (Figure 3)		Full	2	2.3	-	V
		R_L = 54Ω (RS-485) (Figure 3)		Full	1.5	2	V_{CC}	V
		No Load			-	-	V_{CC}	
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 4)		Full	1.5	2.2	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 3)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 3)		Full	-	2	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 3)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DI, DE, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DI, DE, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Hysteresis	V_{HYS}	DE, $\overline{RE}$ [4]		25	-	100	-	mV
Logic Input Current	I_{IN1}	DI = DE = $\overline{RE}$ = 0V or V_{CC}[5]		Full	-2	-	2	µA
Input Current (A, B, A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	80	125	µA
			V_{IN} = -7V	Full	-100	-50	-	µA
Output Leakage Current (Y, Z) (Full Duplex Versions Only)	I_{IN3}	$\overline{RE}$ = 0V, DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	10	40	µA
			V_{IN} = -7V	Full	-40	-10	-	µA
Output Leakage Current (Y, Z) in Shutdown Mode (Full Duplex)	I_{IN4}	$\overline{RE}$ = V_{CC}, DE = 0V, V_{CC} = 0V or 3.6V	V_{IN} = 12V	Full	-	10	40	µA
			V_{IN} = -7V	Full	-40	-10	-	µA

Test Conditions: V_{CC} = 3.0V to 3.6V; unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C[1]

Parameter	Symbol	Test Conditions	Temp (°C)	Min[2]	Typ	Max[2]	Unit
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V[6]	Full	-	-	±250	mA
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V	Full	-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V	25	-	15	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = -50mV	Full	V_{CC} - 0.6	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = -4mA, V_{ID} = -200mV	Full	-	0.17	0.4	V
Three-State (high impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V	Full	-1	0.015	1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	Full	96	150	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}	Full	±7	30	±60	mA
Thermal Shutdown Threshold	T_{SD}		Full	-	150	-	°C
Supply Current							
No-Load Supply Current[7]	I_{CC}	DI = 0V or V_{CC}; DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}	Full	-	510	800	µA
		DI = 0V or V_{CC}; DE = 0V, $\overline{RE}$ = 0V	Full	-	480	700	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}	Full	-	0.01	12	µA
Driver Switching Characteristics (RAA788170, RAA788172, 250kbps)							
Maximum Data Rate[8]	f_{MAX}	V_{OD} = ±1.5V, C_D = 820pF (Figure 9)	Full	250	800	-	kbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)	Full	250	1100	1500	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)	Full	-	6	100	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)	Full	350	960	1600	ns
Driver Enable to Output High[9]	t_{ZH}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)	Full	-	26	600	ns
Driver Enable to Output Low[9]	t_{ZL}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)	Full	-	200	600	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)	Full	-	28	55	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)	Full	-	30	55	ns
Time to Shutdown[10]	t_{SHDN}		Full	50	200	600	ns
Driver Enable from Shutdown to Output High[10][11]	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)	Full	-	180	700	ns
Driver Enable from Shutdown to Output Low[10][11]	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)	Full	-	100	700	ns
Driver Switching Characteristics (RAA788173, RAA788175, 500kbps)							
Maximum Data Rate[8]	f_{MAX}	V_{OD} = ±1.5V, C_D = 820pF (Figure 9)	Full	500	1600	-	kbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)	Full	180	350	800	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)	Full	-	1	30	ns

Test Conditions: V_{CC} = 3.0V to 3.6V; unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C[1]

Parameter	Symbol	Test Conditions		Temp (°C)	Min[2]	Typ	Max[2]	Unit
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	200	380	800	ns
Driver Enable to Output High[9]	t_{ZH}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)		Full	-	26	350	ns
Driver Enable to Output Low[9]	t_{ZL}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	100	350	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)		Full	-	28	55	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	30	55	ns
Time to Shutdown[10]	t_{SHDN}			Full	50	200	600	ns
Driver Enable from Shutdown to Output High[10][11]	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)		Full	-	180	700	ns
Driver Enable from Shutdown to Output Low[10][11]	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	100	700	ns
Driver Switching Characteristics (RAA788176, RAA788178, 20Mbps)								
Maximum Data Rate[8]	f_{MAX}	V_{OD} = ±1.5V, C_D = 350pF (Figure 9)		Full	20	28	-	Mbps
Driver Differential Output Delay	t_{DD}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	-	27	40	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	-	1	3	ns
Driver Output Skew, Part-to-Part[12]	Δt_{DSKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	-	-	11	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 6)		Full	-	9	15	ns
Driver Enable to Output High[9]	t_{ZH}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)		Full	-	17	50	ns
Driver Enable to Output Low[9]	t_{ZL}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	16	40	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)		Full	-	25	40	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	28	50	ns
Time to Shutdown[10]	t_{SHDN}			Full	50	200	600	ns
Driver Enable from Shutdown to Output High[10][11]	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 7)		Full	-	180	700	ns
Driver Enable from Shutdown to Output Low[10][11]	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 7)		Full	-	90	700	ns
Receiver Switching Characteristics (All Versions)								
Maximum Data Rate[8]	f_{MAX}	V_{ID} = ±1.5V	RAA788170-75	Full	12	20	-	Mbps
			RAA788176-78	Full	20	35	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 12)	RAA788170-75	Full	25	70	120	ns
			RAA788176-78	Full	25	33	60	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 12)		Full	-	1.5	4	ns

Test Conditions: V_{CC} = 3.0V to 3.6V; unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C[1]

Parameter	Symbol	Test Conditions		Temp (°C)	Min[2]	Typ	Max[2]	Unit
Receiver Skew, Part-to-Part[12]	Δt_{RSKEW}	(Figure 12)		Full	-	-	15	ns
Receiver Enable to Output High[13]	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 13)	RAA788170-75	Full	5	15	20	ns
			RAA788176-78	Full	5	11	17	ns
Receiver Enable to Output Low[13]	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 13)	RAA788170-75	Full	5	15	20	ns
			RAA788176-78	Full	5	11	17	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 13)	RAA788170-75	Full	5	12	20	ns
			RAA788176-78	Full	4	7	15	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 13)	RAA788170-75	Full	5	13	20	ns
			RAA788176-78	Full	4	7	15	ns
Time to Shutdown[10]	t_{SHDN}			Full	50	180	600	ns
Receiver Enable from Shutdown to Output High[10] [14]	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 13)		Full	-	240	500	ns
Receiver Enable from Shutdown to Output Low[10][14]	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 13)		Full	-	240	500	ns

1. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
3. $V_{CC} \geq 3.15V$.
4. RAA788170 through RAA788175 only.
5. If the Tx or Rx enable function is not needed, connect the enable pin to the appropriate supply (see Pin Descriptions) through a 1kΩ to 3kΩ resistor.
6. Applies to peak current. See Typical Performance Curves for more information.
7. Supply current specification is valid for loaded drivers when DE = 0V.
8. Limits established by characterization and are not production tested.
9. When testing devices with the shutdown feature, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
10. Versions with a shutdown feature are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are ensured not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are ensured to have entered shutdown. Low Power Shutdown Mode.
11. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.
12. Δt_{SKEW} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (V_{CC}, temperature, etc.). Applies only to the RAA788176 through RAA788178.
13. When testing devices with the shutdown feature, the $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
14. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.

4. Test Circuits and Waveforms

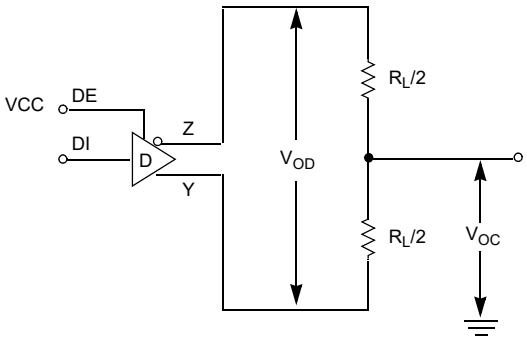


Figure 3. DC Driver Test Circuit (V_{OD} and V_{OC})

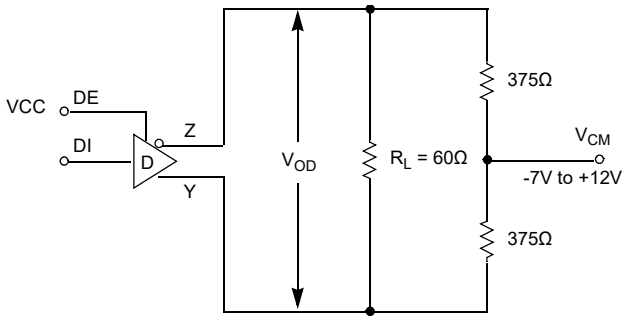


Figure 4. DC Driver Test Circuit (V_{OD} with Common Mode Load)

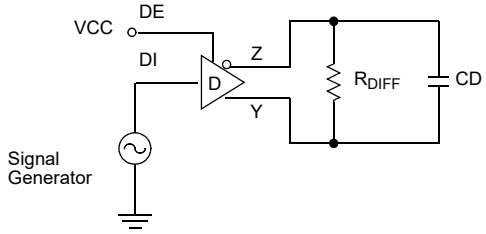


Figure 5. Driver Propagation Delay and Differential Transition Times (Test Circuit)

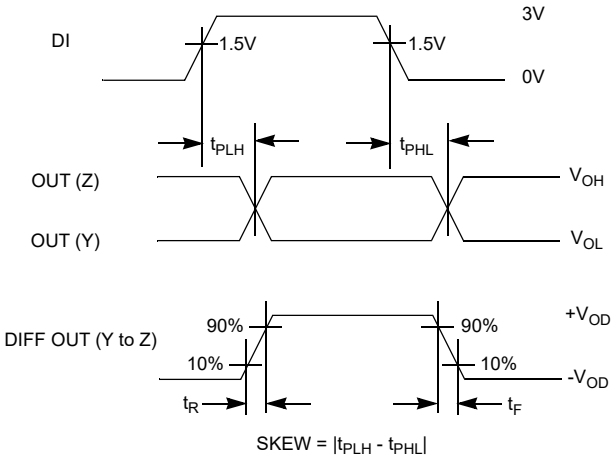
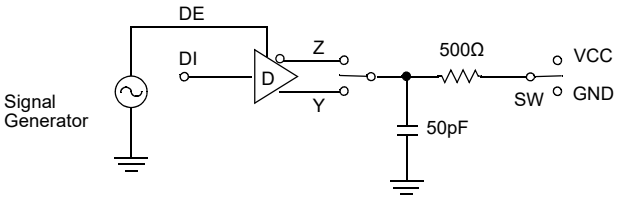


Figure 6. Driver Propagation Delay and Differential Transition Times (Measurement Points)



Parameter	Output	$\overline{RE}$	DI	SW
t_{HZ}	Y/Z	X	1/0	GND
t_{LZ}	Y/Z	X	0/1	VCC
t_{ZH}	Y/Z	0[1]	1/0	GND
t_{ZL}	Y/Z	0[1]	0/1	VCC
$t_{ZH(SHDN)}$	Y/Z	1[2]	1/0	GND
$t_{ZL(SHDN)}$	Y/Z	1[2]	0/1	VCC

1. When testing devices with the shutdown feature, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
2. Keep $\overline{RE}$ = VCC, and set the DE signal low time >600ns to ensure that the device enters SHDN.

Figure 7. Driver Enable and Disable Times (Test Circuit)

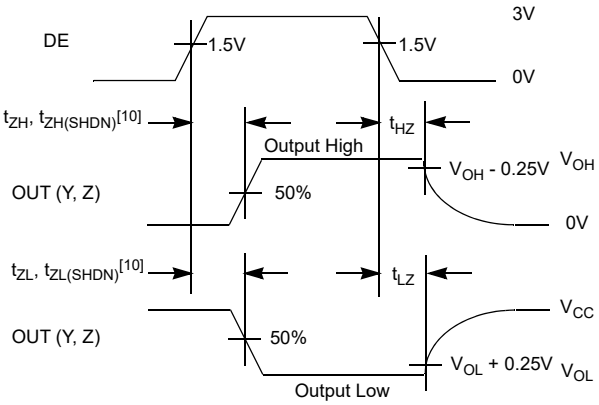


Figure 8. Driver Enable and Disable Times (Measurement Points)[11]

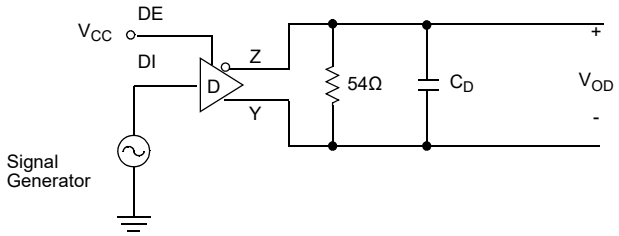


Figure 9. Driver Data Rate (Test Circuit)

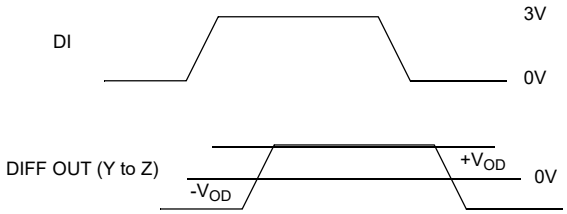


Figure 10. Driver Data Rate (Measurement Points)

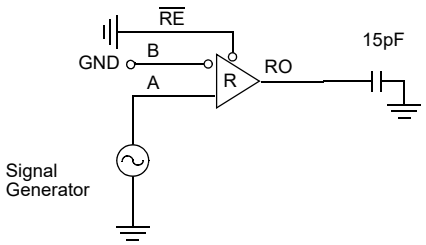


Figure 11. Receiver Propagation Delay (Test Circuit)

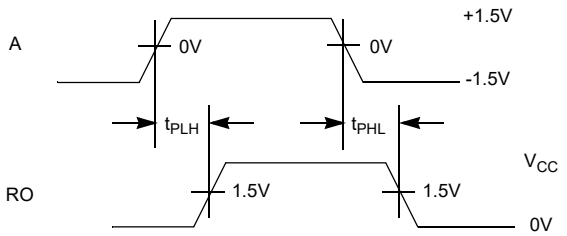
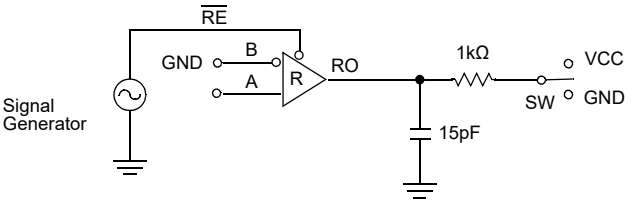


Figure 12. Receiver Propagation Delay (Measurement Points)



Parameter	DE	A	SW
t_{HZ}	X	+1.5V	GND
t_{LZ}	X	-1.5V	VCC
t_{ZH}[1]	0	+1.5V	GND
t_{ZL}[1]	0	-1.5V	VCC
$t_{ZH(SHDN)}$[2]	0	+1.5V	GND
$t_{ZL(SHDN)}$[2]	0	-1.5V	VCC

1. When testing devices with the shutdown feature, the $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
2. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters SHDN.

Figure 13. Receiver Enable and Disable Times (Test Circuit)

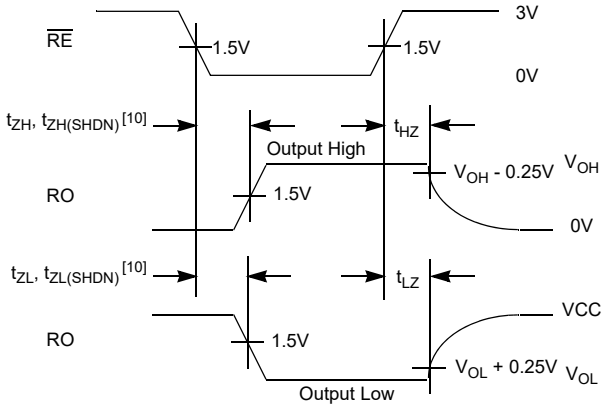


Figure 14. Receiver Enable and Disable Times (Measurement Points)[11]

5. Typical Performance Curves

V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified

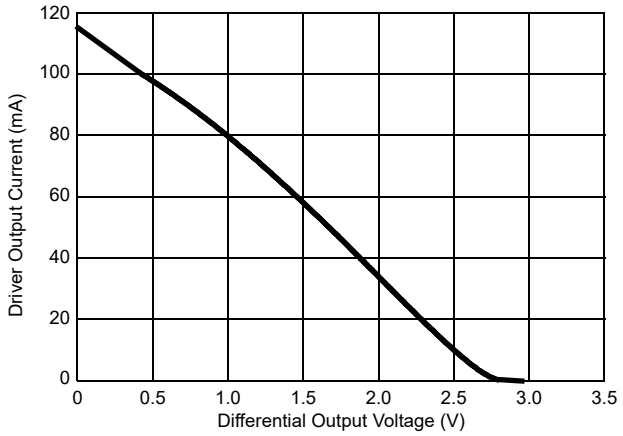


Figure 15. Driver Output Current vs Differential Output Voltage

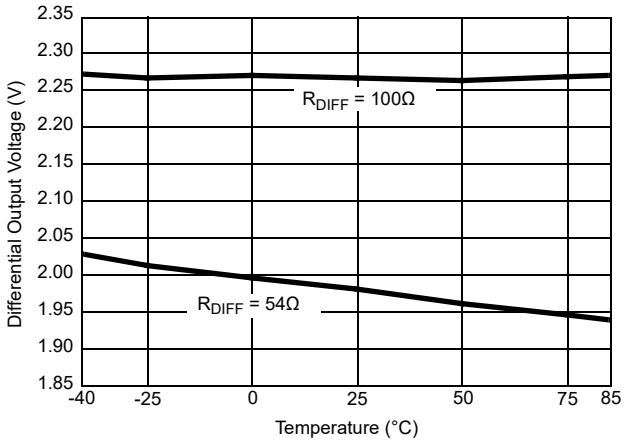


Figure 16. Driver Differential Output Voltage vs Temperature

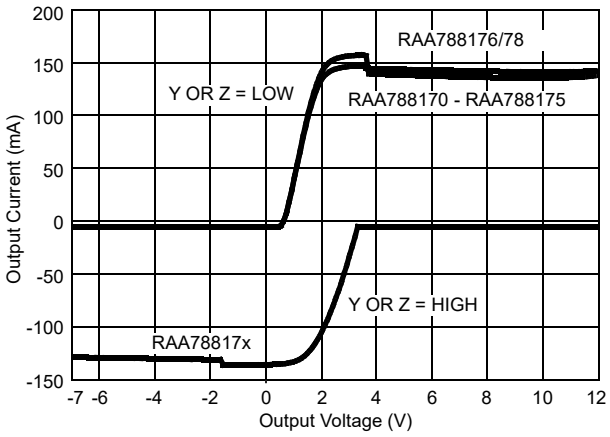


Figure 17. Driver Output Current vs Short-Circuit Voltage

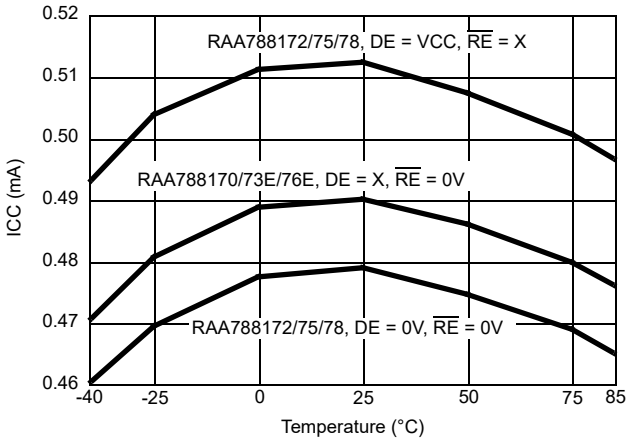


Figure 18. Supply Current vs Temperature

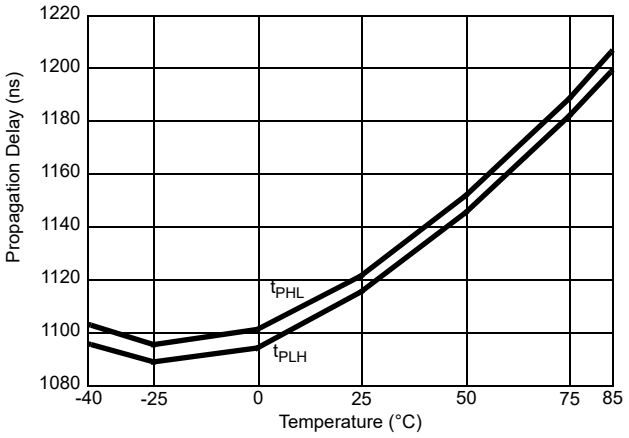


Figure 19. Driver Differential Propagation Delay vs Temperature (RAA788170, RAA788172)

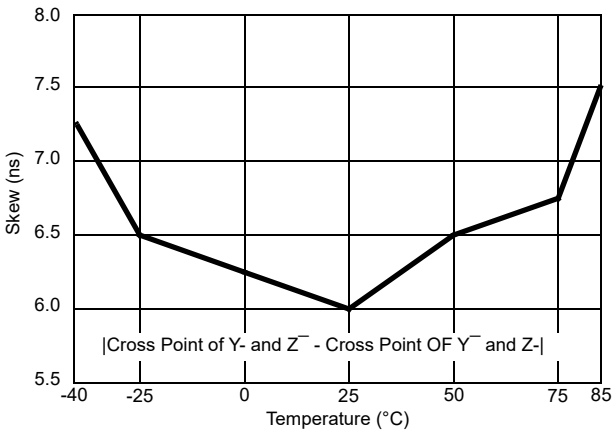


Figure 20. Driver Differential Skew vs Temperature (RAA788170, RAA788172)

V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified (Cont.)

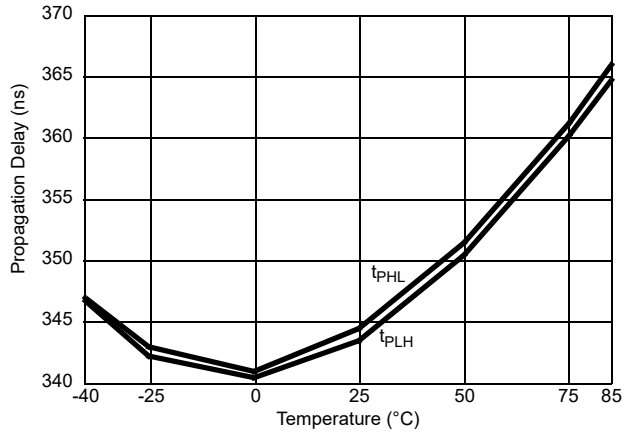


Figure 21. Driver Differential Propagation Delay vs Temperature (RAA788173, RAA788175)

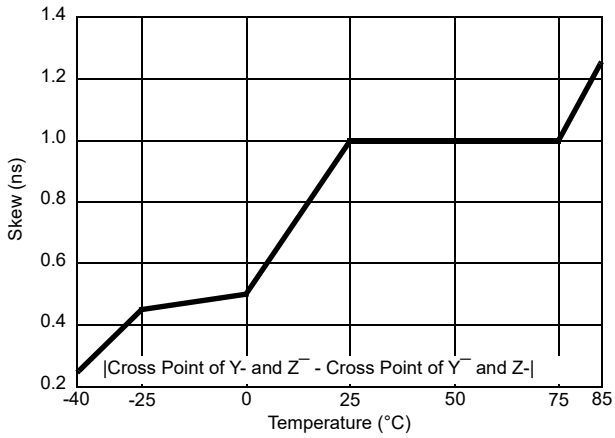


Figure 22. Driver Differential Skew vs Temperature (RAA788173, RAA788175)

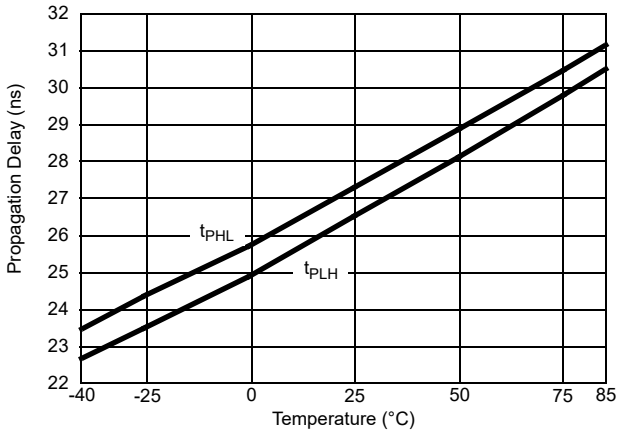


Figure 23. Driver Differential Propagation Delay vs Temperature (RAA788176, RAA788178)

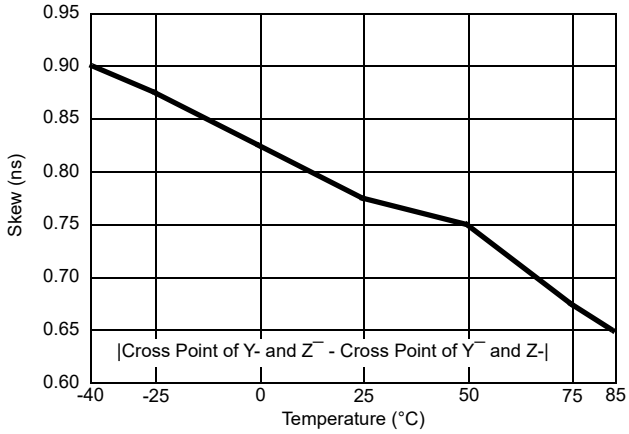


Figure 24. Driver Differential Skew vs Temperature (RAA788176, RAA788178)

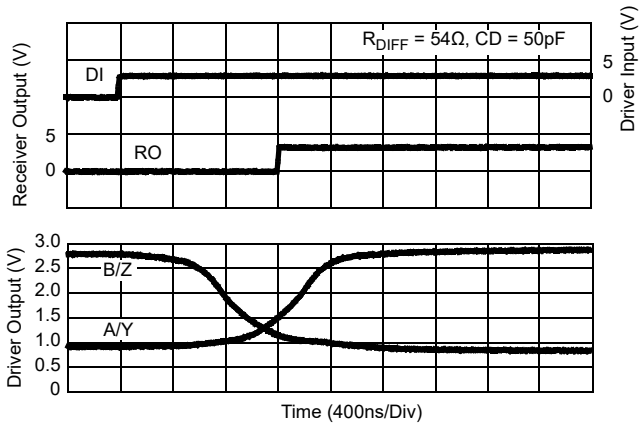


Figure 25. Driver and Receiver Waveforms, Low to High (RAA788170, RAA788172)

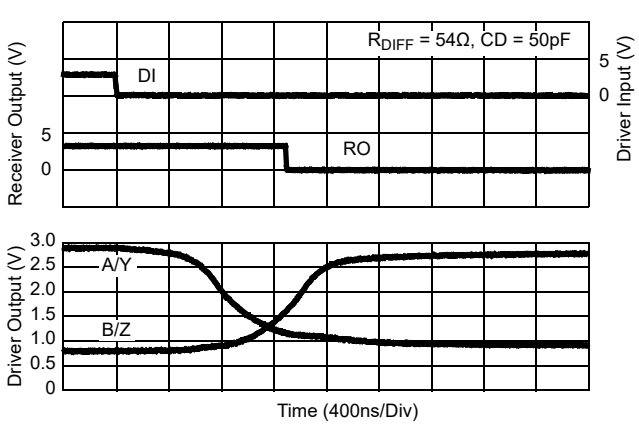


Figure 26. Driver and Receiver Waveforms, High to Low (RAA788170, RAA788172)

V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified (Cont.)

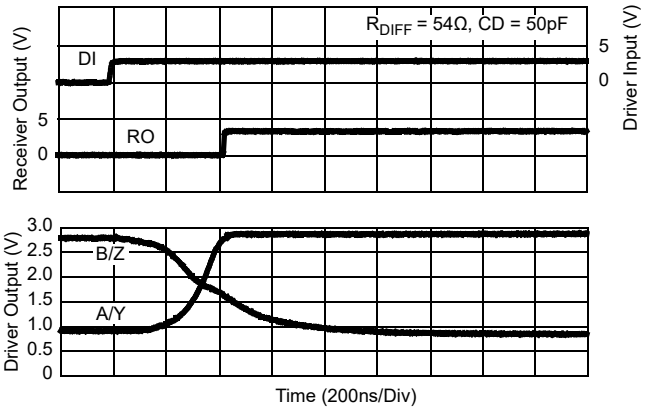


Figure 27. Driver and Receiver Waveforms, Low to High (RAA788173, RAA788175)

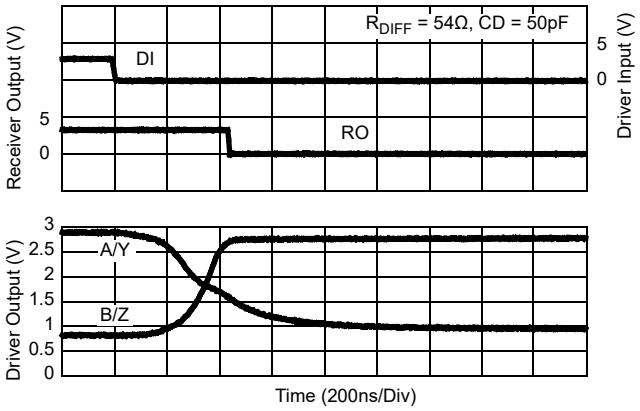


Figure 28. Driver and Receiver Waveforms, High to Low (RAA788173, RAA788175)

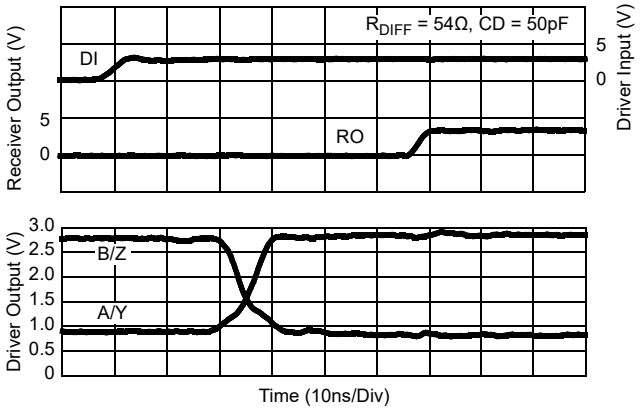


Figure 29. Driver and Receiver Waveforms, Low to High (RAA788176, RAA788178)

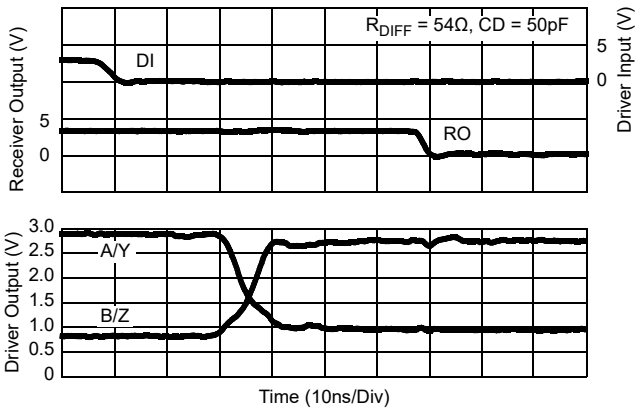


Figure 30. Driver and Receiver Waveforms, High to Low (RAA788176, RAA788178)

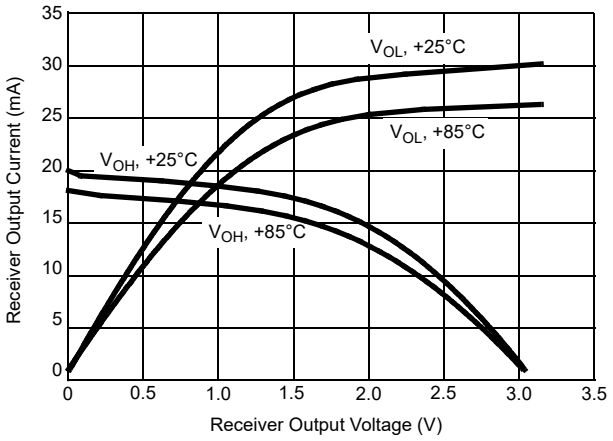


Figure 31. Receiver Output Current vs Receiver Output Voltage

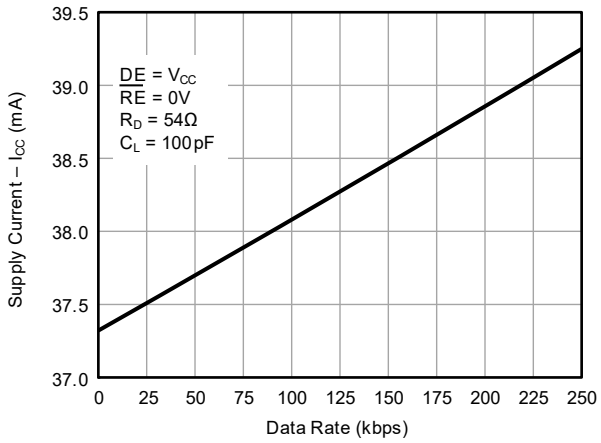


Figure 32. Supply Current vs Data Rate (RAA788170, RAA788172)

V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified (Cont.)

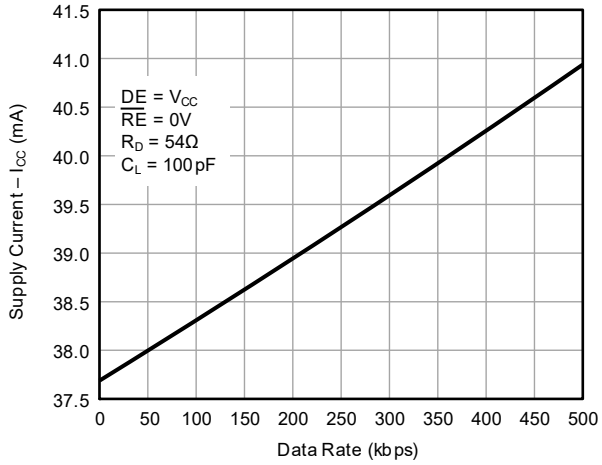


Figure 33. Supply Current vs Data Rate (RAA788173, RAA788175)

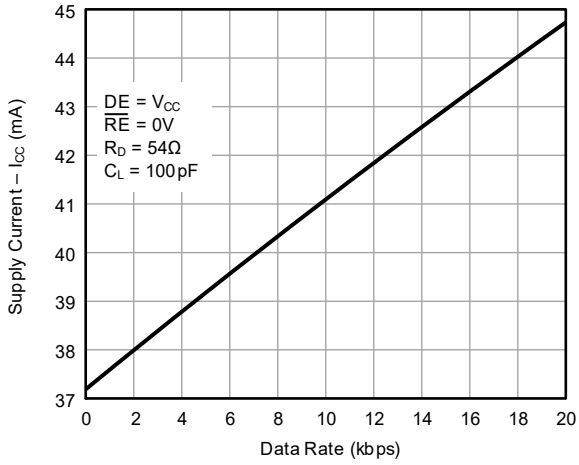


Figure 34. Supply Current vs Data Rate (RAA788176, RAA788178)

6. Die Characteristics

Characteristic	Value
Substrate Potential (Powered Up)	GND
Transistor Count	535
Process	Si Gate BiCMOS

7. Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard, allowing up to 32 one-unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common-mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

7.1 Receiver Features

These devices use a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ and is eight times the RS-485 Unit Load (UL) requirement of 12kΩ minimum. Therefore, these products are known as 1/8 UL transceivers and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (that is, +12V and -7V), making them ideal for long networks where induced voltages and ground potential differences are realistic concerns.

All the receivers include a Full Fail-Safe function that ensures a high-level receiver output if the receiver inputs are unconnected (floating) or shorted. Fail-safe with shorted inputs is achieved by setting the Rx upper switching point to -50mV, thereby ensuring that the Rx sees 0V differential as a high input level.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs are tri-statable using the active low $\overline{RE}$ input.

7.2 Driver Features

The RS-485/422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485) and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width and to minimize EMI.

All drivers are tri-statable through the active high DE input.

The 250kbps and 500kbps driver outputs are slew rate limited to minimize EMI and to reduce reflections in unterminated or improperly terminated networks. Outputs of the RAA788176 through RAA788178 drivers are not limited, so faster output transition times allow data rates of at least 20Mbps.

7.3 Hot Plug Function

When a piece of equipment powers up, a period of time occurs in which the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the RAA78817x versions with output enable pins incorporate a Hot Plug function. During power-up, circuitry monitoring V_{CC} ensures that the Tx and Rx outputs remain disabled for a period of time, regardless of the state of DE and $\overline{RE}$. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

7.4 High EFT Immunity

The bus pins of the RAA78817x transceivers withstand ±3kV Electrical Fast Transient (EFT) immunity per IEC61000-4-4. During the EFT test, the EFT generator produces a burst of 75 fast transients that are capacitively coupled onto RS-485 data lines using a capacitive clamp.

A burst period is 300ms and includes 75 EFT pulses followed by a break interval. Over a test time of 60 seconds minimum, multiple bursts are applied at a predefined repetition frequency of either 5kHz or 100kHz. Therefore, a minimum of 15000 EFT pulses is unleashed onto the data link.

The RAA78817x transceivers have been tested with both repetition frequencies, 5kHz and 100kHz. In the test setup, a complete RS-485 data link (driver, receiver, and unshielded twisted pair cable) has been tested during data transmission. Afterwards, the devices were tested on an automatic test system (ATE) for parametric performance. The ATE pass criterion requires that a device shows no parametric shift at all.

All RAA78817x transceivers passed the EFT tests with ±3kV test voltage, which places this transceiver family into the highest special test level category (test level X) of the IEC61000-4-4 standard.

7.5 ESD Protection

All pins on these devices include Class 3 (>7kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM and ±15kV IEC61000. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (for example, transient suppression diodes), and the associated, undesirable capacitive load they present.

7.6 IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into the RS-485 pins allows the design of equipment meeting Level 4 criteria without the need for additional board-level protection on the RS-485 port.

7.6.1 Air-Gap Discharge Test Method

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on variables such as approach speed, humidity, and temperature, so it is difficult to obtain repeatable results. The RAA78817x RS-485 pins withstand ±15kV air-gap discharges.

7.6.2 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. The RAA78817x survive ±8kV contact discharges on the RS-485 pins.

7.7 Data Rate, Cables, and Terminations

RS-485/422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 20Mbps are limited to lengths less than 100ft, while the 250kbps versions can operate at full data rates with lengths of several thousand feet.

Twisted pair is the cable of choice for RS-485/422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative when using the 20Mbps devices to minimize reflections. Short networks using the 250kbps versions do not need to be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

7.8 Built-In Driver Overload Protection

As stated previously, the RS-485 spec requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement using driver output short-circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry, which ensures that the output current never exceeds the RS-485 specification, even at the common-mode voltage range extremes. Additionally, these devices use a foldback circuit that reduces the short-circuit current, and therefore the power dissipation, whenever the contending voltage exceeds either supply.

If a major short-circuit condition occurs, devices use a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about 15°. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

7.9 Low Power Shutdown Mode

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but some also include a shutdown feature that reduces the already low quiescent I_{CC} to a 10nA trickle. These devices enter shutdown whenever the receiver and driver are simultaneously disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 50ns ensures that the transceiver does not enter shutdown.

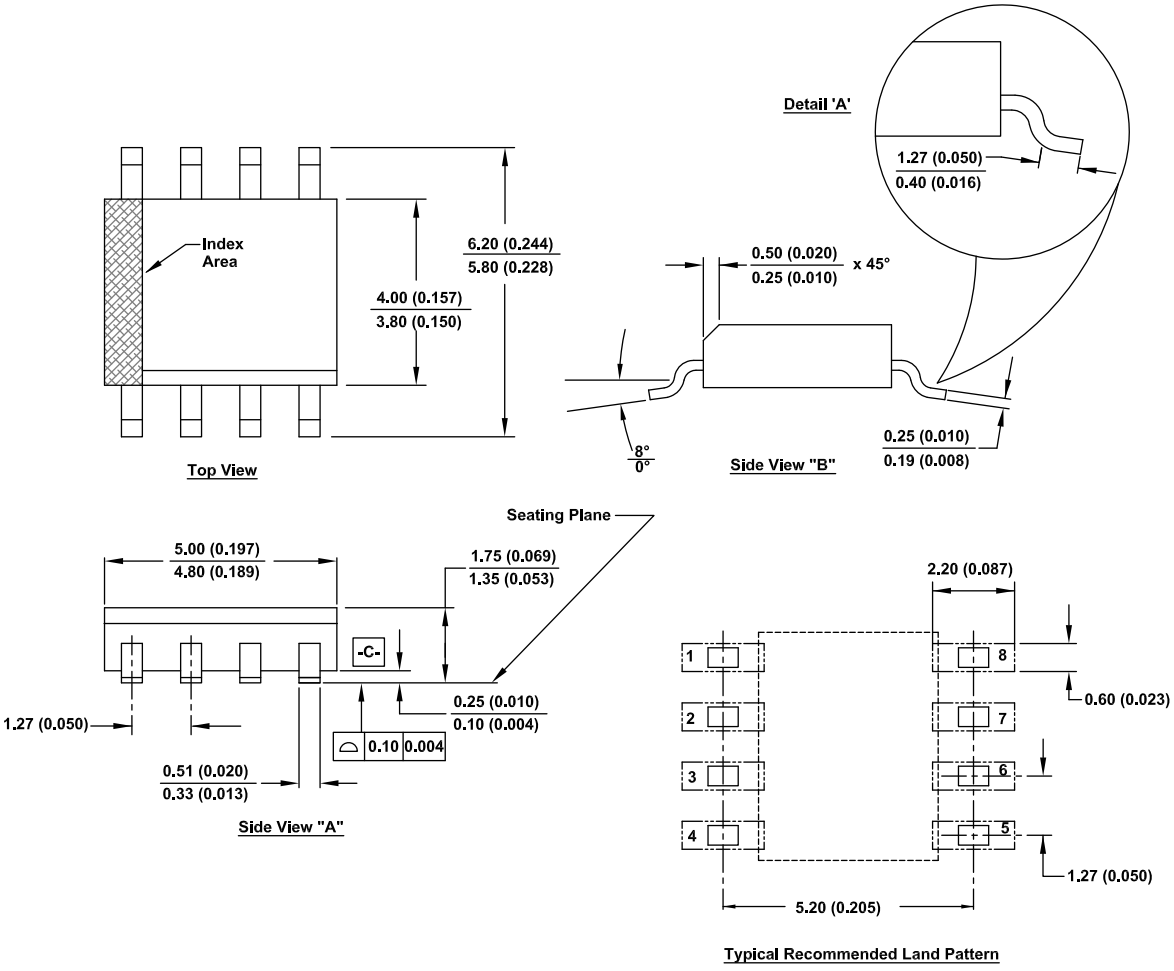
Note: Receiver and driver enable times increase when the transceiver enables from shutdown. See the notes at the end of the Electrical Specifications table for more information.

8. Package Outline Drawings

For the most recent package outline drawing, see M8.15.

M8.15

8 Lead Narrow Body Small Outline Plastic Package
Rev 7, 9/2023

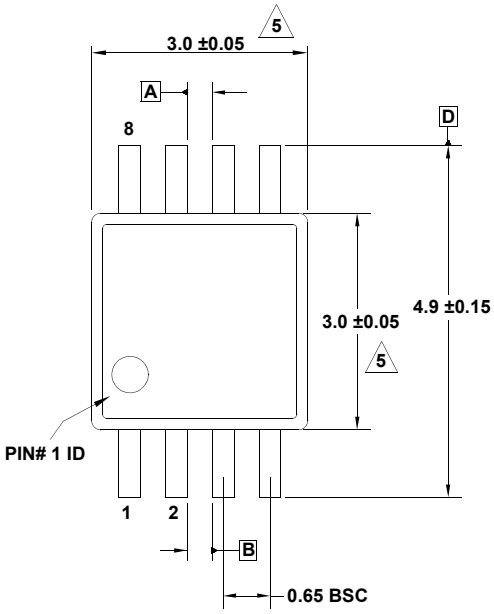


Notes:

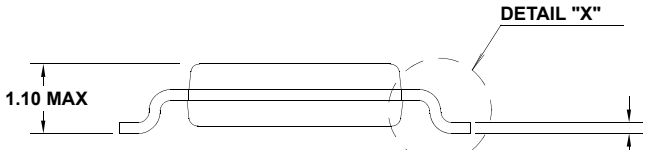
1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not Include mold flash, protruslon or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

For the most recent package outline drawing, see M8.118.

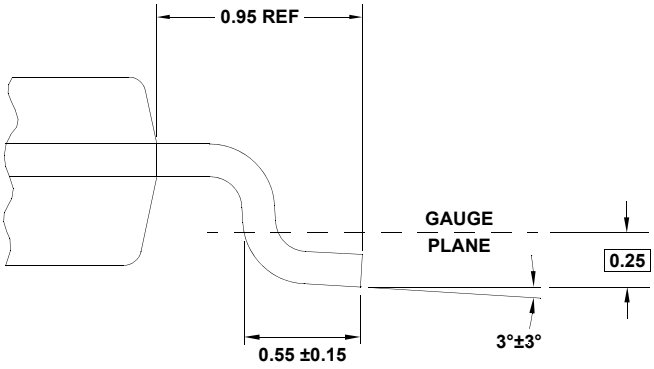
M8.118
8 Lead Mini Small Outline Plastic Package
Rev 5, 5/2021



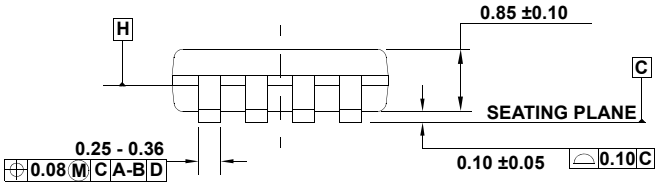
TOP VIEW



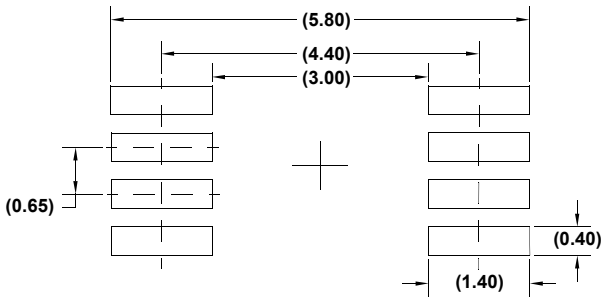
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



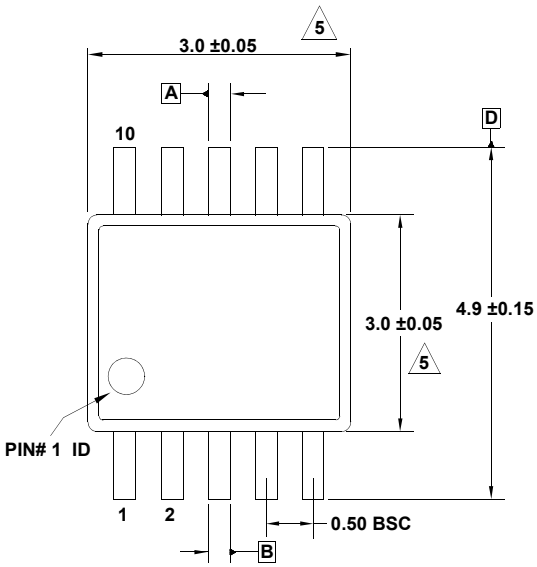
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

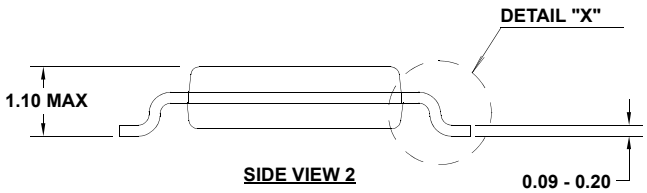
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

For the most recent package outline drawing, see M10.118.

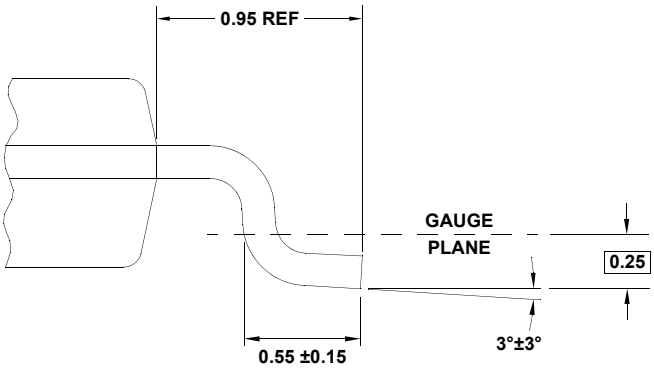
M10.118
10 Lead Mini Small Outline Plastic Package
Rev 2, 5/2021



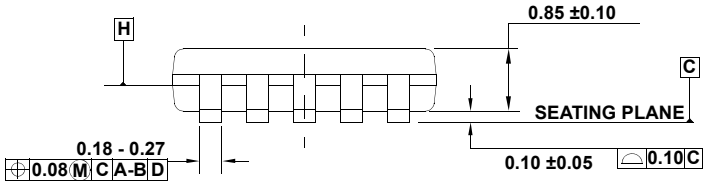
TOP VIEW



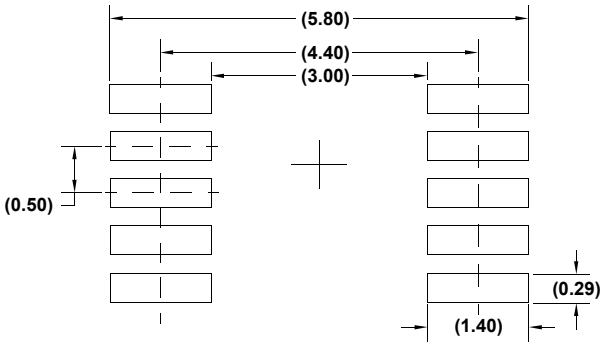
SIDE VIEW 2



DETAIL "X"



SIDE VIEW 1



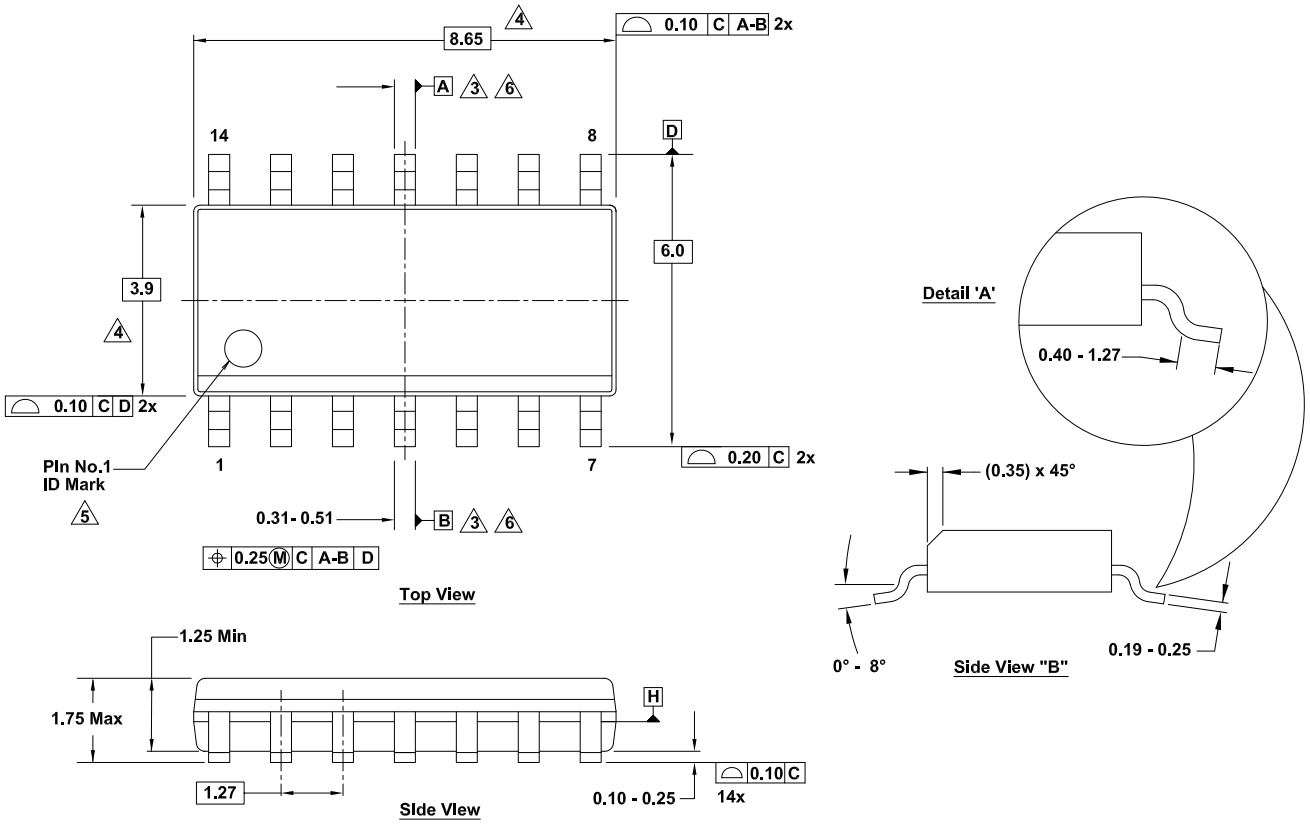
TYPICAL RECOMMENDED LAND PATTERN

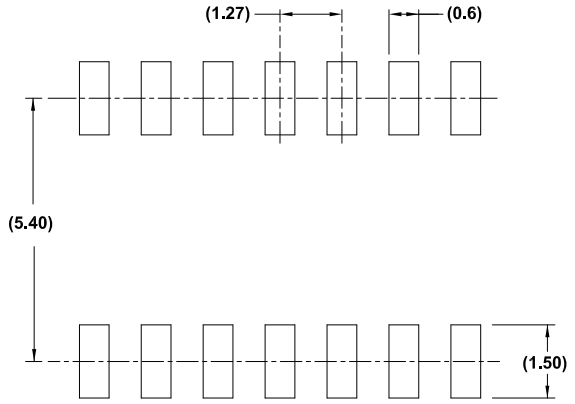
NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

For the most recent package outline drawing, see M14.15.

M14.15
14 Lead Narrow Body Small Outline Plastic Package
Rev 2, 6/20





Typical Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Datums A and B are determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier can be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
RAA7881702GSP#AB0	RAA788 1702GSP	14 Ld SOIC	M14.15	Tube	-40 to +85
RAA7881702GSP#HB0				Reel, 2.5k	
RAA7881702GSU#AB0	81702	10 Ld MSOP	M10.118	Tube	
RAA7881702GSU#HB0				Reel, 2.5k	
RAA7881722GSP#AB0	7881722	8 Ld SOIC	M8.15	Tube	
RAA7881722GSP#HB0				Reel, 2.5k	
RAA7881722GSU#AB0	81722	8 Ld MSOP	M8.118	Tube	
RAA7881722GSU#HB0				Reel, 2.5k	
RAA7881732GSP#AB0	RAA788 1732GSP	14 Ld SOIC	M14.15	Tube	
RAA7881732GSP#HB0				Reel, 2.5k	
RAA7881732GSU#AB0	81732	10 Ld MSOP	M10.118	Tube	
RAA7881732GSU#HB0				Reel, 2.5k	
RAA7881752GSP#AB0	7881752	8 Ld SOIC	M8.15	Tube	
RAA7881752GSP#HB0				Reel, 2.5k	
RAA7881752GSU#AB0	81752	8 Ld MSOP	M8.118	Tube	
RAA7881752GSU#HB0				Reel, 2.5k	
RAA7881762GSP#AB0	RAA788 1762GSP	14 Ld SOIC	M14.15	Tube	
RAA7881762GSP#HB0				Reel, 2.5k	
RAA7881762GSU#AB0	81762	10 Ld MSOP	M10.118	Tube	
RAA7881762GSU#HB0				Reel, 2.5k	
RAA7881782GSP#AB0	7881782	8 Ld SOIC	M8.15	Tube	
RAA7881782GSP#HB0				Reel, 2.5k	
RAA7881782GSU#AB0	81782	8 Ld MSOP	M8.118	Tube	
RAA7881782GSU#HB0				Reel, 2.5k	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the product information page for the RAA788170, RAA788172, RAA788173, RAA788175, RAA788176, RAA788178. For more information on MSL refer to TB363.
3. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.01	Oct 2, 2023	Updated M8.15 POD to the latest revision (corrected typo).
1.00	Aug 24, 2022	Initial release.

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