1. INTRODUCTION

1.1 Features

- **Fully integrated battery management solution with battery capacity measurement and programmable protection capability.**
- **Supports up to 7 Li-ion or Li-Polymer battery cells in series.**
- **Integrated with Renesas Ultra Low Power RL78 CPU core for multi-function process**
- **Memory**
  - Code flash memory: 128 kB
  - Data flash memory (up to 100,000 erase/write cycles): 4 kB
  - SRAM: 7kB
- **Clock generator**
  - High speed on-chip oscillator: up to 32 MHz
  - Low speed on-chip oscillator: 15 kHz
  - AFE high speed on-chip oscillator: 4.194 MHz
  - AFE low speed on-chip oscillator: 131.072 kHz
- **General Purpose I/O Ports**
  - Total: 19 pins
  - CMOS input/output: 12
  - CMOS input: 2
  - N-ch open drain Input/output [6 V tolerance]: 3
  - High voltage input/output [VCC tolerance]: 2
- **Serial interface**
  - CSI (SPI): 2 channels
  - I2C: 1 channel
  - UART: 2 channels
  - Simplified I2C: 2 channels
- **Timer**
  - MCU 16-bit timer: 6 channels
  - MCU 12-bit interval timer: 1 channel
  - MCU Real time clock: 1 channel
  - AFE timer: 2 channels
    - AFE timer A: setting range: 125 ms to 64 s
    - AFE timer B: setting range: 30.52 us to 125 ms
- **Embedded A/D converter**
  - AFE 15-bit resolution sigma-delta A/D converter
  - MCU 8/10-bit resolution A/D converter
- **Battery cell voltage and temperature (AN port voltage) detection circuit**
  - Monitoring over/under voltage and temperature by Sigma-delta AD converter (AFE) without controlling from MCU
- **Current integration circuit**
  - 18-bit resolution sigma-delta A/D converter
- **Impedance measurement circuit**
  - Simultaneous measurement of battery voltage and current
- **Over current detection circuit**
  - Short circuit current detection
  - Charge overcurrent detection
  - Discharge overcurrent detection
  - Charge wakeup current detection
  - Discharge wakeup current detection
- **Series regulator**
  - 3.3 V or 5.0 V CREG2
- **Charge and Discharge MOSFET control**
  - High side Nch MOSFET drive circuit embedded
  - Programmable MOSFET control by 8-bit PWM
- **Voltage and temperature condition**
  - Power supply voltage: VCC = 4.0 to 50 V
  - Operating ambient temperature
    - T_A=-20 to 85C (REG2T6 bit = 0)
    - T_A=-40 to 85C (REG2T6 bit = 1)

    Operating ambient temperature is configurable by REG2T6 bit of REG2T register setting.
- **Package Information**
  - 48 pin plastic mold QFN
    ([Body] 6.0 mm x 6.0 mm, 0.4 mm pitch)

1.2 Applications

- E-Bike, E-Scooter, Pedal-Assist Bicycle
- Power Tool, Vacuum Cleaner, Drone
- Battery Backup System, Energy Storage System (ESS)

1.3 Description

RAJ240091 is Renesas Li-ion battery fuel gauge IC (FGIC) which consist of a MCU device and an AFE device in a single package. Pack with a variety of battery management features and Renesas RL78 CPU core which has multiple low power modes and capable of achieving high performance in ultra-low power operation. RAJ240091 fuel gauge IC has control firmware stored in embedded flash memory to control attached embedded analog and digital circuits to execute battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

Table of Contents

2. OUTLINE

2.1 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0 (PIOR0) is set to "02H".

(1/2)

Item		Description
Code flash memory		128 kB
Data Flash memory		4 kB
RAM		7 kB
Address size		1MB
Main system clock	High speed on-chip Oscillator clock(fIH)	HS (high-speed main) mode: 1 to 32 MHz LS (low-speed main) mode: 1 to 8 MHz ,
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.03125 us(Internal high speed oscillation clock: fIH = 32 MHz) 30.5 us (Subsystem clock : f_{SUB} = 32.768 kHz operation)
Instruction set		• Data transmission (8/16 bits) • Addition and subtraction/logical operations (8/16 bits) • Multiplication (8×8 bits,16×16 bits),Division (16÷16 bits,32÷32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.
I/O Port	CMOS I/O	12
	CMOS input	2
	N-ch open-drain I/O [6 V tolerance)	3
	High voltage I/O	2
Timer	16-bit timer	6 channels (TAU : 4 channels, Timer RD : 2 channels)
	Watchdog timer	1 channel
	Real time clock	1 channel
	12-bit interval timer	1 channel
	Timer output	PWM outputs: 3 channels
	RTC output	1 channel
8/10-bit resolution A/D converter		3 channels
Serial interface		• CSI: 2 channel/UART: 2 channels/simplified I2C: 2 channels
	I^2C bus	1 channel
Vector interrupt source	Internal	22
	External	11 (6 sources is connected to AFE in the chip)
Reset		・Reset by RESET pin (reset circuit output of AFE connected to RESETOUT) ・Internal reset by watchdog timer ・Internal reset by illegal instruction execution Note ・internal reset by RAM parity error ・internal reset by illegal memory access
On-chip debug function		Support

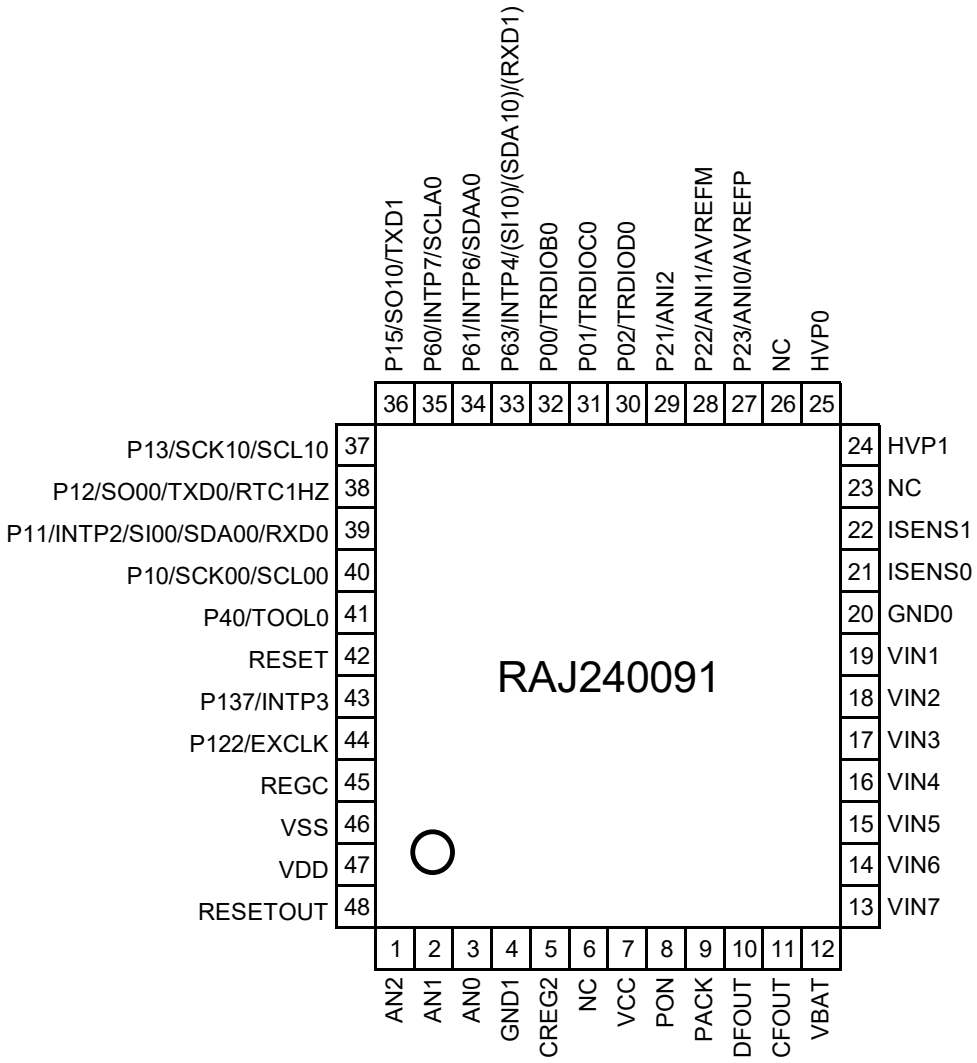
Note The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

Item	Description
PWM	8 bits or 10 bits ×1 for FET control
Sigma-delta A/D converter	15-bit resolution (sigma-delta method) • Battery Cell voltage (Cell 1 to 7) • Battery Cell total voltage (VIN7 pin) • Charge voltage (PACK pin) • PON pin input voltage • Thermistor sensor port with on-chip pull-up 10kohm resistor: 3 channels • On-chip simple temperature sensor (temperature range: -40 to 85°C) • Internal reference and supply voltage (MCU and AFE)
Battery cell voltage and temperature (AN port voltage) detection circuit	Battery Cell voltage detection • Over voltage (Overcharge voltage) • Under voltage (Overdischarge voltage) Temperature (AN port voltage) detection • Over temperature • Under temperature
Current integrating circuit	1 channel:18-bit resolution
Current integrating circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wake up current detection circuit	• Discharge short-circuit current detection • Discharge overcurrent detection • Charge overcurrent detection, • Wake up current detection (discharge and charge)
Simple temperature sensor	1 channel
Charge/Discharge FET control circuit	NchFET driver for charge control NchFET driver for discharge control
Power on reset circuit	Return from power down mode by detecting voltage and connecting charger
Series regulator	VREG2：power supply for MCU (3.3 V or 5.0 V)
Reset circuit	Series regulator output monitoring (VREG2)
Cell balancing circuit	7 series cells support (On-resistor: 200ohm TYP)
MCU runaway detection circuit	20 bits×1(2 / 4 / 8 / 16 / 32 / 64 [s] to be selected)
AFE On-chip oscillator	4.194 MHz (TYP)
AFE low speed On-chip oscillator	131.972 kHz (TYP)
AFE timer	2 channels • AFE timer A (setting range：125 ms to 64 s) • AFE timer B (setting range：30.52 us to 125 ms)
MCU-AFE communication interface(C2C)	AFE ~ MCU communication (Chip to Chip Interface)
Power supply voltage	VCC = 4.0 to 50 V
Operation ambient temperature	-20 to 85°C (REG2T6 bit (bit6 of REG2T)= 0) -40 to 85°C (REG2T6 bit (bit6 of REG2T)= 1)
Package	48 pin plastic mold QFN ([Body] 6.0mm x 6.0mm, 0.4 mm pitch, 0.85 mm thickness)

2.2 Pin Configuration

・48 pin plastic mold QFN ([Body] 6.0mm x 6.0mm, 0.4 mm pitch)



Caution 1. REGC pin connects to VSS pin through a capacitor (0.47 to 1.0 uF)

Caution 2. CREG2 pin connects to GND0/GND1 pin through a capacitor (1.0 to 4.7 uF).

Remark 1. Pin name refer to [Section 3.1 pin identification].

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

3. PIN FUNCTIONS

3.1 Pin identification

(1/2)

No.	Name	Type	Description
1	AN2	AIN	Analog Input
2	AN1	AIN	Analog Input
3	AN0	AIN	Analog Input
4	GND1	P	Ground
5	CREG2	P	Regulator Output
6	NC	NC	No connect
7	VCC	P	Power supply
8	PON	HVIN	High voltage Port for power on
9	PACK	HVIN	Charger voltage input
10	DFOUT	HVO	Discharge MOSFET control
11	CFOUT	HVO	Charge MOSFET control
12	VBAT	AIN	Battery voltage input
13	VIN7	AIN	Battery voltage input
14	VIN6	AIN	Battery voltage input
15	VIN5	AIN	Battery voltage input
16	VIN4	AIN	Battery voltage input
17	VIN3	AIN	Battery voltage input
18	VIN2	AIN	Battery voltage input
19	VIN1	AIN	Battery voltage input
20	GND0	P	Ground
21	ISENS0	AIN	Analog input for current integration circuit
22	ISENS1	AIN	Analog input for current integration circuit
23	NC	NC	No connect
24	HVP1	HVIO	High Voltage Port

(2/2)

No.	Name	Type	Description
25	HVP0	HVIO	High Voltage Port
26	NC	NC	No connect
27	P23 / ANI0 / AVREFP	DIO/AIN	Port2 / Analog Input / Analog Reference Voltage Plus
28	P22 / ANI1 / AVREFM	DIO/AIN	Port2 / Analog Input / Analog Reference Voltage Minus
29	P21 / ANI2	DIO/AIN	Port2 / Analog Input
30	P02 / TRDIOD0	DIO	Port0 / Timer Output
31	P01 / TRDIOC0	DIO	Port0 / Timer Output
32	P00 / TRDIOB0	DIO	Port0 / Timer Output
33	P63 / INTP4 / (SI10) / (SDA10) / (RXD1)	DIO	Port6 / External Interrupt Input / Serial Data Input / Serial Data Input/Output / Receive Data
34	P61 / INTP6 / SDAA0	DIO	Port6 / External Interrupt Input / I2C Bus data I/O
35	P60 / INTP7 / SCLA0	DIO	Port6 / External Interrupt Input / I2C Bus clock I/O
36	P15 / SO10 / TXD1	DIO	Port1 / Serial Data Output / Transmit Data
37	P13 / SCK10 / SCL10	DIO	Port1 / Serial Clock Input/Output
38	P12 / SO00 / TXD0 / RTC1HZ	DIO	Port1 / Serial Data Output / Transmit Data / Real-time Clock Correction Clock (1 Hz) Output
39	P11 / INTP2 / SI00 / SDA00 / RXD0	DIO	Port1 / External Interrupt Input / Serial Data Input / Serial Data Input/Output / Receive Data
40	P10 / SCK00 / SCL00	DIO	Port1 / Serial Clock Input/Output
41	P40 / TOOL0	DIO	Port4 / Data Input/Output for Tool
42	RESET	DIN	Reset Input for MCU
43	P137 / INTP3	DI	Port13 / External Interrupt Input
44	P122 / EXCLK	DI	Port12 / External Clock Input
45	REGC	P	Regulator Capacitance
46	VSS	P	Ground
47	VDD	P	Power Supply
48	RESETOUT	AO	Reset Output

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

HVO: high voltage output
HVIN: high voltage input
HVIO: high voltage input/output
P: power
DIO: digital I/O
DIN: digital input
AIN: analog input
AO: analog output

3.2 Pin Functions

3.2.1 Pin type and alternate functions

Function name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P00	7-1-7	I/O	Input port	TRDIOB0	Port 0. 8-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P03 and P04 can be set to TTL input buffer. Output of P03 and P04 can be set to N-ch open-drain output (VDD tolerance).
P01	7-1-7			TRDIOC0	
P02	7-1-7			TRDIOD0	
P03 Note 3	8-1-4			-	
P04 Note 3	8-1-4			-	
P05 Note 3	7-1-3			-	
P06 Note 3	7-1-3			-	
P07 Note 3	7-1-3			-	
P10	8-1-4	I/O	Input port	SCK00/SCL00	Port 1. 7-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 to P14 can be set to TTL input buffer. Output of P10 to P16 can be set to N-ch open-drain output (VDD tolerance).
P11	8-1-4			INTP2/SI00/SDA00/RXD0	
P12	7-1-4			SO00/TXD0/RTC1HZ	
P13	8-1-4			SCK10/SCL10	
P14 Note 3	8-1-4			-	
P15	7-1-4			SO10/TXD10	
P16 Note 3	7-1-4			-	
P20 Note 3	4-3-3	I/O	Analog function	-	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit unit. Can be set to analog input Note 1.
P21	4-3-3			ANI2	
P22	4-3-3			ANI1/AVREFM	
P23	4-3-3			ANI0/AVREFP	
P30 Note 2	7-1-3	I/O	Input port	INTP13	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P31 Note 2	7-1-3			INTP12	
P32 Note 2	7-1-3			INTP11	
P33 Note 2	7-1-3			INTP10	
P40	7-1-3	I/O	Input port	TOOL0	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P60	12-1-2	I/O	Input port	INTP7/SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit unit. Output of P60 to P63 can be set to N-ch open-drain output (6.0 V tolerance).
P61	12-1-2			INTP6/SDAA0	
P62 Note 3	12-1-2			-	
P63	12-1-2			INTP4/(SI10)/(SDA10)/(RXD1)	
P70 Note 2	7-1-3	I/O	Input port	INTP9	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71 Note 2	7-1-3			INTP8	
P72 Note 2	7-1-3			EXBSEL	
P73 Note 2	7-1-3			EXBCK	
P74 Note 2	7-1-3			EXBO0/EXBI0	
P75 Note 2	7-1-3			EXBO1/EXBI1	
P76 Note 2	7-1-3			EXBO2/EXBI2	
P77 Note 2	7-1-3			EXBO3/EXBI3	
P122	2-2-2	input	Input port	EXCLK	Port 12. 3-bit input-only port.
P123 Note 4	2-2-1			-	
P124 Note 4	2-2-1			-	
P137	2-1-2	input	Input port	INTP3	Port 13. 1-bit input-only port.
RESET	2-1-1	input	-	-	Input-only pin for external reset. Connect to VDD directly or via a resistor when external reset is not used.

Note 1. Each pin can be configured as digital or analog pin by setting the port mode in the control register x (PMCx) (Can be specified in 1-bit units).

Note 2. Connected to internal AFE circuit.

Note 3. This pin is not connected anywhere. To fix pin level, be sure to set the port mode to output mode.

Note 4. This pin is fixed level in package.

3.2.2 External Pin Functions

(1/2)

Category	Pin name	I/O	Function
Power supply	VCC	—	Power supply input. Apply power supply voltage to VCC pin from a charger or battery.
	GND0, GND1	—	Device ground input. Connect the negative input terminal of lithium-ion battery 1 to the GND0 and GND1 pins
	CREG2	—	Series regulator output port. Connect to GND0 and GND1 via a capacitor (1 uF to 4.7 uF)
	VDD	—	Positive power supply for MCU Connect to CREG2
	VSS	—	Ground input for MCU Connect the negative input terminal of lithium-ion battery 1 to the GND0 and GND1 pins
	REGC Note 1.	—	Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to VSS via a capacitor (0.47 to 1.0 uF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
RESET	RESET	Input	This is the active-low system reset input pin for MCU.
	RESETOUT	output	This is the active-low system reset output pin for AFE.
TOOL0	TOOL0 Note 2	input	Data I/O for flash memory programmer/debugger. Connect to the VDD via an external pull-up resistor in the on chip debug mode
Serial interface (UART0, UART1)	RxD0, RxD1	input	Serial data input pins of serial interface UART0 to UART1
	TxD0, TxD1	output	Serial data output pins of serial interface UART0 to UART1
Serial interface (CSI00, CSI10)	SCK00, SCK10	I/O	Serial clock I/O pins of serial interface CSI00 and CSI10
	SI00, SI10	input	Serial data input pins of serial interface CSI00 and CSI10
	SO00, SO10	output	Serial data output pins of serial interface CSI00 and CSI10
Serial interface (IIC00, IIC10)	SCL00, SCL10	output	Serial clock output pins of serial interface IIC00 and IIC10
	SDA00, SDA10	I/O	Serial data I/O pins of serial interface IIC00 and IIC10
Serial interface (IICA0)	SCLA0	I/O	Serial clock I/O pins of serial interface IICA0
	SDAA0	I/O	Serial data I/O pins of serial interface IICA0,
A/D converter	AN0, AN1, AN2	input	AFE A/D converter analog input
	ANI0, ANI1, ANI2	input	MCU A/D converter analog input
	AVREFP	input	A/D converter reference voltage (+ side).
	AVREFM	input	A/D converter reference voltage (- side).
Current integration circuit and overcurrent detection circuit	ISENS0, ISENS1	input	Analog input for current integration circuit and over current detection circuit
Timer	TRDIOB0 TRDIOC0 TRDIOD0	I/O	Timer RD input/output
	RTC1HZ	output	Real-time clock supports clock (1 Hz) output

(2/2)

Category	Pin name	I/O	Function
High voltage I/O port	HVP0, HVP1	I/O	High voltage I/O in correspondence with VCC tolerance
External clock	EXCLK	Input	External clock input for main system clock
External interrupt input	INTP0 to INTP13	input	Interrupt request input pin. INTP8 to INTP13 connects interrupt request signal of AFE in the package and do not connect to any pin
Power on circuit	PON	input	Power on input for release from power down state
Charger connection detect	PACK	Input	Charger voltage input and source voltage of discharge FET drive port (DFOUT)
Battery connection detect	VBAT	input	Sense voltage input pin for most positive cell and source voltage for charge FET drive port (CFOUT)
Battery voltage detection circuit	VIN7	Input	The positive input terminal of lithium-ion battery 7
	VIN6	Input	The negative input terminal of lithium-ion battery 7 and the positive input terminal of lithium-ion battery 6
	VIN5	Input	The negative input terminal of lithium-ion battery 6 and the positive input terminal of lithium-ion battery 5
	VIN4	Input	The negative input terminal of lithium-ion battery 5 and the positive input terminal of lithium-ion battery 4
	VIN3	Input	The negative input terminal of lithium-ion battery 4 and the positive input terminal of lithium-ion battery 3
	VIN2	Input	The negative input terminal of lithium-ion battery 3 and the positive input terminal of lithium-ion battery 2
	VIN1	Input	The negative input terminal of lithium-ion battery 2 and the positive input terminal of lithium-ion battery 1
FET control output	DFOUT	Output	ON/OFF signal output pin for discharge FET.
	CFOUT	Output	ON/OFF signal output pin for charge FET.
Communication between AFE and MCU	P72	input	Control signal of communication between AFE and MCU with setting to output port. P72 is connected to AFE in a package and not external pin.
	EXBCK	Output	Clock signal of communication between AFE and MCU
	EXBD0-3	I/O	Data signal of communication between AFE and MCU

Note 1. REGC is not external power supply pin. (Do not draw current from REGC.)

Note 2. After reset release, the connection between P40/TOOL0 and the operating mode are as follows.

Table 3-1 TOOL0 Pin Operation Mode after Reset Release

P40/TOOL0	Operation Mode
VDD	Normal operation mode
0 V	Flash memory programming mode

3.3 Pin Block Diagram

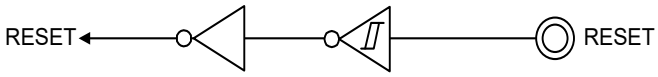
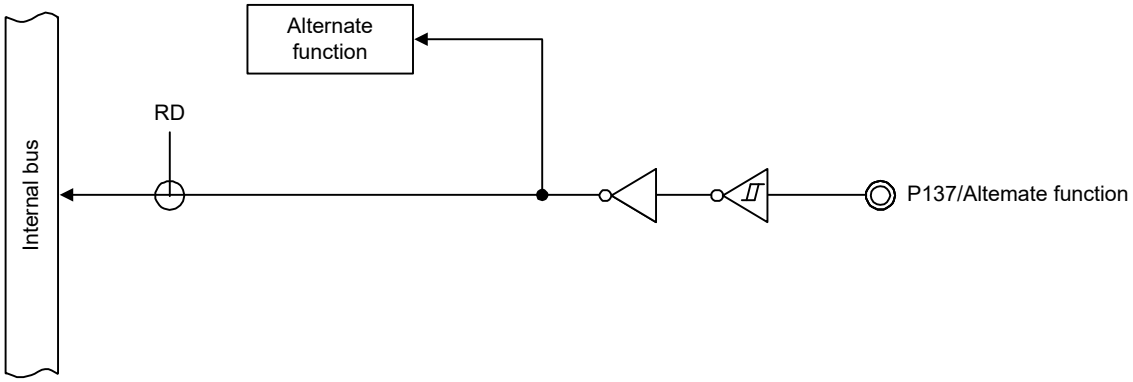
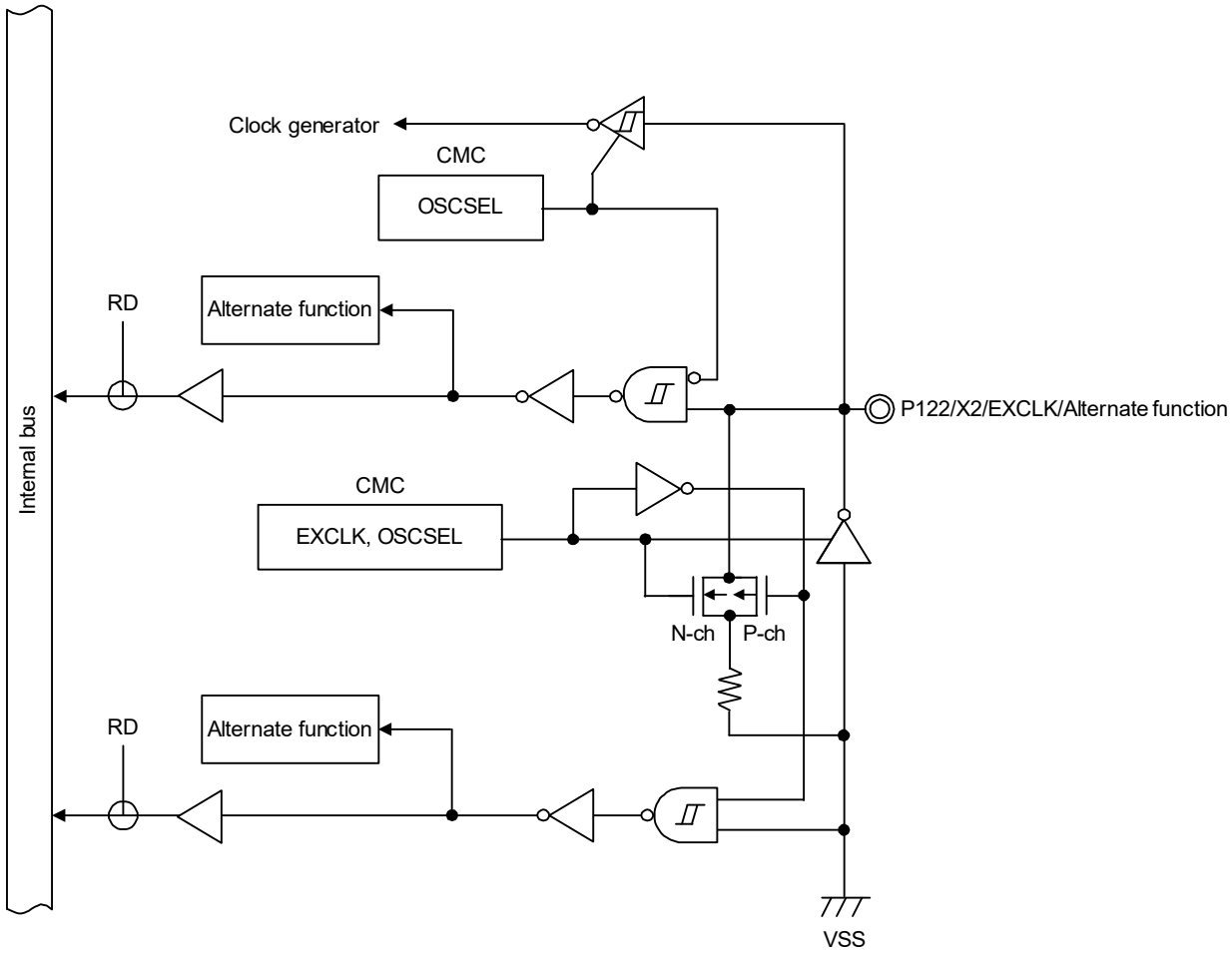


Figure 3-1 Pin Block Diagram for Pin type 2-1-1



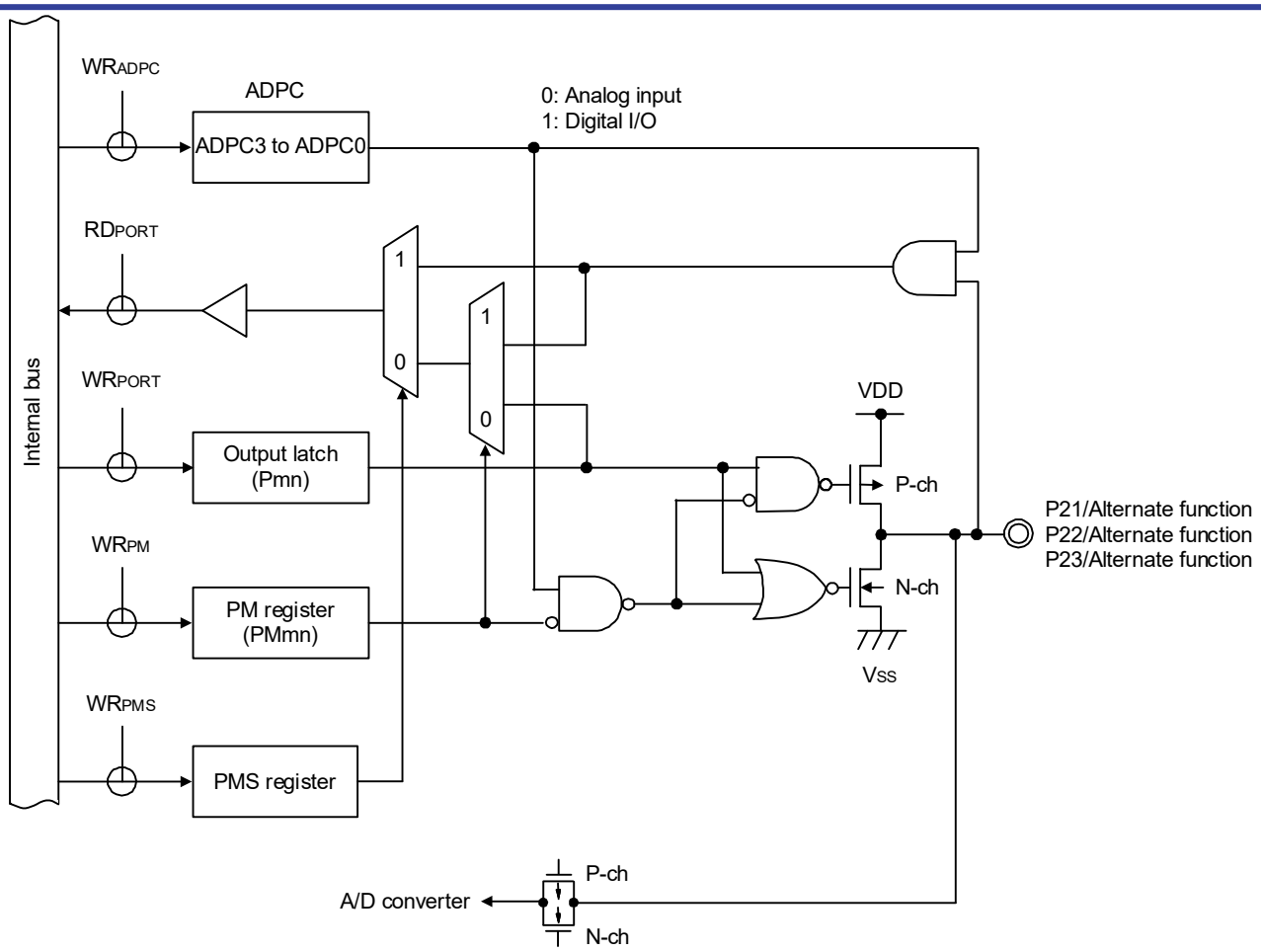
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-2 Pin Block Diagram for Pin type 2-1-2



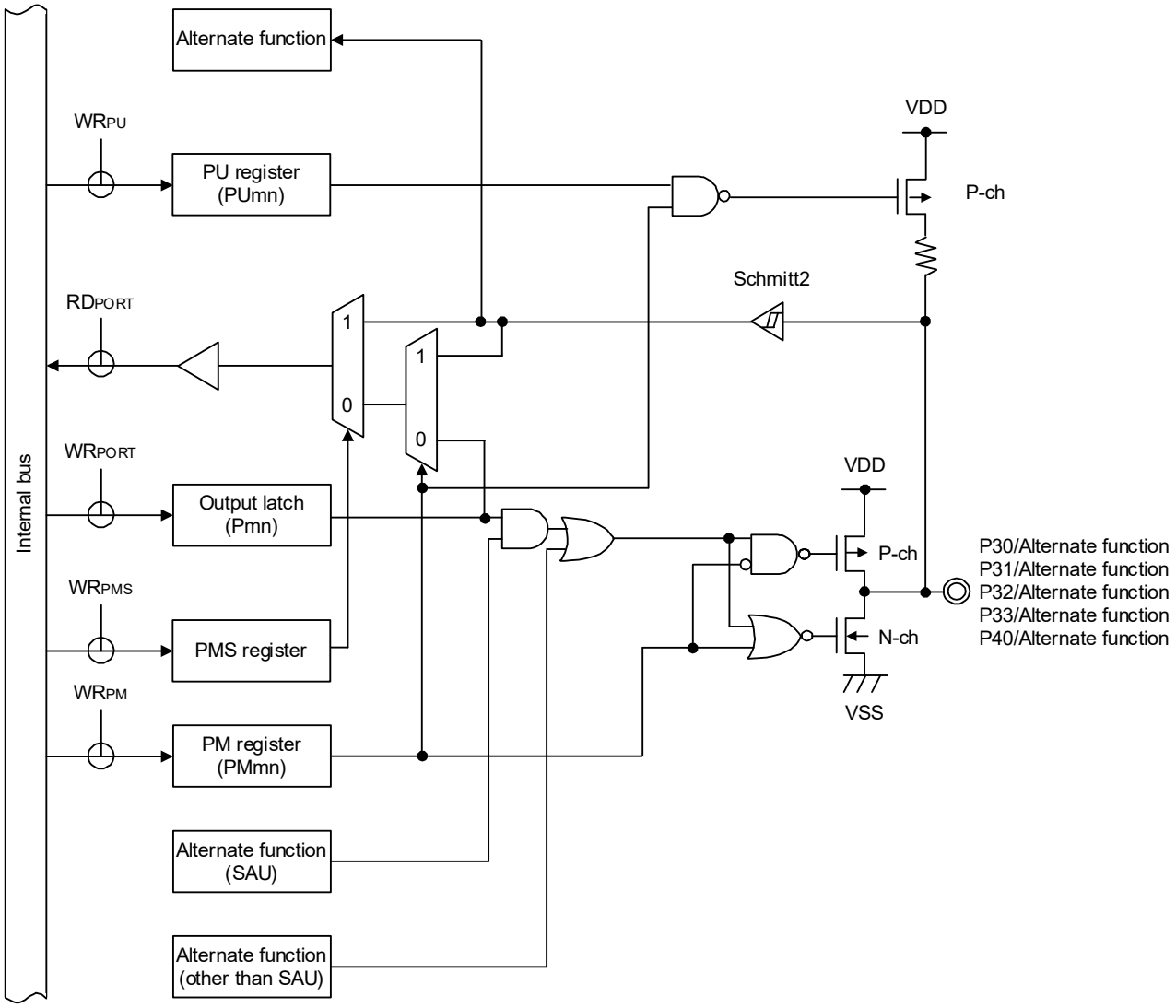
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-3 Pin Block Diagram for Pin type 2-2-2



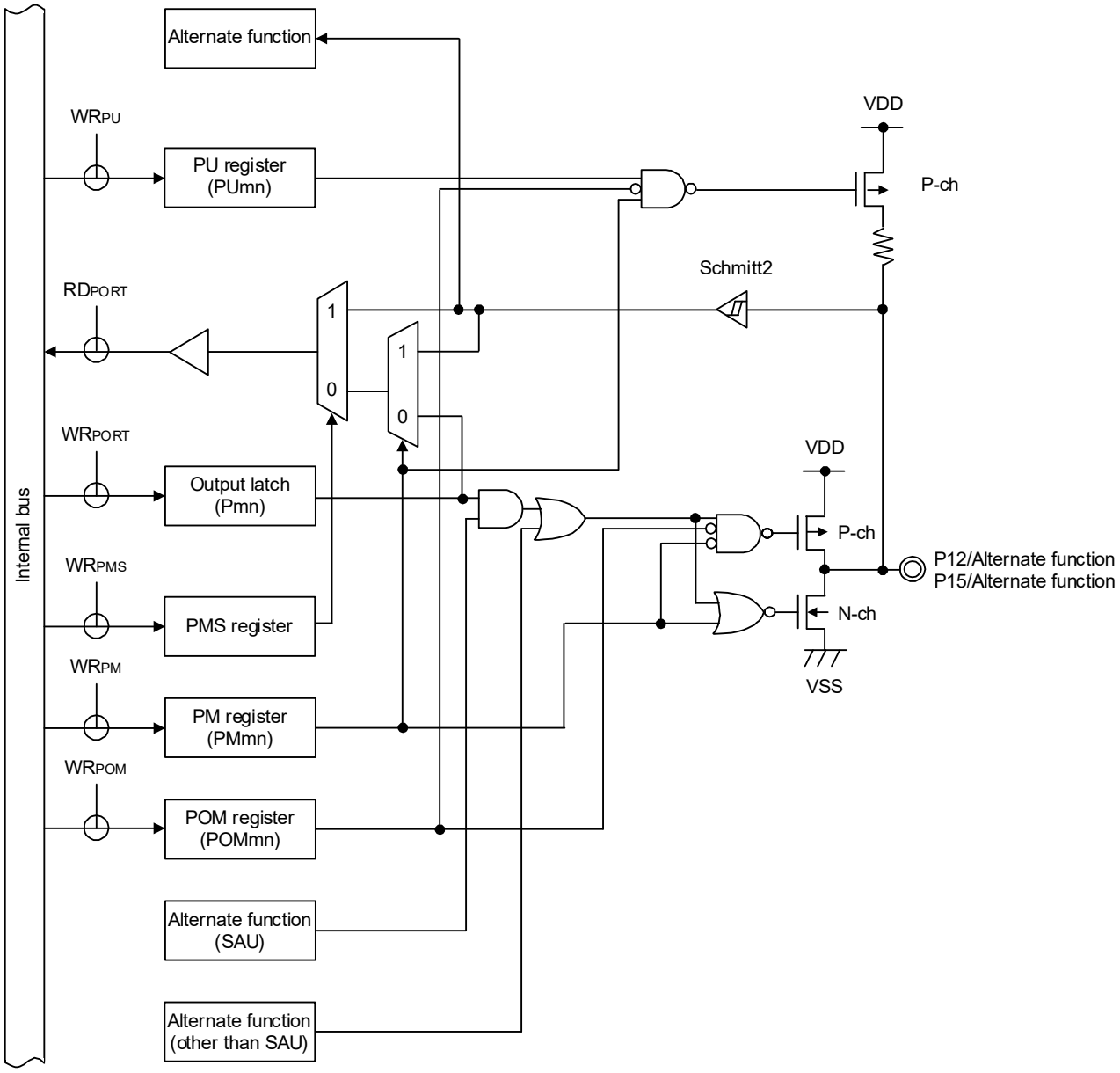
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-4 Pin Block Diagram for Pin type 4-3-3



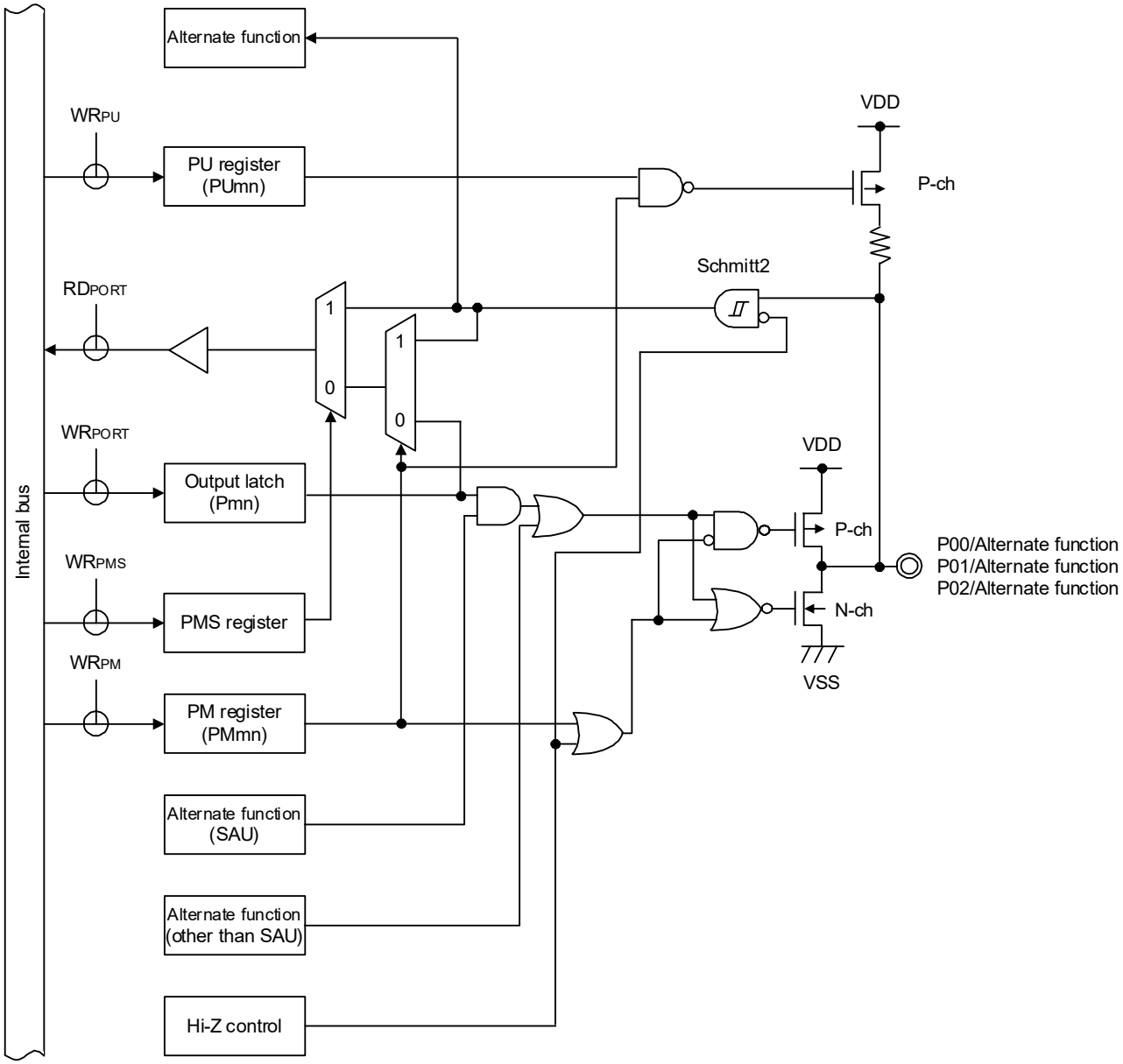
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-5 Pin Block Diagram for Pin type 7-1-3



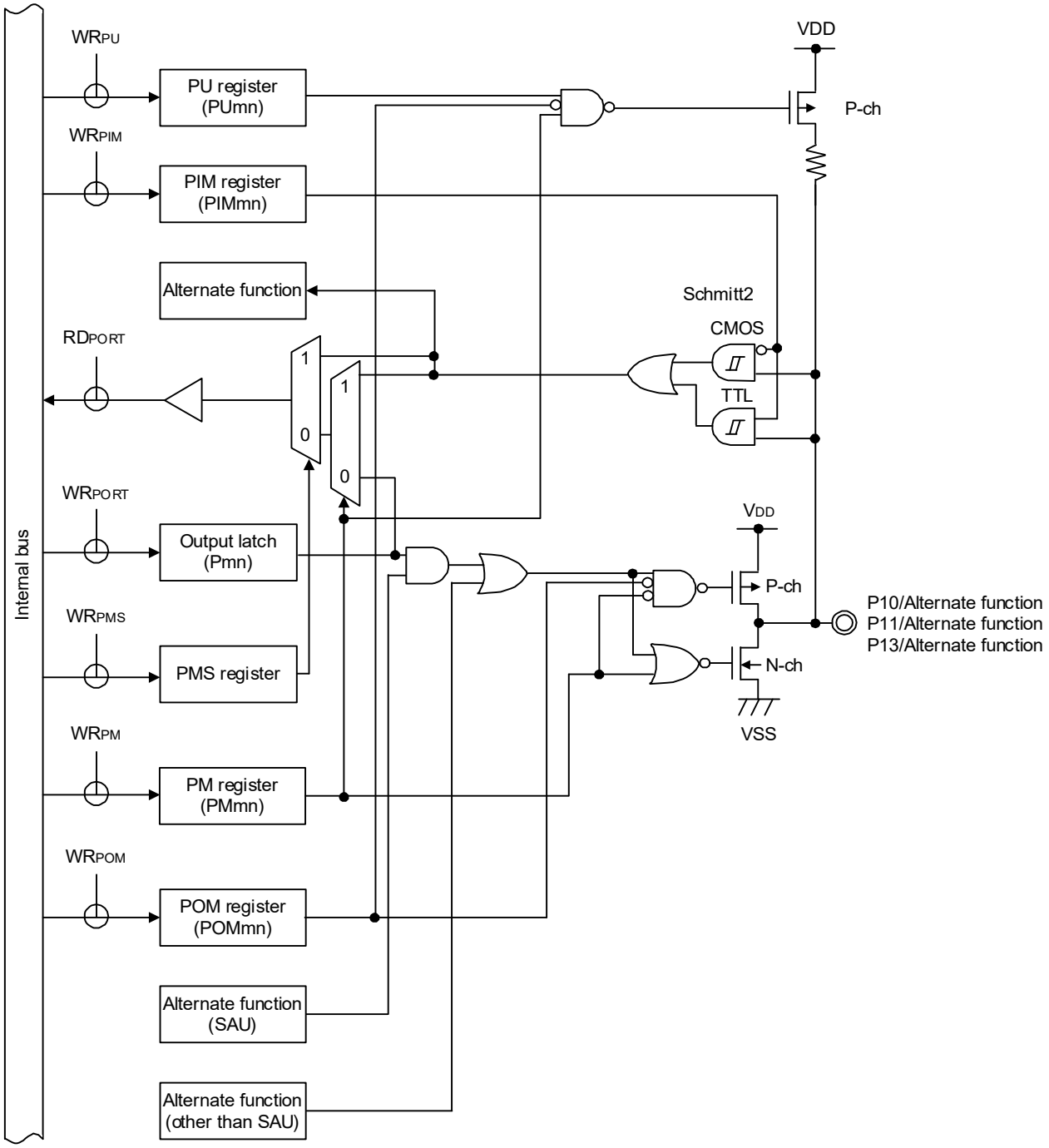
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-6 Pin Block Diagram for Pin type 7-1-4



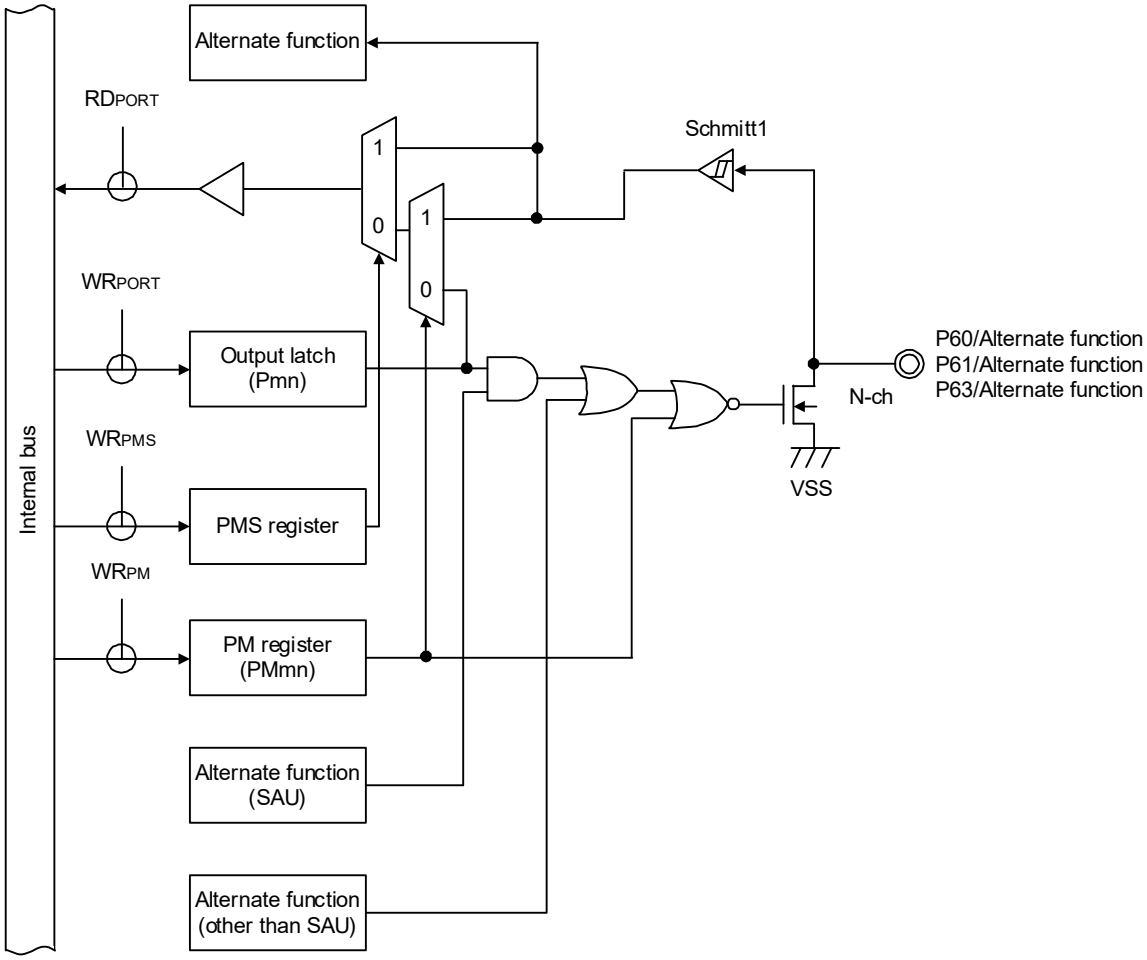
Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-7 Pin Block Diagram for Pin type 7-1-7



Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-8 Pin Block Diagram for Pin type 8-1-4



Remark Refer to Section 3.2.1 Pin type and alternate function for alternate functions.

Figure 3-9 Pin Block Diagram for Pin type 12-1-2

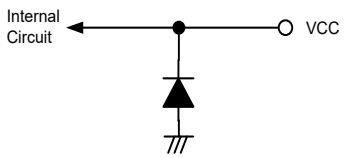


Figure 3-10 Pin Block Diagram for VCC Pin

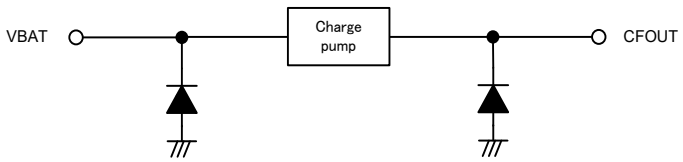


Figure 3-11 Pin Block Diagram for VBAT and CFOUT Pin

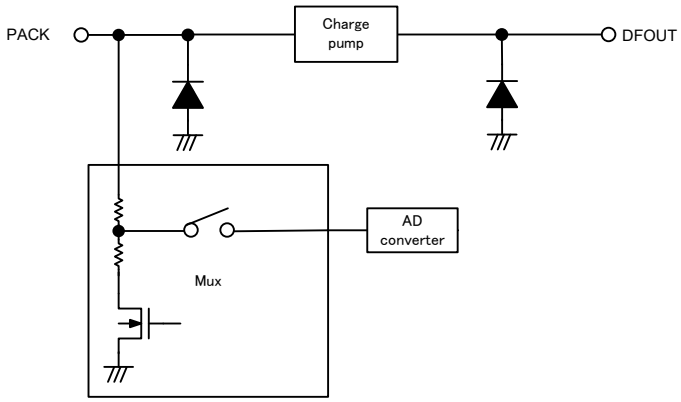


Figure 3-12 Pin Block Diagram for PACK and DFOUT Pin

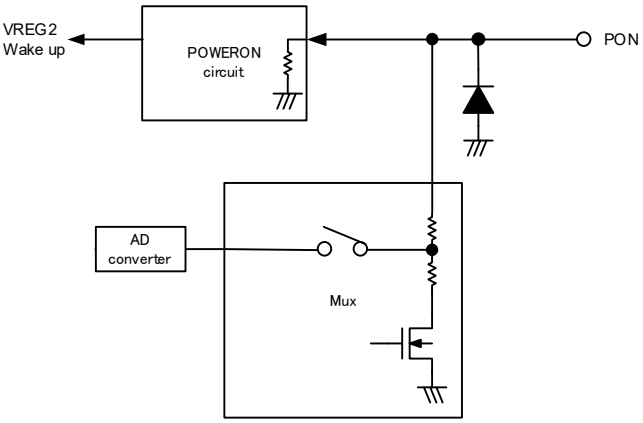


Figure 3-13 Pin Block Diagram for PON Pin

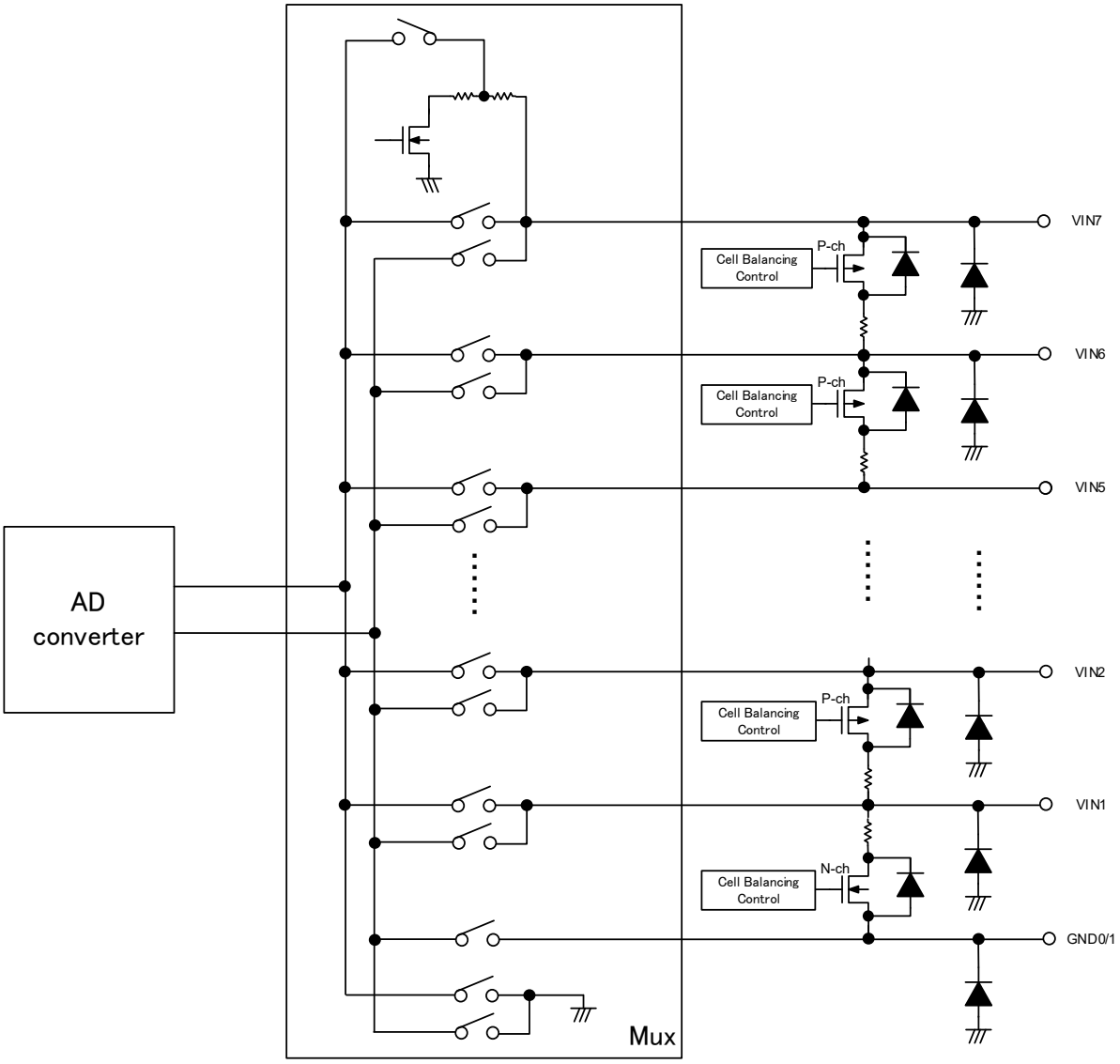


Figure 3-14 Pin Block Diagram for VIN7 to GND0/1 Pin

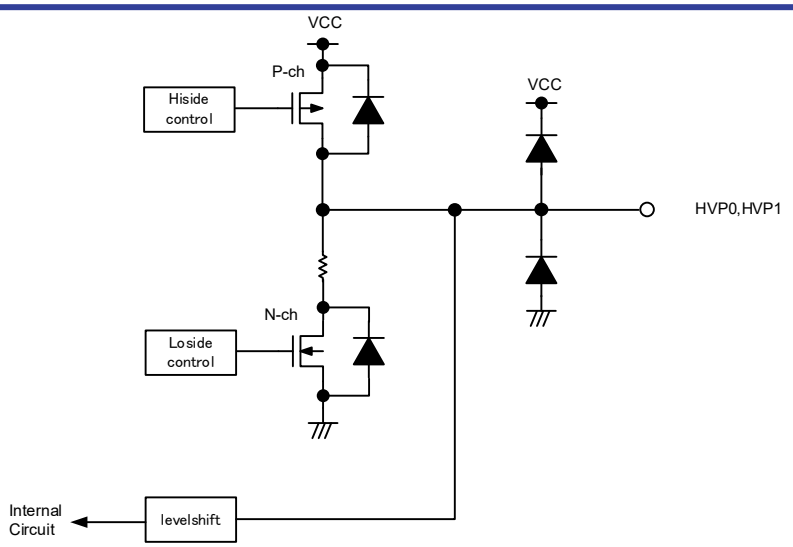


Figure 3-15 Pin Block Diagram for HVP0 Pin and HVP1 Pin

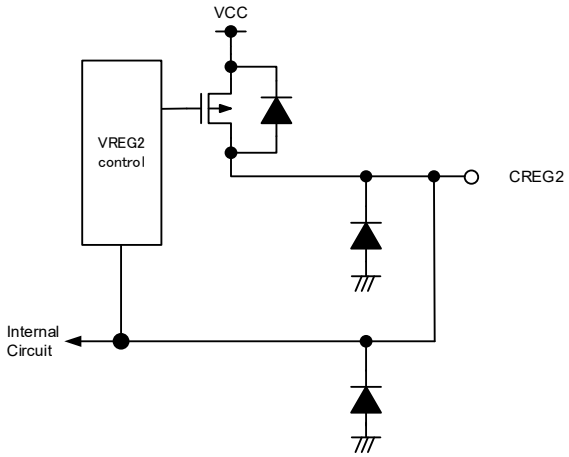


Figure 3-16 Pin Block Diagram for CREG2 Pin

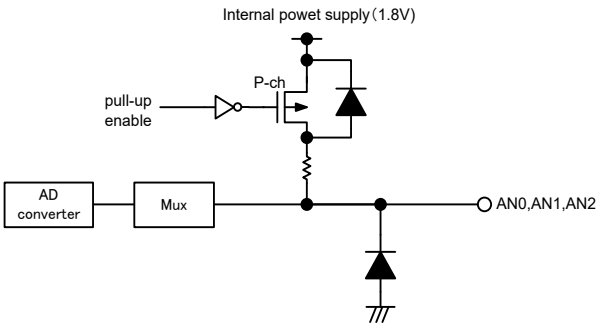


Figure 3-17 Pin Block Diagram for AN0, AN1 and AN2 Pin

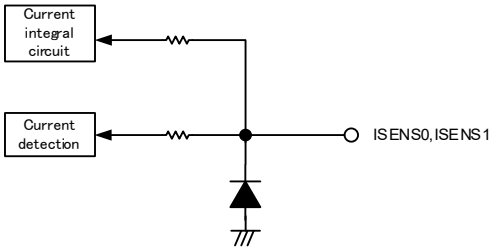


Figure 3-18 Pin Block Diagram for ISENS0 and ISENS1 Pin

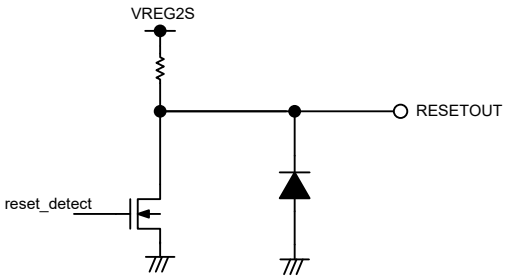


Figure 3-19 Pin Block Diagram for RESETOUT Pin

4. ELECTRICAL SPECIFICATIONS

Caution This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Remark Operating ambient temperature is configurable by REG2T6 bit of REG2T register setting.
In case of setting REG2T6 bit of REG2T register to "0", this device is available in range of TA= -20 to 85°C .
In case of setting REG2T6 bit of REG2T register to "1", this device is available in range of TA= -40 to 85°C.
However, even if REG2T6 bit of REG2T register set to "1", the electrical characteristics which is guaranteed in range of TA = -20 to 85°C is not changed.

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	V_{CC}	VCC		-0.5 to +60.0	V
	V_{DD}	VDD		-0.5 to +6.5	V
	GND	GND0, GND1, VSS		-0.5 to 0.3	V
CREG2 pin input voltage	V_{CREG2}	CREG2		-0.3 to +6.5 Note 2	V
REGC pin input voltage	V_{IREGC}	REGC		-0.3 to 2.8 and -0.3 to (VDD+0.3) Note 1	V
Input voltage	V_{I1}	P00 to P02, P10 to P13, P15, P21 to 23, P40 (TOOL0), P122 to P124, P137, RESET		-0.3 to (VDD+0.3) Note 3	V
	V_{I2}	P60 to P63(N-ch open-drain)		-0.3 to +6.5	V
	V_{IN-H1}	VIN7, VIN6, VIN5, VIN4, VIN3, VIN2, VIN1, VBAT, PACK, PON,		-0.5 to +60.0	V
	V_{IN-H2}	HVP0, HVP1		-0.5 to (VCC+0.3) Note 5	V
	V_{IN-B}	VIN7 to VIN6, VIN6 to VIN5, VIN5 to VIN4, VIN4 to VIN3, VIN3 to VIN2, VIN2 to VIN1		-0.5 to +6.5	V
	V_{IN-L}	AN0, AN1, AN2, ISENS0, ISENS1		-0.5 to +2.0	V
	V_{AI}	ANI0 to ANI2		-0.3 to VDD +0.3 and -0.3 to AVREF(+) +0.3 Notes 3, 4	V
Output voltage	V_{O1}	P00 to P02, P10 to P13, P15, P21 to 23, P40 (TOOL0), RESETOUT		-0.3 to (VDD+0.3) Note 3	V
	V_{O-H}	CFOUT, DFOUT, HVP0, HVP1		-0.5 to +60.0	V
High-level output current	I_{OH1}	Per pin	P00 to P02, P10 to P13, P15, P40 (TOOL0)	-40	mA
		Total of all pins	P00 to P02, P10 to P13, P15, P40 (TOOL0)	-70	mA
	I_{OH2}	Per pin	P21 to P23	-0.5	mA
		Total of all pins	P21 to P23	-2.0	mA
Low-level output current	I_{OL1}	Per pin	P00 to P02, P10 to P13, P15, P40 (TOOL0)	+40	mA
		Total of all pins	P00 to P02, P10 to P13, P15 P40 (TOOL0), P60 to P63	+70	mA
Power consumption	Pd	Topr = 25°C		300	mW
Operating ambient Temperature	TA	REG2T6 bit = 0		-20 to +85	°C
	T_{AL}	REG2T6 bit = 1		-40 to +85	°C
Storage temperature	Tstg	-		-65 to +150	°C

(Note, Caution and Remark are listed on next page.)

Note 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1.0 uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the CREG2 pin to GND0 or GND1 via a capacitor (2.2 uF). This value regulates the absolute maximum rating of the CREG2 pin.

Note 3. Must be 6.5 V or lower.

Note 4. Do not exceed AVREF (+) + 0.3 V in case of A/D conversion target pin.

Note 5. Must be 60 V or lower.

Caution **Product quality may degrade if the absolute maximum rating has been exceeded. The absolute maximum ratings are rated values where the product is on the verge of suffering physical damage, therefore the product must be used within conditions that ensure the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AVREF (+): + side reference voltage of the A/D converter.

Remark 3. GND (GND0, GND1 and VSS): Reference voltage.

4.2 Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply	VCC, VBAT		4.0	-	50.0	V
	VDD		2.7	-	5.5	V
	GND	GND0, GND1, VSS	-	0.0	-	V

4.3 Supply current characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, VDD = CREG2, GND0 = GND1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power down mode current 1	I_{PD}	VCC = 35.0 V			2.0	uA
Power down mode current 2 (Low voltage)	I_{PDL}	VCC = 4.0 V			1.0	uA
Sleep mode current 1	I_{SLP1}	-20°C ≤ T_A ≤ 85°C, REG2T6 bit = 0, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = L, DFOUT = L, AD(AFE) = OFF, CC = OFF		25.0	50.0	uA
	I_{SLP1L}	-40°C ≤ T_A ≤ 85°C, REG2T6 bit = 1, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = L, DFOUT = L, AD(AFE) = OFF, CC = OFF		35	70.0	uA
Sleep mode current 2	I_{SLP2}	-20°C ≤ T_A ≤ 85°C, REG2T6 bit = 0, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = OFF, CC = OFF		50.0	100.0	uA
	I_{SLP2L}	-40°C ≤ T_A ≤ 85°C, REG2T6 bit = 1, MCU operation mode: STOP mode ALOCO = ON, AOCO = OFF CD = ALL ON, AFE timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = OFF, CC = OFF		60	120.0	uA
Normal mode current	I_{NOM}	MCU operation mode: LS (Low-Speed main) mode, f_{HOCO}=8MHz ALOCO = ON, AOCO = ON CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = ON, CC = ON		2.0	3.0	mA

Note. "Sleep mode current 1" is the current consumption when PCON register value is set to "63H".
"Sleep mode current 2" is the current consumption when PCON register value is set to "43H".

Caution After trimming.

4.4 Oscillator Characteristics

4.4.1 MCU On-chip oscillator characteristics

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1, 2	f_{IH}		1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20°C ≤ T_A ≤ 85°C	-1.0		+1.0	%
		-40°C ≤ T_A ≤ 85°C	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.4.2 AFE On-chip oscillator characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AFE on-chip oscillator clock frequency	f_{AOCO}		-	4.194	-	MHz
AFE on-chip oscillator clock frequency accuracy			-2	-	+2	%
AFE on-chip oscillator clock frequency stabilization wait time			-	-	(50)	us
AFE Low-speed on-chip oscillator clock frequency	f_{ALOCO}		-	131.072	-	kHz
AFE Low-speed on-chip oscillator clock frequency accuracy			-5	-	+5	%
AFE Low-speed on-chip oscillator clock frequency stabilization wait time			-	-	(50)	us

Caution After trimming.

Remark Values in brackets are design value.

4.5 Pin characteristics

(1/5)

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00 to P02, P10 to P13, P15, P40	2.7 V ≤ VDD ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P02, P10 to P13, P15, P40 (When duty ≤ 70% Note 3)	4.0 V ≤ VDD ≤ 5.5 V			-55.0	mA
			2.7 V ≤ VDD < 4.0 V			-10.0	mA
		Total of all pins (When duty ≤70% Note 3)	2.7 V ≤ VDD ≤ 5.5 V			-100.0	mA
	I_{OH2}	Per pin for P21 to P23	2.7 V ≤ VDD ≤ 5.5 V			-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.7 V ≤ VDD ≤ 5.5 V			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current from pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = -10.0 mA
Total output current from pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.
A current higher than the absolute maximum rating must not flow into any one pin.

Caution P10 to P13, P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/5)

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00 to P02, P10 to P13, P15, P40				20.0 Note 2	mA
		Per pin for P60, P61, P63				15.0 Note 2	mA
		Total of P00 to P02, P10 to P13, P15, P40 (When duty ≤ 70% Note 3)	4.0 V ≤ VDD ≤ 5.5 V			70.0	mA
			2.7 V ≤ VDD < 4.0 V			15.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				150.0	mA
	I_{OL2}	Per pin for P21 to P23				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.7 V ≤ VDD ≤ 5.5 V			5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.
A current higher than the absolute maximum rating must not flow into any one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/5)

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P02, P10 to P13, P15, P40	Normal input buffer	0.8 VDD		VDD	V
	V_{IH2}	P10, P11, P13	TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V	2.2		VDD	V
			TTL input buffer 3.3 V ≤ VDD < 4.0 V	2.0		VDD	V
			TTL input buffer 2.7 V ≤ VDD < 3.3 V	1.5		VDD	V
	V_{IH3}	P21 to P23		0.7 VDD		VDD	V
	V_{IH4}	P60, P61, P63		0.7 VDD		6.0	V
	V_{IH5}	P122, P137, RESET		0.8 VDD		VDD	V
Input voltage, low	V_{IL1}	P00 to P02, P10 to P13, P15, P40	Normal input buffer	0		0.2 VDD	V
	V_{IL2}	P10, P11, P13	TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ VDD < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ VDD < 3.3 V	0		0.32	V
	V_{IL3}	P21 to P23		0		0.3 VDD	V
	V_{IL4}	P60, P61, P63		0		0.3 VDD	V
	V_{IL5}	P122, P137, RESET		0		0.2 VDD	V

Caution The maximum value of VIH of pins P10 to P13, P15 is VDD, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(4/5)

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P02, P10 to P13, P15, P40	4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -10.0 mA	VDD - 1.5			V
			4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -3.0 mA	VDD - 0.7			V
			2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -1.5 mA	VDD - 0.5			V
	V_{OH2}	P21 to P23	2.7 V ≤ VDD ≤ 5.5 V, IOH2 = -100 uA	VDD - 0.5			V
Output voltage, low	V_{OL1}	P00 to P02, P10 to P13, P15, P40	4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 20.0 mA			1.3	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA			0.7	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 3.0 mA			0.6	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA			0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 0.6 mA			0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 0.3 mA			0.4	V
	V_{OL2}	P21 to P23	1.6 V ≤ VDD ≤ 5.5 V, IOL2 = 400 uA			0.4	V
	V_{OL3}	P60, P61, P63	4.0 V ≤ VDD ≤ 5.5 V, IOL3 = 15.0 mA			2.0	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL3 = 5.0 mA			0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL3 = 3.0 mA			0.4	V
			1.8 V ≤ VDD ≤ 5.5 V, IOL3 = 2.0 mA			0.4	V
			1.6 V ≤ VDD ≤ 5.5 V, IOL3 = 1.0 mA			0.4	V

Caution P10 to P13, P15 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(5/5)

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P02, P10 to P13, P15, P40	VI = VDD				1	uA
	I_{LIH2}	P21 to P23, P137, RESET	VI = VDD				1	uA
	I_{LIH3}	P122	VI = VDD	In input port or external clock input			1	uA
				In resonator connection			10	uA
Input leakage current, low	I_{LIL1}	P00 to P02, P10 to P13, P15, P40	VI = VSS				-1	uA
	I_{LIL2}	P21 to P23, P137, RESET	VI = VSS				-1	uA
	I_{LIL3}	P122	VI = VSS	In input port or external clock input			-1	uA
				In resonator connection			-10	uA
On-chip pull-up resistance	R_U	P00 to P02, P10 to P13, P15, P40	VI = VSS, In input port		10	20	100	kΩ
	R_{UA}	AN0, AN1, AN2			7.5	10	12.5	kΩ
	R_{UAR}	RESETOUT				20		kΩ

Remark 1. Unless specified, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. Regarding pin characteristics of CFOUT, DFOUT, refer to Section 4.8.6 Charge/discharge FET control circuit characteristics.

Remark 3. Regarding pin characteristics of VIN1 to VIN7 refer to Section 4.8.2 Multiplexer.

Remark 4. Regarding pin characteristics of HVP0 to HVP1 refer to Section 4.8.1 High-voltage port characteristics.

4.6 AC Characteristics

(1/2)

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	0.03125		1	us
			LS (low-speed main) mode	0.125		1	us
			LV (low-voltage main) mode	0.25		1	us
		Subsystem clock (f_{SUB}) operation		28.5	30.5	31.3	us
		In the self-programming mode	HS (high-speed main) mode	0.03125		1	us
			LS (low-speed main) mode	0.125		1	us
			LV (low-voltage main) mode	0.25		1	us
External system clock frequency	f_{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t_{EXHS}, t_{EXLS}			13.7			us
TI00 to TI02 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} +10			ns

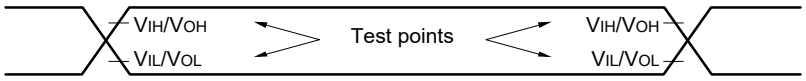
Remark f_{MCK} : Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

(2/2)

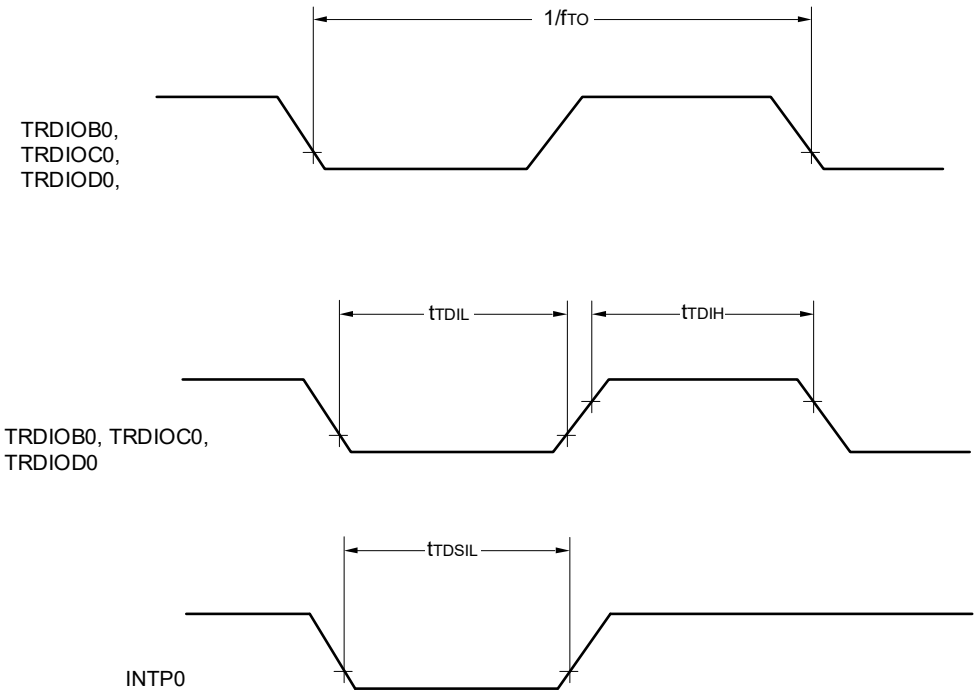
(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOB0, TRDIOC0, TRDIOD0		3/f_{CLK}			ns
TRDIOB0, TRDIOC0, TRDIOD0 output frequency	f_{TO}	HS (high-speed main) mode	4.0 V ≤ VDD ≤ 5.5 V			16	MHz
			2.7 V ≤ VDD < 4.0 V			8	MHz
		LS (low-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V			4	MHz
		LV (low-voltage main) mode	2.7 V ≤ VDD ≤ 5.5 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP13	1.6 V ≤ VDD ≤ 5.5 V	1			us
RESET low-level width	t_{RSL}			10			us

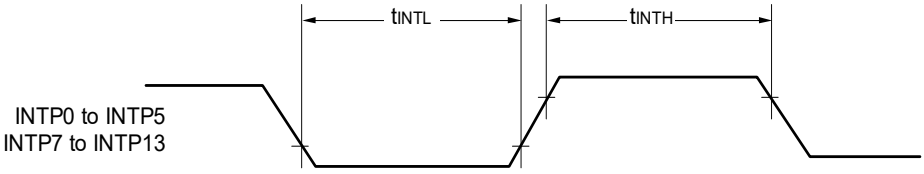
AC Timing Test Points



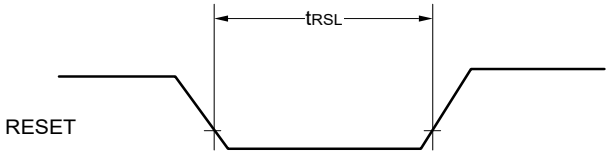
TI/TO Timing



Interrupt Request Input Timing

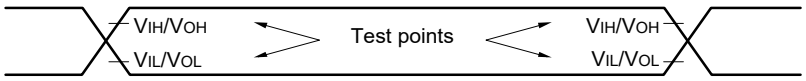


RESET Input Timing



4.7 MCU peripheral circuit characteristics

AC Timing Test Points



4.7.1 Serial array unit

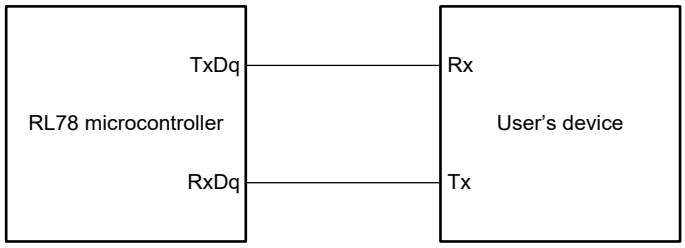
(1) During communication at same potential (UART mode)

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

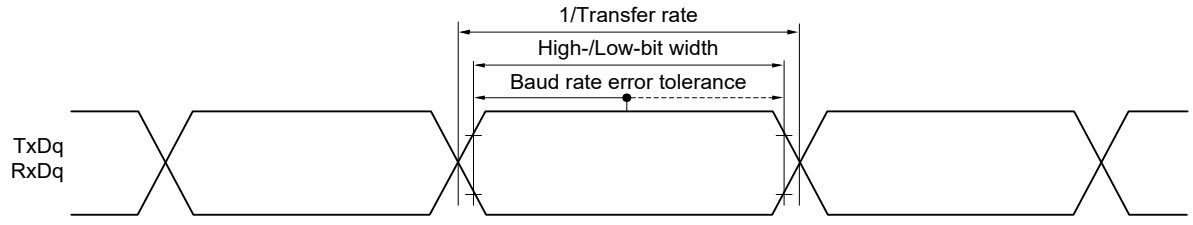
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note				fMCK/6		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK		5.3		1.3		0.6	Mbps

Note Transfer rate in the SNOOZE mode is only 4800 bps.

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).



UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	125		500		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ VDD ≤ 5.5 V	t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ VDD ≤ 5.5 V	t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ VDD ≤ 5.5 V	44		110		110		ns
		2.7 V ≤ VDD ≤ 5.5 V	44		110		110		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		19		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4		25		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ VDD ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ VDD ≤ 5.5 V	1 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ VDD ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ VDD ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}			1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4			2/f_{MCK} + 44		2/f_{MCK} + 110		2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

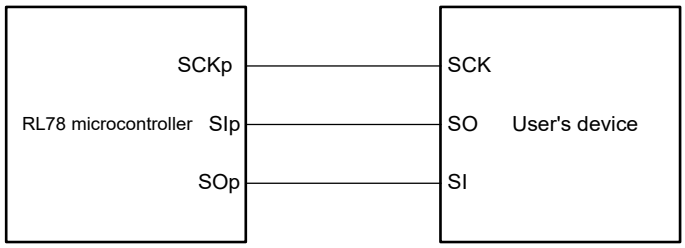
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02))

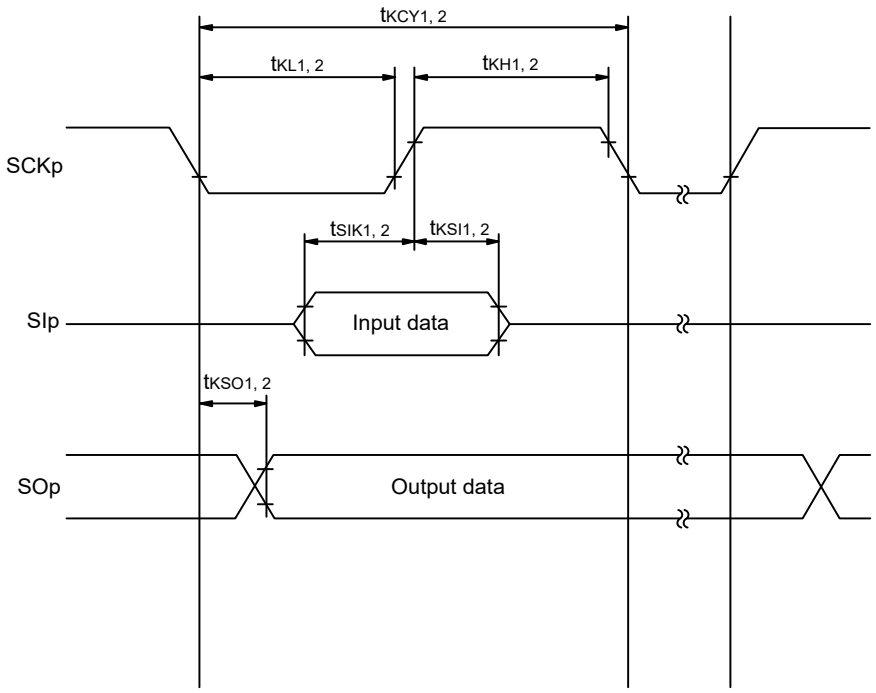


CSI mode connection diagram (during communication at same potential)

Remark 1. p: CSI number (p = 00, 10)

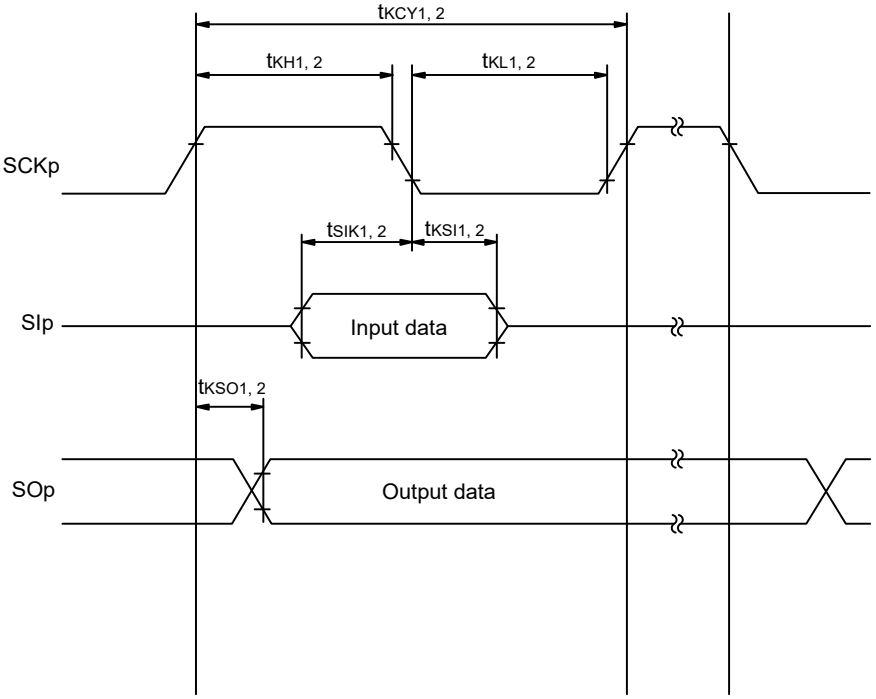
Remark 2. m: Unit number, n: Channel number (mn = 00, 02)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



CSI mode serial transfer timing (during communication at same potential)

Remark 1. p: CSI number (p = 00, 10)

Remark 2. m: Unit number, n: Channel number (mn = 00, 02)

(4) During communication at same potential (simplified I²C mode)

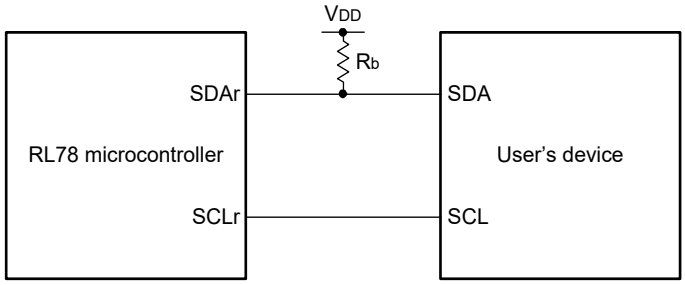
(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note2		ns
Data hold time (transmission)	$t_{HD: DAT}$	2.7 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns

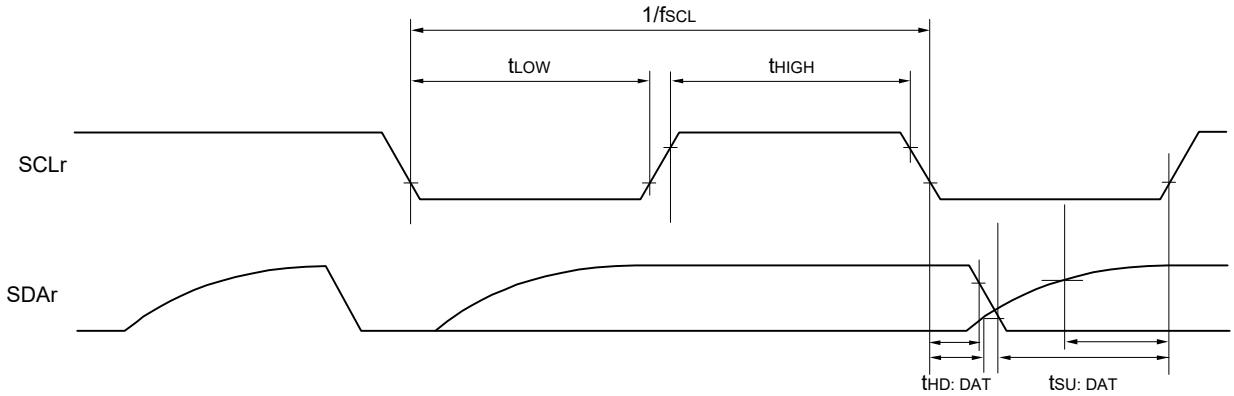
Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value not to over the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)

Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 10), g: PIM number (g = 10, 13), h: POM number (h = 11, 14)

Remark 3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

4.7.2 Serial interface IICA

(1) I^2C standard mode

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0	100	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		4.7		4.7		us
Hold time Note 1	$t_{HD:STA}$		4.0		4.0		4.0		us
Hold time when SCLA0 = “L”	t_{LOW}		4.7		4.7		4.7		us
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		4.0		4.0		us
Data setup time (reception)	$t_{SU:DAT}$		250		250		250		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	0	3.45	0	3.45	us
Setup time of stop condition	$t_{SU:STO}$		4.0		4.0		4.0		us
Bus-free time	t_{BUF}		4.7		4.7		4.7		us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

(2) I^2C fast mode

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: fCLK ≥ 3.5 MHz	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$		0.6		0.6		0.6		us
Hold time[Note1]	$t_{HD: STA}$		0.6		0.6		0.6		us
Hold time when SCLA0 = “L”	t_{LOW}		1.3		1.3		1.3		us
Hold time when SCLA0 = “H”	t_{HIGH}		0.6		0.6		0.6		us
Data setup time (reception)	$t_{SU: DAT}$		100		100		100		ns
Data hold time (transmission) Note2	$t_{HD: DAT}$		0	0.9	0	0.9	0	0.9	us
Setup time of stop condition	$t_{SU: STO}$		0.6		0.6		0.6		us
Bus-free time	t_{BUF}		1.3		1.3		1.3		us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

(3) I^2C fast mode plus

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

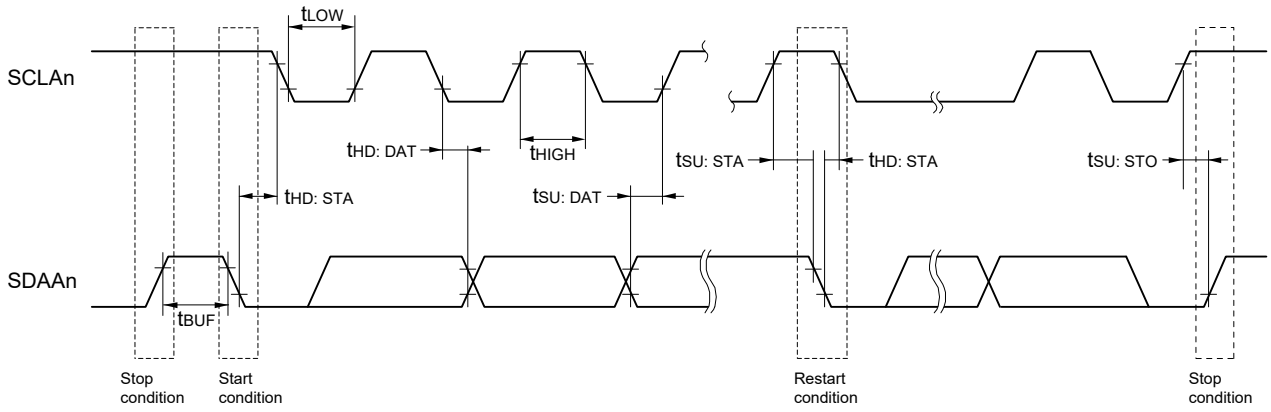
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: fCLK ≥ 10 MHz	0	1000					kHz
Setup time of restart condition	$t_{SU: STA}$		0.26						us
Hold time Note 1	$t_{HD: STA}$		0.26						us
Hold time when SCLA0 = “L”	t_{LOW}		0.5						us
Hold time when SCLA0 = “H”	t_{HIGH}		0.26						us
Data setup time (reception)	$t_{SU: DAT}$		50						ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	0.45					us
Setup time of stop condition	$t_{SU: STO}$		0.26						us
Bus-free time	t_{BUF}		0.5						us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: Cb = 120 pF, Rb = 1.1 kΩ



IICA serial transfer timing

Remark n = 0

4.7.3 A/D converter characteristics

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI2, internal reference voltage, and temperature sensor output voltage

(T_A = -40/-20 to +85°C, 2.7 V ≤ AVREFP = VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bits
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 3	2.7 V ≤ AVREFP ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin : ANI2-ANI3	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	us
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	us
		10-bit resolution Target pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	us
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	us
Zero-scale error Note 1, 2	EZS	10-bit resolution AVREFP = VDD Note 3	2.7 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Full-scale error Note 1, 2	EFS	10-bit resolution AVREFP = VDD Note 3	2.7 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 3	2.7 V ≤ AVREFP ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 3	2.7 V ≤ AVREFP ≤ 5.5 V			±1.5	LSB
Analog input voltage	VAIN	ANI2		0		AVREFP	V
		Internal reference voltage (2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VBGR Note 4			V
		Temperature sensor output voltage (2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VTMPS25 Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. Refer to Section 4.7.4 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = VSS (ADREFM = 0),

target pin: ANI0 to ANI02, internal reference voltage, and temperature sensor output voltage

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V, Reference voltage (+) = VDD, Reference voltage (-) = VSS)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bits
Overall error Note 1	AINL	10-bit resolution			1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin : ANI0 to ANI2	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	us
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	us
		10-bit resolution Target pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	us
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	us
Zero-scale error Note 1, 2	EZS	10-bit resolution				±0.60	%FSR
Full-scale error Note 1, 2	EFS	10-bit resolution				±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution				±4.0	LSB
Differential linearity Note 1	DLE	10-bit resolution				±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI2		0		VDD	V
		Internal reference voltage (2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VBGR Note 3			V
		Temperature sensor output voltage (2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)		VTMPS25 Note 3			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to Section 4.7.4 Temperature sensor characteristics/internal reference voltage characteristic.

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V, Reference voltage (+) = VBGR Note 3, Reference voltage (-) = AVREFM = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bits	
Conversion time	tCONV	8-bit resolution		17		39	us
Zero-scale error Note 1, 2	EZS	8-bit resolution				±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution				±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution				±1.0	LSB
Analog input voltage	VAIN			0		VBGR Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 4.7.4 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

4.7.4 Temperature sensor characteristics/internal reference voltage characteristic

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output	VTMPS25	Setting ADS register = 80H, TA = +25C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		5			us

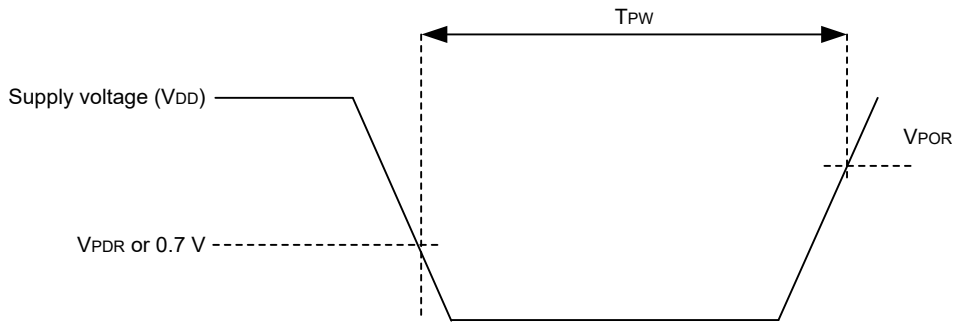
4.7.5 POR circuit characteristics (MCU)

(T_A = -40/-20 to +85°C, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	V_{PDR}	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW}		300			us

Note 1. However, when operating voltage drops when LVD is off, it enters STOP mode, or enable the reset status using external reset pin before the voltage drops below the operating voltage range shown in Section 4.6 AC Characteristics.

Note 2. Minimum time required for POR to reset when VDD is below VPDR. This is also the minimum time required for a POR reset when VDD exceeds VPOR after VDD is below 0.7 V during STOP mode or while the main system clock is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.7.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T_A= -40/-20 to +85°C, VPDR ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVI0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVI1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVI2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVI3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVI4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVI5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVI6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVI7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVI8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVI9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVI10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVI11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVI12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVI13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			us
Detection delay time		t_{LD}				300	us

(2) Interrupt & Reset Mode

(T_A= -40/-20 to +85°C, VPDR ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V_{LVDA0}	VPOC2, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V_{LVDA1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVDB1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVDC1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVDD1}		LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}		LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}		LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

4.8 AFE peripheral circuit characteristics

4.8.1 High-voltage port characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		2.6			V
Input voltage, low	V_{IL}				0.7	V
Output voltage, high	V_{OH}	IOH = -1 mA	VCC - 0.7		VCC	V
Output voltage, low	VoL	IOL = 1 mA			0.7	V
On resistance, high level output (Pch MOS output)	R_{ONP}	IOH = -1 mA			700	Ω
On resistance, high level output (Nch MOS output)	R_{ONN}	IOL = 1 mA			700	Ω
Pin leakage current	I_{LK}	VI = VCC, GND			±1	uA

4.8.2 Multiplexer characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain VIN(n)-VIN(n-1)	GAIN1	VIN7, VIN6, VIN5 ≥ 2.0 V VIN4, VIN3, VIN2, VIN1 ≥ 0 V Note		1.0		V/V
Gain PACK, VIN7, PON	GAIN2			0.1		V/V
Gain AN0,1,2	GAIN3			1.0		V/V
Input voltage range VIN(n)-VIN(n-1)	VRA1		-0.1		5.1	V
Input voltage range PACK, VIN7, PON	VRA2		0.0		50.0	V
Input voltage range AN0, 1, 2	VRA3		0.0		1.8	V
Pin leakage current	I_{LKV1}	VIN1 = 5 V			2	uA
		VIN2 = 10 V			2	uA
		VIN3 = 15 V			2	uA
		VIN4 = 20 V			2	uA
		VIN5 = 25 V			2	uA
		VIN6 = 30 V			2	uA
		VIN7 = 35 V			2	uA

Note Reference voltage is GND0 and GND1

4.8.3 Sigma-delta A/D converter characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution Note1	RESAD	Conversion time = 8 ms			15	bits
		Conversion time = 4 ms			14	bits
		Conversion time = 2 ms			13	bits
		Conversion time = 1 ms			12	bits
		Conversion time = 0.5 ms			11	bits
		Conversion time = 0.25 ms			10	bits
Input voltage range	VINAD		-0.1		5.1	V
Integral nonlinearity	INLAD	End fit	-27		27	LSB
Conversion result in zero input	ADZERO	VIN = 0 V		3317 Note 2		LSB
Temperature dependency In zero input	dTADZERO	VIN = 0 V	-0.24		+0.24	LSB/°C
Conversion result in full-scale input	ADFS	VIN = 5.1 V		24100 Note 2		LSB
Temperature dependency in full-scale input	dTADFS	VIN = 5.1 V	-0.24		+0.24	LSB/°C
Input resistance	RINAD			(1.0)		MΩ
Battery cell voltage measurement error	ERRCELL1	T_A = +25°C After calibration			±5	mV
	ERRCELL2	-20°C ≤ T_A ≤ 85°C After calibration			±10	mV
	ERRCELL2L	-40°C ≤ T_A ≤ 85°C After calibration			±12	mV

Note 1. AD conversion result is output in 15-bit.

Note 2. This value is before subtracting the offset voltage.

Caution 1. Except for Battery cell voltage measurement error (ERRCELL), these parameters are sigma-delta converter circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in brackets are design value.

4.8.4 Current integrating circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RESCC				18	bits
Conversion time	TCC			250		ms
Input voltage range	VINCC	±50 mV mode ISENS1 to ISENS0	-50		+50	mV
		±100 mV mode ISENS1 to ISENS0	-100		+100	mV
		±200 mV mode ISENS1 to ISENS0	-200		+200	mV
Integral nonlinearity	INLCC	End fit			0.02	%FSR
Input resistance	RINCC	ISENS0, ISENS1		(1.0)		MΩ
Current measurement error	ERRCURR	±50 mV mode, -20°C ≤ T_A ≤ 85°C After calibration			(±25)	uV
		±50 mV mode, -40°C ≤ T_A ≤ 85°C After calibration			(±30)	uV
		±100 mV mode -20°C ≤ T_A ≤ 85°C After calibration			(±50)	uV
		±100 mV mode -40°C ≤ T_A ≤ 85°C After calibration			(±60)	uV
		±200 mV mode -20°C ≤ T_A ≤ 85°C After calibration Input voltage range : -100 mV to 200 mV			(±100)	uV
		±200 mV mode -40°C ≤ T_A ≤ 85°C After calibration Input voltage range : -100 mV to 200 mV			(±120)	uV

Caution 1. Except for Current measurement error (ERRCURR), these parameters are current integration circuit characteristics

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in brackets are design value.

4.8.5 Overcurrent detection / wakeup current detection circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current detection setting voltage step	dSVSC	25 mV to 200 mV		12.5		mV
		200 mV to 300 mV		25		mV
Discharge short-circuit current detection voltage error	dVSC	25 mV to 200 mV setting			±12.5	mV
		225 mV to 300 mV setting			±25.0	mV
Discharge overcurrent detection setting voltage step	dSVDOC	15 mV to 100 mV		2.5		mV
		100 mV to 200 mV		5		mV
Discharge overcurrent detection voltage error Note 1	dVDOC	15 mV to 100 mV setting			±5.0	mV
		105 mV to 200 mV setting			±7.5	mV
Charge overcurrent detection setting voltage step	dSVCOC	-60 mV to -2.5 mV		2.5		mV
		-100 mV to -60 mV		5		mV
Charge overcurrent detection voltage error Note 1	dVCOC	-60 mV to -2.5 mV setting			±5.0	mV
		-100 mV to -65 mV setting			±7.5	mV
Discharge wakeup current detection setting voltage step	dSVDWU	0 mV to 140 mV		1.25		mV
Charge wakeup current detection setting voltage step	dSVCWU	-140 mV to 0 mV		1.25		mV
DBPT current detection setting voltage step	dSVDBPT	0 mV to 140 mV		1.25		mV
Discharge wakeup current detection voltage error Note 1	dVDWU	20 times mode ISENS1 to ISENS0: 0.25 mV to 2.5 mV	-0.10	0.0	+0.25	mV
Charge wakeup current detection voltage error Note 1	dVCWU	20 times mode ISENS1 to ISENS0: -0.25 mV to -2.5 mV	-0.25	0.0	+0.10	mV
DBPT current detection voltage error Note 1	dVDBPT	20 times mode ISENS1 to ISENS0: 0.25 mV to 2.5 mV	-0.10	0.0	+0.25	mV
Discharge short-circuit current detection time error Note 2	dTSC	0 us to 916 us (61us step	0.0		30.5	us
Discharge overcurrent detection time error Note 2	dTDOC	0.488 ms to 32 s (0.488ms step)	0.0		122	us
Charge overcurrent detection time error	dTCOC	0 us to 15564 us (61us step)	0.0		30.5	us
Discharge wakeup current detection time error Note 2	dTDWU	3.91 ms to 62.56 ms (61us step)	0		3.9	ms
Charge wakeup current detection time error Note 2	dTCWU	3.91 ms to 62.56 ms (61us step)	0		3.9	ms
DBPT current detection time error Note 2	dTDBPT	0 us to 916 us (61us step)	0.0		30.5	us

Note 1. This is the specification after zero-calibration is executed.

Note 2. The frequency error of On-chip oscillator (AOCO and ALOCO) is excluded from these detection time error.

4.8.6 Charge/discharge FET control circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-side Charge FET control Output voltage, CFOUT=H	CFON1	4.0 V ≤ VCC < 6.0 V Load between CFOUT to VBAT = 50nF/10MΩ Based on VBAT pin	5.0	9.5	10.0	V
	CFON2	6.0 V ≤ VCC, -20°C ≤ T_A ≤ 85°C Load between CFOUT to VBAT = 50nF/10MΩ Based on VBAT pin	8.0	9.5	10.0	V
	CFON2L	6.0 V ≤ VCC, -40°C ≤ T_A ≤ 85°C Load between CFOUT to VBAT = 50nF/10MΩ Based on VBAT pin	6.5	9.5	10.0	V
High-side Charge FET control Output voltage, CFOUT=L	CFOFF	Load between CFOUT to VBAT = 50nF/10MΩ Based on VBAT pin	-0.2	0.0	0.2	V
High-side Charge FET control CFOUT rise Time	CFTR1	4.0 V ≤ VCC < 6.0 V Load between CFOUT to VBAT = 50nF/10MΩ Lo(VBAT)→Hi(VBAT+5 V)		1.5	2.5	ms
	CFTR2	6.0 V ≤ VCC Load between CFOUT to VBAT = 50nF/10MΩ Lo(VBAT)→Hi(VBAT+5 V)		1.0	1.5	ms
High-side Charge FET control CFOUT fall Time	CFTF1	Load between CFOUT to VBAT = 50nF/10MΩ Hi(VBAT+CFON1)→Lo(VBAT+1 V) OFF speed acceleration = Disable		0.5	1.0	ms
	CFTF2	Load between CFOUT to VBAT = 50nF/10MΩ Hi(VBAT+CFON1)→Lo(VBAT+1 V) OFF speed acceleration = Enable		(0.2)	(0.5)	ms
High-side Discharge FET control Output voltage, DFOUT=H	DFON1	4.0 V ≤ VCC < 6.0 V Load between DFOUT to PACK = 50nF/10MΩ Based on PACK pin	5.0	9.5	10.0	V
	DFON2	6.0 V ≤ VCC, -20°C ≤ T_A ≤ 85°C Load between DFOUT to PACK = 50nF/10MΩ Based on PACK pin	8.0	9.5	10.0	V
	CFON2L	6.0 V ≤ VCC, -40°C ≤ T_A ≤ 85°C Load between CFOUT to VBAT = 50nF/10MΩ Based on VBAT pin	6.5	9.5	10.0	V
High-side Discharge FET control Output voltage, DFOUT=L	DFOFF	Load between DFOUT to PACK = 50nF/10MΩ Based on PACK pin	-0.2	0.0	0.2	V
High-side Discharge FET control DFOUT rise Time	DFTR1	4.0 V ≤ VCC < 6.0 V Load between DFOUT to PACK = 50nF/10MΩ Lo(PACK)→Hi(PACK+5 V)		1.5	2.5	ms
	DFTR2	6.0 V ≤ VCC Load between DFOUT to PACK = 50nF/10MΩ Lo(PACK)→Hi(PACK+5 V)		1.0	1.5	ms
High-side Discharge FET control DFOUT fall Time	DFTF1	Load between DFOUT to PACK = 50nF/10MΩ Hi(PACK+DFON1)→Lo(PACK+1 V) OFF speed acceleration = Disable		0.5	1.0	ms
	DFTF2	Load between DFOUT to PACK = 50nF/10MΩ Hi(PACK+DFON1)→Lo(PACK+1 V) OFF speed acceleration = Enable		(0.2)	(0.5)	ms
Low-side Charge FET control Clamp voltage	CCLPON1	Based on VBAT pin 4.0 V ≤ VBAT < 7.0 V	-6.0		-3.0	V
	CCLPON2	Based on VBAT pin 7.0 V ≤ VBAT	-14.0	-10.0	-6.0	V
Low-side Discharge FET control Clamp voltage	DCLPON1	Based on PACK pin 4.0 V ≤ PACK < 7.0 V	-6.0		-3.0	V
	DCLPON2	Based on PACK pin 7.0 V ≤ PACK	-14.0	-10.0	-6.0	V

Caution After trimming.

Remark Values in brackets are design value.

4.8.7 Power on circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, High	V_{IH}		2.6		VCC	V
Input voltage, Low	V_{IL}		0.0		0.7	V
Pull-down resistance	Rdpon			12.4		MΩ

Caution To entry power down mode, it is necessary to input power down command while PON port is L.

4.8.8 Series regulator circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage	VR2O	3.3 V setting	Io = 50 uA to 20 mA,	3.20	3.30	3.40	V
	VR2O5	5.0 V setting	6.0 V ≤ VCC ≤ 50.0 V, Io = 50 uA to 20 mA	4.85	5.00	5.15	V
Load drive capability Note	IOMAX	3.3 V setting	4.0 V ≤ VCC < 5.0 V	10.0			mA
			5.0 V ≤ VCC ≤ 50.0 V	20.0			mA
	IOMAX5	5.0 V setting	6.0 V ≤ VCC < 7.0 V	10.0			mA
			7.0 V ≤ VCC ≤ 50.0 V	20.0			mA

Note In case of using load drive, total power consumption must be under the maximum ratings power consumption (Pd).

Caution After trimming.

4.8.9 AFE reset circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 release voltage	V_{REL}		2.8	2.9	3.0	V
VREG2 detection voltage	V_{DET}	After trimming	2.7	2.8	2.9	V

4.8.10 Cell balancing circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
1st cell on resistance	R_{COND1}	VIN1 – GND0/1 = 3.5 V	100	200	400	Ω
2nd cell on resistance	R_{COND2}	VIN2 – VIN1 = 3.5 V	100	200	400	Ω
3rd cell on resistance	R_{COND3}	VIN3 – VIN2 = 3.5 V	100	200	400	Ω
4th cell on resistance	R_{COND4}	VIN4 – VIN3 = 3.5 V	100	200	400	Ω
5th cell on resistance	R_{COND5}	VIN5 – VIN4 = 3.5 V	100	200	400	Ω
6th cell on resistance	R_{COND6}	VIN6 – VIN5 = 3.5 V	100	200	400	Ω
7th cell on resistance	R_{COND7}	VIN7 – VIN6 = 3.5 V	100	200	400	Ω

4.8.11 VREG2 Voltage Drop Detection Circuit characteristics

(T_A = -40/-20 to +85°C, 4.0 V ≤ VCC ≤ 50 V, GND0 = GND1 = VSS = 0 V)

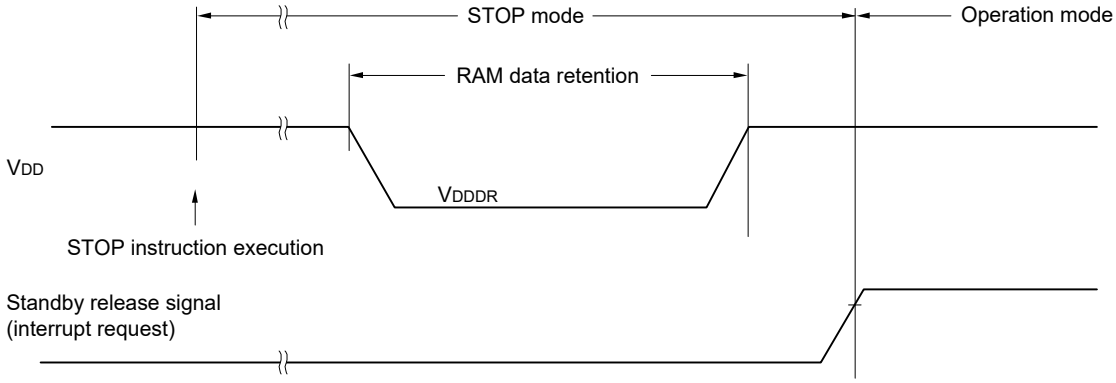
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 Voltage detection threshold	VR2LVD	3.3 V setting	2.85	2.90	2.95	V
	VR2LVD5	5.0 V setting	4.55	4.60	4.65	V

4.9 RAM Data Retention Characteristics

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



4.10 Flash Memory Programming Characteristics

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1		32	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retained years are until next rewrite completion.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4.11 Dedicated Flash Memory Programmer Communication (UART)

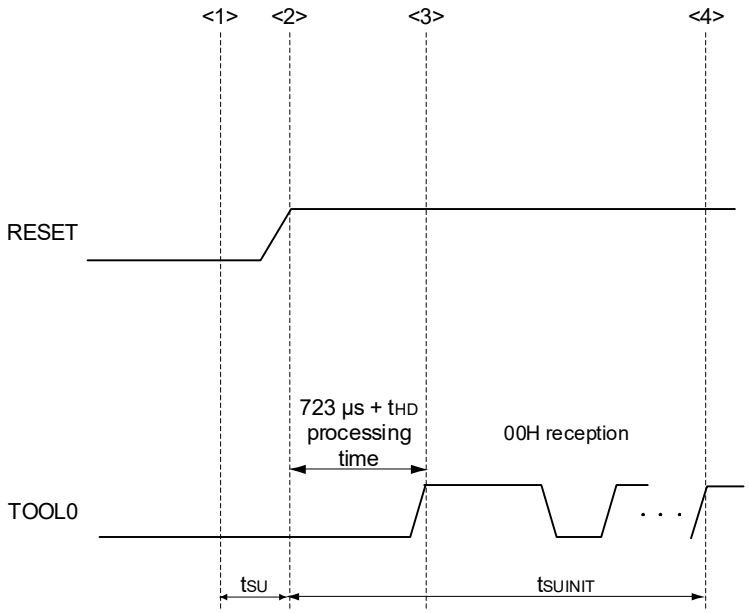
(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.12 Timing of Entry to Flash Memory Programming Modes

(T_A = -40/-20 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
The time needed when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
The time needed from when the TOOL0 pin is placed at low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			us
The time needed for the TOOL0 pin must be kept at low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tSUINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tSU: Time needed for the TOOL0 pin is placed at low level until the pin reset ends

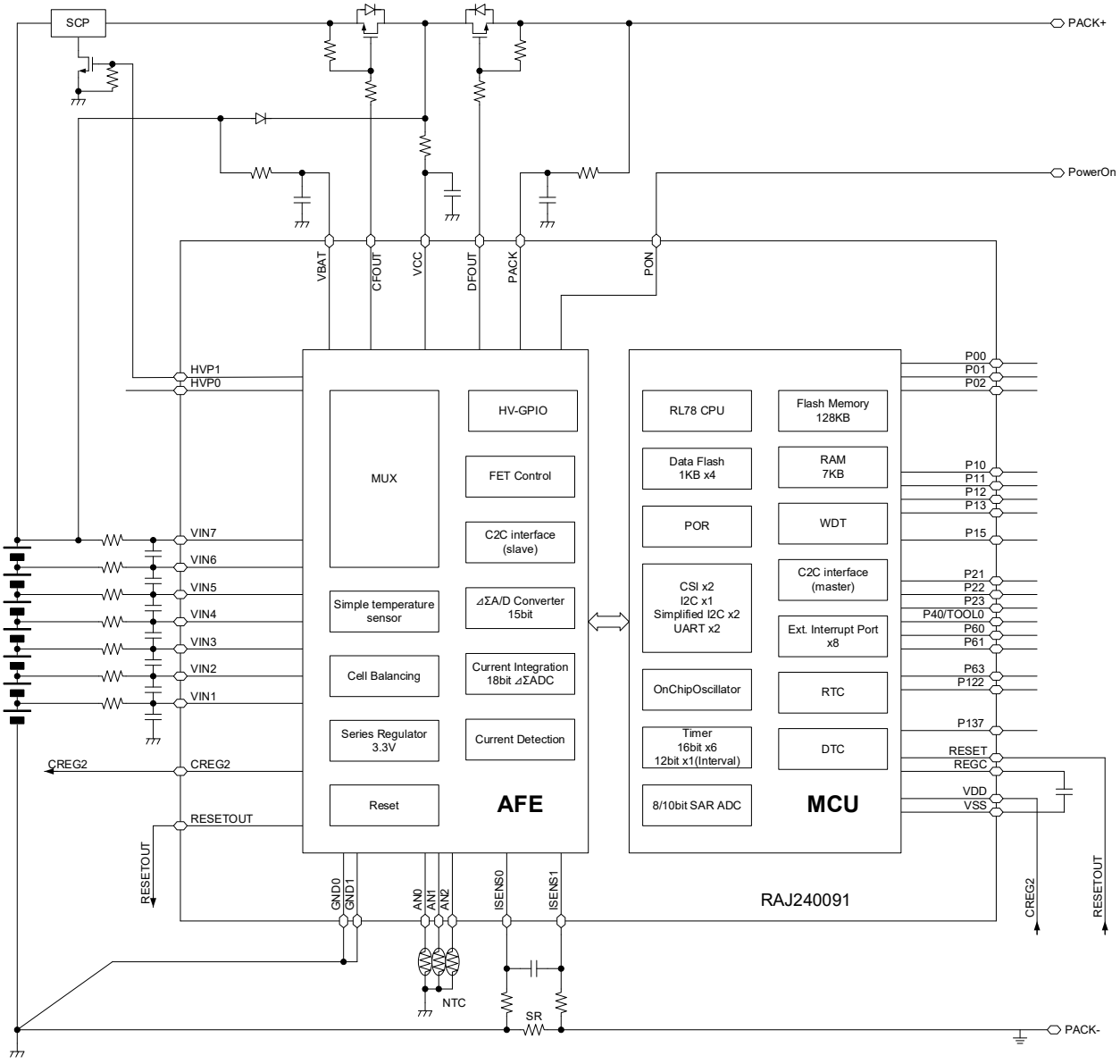
tHD: Time needed for the TOOL0 pin at low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

5. DETAILED DESCRIPTION

5.1 Overview

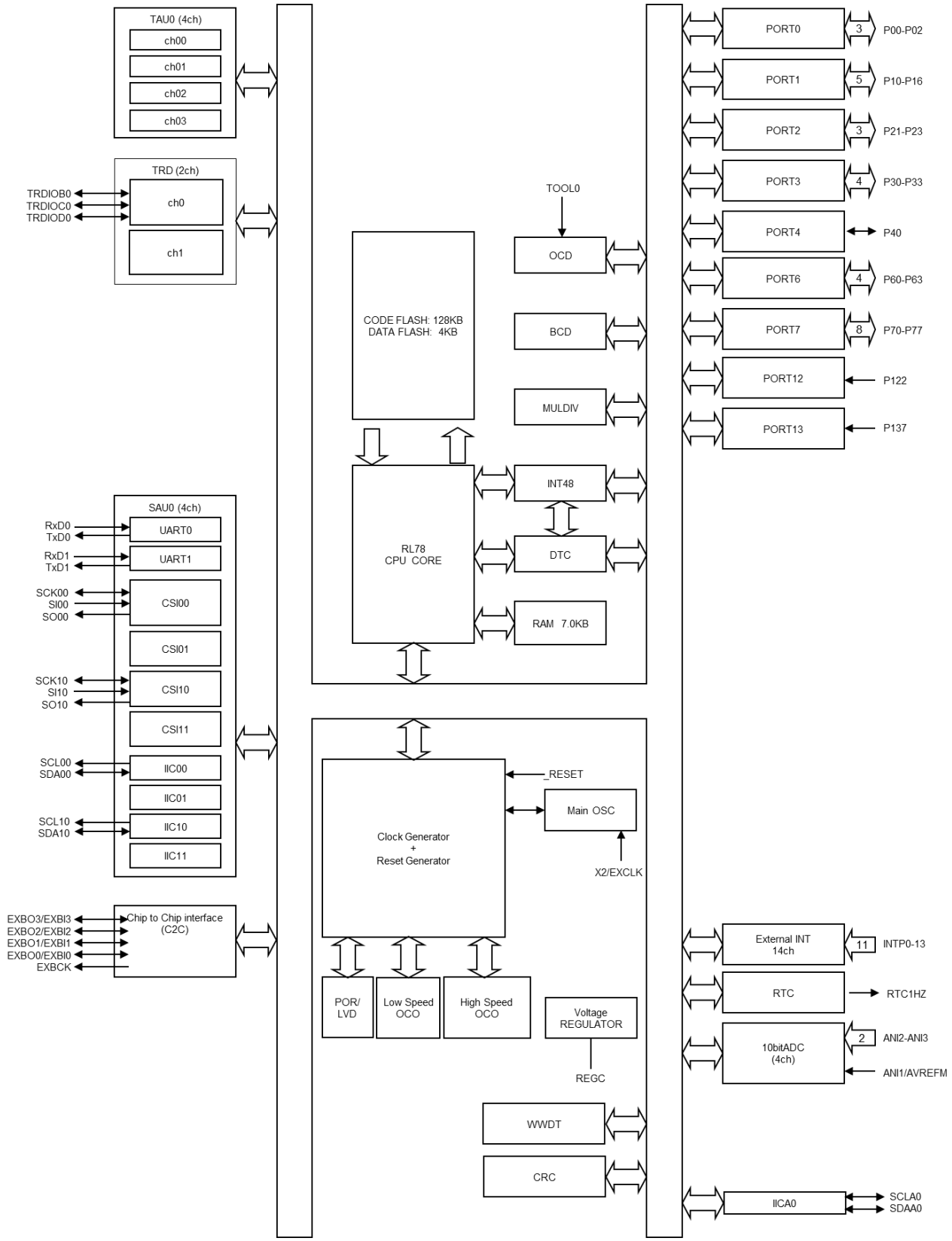
RAJ240091 is Renesas fuel gauge ICs which consist of a MCU block and an AFE block in a single package and accomplish various protection mechanisms. These IC's incorporates advanced battery management features such as primary and secondary protection, voltage and current measurement, current integration, host communication interface. By using the battery management controlled firmware and data are stored in the embedded flash memory to control the embedded analog and digital hardware circuits, optimum battery management operation including high accuracy remaining capacity estimation and battery safety can be achieved.

5.2 System block diagram



Caution The example peripheral circuit does not guarantee proper operation. Please perform sufficient evaluation using the actual application to determine the circuits and peripherals.

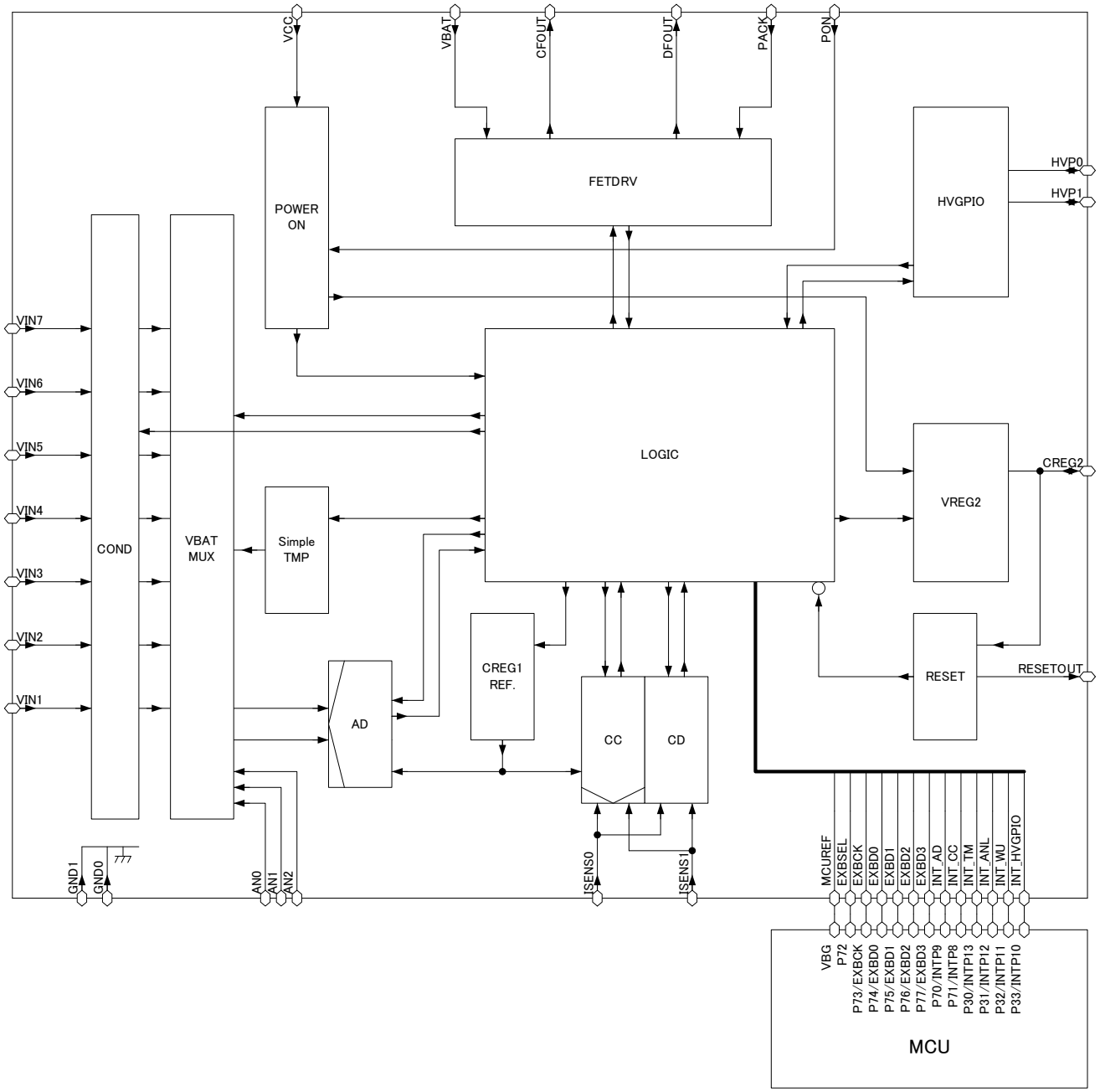
5.3 MCU block diagram



Caution 1. P30, P31, P32, P33, P70, P72, P73, P74, P75, P76 and P77 are connected to the internal AFE chip and not connected to the package external pins.

Caution 2. Each interrupt request of AFE is assigned to P30/INTP13, P31/INTP12, P32/INTP11, P33/INTP10, P70/INTP9 and P71/INTP8.

5.4 AFE block diagram



6. APPLICATION GUIDELINE

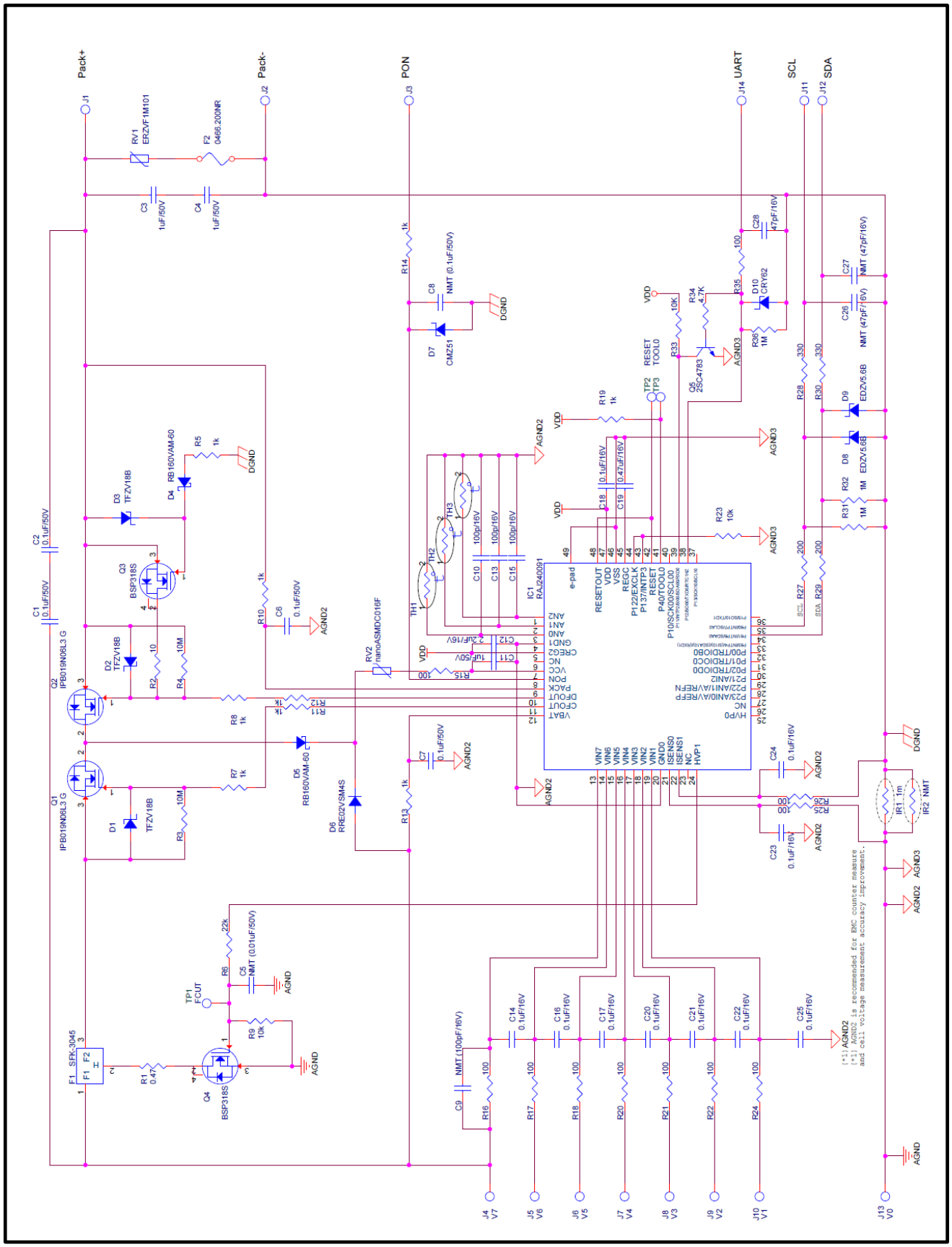
6.1 Typical Application Specification

A typical specification example of Li-ion battery management unit as shown below.

From the next page, the typical application guideline is explained for RAJ240091.

Battery cell assembly	7S1P	
Host Interface	System Management Bus (SMBus) Specification, version 1.1.	
	UART	
Primary protection	Charge FET and Discharge FET	
Secondary protection	Fuse blow by FGIC or a secondary protection device.	
Connect pins	Pack+	Positive battery pack terminal
	SMC	SMBus clock
	SMD	SMBus data
	UART	UART communication port
	Pack-	Negative battery pack terminal
Additional Features	External reverse charge protection circuit	
	Battery and charge/discharge MOSFET temperature measurement with three thermistors	

6.2 Typical Application Circuit

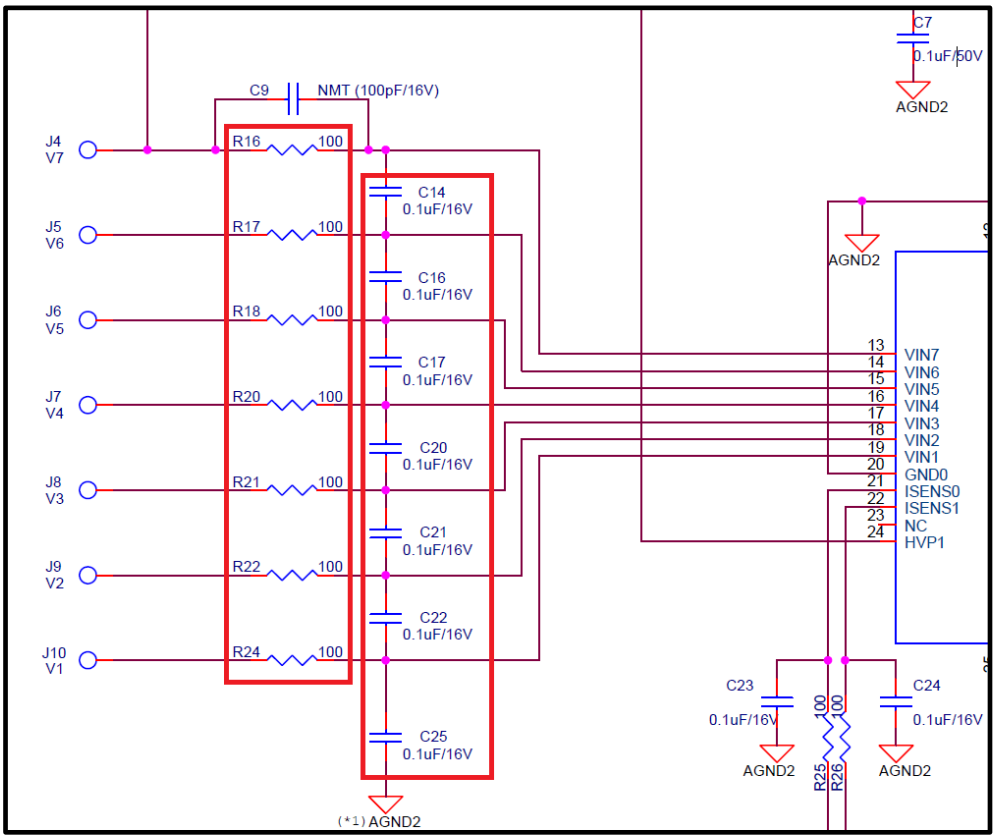


6.3 Circuit Design Guideline

6.3.1 Cell voltage monitor circuit

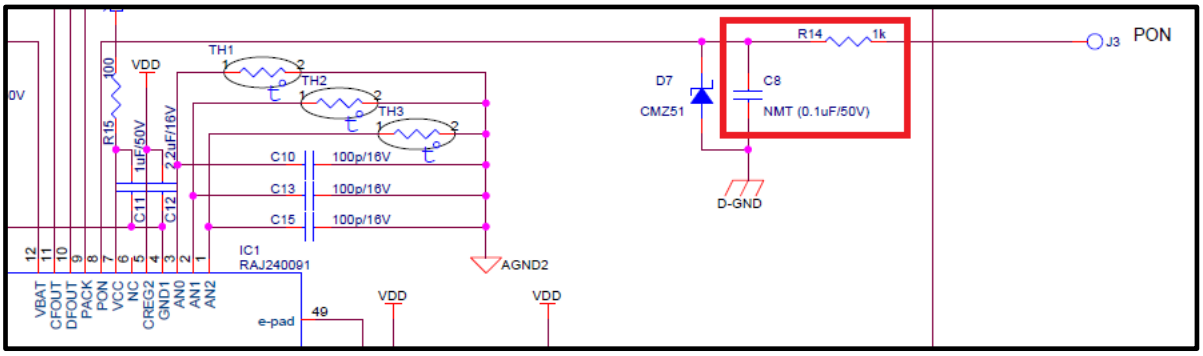
- Place an input filter between FGIC's VIN pins and each of the cells.
- Place resistors valued 100 Ω and capacitors valued 0.1 uF to VIN1 – VIN7 pins for surge protection.

  It is necessary to calculate the cut-off frequency and use correct resistance and capacitance value based on application.



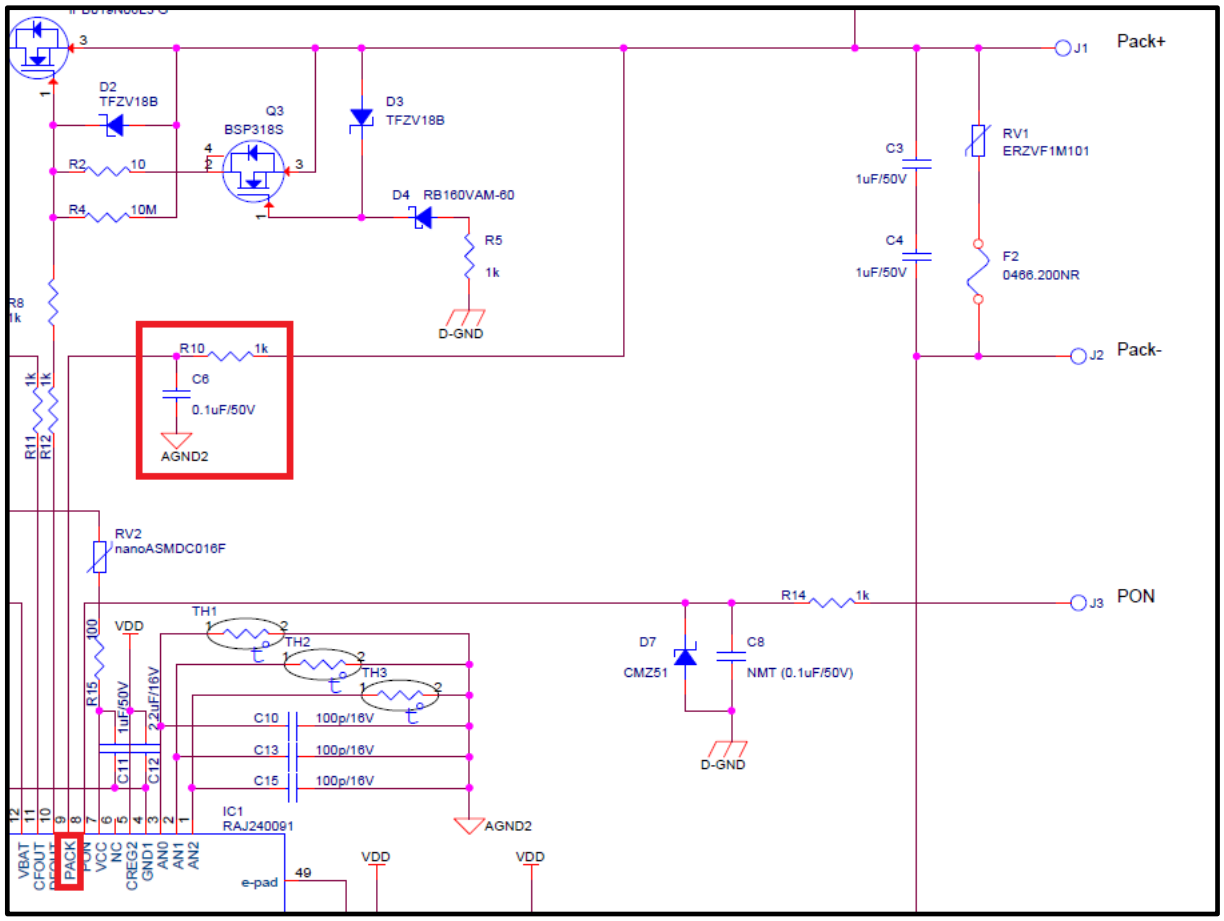
6.3.2 Battery power on circuit

Place resistors value around 2 kΩ (1 kΩ+1 kΩ), capacitor 0.1 uF and Zener diode to PON for surge protection. It is necessary to calculate cut-off frequency and use correct resistance and capacitance value based on application.



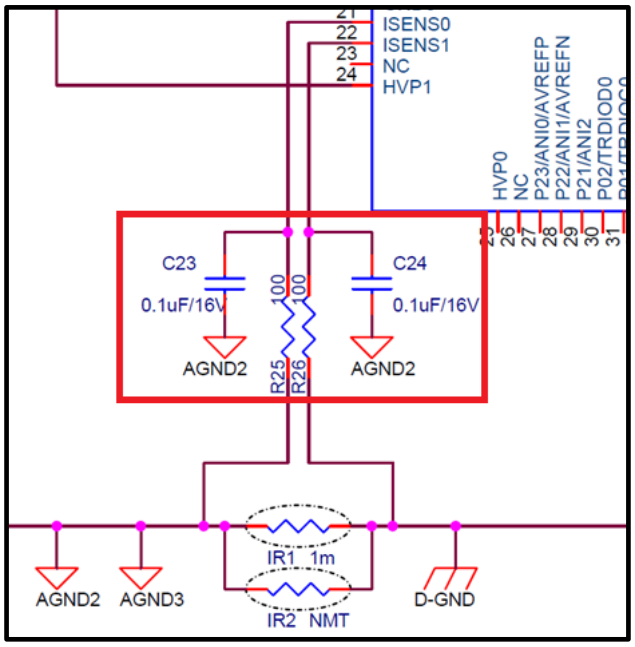
6.3.3 PACK port

- PACK port is source voltage of DFOUT (D-FET gate control signal). R10 plays a role in limiting the current limit when charger is reverse-charged. 1 kΩ is recommended, if it is too large, the D-FET turn off speed will become too slow.
- C6 helps to provide stable D-FET boost operation. 0.1 uF is recommended. If any problems occur in short circuit protection or ESD etc., adjust the value of C6.



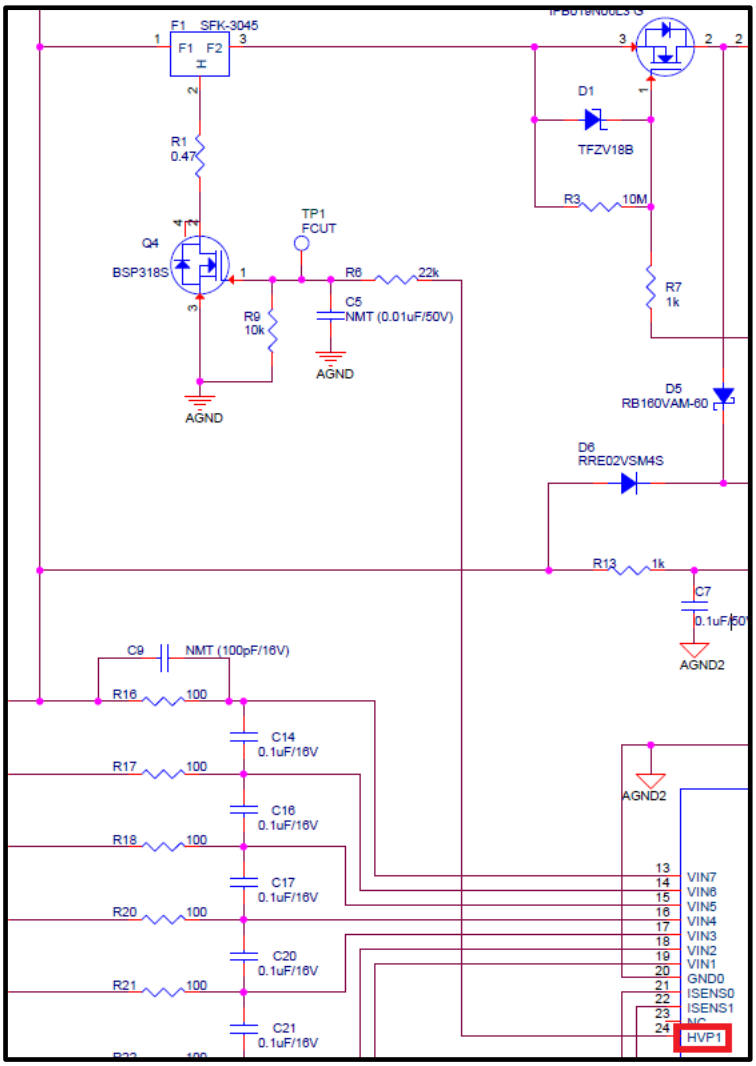
6.3.4 Current monitor

- Potential difference on the sense resistor is monitored by current integrating circuit.
- Place a Low Pass Filter (100 Ω, 0.1 uF) at input stage.
- Sense lines should be shielded if small voltage difference is detected to ensure high accurate current sensing.



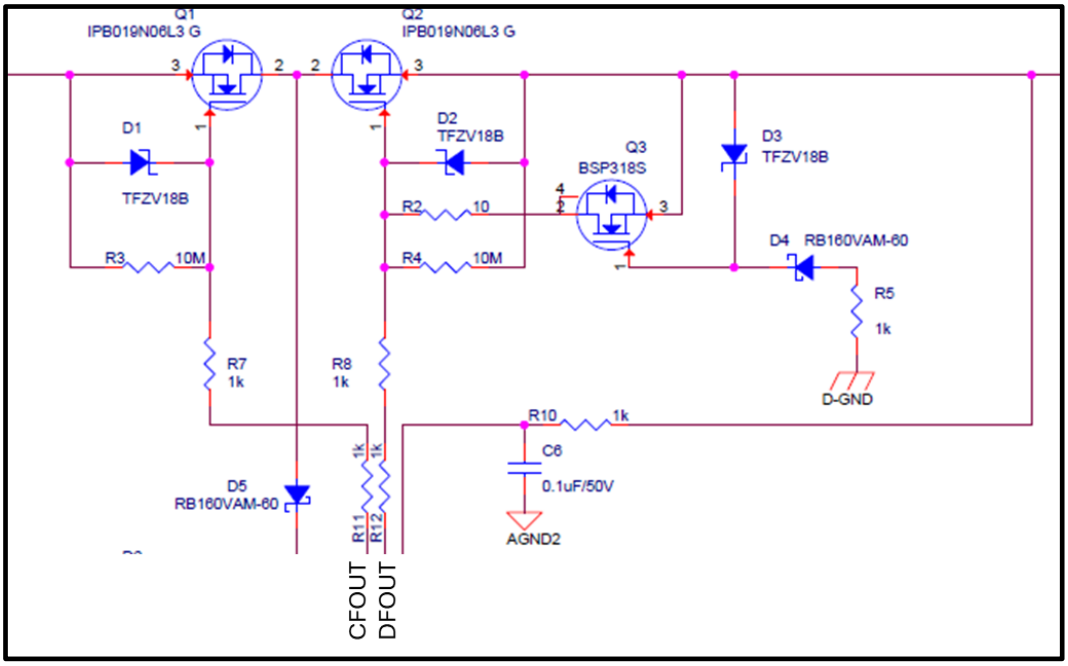
6.3.5 Fuse control

- Self-control protector (SCP) is used for fuse in reference circuit.
- The fuse will blow when RAJ240091 drives HVP1 (High voltage GPIO) pin high to make Q4 ON.
- The fuse will blow when overcurrent exceeds the limit of SCP.
- R1 are used for battery electrochemical migration short circuit countermeasures.



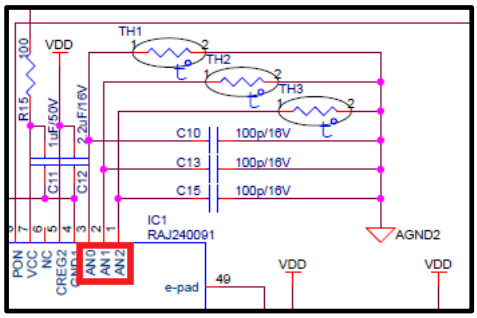
6.3.6 C-FET and D-FET control

- Q3 is located between gate and source of Q2 to make D-FET turn off when charger is reverse connected.
- R5 is for Q3 gate protection. (1 kΩ is recommended.)
- R8, R12 and R7, R11 are use as gate protection and C-FET/D-FET noise reduction. (1 kΩ each is recommended.)
- R3 and R4 are used to fix C-FET/D-FET gate voltage in order to keep stable off state when FET is turn off.
  10 MΩ is recommended to prevent voltage drop.



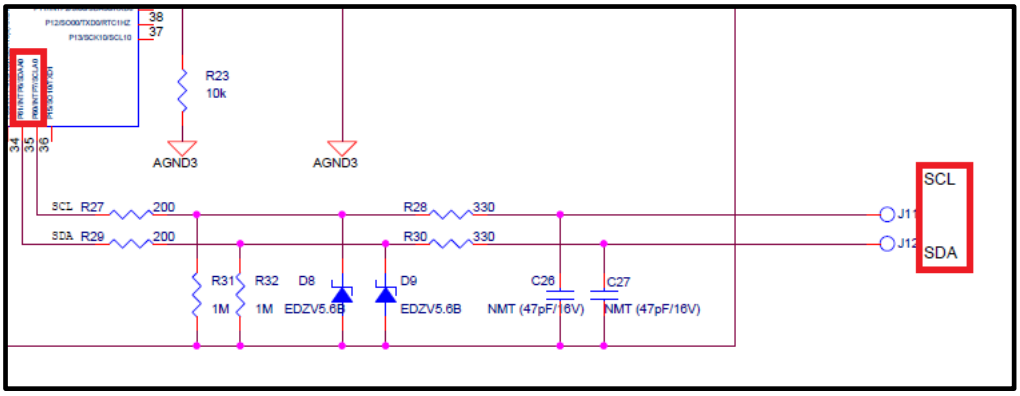
6.3.7 Thermistor

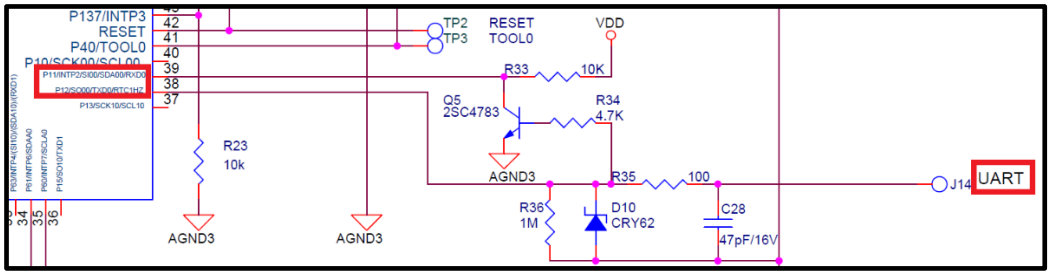
- ADC voltage measurement pins (AN0, AN1, AN2) are assigned for thermistor. To prevent EMC noise issue, an additional 100 pF capacitor is recommended.



6.3.8 Communication line

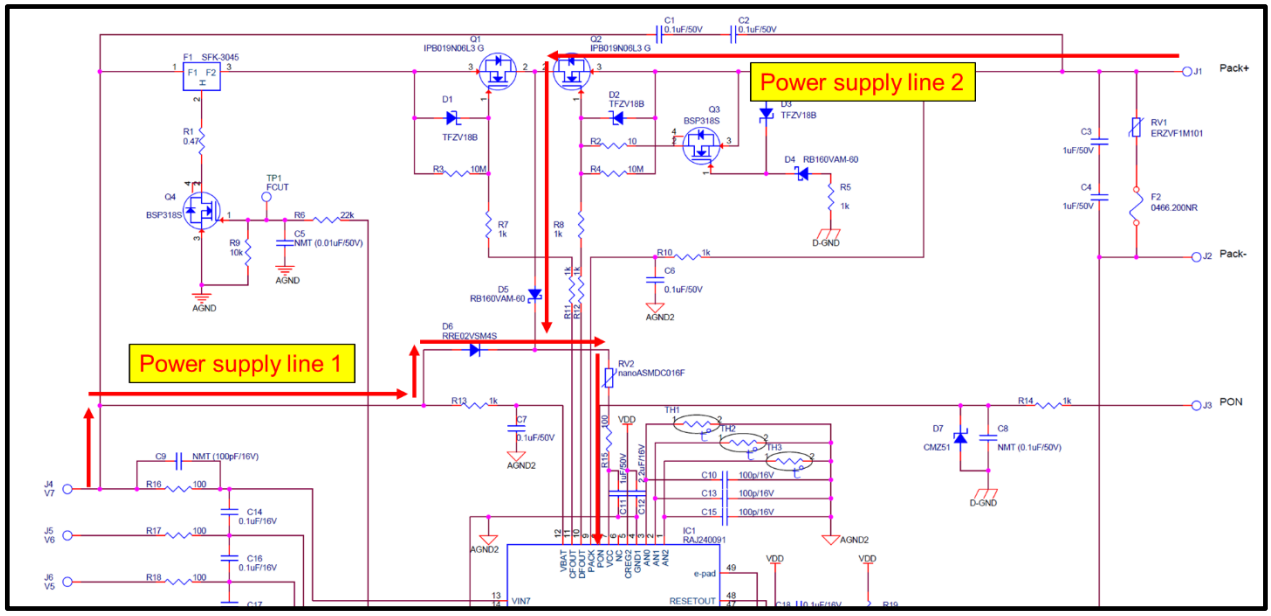
- RAJ240091 supports 2 kinds of communication, SMBus and UART.
- For electrical over stress countermeasure, input 200 Ω, 330 Ω resistance, Zener diode and capacitance (NMT) are recommended in SMBus communication line.
- For UART communication, it is necessary to add the circuit with appropriate protection by user's UART protocol. RXD/TXD line pull up voltage should be the same as VDD.

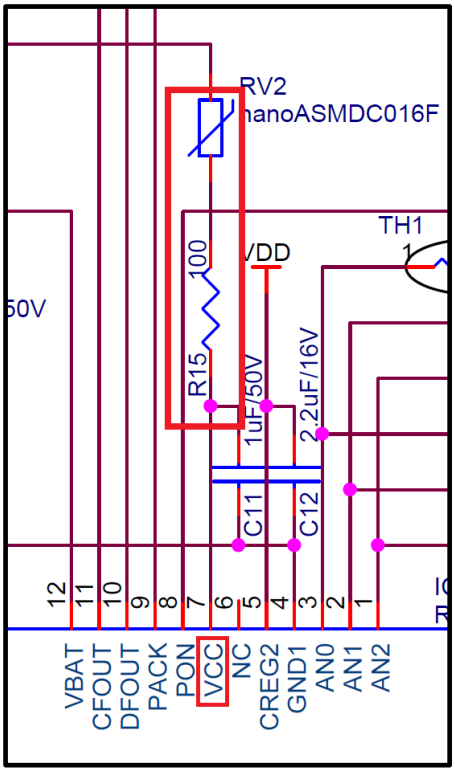




6.3.9 Power supply path

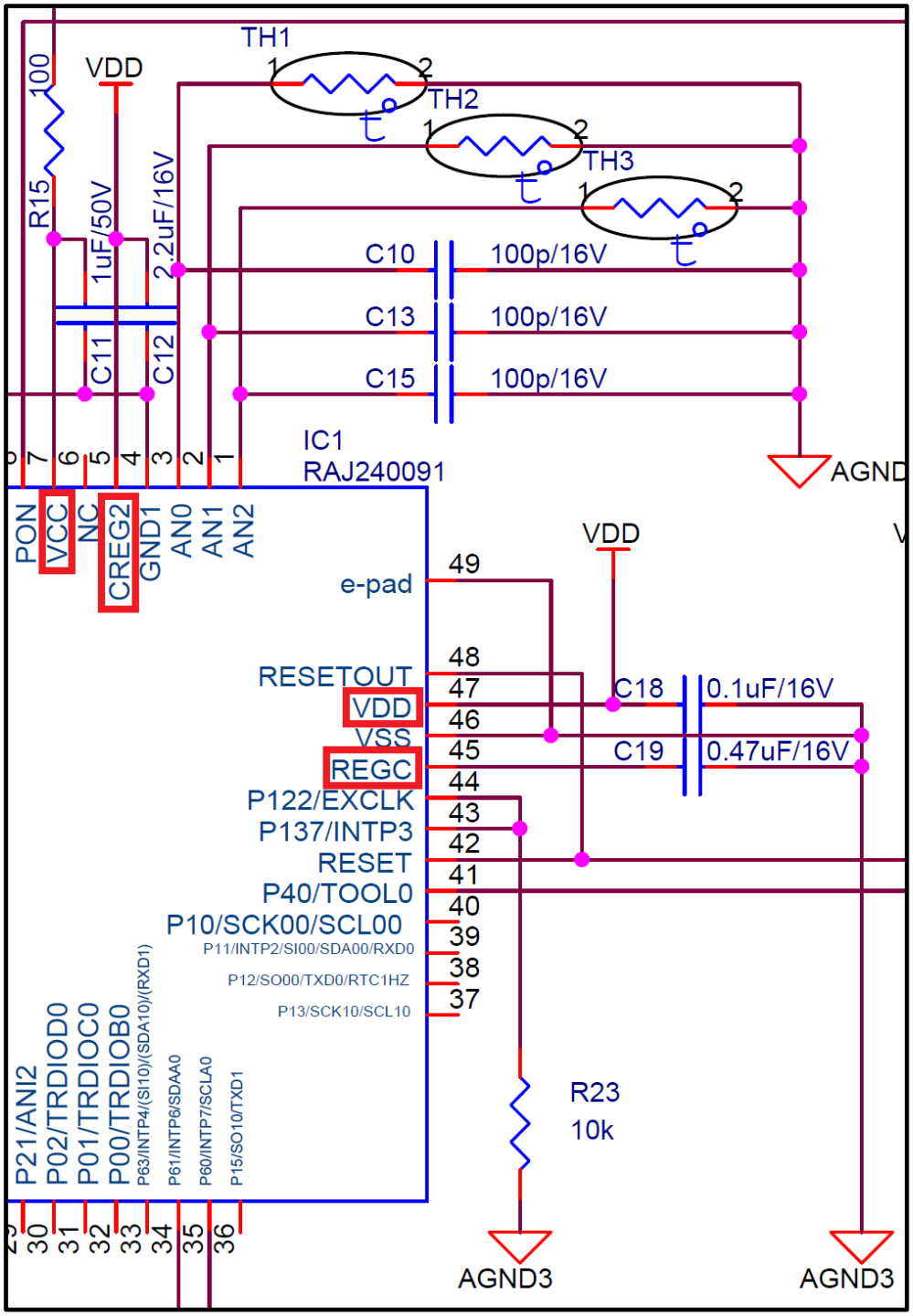
- Power is supplied to VCC through the following two paths depending on circumstance.
- Power is supplied from battery side when Pack+/- is not connected to a charger or the fuse is blown.
  See power supply line 1.
- Higher output voltage from battery and charger is used as power supply. See power supply line 2.
- For protection of the VCC pin, it is recommended to add resistor 100 Ω and PTC for current limit.





6.3.10 VCC, CREG2, VDD and REGC capacitance

- The following decoupling capacitors must be located adjacent to each terminal.
- C11: VCC (1.0 uF is recommended.)
- C12: CREG2 (1.0 to 4.7 uF is recommended.)
- C18: VDD (0.1 uF is recommended.)
- C19: REGC (0.47 to 1.0 uF is recommended.)



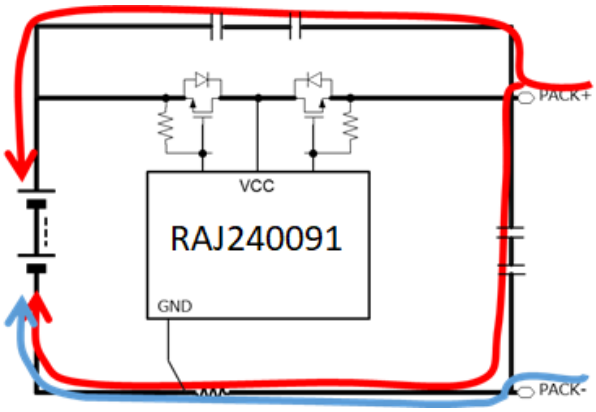
6.4 Layout Guidelines

6.4.1 Summary

- Large current patterns must be wide and short to minimize voltage drop and heat generation.
- Bypass capacitors must be mounted as close as possible to the device VCC / VBAT and GND pins to prevent erroneous operation due to noise from power supply.
- Capacitors for voltage regulators must be located close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- RAJ240091 must be located away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.

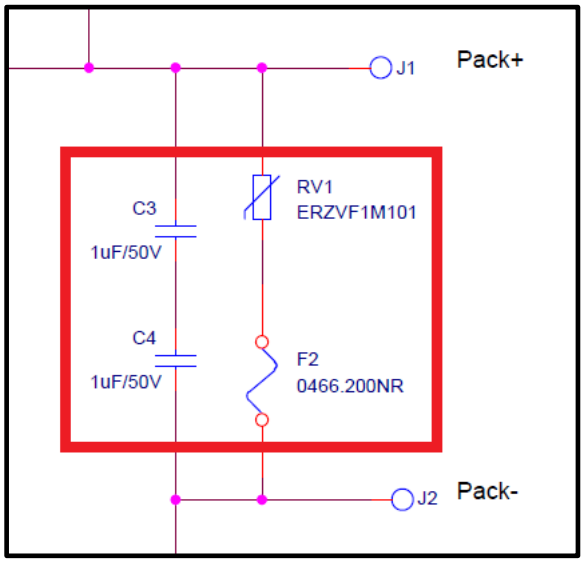
6.4.2 ESD protections on each terminal (basic policy)

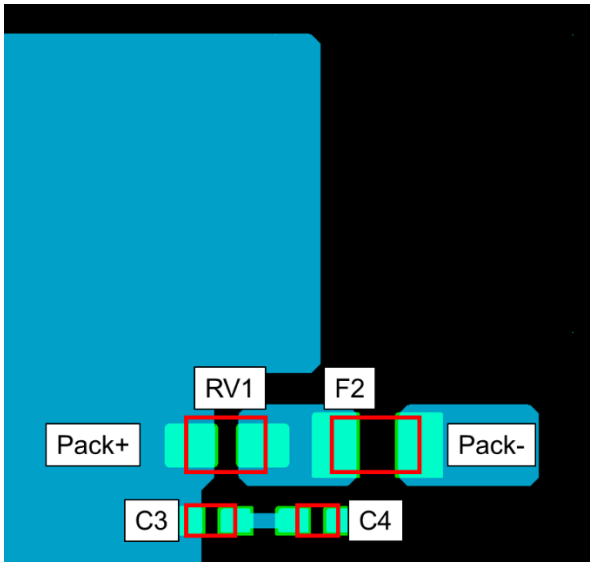
- ESD on Pack+ terminal must be discharged to the top side of the cell or to Pack- terminal through a capacitor.
- ESD on Pack- terminal must be discharged to the GND side of the cell.
- ESD on communication terminals and other GPIOs must be discharged to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- must be discharged to the battery cells so that it will not interfere with FGIC functions and measurements.



6.4.3 Pack+, Pack- (Noise protection element)

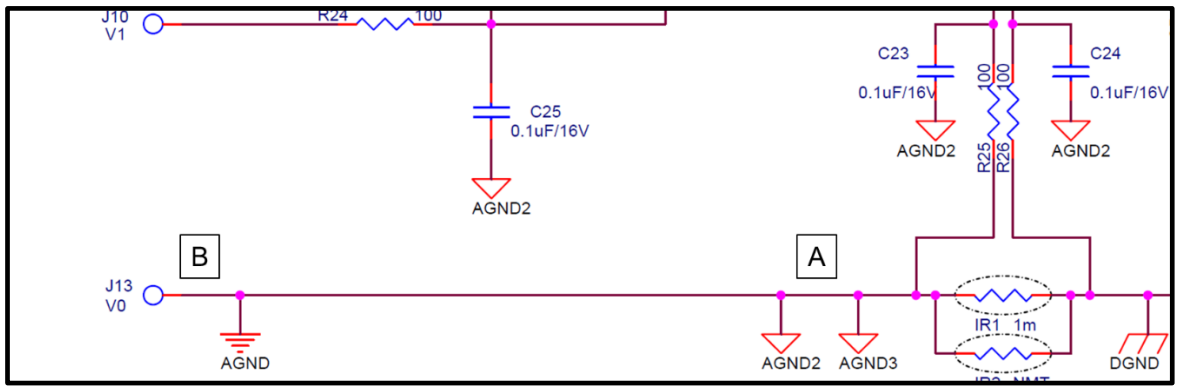
- A bypass capacitor must be placed between Pack+ and Pack-. (Countermeasure against ESD)
- A bypass capacitor must be located adjacent to Pack+, Pack-. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don’t use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)
- For the terminal protection against noise and overvoltage, it is recommended that it carries varistor or TVS diode.(RV3)
- It is recommended to add Fuse to prevent short circuit. (F2)
- C3, C4, RV1, F2 must be placed as short as possible between PACK + and PACK-.
  However, be careful not to narrow the distance between Pack + and Pack-.

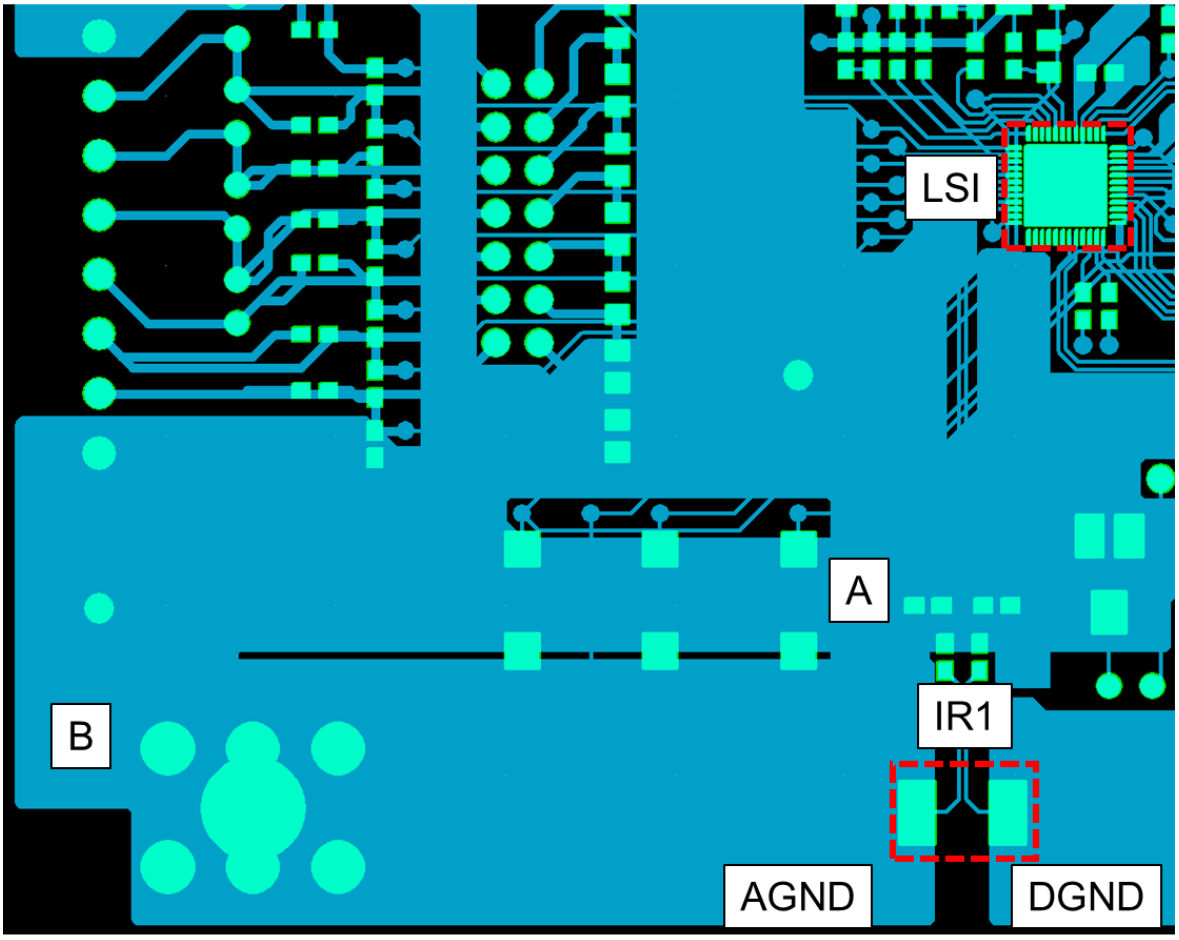




6.4.4 GND connection

- Each analog GND of FGIC should be connected to the point (A) of current detection resistor of the cell side by the pattern with an adequate width. (Prevent potential variation by large current.)
- VIN0 should be connected near point V0 (B).
- The patterns between AGND, AGND2 and AGND3 must not be divided.
  Keeping the GND potential of MCU and AFE equal.
- Exposed pad should be connected to GND0 and GND1.





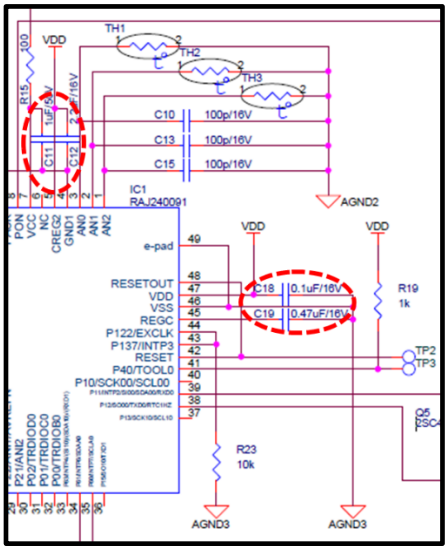
6.4.5 Bypass capacitor between VCC/VDD/CREG2S/REGC and GND1/VSS

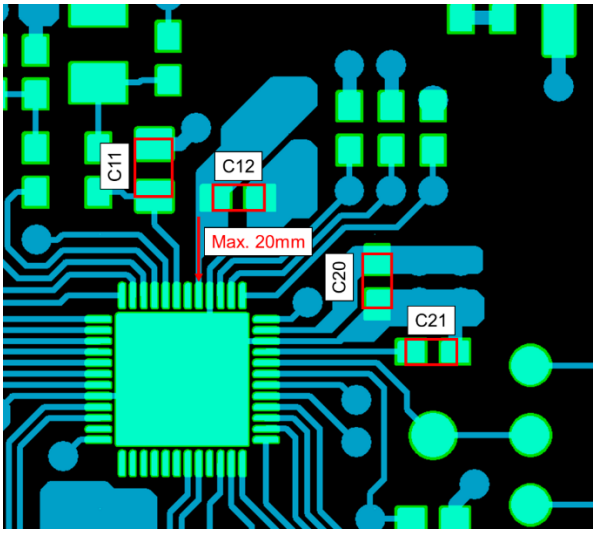
- The patterns between VCC/CREG2S pin and GND1 pin, and VDD/REGC pin and VSS pin, a bypass capacitor is connected and the path must be as short as possible. (Countermeasure for ESD)

  The FGIC and bypass capacitor must be placed on the same side of the PCB without through-holes and the maximum loop length must be about 20 mm.

- The lines to bypass capacitor must be wide and short.

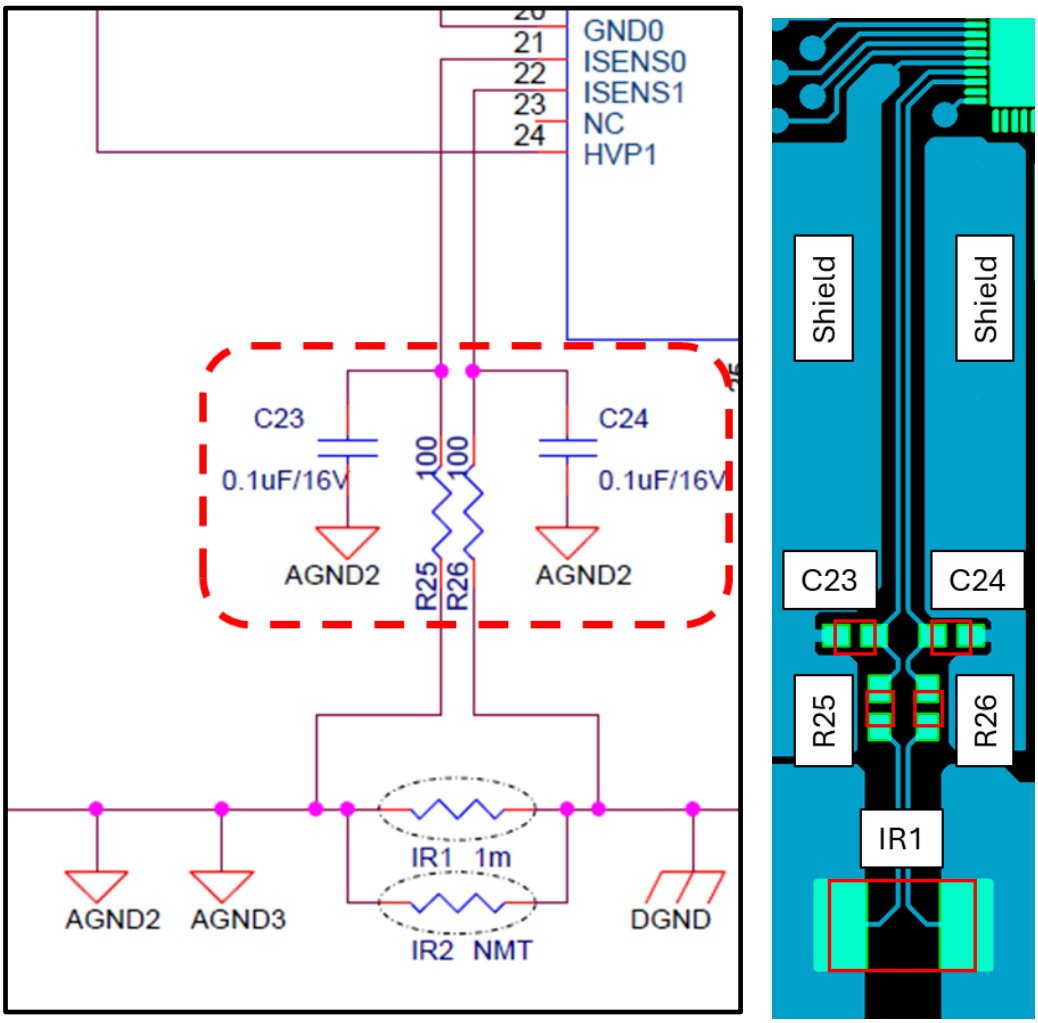
  To keep bypass capacitor effective in suppressing the potential variation.





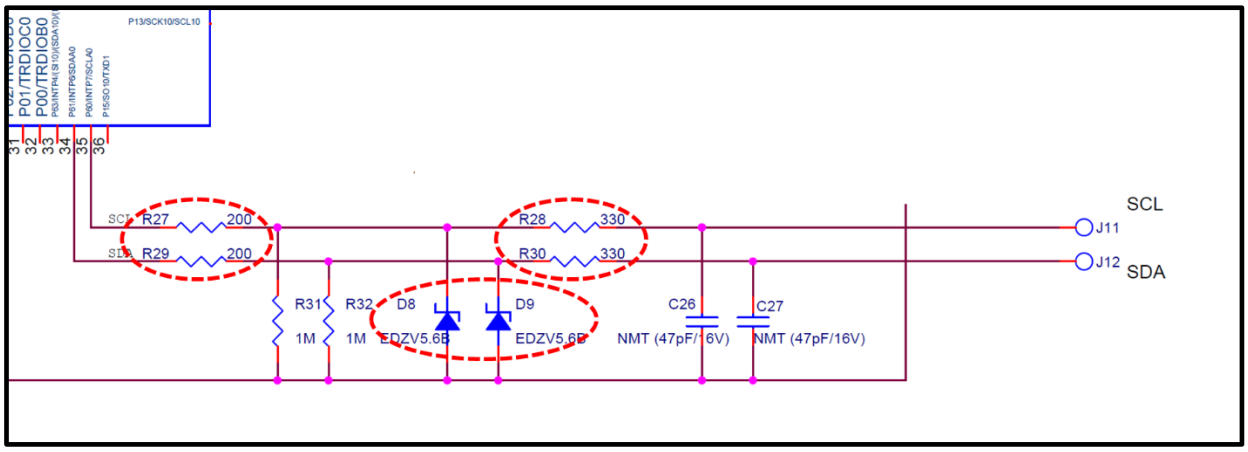
6.4.6 Current Monitor (ISENS0, ISENS1)

- Two lines from current sense resistor to ISENS0, ISENS1 must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise)
- LPF (100 Ω and 0.1 uF) and a shield pattern should be placed to ISENS0/1 lines. (Countermeasure against noise)
- Minimizing wire length and its number of branches between current sense resistors and ISENS0/ISENS1 pins to suppress incoming noise from unnecessary pattern.



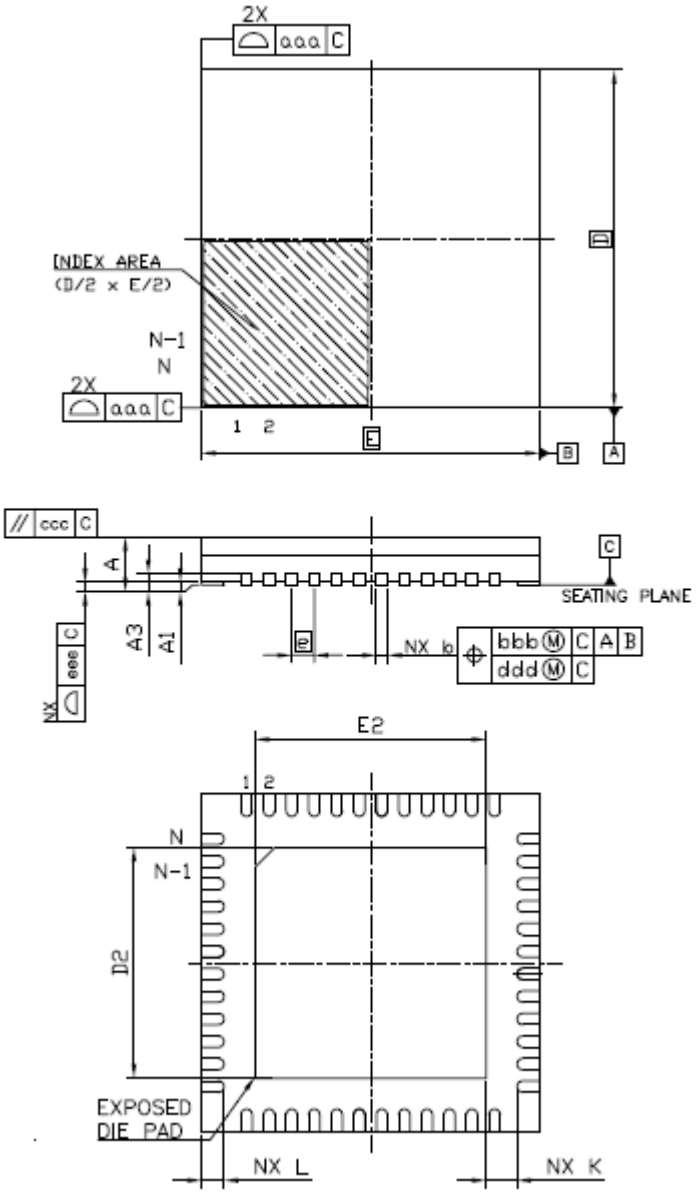
6.4.7 Communication line (SMBus)

- SMBus lines must be equipped with Zener diodes. And it is necessary to mount resistors on the side of FGIC and pack connector. Zener diode and the resistor on the side of connector are for surge countermeasures, the resistor on the side of FGIC for noise countermeasure.
- The resistor on the side of the FGIC must be located as close to the FGIC as possible.



7. PACKAGE DRAWINGS

JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-HVQFN48-6×6-0.40	PVQN0048LG-A	0.11



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	-	-	1.00
A1	0.00	-	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D	-	6.00	-
E	-	6.00	-
e	-	0.40	-
N		48	
L	0.30	0.40	0.50
K	0.20	-	-
D2	4.00	4.10	4.20
E2	4.00	4.10	4.20
aaa	-	-	0.10
bbb	-	-	0.10
ccc	-	-	0.10
ddd	-	-	0.50
eee	-	-	0.08

REVISION HISTORY

Rev.	Date	Page	Description
1.00	Mar. 31, 2025		First release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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