

## CHAPTER 1. INTRODUCTION

### 1.1 Features

- **Fully integrated battery management solution with battery capacity measurement and programmable protection capability.**
- **Supports up to 7 Li-ion or Li-Polymer battery cells in series.**
- **Supports various self-diagnosis functions for functional safety.**
- **Integrated with Renesas Ultra Low Power RL78 CPU core for multi-function process.**
- **Memory**  
Code flash memory: 64 KB  
Data flash memory (up to 100,000 erase/write cycles): 4 KB  
SRAM: 5.5 KB
- **Clock generator**  
High speed on-chip oscillator: up to 32 MHz  
Low speed on-chip oscillator: 15 kHz  
AFE high speed on-chip oscillator: 4.194 MHz  
AFE low speed on-chip oscillator: 131.072 kHz
- **General Purpose I/O Ports**  
Total: 21 pins  
CMOS input/output: 15, CMOS input: 2  
N-ch open drain input/output [6 V tolerance]: 2  
High voltage N-ch open-drain input/output [50 V tolerance]: 2
- **Serial interface**  
CSI (SPI): 1 channel, UART: 2 channels  
Simplified I2C: 1 channel, I2C: 1 channel
- **Timer**  
MCU 16-bit timer: 6 channels  
MCU 12-bit interval timer: 1 channel  
AFE timer: 2 channels
  - AFE timer A: setting range: 125 ms to 64 s
  - AFE timer B: setting range : 30.52 us to 125 ms
- **Embedded A/D converter**  
AFE 15-bit resolution sigma-delta A/D converter  
MCU 8/10-bit resolution A/D converter
- **Current integration circuit**  
18-bit resolution sigma-delta A/D converter
- **Battery cell voltage, Internal voltage and temperature (AN port voltage) detection circuit**  
Monitoring over/under voltage and temperature by Sigma-delta AD converter (AFE) without controlling from MCU.
- **Impedance measurement circuit**  
Simultaneous measurement of battery voltage and current
- **Over current detection circuit**  
Short circuit current detection  
Charge overcurrent detection  
Discharge overcurrent detection (Up to 4 detection condition)  
Charge wakeup current detection  
Discharge wakeup current detection
- **Series regulator**  
3.3 V output (> 20 mA)
- **Charge and Discharge MOSFET control**  
Supports Low side Nch MOSFET drive
- **Ultra Low power consumption**  
Power down mode: 1 uA  
Sleep mode1 current: 25 uA (DFET and CFET off)  
Sleep mode2 current: 40 uA (DFET and CFET on)  
In Sleep mode2, enable All H/W protection function
- **Additional features**  
Internal Cell Balancing Circuit (On-resistance100ohm typ.)  
Internal Watchdog Timer (MCU)  
MCU Runaway Detection Circuit (AFE)  
3 Thermistor Sensor Ports with On-chip Pull-up Resistors  
Random cell connection tolerant
- **Voltage and temperature condition**  
Power supply voltage: VCC = 4.0 to 40 V  
Operating ambient temperature T<sub>A</sub> = -40 to +85°C
- **Package Information**  
48 pin plastic mold LQFP  
([Body] 7.0 mm x 7.0 mm, 0.5 mm pitch)

### 1.2 Applications

- Vacuum cleaner, Handheld equipment, Power Tool, E-bike, UPS, Power bank

### 1.3 Description

RAJ240301 is a Renesas battery fuel gauge and management device which combines a separate MCU and AFE blocks in a single package to accomplish various battery protection and management functions. This device incorporates advanced battery management features such as primary and secondary protection, voltage and current measurement, current integration, and host communication interface. Through user programmable control firmware and configuration data stored in the onboard MCU's embedded flash memory, the embedded analog and digital hardware circuits offer optimum battery management operations including high accuracy remaining capacity estimation and battery safety.

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## CHAPTER 2. OUTLINE

## 2.1 Outline of Functions

(1/2)

Item		Description
Code flash memory		64 kB
Data Flash memory		4 kB
RAM		5.5 kB
Address size		1 MB
Main system clock	High speed on-chip Oscillator clock( $f_{IH}$ )	HS (high-speed main) mode: 1 to 32 MHz LS (low-speed main) mode: 1 to 8 MHz,
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.03125 usec (Internal high-speed oscillation clock: $f_{IH}$ = 32 MHz)
Instruction set		<ul style="list-style-type: none"> <li>• Data transmission (8/16 bits)</li> <li>• Addition and subtraction/logical operations (8/16 bits)</li> <li>• Multiplication (8×8 bits, 16×16 bits), Division (16÷16 bits, 32÷32 bits)</li> <li>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)</li> <li>• Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.</li> </ul>
I/O Port	CMOS I/O	15
	CMOS input	2
	N-ch open-drain I/O [6V tolerance]	2
	High voltage N-ch open-drain I/O	2
Timer	16-bit timer	6 channels (TAU: 4 channels, Timer RD : 2 channels)
	Watchdog timer	1 channel
	Real-time clock (RTC) <sup>Note 1</sup>	1 channel
	12-bit interval timer	1 channel
	Timer output	Timer outputs: 7 channels PWM outputs: 6 channels
8/10-bit resolution A/D converter		4 channels
Serial interface		<ul style="list-style-type: none"> <li>• CSI: 1 channel/UART: 1 channel</li> <li>• CSI: 1 channel/UART: 1 channel/Simplified I2C: 1 channel</li> </ul>
	I <sup>2</sup> C bus	1 channel
Vector interrupt source	Internal	20
	External	11 (6 sources are connected to AFE in the chip)
Reset		<ul style="list-style-type: none"> <li>• Reset by RESET pin (reset circuit output of AFE connected to RESETOUT)</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by illegal instruction execution <sup>Note 2</sup></li> <li>• internal reset by RAM parity error</li> <li>• internal reset by illegal memory access</li> </ul>
On-chip debug function		Support

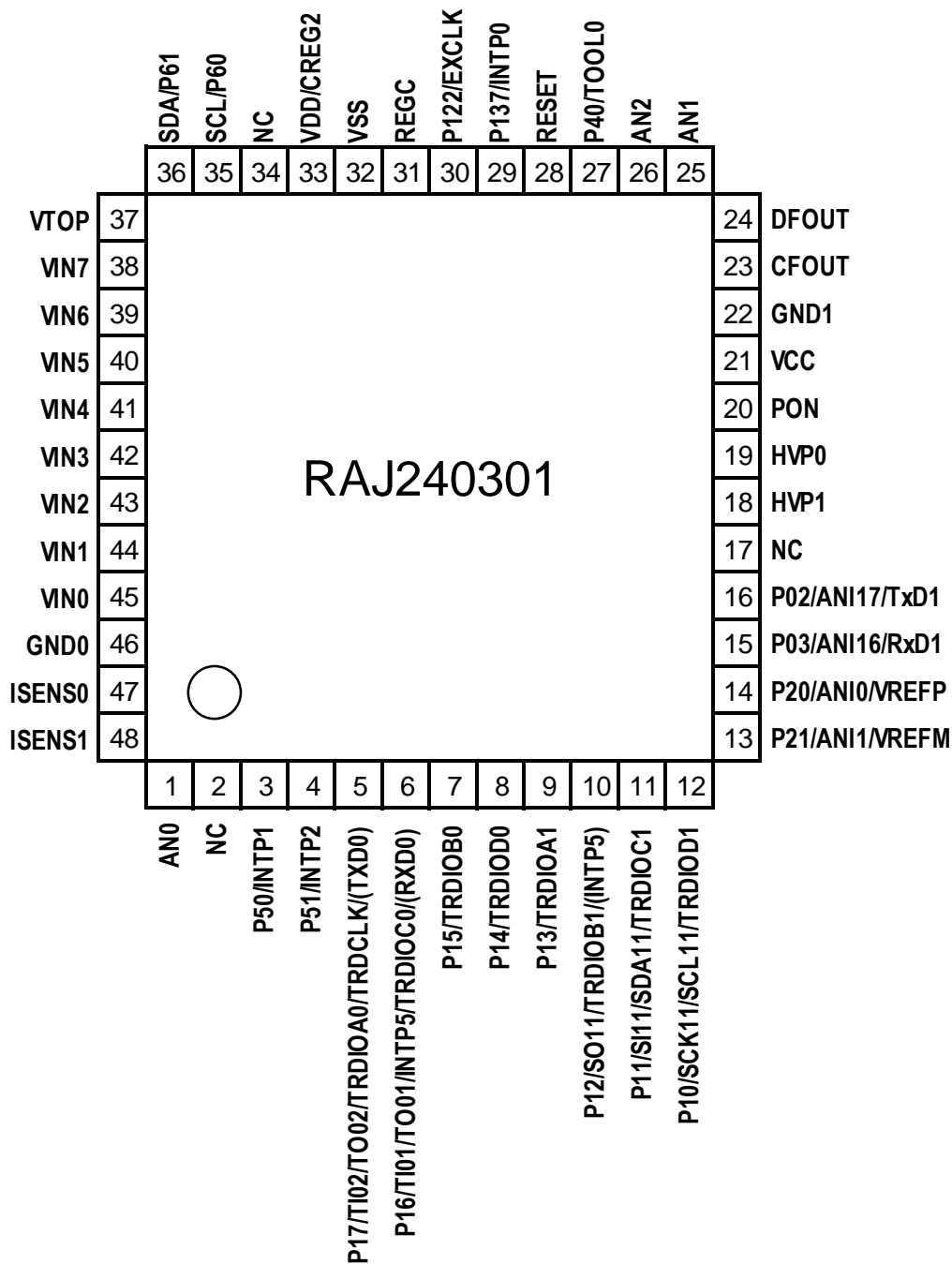
**Note 1.** This product has the constant-period interrupt function only, because these products have no subsystem clock.

**Note 2.** The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Item	Description
Sigma-delta A/D converter	15-bit resolution (sigma-delta method) <ul style="list-style-type: none"> <li>• Battery Cell voltage (Cell 1 to Cell 7)</li> <li>• Battery Cell total voltage (VTOP pin)</li> <li>• PON pin input voltage</li> <li>• Thermistor sensor port with on-chip pull-up 10 K<math>\Omega</math> resistor: 3 channels</li> <li>• On-chip simple temperature sensor (temperature range: -40 to 85°C)</li> <li>• Internal reference and supply voltage (AFE)</li> </ul>
Battery cell voltage and temperature (AN port voltage) detection circuit	Battery Cell voltage detection <ul style="list-style-type: none"> <li>• Over voltage (Overcharge voltage)</li> <li>• Under voltage (Overdischarge voltage)</li> </ul> Temperature (AN port voltage) detection <ul style="list-style-type: none"> <li>• Over temperature</li> <li>• Under temperature</li> </ul>
Current integrating circuit	1 channel:18-bit resolution
Current integrating circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wake up current detection circuit	<ul style="list-style-type: none"> <li>• Discharge short-circuit current detection</li> <li>• Discharge overcurrent detection</li> <li>• Charge overcurrent detection</li> <li>• Wake up current detection (discharge and charge)</li> </ul>
Simple temperature sensor	1 channel
Charge/Discharge Low side FET control circuit	N-ch MOSFET driver for charge control N-ch MOSFET driver for discharge control
Power on circuit	Return from power down mode by detecting high voltage input to PON pin
Series regulator	VREG2: power supply for MCU (3.3 V)
Reset circuit	Series regulator output monitoring (VREG2)
Cell balancing circuit	Support 7 series cells (On-resistor: 200 $\Omega$ MAX)
MCU runaway detection circuit	20 bits $\times$ 1(2 / 4 / 8 / 16 / 32 / 64 [s] to be selected)
AFE On-chip oscillator	4.194 MHz (TYP)
AFE low speed On-chip oscillator	131.072 kHz (TYP)
AFE timer	2 channels <ul style="list-style-type: none"> <li>• AFE timer A (setting range: 125 ms to 64 s)</li> <li>• AFE timer B (setting range: 30.52 us to 2 s)</li> </ul>
MCU-AFE communication interface(C2C)	AFE to MCU communication (Chip to Chip Interface)
Power supply voltage	VCC = 4.0 to 40 V
Operation ambient temperature	-40 to 85°C
Package	48 pin plastic mold LQFP([Body] 7.0 mm x 7.0 mm, 0.5 mm pitch, 1.4 mm thickness)

## 2.2 Pin Configuration (RAJ240301)

48 pin plastic mold LQFP ([Body] 7.0 mm x 7.0 mm, 0.5 mm pitch)



**Caution 1.** REGC pin connects to VSS pin through a capacitor (0.47 to 1.0 uF)

**Caution 2.** CREG2 pin connects to GND0/1 pin through a capacitor (1 uF to 4.7 uF).

**Remark 1.** Pin names refer to 3.1 Pin Identification.

**Remark 2.** The function shown above in ( ) is assigned by setting of peripheral I/O re-direction register 0 (PIOR0).

## CHAPTER 3. PIN FUNCTIONS

## 3.1 Pin Identification

(1/2)

No.	Name	Type	Description
1	AN0	AIN	Analog Input for Thermistor
2	NC	NC	No connect
3	P50/INTP1	DIO	Port5 / External Interrupt Input
4	P51/INTP2	DIO	Port5 / External Interrupt Input
5	P17/TI02/TO02/TRDIOA0/TRDCLK/ (TXD0)	DIO	Port1 / Timer Input / Timer Output / Timer Output / Timer External Clock input / UART Transmit Data
6	P16/TI01/TO01/INTP5/TRDIOC0/ (RXD0)	DIO	Port1 / Timer Input / Timer Output / External Interrupt Input / Timer Output / UART Receive Data
7	P15/TRDIOB0	DIO	Port1 / Timer output
8	P14/TRDIOD0	DIO	Port1 / Timer output
9	P13/TRDIOA1	DIO	Port1 / Timer output
10	P12/SO11/TRDIOB1/(INTP5)	DIO	Port1 / Serial Data Output / Timer output / External Interrupt Input
11	P11/SI11/SDA11/TRDIOC1	DIO	Port1 / Serial Data Input / Serial Data I/O / Timer output
12	P10/SCK11/SCL11/TRDIOD1	DIO	Port1 / Serial Clock I/O / Serial Clock I/O / Timer output
13	P21/ANI1/VREFM	DIO/AIN	Port2 / Analog Input / Analog Reference Voltage Minus
14	P20/ANI0/VREFP	DIO/AIN	Port2 / Analog Input / Analog Reference Voltage Plus
15	P03/ANI16/RxD1	DIO/AIN	Port0 / Analog Input / UART Receive Data
16	P02/ANI17/TxD1	DIO/AIN	Port0 / Analog Input / UART Transmit Data
17	NC	NC	No connect
18	HVP1	HVIO	High Voltage Port
19	HVP0	HVIO	High Voltage Port
20	PON	HVIN	High voltage Port for power on
21	VCC	P	Power supply
22	GND1	P	Ground
23	CFOUT	HVO	Charge MOSFET control
24	DFOUT	HVO	Discharge MOSFET control
25	AN1	AIN	Analog Input for Thermistor
26	AN2	AIN	Analog Input for Thermistor
27	P40/TOOL0	DIO	Port4 / Data Input/Output for Tool
28	RESET	DIN/DOUT	Reset Input for MCU / Reset Output for AFE
29	P137/INTP0	DIN	Port13 / External Interrupt Input
30	P122/EXCLK	DIN	Port12 / External Clock Input
31	REGC	P	Regulator Capacitance
32	VSS	P	Ground
33	VDD/CREG2	P	Power Supply for MCU / Regulator output

(2/2)

No.	Name	Type	Description
34	NC	NC	No connect
35	SCL/P60	DIO	I2C Bus clock I/O / Port6
36	SDA/P61	DIO	I2C Bus data I/O / Port6
37	VTOP	AIN	Battery voltage input
38	VIN7	AIN	Battery voltage input
39	VIN6	AIN	Battery voltage input
40	VIN5	AIN	Battery voltage input
41	VIN4	AIN	Battery voltage input
42	VIN3	AIN	Battery voltage input
43	VIN2	AIN	Battery voltage input
44	VIN1	AIN	Battery voltage input
45	VIN0	AIN	Battery voltage input
46	GND0	P	Ground
47	ISENS0	AIN	Analog input for current integration circuit
48	ISENS1	AIN	Analog input for current integration circuit

**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 (PIOR0).

**HVO:** high voltage output

**HVIN:** high voltage input

**HVIO:** high voltage input/output

**P:** power

**DIO:** digital I/O

**DIN:** digital input

**DOUT:** digital output

**AIN:** analog input

**AO:** analog output

## 3.2 Pin Functions

### 3.2.1 Pin type and alternate functions

(1/2)

Function name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P00 <sup>Note 4</sup>	7-1-4	I/O	Input port	-	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00 and P02 to P04 can be set to N-ch open-drain output (EVDD tolerance). P02 and P03 can be set to analog input <sup>Note 1</sup> .
P01 <sup>Note 4</sup>	8-1-3			-	
P02	7-3-4		Analog function	P02/ANI17/TxD1	
P03	8-3-4			P03/ANI16/RxD1	
P04 <sup>Note 4</sup>	8-1-4		Input port	-	
P05 <sup>Note 3</sup>	7-1-3			(INTP10)	
P06 <sup>Note 3</sup>				(INTP11)	
P10	8-1-8	I/O	Input port	SCK11/SCL11/TRDIOD1	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P10 and P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance).
P11	7-1-8			SI11/SDA11/TRDIOC1	
P12	7-1-7			SO11/TRDIOB1/(INTP5)	
P13	7-1-8			TRDIOA1	
P14	8-1-8			TRDIOD0	
P15				TRDIOB0	
P16			8-1-7	TI01/TO01/INTP5/TRDIOC0/(RXD0)	
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK/(TXD0)	
P20	4-3-3		I/O	Analog function	
P21				ANI1/VREFM	
P22 <sup>Note 4</sup>				-	
P23 <sup>Note 4</sup>				-	
P24 <sup>Note 4</sup>				-	
P25 <sup>Note 4</sup>				-	
P26 <sup>Note 4</sup>				-	
P27 <sup>Note 4</sup>				-	
P30 <sup>Note 3</sup>	8-1-4	I/O	Input port	INTP3	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch open-drain output (EVDD tolerance).
P31 <sup>Note 3</sup>	7-1-3			INTP4	
P40	7-1-3	I/O	Input port	TOOL0	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41 <sup>Note 4</sup>				-	
P42 <sup>Note 4</sup>				-	
P43 <sup>Note 4</sup>				-	
P50	8-1-4	I/O	Input port	INTP1	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Input of P50 and P55 can be set to TTL input buffer. Output of P50, P51, and P55 can be set to N-ch open-drain output (EVDD tolerance).
P51	7-1-4			INTP2	
P52 <sup>Note 4</sup>	7-1-3			-	
P53 <sup>Note 4</sup>				-	
P54 <sup>Note 4</sup>				-	
P55 <sup>Note 4</sup>	8-1-4			-	
P60	12-1-5	I/O	Input port	SCL	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6 V tolerance).
P61				SDA	
P62 <sup>Note 4</sup>				-	
P63 <sup>Note 4</sup>				-	
P70 <sup>Note 3</sup>	7-1-3	I/O	Input port	SCL21	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. Output of P71 and P74 can be set to N-ch open-drain output (EVDD tolerance).
P71 <sup>Note 3</sup>	7-1-4			SI21	
P72 <sup>Note 3</sup>	7-1-3			SO21	
P73 <sup>Note 3</sup>				-	
P74 <sup>Note 3</sup>	7-1-4			INTP8	
P75 <sup>Note 3</sup>	7-1-3			INTP9	
P76 <sup>Note 3</sup>				KR6	
P77 <sup>Note 4</sup>				-	

**Note 1.** Each pin can be configured as digital or analog pin by setting the port mode in the control register x (PMCx) (Can be specified in 1-bit units).

**Note 2.** Each pin can be specified as either digital or analog by setting the A/D port configuration register (ADPC).

**Note 3.** This pin is used for chip to chip connection.

**Note 4.** This pin is not connected anywhere.

(2/2)

Function name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P120 <sup>Note</sup>	7-3-3	I/O	Analog function	-	Port 12. 1-bit I/O port and 4-bit input-only port. P120 can be set to analog input. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a software setting at input port.
P121 <sup>Note</sup>	2-2-1	Input	Input port	-	
P122				-	
P123 <sup>Note</sup>				-	
P124 <sup>Note</sup>				-	
P130 <sup>Note</sup>	1-1-1	Output	Output port	-	Port 13. 1-bit output-only port and 1-bit input-only port.
P137	2-1-2	Input	Input port	INTP0	
P140 <sup>Note</sup>	7-1-3	I/O	Input port	-	Port 14. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P147 can be set to analog input <sup>Note y</sup> .
P141 <sup>Note</sup>				-	
P146 <sup>Note</sup>				-	
P147 <sup>Note</sup>			7-3-3	Analog function	
RESET	2-2-1	Input		-	

**Note** This pin is not connected anywhere.

## 3.2.2 External Pin Functions

(1/2)

Category	Pin name	I/O	Function
Power supply	VCC	–	Power supply input Apply power supply voltage to VCC pin from a charger or battery.
	GND0, GND1	–	Device ground input. Connect the negative input terminal of lithium-ion battery 1 to the GND0 pin
	CREG2	–	Series regulator output port Connect to GND0 and GND1 via a capacitor (1.0 uF to 4.7uF)
	VDD	–	Positive power supply for MCU
	VSS	–	Ground input for MCU Connect the negative input terminal of lithium-ion battery 1 to the GND0 pin
	REGC <sup>Note 1.</sup>	–	Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to VSS via a capacitor (0.47 uF to 1 uF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
RESET	RESET	Input	This is the active-low system reset input pin for MCU.
		Output	This is the active-low system reset output pin for AFE.
TOOL0	TOOL0 <sup>Note 2</sup>	input	Data I/O for flash memory programmer/debugger. Connect to the VDD via an external pull-up resistor in the on-chip debug mode
Serial interface (UART0, UART1)	RxD0, RxD1	input	Serial data input pins of serial interface UART0 and UART1
	TxD0, TxD1	output	Serial data output pins of serial interface UART0 and UART1
Serial interface (CSI11, CSI20)	SCK11, SCK21	I/O	Serial clock I/O pins of serial interface CSI11, CSI21
	SI11, SI21	input	Serial data input pins of serial interface CSI11, CSI21
	SO11, SO21	output	Serial data output pins of serial interface CSI11, CSI21
Serial interface (IIC11)	SCL11	output	Serial clock output pins of serial interface IIC11
	SDA11	I/O	Serial data I/O pins of serial interface IIC11
Serial interface (IICA0)	SCL (SCLA0)	I/O	Serial clock I/O pins of serial interface IICA0
	SDA (SDAA0)	I/O	Serial data I/O pins of serial interface IICA0
A/D converter	AN0 to AN2	input	AFE A/D converter analog input
	ANI0, ANI1, ANI16, ANI17	input	MCU A/D converter analog input
Current integration circuit and overcurrent detection circuit	ISENS0, ISENS1	input	Analog input for current integration circuit and over current detection circuit
Timer	TRDIOA0 TRDIOB0 TRDIOC0 TRDIOD0 TRDIOA1 TRDIOB1 TRDIOC1 TRDIOD1	I/O	Timer RD input/output
High voltage I/O port	HVP0, HVP1	I/O	High voltage N-ch open-drain I/O in correspondence with 50V tolerance
External interrupt input	INTP0 to INTP5 INTP8 to INTP11	input	Interrupt request input pin. Only INTP0 to INTP2 and INTP5 pins are connected to the external pin. INTP3, INTP4, and INTP8 to INTP11 connect interrupt request signal of AFE in the package and do not connect to any pin
Key interrupt input	KR6		Key interrupt request input pin
External clock	EXCLK	Input	External clock input for main system clock
Power on circuit	PON	input	Power on input for release from power down state

(2/2)

Category	Pin name	I/O	Function
Cell voltage input	VTOP	input	Total battery cell voltage input pin.
	VIN7	input	The positive input terminal of lithium-ion battery 7.
	VIN6	Input	The negative input terminal of lithium-ion battery 7 and the positive input terminal of lithium-ion battery 6
	VIN5	Input	The negative input terminal of lithium-ion battery 6 and the positive input terminal of lithium-ion battery 5
	VIN4	Input	The negative input terminal of lithium-ion battery 5 and the positive input terminal of lithium-ion battery 4
	VIN3	Input	The negative input terminal of lithium-ion battery 4 and the positive input terminal of lithium-ion battery 3
	VIN2	Input	The negative input terminal of lithium-ion battery 3 and the positive input terminal of lithium-ion battery 2
	VIN1	Input	The negative input terminal of lithium-ion battery 2 and the positive input terminal of lithium-ion battery 1
	VIN0	Input	The negative input terminal of lithium-ion battery 1

**Note 1.** REGC is not external power supply pin. (Do not draw current from REGC.)

**Note 2.** After reset release, the connection between P40/TOOL0 and the operating mode are as follows.

**Table 3-1 TOOL0 Pin Operation Mode after Reset Release**

P40/TOOL0	P137/INTP0	Operation Mode
VDD	-	Normal operation mode
0 V	VDD	Flash memory programming mode
0 V	0 V	SMBus or UART Boot programming mode

### 3.2.3 Connect Pins Between AFE and MCU

AFE and MCU are connected with dedicated communication signals which are reference voltage for MCU and interrupt signal from AFE to MCU in the package.

MCU pin	AFE pin	Pin state of AFE	Function
P30/INTP3	INT_PT	Output	High voltage pin input edge detection interrupt output
P31/INTP4	INT_I2C	Output	SCL/SDA pin through
P74/INTP8	INT_AD	Output	ADC completion interrupt output
P75/INTP9	INT_CC	Output	Current Integration (CC) completion interrupt output
P05/INTP10	INT_TM	Output	AFE Timer underflow interrupt output (AFE timer A or AFE timer B)
P06/INTP11	INT_ANL	Output	Abnormal interrupt output (Over current detection x3, MCU runaway detection, or Cell voltage and Temperature (AN pin) detection circuit)
P76/KR6	INT_WU	Output	Wakeup interrupt output (Wakeup current detection or PON pin input edge detection)
P70/SCK21	CLK	Input	Clock signal of communication between AFE and MCU
P71/SI21	DO	Output	Data signal (From AFE to MCU) communication between AFE and MCU
P72/SO21	DI	Input	Data signal (From MCU to AFE) communication between AFE and MCU
P73	CS	Input	Control signal of communication between AFE and MCU
P60	SCL_A	-	Connection of P60/SCLA0 and SCL pin. (With pull-down resistor and external interrupt function in the AFE.)
P61	SDA_A	-	Connection of P61/SDAA0 and SDA pin. (With pull-down resistor and external interrupt function in the AFE.)

**Note** CLK, DI and CS are connected to GND0 and GND1 via pull up resistor.

### 3.3 Unused Pins Connection

**Table 3-2 Unused Pins connection**

Pin Name	Recommended Connection of Unused Pins
P02, P03	Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P10-P17	Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P20-P27	Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P40/TOOL0	Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P50, P51	Input: Independently connect to VDD or VSS via a resistor. Output: Leave open.
P60-P61	Input: Leave open Output: Set the port's output latch to 0 and leave the pins open.
P122	Input: Independently connect to VDD or VSS via a resistor.
P137	Input: Independently connect to VDD or VSS via a resistor.
HVP0-1	Leave open.
AN0-AN2	Leave open.
DFOUT	Leave open.
CFOUT	Leave open.
VIN7-VIN2	Connect input pin for most positive cell.
ISENS1, ISENS0	Connect to GND 0 or GND1.

3.4 AFE Pin Block Diagram

Figure 3-1 Pin Block Diagram of VCC Pin

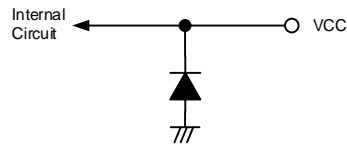


Figure 3-2 Pin Block Diagram of CFOUT and DFOUT Pin

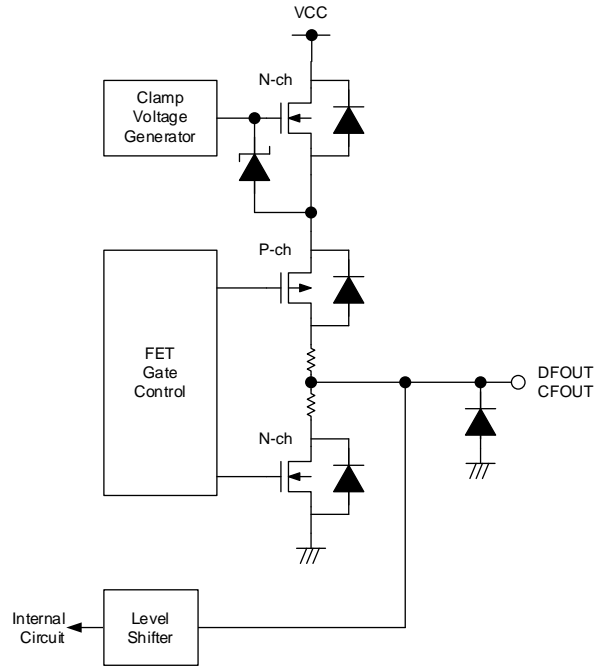


Figure 3-3 Pin Block Diagram of PON Pin

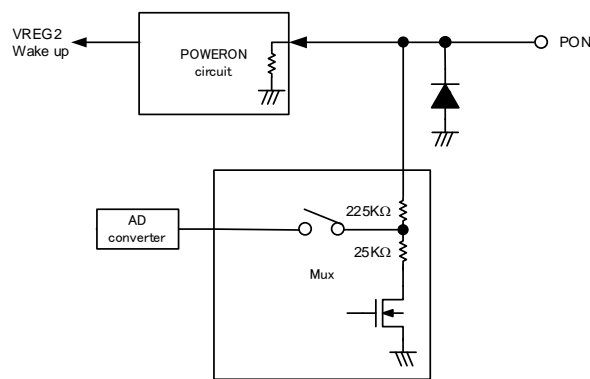


Figure 3-4 Pin Block Diagram of VTOP pin and VIN7 to VIN0 Pin

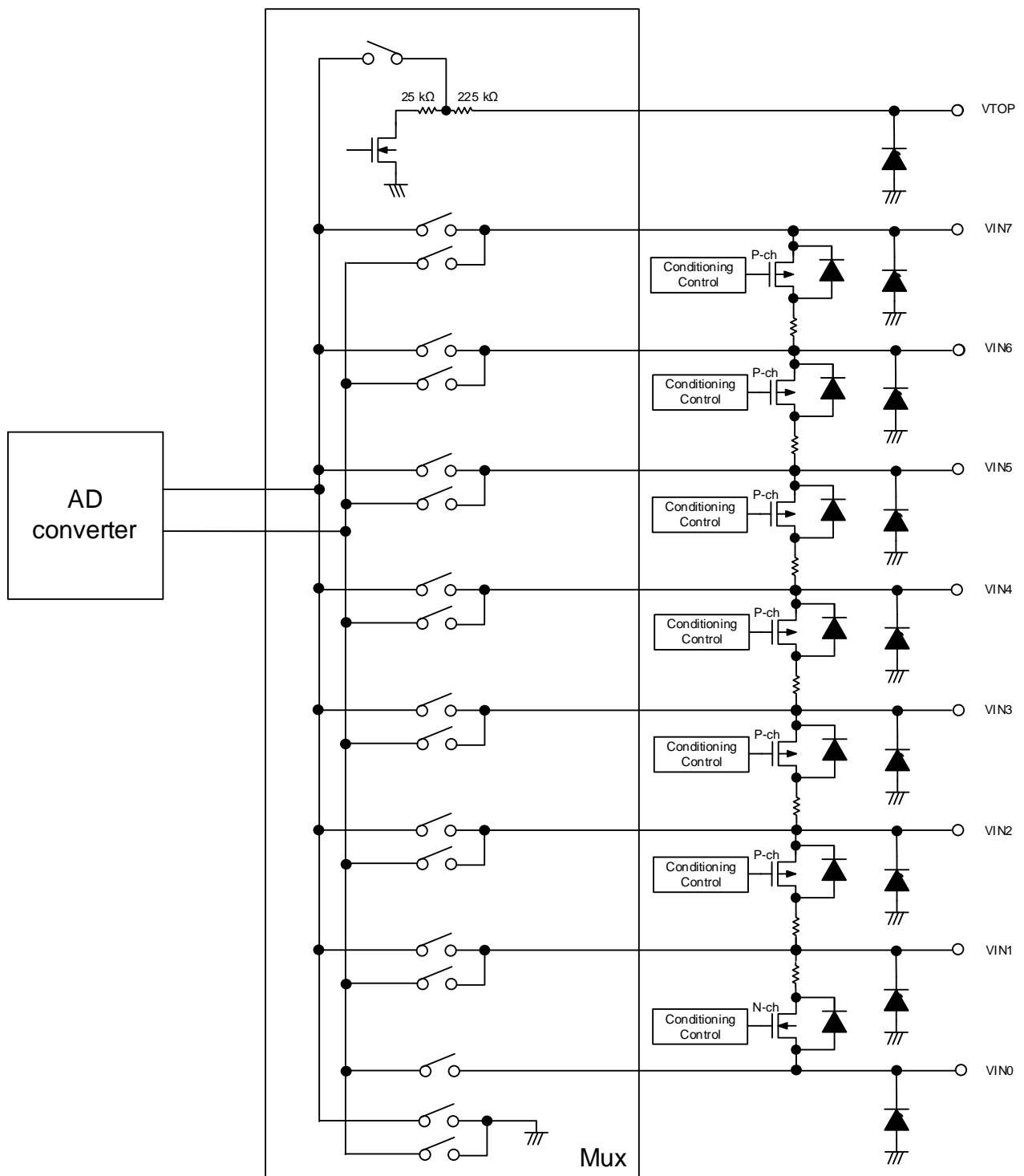


Figure 3-5 Pin Block Diagram of HVP0 and HVP1 Pin

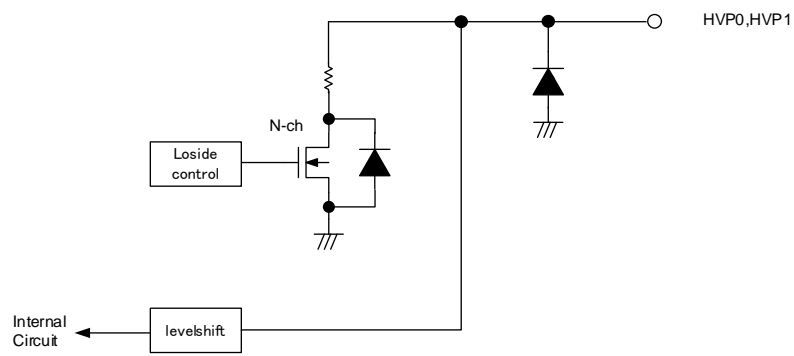


Figure 3-6 Pin Block Diagram of CREG2 Pin

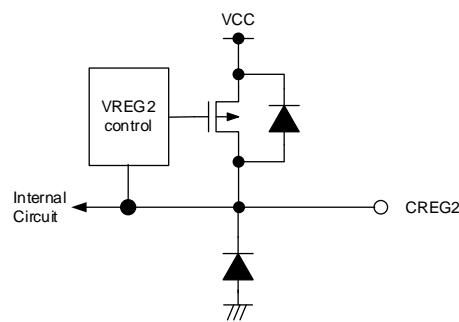


Figure 3-7 Pin Block Diagram of AN0, AN1 and AN2 Pin

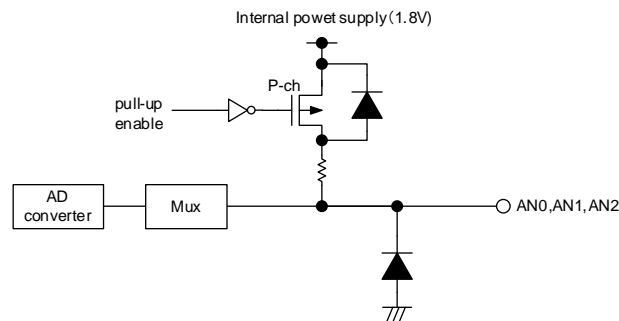


Figure 3-8 Pin Block Diagram of ISENSE0 and ISENSE1 Pin

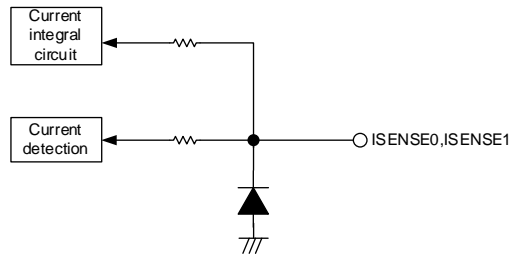
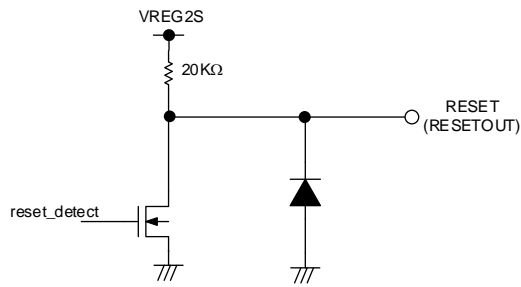


Figure 3-9 Pin Block Diagram of RESETOUT Pin



### 3.5 MCU Pin Block Diagram

Figure 3-10 Pin Block Diagram of Pin type 2-1-1

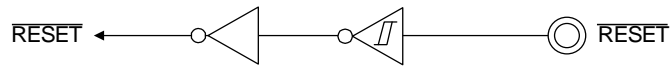
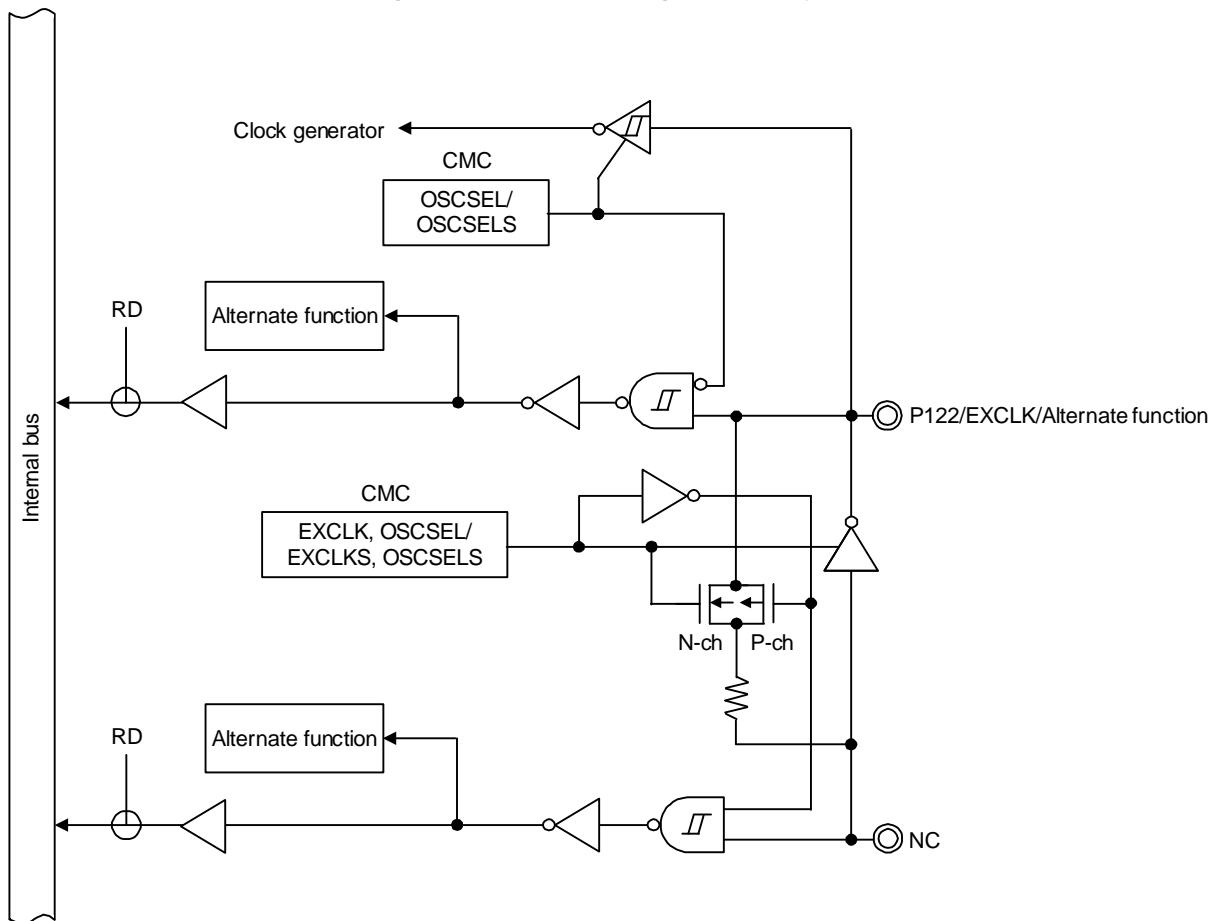


Figure 3-11 Pin Block Diagram of Pin type 2-1-2

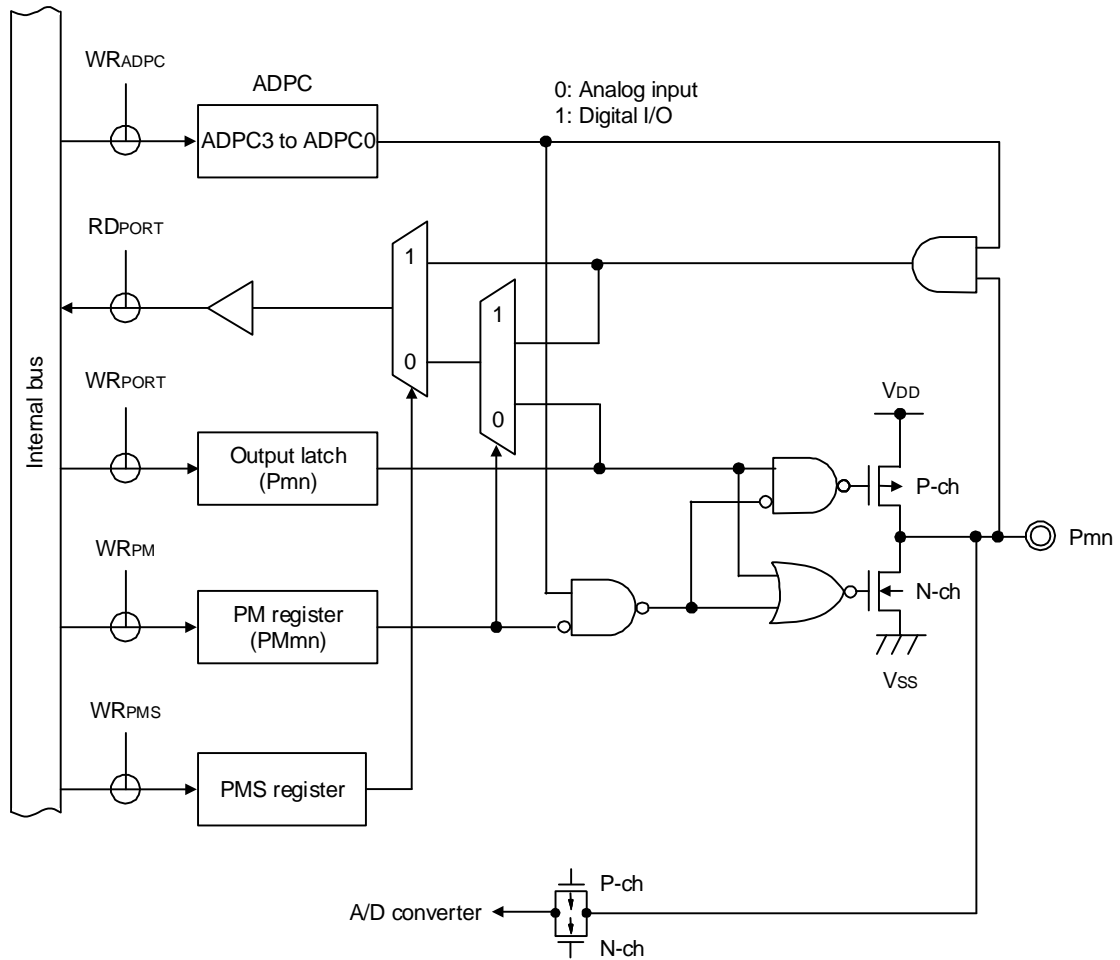
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-12 Pin Block Diagram of Pin type 2-2-1



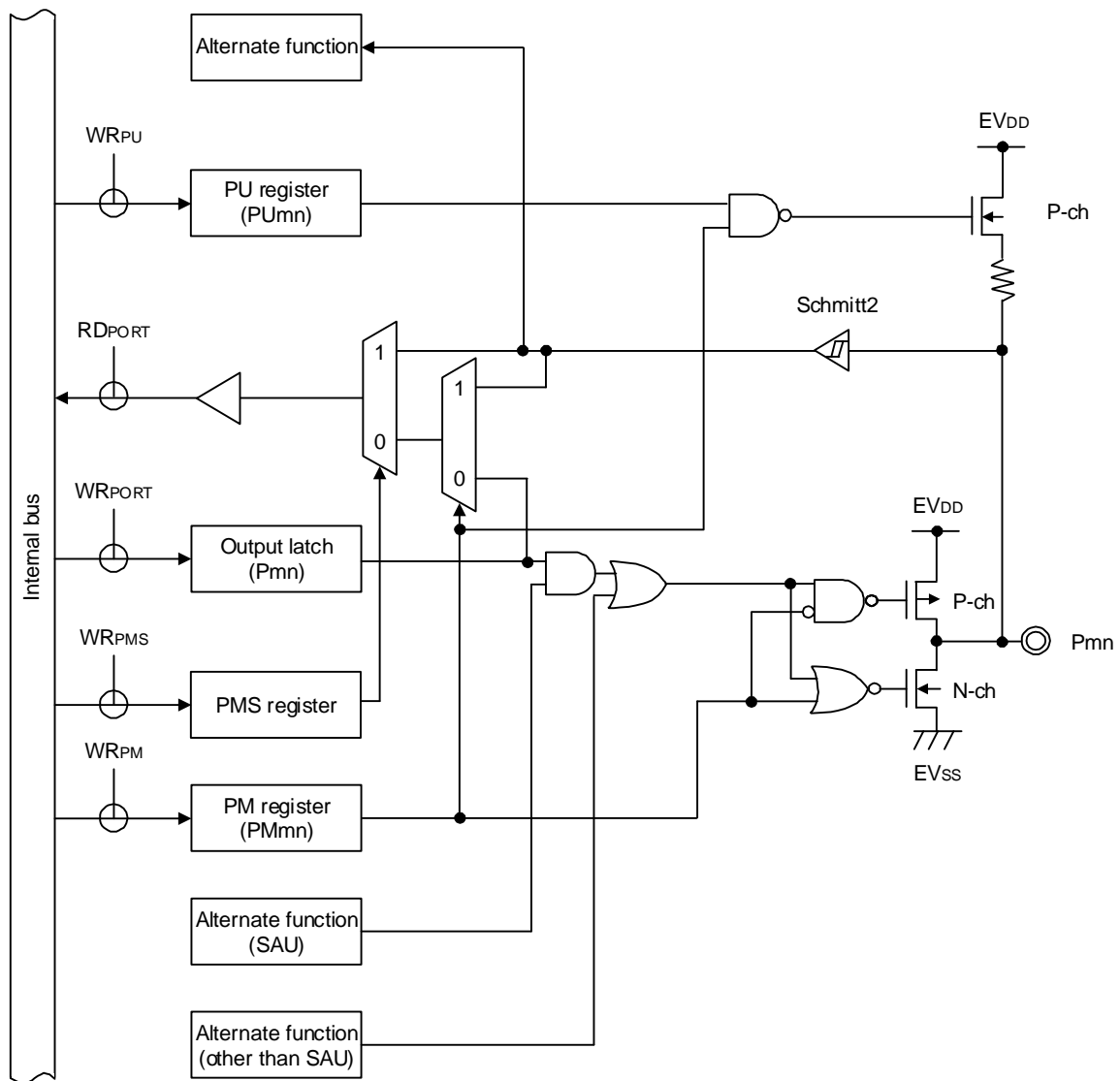
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-13 Pin Block Diagram of Pin type 4-3-3



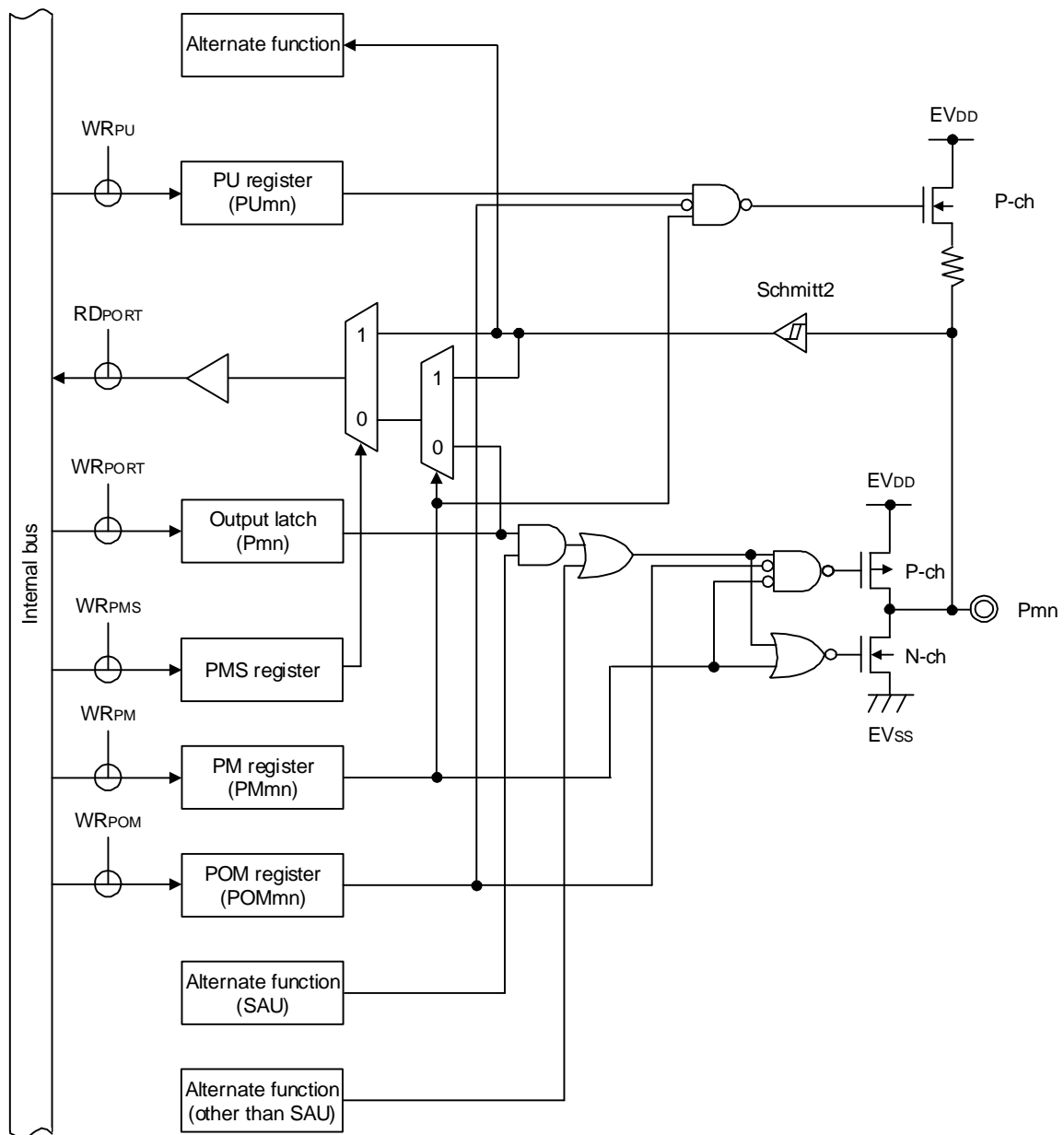
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-14 Pin Block Diagram of Pin type 7-1-3



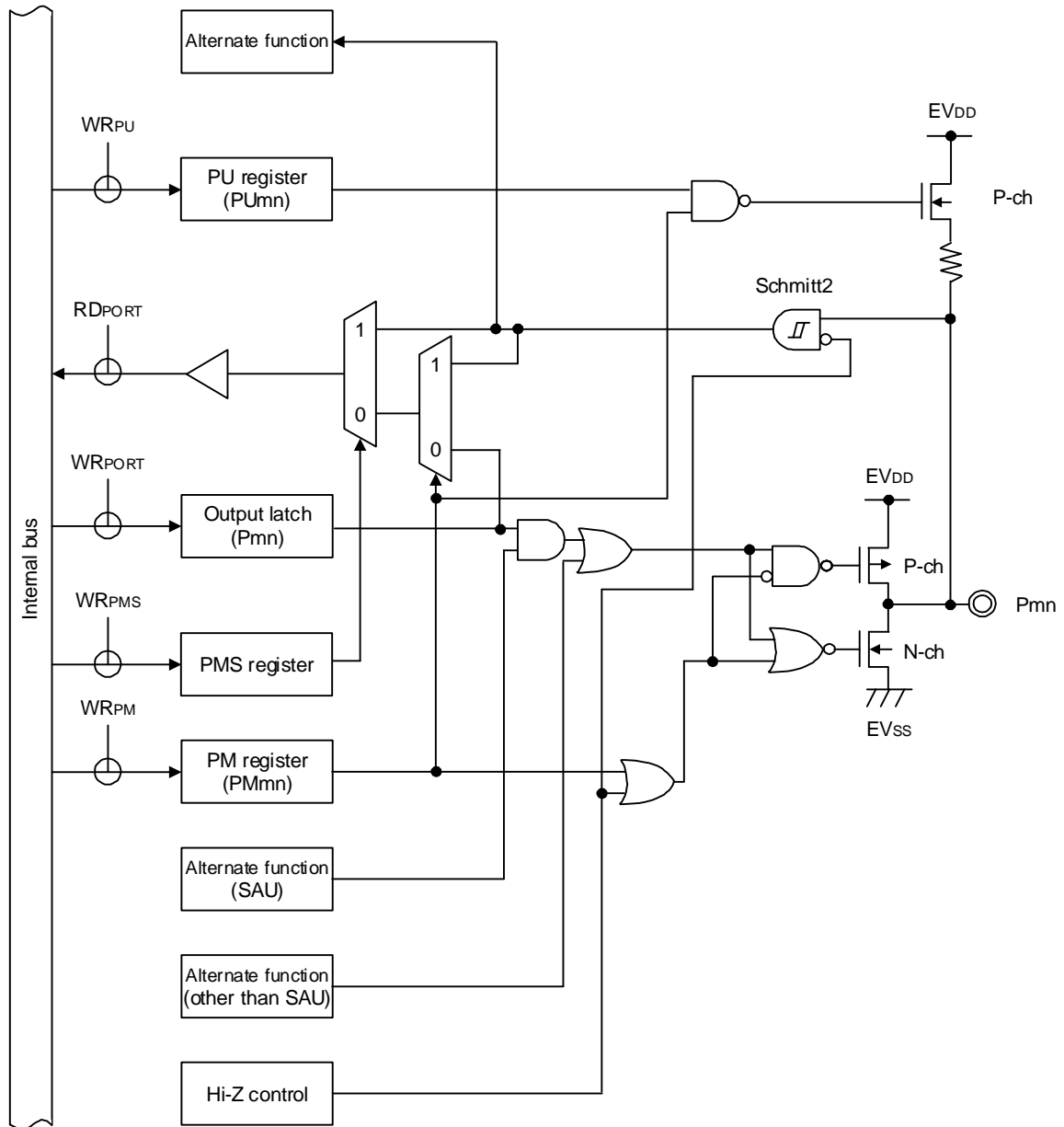
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-15 Pin Block Diagram of Pin type 7-1-4



**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

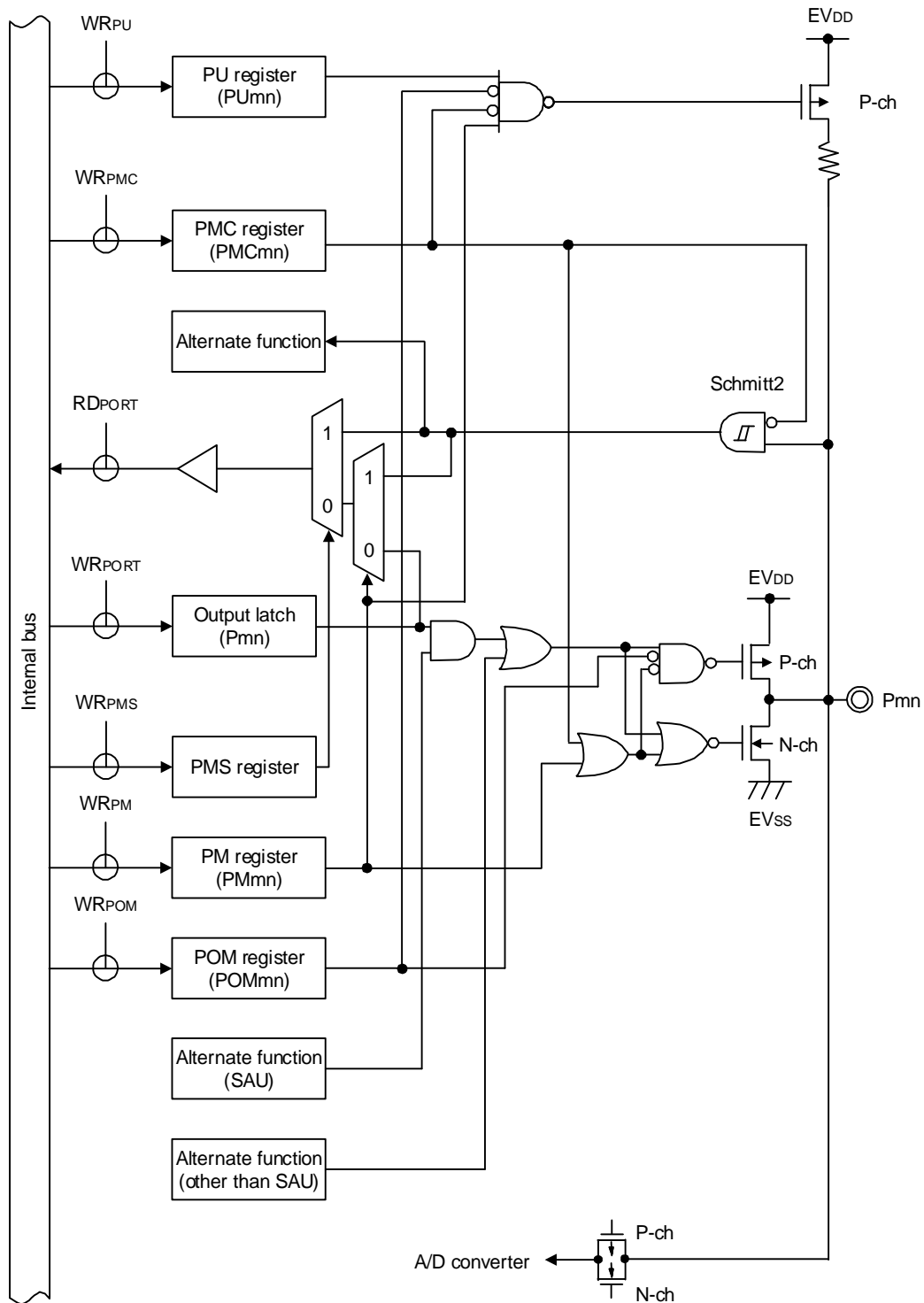
Figure 3-16 Pin Block Diagram of Pin type 7-1-7



**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

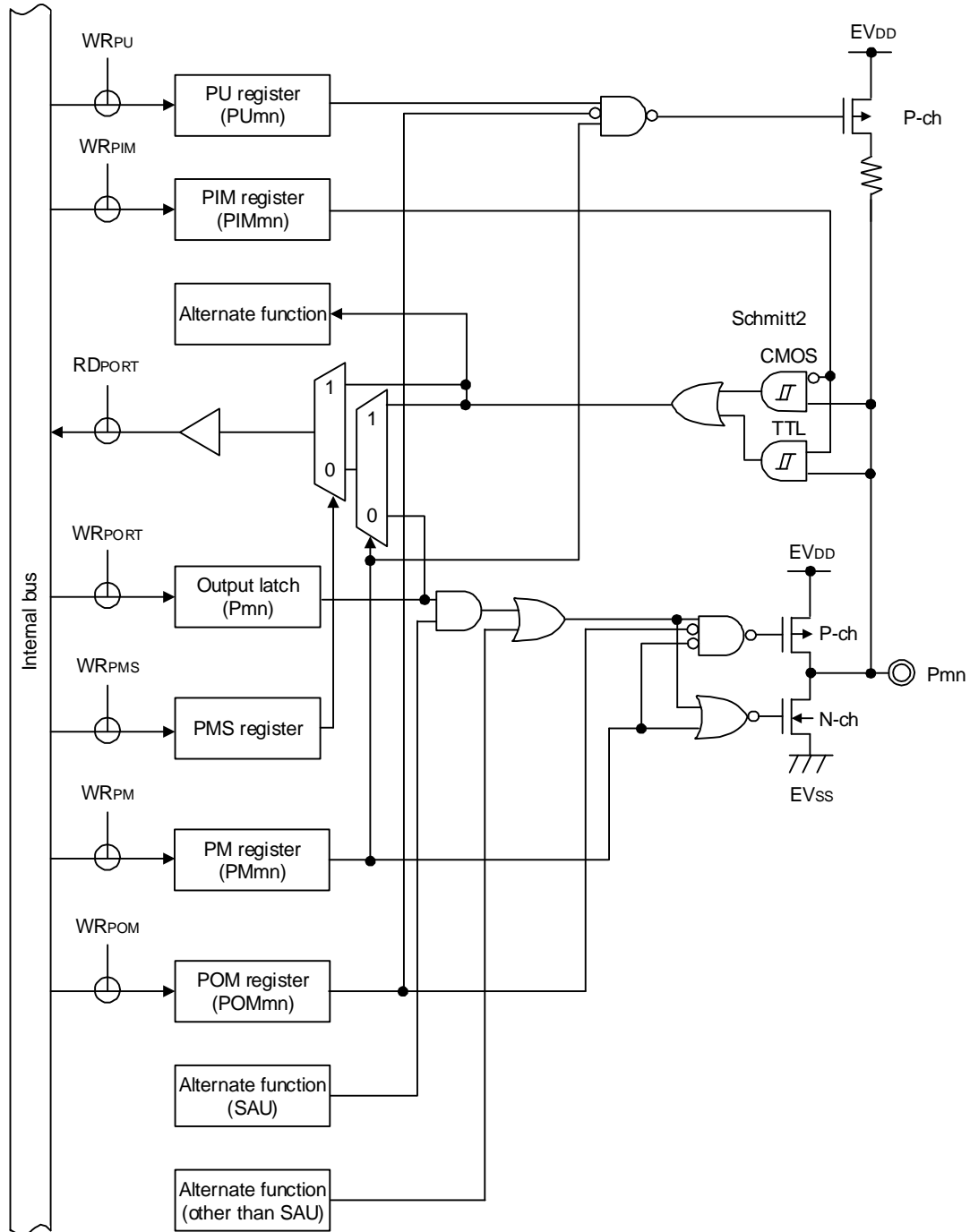


Figure 3-18 Pin Block Diagram of Pin type 7-3-4



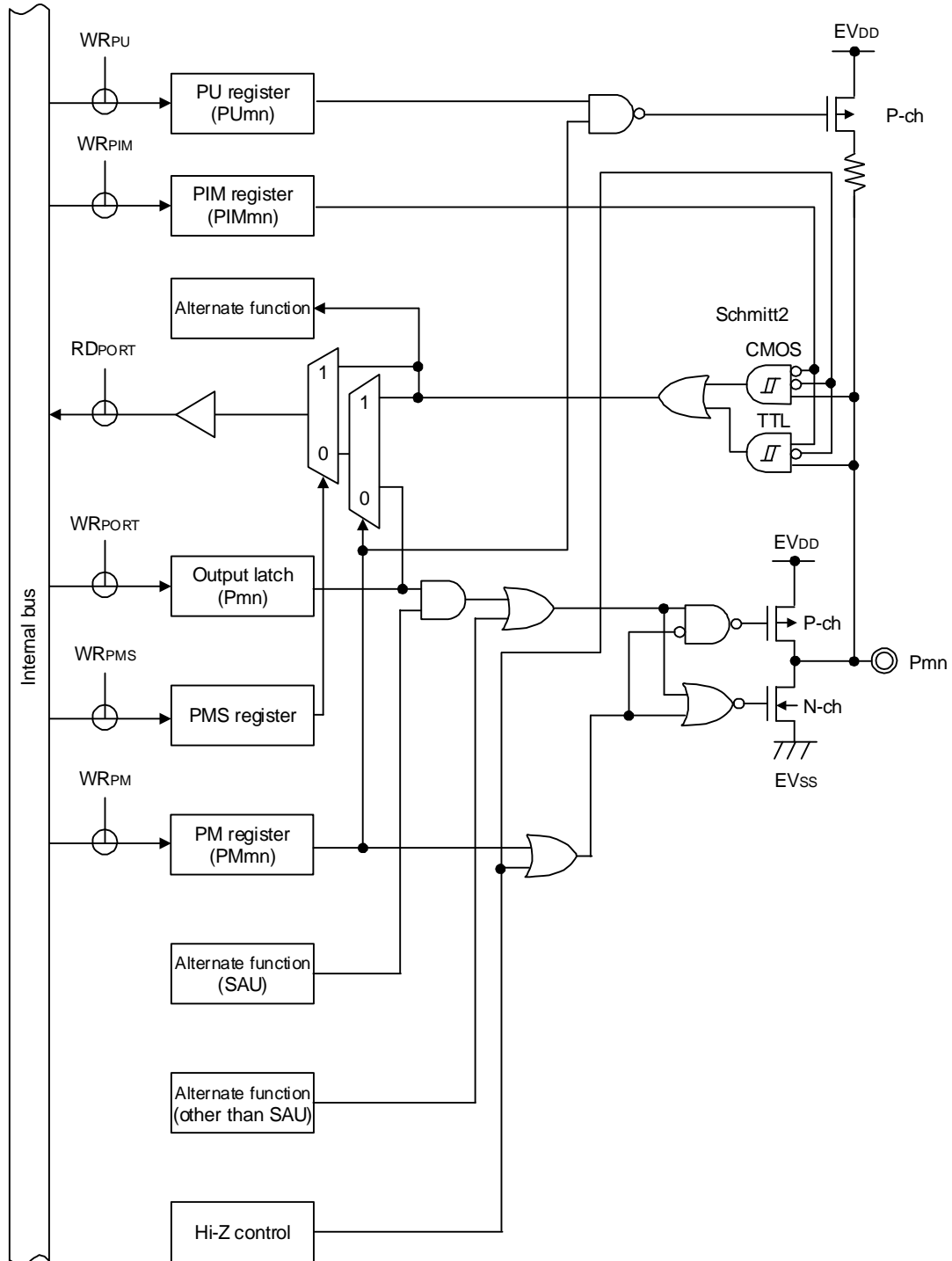
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-19 Pin Block Diagram of Pin type 8-1-4



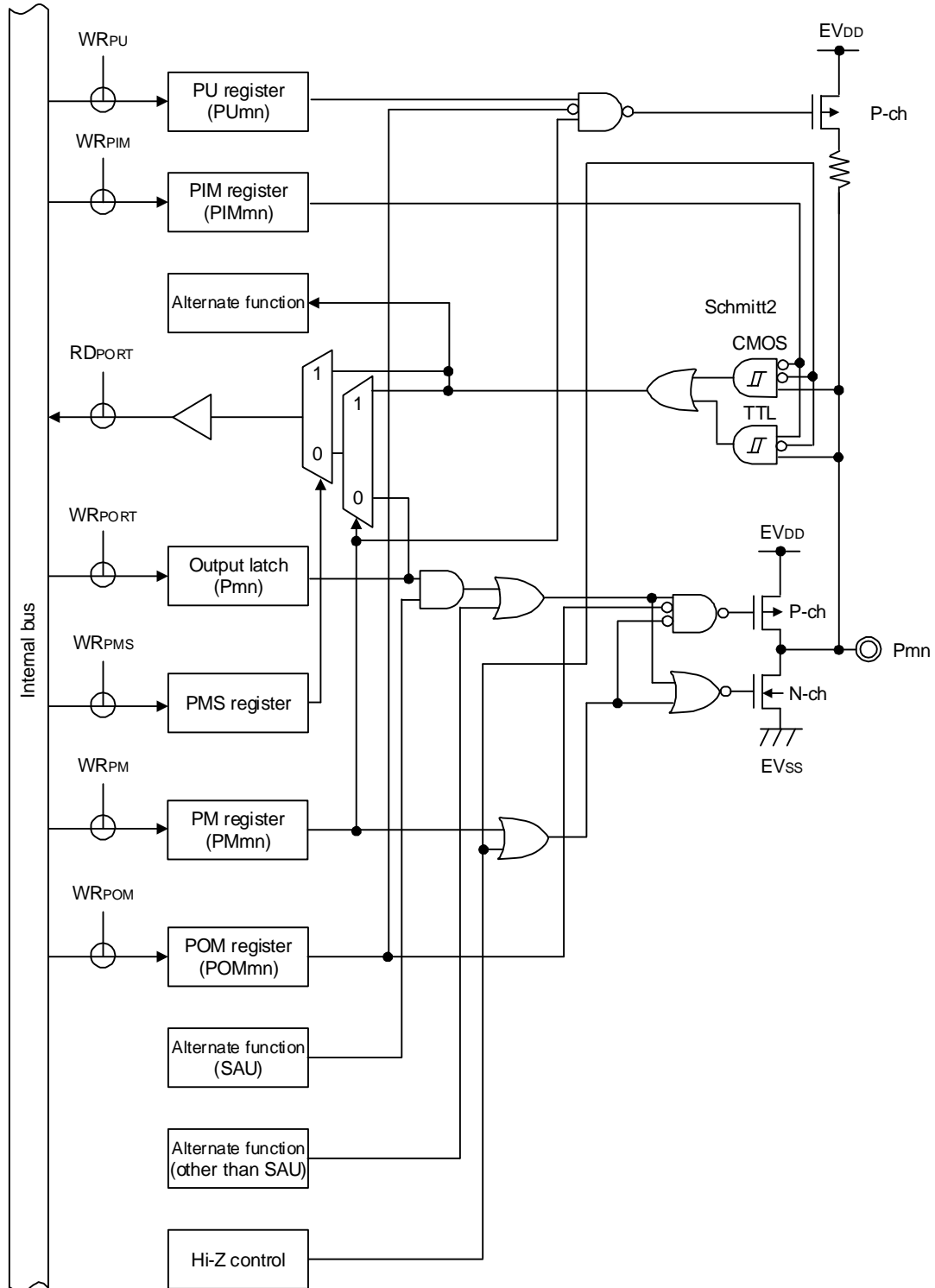
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-20 Pin Block Diagram of Pin type 8-1-7



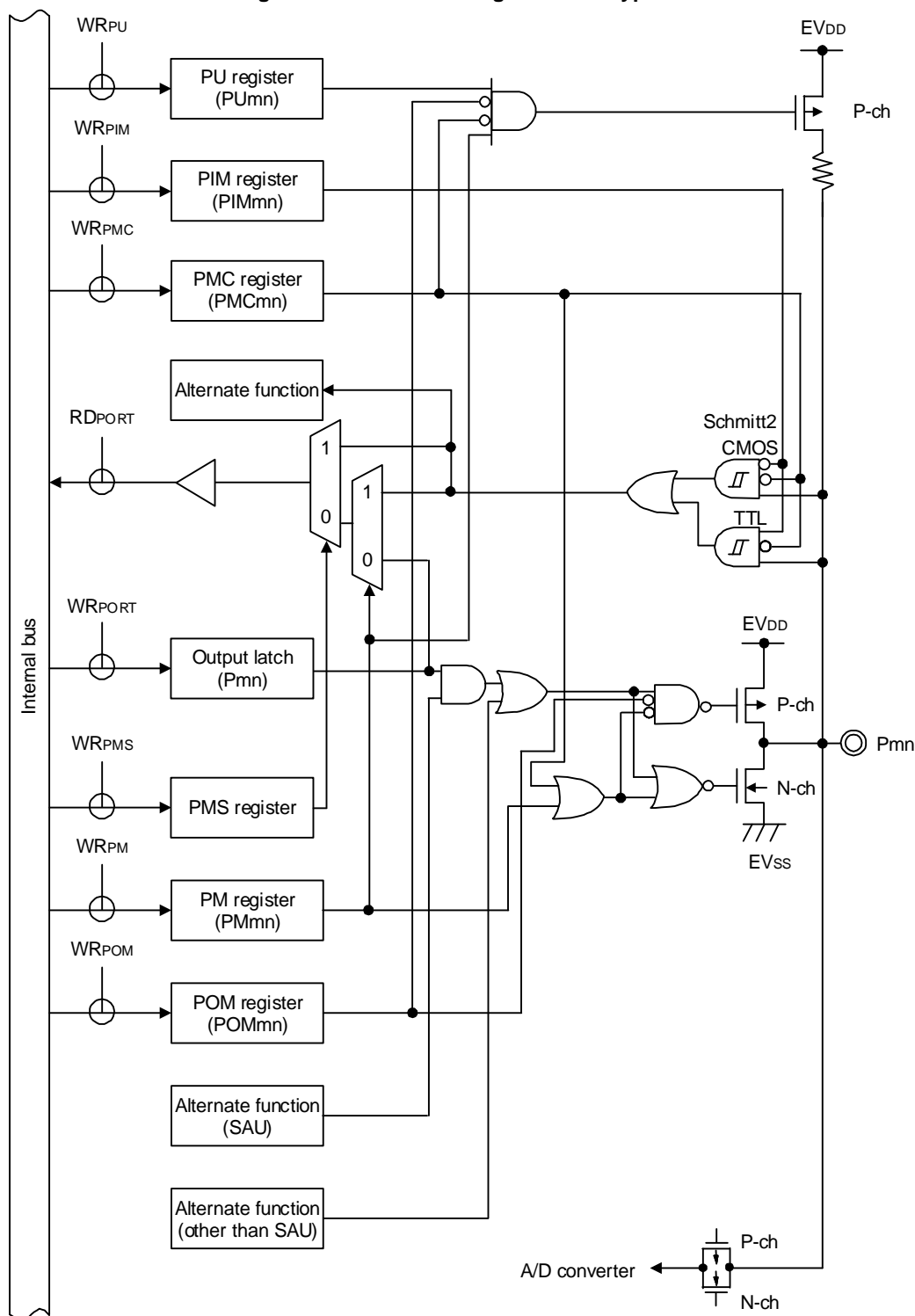
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-21 Pin Block Diagram of Pin type 8-1-8



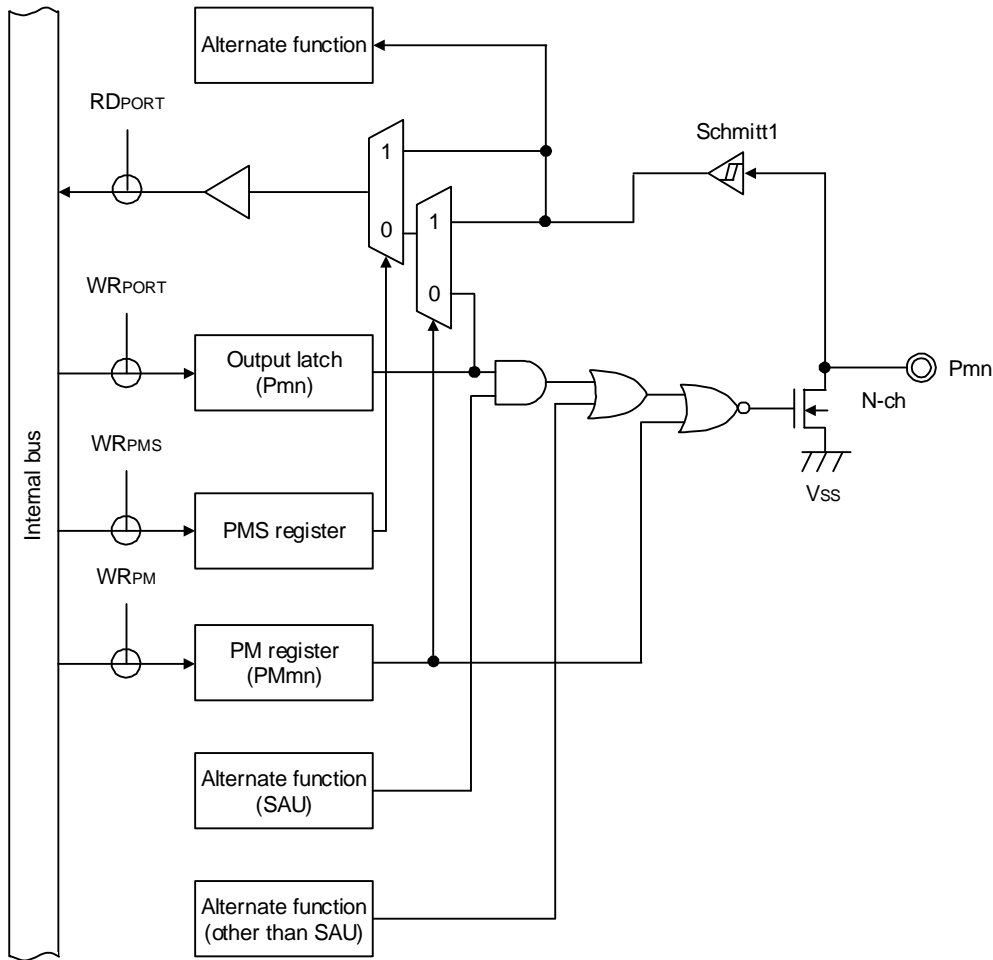
**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-22 Pin Block Diagram of Pin type 8-3-4



**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

Figure 3-23 Pin Block Diagram of Pin type 12-1-5



**Remark** Refer to 3.2.1 Pin type and alternate functions for alternate functions.

## CHAPTER 4. ELECTRICAL SPECIFICATIONS

**Caution** This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	V <sub>CC</sub>	VCC		-0.5 to +50.0	V
	V <sub>DD</sub>	VDD		-0.5 to +6.5	V
	GND	GND0, GND1, VSS		-0.5 to 0.3	V
CREG2 pin input voltage	V <sub>CREG2</sub>	CREG2		-0.3 to 6.5 <sup>Note 2</sup>	V
REGC pin input voltage	V <sub>IREGC</sub>	REGC		-0.3 to 2.8 and -0.3 to (VDD+0.3) <sup>Note 1</sup>	V
Input voltage	V <sub>I1</sub>	P02, P03, P10 to P17, P40, P50, P51, P122, P137, RESET		-0.3 to (VDD+0.3) <sup>Note 3</sup>	V
	V <sub>I2</sub>	P60 to P61(N-ch open-drain)		-0.3 to +6.5	V
	V <sub>IN-H1</sub>	V <sub>TOP</sub> , VIN7, VIN6, VIN5, VIN4, VIN3, VIN2, VIN1, PON <sup>Note 5</sup>		-0.5 to +50.0	V
	V <sub>IN-H2</sub>	HVP0, HVP1 <sup>Note 5</sup>		-0.5 to +50.0	V
	V <sub>IN-B</sub>	VIN7 to VIN6, VIN6 to VIN5, VIN5 to VIN4, VIN4 to VIN3, VIN3 to VIN2, VIN2 to VIN1, VIN1 to VIN0		-0.5 to +6.5	V
	V <sub>IN-M</sub>	VIN0		-0.5 to +5.0	V
	V <sub>IN-L</sub>	AN0, AN1, AN2, ISENS0, ISENS1		-0.5 to +2.0	V
	V <sub>AI</sub>	ANI0, ANI1, ANI16, ANI17		-0.3 to VDD +0.3 and -0.3 to AVREF(+) +0.3 <sup>Notes 3, 4</sup>	V
Output voltage	V <sub>O1</sub>	P02, P03, P10 to P17, P40, P50, P51		-0.3 to (VDD+0.3) <sup>Note 3</sup>	V
	V <sub>O-H</sub>	CFOUT, DFOUT		-0.5 to +50.0	V
High-level output current	I <sub>OH1</sub>	Per pin	P02, P03, P10 to P17, P40, P50, P51	-40	mA
		Total of all pins	P02, P03, P10 to P17, P40, P50, P51	-70	mA
	I <sub>OH2</sub>	Per pin	P20, P21	-0.5	mA
		Total of all pins	P20, P21	-2.0	mA
Low-level output current	I <sub>OL1</sub>	Per pin	P02, P03, P10 to P17, P40, P50, P51, P60, P61	+40	mA
		Total of all pins	P02, P03, P10 to P17, P40, P50, P51, P60, P61	+70	mA
	I <sub>OL2</sub>	Per pin	P20, P21	+1	mA
		Total of all pins	P20, P21	+5	mA
Power consumption	P <sub>d</sub>	T <sub>opr</sub> = 25 C		300	mW
Operating ambient Temperature	T <sub>A</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

(Note, Caution and Remark are listed on next page.)

- Note 1.** Connect the REGC pin to VSS via a capacitor (0.47 uF to 1uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- Note 2.** Connect the CREG2 pin to GND0 or GND1 via a capacitor (1 uF to 4.7 uF). This value regulates the absolute maximum rating of the CREG2 pin.
- Note 3.** Must be 6.5 V or lower.
- Note 4.** Do not exceed AVREF (+) + 0.3 V in case of A/D conversion target pin.
- Note 5.** Do not exceed total battery cell voltage.

**Caution** Product quality may degrade if the absolute maximum rating has been exceeded. The absolute maximum ratings are rated values where the product is on the verge of suffering physical damage, therefore the product must be used within that ensure the absolute maximum ratings are not exceeded.

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** AVREF (+): + side reference voltage of the A/D converter.

**Remark 3.** GND (GND0, GND1 and VSS): Reference voltage.

## 4.2 Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply	VCC		4.0	-	40.0	V
	GND	GND0, GND1, VSS	-	0.0	-	V

## 4.3 Supply current characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = 0\text{V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power down mode current 1	IPD	VCC = 24.5 V	-	-	2.0	uA
Power down mode current 2 (Low voltage)	IPDL	VCC = 4.0 V	-	-	1.0	uA
Sleep mode current 1	ISLP1	MCU operation mode: STOP mode AFE operation mode: Low power operation mode <sup>Note</sup> ALOCO = ON, AOCO = OFF CD = SC is ON, AFE Timer = ON, AFE WDT = ON, CFOUT = L, DFOUT = L, AD(AFE) = OFF, CC = OFF	-	25.0	50.0	uA
Sleep mode current 2	ISLP2	MCU operation mode: STOP mode AFE operation mode: Low power operation mode <sup>Note</sup> ALOCO = ON, AOCO = OFF CD = ALL ON, AFE timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = OFF, CC = OFF	-	40.0	60.0	uA
Normal mode current	INOM	MCU operation mode: LS (Low-Speed main) mode, fHOCO = 8 MHz AFE operation mode: Normal operation mode ALOCO = ON, AOCO = ON CD = ALL ON, AFE Timer = ON, AFE WDT = ON, CFOUT = H, DFOUT = H, AD(AFE) = ON, CC = ON	-	2.0	3.0	mA

**Note** "Sleep mode current 1 and 2" is the current consumption when PCON register value is set to "43H".

**Caution** After trimming.

## 4.4 Oscillator Characteristics

### 4.4.1 MCU On-chip oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency <sup>Note 1, 2</sup>	f <sub>IH</sub>		1	-	32	MHz
High-speed on-chip oscillator clock frequency accuracy		$-20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-1.0	-	+1.0	%
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	-1.5	-	+1.5	%
Low-speed on-chip oscillator clock frequency	f <sub>IL</sub>		-	15	-	kHz
Low-speed on-chip oscillator clock frequency accuracy			-15	-	+15	%

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

### 4.4.2 AFE On-chip oscillator characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AFE on-chip oscillator clock frequency	f <sub>AOCO</sub>		-	4.194	-	MHz
AFE on-chip oscillator clock frequency accuracy			-2	-	+2	%
AFE Low-speed on-chip oscillator clock frequency	f <sub>ALOCO</sub>		-	131.072	-	KHz
AFE Low-speed on-chip oscillator clock frequency accuracy			-5	-	+5	%

**Caution** After trimming.

**Remark** Values in brackets are design value.

## 4.5 Pin characteristics

(1/5)

(T<sub>A</sub> = -40 to +85°C, 4.0 V ≤ VCC ≤ 40 V, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	IOH1	Per pin for P02, P03, P10 to P17, P40, P50, P51	-	-	-10.0 <sup>Note 2</sup>	mA
		Total of P02, P03, P10 to P17, P40, P50, P51 (When duty ≤ 70 % <sup>Note 3</sup> )	-	-	-55.0	mA
		Total of all pins (When duty ≤ 70 % <sup>Note 3</sup> )	-	-	-100.0	mA
	IOH2	Per pin for P20, P21	-	-	-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70 % <sup>Note 3</sup> )	-	-	-1.5	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the VDD pins to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where duty factor ≤ 70 %.

The output current value that has changed to the duty factor > 70 % the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n %).

$$\bullet \text{ Total output current from pins} = (I_{OH} \times 0.7) / (n \times 0.01)$$

<Example> Where n = 80 % and I<sub>OH</sub> = -10.0 mA

$$\text{Total output current from pins} = (-10.0 \times 0.7) / (80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

**Caution** P02, P03, P10, P11, P13 to P15, P17, P50 and P51 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low <sup>Note 1</sup>	IOL1	Per pin for P02, P03, P10 to P17, P40, P50, P51	-	-	20.0 <small>Note 2</small>	mA
		Per pin for P60, P61	-	-	15.0 <small>Note 2</small>	mA
		Total of P02, P03, P10 to P17, P40, P50, P51 (When duty $\leq 70\%$ <small>Note 3</small> )	-	-	70.0	mA
			-	-	15.0	mA
	Total of all pins (When duty $\leq 70\%$ <small>Note 3</small> )		-	-	150.0	mA
	IOL2	Per pin for P20, P21	-	-	0.4 <small>Note 2</small>	mA
		Total of all pins (When duty $\leq 70\%$ <small>Note 3</small> )	-	-	5.0	mA

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor  $\leq 70\%$ .

The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from  $70\%$  to  $n\%$ ).

- Total output current of pins =  $(IOL \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $IOL = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7\text{ mA}$$

However, the allowable current flow into one pin does not change with the duty factor.

A current higher than the absolute maximum rating must not flow into any one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	$V_{IH1}$	P02, P03, P10 to P17, P40, P50, P51	Normal input buffer	0.8 VDD	-	VDD	V
	$V_{IH2}$	P03, P04, P10, P14 to P17, P50, P51	TTL input buffer $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5	-	VDD	V
	$V_{IH3}$	P20, P21		0.7 VDD	-	VDD	V
	$V_{IH4}$	P60, P61		0.7 VDD	-	6.0	V
	$V_{IH5}$	P122, P137, RESET		0.8 VDD	-	VDD	V
Input voltage, low	$V_{IL1}$	P02, P03, P10 to P17, P40, P50, P51	Normal input buffer	0	-	0.2 VDD	V
	$V_{IL2}$	P03, P04, P10P14 to P17, P50, P51	TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	0	-	0.5	V
	$V_{IL3}$	P20, P21		0	-	0.3 VDD	V
	$V_{IL4}$	P60, P61		0	-	0.3 VDD	V
	$V_{IL5}$	P122, P137, RESET		0	-	0.2 VDD	V

**Caution** The maximum value of  $V_{IH}$  of pins P02, P03, P10, P11, P13, P14, P17 is VDD, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high	$V_{OH1}$	P02, P03, P10 to P17, P40, P50, P51	$I_{OH1} = -1.5\text{ mA}$	VDD - 0.5	-	-	V
	$V_{OH2}$	P20, P21	$I_{OH2} = -100\text{ }\mu\text{A}$	VDD - 0.5	-	-	V
Output voltage, low	$V_{OL1}$	P02, P03, P10 to P17, P40, P50, P51	$I_{OL1} = 3.0\text{ mA}$	-	-	0.6	V
			$I_{OL1} = 1.5\text{ mA}$	-	-	0.4	V
			$I_{OL1} = 0.6\text{ mA}$	-	-	0.4	V
			$I_{OL1} = 0.3\text{ mA}$	-	-	0.4	V
	$V_{OL2}$	P20, P21	$I_{OL2} = 400\text{ }\mu\text{A}$	-	-	0.4	V
$V_{OL3}$	P60, P61	$I_{OL3} = 3.0\text{ mA}$	-	-	0.4	V	

**Caution** P02, P03, P10, P11, P13, P14, P17 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 4.0 V ≤ VCC ≤ 40 V, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	ILIH1	P02, P03, P10 to P17, P40, P50, P51	VI = VDD	-	-	1	uA	
	ILIH2	P20, P21, P137	VI = VDD	-	-	1	uA	
	ILIH3	P122	VI = VDD	In input port or external clock input	-	-	1	uA
				In resonator connection	-	-	10	uA
Input leakage current, low	ILIL1	P02, P03, P10 to P17, P40, P50, P51	VI = VSS	-	-	-1	uA	
	ILIL2	P20, P21, P137	VI = VSS	-	-	-1	uA	
	ILIL3	P122	VI = VSS	In input port or external clock input	-	-	-1	uA
				In resonator connection	-	-	-10	uA
On-chip pull-up resistance	RU	P02, P03, P10 to P17, P40, P50, P51	VI = VSS, In input port	10	20	100	kΩ	
	RUA	AN0, AN1, AN2		7.5	10	12.5	kΩ	
	RUAR	RESET/RESETOUT		-	20	-	kΩ	

**Remark 1.** Unless specified, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** Regarding pin characteristics of CFOUT, DFOUT, refer to Section 4.8.6 Charge/discharge FET control circuit characteristics.

**Remark 3.** Regarding pin characteristics of VIN1 to VIN5 refer to Section 4.8.2 Multiplexer.

**Remark 4.** Regarding pin characteristics of HVP0 to HVP1 refer to Section 4.8.1 High-voltage port characteristics.

## 4.6 AC Characteristics

(1/2)

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T <sub>CY</sub>	Main system clock (f <sub>MAIN</sub> ) operation	HS (high-speed main) mode	0.03125	-	1	us
			LS (low-speed main) mode	0.125	-	1	us
			LV (low-voltage main) mode	0.25	-	1	us
		Subsystem clock (f <sub>SUB</sub> ) operation		28.5	30.5	31.3	us
		In the self-programming mode	HS (high-speed main) mode	0.03125	-	1	us
			LS (low-speed main) mode	0.125	-	1	us
LV (low-voltage main) mode	0.25		-	1	us		
External system clock frequency	f <sub>EXS</sub>		32	-	35	kHz	
External system clock input high-level width, low-level width	t <sub>EXHS</sub> , t <sub>EXLS</sub>		13.7	-	-	us	
Ti01, Ti02 input high-level width, low-level width	t <sub>TIH</sub> , t <sub>TIL</sub>		1/f <sub>MCK</sub> + 10	-	-	ns	

**Remark** f<sub>MCK</sub>: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1),

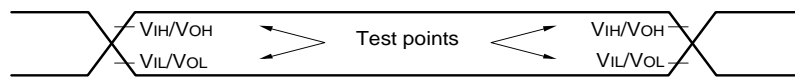
n: Channel number (n = 0 to 3))

(2/2)

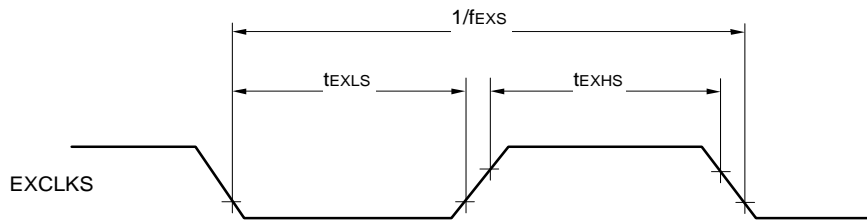
(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Timer RD input high-level width, low-level width	t <sub>TDIH</sub> , t <sub>TDIL</sub>	TRDIOA0, TRDIOA1, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	3/f <sub>CLK</sub>	-	-	ns	
Timer RD forced cutoff signal input low-level width	t <sub>TDSIL</sub>	P137/INTP0	2 MHz < f <sub>CLK</sub> ≤ 32 MHz	1	-	-	us
			f <sub>CLK</sub> ≤ 2 MHz	1/f <sub>CLK</sub> + 1	-	-	
TO01, TO02, TRDIOA0, TRDIOA1, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 output frequency	f <sub>TO</sub>	HS (high-speed main) mode	-	-	8	MHz	
		LS (low-speed main) mode	-	-	4	MHz	
		LV (low-voltage main) mode	-	-	2	MHz	
Interrupt input high-level width, low-level width	t <sub>INTH</sub> , t <sub>INTL</sub>	INTP0 to INTP11	1	-	-	us	
RESET low-level width	t <sub>RSL</sub>		10	-	-	us	

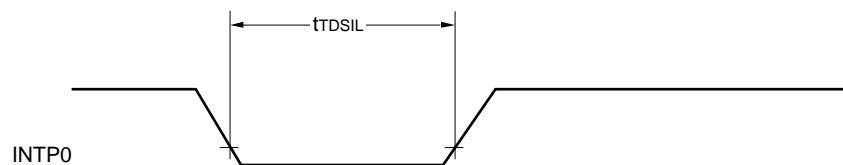
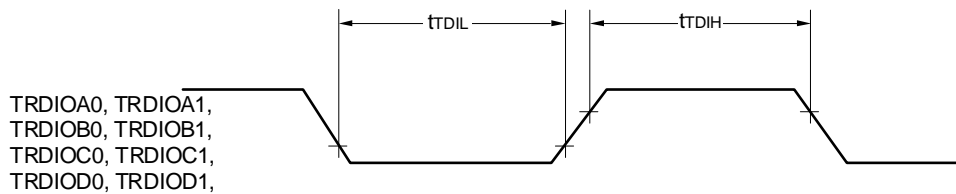
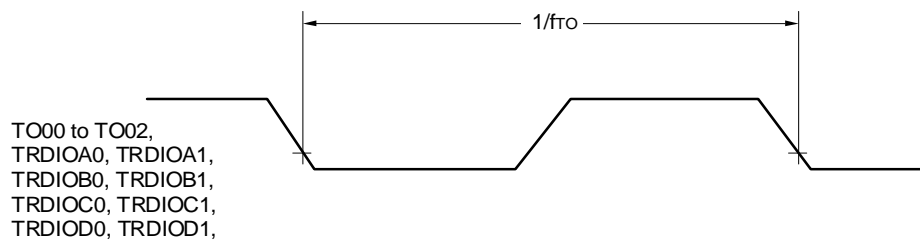
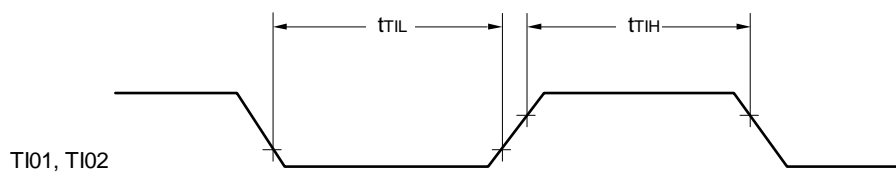
AC Timing Test Points



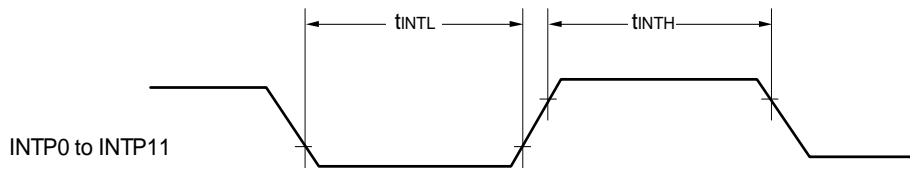
External System Clock Timing



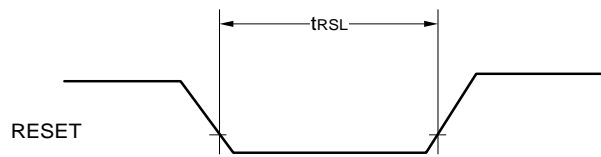
TI/TO Timing



**Interrupt Request Input Timing**

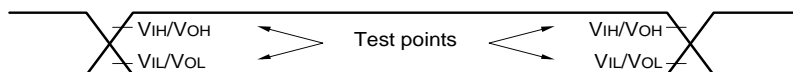


**RESET Input Timing**



## 4.7 MCU peripheral circuit characteristics

### AC Timing Test Points



### 4.7.1 Serial array unit

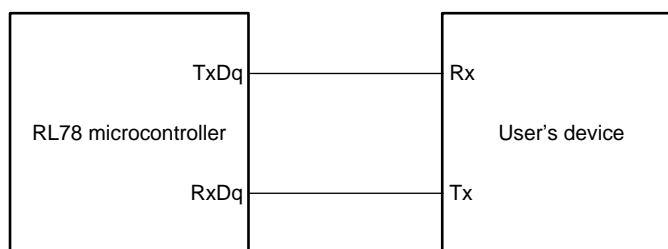
(1) During communication at same potential (UART mode)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

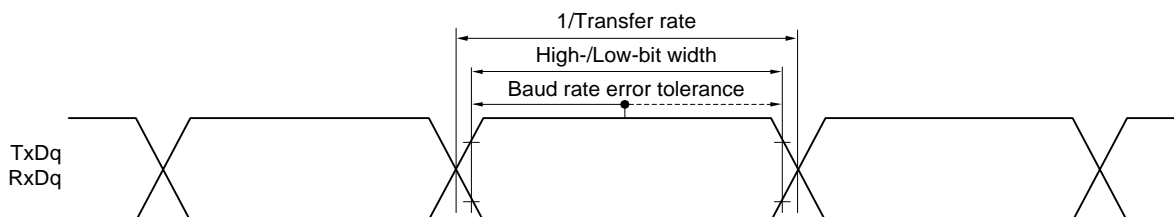
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate <small>Note</small>			-	$f_{MCK}/6$	-	$f_{MCK}/6$	-	$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$	-	5.3	-	1.3	-	0.6	Mbps

**Note** Transfer rate in the SNOOZE mode is only 4800 bps.

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).



UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 2.**  $f_{MCK}$ : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = \text{CREG2}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	125	-	500	-	1000	-	ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>		t <sub>KCY1</sub> /2 - 18	-	t <sub>KCY1</sub> /2 - 50	-	t <sub>KCY1</sub> /2 - 50	-	ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK1</sub>		44	-	110	-	110	-	ns
Slp hold time (from SCKp↓) <sup>Note 2</sup>	t <sub>SH1</sub>		19	-	19	-	19	-	ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO1</sub>	C = 30 pF <sup>Note 4</sup>	-	25	-	25	-	25	ns

**Note 1.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1.

The Slp setup time becomes "to SCKp↓" when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**Note 2.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1.

The Slp hold time becomes "from SCKp↓" when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**Note 3.** When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1.

The delay time to SOp output becomes "from SCKp↑" when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency (Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>).

m: Unit number, n: Channel number (mn = 00, 02))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

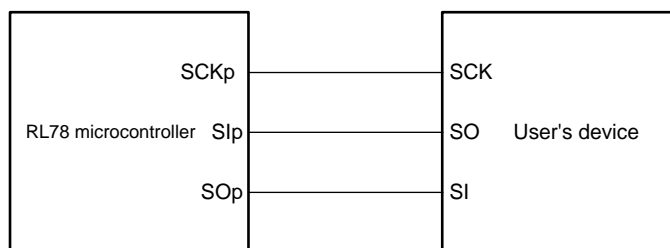
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time <small>Note 5</small>	tkCY2	1 MHz < fMCK	8/fMCK	-	—	-	—	-	ns
		fMCK ≤ 16MHz	6/fMCK	-	6/fMCK	-	6/fMCK	-	ns
SCKp high-/low-level width	tkH2, tkL2		tkCY2/2 - 8	-	tkCY2/2 - 8	-	tkCY2/2 - 8	-	ns
Slp setup time (to SCKp↑) <small>Note 1</small>	tsIK2		1/fMCK + 20	-	1/fMCK + 30	-	1/fMCK + 30	-	ns
Slp hold time (from SCKp↑) <small>Note 2</small>	tkSI2		1/fMCK + 31	-	1/fMCK + 31	-	1/fMCK + 31	-	ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	tkSO2	C = 30pF <small>Note 4</small>	-	2/fMCK + 44	-	2/fMCK + 110	-	2/fMCK + 110	ns

- Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  
The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  
The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  
The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** C is the load capacitance of the SCKp and SOp output lines.
- Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00, 10), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

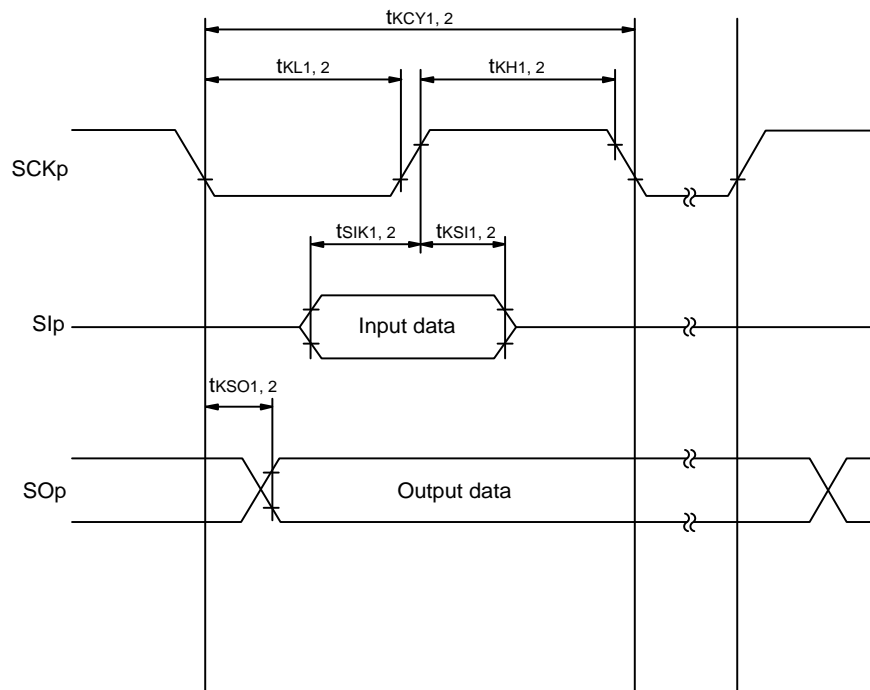
**Remark 2.** fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02))



**CSI mode connection diagram (during communication at same potential)**

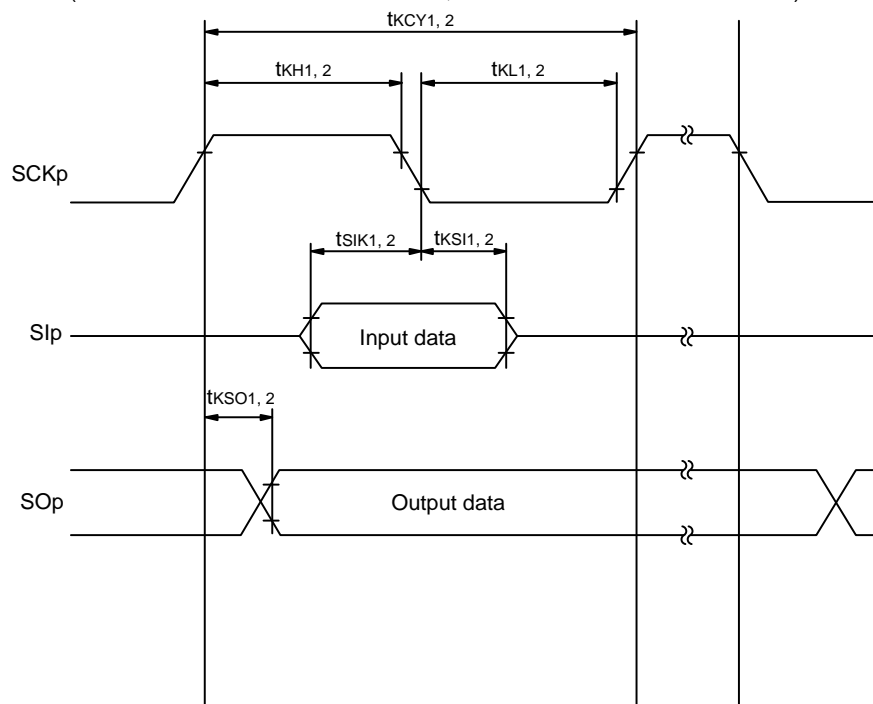
- Remark 1.** p: CSI number (p = 00, 10)
- Remark 2.** m: Unit number, n: Channel number (mn = 00, 02)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



**CSI mode serial transfer timing (during communication at same potential)**

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



**CSI mode serial transfer timing (during communication at same potential)**

**Remark 1.** p: CSI number (p = 00, 10)

**Remark 2.** m: Unit number, n: Channel number (mn = 00, 02)

(4) During communication at same potential (simplified I<sup>2</sup>C mode)

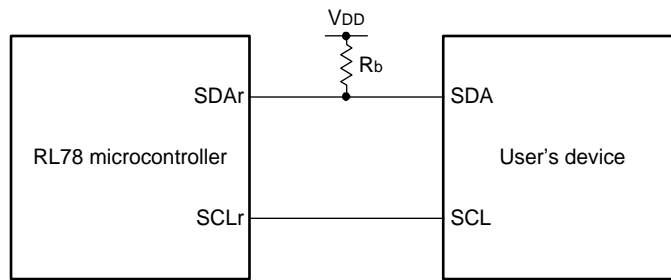
(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS ( high-speed main ) mode		LS ( low-speed main ) mode		LV ( low-voltage main ) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f <sub>SCL</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	-	1000 <sup>Note 1</sup>	-	400 <sup>Note 1</sup>	-	400 <sup>Note 1</sup>	kHz
Hold time when SCLr = "L"	t <sub>LOW</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475	-	1150	-	1150	-	ns
Hold time when SCLr = "H"	t <sub>HIGH</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	475	-	1150	-	1150	-	ns
Data setup time (reception)	t <sub>SU: DAT</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 85 <sup>Note 2</sup>	-	1/f <sub>MCK</sub> + 145 <sup>Note 2</sup>	-	1/f <sub>MCK</sub> + 145 <sup>Note 2</sup>	-	ns
Data hold time (transmission)	t <sub>HD: DAT</sub>	C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns

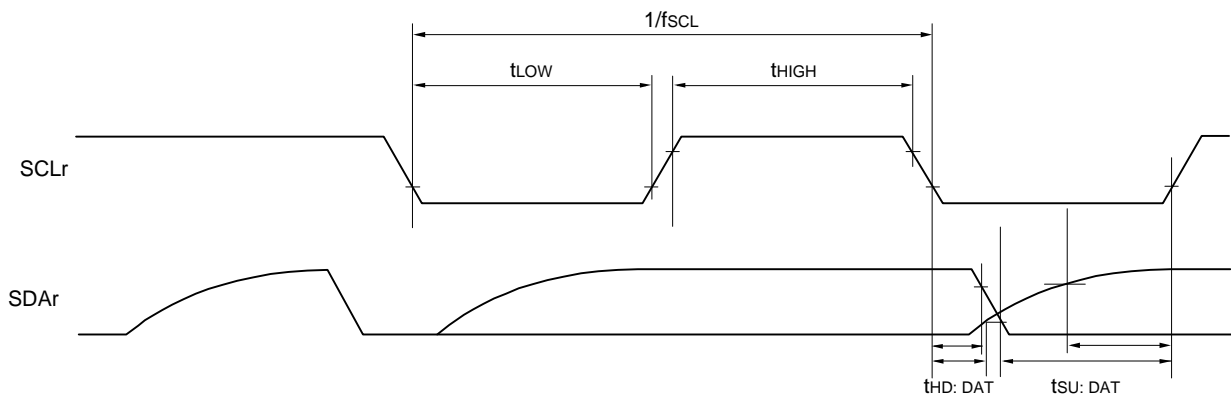
**Note 1.** The value must also be equal to or less than f<sub>MCK</sub>/4.

**Note 2.** Set the f<sub>MCK</sub> value not to over the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).



Simplified I<sup>2</sup>C mode connection diagram (during communication at same potential)



Simplified I<sup>2</sup>C mode serial transfer timing (during communication at same potential)

**Remark 1.** R<sub>b</sub>[Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 10), g: PIM number (g = 10, 13), h: POM number (h = 11, 14)

**Remark 3.** f<sub>MCK</sub>: Serial array unit operation clock frequency (Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

## 4.7.2 Serial interface IICA

### (1) I<sup>2</sup>C standard mode

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Standard mode: fCLK ≥ 1 MHz	0	100	0	100	0	100	kHz
Setup time of restart condition	tSU: STA		4.7	-	4.7	-	4.7	-	us
Hold time <sup>Note 1</sup>	tHD: STA		4.0	-	4.0	-	4.0	-	us
Hold time when SCLA0 = "L"	tLOW		4.7	-	4.7	-	4.7	-	us
Hold time when SCLA0 = "H"	tHIGH		4.0	-	4.0	-	4.0	-	us
Data setup time (reception)	tSU: DAT		250	-	250	-	250	-	ns
Data hold time (transmission) <sup>Note 2</sup>	tHD: DAT		0	3.45	0	3.45	0	3.45	us
Setup time of stop condition	tSU: STO		4.0	-	4.0	-	4.0	-	us
Bus-free time	tBUF		4.7	-	4.7	-	4.7	-	us

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ

(2) I<sup>2</sup>C fast mode(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	0	400	0	400	0	400	kHz
Setup time of restart condition	tSU: STA		0.6	-	0.6	-	0.6	-	us
Hold time <sup>Note1</sup>	tHD: STA		0.6	-	0.6	-	0.6	-	us
Hold time when SCLA0 = "L"	tLOW		1.3	-	1.3	-	1.3	-	us
Hold time when SCLA0 = "H"	tHIGH		0.6	-	0.6	-	0.6	-	us
Data setup time (reception)	tSU: DAT		100	-	100	-	100	-	ns
Data hold time (transmission) <sup>Note2</sup>	tHD: DAT		0	0.9	0	0.9	0	0.9	us
Setup time of stop condition	tSU: STO		0.6	-	0.6	-	0.6	-	us
Bus-free time	tBUF		1.3	-	1.3	-	1.3	-	us

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ

(3) I<sup>2</sup>C fast mode plus

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

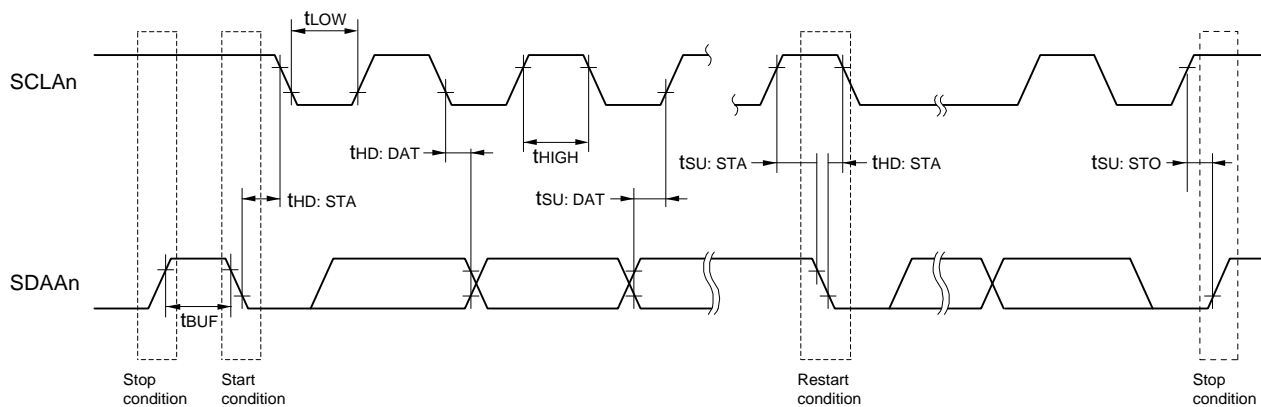
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fsCL	Fast mode plus: fCLK ≥ 10 MHz	0	1000	-	-	-	-	kHz
Setup time of restart condition	tSU: STA		0.26	-	-	-	-	-	us
Hold time <sup>Note 1</sup>	tHD: STA		0.26	-	-	-	-	-	us
Hold time when SCLA0 = "L"	tLOW		0.5	-	-	-	-	-	us
Hold time when SCLA0 = "H"	tHIGH		0.26	-	-	-	-	-	us
Data setup time (reception)	tSU: DAT		50	-	-	-	-	-	ns
Data hold time (transmission) <sup>Note 2</sup>	tHD: DAT		0	0.45	-	-	-	-	us
Setup time of stop condition	tSU: STO		0.26	-	-	-	-	-	us
Bus-free time	tBUF		0.5	-	-	-	-	-	us

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected

**Note 2.** The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ



I<sup>2</sup>C serial transfer timing

**Remark** n = 0

4.7.3 A/D converter characteristics

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI02, ANI03, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, AVREFP = VDD = CREG2, GND0 = GND1 = VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8	-	10	bits
Overall error <sup>Note 1</sup>	AINL	10-bit resolution AVREFP = VDD <sup>Note 3</sup>	-	1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin : ANI02 - ANI03	2.125	-	39	us
			3.1875	-	39	us
		10-bit resolution Target pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	2.375	-	39	us
			3.5625	-	39	us
Zero-scale error <sup>Note 1, 2</sup>	Ezs	10-bit resolution AVREFP = VDD <sup>Note 3</sup>	-	-	±0.25	%FSR
Full-scale error <sup>Note 1, 2</sup>	Efs	10-bit resolution AVREFP = VDD <sup>Note 3</sup>	-	-	±0.25	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution AVREFP = VDD <sup>Note 3</sup>	-	-	±2.5	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution AVREFP = VDD <sup>Note 3</sup>	-	-	±1.5	LSB
Analog input voltage	VAIN	ANI02 to ANI03	0	-	AVREFP	V
		Internal reference voltage (HS (high-speed main) mode)	VBGR <sup>Note 4</sup>			V
		Temperature sensor output voltage (HS (high-speed main) mode)	VTMPS25 <sup>Note 4</sup>			V

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.  
 Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.  
 Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

**Note 4.** Refer to Section 4.7.4 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = VSS (ADREFM = 0),

target pin: ANI00 to ANI03, internal reference voltage, and temperature sensor output voltage

(T<sub>A</sub> = -40 to +85C, VDD = CREG2, GND0 = GND1 = VSS = 0V, Reference voltage (+) = VDD, Reference voltage (-) = VSS)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8	-	10	bits
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	-	1.2	±7.0	LSB
Conversion time	t <sub>CONV</sub>	10-bit resolution Target pin : ANI00 to ANI03	3.1875	-	39	us
		10-bit resolution Target pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.5625	-	39	us
Zero-scale error <sup>Note 1, 2</sup>	E <sub>ZS</sub>	10-bit resolution	-	-	±0.60	%FSR
Full-scale error <sup>Note 1, 2</sup>	E <sub>FS</sub>	10-bit resolution	-	-	±0.60	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	-	-	±4.0	LSB
Differential linearity <sup>Note 1</sup>	DLE	10-bit resolution	-	-	±2.0	LSB
Analog input voltage	V <sub>AIN</sub>	ANI0 to ANI3	0	-	V <sub>DD</sub>	V
		Internal reference voltage (HS (high-speed main) mode)	V <sub>BGR</sub> <sup>Note 3</sup>			V
		Temperature sensor output voltage (HS (high-speed main) mode)	V <sub>TMPS25</sub> <sup>Note 3</sup>			V

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to Section 4.7.4 Temperature sensor characteristics/internal reference voltage characteristic.

(3) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI00, ANI02, ANI03

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V, Reference voltage (+) = VBGR <sup>Note 3</sup>, Reference voltage (-) = AVREFM = 0 V <sup>Note</sup>

<sup>4</sup>, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		bits	
Conversion time	tCONV	8-bit resolution	17	-	39	us
Zero-scale error <sup>Note 1, 2</sup>	Ezs	8-bit resolution	-	-	±0.60	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	8-bit resolution	-	-	±2.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	8-bit resolution	-	-	±1.0	LSB
Analog input voltage	VAIN		0	-	VBGR <sup>Note 3</sup>	V

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to 4.7.4 Temperature sensor characteristics/internal reference voltage characteristic.

**Note 4.** When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35 %FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

**4.7.4 Temperature sensor characteristics/internal reference voltage characteristic**(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output	VTMPS25	Setting ADS register = 80H, T <sub>A</sub> = +25°C	-	1.05	-	V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature	-	-3.6	-	mV/C
Operation stabilization wait time	tAMP		5	-	-	us

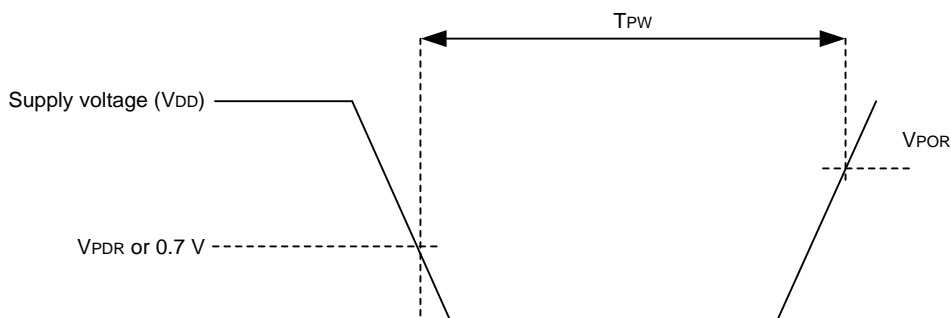
4.7.5 POR circuit characteristics (MCU)

(T<sub>A</sub> = -40 to +85°C, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V <sub>POR</sub>	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	V <sub>PDR</sub>	Voltage threshold on VDD falling <sup>Note 1</sup>	1.46	1.50	1.54	V
Minimum pulse width <sup>Note 2</sup>	T <sub>PW</sub>		300	-	-	us

**Note 1.** However, when operating voltage drops when LVD is off, it enters STOP mode, or enable the reset status using external reset pin before the voltage drops below the operating voltage range shown in Section 4.6 AC Characteristics.

**Note 2.** Minimum time required for POR to reset when VDD is below V<sub>PDR</sub>. This is also the minimum time required for a POR reset when VDD exceeds V<sub>POR</sub> after VDD is below 0.7 V during STOP mode or while the main system clock is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.7.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(T<sub>A</sub>= -40 to +85°C, V<sub>PDR</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, GND0 = GND1 = VSS= 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	V <sub>LV10</sub>	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	V <sub>LV11</sub>	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	V <sub>LV12</sub>	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V <sub>LV13</sub>	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V <sub>LV14</sub>	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V <sub>LV15</sub>	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V <sub>LV16</sub>	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V <sub>LV17</sub>	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V <sub>LV18</sub>	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V <sub>LV19</sub>	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V <sub>LV110</sub>	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V <sub>LV111</sub>	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
V <sub>LV112</sub>	Power supply rise time	1.74	1.77	1.81	V	
	Power supply fall time	1.70	1.73	1.77	V	
V <sub>LV113</sub>	Power supply rise time	1.64	1.67	1.70	V	
	Power supply fall time	1.60	1.63	1.66	V	
Minimum pulse width	t <sub>LW</sub>		300	-	-	μs
Detection delay time	t <sub>LD</sub>		-	-	300	μs

(1) Interrupt & Reset Mode

(T<sub>A</sub>= -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, GND0 = GND1 = VSS= 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Voltage detection threshold	V <sub>LVDA0</sub>	VPOC2, VPOC1, VPOC2 = 0, 0, 0, falling reset voltage	1.60	1.63	1.66	V	
	V <sub>LVDA1</sub>	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V <sub>LVDA2</sub>	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V <sub>LVDA3</sub>	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V <sub>LVDB0</sub>	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V	
	V <sub>LVDB1</sub>	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V <sub>LVDB2</sub>	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V <sub>LVDB3</sub>	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V <sub>LVDC0</sub>	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage	2.40	2.45	2.50	V	
	V <sub>LVDC1</sub>	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V <sub>LVDC2</sub>	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V <sub>LVDC3</sub>	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V <sub>LVDD0</sub>	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V	
	V <sub>LVDD1</sub>	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
V <sub>LVDD2</sub>	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	
V <sub>LVDD3</sub>	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V	
		Falling interrupt voltage	3.90	3.98	4.06	V	

## 4.8 Analog front end peripheral circuit characteristics

### 4.8.1 High-voltage port characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{V} \leq \text{VCC} \leq 40\text{V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	$V_{IH}$		2.6	-	-	V
Input voltage, low	$V_{IL}$		-	-	0.7	V
Output voltage, low	$V_{oL}$	$I_{OL} = 1\text{ mA}$	-	-	0.7	V
On resistance, Low level output (Nch MOS output)	$R_{ONN}$	$I_{OL} = 1\text{ mA}$	-	-	700	$\Omega$
Pin leakage current	$I_{LK}$	$V_I = \text{VCC}, \text{GND}$	-	-	$\pm 1$	$\mu\text{A}$

## 4.8.2 Multiplexer characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain VIN(n)-VIN(n-1)	GAIN1	VIN7,VIN6,VIN5 > 2.0 V VIN4,VIN3,VIN2,VIN1,VIN0 > 0 V <sup>Note</sup>	-	1.0	-	V/V
Gain V <sub>TOP</sub> , PON	GAIN2		-	0.1	-	V/V
Gain AN0,1,2	GAIN3		-	1.0	-	V/V
Input voltage range VIN(n)-VIN(n-1)	VRA1		-0.1	-	5.1	V
Input voltage range V <sub>TOP</sub> , PON	VRA2		0.0	-	40.0	V
Input voltage range AN0, 1, 2	VRA3		0.0	-	1.8	V
Input resistance V <sub>TOP</sub> , PON	RI1		-	250	-	KΩ
Pin leakage current	ILKV1	VIN1 = 5 V	-	-	2	μA
		VIN2 = 10 V	-	-	2	μA
		VIN3 = 15 V	-	-	2	μA
		VIN4 = 20 V	-	-	2	μA
		VIN5 = 25 V	-	-	2	μA
		VIN6 = 30 V	-	-	2	μA
		VIN7 = 35 V	-	-	2	μA

Note Reference voltage is GND0 and GND1

### 4.8.3 Sigma-delta A/D converter characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $GND0 = GND1 = VSS = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution <sup>Note1</sup>	RESAD	Conversion time = 8 ms	-	-	15	bits
		Conversion time = 4 ms	-	-	14	bits
		Conversion time = 2 ms	-	-	13	bits
		Conversion time = 1 ms	-	-	12	bits
		Conversion time = 0.5 ms	-	-	11	bits
		Conversion time = 0.25 ms	-	-	10	bits
Input voltage range	VINAD		-0.1	-	5.1	V
Integral nonlinearity	INLAD	End fit	-27	-	27	LSB
Conversion result in zero input	ADZERO	VIN = 0 V	-	3340 <sup>Note 2</sup>	-	LSB
Temperature dependency in zero input	dTADZERO	VIN = 0 V	-0.24	-	+0.24	LSB/C
Conversion result in full-scale input	ADFS	VIN = 5.1 V	-	31010 <sup>Note 2</sup>	-	LSB
Temperature dependency in full-scale input	dTADFS	VIN = 5.1 V	-0.24	-	+0.24	LSB/C
Input resistance	RINAD		-	(1.0)	-	MΩ
Battery cell voltage measurement error	ERRCELL1	$T_A = +25^\circ\text{C}$ After calibration	-	-	±5	mV
	ERRCELL2	$-20^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ After calibration	-	-	±10	mV
	ERRCELL3	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ After calibration	-	-	±12	mV

**Note 1.** AD conversion result is output in 15-bit.

**Note 2.** This value is before subtracting the offset voltage.

**Caution 1.** Except for Battery cell voltage measurement error (ERRCELL), these parameters are sigma-delta converter circuit characteristics.

**Caution 2.** Calibration is needed to keep high accuracy in system.

**Remark** Values in brackets are design value.

#### 4.8.4 Current integrating circuit characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RESCC		-	-	18	bits
Conversion time	TCC		-	250	-	ms
Input voltage range	VINCC	$\pm 50\text{ mV}$ mode ISENS1 to ISENS0	-50	-	+50	mV
		$\pm 100\text{ mV}$ mode ISENS1 to ISENS0	-100	-	+100	mV
		$\pm 200\text{ mV}$ mode ISENS1 to ISENS0	-200	-	+200	mV
Integral nonlinearity	INLCC	End fit	-	-	0.02	%FSR
Input resistance	RINCC	ISENS0, ISENS1	-	(1.0)	-	$\text{M}\Omega$
Current measurement error	ERRCURR	$\pm 50\text{ mV}$ mode, $T_A = +25^\circ\text{C}$ After calibration	-	-	( $\pm 10$ )	$\mu\text{V}$
		$\pm 50\text{ mV}$ mode, After calibration	-	-	( $\pm 60$ )	$\mu\text{V}$
		$\pm 100\text{ mV}$ mode, $T_A = +25^\circ\text{C}$ After calibration	-	-	( $\pm 10$ )	$\mu\text{V}$
		$\pm 100\text{ mV}$ mode, After calibration	-	-	( $\pm 100$ )	$\mu\text{V}$
		$\pm 200\text{ mV}$ mode, $T_A = +25^\circ\text{C}$ After calibration Input voltage range: $-100\text{ mV}$ to $200\text{ mV}$	-	-	( $\pm 20$ )	$\mu\text{V}$
		$\pm 200\text{ mV}$ mode, After calibration Input voltage range: $-100\text{ mV}$ to $200\text{ mV}$	-	-	( $\pm 200$ )	$\mu\text{V}$

**Caution 1.** Except for Current measurement error (ERRCURR), these parameters are current integration circuit characteristics.

**Caution 2.** Calibration is needed to keep high accuracy in system.

**Remark** Values in brackets are design value.

## 4.8.5 Overcurrent detection / wakeup current detection circuit characteristics

(T<sub>A</sub> = -40 to +85°C, 4.0 V ≤ VCC ≤ 40 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current detection setting voltage step	dSVSC	25 mV to 200 mV	-	12.5	-	mV
		200 mV to 300 mV	-	25	-	mV
Discharge short-circuit current detection voltage error	dVSC	25 mV to 200 mV setting	-	-	±12.5	mV
		225 mV to 300 mV setting	-	-	±25.0	mV
Discharge overcurrent detection setting voltage step	dSVD0C	15 mV to 100 mV	-	2.5	-	mV
		100 mV to 200 mV	-	5	-	mV
Discharge overcurrent detection voltage error <sup>Note 1</sup>	dVDOC	15 mV to 100 mV setting	-	-	±5.0	mV
		105 mV to 200 mV setting	-	-	±7.5	mV
Charge overcurrent detection setting voltage step	dSVCOC	-60 mV to -2.5 mV	-	2.5	-	mV
		-100 mV to -60 mV	-	5	-	mV
Charge overcurrent detection voltage error <sup>Note 1</sup>	dVCOC	-60 mV to -2.5 mV setting	-	-	±5.0	mV
		-100 mV to -65 mV setting	-	-	±7.5	mV
Discharge wakeup current detection setting voltage step	dSVDWU	0 mV to 140 mV	-	1.25	-	mV
Charge wakeup current detection setting voltage step	dSVCWU	-140 mV to 0 mV	-	1.25	-	mV
DBPT current detection setting voltage step	dSVDBPT	0 mV to 140 mV	-	1.25	-	mV
Discharge wakeup current detection voltage error <sup>Note 1</sup>	dVDWU	20 times mode ISENS1 to ISENS0: 0.25 mV to 2.5 mV	-0.10	0.0	+0.25	mV
Charge wakeup current detection voltage error <sup>Note 1</sup>	dVCWU	20 times mode ISENS1 to ISENS0: -0.25 mV to -2.5 mV	-0.25	0.0	+0.10	mV
DBPT current detection voltage error <sup>Note 1</sup>	dVDBPT	20 times mode ISENS1 to ISENS0: 0.25 mV to 2.5 mV	-0.10	0.0	+0.25	mV
Discharge short-circuit current detection time error <sup>Note 2</sup>	dTSC	0 us to 916 us (61 us step)	0.0	-	30.5	us
Discharge overcurrent detection time error <sup>Note 2</sup>	dTDOC	0.488 ms to 32 s (0.488 ms step)	0.0	-	122	us
Charge overcurrent detection time error	dTCOC	0 us to 15564 us (61 us step)	0.0	-	30.5	us
Discharge wakeup current detection time error <sup>Note 2</sup>	dTDWU	3.91 ms to 62.56 ms (61 us step)	-3.91	-	0	ms
Charge wakeup current detection time error <sup>Note 2</sup>	dTCWU	3.91 ms to 62.56 ms (61 us step)	-3.91	-	0	ms
DBPT current detection time error <sup>Note 2</sup>	dTDBPT	0 us to 916 us (61 us step)	0.0	-	30.5	us

**Note 1.** This is the specification after zero-calibration is executed.**Note 2.** The frequency error of On-chip oscillator (AOCO and ALOCO) is excluded from these detection time error.

## 4.8.6 Charge/discharge FET control circuit characteristics

(T<sub>A</sub> = -40 to +85°C, 4.0 V ≤ VCC ≤ 40 V, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-side Discharge/Charge FET control Output voltage, C <sub>FOUT</sub> /D <sub>FOUT</sub> = H	FON1	4.0 ≤ VCC < 10.0 V Load resistance = 10 MΩ Based on GND0/1 pin T <sub>A</sub> = 0 to +60°C	3	-	-	V
		4.0 ≤ VCC < 10.0 V Load resistance = 10 MΩ Based on GND0/1 pin T <sub>A</sub> = -40 to +85°C	2.9	-	-	V
	FON2	10.0 ≤ VCC Load resistance = 10 MΩ Based on GND0/1 pin	8.0	10	12.0	V
Low-side Discharge/Charge FET control Output voltage, C <sub>FOUT</sub> /D <sub>FOUT</sub> = L	FOFF	Load capacitance = 50 nF Based on GND0/1 pin	-0.1	-	+0.1	V
Low-side Discharge FET control C <sub>FOUT</sub> /D <sub>FOUT</sub> rise Time	FTR1	4.0 V ≤ VCC < 7.0 V Load capacitance = 50 nF Resistor between Gate and C <sub>FOUT</sub> /D <sub>FOUT</sub> pin = 200 ohm Lo(GND) → Hi(2.5 V)	-	1.5	3.0	ms
	FTR2	7.0 V ≤ VCC < 10.0 V Load capacitance = 50 nF Resistor between Gate and C <sub>FOUT</sub> /D <sub>FOUT</sub> pin = 200 ohm Lo(GND) → Hi(4 V)	-	1.0	2.0	ms
	FTR3	10.0 V ≤ VCC Load capacitance = 50 nF Resistor between Gate and C <sub>FOUT</sub> /D <sub>FOUT</sub> pin = 200 ohm Lo(GND) → Hi(4 V)	-	0.4	0.8	ms
Low-side Discharge FET control D <sub>FOUT</sub> fall Time	DFTF	Load capacitance = 50 nF Resistor between Gate and D <sub>FOUT</sub> pin = 200 ohm Hi(F <sub>LON1</sub> , F <sub>LON2</sub> ) → Lo(1 V)	-	0.1	0.3	ms
Low-side Charge FET control C <sub>FOUT</sub> fall Time	CFTF	Load capacitance = 50 nF Resistor between Gate and C <sub>FOUT</sub> pin = 200 ohm Hi(F <sub>LON1</sub> , F <sub>LON2</sub> ) → Lo(1 V)	-	0.7	1.4	ms

**Caution** After trimming.

### 4.8.7 Power on circuit characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, High	$V_{IH}$	PON	2.6	-	VCC	V
Input voltage, Low	$V_{IL}$	PON	0.0	-	0.7	V
Pull-down resistance	Rdpon1		-	12.4	-	M $\Omega$
	Rdpon2	PONPDEN bit of PINSEL register = 1	-	50	-	K $\Omega$

**Caution** To entry power down mode, it is necessary to input power down command while PON port is L.

### 4.8.8 Series regulator circuit characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	VR2O	$I_o = 50\text{ }\mu\text{A}$ to $20\text{ mA}$	3.20	3.30	3.40	V
Load drive capability <sup>Note</sup>	IOMAX	$4.0\text{ V} \leq V_{CC} < 5.0\text{ V}$	10.0	-	-	mA
		$5.0\text{ V} \leq V_{CC} \leq 40.0\text{ V}$	20.0	-	-	mA

**Note** In case of using load drive, total power consumption must be under the maximum ratings power consumption ( $P_d$ ).

**Caution** After trimming.

### 4.8.9 AFE reset circuit characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 release voltage	VREL		2.8	2.9	3.0	V
VREG2 detection voltage	VDET	After trimming	2.7	2.8	2.9	V

### 4.8.10 Cell balancing circuit characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $4.0\text{ V} \leq V_{CC} \leq 40\text{ V}$ ,  $\text{GND0} = \text{GND1} = \text{VSS} = 0\text{ V}$ )

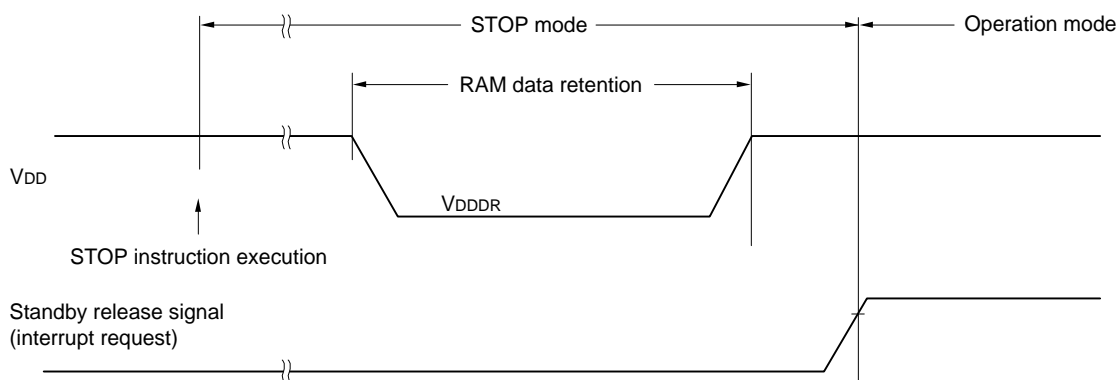
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
1st cell on resistance	RCOND1	$V_{IN1} - V_{IN0} = 3.5\text{ V}$	-	100	200	$\Omega$
2nd cell on resistance	RCOND2	$V_{IN2} - V_{IN1} = 3.5\text{ V}$	-	100	200	$\Omega$
3rd cell on resistance	RCOND3	$V_{IN3} - V_{IN2} = 3.5\text{ V}$	-	100	200	$\Omega$
4th cell on resistance	RCOND4	$V_{IN4} - V_{IN3} = 3.5\text{ V}$	-	100	200	$\Omega$
5th cell on resistance	RCOND5	$V_{IN5} - V_{IN4} = 3.5\text{ V}$	-	100	200	$\Omega$
6th cell on resistance	RCOND6	$V_{IN6} - V_{IN5} = 3.5\text{ V}$	-	100	200	$\Omega$
7th cell on resistance	RCOND7	$V_{IN7} - V_{IN6} = 3.5\text{ V}$	-	100	200	$\Omega$

### 4.9 RAM Data Retention Characteristics

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 <sup>Note</sup>	-	5.5	V

**Note** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



### 4.10 Flash Memory Programming Characteristics

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK		1	-	32	MHz
Number of code flash rewrites <sup>Note 1, 2, 3</sup>	C <sub>erwr</sub>	Retained for 20 years T <sub>A</sub> = 85°C	1,000	-	-	Times
Number of data flash rewrites <sup>Note 1, 2, 3</sup>		Retained for 1 year T <sub>A</sub> = 25°C	-	1,000,000	-	
		Retained for 5 years T <sub>A</sub> = 85°C	100,000	-	-	
		Retained for 20 years T <sub>A</sub> = 85°C	10,000	-	-	

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retained years are until next rewrite completion.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

### 4.11 Dedicated Flash Memory Programmer Communication (UART)

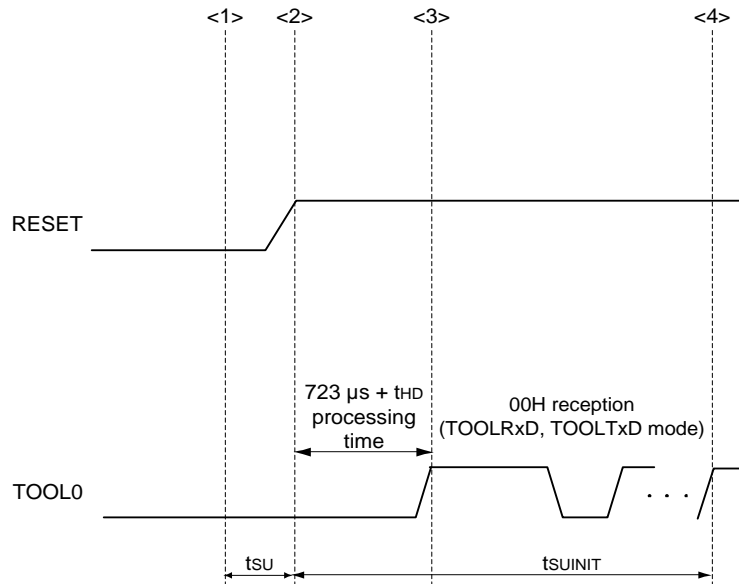
(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200	-	1,000,000	bps

4.12 Timing of Entry to Flash Memory Programming Modes

(T<sub>A</sub> = -40 to +85°C, VDD = CREG2, GND0 = GND1 = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
The time needed when an external reset ends until the initial communication settings are specified	tsUNIT	POR and LVD reset must end before the external reset ends.	-	-	100	ms
The time needed from when the TOOL0 pin is placed at low level until an external reset ends	tsU	POR and LVD reset must end before the external reset ends.	10	-	-	us
The time needed for the TOOL0 pin must be kept at low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1	-	-	ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the external reset ends).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** tsUNIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsU: Time needed for the TOOL0 pin is placed at low level until the pin reset ends

tHD: Time needed for the TOOL0 pin at low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

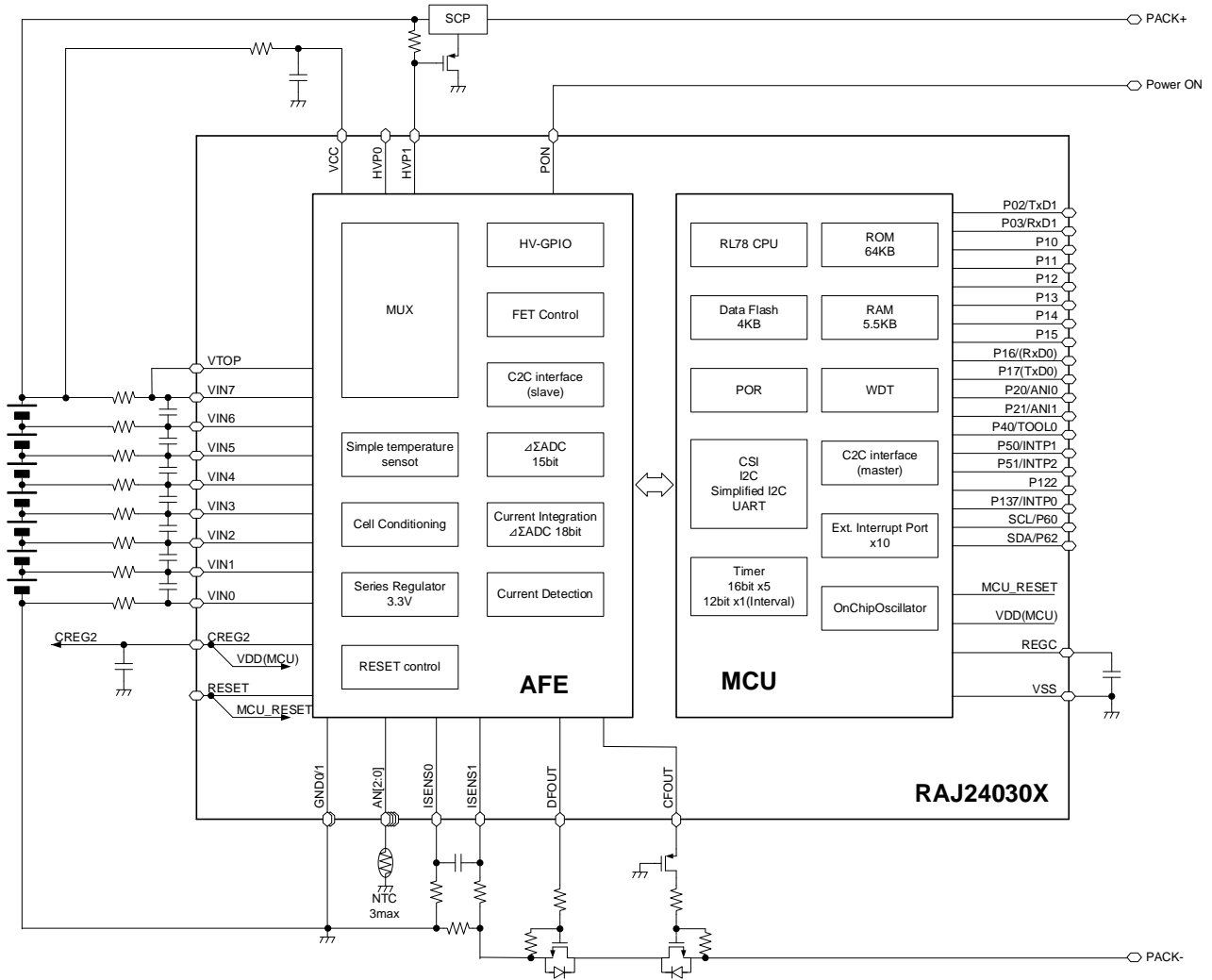
CHAPTER 5. DETAILED DESCRIPTION

5.1 Overview

RAJ240301 is Renesas Li-ion battery fuel gauge IC (FGIC) which consist of a MCU device and an AFE device in a single package. This device integrates a variety of battery management features.

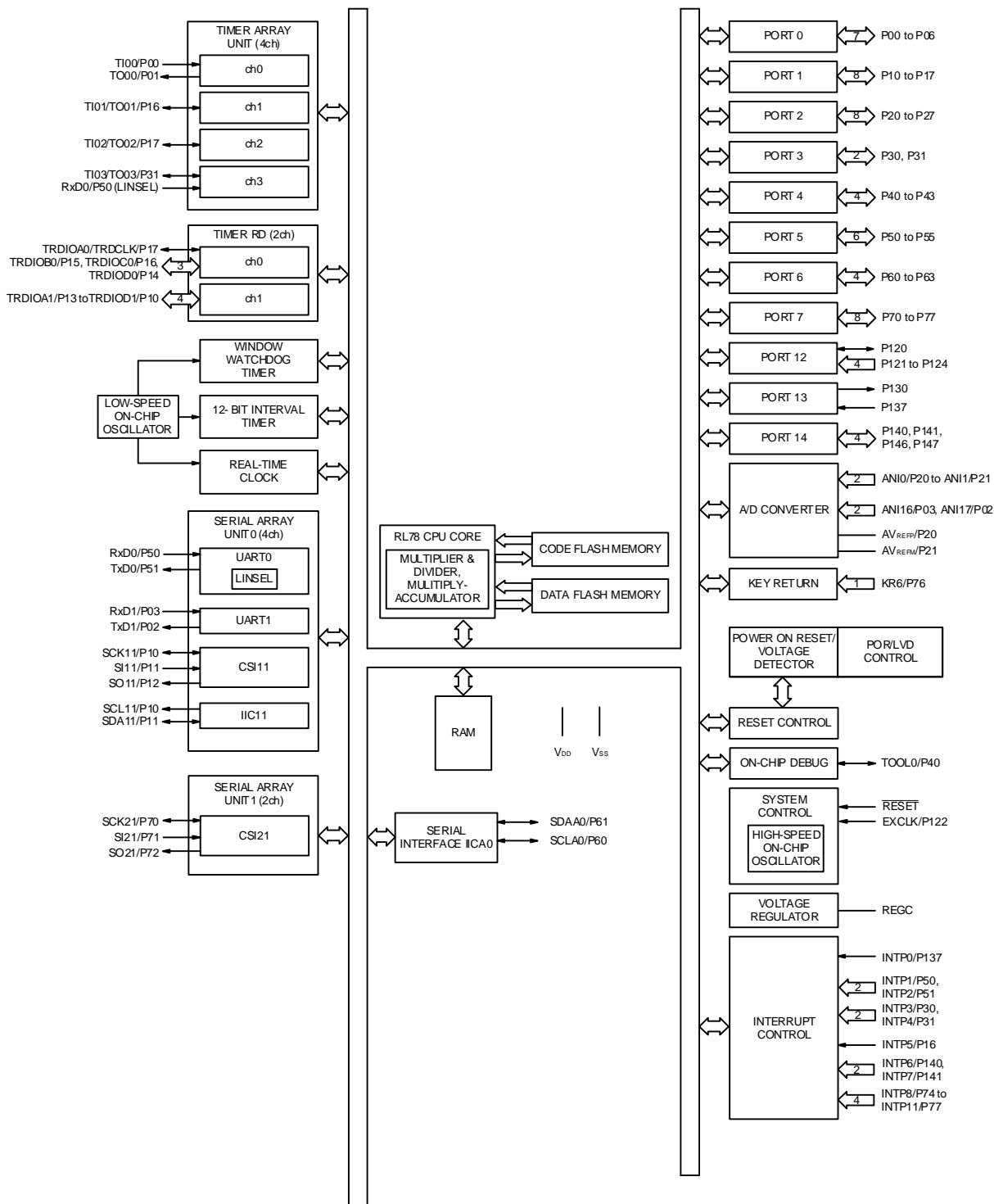
5.2 Block diagram

5.2.1 System block diagram



**Caution** This example of a peripheral circuit does not guarantee the operation of this device. Evaluate the operation adequately with actual applications, and then determine the circuits and constants.

5.2.2 MCU block diagram

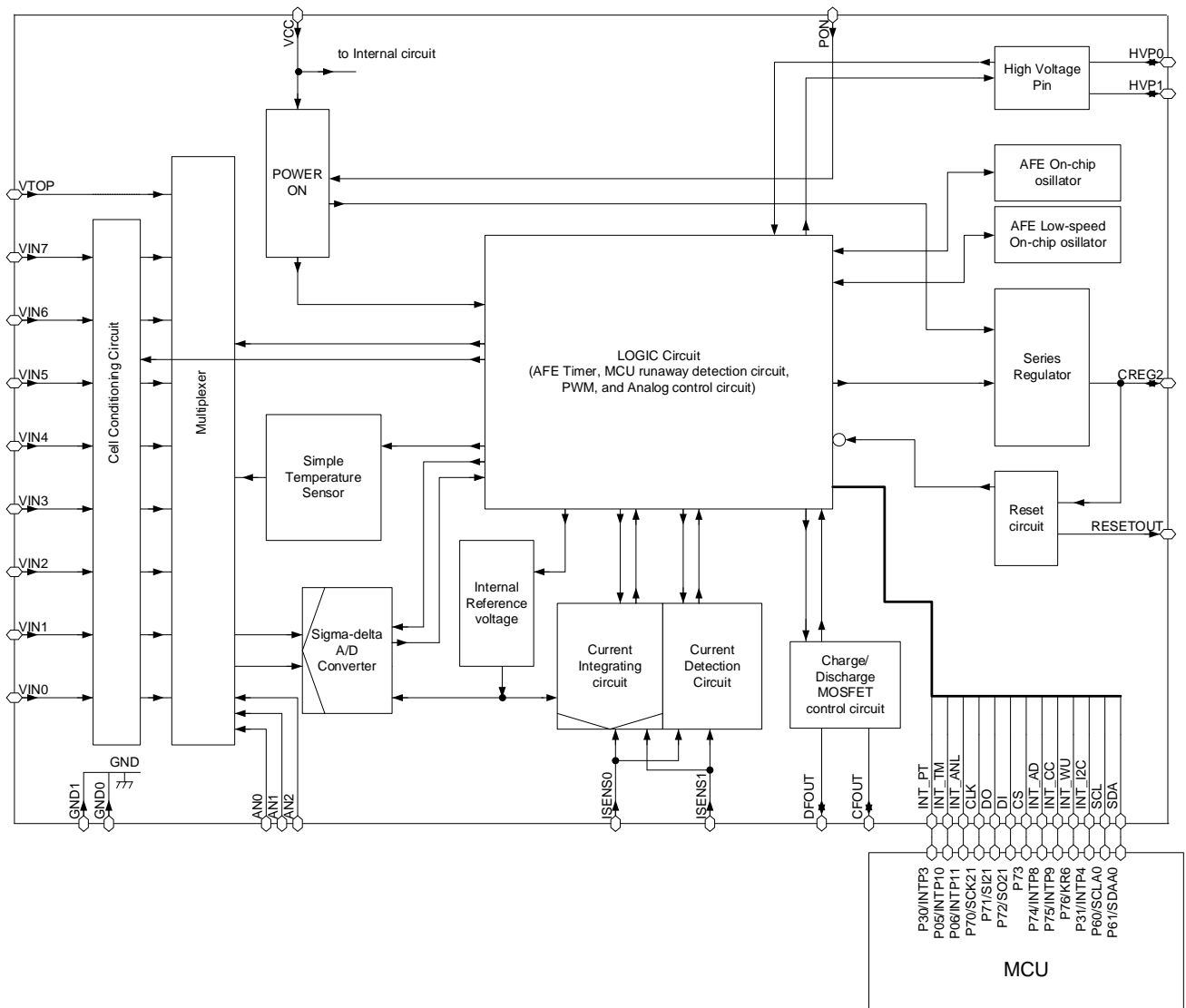


**Caution 1.** P05, P06, P30, P31, P70 to P76 are connected to AFE chip in the package and not connected to the package external pin.

**Caution 2.** Each interrupt request of AFE is assigned to INTP3/P30, INTP4/P31, INTP8/P74, INTP9/P75, INTP10/P05, INTP11/P06 and KR6/P76.

**Caution 3.** P00, P01, P04, P22 to P27, P41 to P43, P52 to P55, P62, P63, P77, P120, P121, P123, P124, P130, P140 to P147 is not connected anywhere.

5.2.3 AFE block diagram



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## CHAPTER 6. APPLICATION GUIDELINE

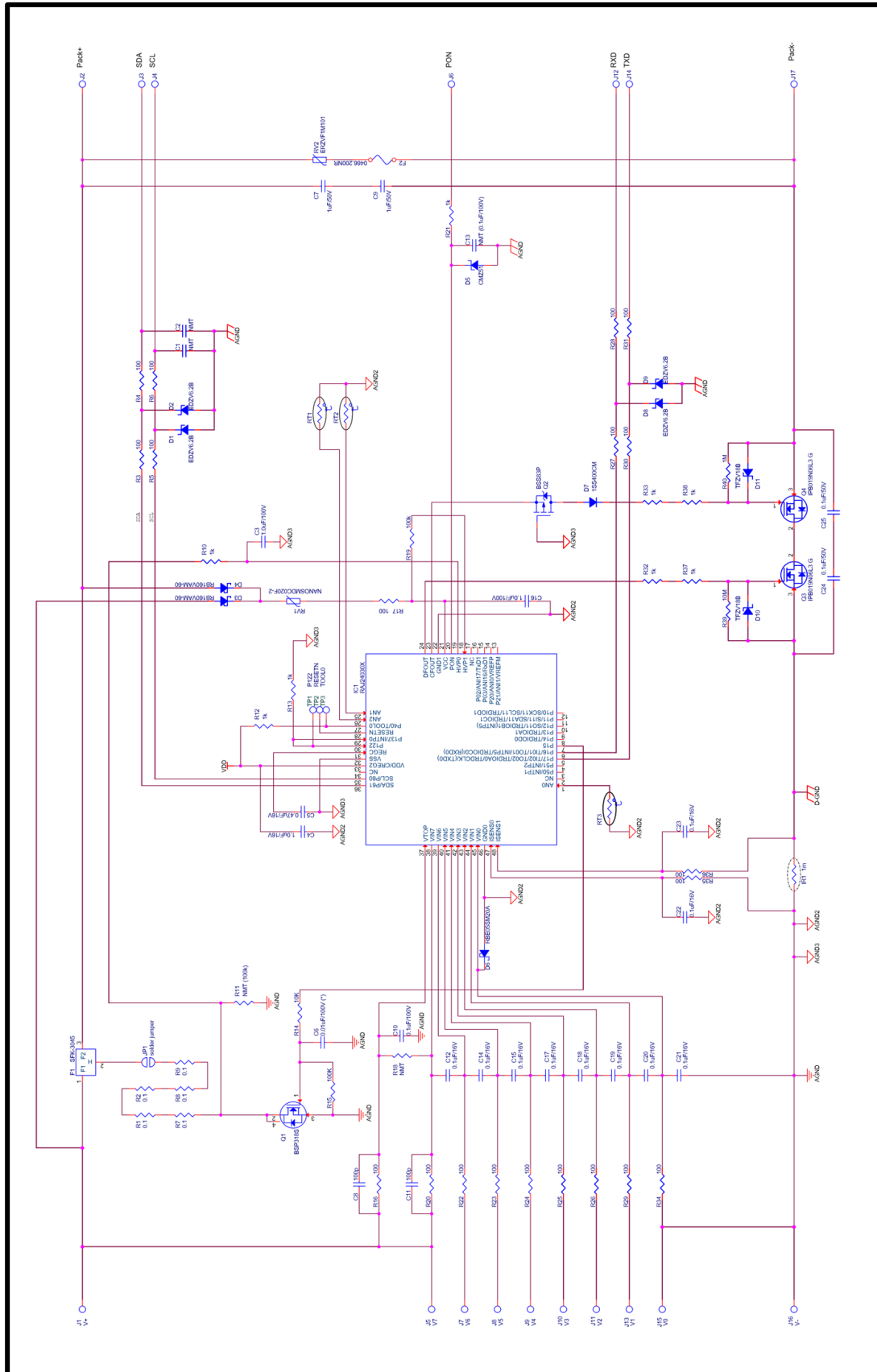
### 6.1 Typical Application Specification

A typical specification example of Li-ion battery management unit as shown below.

From the next page, the typical application guideline is explained for RAJ240301.

Battery cell assembly	7S1P	
Host Interface	System Management Bus (SMBus) Specification, version 1.1. UART	
Primary protection	Charge FET and Discharge FET	
Secondary protection	Fuse blow by FGIC or a secondary protection device	
Connect pins	Pack+	Positive battery pack terminal
	SCL	SMBus clock
	SDA	SMBus data
	TXD	UART transmit data
	RXD	UART receive data
	PON	High voltage port for battery power on
	Pack-	Negative battery pack terminal
Additional Features	External reverse charge protection circuit Battery and charge/discharge MOSFET temperature measurement with three thermistors	

### 6.2 Typical Application Circuit

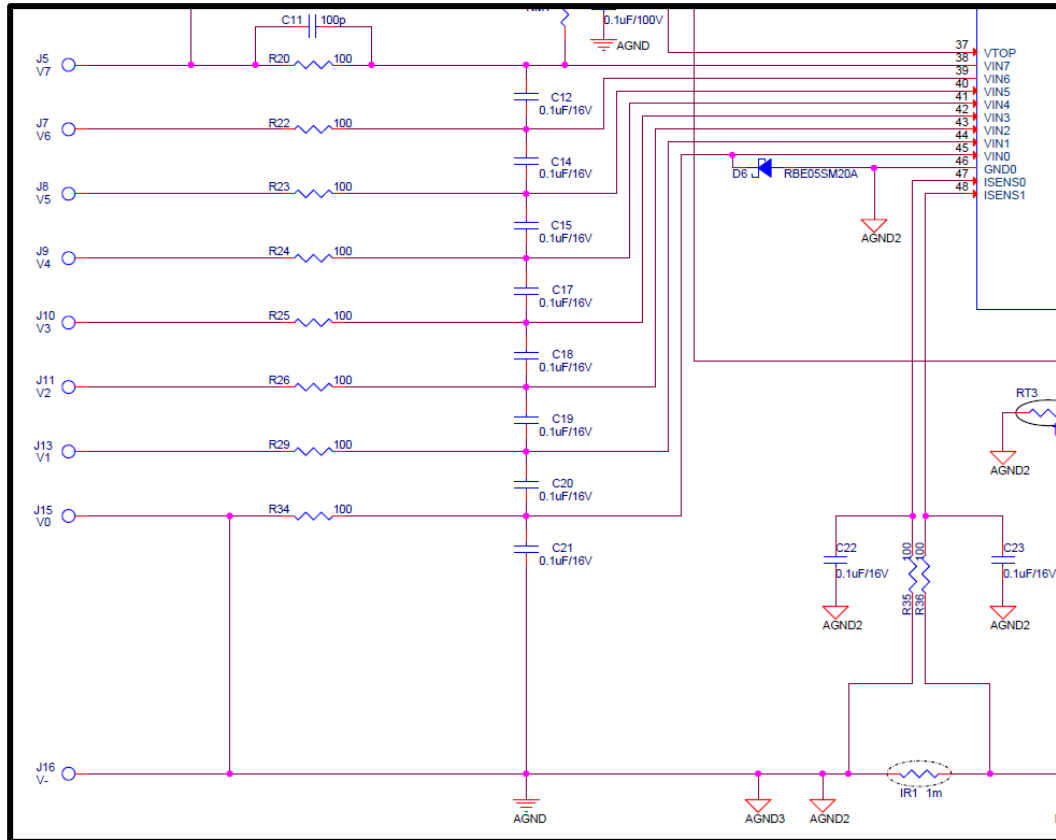


### 6.3 Circuit Design Guideline

#### 6.3.1 Cell voltage monitor circuit

- Place an input filter between FGIC's VIN pins and each of the cells.
- Place resistors valued 100 Ω and capacitors valued 0.1 uF to VIN0 – VIN7 pins for surge protection.

It is necessary to calculate the cut-off frequency and use correct resistance and capacitance value based on application.



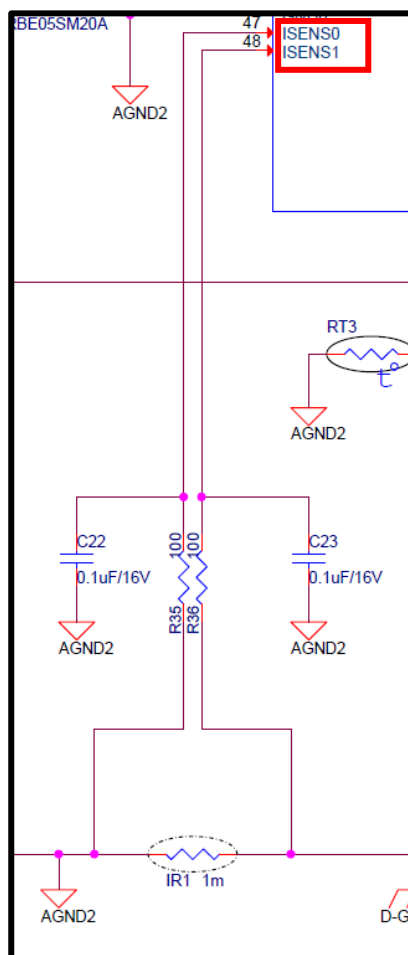
### 6.3.2 Battery power on circuit

- Place resistors value around 1 kΩ, capacitor 0.1 uF and zener diode to PON for surge protection. It is necessary to calculate cut-off frequency and use correct resistance and capacitance value based on application.



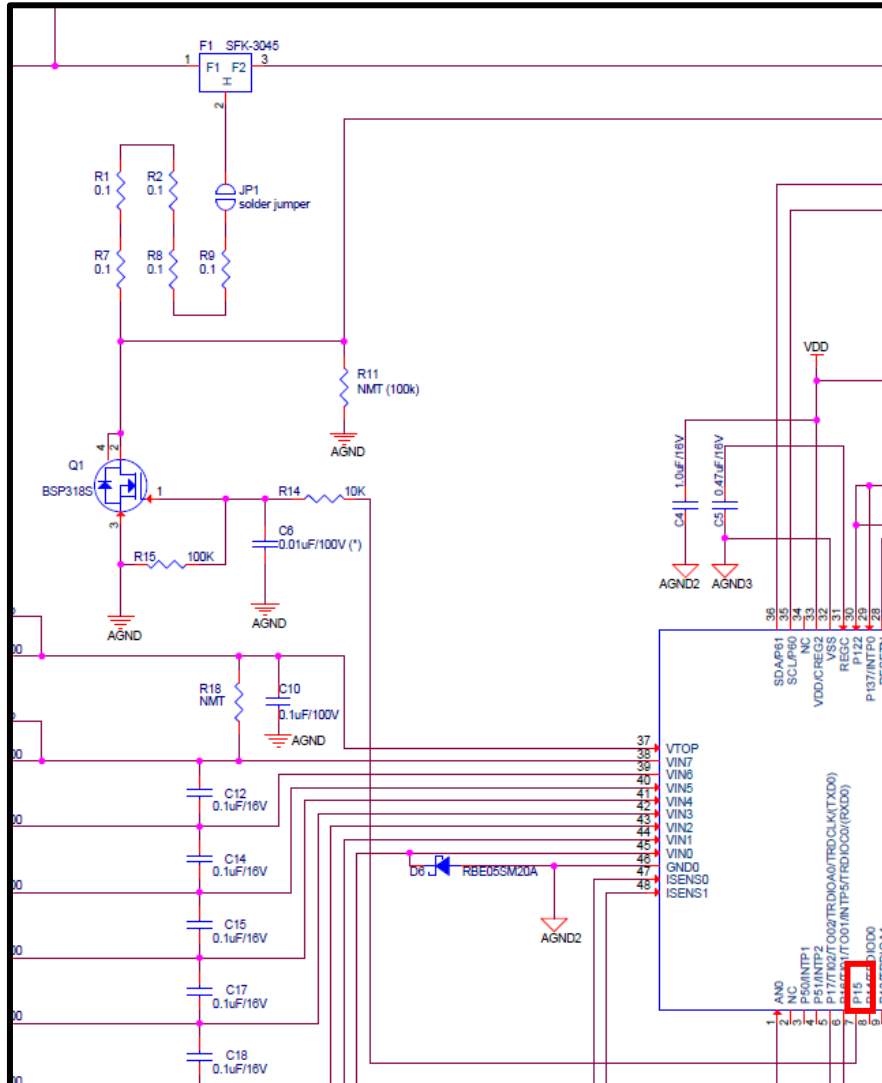
### 6.3.3 Current monitor

- Potential difference on the sense resistor is monitored by current integrating circuit.
- Place a Low Pass Filter (100 Ω, 0.1 uF) at input stage. LPF's ground should be connected from a place close to FGIC ground (GND0/1).
- Sense lines should be shielded if small voltage difference is detected to ensure high accurate current sensing.



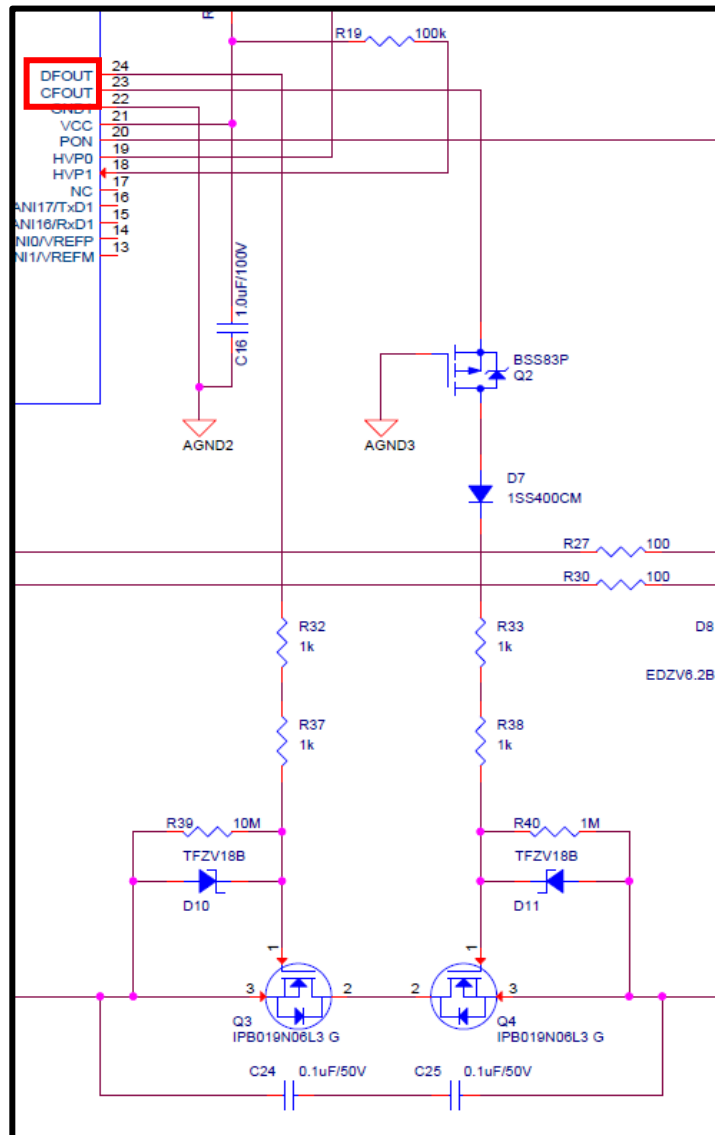
6.3.4 Fuse control

- Self-control protector (SCP) is used for fuse in reference circuit.
- The fuse will blow when RAJ240301 drives P15 pin high to make Q1 ON.
- The fuse will blow when overcurrent exceeds the limit of SCP.
- R1, R2 and R7 – R9 are used for battery electrochemical migration short circuit countermeasures.



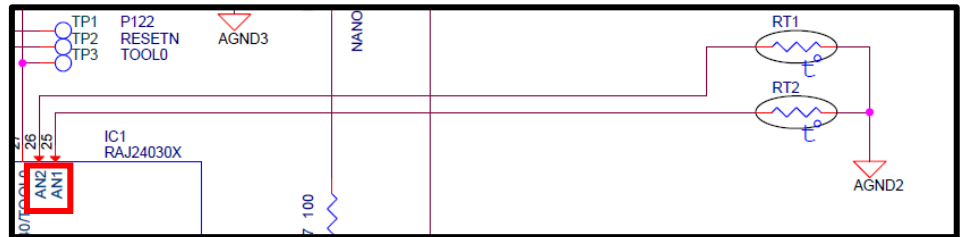
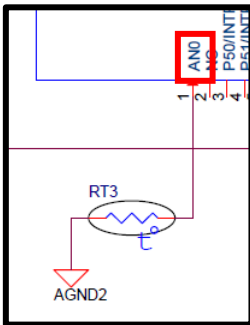
6.3.5 C-FET and D-FET control

- R32, R37 and R33, R38 are placed for gate protection and C-FET/D-FET noise reduction. 2 kΩ is recommended.
- R39 and R40 are placed to fix C-FET/D-FET gate voltage in order to keep stable off when FET state is off. 10MΩ is recommended for D-FET control and 1MΩ is recommended for C-FET control to prevent voltage drop.
- D10 and D11 is for D-FET and C-FET protection.
- Q2 is used for negative voltage protection and D7 is used to prevent reverse input from the system..



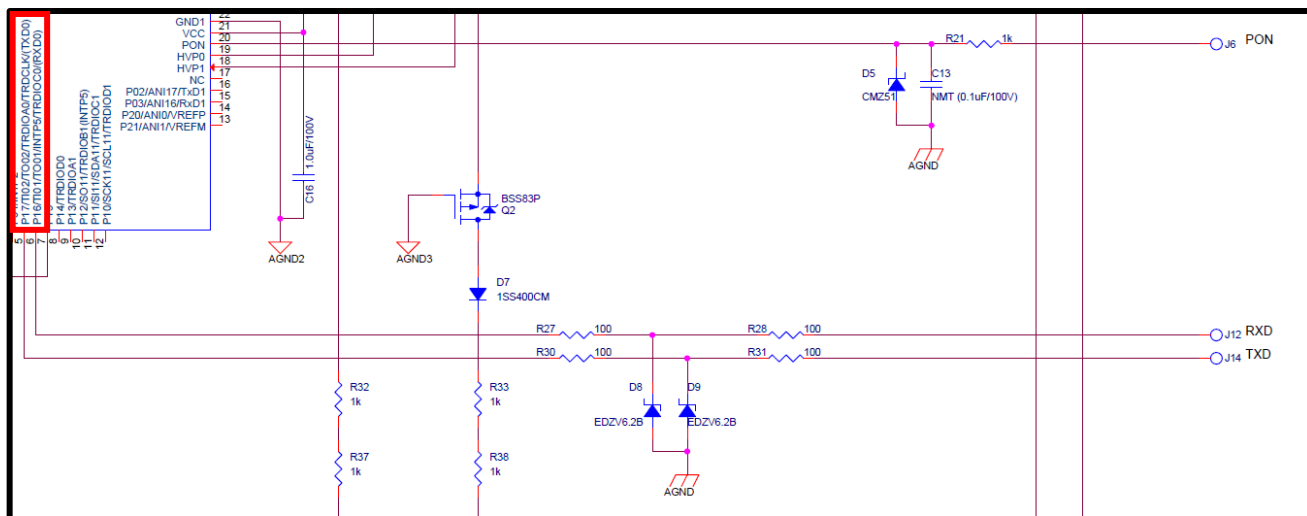
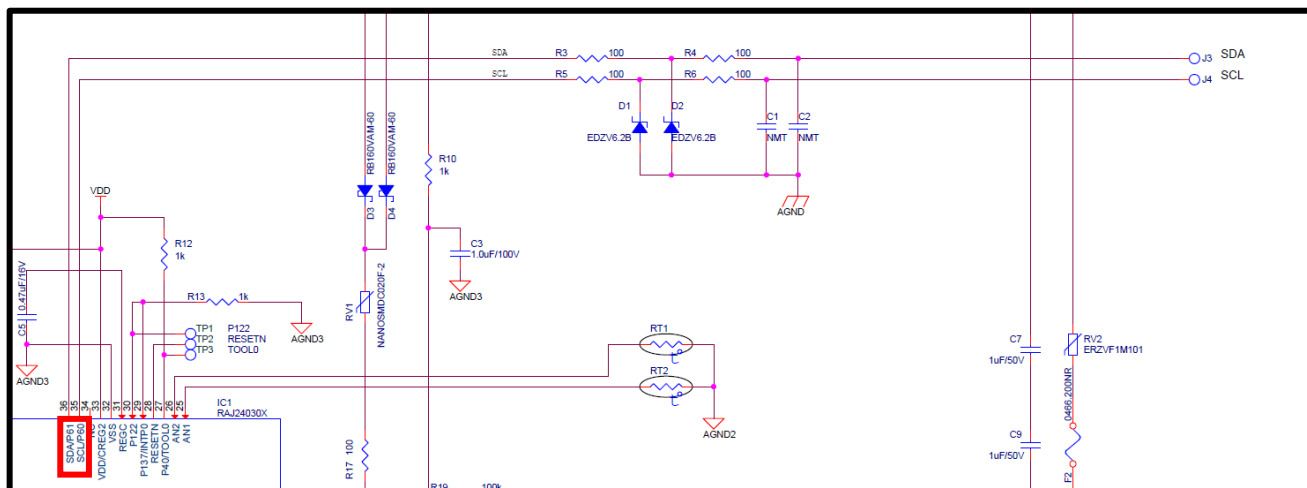
### 6.3.6 Thermistor

- ADC voltage measurement pins (AN0, AN1, AN2) are assigned for thermistor.



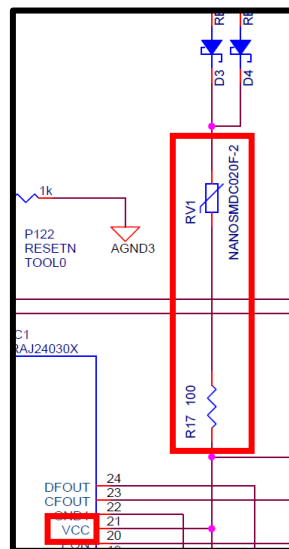
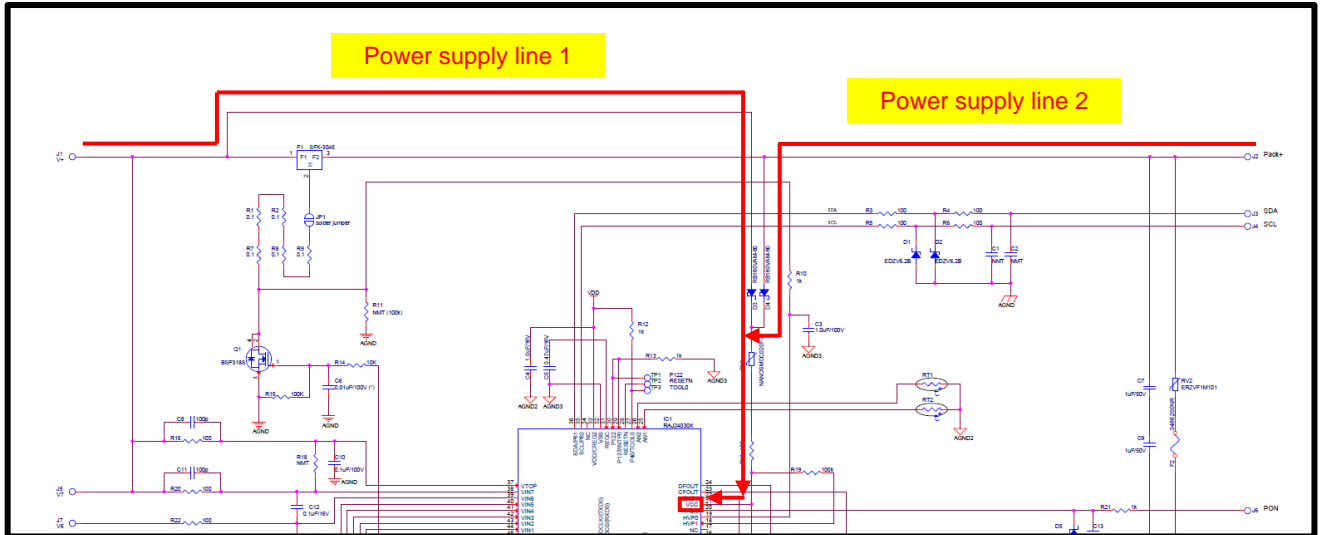
### 6.3.7 Communication line

- RAJ240301 support 2 kinds of communication, SMBus and UART.
- For electrical over stress countermeasure, input 100Ω, 100Ω resistor, Zener diode, and capacitance are recommended in SMBus communication line. The zener voltage must be less than 6.5V, an absolute maximum rating of CREG2 pin.
- For UART communication, P16 and P17 pins have VDD output circuit, therefore RXD/TXD line pull up voltage should be the same as VDD.



### 6.3.8 Power supply path

- Power is supplied to VCC pin through the following two paths depending on circumstance.
- Power supplied from battery side when fuse is blown. See power supply line 1.
- Higher output voltage from battery and charger is used as power supply. See power supply line 2.
- For protection of the VCC pin, it is recommended to add resistor and PTC for current limit.



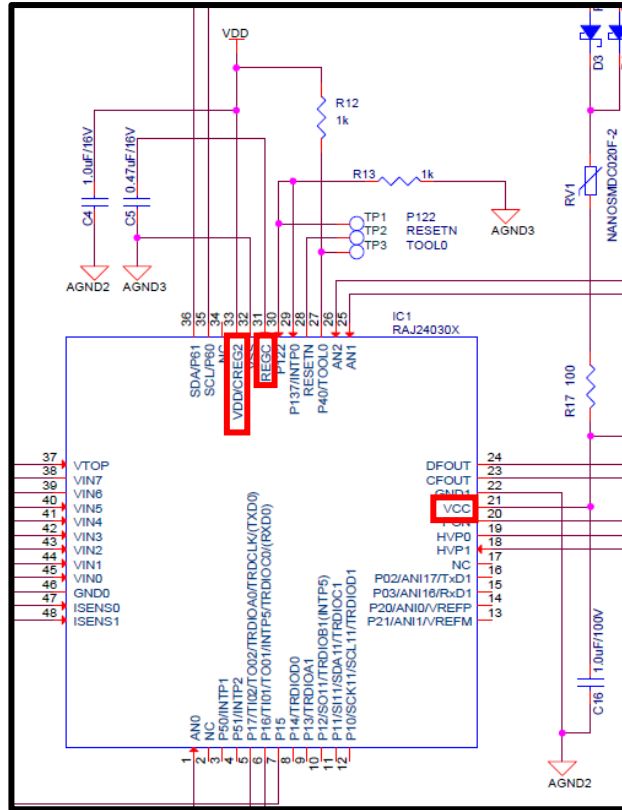
6.3.9 VCC, CREG2, REGC capacitance

- The following decoupling capacitors must be placed adjacent to each pin.

C16: VCC to AGND2 (1 uF is recommended.)

C4: CREG2 to AGND2 (1 to 4.7 uF is recommended.)

C15: REGC to AGND3 (0.47 to 1 uF is recommended.)



## 6.4 Layout Guidelines

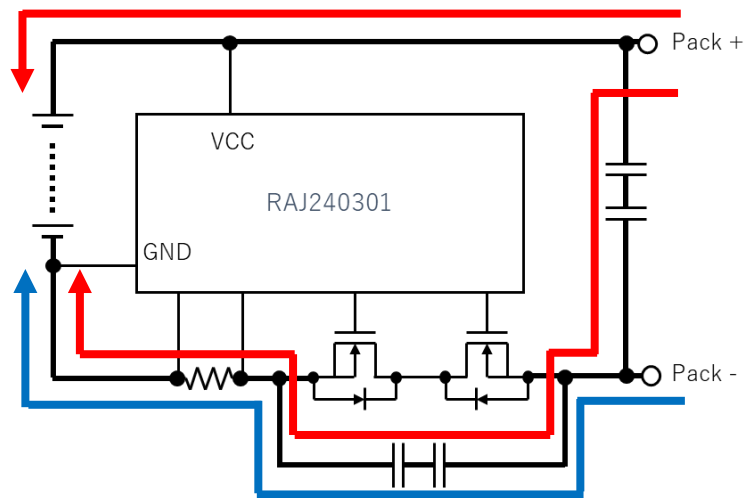
### 6.4.1 Summary

- Large current pattern should be wide and short to minimize voltage drop and heat generation.
- Decoupling capacitor must be placed as close as possible to the device VCC and GND pins to prevent erroneous operation due to noise from power supply.
- Capacitors for voltage regulators must be placed close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- To decrease parasitic PCB impedance and improve tolerance against noise, it is preferred to enhance ground pattern as much as possible.
- FGIC (RAJ240301) must be placed away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.

**6.4.2 ESD protections on each terminal (basic policy)**

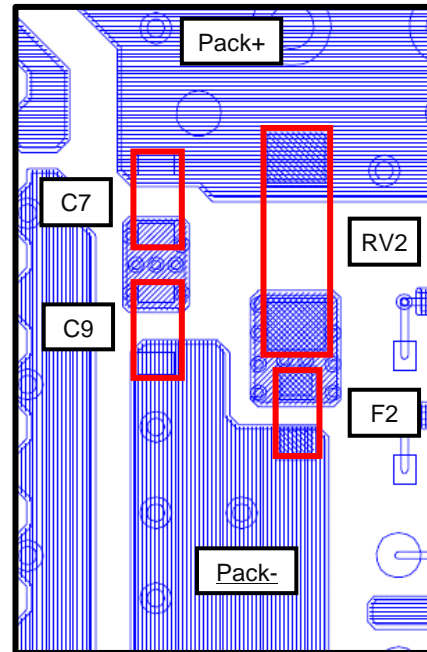
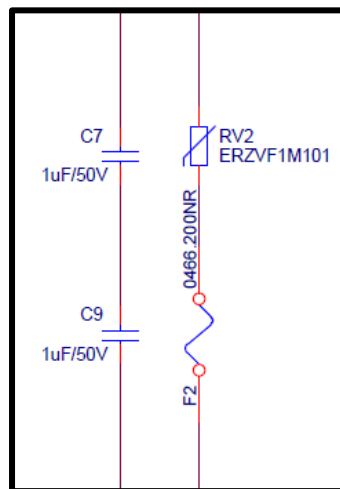
- ESD on Pack+ terminal must be discharged to the top side of the cell or to Pack- terminal through a capacitor.
- ESD on Pack- terminal must be discharged to the GND side of the cell.
- ESD on communication terminals and other GPIOs must be discharged to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- terminal must be discharged to the battery cells so that it will not interfere with FGIC functions and measurements.
- Sufficient current capacity in the power line is required to effectively discharge ESD noise.

Power line: Pack+ terminal to the top side of the cell, Pack- terminal to the GND side of the cell, etc.



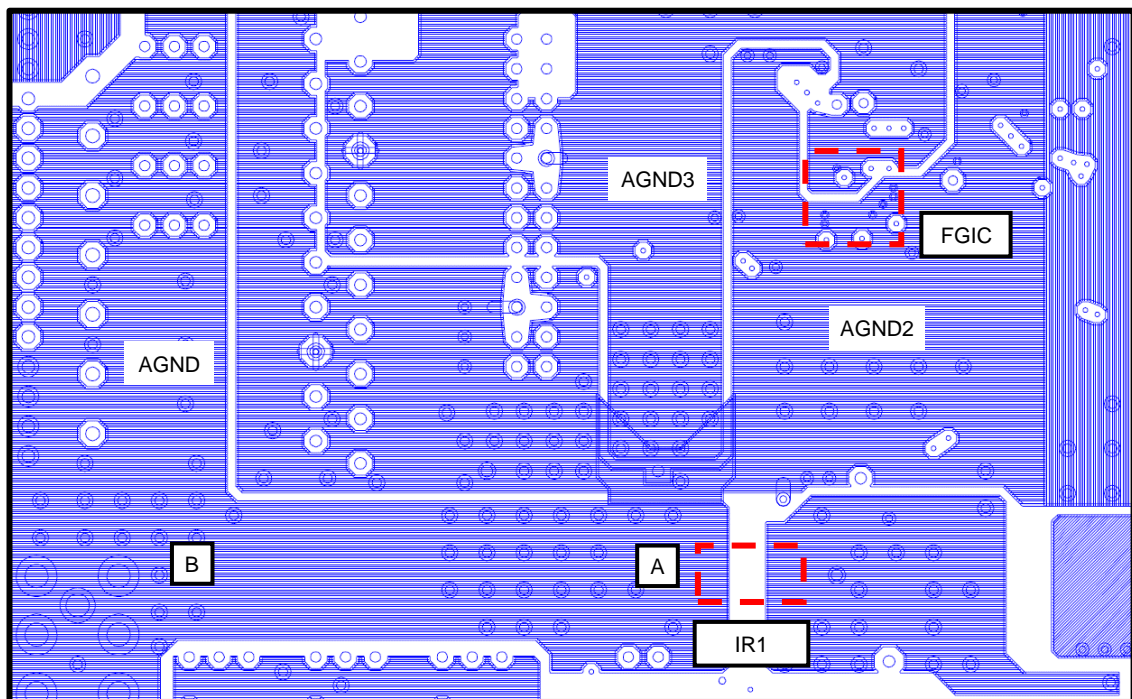
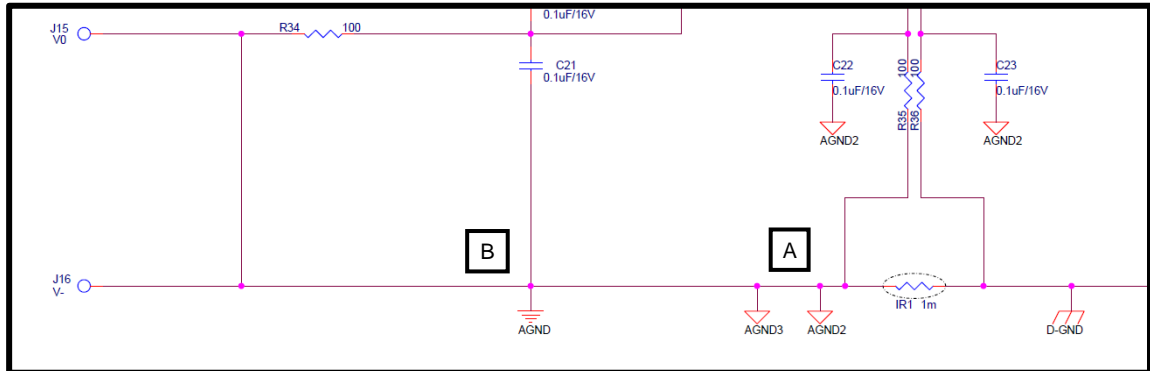
### 6.4.3 Pack+, Pack- (Noise protection element)

- Bypass capacitors must be placed across Pack+ and Pack- terminals. (Countermeasure against ESD)
- Bypass capacitors must be placed adjacent to Pack+ and Pack- terminals. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don't use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)
- For the terminal protection against noise and overvoltage, it is recommended to add varistor or TVS diode. (RV2)
- It is recommended to add Fuse to prevent short circuit. (F2)
- C7, C9, RV2, F2 must be placed as short as possible between PACK + and PACK-. However, be careful not to narrow the distance between Pack + and Pack-.



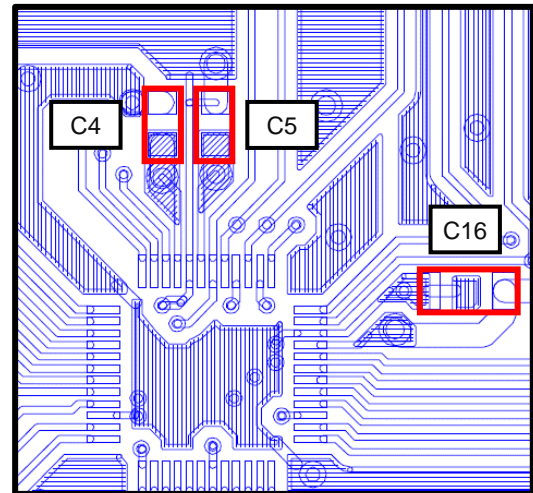
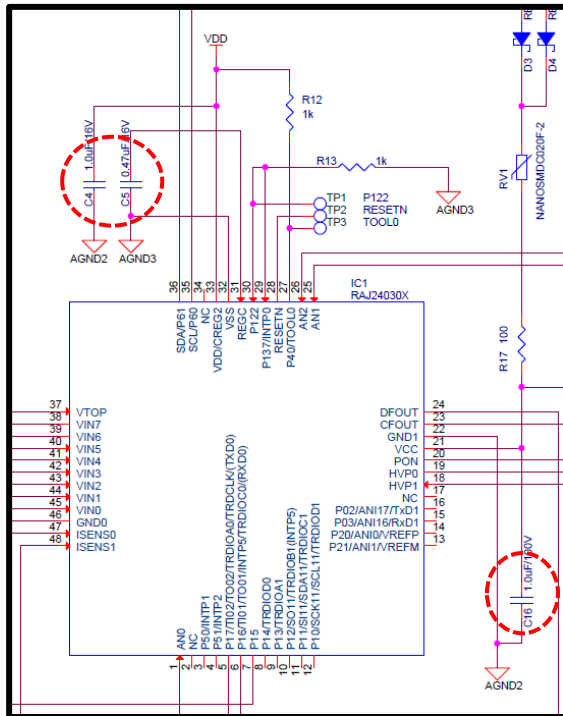
6.4.4 GND connection

- Each analog GND of FGIC should be connected to the point (A) of the cell- side by the pattern with an adequate width. (Prevent potential variation by large current.)
- Minimize parasitic impedance between point (A) and (B).
- Minimize parasitic impedance between GND0 and GND1 pins.
- VIN0 should be connected near point V0 (B).
- The pattern from GND0, GND1 and VSS pins to AGND, AGND2 and AGND3 should not be diverged on the way, nor be connected to the other GND. (Keeping the GND potential of MCU and AFE equal)



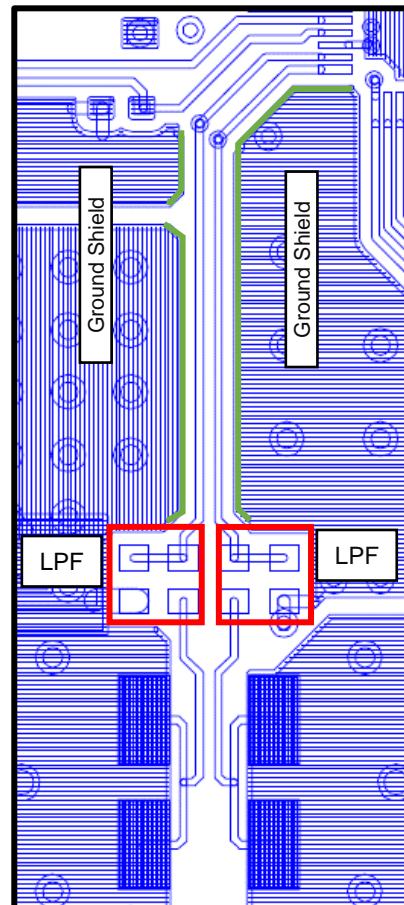
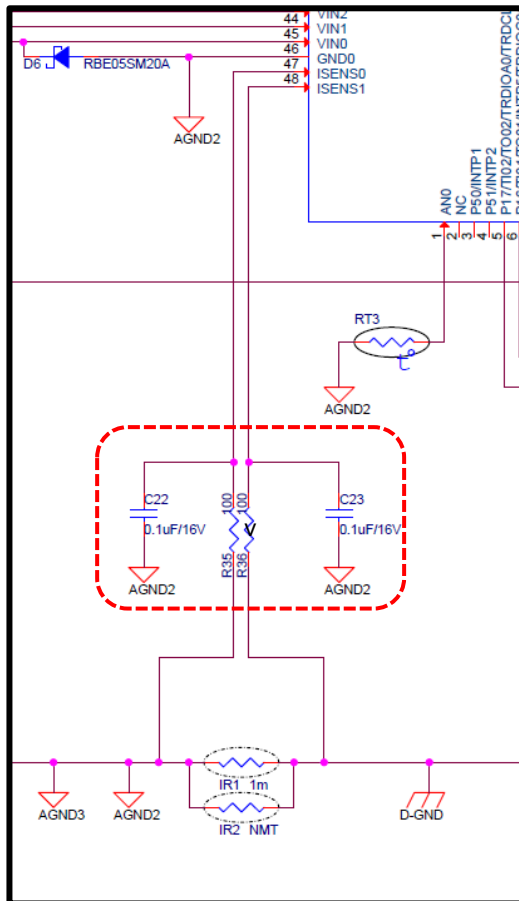
6.4.5 Bypass capacitor between VCC/CREG2/REGC and GND0/GND1/VSS

- The patterns between VCC/CREG2 pin and GND0/GND1 pin, and between REGC pin and VSS pin, a bypass capacitor is connected and the path must be as short as possible. (Countermeasure for ESD, EMC noise and etc.)  
The FGIC and bypass capacitors must be placed on the same side of the PCB without through-holes.
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)



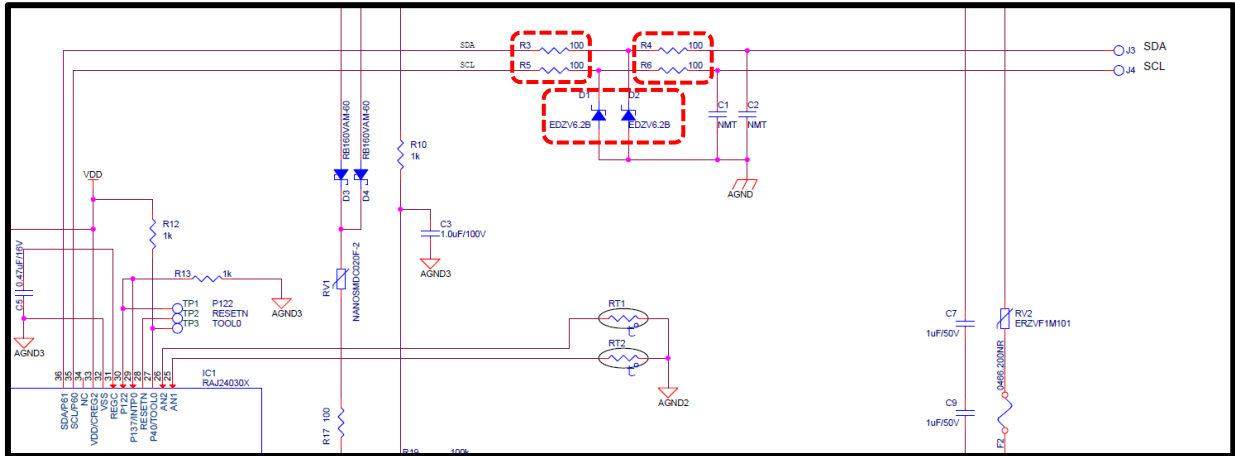
6.4.6 Current Monitor (ISENS0, ISENS1)

- Two lines from current sense resistor to ISENS0, ISENS1 pins must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise).
- Both sides of the 2 lines from the sense resistor should be protected by the shielding pattern which is connected with GND. (Prevention of erroneous detections due to noise)
- Minimizing wire length and its number of branches between current sense resistors and ISENS0/ISENS1 pins to suppress incoming noise from unnecessary pattern.
- LPF (100 Ω and 0.1 uF) to suppress noise should be placed to ISENS0/ISENS1 lines.



### 6.4.7 Communication line (SMBus)

- Zener diodes must be placed to SMBus lines. And it is necessary to mount resistors on the side of FGIC and pack connector. (Zener diode and the resistor on the side of connector are for surge countermeasures, the resistor on the side of FGIC for noise countermeasure.)
- The resistor on the side of the FGIC must be placed as close to the FGIC as possible.

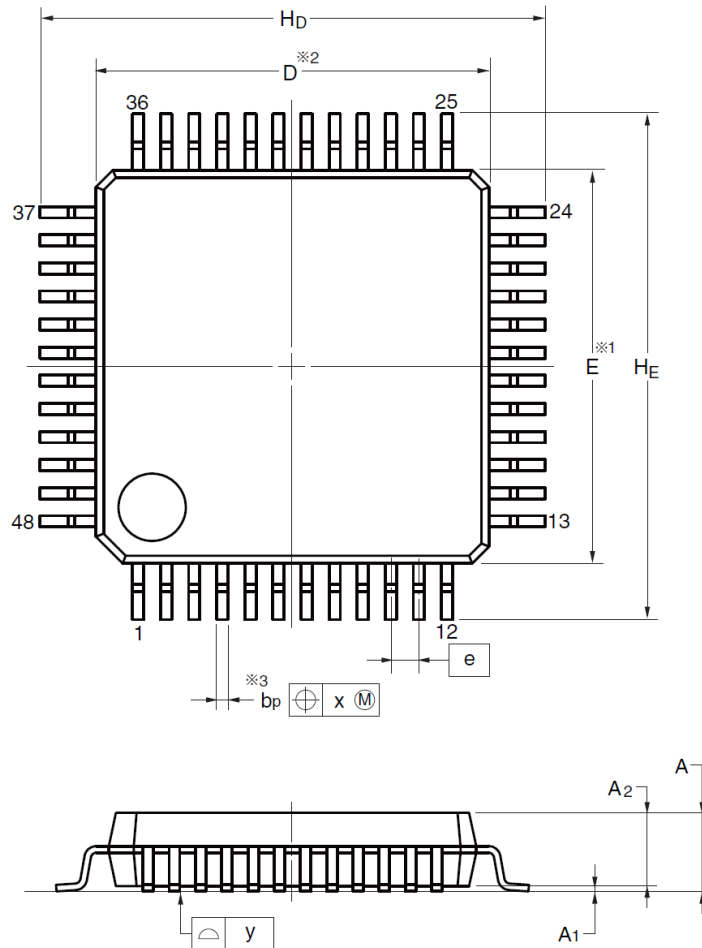


### 6.4.8 Unused Pins

- Unused pins are recommended to be connected to GND via resistors as ESD countermeasure. (Setting low output by software prevents the terminal from becoming indefinite).

CHAPTER 7. PACKAGE OUTLINE

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2



**NOTE**

1. Dimensions “※1” and “※2” do not include mold flash.
2. Dimension “※3” does not include trim offset.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.90	7.00	7.10
E	6.90	7.00	7.10
$H_D$	8.80	9.00	9.20
$H_E$	8.80	9.00	9.20
A	—	—	1.70
$A_1$	0.00	0.10	0.20
$A_2$	—	1.40	—
$b_p$	0.17	0.22	0.27
c	0.105	0.125	0.175
L	0.35	0.50	0.65
$\theta$	0°	—	8°
$e$	—	0.50	—
x	—	—	0.08
y	—	—	0.10

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**REVISION HISTORY**

Rev.	Date	Page	Description
1.00	Jun. 23, 2023	-	First release

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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