RAJ2930004AGM Datasheet

Gate Driver IC for IGBTs and SiC MOSFETs

1. Description

The RAJ2930004AGM is a gate driver IC for IGBT and SiC MOSFET gate-drive in high voltage inverter applications. Integrated 3750Vrms micro-isolators provide data transfer with high voltage isolation between the primary circuit (MCU side) and the secondary circuit (IGBT side). In addition, it boasts superior CMTI (Common Mode Transient Immunity) performance over 150 V/ns, providing reliable communication and increased noise immunity while meeting the high voltages and fast switching speeds required in inverter systems.

This device contains Gate drive circuit, Miller clamp circuit, and Soft turn-off circuit as well as several types of protection circuits such as Overcurrent detection.

Part Number	Package	Body Size
RAJ2930004AGM	SOP16	7.5mm x 10.3mm

2. Features

- On-chip Micro Isolator (isolated circuit)
  - High voltage isolation: 3750Vrms, 1min
  - High CMTI (Common Mode Transient Immunity): over 150V/ns
- High output gate drive circuit
  - Gate drive output peak current (Source / Sink): 10A typ. / 10A typ.
  - On-chip active miller clamp
  - Soft turn-off function
- Various on-chip protection circuits
  - Over current detection by DESAT (Desaturation Protection): 8.9V typ.
  - On-chip under voltage lockout circuit (UVLO)
    VCC1 (5 V system): 4.1V typ.
    VCC2 (15 V system): 10V typ.
  - Fault Alarm outputs on FOB pin and the latched fault status can be reset by RSTB pin
- Operating temperature: - 40 to 125 °C (Junction temperature: 150 °C max)
- AEC-Q100 Qualified (Grade 1)

3. Applications

- Traction inverters for EV/HEV in automotive applications
- DC-DC converters for EV/HEV in automotive applications
- On-board charger for EV in automotive applications
- Inverters and converters for industrial instruments, etc.

Note: The information contained in this document is the one that was obtained when the document was issued and may be subject to change.

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4. Pin Configuration

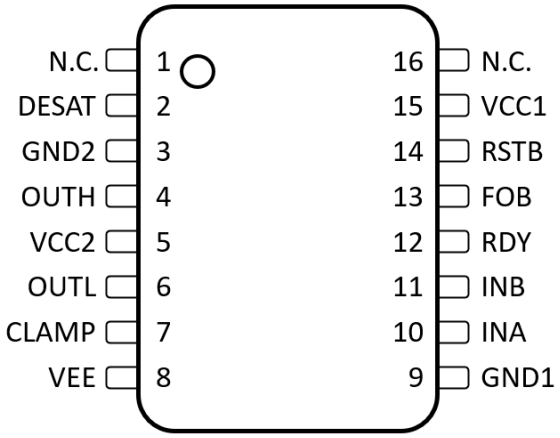


Figure 1 Pin assignment

Table 1 Pin assignment and Functions

No.	Pin Name	I/O	Functions
1	N.C.	-	Non-Connection
2	DESAT	I	DESAT input
3	GND2	P	Secondary side GND. Connect to IGBT Emitter
4	OUTH	O	Gate drive output (Positive)
5	VCC2	P	Secondary power supply input (15 V typ.)
6	OUTL	O	Gate drive output (Negative)
7	CLAMP	I/O	Active Miller clamp input / output
8	VEE	P	Negative power supply input. Connect to GND2 for Unipolar supply application.
9	GND1	P	Primary side GND
10	INA	I	Non-inverted gate drive input
11	INB	I	Inverted gate drive input
12	RDY	O	Power-good output
13	FOB	O	Inverted fault output (L level output at error)
14	RSTB	I	Reset input. Apply a low pulse to reset fault (FOB) latch.
15	VCC1	P	Primary side power supply input (5 V typ.)
16	N.C.	-	Non-Connection

5. Specification

Table 2 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
VCC1	VCC1 – GND1	–0.3	6	V
VCC2	VCC2 – GND2	–0.3	36	V
VEE	VEE – GND2	–17.5	0.3	V
VMAX	VCC2 – VEE	–0.3	36	V
INA, INB, RSTB	DC	GND1–0.3	VCC1+0.3	V
DESAT	Reference to GND2	GND2–0.3	VCC2+0.3	V
OUTH, OUTL, CLAMP	DC	VEE–0.3	VCC2+0.3	V
I_{OUTH}	Peak source current	-15		A
I_{OUTL}	Peak sink current		15	A
RDY, FOB		GND1–0.3	VCC1+0.3	V
IFOB, IRDY	FOB, and RDY pin input current		20	mA
TJ	Junction temperature range	-40	150	°C
Tstg	Storage temperature range	-55	150	°C
VCC1SR1	Slew rate of VCC1 for no destruction		20	V/us
VCC2SR1	Slew rate of VCC2 for no destruction		20	V/us
VEESR1	Slew rate of VEE for no destruction	-20		V/us

Table 3 ESD Ratings

Symbol	Parameter	Conditions	VALUE	Unit
V(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750(Corner Pins) ±500(Other Pins)	V

Table 4 Recommended Operating Conditions

Recommended operating conditions unless otherwise noted.

Symbol	Parameter	MIN	MAX	Unit
VCC1	VCC1 – GND1	4.5	5.5	V
VCC2	VCC2 – GND2	12.5	33	V
VMAX	VCC2 – VEE	12.5	33	V
VEE	VEE – GND2	-16.5	0	V
INA, INB, RSTB	Reference to GND1, High level input voltage	0.7×VCC1	VCC1	V
	Reference to GND1, Low level input voltage	0	0.3×VCC1	V
T_A	Ambient Temperature	-40	125	°C
T_J	Junction temperature	-40	150	°C
VCC1SR2	Slew rate of VCC1 for no change parameters		0.5	V/us
VCC2SR2	Slew rate of VCC2 for no change parameters		0.5	V/us
VEESR2	Slew rate of VEE for no change parameters	-0.5		V/us

Table 5 Thermal Information

Symbol	Parameter	VALUE	Unit
$R_{\theta JA}$ (1)(4)	Junction-to-ambient thermal resistance	64.9	°C/W
$R_{\theta JC(top)}$ (3)(4)	Junction-to-case (top) thermal resistance	27.8	°C/W
$R_{\theta JB}$ (2)(4)	Junction-to-board thermal resistance	33.4	°C/W
ψ_{JT} (1)(4)	Junction-to-top characterization parameter	9.4	°C/W
ψ_{JB} (1)(4)	Junction-to-board characterization parameter	31.8	°C/W

(1) $R_{\theta JA}$, ψ_{JT}, ψ_{JB} : Based on JESD51-2 environment, JESD51-7 test board (4 layer board)

(2) $R_{\theta JB}$: Based on JESD51-8 environment

(3) $R_{\theta JC(top)}$: Based on Mil Std 883 Method 1012.1 described in JESD51-12

(4) These thermal parameters were obtained by simulation and these figures are reference values.

Table 6 Power Ratings

Symbol	Parameter	Conditions	VALUE	Unit
P_D	Maximum power dissipation (both sides)	VCC1 = 5V, VCC2-GND2 = 20V, GND2-VEE = 5V, INA/INB = 5V, 150kHz, 50% Duty Cycle for 10nF load, Ta=25°C, Tj=150℃	1926	mW
P_{D1}	Maximum power dissipation by transmitter side		20	mW
P_{D2}	Maximum power dissipation by receiver side		1906	mW

Table 7 Insulation Specifications

Symbol	Parameter	Conditions	VALUE	Unit
V_{iso}(1)	Withstand isolation voltage	VTEST = VISO = 3750 VRMS, t = 60 s (qualification); VTEST = 1.2 × VISO = 4500 VRMS, t = 1 s (100% production)	3750	V_{RMS}
V_{IOWM}(2)	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	970	V_{RMS}
		DC voltage	1375	V_{DC}
R_{IO}(2)	Insulation resistance, input to output	V_{IO} = 500 V, T_S = 150°C	≥ 10^9	Ω

(1) Refer to UL 1577

(2) Refer to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01

Table 8 Safety Limiting Values

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
I_S	Safety input, output, or supply current	RθJA =64.9°C/W, VCC2 = 15V, VEE=-5V, TJ = 150°C, TA = 25°C			96	mA
		RθJA =64.9°C/W, VCC2 = 20V, VEE=-5V, TJ = 150°C, TA = 25°C			77	mA
P_S	Safety input, output, or total power	RθJA =64.9°C/W, VCC2 = 20V, VEE=-5V, TJ = 150°C, TA = 25°C			1926	mW
T_S	Safety temperature				150	°C

For electrical characteristics, the external circuit of the gate driver is shown in Figure 2.
RON=ROFF=0ohm and CL=100pF unless otherwise noted.

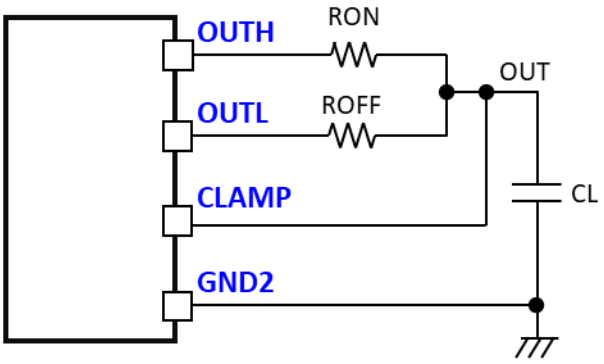


Figure 2 The external circuit of the gate driver

Table 9 Electrical Characteristics (1/5)

VCC1=5V, VCC2-GND2=20V, GND2-VEE=0V, CL=100pF, -40°C<Tj<150°C unless otherwise noted

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{VCC1_ON}	VCC1–GND1		3.9	4.2	4.5	V
V_{VCC1_OFF}			3.8	4.1	4.4	V
V_{VCC1_HYS}				0.1		V
$t_{VCC1+\ to\ OUT}$	VCC1 UVLO on delay to output high	INA = VCC1, INB = GND1	15	30	60	µs
$t_{VCC1-\ to\ OUT}$	VCC1 UVLO off delay to output low	VCC1>3.6V	5	10	25	µs
$t_{VCC1+\ to\ RDY}$	VCC1 UVLO on delay to RDY high	RSTB = VCC1	15	30	60	µs
$t_{VCC1-\ to\ RDY}$	VCC1 UVLO off delay to RDY low		5	10	25	µs

Table 9 Electrical Characteristics (2/5)

VCC1=5V, VCC2-GND2=20V, GND2-VEE=0V, CL=100pF, -40°C<Tj<150°C unless otherwise noted

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VCC2 UVLO THRESHOLD AND DELAY						
V_{VCC2_ON}	VCC2–GND2		10	11	12	V
V_{VCC2_OFF}			9	10	11	V
V_{VCC2_HYS}				1.0		V
$t_{VCC2+ \text{ to OUT}}$	VCC2 UVLO on delay to output high	INA= VCC1, INB = GND1 SR of VCC2 = 10mV/us		10	20	µs
$t_{VCC2- \text{ to OUT}}$	VCC2 UVLO off delay to output low			5	15	µs
$t_{VCC2+ \text{ to RDY}}$	VCC2 UVLO on delay to RDY high	RSTB = FOB=High SR of VCC2 = 10mV/us		10	20	µs
$t_{VCC2- \text{ to RDY}}$	VCC2 UVLO off delay to RDY low			10	20	µs
VCC1, VCC2 QUIESCENT CURRENT						
I_{VCC1Q}	VCC1 quiescent current	OUTH = High, fS = 0Hz	1.45	2	3.2	mA
		OUTL = Low, fS = 0Hz	1.45	2	3.2	mA
I_{VCC2Q}	VCC2 quiescent current	OUTH = High, fS = 0Hz	2.0	4	5.9	mA
		OUTL = Low, Fs = 0Hz	2.0	3.7	5.3	mA
LOGIC INPUTS — INA, INB and RSTB						
V_{INH}	Input high threshold	VCC1 = 5V	0.7×VCC1			V
V_{INL}	Input low threshold	VCC1 = 5V			0.3×VCC1	V
V_{INHYS}	Input threshold hysteresis	VCC1 = 5V		0.12×VCC1		V

Table 9 Electrical Characteristics (3/5)

VCC1=5V, VCC2-GND2=20V, GND2-VEE=0V, CL=100pF, -40°C<Tj<150°C unless otherwise noted

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LOGIC INPUTS —INA, INB and RSTB						
R_{IND}	Input pins pull down resistance	INA = VCC1 RSTB = VCC1		55		kΩ
R_{INU}	Input pins pull up resistance	INB = GND1		55		kΩ
T_{INFIL}	INA, INB and RSTB deglitch (ON and OFF) filter time	fS = 50kHz	28	40	60	ns
T_{RSTFIL}	Deglitch filter time to reset FOB		1.0	-	8.0	us
GATE DRIVER STAGE						
I_{OUTH}	Peak source current	CL=0.18μF, fS=1kHz		-10		A
I_{OUTL}	Peak sink current			10		A
R_{OUTH}	Output pull-up resistance	IOUTH= –0.1A		2.5		Ω
R_{OUTL}	Output pull-down resistance	IOUTL = 0.1A		0.3		Ω

Table 9 Electrical Characteristics (4/5)

VCC1=5V, VCC2-GND2=20V, GND2-VEE=0V, CL=100pF, -40°C<Tj<150°C unless otherwise noted

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
ACTIVE PULLDOWN						
VOUTPD	Output active pull down on OUTL	IOUTL = 1A (IOUTL(typ)x0.1), VCC2=OPEN			2.5	V
INTERNAL ACTIVE MILLER CLAMP						
$V_{CLAMPTH}$	Miller clamp threshold voltage	Reference to VEE	1.5	2	2.5	V
V_{CLAMP}	Output low clamp voltage	ICLAMP = 1A		VEE + 0.5		V
I_{CLAMP}	Output low clamp current	CLAMP= 0 V, VEE = -2.5V		4		A
R_{CLAMP}	Miller clamp pull down resistance	ICLAMP = 0.2A		0.6		Ω
T_{DCLAMP}	Miller clamp ON delay time	CL = 1.8nF		15	50	ns
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUTH}$	OUTH–VCC2	IOUTH = 500mA, tCLP = 10us		0.8	1.0	V
$V_{CLP-OUTL}$	OUTL–VCC2	IOUTL = 500mA, tCLP = 10us		1.55	1.8	V
$V_{CLP-CLAMP}$	CLAMP–VCC2	ICLAMP = 20mA, tCLP = 10us		0.9		V

Table 9 Electrical Characteristics (5/5)

VCC1=5V, VCC2-GND2=20V, GND2-VEE=0V, CL=100pF, -40°C<Tj<150°C unless otherwise noted

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
DESAT PROTECTION						
I_{CHG}	Blanking capacitor charge current	V(DESAT) - GND2 = 2 V	350	500	650	µA
I_{DCHG}	Blanking capacitor discharge current	V(DESAT) - GND2 = 6 V	9	14		mA
V_{DESAT}	Detection Threshold		8.3	8.9	9.5	V
$t_{DESATLEB}$	Leading edge blank time			200		ns
$t_{DESATFIL}$	DESAT deglitch filter		50	140	230	ns
$t_{DESATOFF}$	DESAT propagation delay to OUTL 90%		60	220	300	ns
$t_{DESATFOB}$	DESAT to FOB low delay		60	400	1600	ns
INTERNAL SOFT TURN-OFF						
I_{STO}	Soft turn-off current on fault conditions	OUTL = VEE + 8 V	250	400	570	mA
FOB AND RDY REPORTING						
t_{RDYHLD}	VCC1 and VCC2 UVLO RDY low minimum holding time		0.20		1	ms
$T_{FOBMUTE}$	Output mute time on fault	Reset fault through RSTB	0.20		1	ms
V_{ODL}	Open drain low output voltage	IODON = 5mA			0.3	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity		150			V/ns

Table 10 Switching Characteristics

VCC1=5V, VCC2-GND2=20V, GND2-VEE=0V, CL=100pF, -40°C<Tj<150°C unless otherwise noted

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{PDHL}	Propagation delay time – High to Low	CL = 100pF	30	70	140	ns
t_{PDLH}	Propagation delay time – Low to High	CL = 100pF	30	70	140	ns
PWD	Pulse width distortion $\|t_{PDHL} - t_{PDLH}\|$				30	ns
t_{sk-pp}	Part to Part skew	Rising or Falling Propagation Delay Difference due to process deviation			50	ns
t_r	Driver output rise time	CL = 10nF		33		ns
t_f	Driver output fall time	CL = 10nF		27		ns
f_{Smax}	Maximum switching frequency			1		MHz

Table 11 Thermal Shut Down Characteristic

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
T_{TSD}	Thermal shut down temperature		150	175	200	°C
T_{TSDREC}	Thermal shut down recover temperature		120	150	180	°C
T_{TSDHYS}	Thermal shut down hysteresis temperature		15	25	35	°C

Typical Characteristics

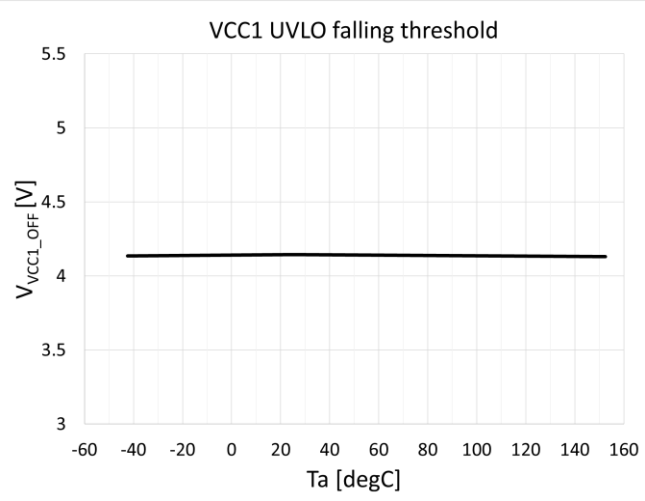


Figure 3 VCC1 UVLO falling threshold

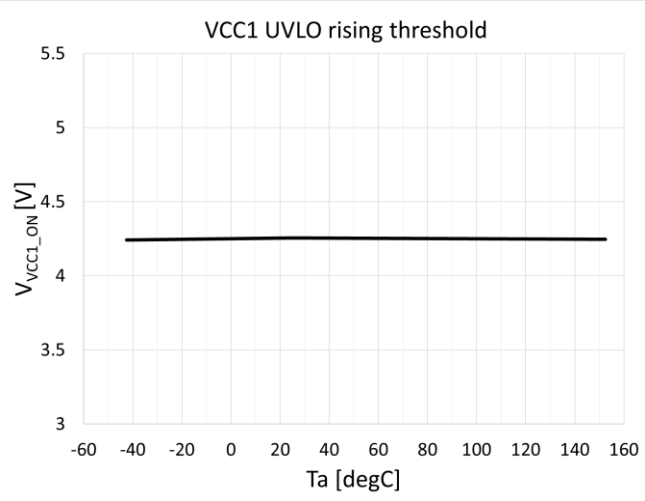


Figure 4 VCC1 UVLO rising threshold

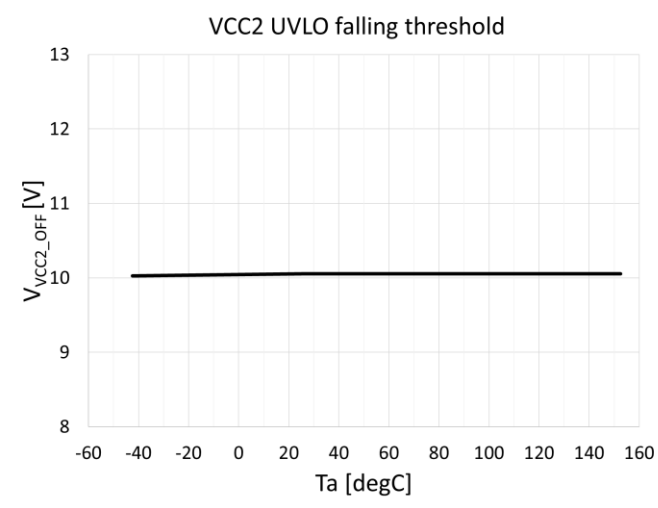


Figure 5 VCC2 UVLO falling threshold

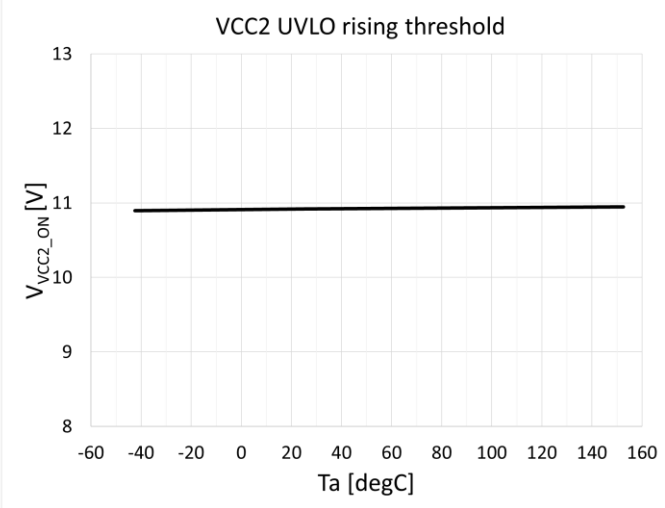


Figure 6 VCC2 UVLO rising threshold

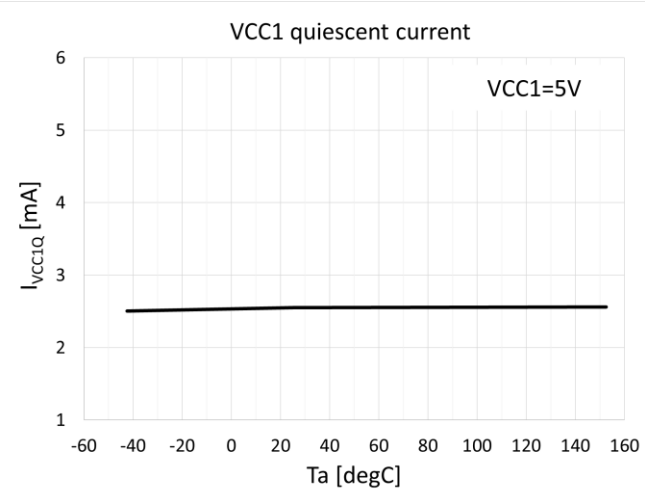


Figure 7 VCC1 quiescent current

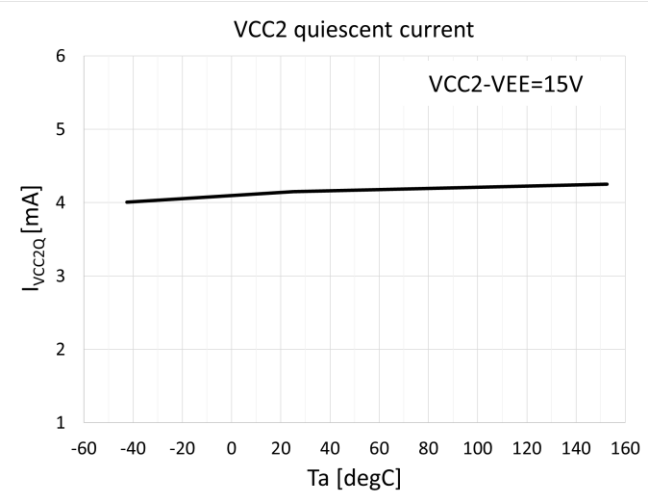


Figure 8 VCC2 quiescent current

Typical Characteristics (continued)

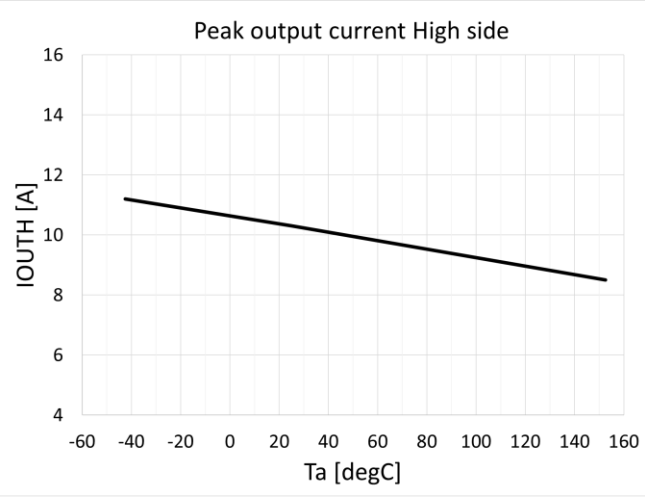


Figure 9 Peak output current High side

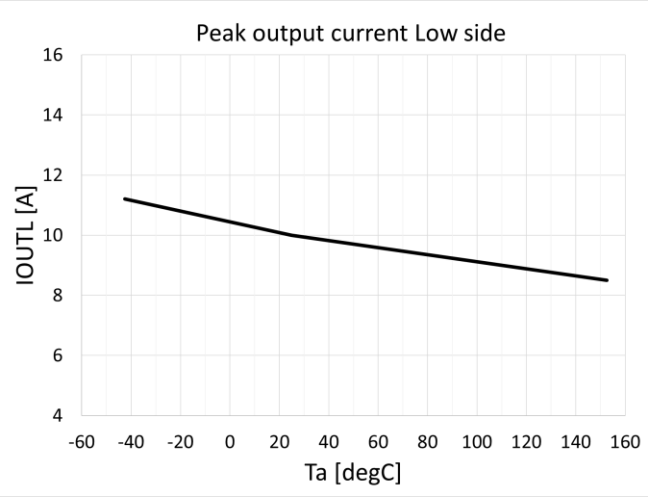


Figure 10 Peak output current Low side

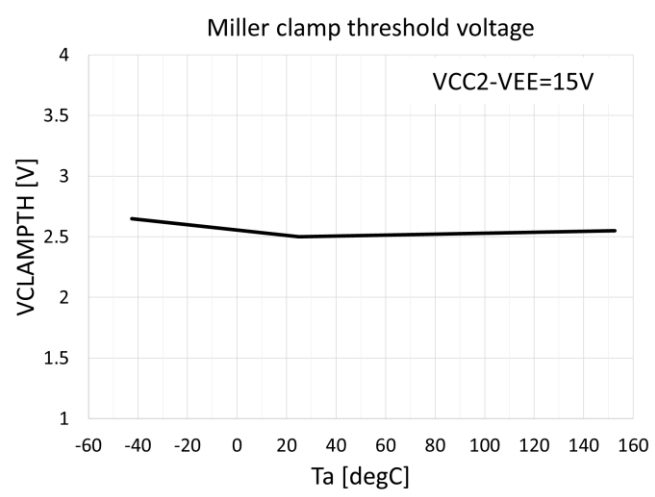


Figure 11 Miller clamp threshold voltage

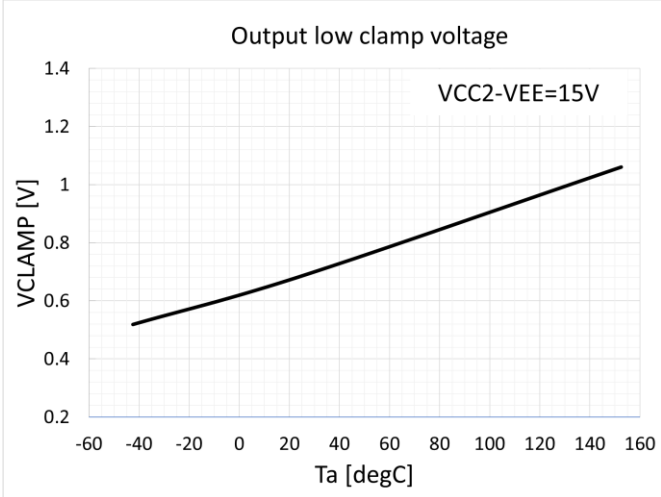


Figure 12 Output low clamp voltage

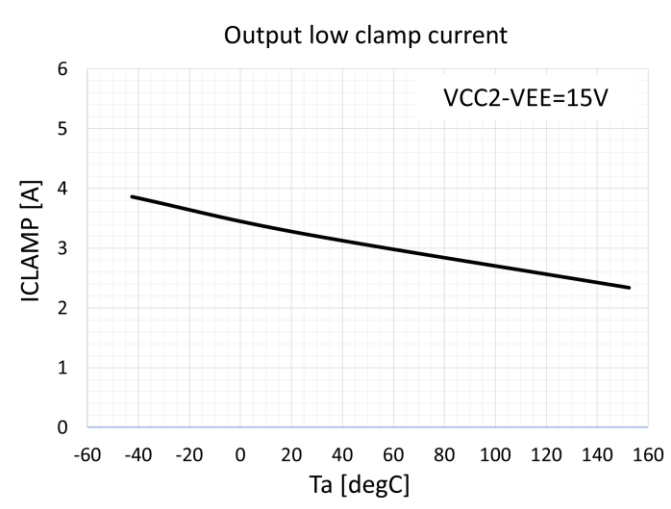


Figure 13 Output low clamp current

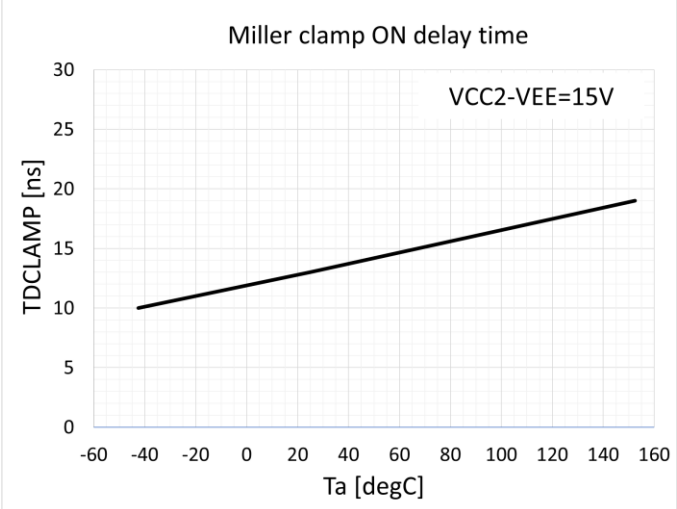


Figure 14 Miller clamp ON delay time

Typical Characteristics (continued)

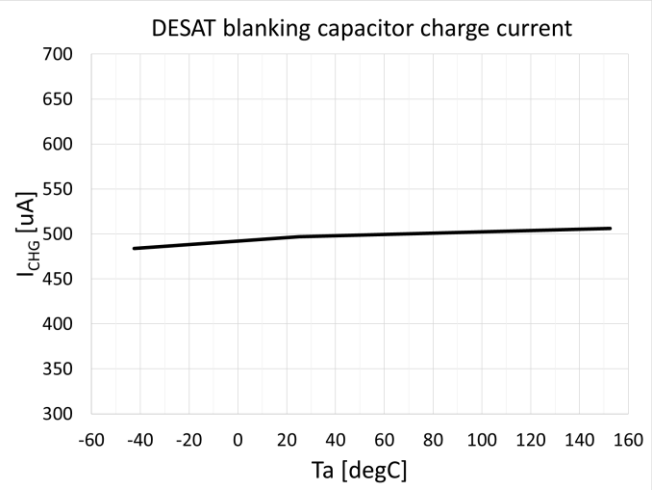


Figure 15 DESAT blanking capacitor charge current

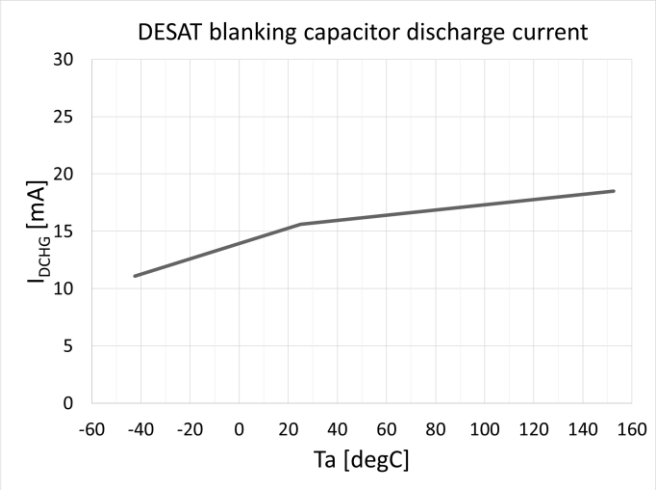


Figure 16 DESAT blanking capacitor discharge current

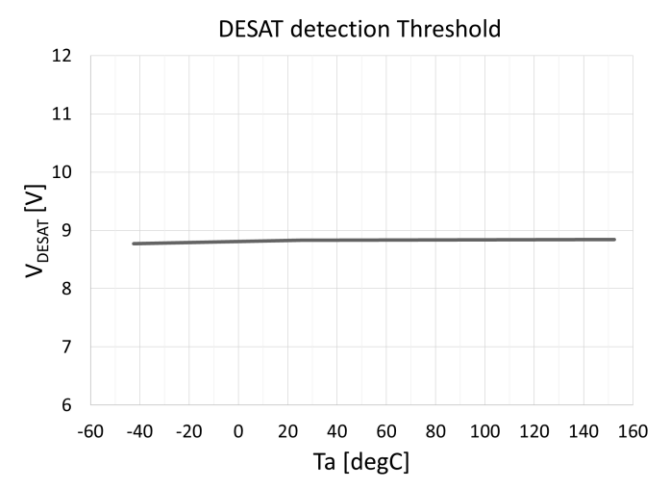


Figure 17 DESAT detection Threshold

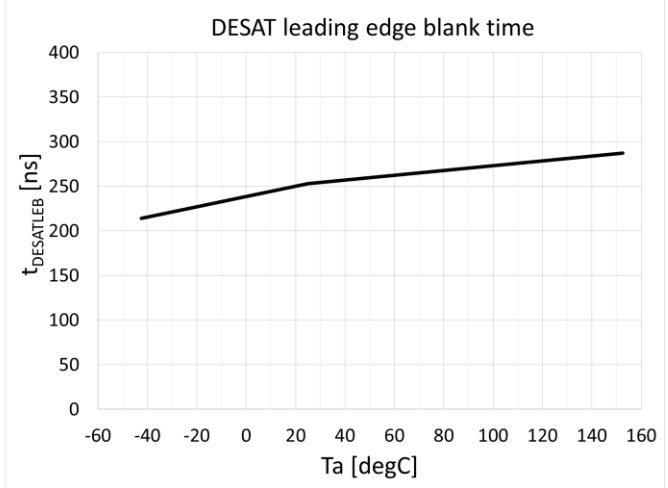


Figure 18 DESAT leading edge blank time

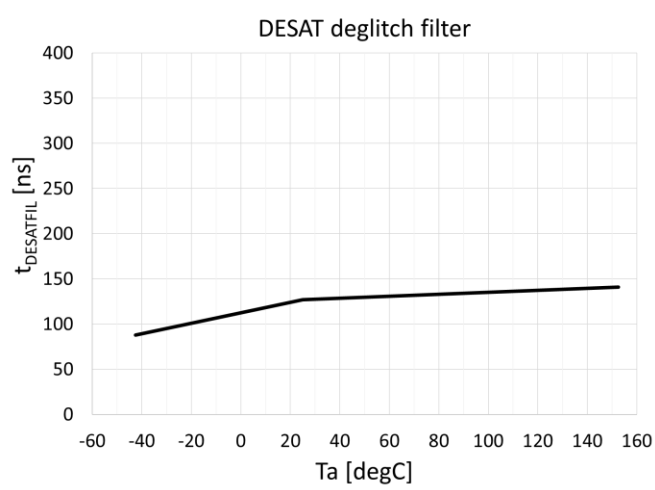


Figure 19 DESAT deglitch filter

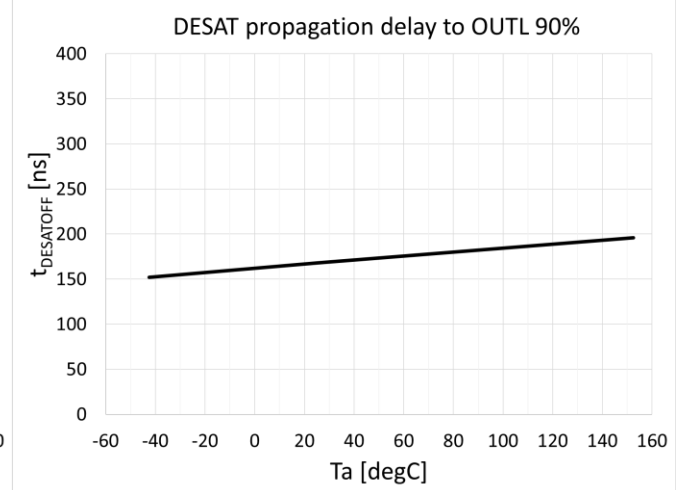


Figure 20 DESAT propagation delay to OUTL 90%

Typical Characteristics (continued)

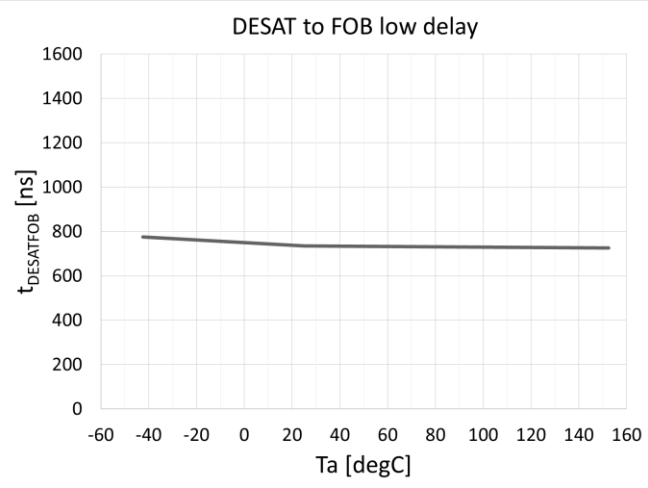


Figure 21 DESAT to FOB low delay

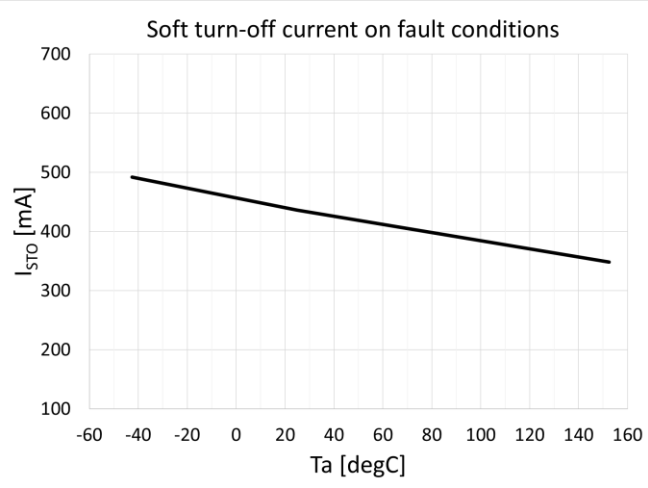


Figure 22 Soft turn-off on fault conditions

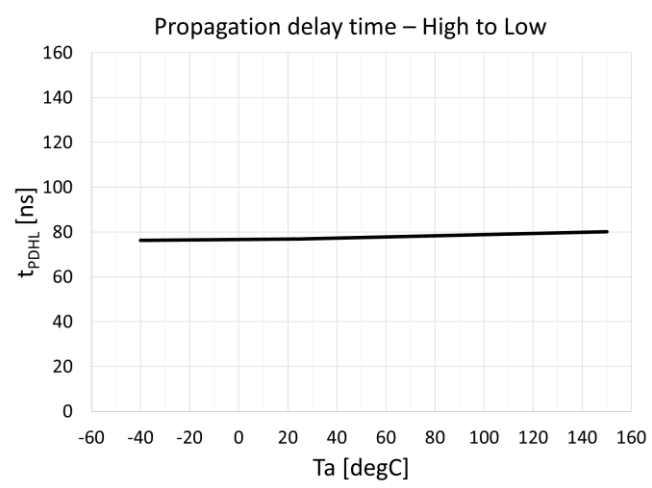


Figure 23 Propagation delay time − High to Low

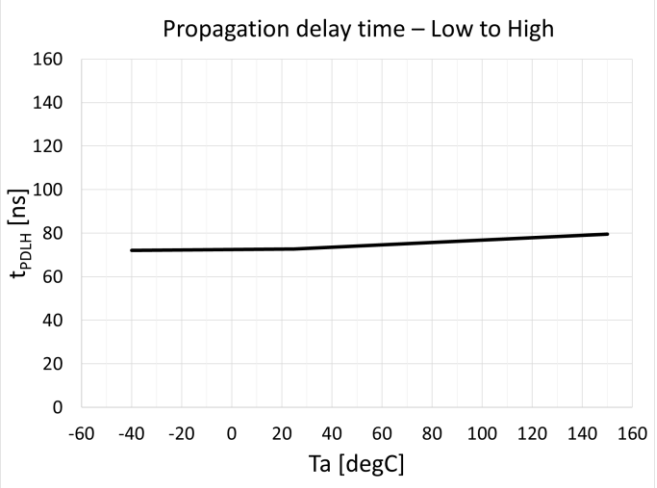


Figure 24 Propagation delay time − Low to High

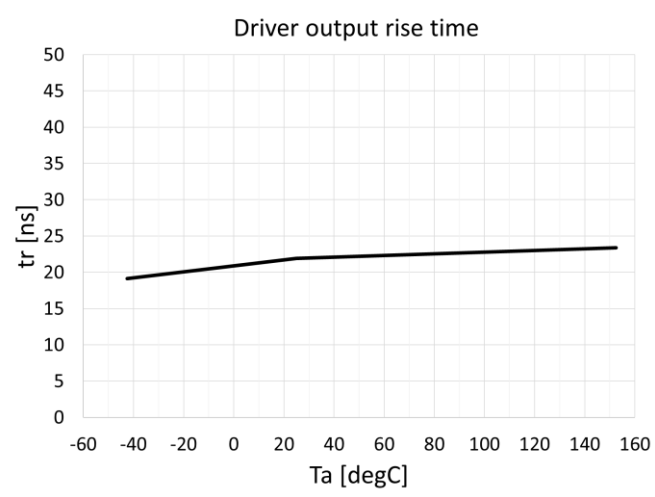


Figure 25 Driver output rise time

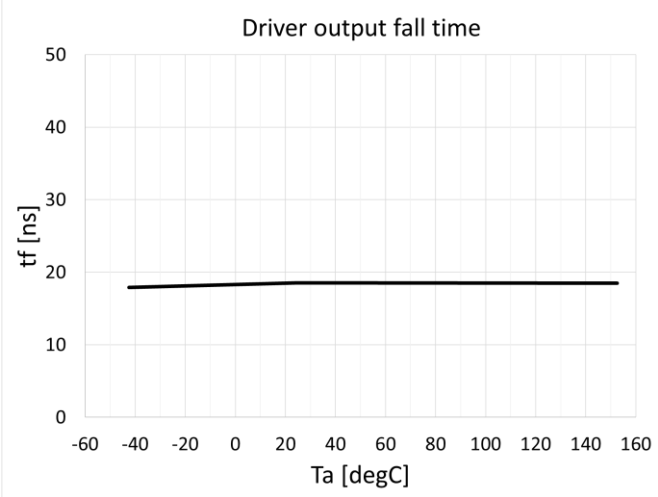


Figure 26 Driver output fall time

Table 12 Function Table

		Supply			Input				Output			
#	State	VCC1	VCC2	VEE	Latched fault (1)	RSTB	INA	INB	RDY	FOB	OUTH/ OUTL	CLAMP
1	VCC1 UVLO	PD	PU	PU	X	X	X	X	Low	HiZ	Low	Low
2	VCC2 UVLO	PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low
3	VCC2 Open	PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ
4	DESAT and TSD	PU	PU	PU	Yes	X	X	X	HiZ	Low	Soft turn-off	Low
5	Reset	PU	PU	PU	No	Low	X	X	HiZ	HiZ	Low	Low
6	Normal operation	PU	PU	PU	No	High	Low	X	HiZ	HiZ	Low	Low
7		PU	PU	PU	No	High	X	High	HiZ	HiZ	Low	Low
8		PU	PU	PU	No	High	High	High	HiZ	HiZ	Low	Low
9		PU	PU	PU	No	High	High	Low	HiZ	HiZ	High	HiZ

(1) Latched fault is reset at rise edge of RSTB.

PU: Power Up (VCC1 ≥ 4.5 V, VCC2 ≥ 12 V); PD: Power Down (3.2V ≤ VCC1 ≤ 3.8 V, VCC2 ≤ 9 V); X:Irrelevant; HiZ: High Impedance

To drive the Power devices, the following methods are recommended (See Table 13):

1. Fix the INA to “L” and Use the INB to drive the Power device.

2. Fix the INB to “H” and Use the INA to drive the Power device.

3. Make the INA and INB in a opposite phases to drive the Power device.

Table 13 Recommended drive method

#	INA	INB	OUTH / OUTL	Power device State
1	L	X	L	OFF
2	X	H	L	OFF
3	H	L	H	ON

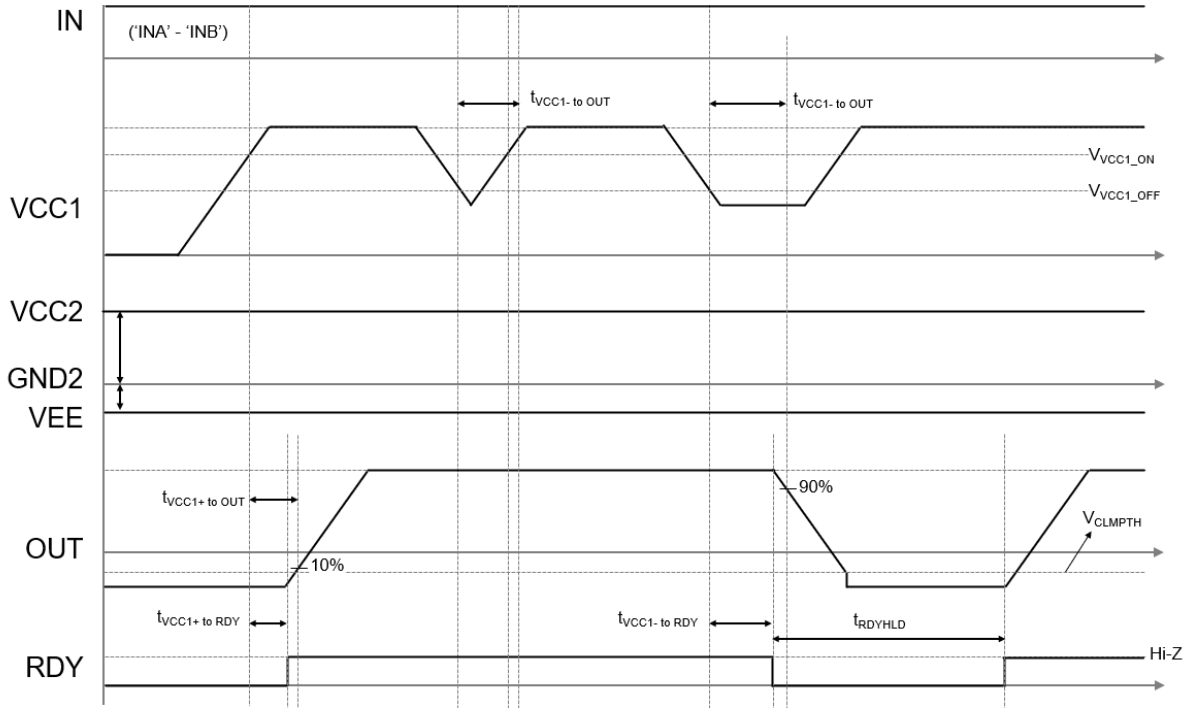


Figure 27 VCC1 UVLO Protection Timing Diagram

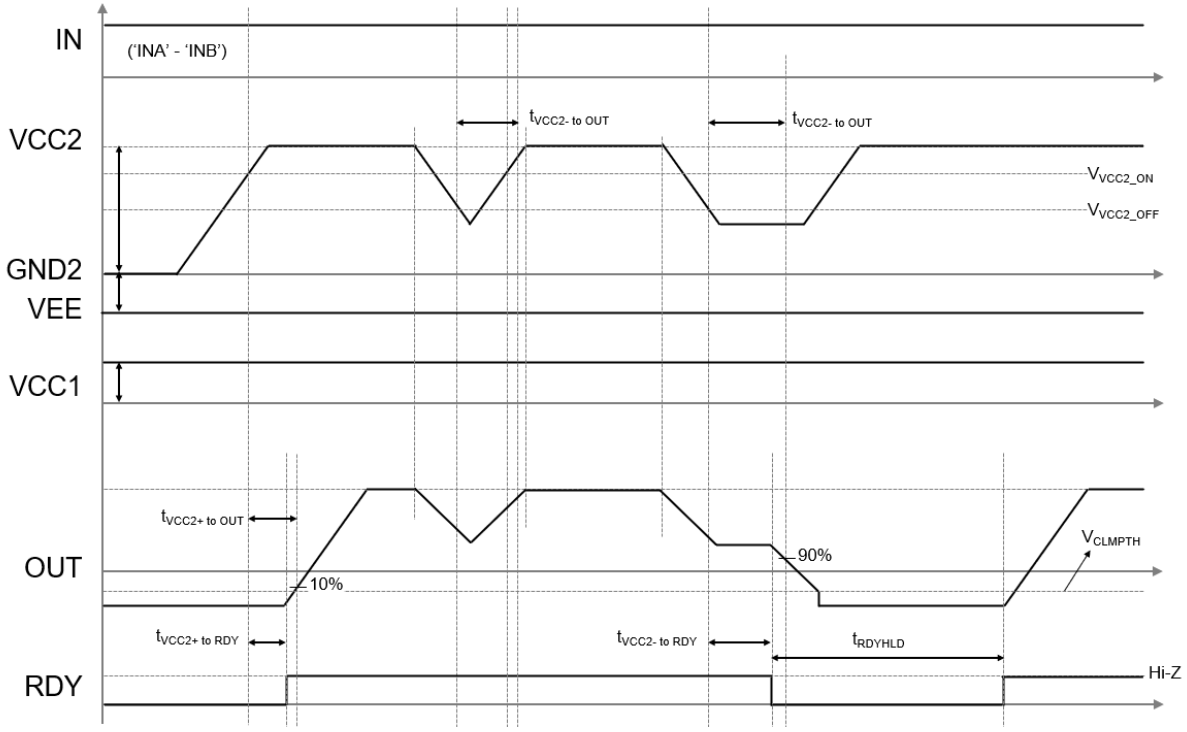


Figure 28 VCC2 UVLO Protection Timing Diagram

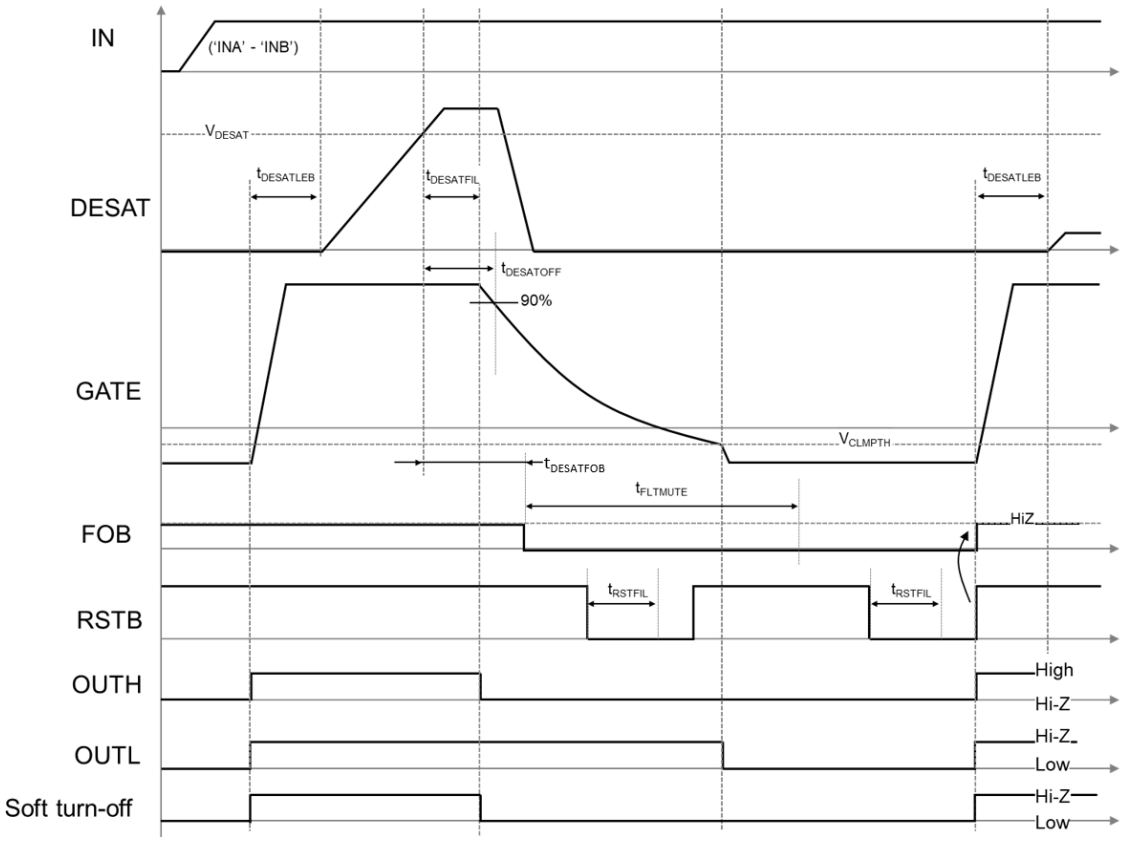


Figure 29 Timing diagram of DESAT Protection with Soft Turn-OFF During Turn-on Transition

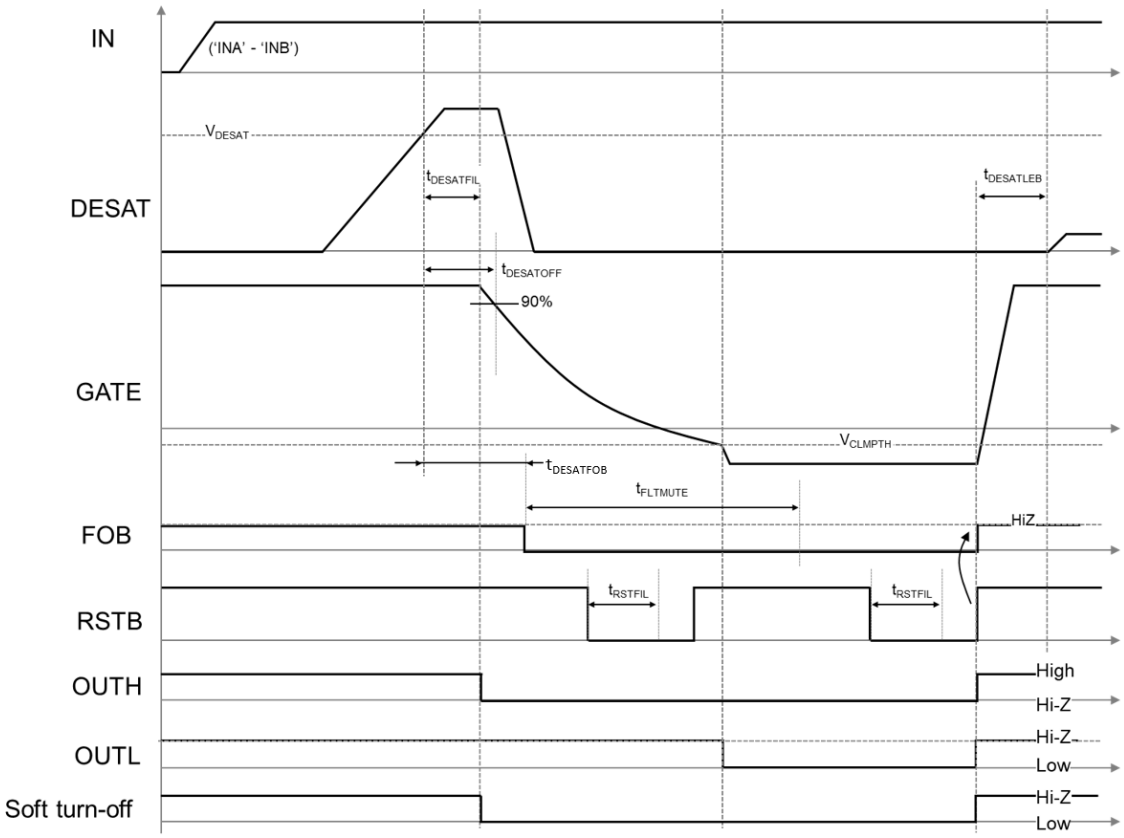


Figure 30 Timing diagram of DESAT Protection with Soft Turn-OFF While Power Device is ON

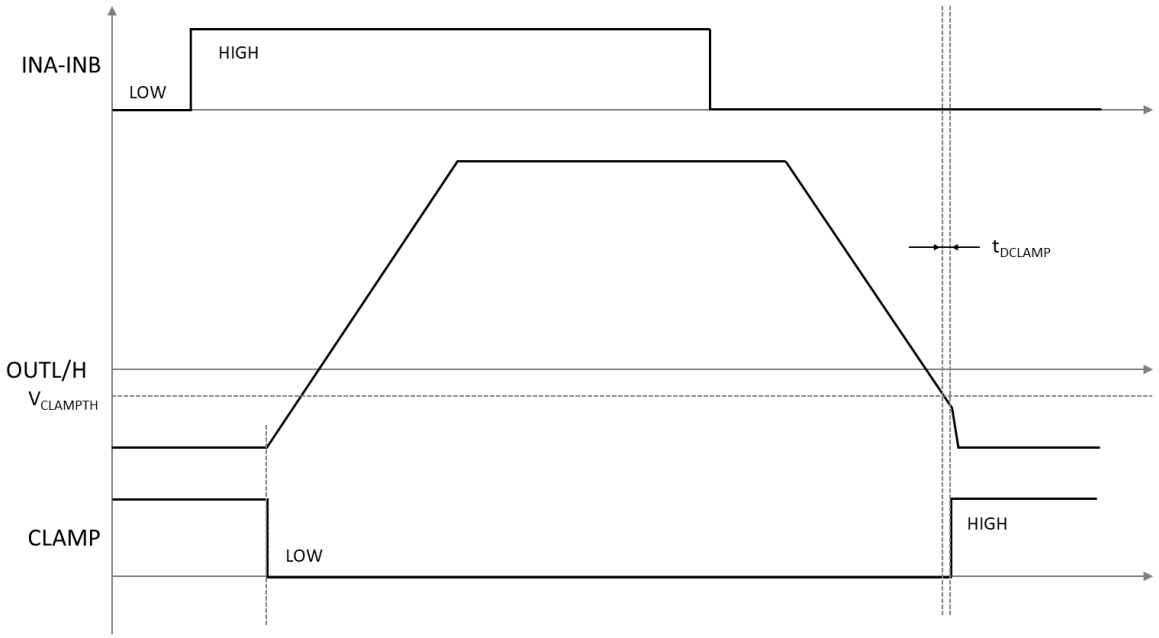


Figure 31 Timing Diagram of Active Miller Clamp

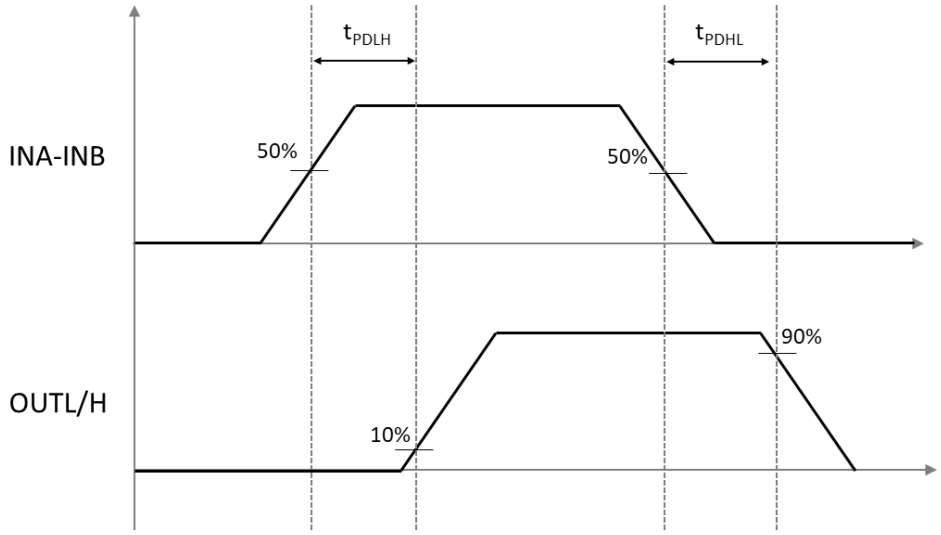


Figure 32 Timing diagram of Propagation delay time

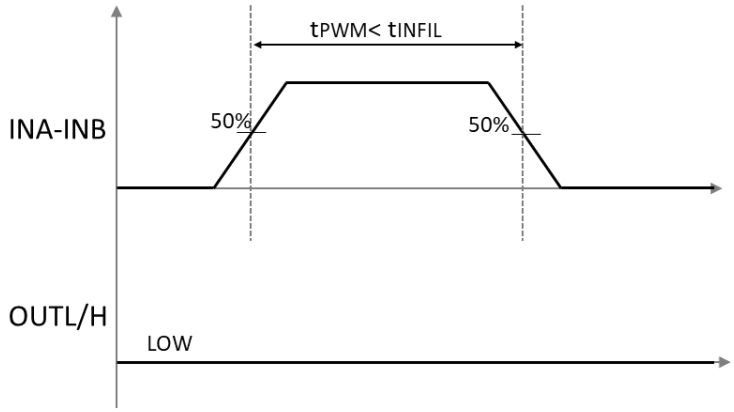


Figure 33 Timing diagram of ON Deglitch Filter

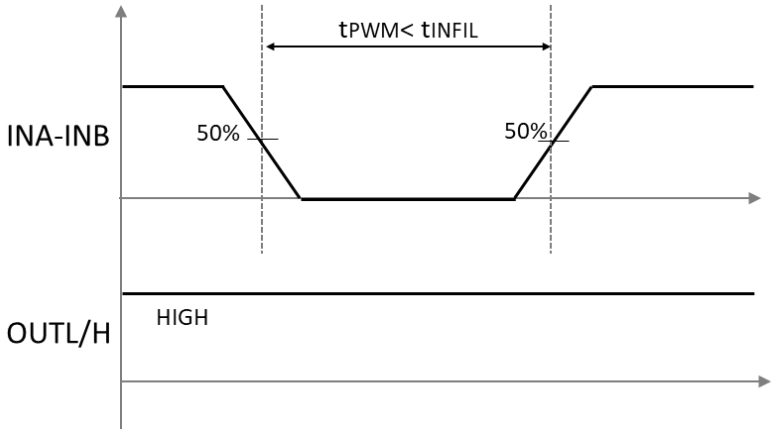


Figure 34 Timing diagram of OFF Deglitch Filter

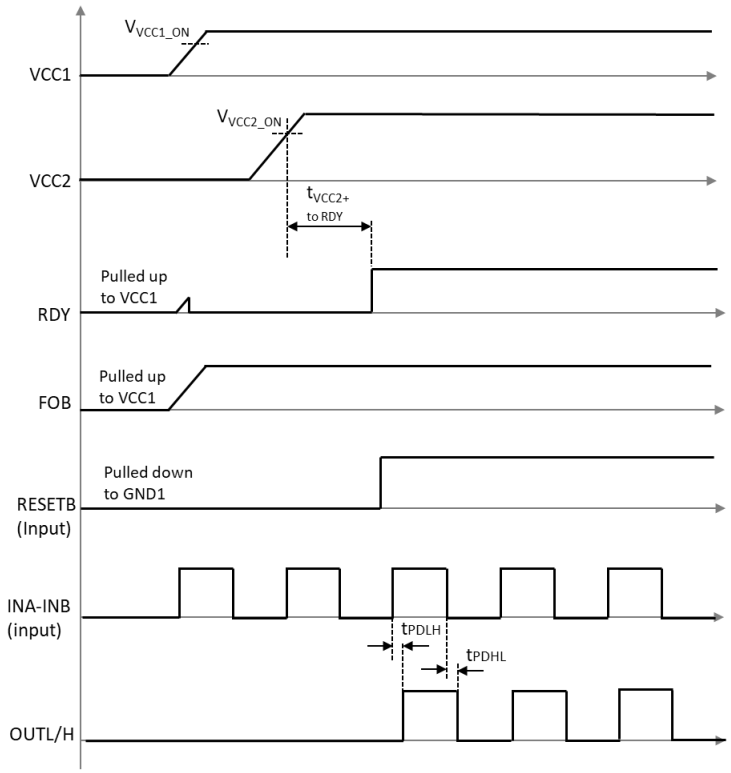


Figure 35 Timing diagram of Power up Sequence

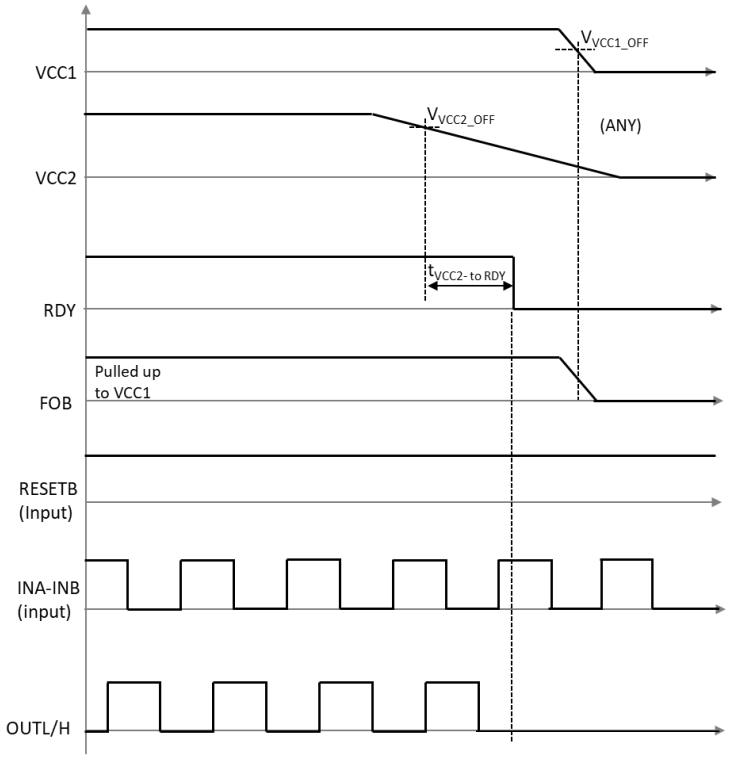


Figure 36 Timing diagram of Power down Sequence

6 Functions

The internal block of the RAJ2930004AGM is shown in Figure 37

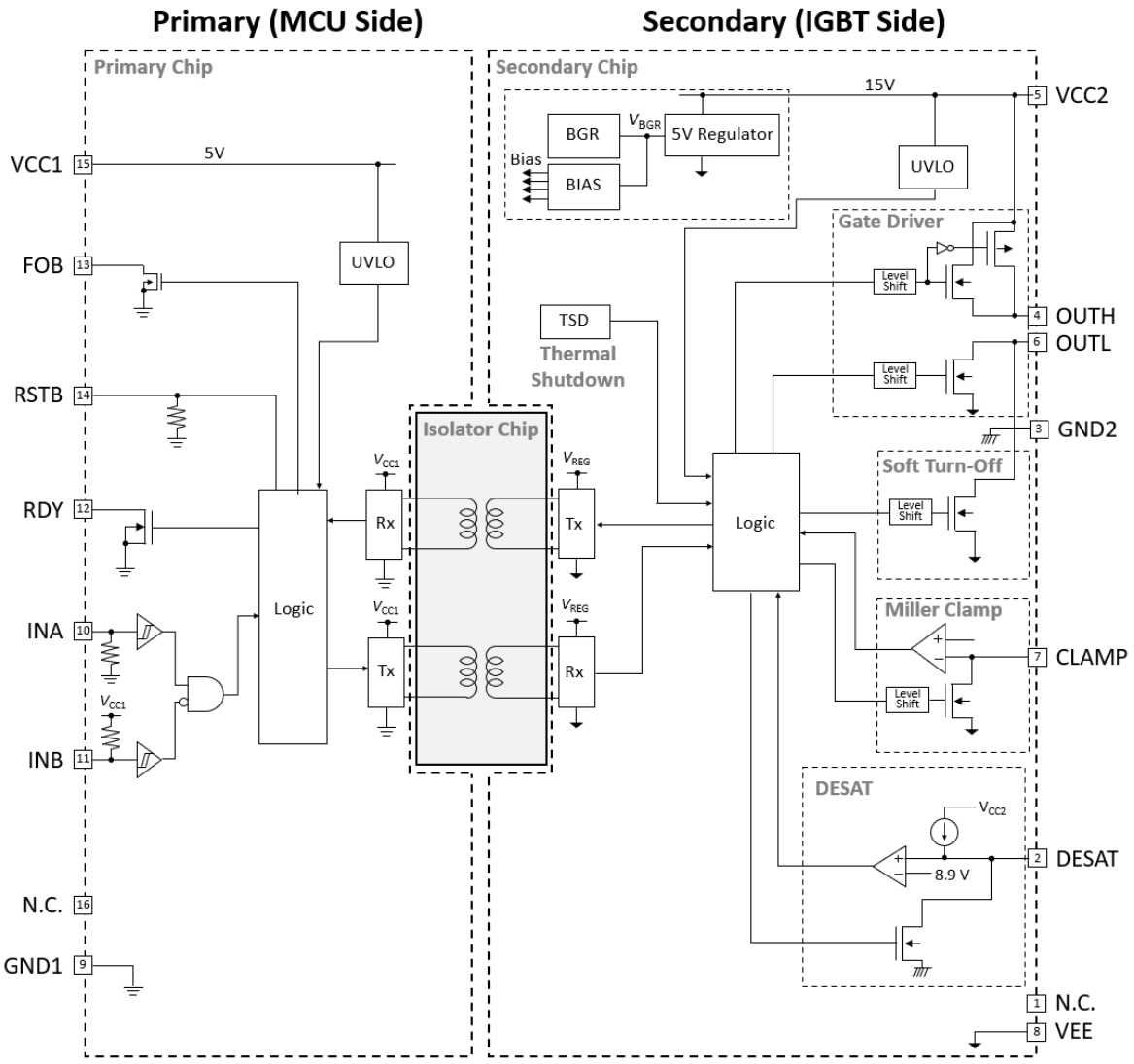


Figure 37 Internal block diagram

6.1 Gate driver

6.1.1 Features

- The gate driver charges or discharges the IGBT gate pins.
- Gate drive output peak current (Source / Sink): 10A(Typ) / 10A(Typ)
- Since the high-side gate drive output pin OUTH and the low-side gate drive output pin OUTL are independent of each other, the slew rates of the rise and fall of the gate voltage can be separately adjusted using the external resistors (RGH and RGL)
- The soft turn-off is the feature to lower the gate voltage of the IGBT gradually and turn it off when any of the following abnormal states is detected on the secondary circuit: DESAT or TSD.
- Switching operation can be resumed by RSTB when the abnormal states that caused soft turn-off returns to normal.
- Active pulldown resistance can clamp the OUTL pin to VEE when VCC2 is open. (Figure 39)
- Short circuit clamping diodes can clamp the OUTH/OUTL/CLAMP pins to VCC2 + Vf when the short circuit event occur and the current input to the pins. (Figure 40)

6.1.2 Block diagram

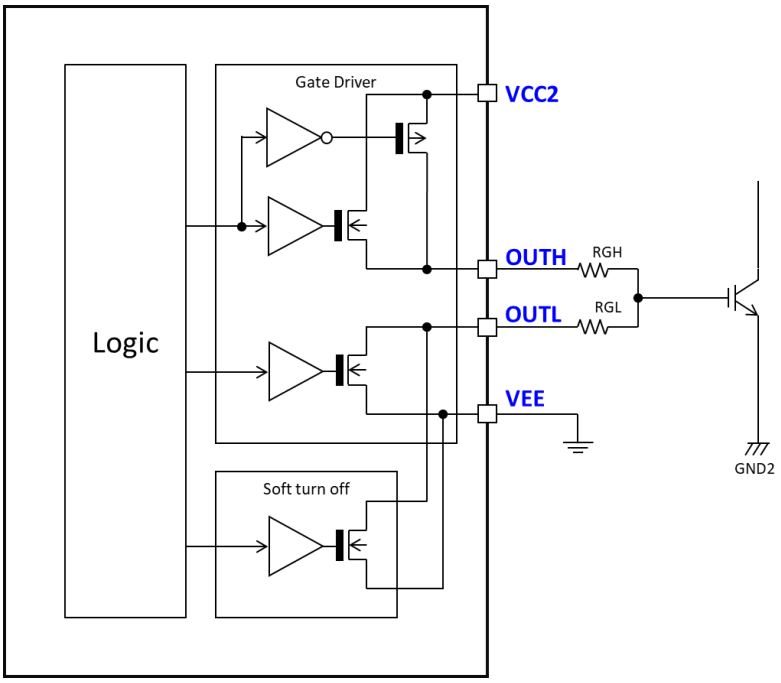


Figure 38 Block diagram of gate driver

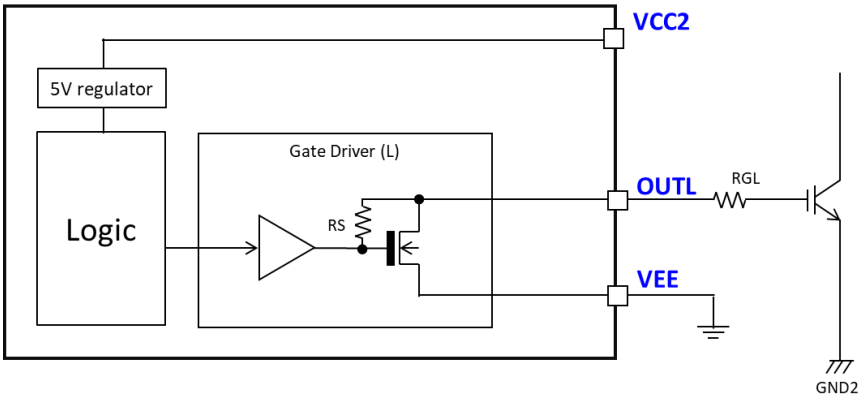


Figure 39 Block diagram of active pulldown

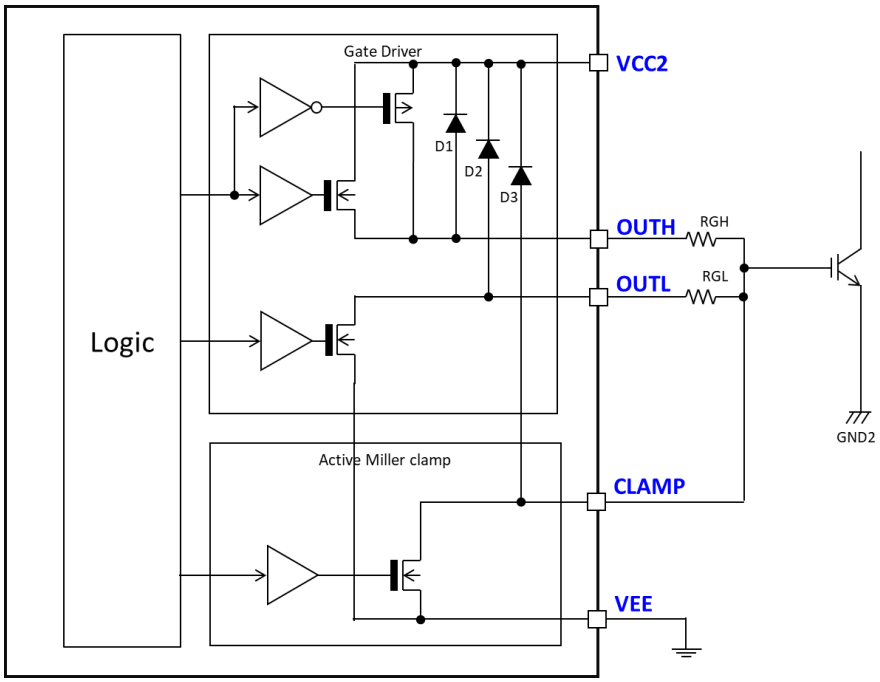


Figure 40 Block diagram of Short circuit clamping

6.2 Active Miller clamp

6.2.1 Features

- The active Miller clamp is the feature to prevent the self-turn-on of the IGBT due to the coupling capacitance between the IGBT gate and collector.
- If the CLAMP pin voltage falls below VCLAMP (2.0 V typ.) while the input signal to turn off the IGBT is applied to the INA or INB pin, the IGBT gate is short-circuited to the VEE pin with low resistance.

6.2.2 Block diagram

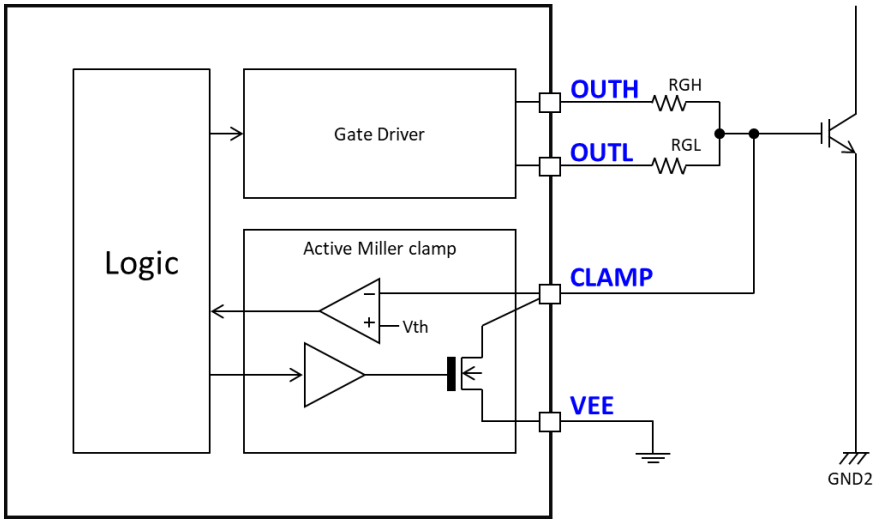


Figure 41 Block diagram of active Miller clamp

6.3 UVLO

6.3.1 Features

- The primary circuit is equipped with a UVLO that detects a voltage drop of VCC1, and the UVLO turns off the IGBT (this is a normal turn-off operation different from a soft turn-off) when the VCC1 voltage drops below 4.1 V. At this time, the low level is output to the RDY pin of the primary circuit.
- The secondary circuit is equipped with a UVLO that detects the voltage drop of VCC2 and a UVLO that detects the voltage drop of VREG (output from 5 V regulator). The IGBT is turned off if the VCC2 voltage drops below 10 V or the VREG voltage drops below 4.1 V. At this time, the low level is output to the RDY pin of the primary circuit.

6.3.2 Block diagram

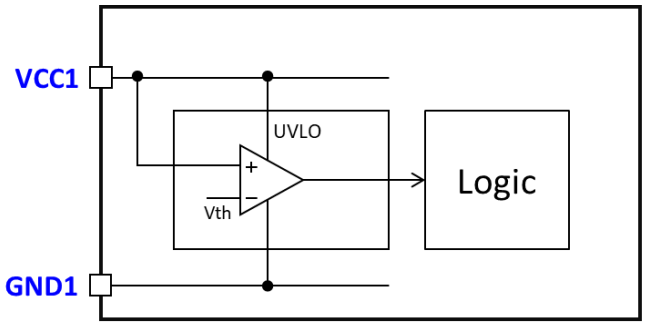


Figure 42 Block diagram of UVLO on primary chip

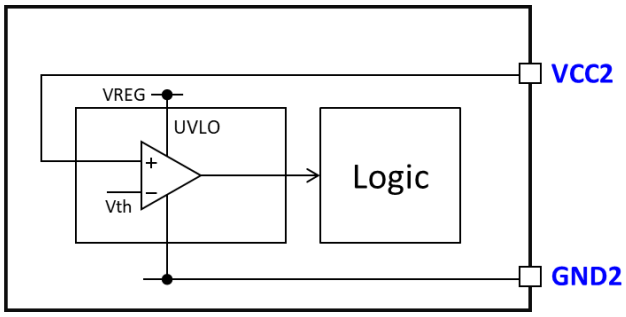


Figure 43 Block diagram of UVLO on secondary chip

6.4 Desaturation protection (DESAT)

6.4.1 Features

- This feature turns off the output from the gate driver if the over current detection by DESAT.
- The IGBT is soft turned-off if the voltage applied to the DESAT pin rises beyond the threshold voltage 8.9V +/- 6.7% when the IGBT is in the on-state. At this time, the low level is output to the FOB pin of the primary circuit.

6.4.2 Block diagram

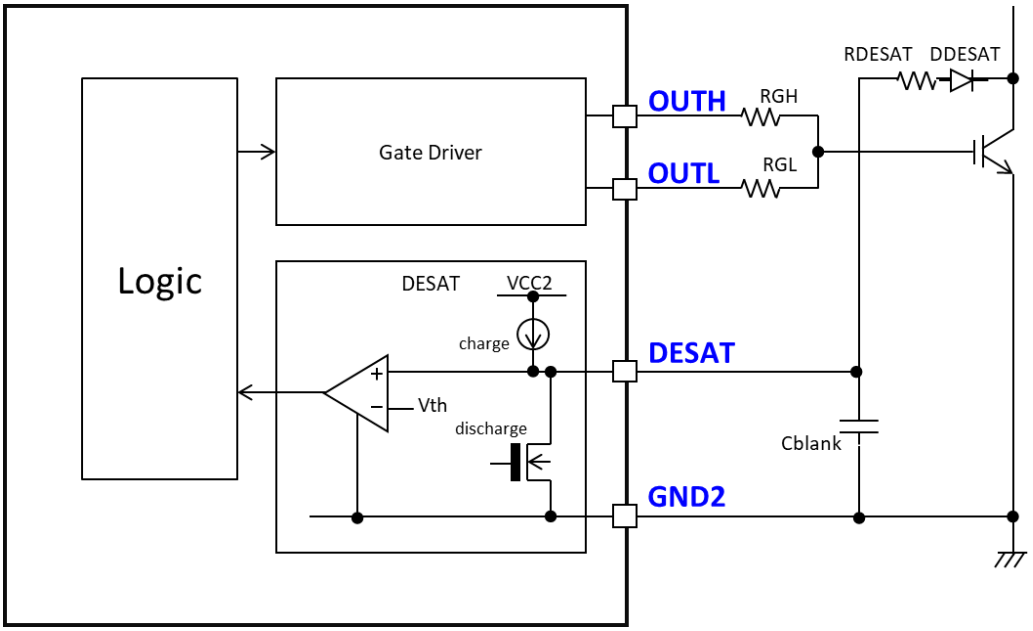


Figure 44 Block diagram of DESAT

6.5 Isolation

6.5.1 Features

- On-chip Micro Isolator (isolated circuit)
- High voltage isolation: 3750VRMS, 1min
- High Common Mode Transient Immunity (CMTI): over 150kV/us

6.5.2 Block diagram

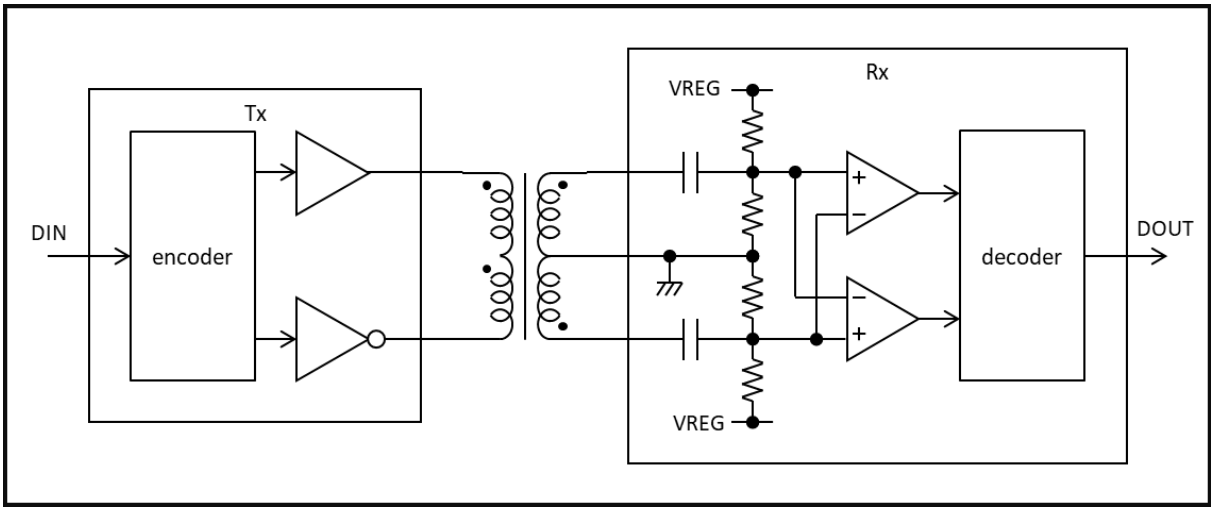


Figure 45 Block diagram of isolation

6.6 Thermal shut down (TSD)

6.6.1 Features

- This feature turns off the IGBT to prevent the damage on the IGBT due to malfunctioning of the IC when an extraordinary over heat (175 °C TYP) is detected in the IC (thermal shut down: TSD). Switching operation can be resumed by RSTB when IC's junction temperature is lower below the TSD recover temperature (typical hysteresis is 25 °C).
- Temperature sense diode is placed near the OUTH pin that tend to be heated in the IC. The IGBT is soft turned off if the temperature of the driver transistor in the IC exceeds a threshold value due to the over load or the increased ambient temperature. At this time, the low level is output to the FOB pin of the primary circuit.

6.6.2 Block diagram

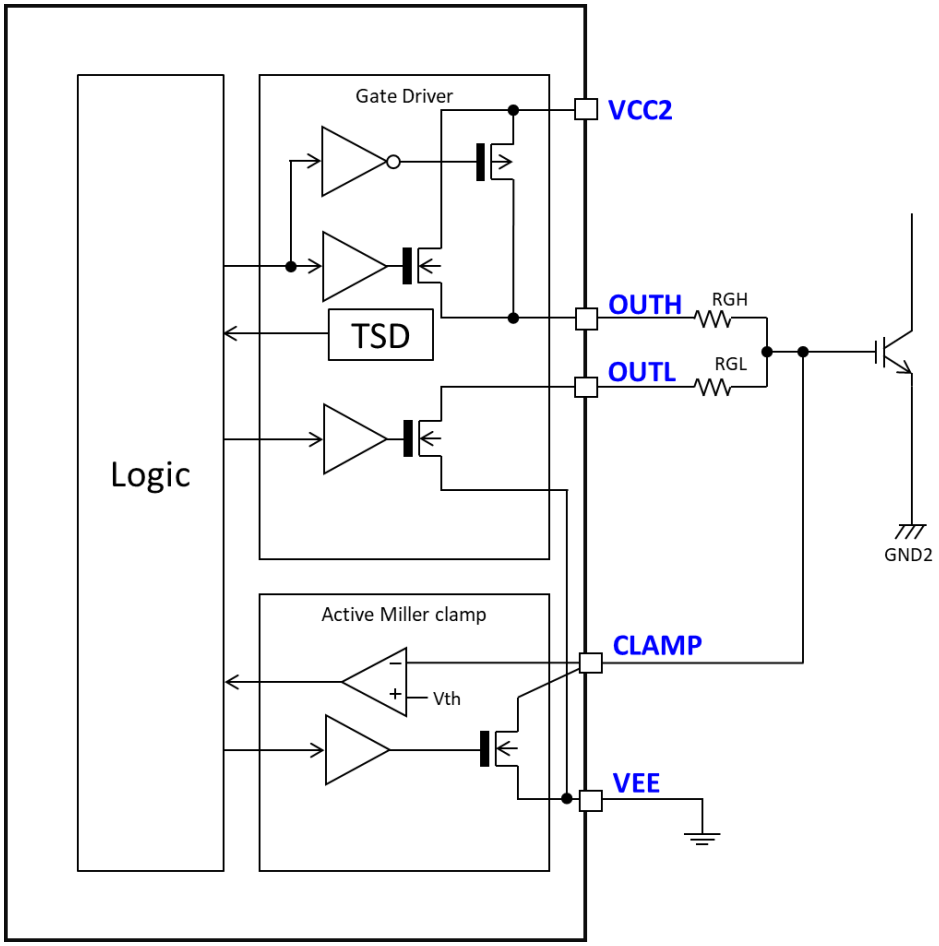


Figure 46 Block diagram of thermal shut down

6.7 Internal regulator, reference voltage

6.7.1 Features

- For primary chip, supply voltage of internal circuit is supplied from external pin.
- For secondary chip, supply voltage of internal circuit is supplied from on-chip 5 V regulator.

6.7.2 Block diagram

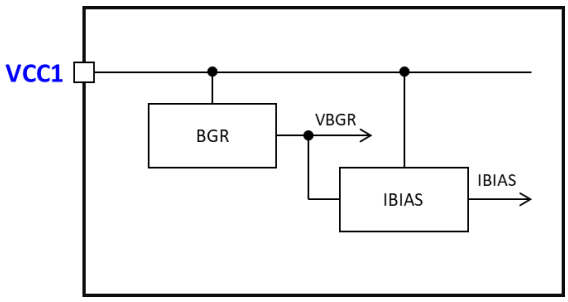


Figure 47 Block diagram of reference voltage on primary chip

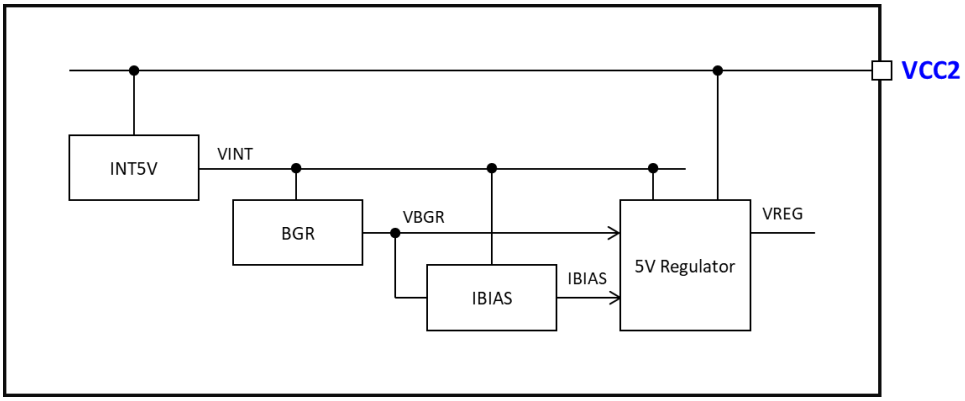


Figure 48 Block diagram of internal regulator and reference voltage on secondary chip

7 Example of application diagram

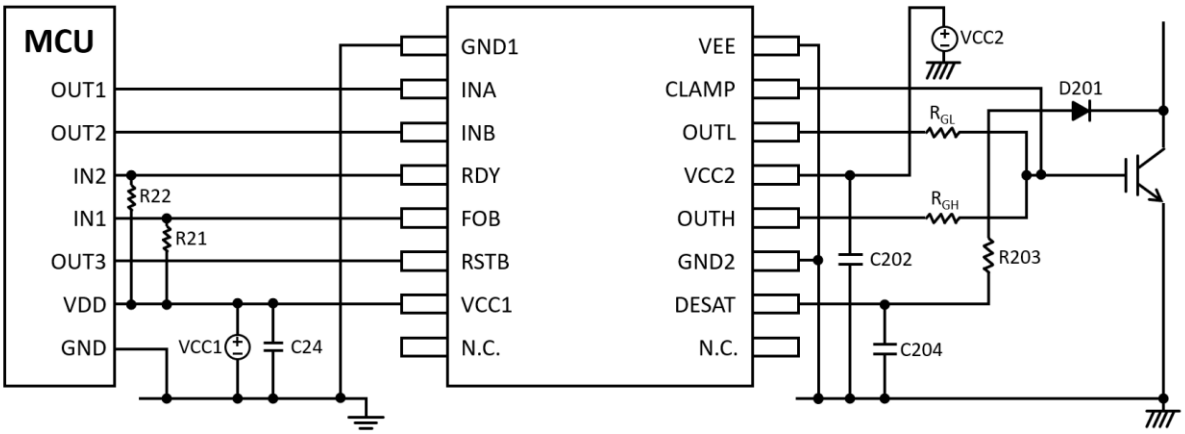


Figure 49 Simplified application diagram for IGBT

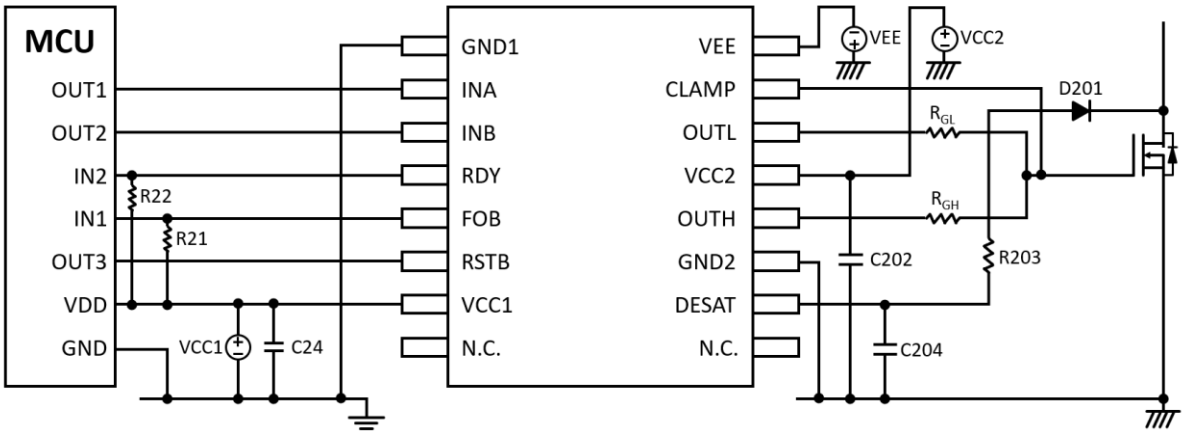


Figure 50 Simplified application diagram for SiC MOSFET

Table 14 Specifications of external components

Component	Specification
R21	5kohm / 5%
R22	5kohm / 5%
C24	0.1uF / 10%
C202	1uF / 10%
C204	100pF / 5%
R203	6.8kohm / 5%
RGL(1)	5.1ohm / 5%
RGH(1)	5.1ohm / 5%
D201	Fast Recovery Diode (RFN1LAM7S)

(1) The type and unit price of the component (resistor RG) may differ depending on the specifications of the IGBT (Gate charge, Gate-emitter peak voltage, etc.). The rated power PG of the resistor RG connected to the IGBT can be calculated by Equations 1 and 2.

$$P_{\mathrm{G}} = I_{\mathrm{G}}^2 R \quad (1)$$

$$I_{\mathrm{G}} = f_{\mathrm{C}} \times \left(\left|+Q_g\right| + \left|-Q_g\right|\right) \quad (2)$$

fc: Switching Frequency

$+Q_g$: Charge amount from 0V to $+V_{GE}$

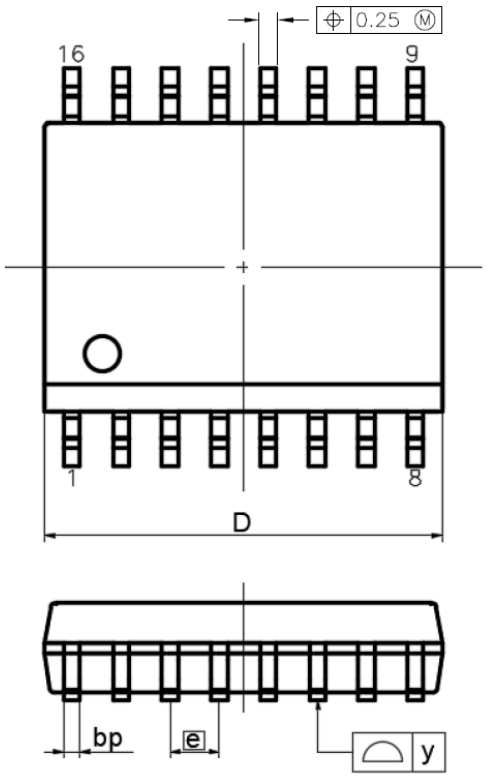
$-Q_g$: Charge amount from $-V_{GE}$ to 0V

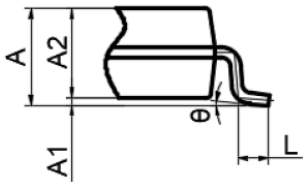
8 Package

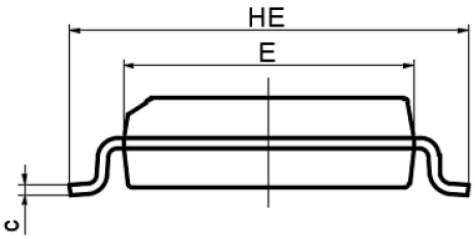
Outline drawing **SOP (PRSP0016DR-A)**	RDK-G-001717-2
	Renesas Electronics Corporation

JEITA Package code	RENESAS code	MASS(TYP.) [g]
P-SOP16 7.5×10.3-1.27	PRSP0016DR-A	0.44[g]

Unit : mm







Reference Symbol	Dimension Millimeters		
	Min	Non	Max
D	10.15	—	10.41
E	7.44	—	7.59
A2	2.24	—	—
HE	10.01	—	10.63
A2	—	—	2.64
A1	0.10	—	0.29
bp	0.33	—	0.51
c	0.23	—	0.32
θ	0°	—	8°
e	—	1.27	—
y	—	—	0.10
L	0.51	—	1.02

9 Revision history

Revision	Date	Page	Changes
1.00	Jan.31.24		Initial release
1.10	Mar.19.24	5	Added VEE recommended operating condition
		13	Added maximum switching frequency
1.20	May.10.24	35	Updated external components

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