RAJ2930104AGM

Gate Driver IC for IGBTs and SiC MOSFETs

Description

The RAJ2930104AGM is a gate driver IC for IGBT and SiC MOSFET gate-drive in high voltage inverter applications. Integrated 3750 V_{RMS} micro-isolators provide data transfer with high voltage isolation between the primary circuit (MCU side) and the secondary circuit (IGBT side). In addition, it boasts superior CMTI (Common Mode Transient Immunity) performance over 150 V/ns, providing reliable communication and increased noise immunity while meeting the high voltages and fast switching speeds required in inverter systems.

This device contains gate drive circuit, miller clamp circuit, and soft turn-off circuit as well as several types of protection circuits such as overcurrent detection.

Part Number	Package	Package Size
RAJ2930104AGM	SOP16	7.5 mm x 10.3 mm



Features

- On-chip micro isolator (Isolated circuit)
  - High voltage isolation: 3750 V_{RMS}, 1 min
  - High Common Mode Transient Immunity (CMTI): over 150 V/ns
- High output gate drive circuit
  - Gate drive output peak current (source/sink): 10 A typ./10 A typ.
  - On-chip active miller clamp
  - Soft turn-off function
- Various on-chip protection circuits
  - Overcurrent detection by current sense: 0.7 V typ.
  - On-chip Under-Voltage Lockout Circuit (UVLO)
    - VCC1 (5 V system): 4.1 V typ.
    - VCC2 (15 V system): 10 V typ.
  - Fault alarm outputs on FOB pin and the latched fault status can be reset by RSTB pin
- Operating temperature: -40 °C to 125 °C (Junction temperature: 150 °C max.)
- AEC-Q100 Qualified (Grade 1)

Applications

- Traction inverters for EV/HEV in automotive applications
- DC-DC converters for EV/HEV in automotive applications
- On-board charger for EV in automotive applications
- Inverters and converters for industrial instruments and so on

© 2024-2026 Renesas Electronics

Contents

1. Pin Information 5
1.1 Pin Assignments 5
1.2 Pin Descriptions 5
2. Specifications 6
2.1 Absolute Maximum Ratings 6
2.2 Recommended Operating Conditions 6
2.3 ESD Specifications 7
2.4 Thermal Specifications 7
2.5 Power Ratings 7
2.6 Insulation Specifications 8
2.7 Safety Limiting Values 8
2.8 Electrical Specifications 9
3. Typical Performance Graphs 12
4. Functional Description 22
4.1 Gate Driver 22
4.1.1 Features 22
4.1.2 Block Diagram 23
4.2 Active Miller Clamp 24
4.2.1 Features 24
4.2.2 Block Diagram 24
4.3 UVLO 25
4.3.1 Features 25
4.3.2 Block Diagram 25
4.4 Current Sense Protection 25
4.4.1 Features 25
4.4.2 Block Diagram 26
4.5 Isolation 26
4.5.1 Features 26
4.5.2 Block Diagram 26
4.6 Thermal Shut Down (TSD) 27
4.6.1 Features 27
4.6.2 Block Diagram 27
4.7 Internal Regulator, Reference Voltage 27
4.7.1 Features 27
4.7.2 Block Diagram 28
5. Application Diagram Examples 29
6. Package Outline Drawings 30
7. Revision History 31

Figures

Figure 1. Pin Assignments 5
Figure 2. External Circuit of the Gate Driver 8
Figure 3. VCC1 UVLO Falling Threshold 12
Figure 4. VCC1 UVLO Rising Threshold 12
Figure 5. VCC2 UVLO Falling Threshold 12
Figure 6. VCC2 UVLO Rising Threshold 12
Figure 7. VCC1 Quiescent Current 12
Figure 8. VCC2 Quiescent Current 12
Figure 9. Peak Output Current High Side 13
Figure 10. Peak Output Current Low Side 13
Figure 11. Miller Clamp Threshold Voltage 13
Figure 12. Output Low Clamp Voltage 13
Figure 13. Output Low Clamp Current 13
Figure 14. Miller Clamp on Delay Time 13
Figure 15. CS Pull-down Current 14
Figure 16. CS Detection Threshold 14
Figure 17. CS Output Low Voltage 14
Figure 18. CS Fault Deglitch Filter 14
Figure 19. CS Propagation Delay to OUTL 90% 14
Figure 20. CS to FOB Low Delay 14
Figure 21. Soft Turn-off on Fault Conditions 15
Figure 22. Propagation Delay Time – High to Low 15
Figure 23. Propagation Delay Time – Low to High 15
Figure 24. Driver Output Rise Time 15
Figure 25. Driver Output Fall Time 15
Figure 26. Timing Diagram of VCC1 UVLO Protection 17
Figure 27. Timing Diagram of VCC2 UVLO Protection 17
Figure 28. Timing Diagram of Current Sense Protection with Soft Turn-off during Turn-on Transition 18
Figure 29. Timing Diagram of Current Sense Protection with Soft Turn-off while Power Device is On 18
Figure 30. Timing Diagram of Active Miller Clamp 19
Figure 31. Timing Diagram of Propagation Delay Time 19
Figure 32. Timing Diagram of On Deglitch Filter 19
Figure 33. Timing Diagram of Off Deglitch Filter 20
Figure 34. Timing Diagram of Power-up Sequence 20
Figure 35. Timing Diagram of Power-down Sequence 21
Figure 36. Internal Block Diagram 22
Figure 37. Block Diagram of Gate Driver 23
Figure 38. Block Diagram of Active Pull-down 23
Figure 39. Block Diagram of Short Circuit Clamping 24
Figure 40. Block Diagram of Active Miller Clamp 24
Figure 41. Block Diagram of UVLO on Primary Chip 25
Figure 42. Block Diagram of UVLO on Secondary Chip 25
Figure 43. Block Diagram of Current Sense 26
Figure 44. Block Diagram of Isolation 26
Figure 45. Block Diagram of Thermal Shut Down 27
Figure 46. Block Diagram of Reference Voltage on Primary Chip 28
Figure 47. Block Diagram of Internal Regulator and Reference Voltage on Secondary Chip 28
Figure 48. Simplified Application Diagram for IGBT 29

Figure 49. Simplified Application Diagram for SiC MOSFET 29

Tables

Table 1. Pin Descriptions 5
Table 2. Absolute Maximum Ratings 6
Table 3. Recommended Operating Conditions 6
Table 4. ESD Specifications 7
Table 5. Thermal Specifications 7
Table 6. Power Ratings 7
Table 7. Insulation Specifications 8
Table 8. Safety Limiting Values 8
Table 9. Electrical Specifications 9
Table 10. Switching Characteristics 11
Table 11. Thermal Shutdown Characteristics 11
Table 12. Function Table 16
Table 13. Recommended Drive Method 16
Table 14. Specifications of External Components 29

1. Pin Information

1.1 Pin Assignments

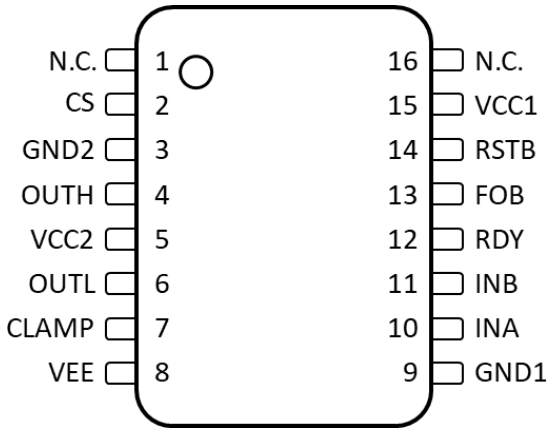


Figure 1. Pin Assignments

1.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	I/O	Description
1	N.C.	-	Non-connection. The pin can be applied in either open or VEE connection.
2	CS	I	Current sense input.
3	GND2	P	Secondary side GND. Connect to IGBT emitter.
4	OUTH	O	Gate drive output (Positive).
5	VCC2	P	Secondary power supply input (15 V typ).
6	OUTL	O	Gate drive output (Negative).
7	CLAMP	I/O	Active miller clamp input/output.
8	VEE	P	Negative power supply input. Connect to GND2 for unipolar supply application.
9	GND1	P	Primary side GND.
10	INA	I	Non-inverted gate drive input.
11	INB	I	Inverted gate drive input.
12	RDY	O	Power-good output.
13	FOB	O	Inverted fault output (L level output at error).
14	RSTB	I	Reset input. Apply a low pulse to reset fault (FOB) latch.
15	VCC1	P	Primary side power supply input (5 V typ)
16	N.C.	-	Non-connection. The pin can be applied in either open or GND1 connection.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
VCC1 – GND1	VCC1	–0.3	6	V
VCC2 – GND2	VCC2	–0.3	36	V
VEE – GND2	VEE	–17.5	0.3	V
VCC2 – VEE	V_{MAX}	–0.3	36	V
Digital inputs	INA, INB, RSTB	GND1–0.3	VCC1+0.3	V
Reference to GND2	CS	GND2–0.3	VCC2+0.3	V
Outputs	OUTH, OUTL, CLAMP	VEE–0.3	VCC2+0.3	V
Peak source current	I_{OUTH}	-15	-	A
Peak sink current	I_{OUTL}	-	15	A
Digital outputs	RDY, FOB	GND1–0.3	VCC1+0.3	V
FOB, and RDY pin input current	I_{FOB}, I_{RDY}	-	20	mA
Junction temperature range	T_J	-40	150	°C
Storage temperature range	T_{STG}	-55	150	°C
Slew rate of VCC1 for no destruction	VCC1SR1	-	20	V/µs
Slew rate of VCC2 for no destruction	VCC2SR1	-	20	V/µs
Slew rate of VEE for no destruction	VEESR1	-20	-	V/µs

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
VCC1 – GND1	VCC1	4.5	5.5	V
VCC2 – GND2	VCC2	12.5	33	V
VCC2 – VEE	VMAX	12.5	33	V
VEE – GND2	VEE	-16.5	0	V
Reference to GND1, high level input voltage	INA, INB, RSTB	0.7×VCC1	VCC1	V
Reference to GND1, low level input voltage		0	0.3×VCC1	V
Ambient temperature	T_A	-40	125	°C
Junction temperature	T_J	-40	150	°C
Slew rate of VCC1 for no change parameters	$VCC1_{SR2}$	-	0.5	V/µs
Slew rate of VCC2 for no change parameters	$VCC2_{SR2}$	-	0.5	V/µs
Slew rate of VEE for no change parameters	VEE_{SR2}	-0.5	-	V/µs

2.3 ESD Specifications

Table 4. ESD Specifications

Parameter	Symbol	Condition	Typical Value	Unit
Electrostatic discharge	V(ESD)	Human Body Model (HBM), per AEC Q100-002	±2000	V
		Charged Device Model (CDM), per AEC Q100-011	±750 (Corner pins) ±500 (Other pins)	V

2.4 Thermal Specifications

Table 5. Thermal Specifications

Parameter	Symbol	Value	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$[1][4]	64.9	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$[3][4]	27.8	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$[2][4]	33.4	°C/W
Junction-to-top characterization parameter	ψ_{JT}[1][4]	9.4	°C/W
Junction-to-board characterization parameter	ψ_{JB}[1][4]	31.8	°C/W

1. $R_{\theta JA}$, ψ_{JT}, ψ_{JB}: Based on JESD51-2 environment, JESD51-7 test board (4-layer board)
2. $R_{\theta JB}$: Based on JESD51-8 environment
3. $R_{\theta JC(top)}$: Based on MIL-STD-883 method 1012.1 described in JESD51-12
4. The thermal parameters were obtained by simulation and the figures are reference values.

2.5 Power Ratings

Table 6. Power Ratings

Parameter	Symbol	Conditions	Value	Unit
Maximum power dissipation (both sides)	P_D	VCC1 = 5 V, VCC2-GND2 = 20 V, GND2-VEE = 5 V, INA/INB = 5 V, 150 kHz, 50% Duty Cycle for 10 nF load, T_A = 25 °C, T_J = 150 ℃	1926	mW
Maximum power dissipation by transmitter side	P_{D1}		20	mW
Maximum power dissipation by receiver side	P_{D2}		1906	mW

2.6 Insulation Specifications

Table 7. Insulation Specifications

Parameter	Symbol	Conditions	Value	Unit
Withstand isolation voltage	V_{ISO}[1]	$V_{TEST} = V_{ISO} = 3750\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 4500\ V_{RMS}$, t = 1 s (100% production)	3750	V_{RMS}
Maximum isolation working voltage	V_{IOWM}[2]	AC voltage (sine wave) Time Dependent Dielectric Breakdown (TDDB) test	970	V_{RMS}
		DC voltage	1375	V_{DC}
Insulation resistance, input to output	R_{IO}[2]	V_{IO} = 500 V, T_S = 150°C	≥ 10^9	Ω

1. Refer to UL 1577.
2. Refer to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01.

2.7 Safety Limiting Values

Table 8. Safety Limiting Values

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Safety input, output, or supply current	I_S	$R_{\theta JA}$ = 64.9°C/W, V_{CC2} = 15 V, V_{EE} = 5 V, T_J = 150°C, T_A = 25°C	-	-	96	mA
		$R_{\theta JA}$ = 64.9°C/W, V_{CC2} = 20 V, V_{EE} = 5 V, T_J = 150°C, T_A = 25°C	-	-	77	mA
Safety input, output, or total power	P_S	$R_{\theta JA}$ = 64.9°C/W, V_{CC2} = 20 V, V_{EE} = 5 V, T_J = 150°C, T_A = 25°C	-	-	1926	mW
Safety temperature	T_S		-	-	150	°C

The external circuit of the gate driver is displayed in the following figure. RON = ROFF = 0 Ω and CL = 100 pF unless otherwise noted.

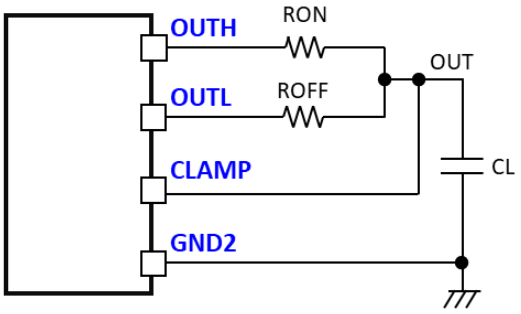


Figure 2. External Circuit of the Gate Driver

2.8 Electrical Specifications

VCC1 = 5 V, VCC2 - GND2 = 20 V, GND2 – VEE = 0 V, CL = 100 pF, -40 °C <T_J <150 °C unless otherwise noted.

Table 9. Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC1 UVLO Threshold and Delay						
VCC1–GND1	V_{VCC1_ON}		3.9	4.2	4.5	V
	V_{VCC1_OFF}		3.8	4.1	4.4	V
	V_{VCC1_HYS}		-	0.1	-	V
VCC1 UVLO on delay to output high	$t_{VCC1+ to OUT}$	INA = VCC1, INB = GND1	15	30	60	µs
VCC1 UVLO off delay to output low	$t_{VCC1- to OUT}$	VCC1 > 3.6V	5	10	25	µs
VCC1 UVLO on delay to RDY high	$t_{VCC1+ to RDY}$	RSTB = VCC1	15	30	60	µs
VCC1 UVLO off delay to RDY low	$t_{VCC1- to RDY}$		5	10	25	µs
VCC2 UVLO Threshold and Delay						
VCC2–GND2	V_{VCC2_ON}		10	11	12	V
	V_{VCC2_OFF}		9	10	11	V
	V_{VCC2_HYS}		-	1.0	-	V
VCC2 UVLO on delay to output high	$t_{VCC2+ to OUT}$	INA= VCC1, INB = GND1 SR of VCC2 = 10 mV/µs	-	10	20	µs
VCC2 UVLO off delay to output low	$t_{VCC2- to OUT}$		-	5	15	µs
VCC2 UVLO on delay to RDY high	$t_{VCC2+ to RDY}$	RSTB = FOB=High SR of VCC2 = 10 mV/µs	-	10	20	µs
VCC2 UVLO off delay to RDY low	$t_{VCC2- to RDY}$		-	10	20	µs
VCC1, VCC2 Quiescent Current						
VCC1 quiescent current	I_{VCC1Q}	OUTH = High, f_S = 0 Hz	1.45	2	3.2	mA
		OUTL = Low, f_S = 0 Hz	1.45	2	3.2	mA
VCC2 quiescent current	I_{VCC2Q}	OUTH = High, f_S = 0 Hz	2.0	4	5.9	mA
		OUTL = Low, f_S = 0 Hz	2.0	3.7	5.3	mA
LOGIC Inputs — INA, INB, and RSTB						
Input high threshold	V_{INH}	VCC1 = 5 V	0.7×VCC1	-	-	V
Input low threshold	V_{INL}	VCC1 = 5 V	-	-	0.3×VCC1	V
Input threshold hysteresis	V_{IN_HYS}	VCC1 = 5 V	-	0.12×VCC1	-	V
LOGIC Inputs – INA, INB, and RSTB						
Input pins pull-down resistance	R_{IND}	INA = VCC1 RSTB = VCC1	-	55	-	kΩ
Input pins pull-up resistance	R_{INU}	INB = GND1	-	55	-	kΩ
INA, INB and RSTB deglitch (ON and OFF) filter time	t_{INFIL}	f_S = 50 kHz	28	40	60	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Deglitch filter time to reset FOB	t_{RSTFIL}		1.0	-	8.0	us
Gate Driver Stage						
Peak source current	I_{OUTH}	CL = 0.18 µF, f_S = 1 kHz	-	-10	-	A
Peak sink current	I_{OUTL}		-	10	-	A
Output pull-up resistance	R_{OUTH}	I_{OUTH} = -0.1 A	-	2.5	-	Ω
Output pull-down resistance	R_{OUTL}	I_{OUTL} = 0.1 A	-	0.3	-	Ω
Active Pull-Down						
Output active pull-down on OUTL	V_{OUT_PD}	I_{OUTL} = 1 A (IOUTL(typ)x0.1), VCC2 = OPEN	-	-	2.5	V
Internal Active Miller Clamp						
Miller clamp threshold voltage	$V_{CLAMPTH}$	Reference to VEE	1.5	2	2.5	V
Output low clamp voltage	V_{CLAMP}	I_{CLAMP} = 1 A	-	VEE + 0.5	-	V
Output low clamp current	I_{CLAMP}	CLAMP = 0 V, VEE = -2.5 V	-	4	-	A
Miller clamp pull-down resistance	R_{CLAMP}	I_{CLAMP} = 0.2 A	-	0.6	-	Ω
Miller clamp ON delay time	t_{DCLAMP}	CL = 1.8 nF	-	15	50	ns
Short Circuit Clamping						
OUTH-VCC2	V_{CLP_OUTH}	I_{OUTH} = 500 mA, t_{CLP} = 10 µs	-	0.8	1.0	V
OUTL-VCC2	$V_{CLP-OUTL}$	I_{OUTL} = 500 mA, t_{CLP} = 10 µs	-	1.55	1.8	V
CLAMP-VCC2	$V_{CLP-CLAMP}$	I_{CLAMP} = 20 mA, t_{CLP} = 10 µs	-	0.9	-	V
Overcurrent Protection with Current Sense						
CS pull-down current	I_{DCHG}	CS = 1 V	-	40	-	mA
CS detection threshold	V_{CSTH}		0.63	0.7	0.77	V
CS output low voltage	V_{CSL}	ICS = 5 mA, Reference to GND2	-	0.13	-	V
CS fault deglitch filter	t_{CSFIL}		50	140	230	ns
CS propagation delay to OUTL 90%	t_{CSOFF}		60	220	300	ns
CS to FOB low delay	t_{CSFOB}		60	400	1600	ns
Internal Soft Turn-off						
Soft turn-off current on fault conditions	I_{STO}	OUTL = VEE + 8 V	250	400	570	mA
FOB and RDY Reporting						
VCC1 and VCC2 UVLO RDY low minimum holding time	t_{RDYHLD}		0.20	-	1	ms
Output mute time on fault	$t_{FOBMUTE}$	Reset fault through RSTB	0.20	-	1	ms
Open drain low output voltage	V_{ODL}	IODON = 5 mA	-	-	0.3	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Common Mode Transient Immunity						
Common-mode transient immunity	CMTI		150	-	-	V/ns

VCC1 = 5 V, VCC2 - GND2 = 20 V, GND2 – VEE = 0 V, CL = 100 pF, -40 °C <T_J <150 °C unless otherwise noted.

Table 10. Switching Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Propagation delay time – high to low	t_{PDHL}	CL = 100 pF	30	70	140	ns
Propagation delay time – low to high	t_{PDLH}	CL = 100 pF	30	70	140	ns
Pulse width distortion $\lvert t_{PDHL} - t_{PDLH} \rvert$	PWD		-	-	30	ns
Part-to-part skew	t_{sk-pp}	Rising or falling propagation delay difference due to process deviation	-	-	50	ns
Driver output rise time	t_r	CL = 10 nF	-	33	-	ns
Driver output fall time	t_f	CL = 10 nF	-	27	-	ns
Maximum switching frequency	f_{Smax}		-	1	-	MHz

Table 11. Thermal Shutdown Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal shutdown temperature	T_{TSD}		150	175	200	°C
Thermal shutdown recover temperature	T_{TSDREC}		120	150	180	°C
Thermal shutdown hysteresis temperature	T_{TSDHYS}		15	25	35	°C

3. Typical Performance Graphs

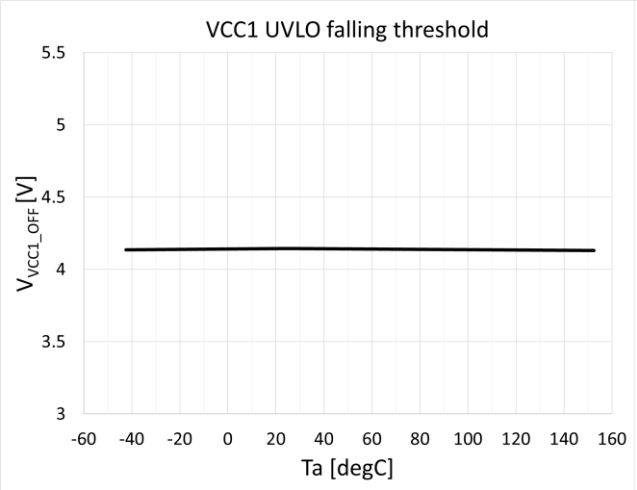


Figure 3. VCC1 UVLO Falling Threshold

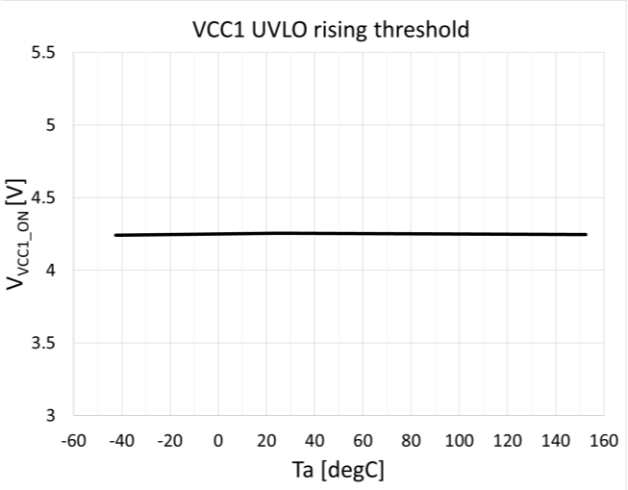


Figure 4. VCC1 UVLO Rising Threshold

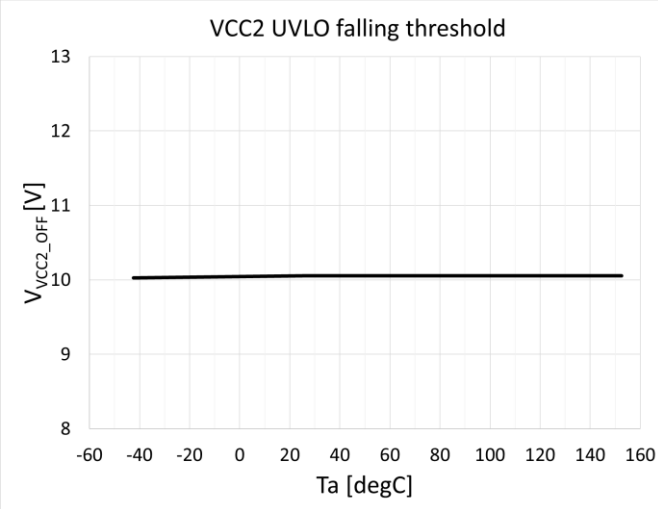


Figure 5. VCC2 UVLO Falling Threshold

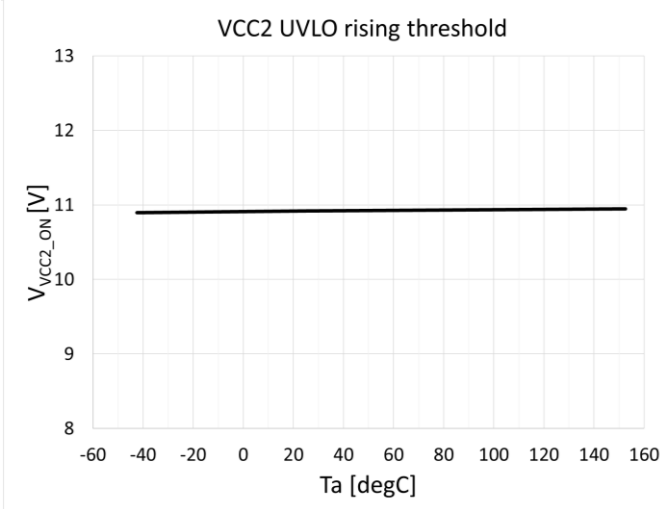


Figure 6. VCC2 UVLO Rising Threshold

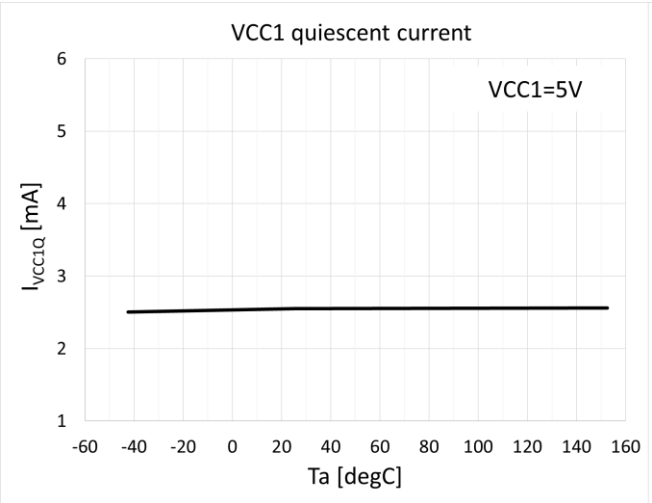


Figure 7. VCC1 Quiescent Current

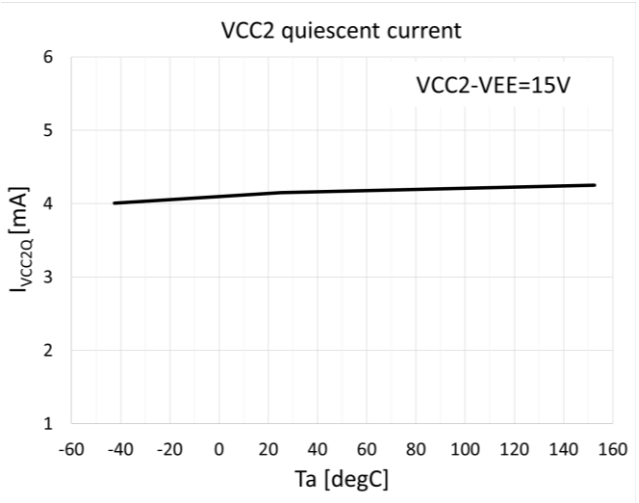


Figure 8. VCC2 Quiescent Current

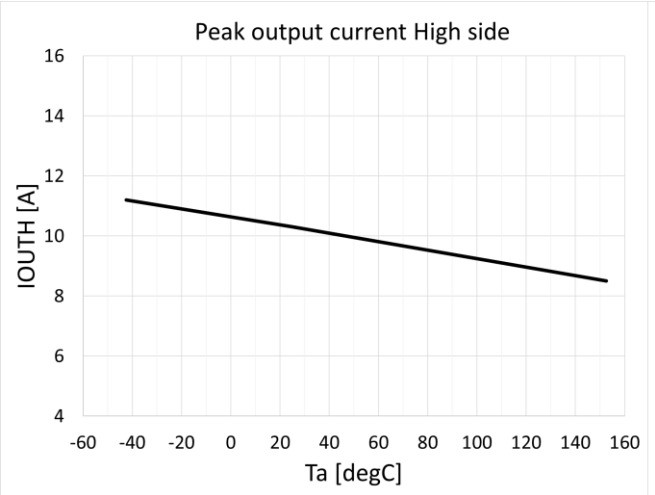


Figure 9. Peak Output Current High Side

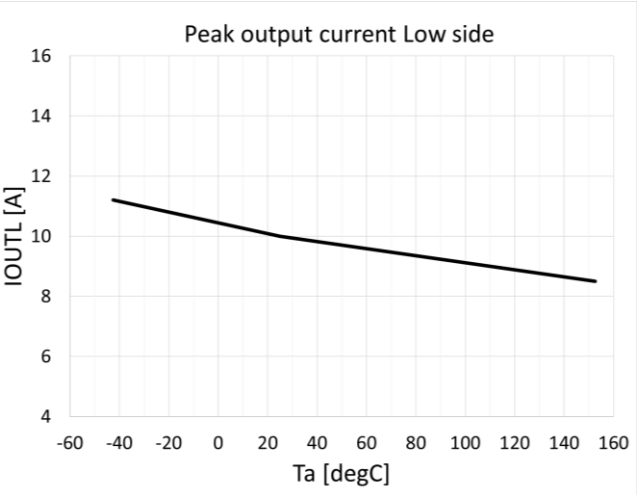


Figure 10. Peak Output Current Low Side

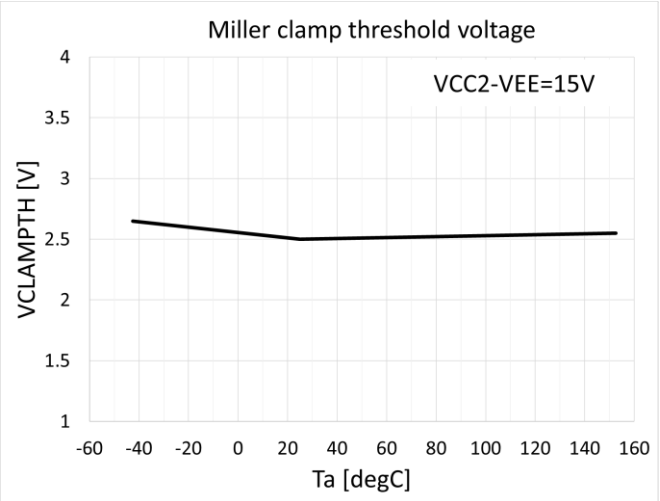


Figure 11. Miller Clamp Threshold Voltage

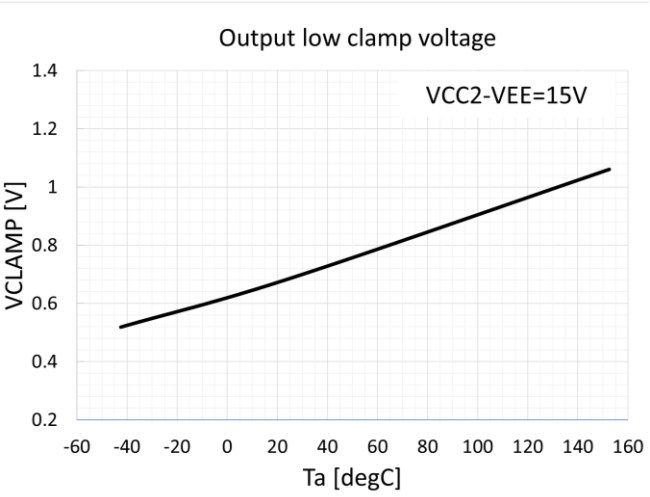


Figure 12. Output Low Clamp Voltage

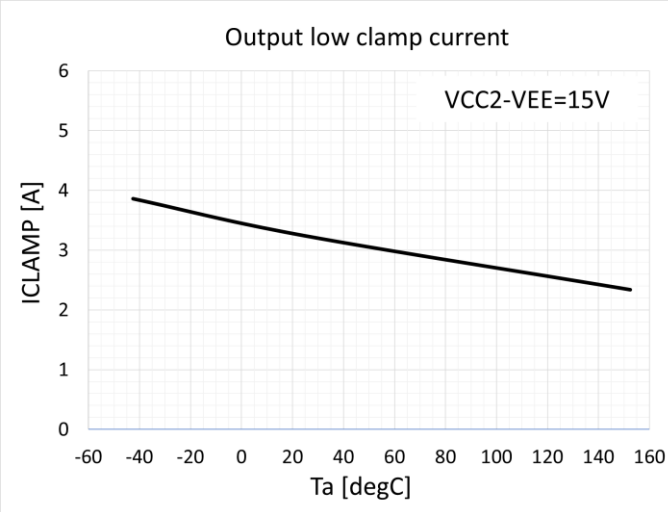


Figure 13. Output Low Clamp Current

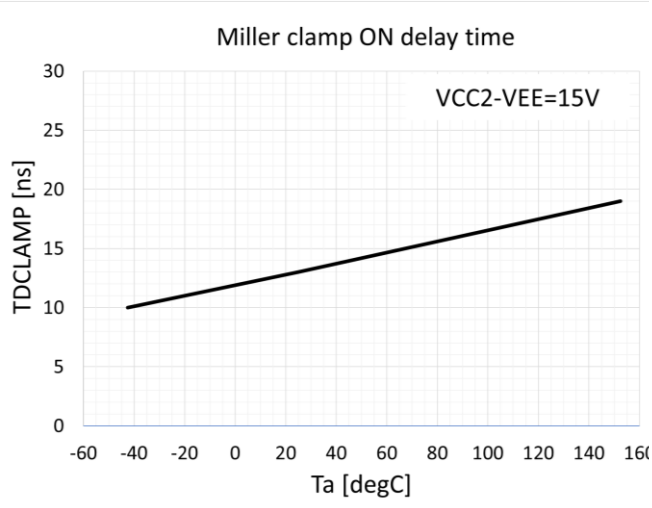


Figure 14. Miller Clamp on Delay Time

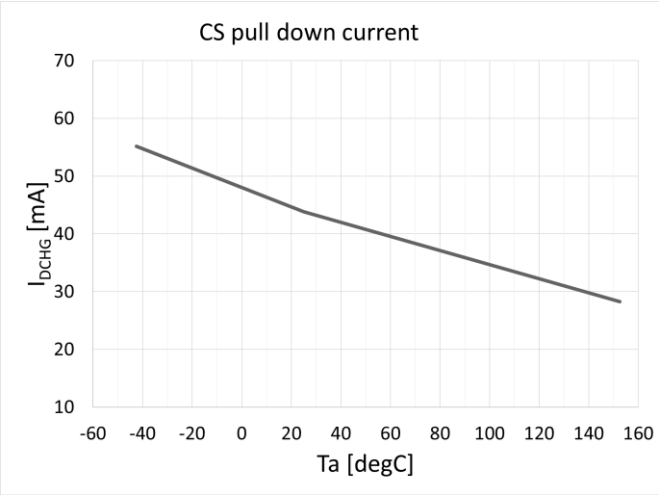


Figure 15. CS Pull-down Current

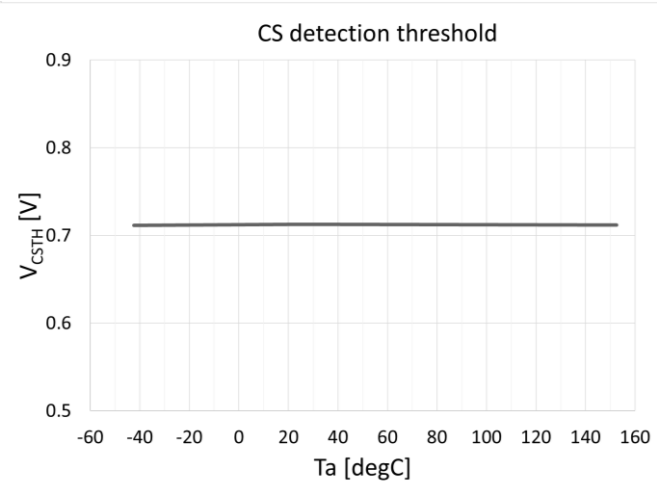


Figure 16. CS Detection Threshold

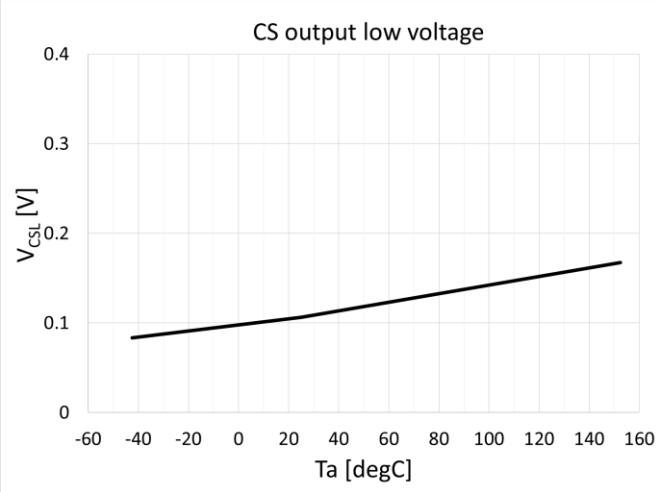


Figure 17. CS Output Low Voltage

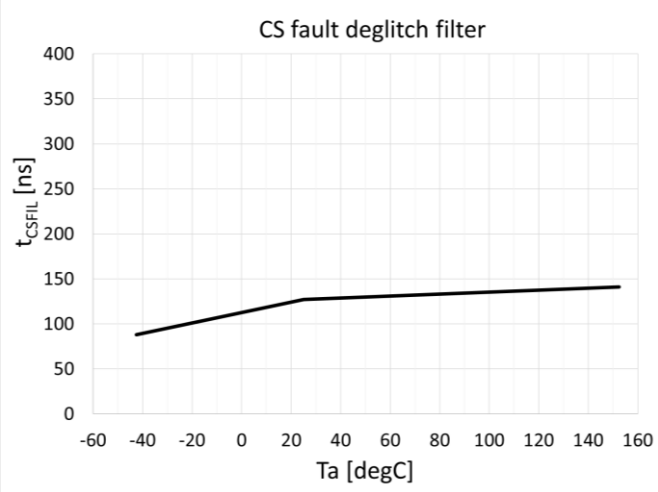


Figure 18. CS Fault Deglitch Filter

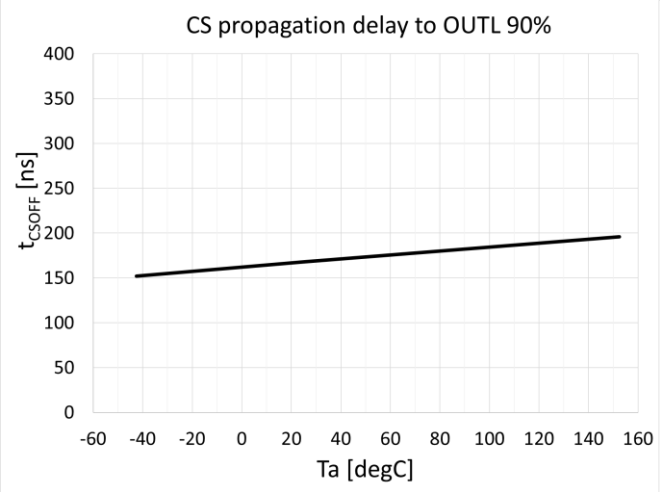


Figure 19. CS Propagation Delay to OUTL 90%

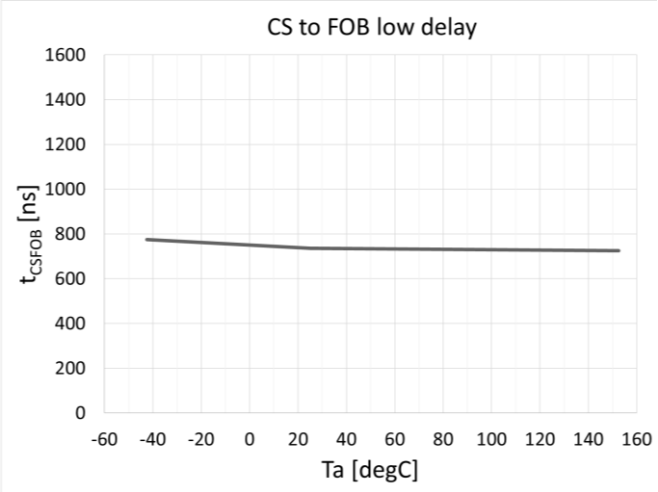


Figure 20. CS to FOB Low Delay

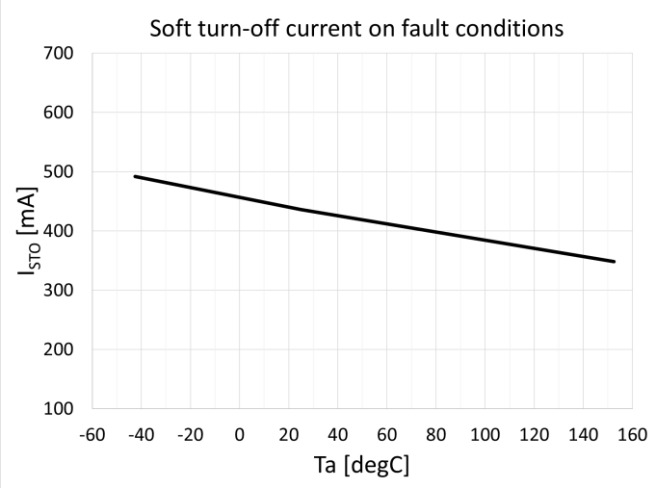


Figure 21. Soft Turn-off on Fault Conditions

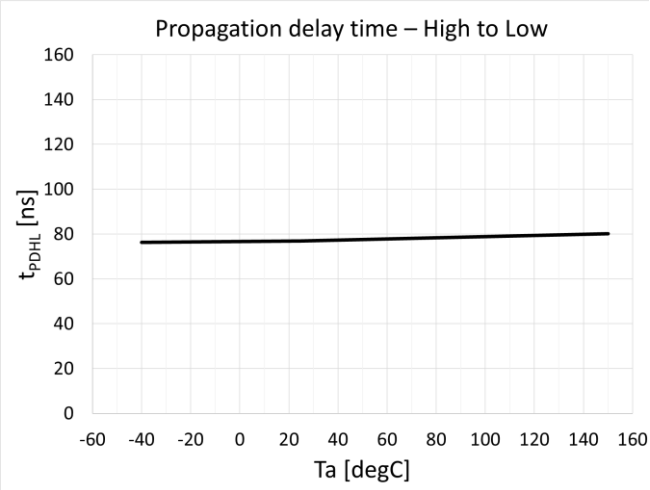


Figure 22. Propagation Delay Time – High to Low

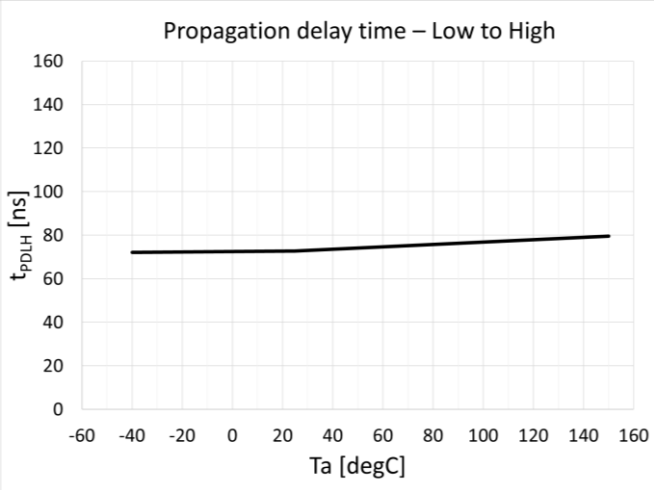


Figure 23. Propagation Delay Time – Low to High

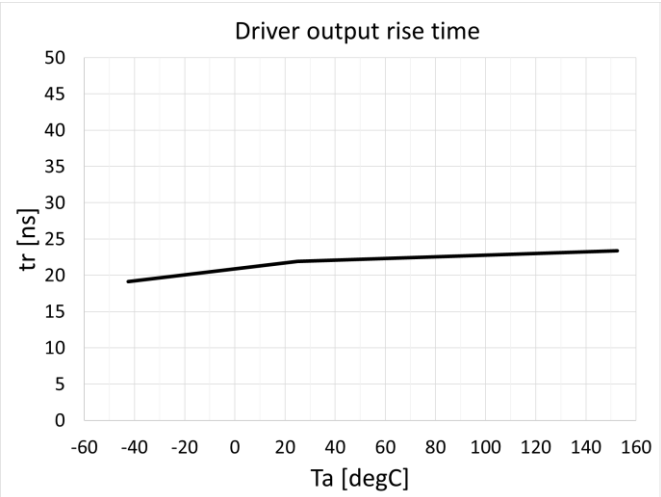


Figure 24. Driver Output Rise Time

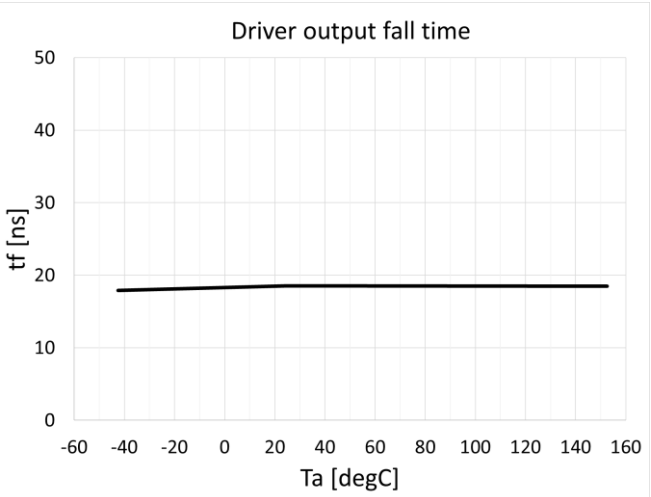


Figure 25. Driver Output Fall Time

Table 12. Function Table

		Supply			Input				Output			
No.	State	VCC1	VCC2	VEE	Latched fault[1]	RSTB	INA	INB	RDY	FOB	OUTH/ OUTL	CLAMP
1	VCC1 UVLO	PD	PU	PU	X	X	X	X	Low	HiZ	Low	Low
2	VCC2 UVLO	PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low
3	VCC2 Open	PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ
4	Current Sense and TSD	PU	PU	PU	Yes	X	X	X	HiZ	Low	Soft turn-off	Low
5	Reset	PU	PU	PU	No	Low	X	X	HiZ	HiZ	Low	Low
6	Normal operation	PU	PU	PU	No	High	Low	X	HiZ	HiZ	Low	Low
7		PU	PU	PU	No	High	X	High	HiZ	HiZ	Low	Low
8		PU	PU	PU	No	High	High	High	HiZ	HiZ	Low	Low
9		PU	PU	PU	No	High	High	Low	HiZ	HiZ	High	HiZ

1. The latched fault is reset at the rising edge of RSTB.
2. PU: Power Up (VCC1 ≥ 4.5 V, VCC2 ≥ 12 V); PD: Power Down (3.2 V ≤ VCC1 ≤ 3.8 V, VCC2 ≤ 9 V); X: Irrelevant; HiZ: High Impedance

To drive the power devices, the following methods are recommended (see Table 13):

1. Fix the INA to L and use the INB to drive the power device.
2. Fix the INB to H and use the INA to drive the power device.
3. Make the INA and INB in a opposite phases to drive the power device.

Table 13. Recommended Drive Method

#	INA	INB	OUTH/OUTL	Power Device State
1	L	X	L	OFF
2	X	H	L	OFF
3	H	L	H	ON

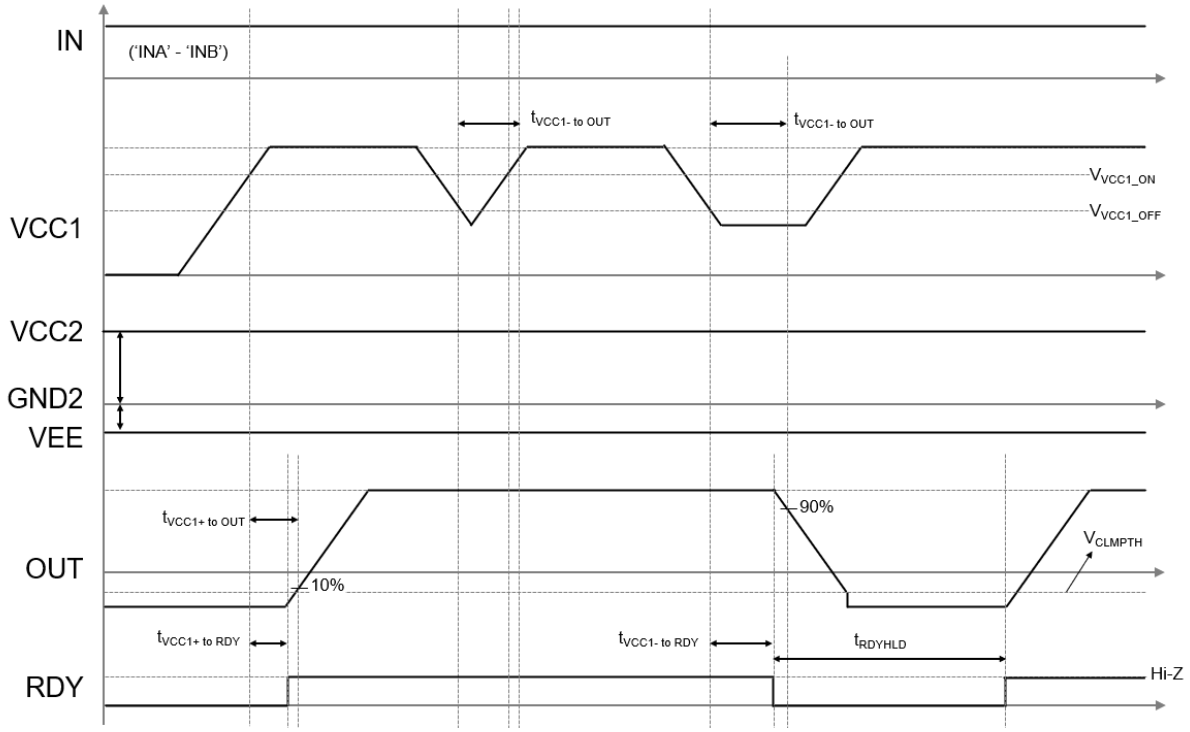


Figure 26. Timing Diagram of VCC1 UVLO Protection

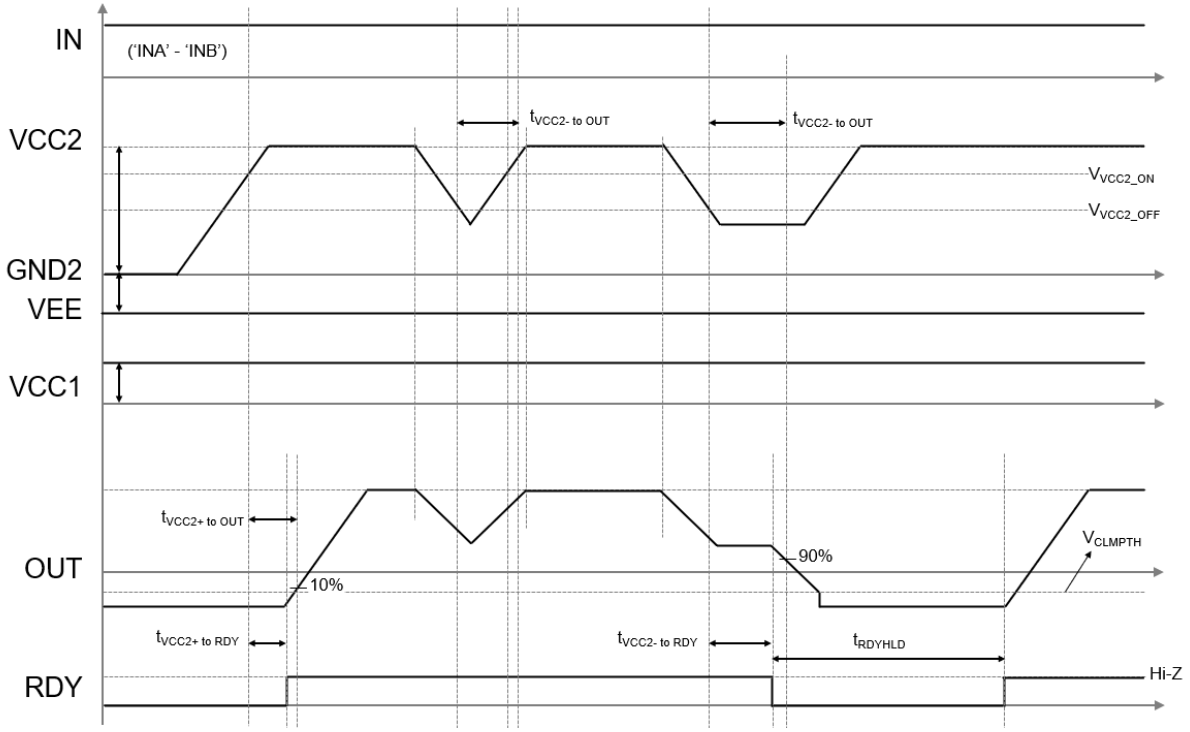


Figure 27. Timing Diagram of VCC2 UVLO Protection

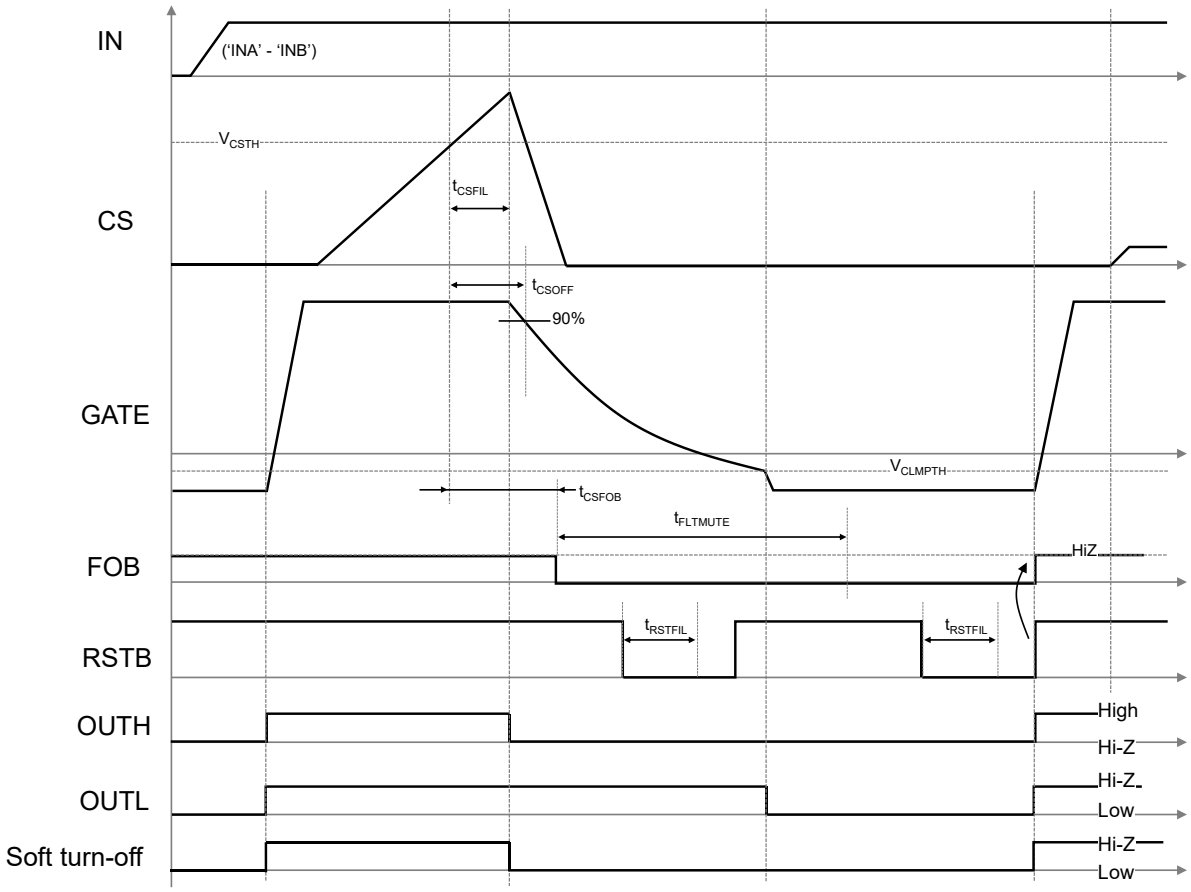


Figure 28. Timing Diagram of Current Sense Protection with Soft Turn-off during Turn-on Transition

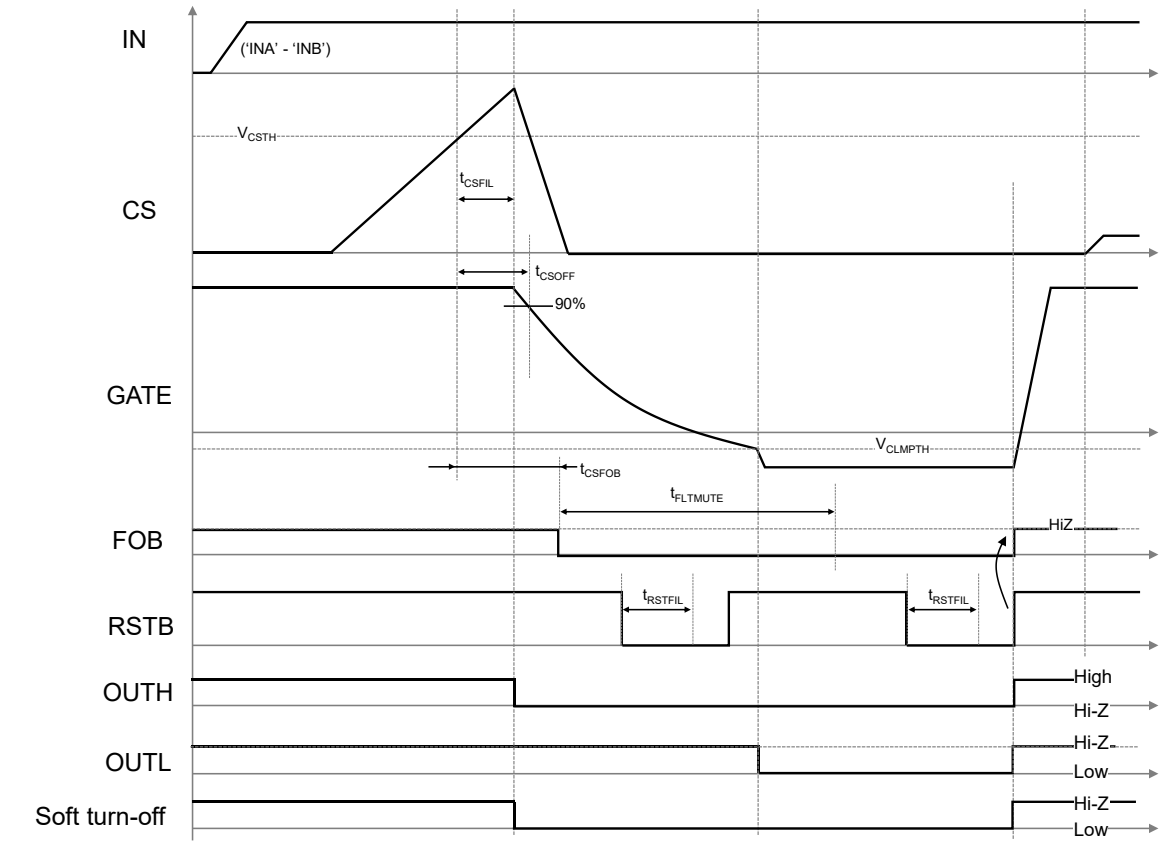


Figure 29. Timing Diagram of Current Sense Protection with Soft Turn-off while Power Device is On

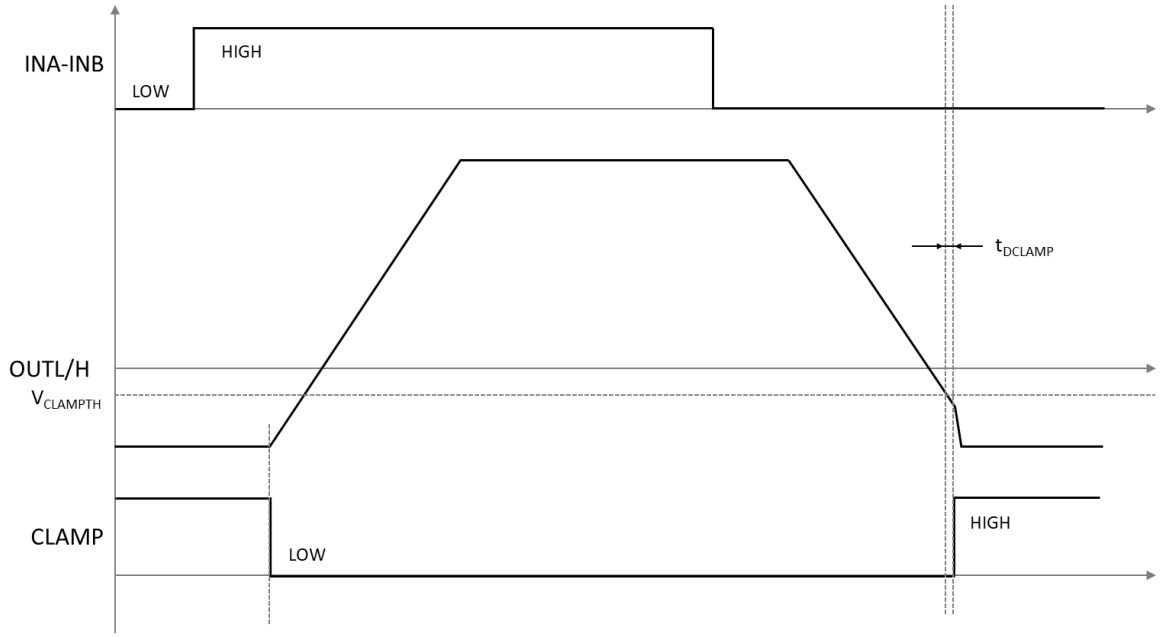


Figure 30. Timing Diagram of Active Miller Clamp

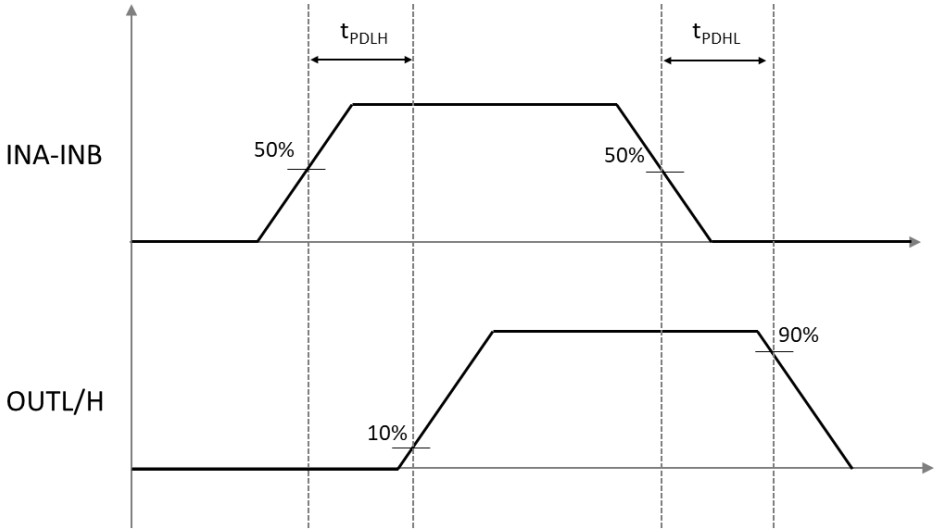


Figure 31. Timing Diagram of Propagation Delay Time

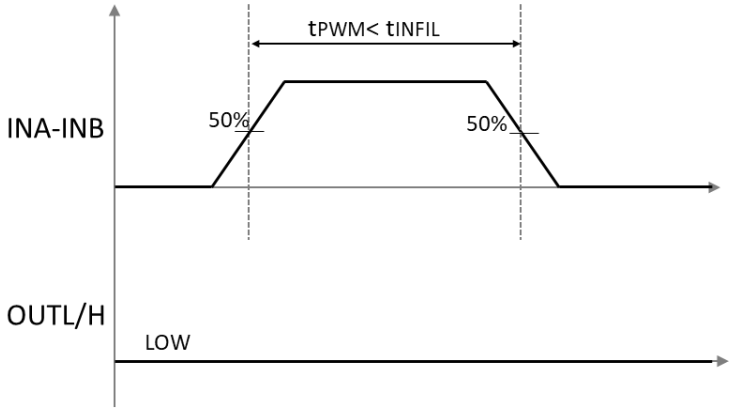


Figure 32. Timing Diagram of On Deglitch Filter

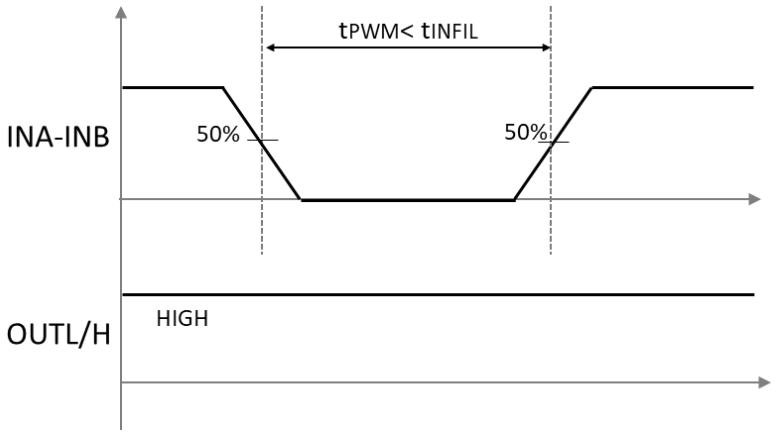


Figure 33. Timing Diagram of Off Deglitch Filter

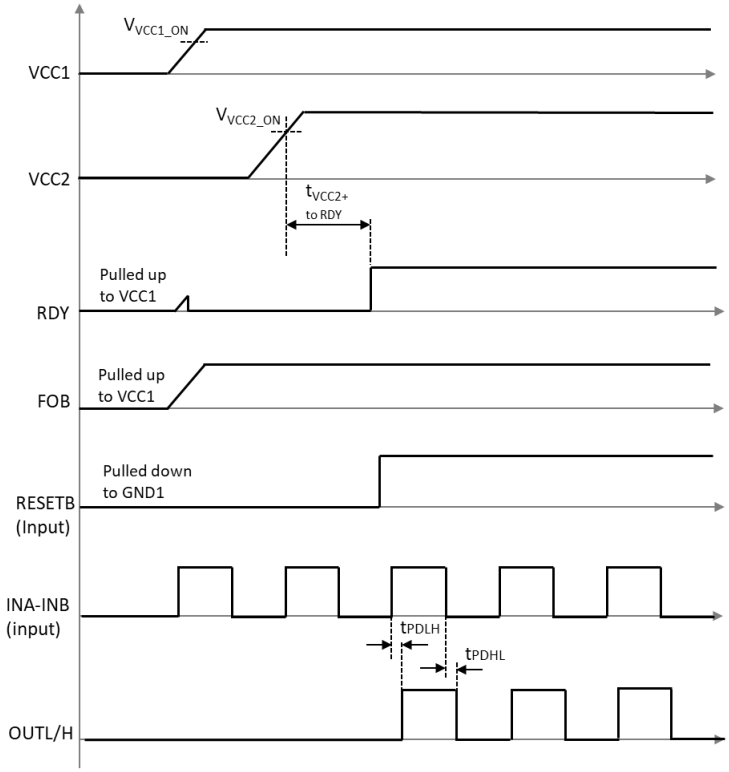


Figure 34. Timing Diagram of Power-up Sequence

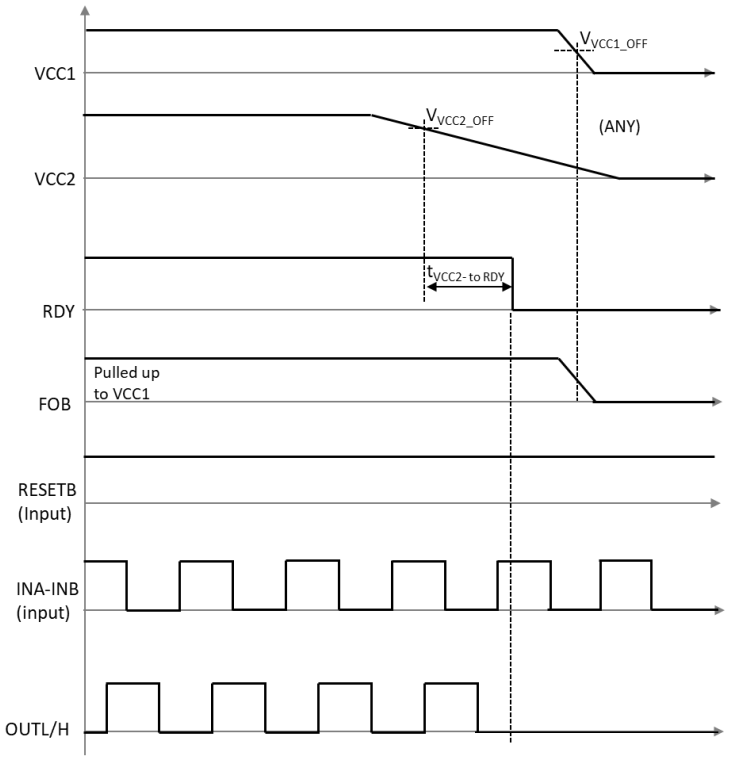


Figure 35. Timing Diagram of Power-down Sequence

4. Functional Description

The internal block of the RAJ2930004AGM is shown in the following figure.

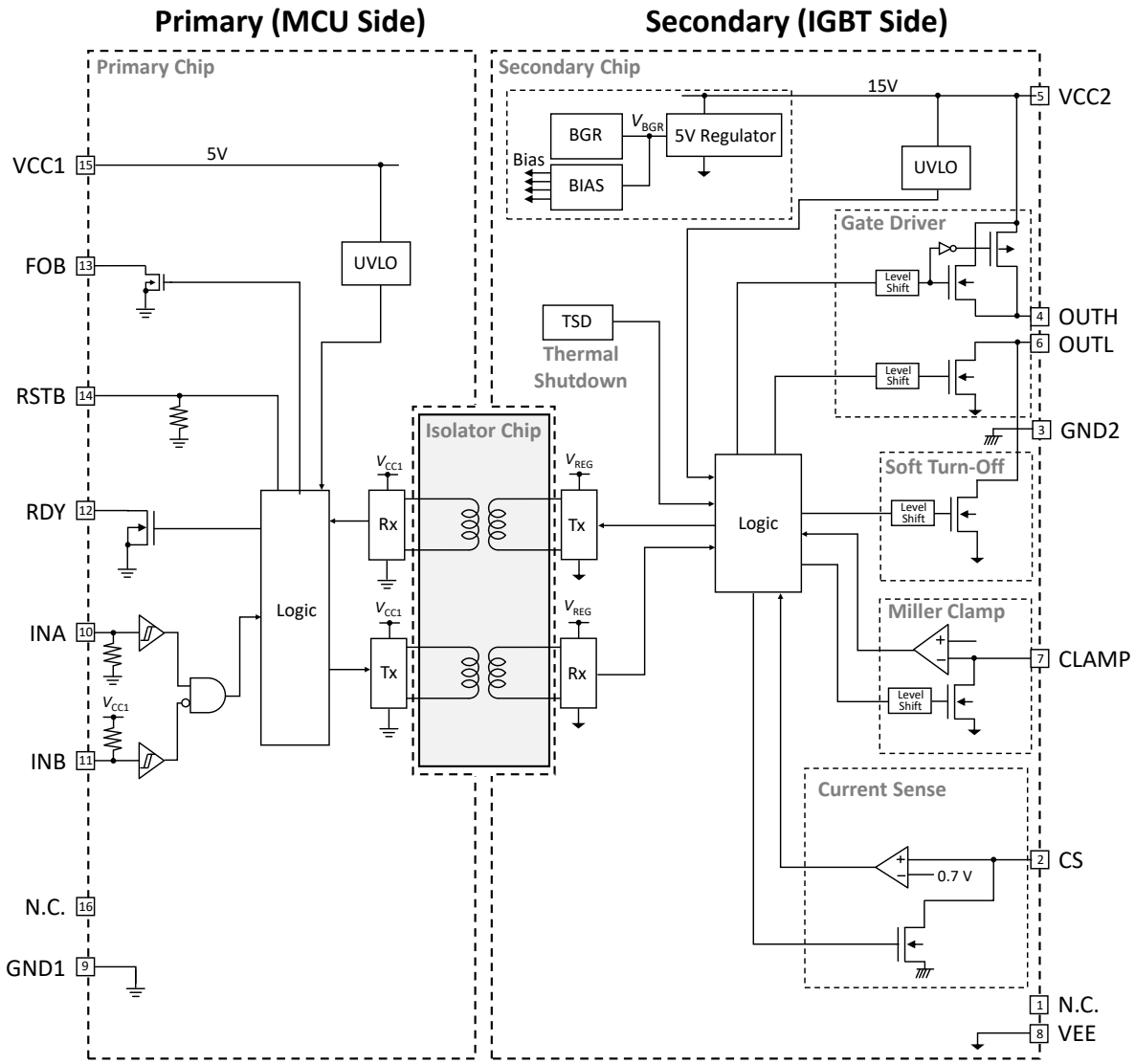


Figure 36. Internal Block Diagram

4.1 Gate Driver

4.1.1 Features

The gate driver charges or discharges the IGBT gate pins. Gate drive output peak current (Source/Sink): 10 A (Typ)/10 A (Typ).

Since the high-side gate drive output pin OUTH and the low-side gate drive output pin OUTL are independent of each other, the slew rates of the rise and fall of the gate voltage can be separately adjusted using the external resistors (RGH and RGL).

The soft turn-off is the feature to lower the gate voltage of the IGBT gradually and turn it off when any of the following abnormal states are detected on the secondary circuit: DESAT or TSD.

The RSTB can resume switching operation when the abnormal states that caused soft turn-off return to normal.

Active pull-down resistance can clamp the OUTL pin to VEE when VCC2 is open (see Figure 38).

Short circuit clamping diodes can clamp the OUTH/OUTL/CLAMP pins to VCC2 + V_f when the short circuit event occurs and the current input to the pins (see Figure 39).

4.1.2 Block Diagram

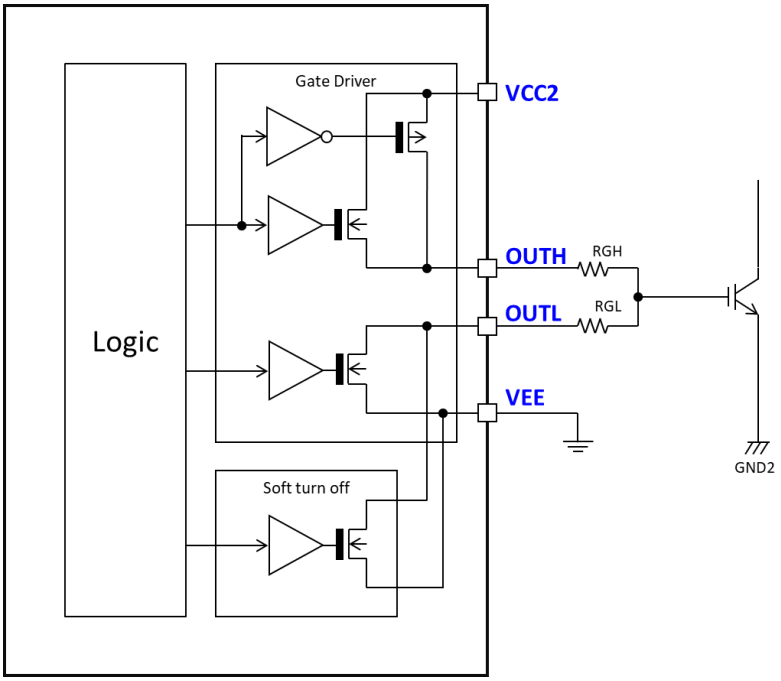


Figure 37. Block Diagram of Gate Driver

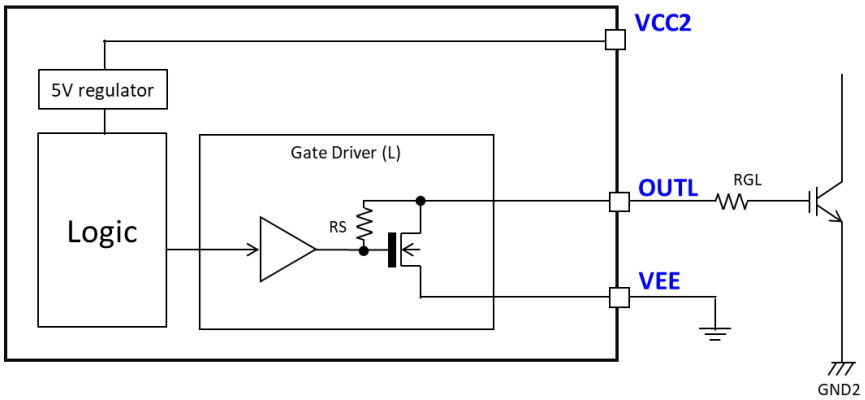


Figure 38. Block Diagram of Active Pull-down

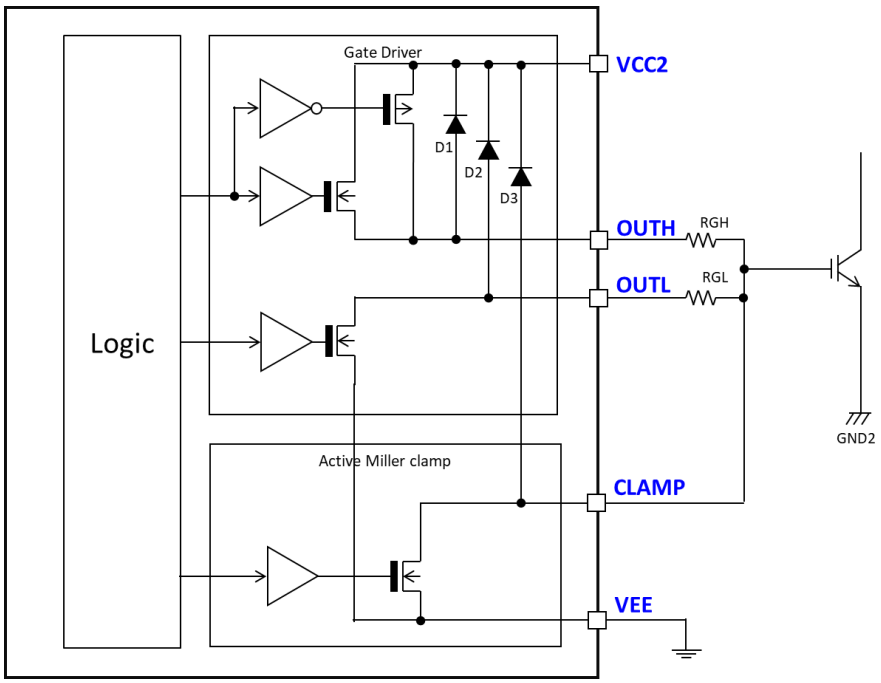


Figure 39. Block Diagram of Short Circuit Clamping

4.2 Active Miller Clamp

4.2.1 Features

The active miller clamp prevents the self turn-on of the IGBT due to the coupling capacitance between the IGBT gate and collector.

If the CLAMP pin voltage falls below VCLAMP (2.0 V typ.) while the input signal to turn off the IGBT is applied to the INA or INB pin, the IGBT gate is short circuited to the VEE pin with low resistance.

4.2.2 Block Diagram

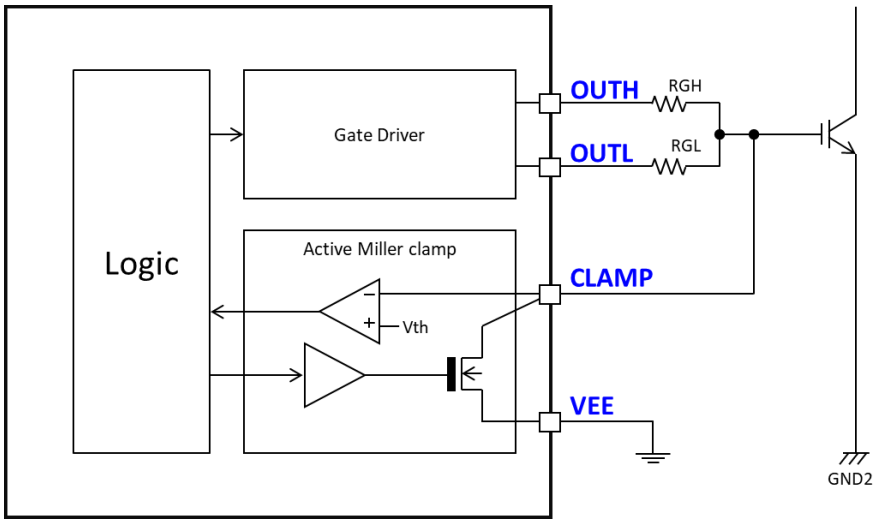


Figure 40. Block Diagram of Active Miller Clamp

4.3 UVLO

4.3.1 Features

The primary circuit is equipped with a UVLO that detects a voltage drop of VCC1; the UVLO turns off the IGBT (this is a normal turn-off operation different from a soft turn-off) when the VCC1 voltage drops below 4.1 V. At this time, the low level is output to the RDY pin of the primary circuit.

The secondary circuit is equipped with a UVLO that detects the voltage drop of VCC2 and a UVLO that detects the voltage drop of VREG (output from 5 V regulator). The IGBT is turned off if the VCC2 voltage drops below 10 V or the VREG voltage drops below 4.1 V. At this time, the low level is output to the RDY pin of the primary circuit.

4.3.2 Block Diagram

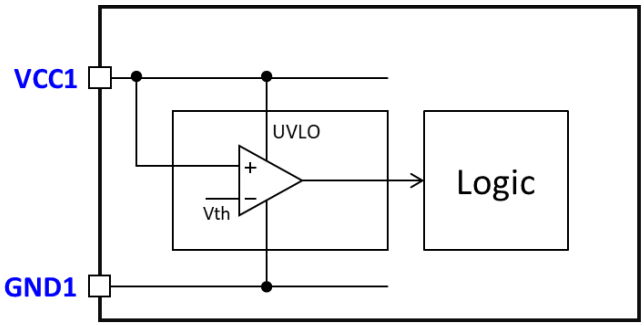


Figure 41. Block Diagram of UVLO on Primary Chip

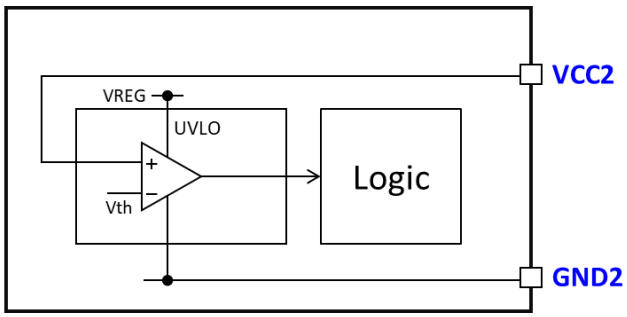


Figure 42. Block Diagram of UVLO on Secondary Chip

4.4 Current Sense Protection

4.4.1 Features

Circuit Sense Protection turns off the output from the gate driver if the overcurrent is detected by current sense.

The IGBT is soft turned off if the voltage applied to the CS pin rises beyond the threshold voltage 0.7 V ± 10% when the IGBT is in the on-state. At this time, the low level is output to the FOB pin of the primary circuit.

4.4.2 Block Diagram

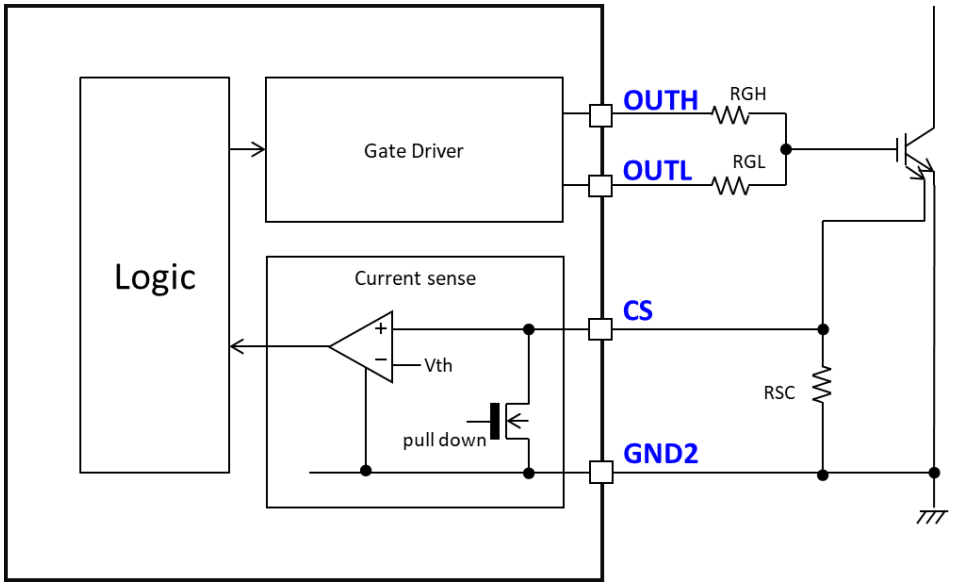


Figure 43. Block Diagram of Current Sense

4.5 Isolation

4.5.1 Features

- On-chip micro isolator (Isolated circuit)
- High voltage isolation: 3750 V_{RMS}, 1 min
- High CMTI: over 150 kV/μs

4.5.2 Block Diagram

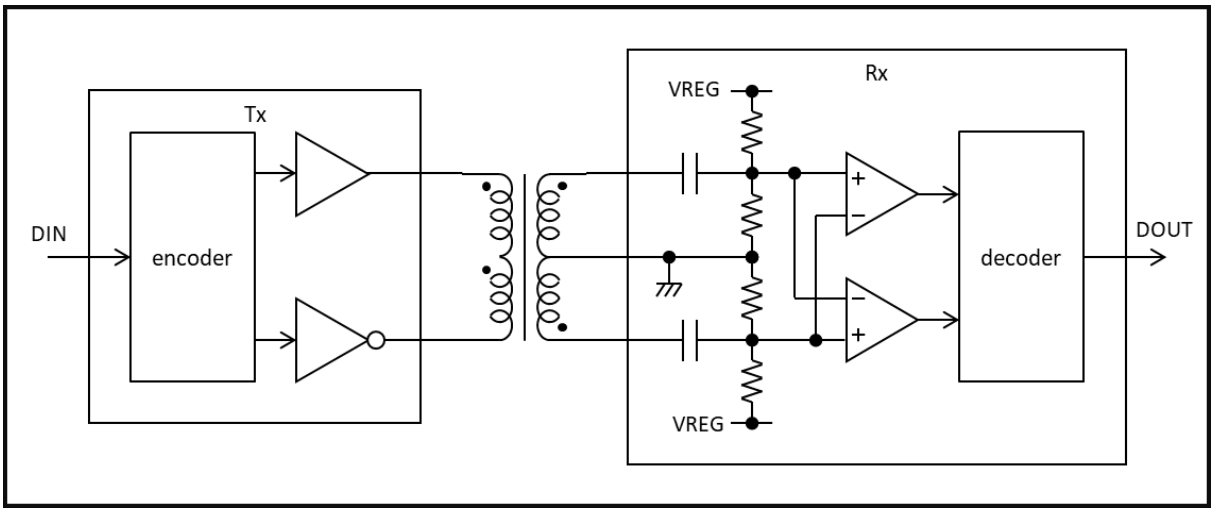


Figure 44. Block Diagram of Isolation

4.6 Thermal Shut Down (TSD)

4.6.1 Features

TSD turns off the IGBT to prevent the damage on the IGBT due to malfunctioning of the IC when an extraordinary overheat (175 °C typ.) is detected in the IC. The RSTB can resume switching operation when the IC's junction temperature is below the TSD recover temperature (typical hysteresis is 25 °C).

Temperature sense diode is placed near the OUTH pin that tends to be heated in the IC. The IGBT is soft turned off if the temperature of the driver transistor in the IC exceeds a threshold value due to the overload or the increased ambient temperature. At this time, the low level is output to the FOB pin of the primary circuit.

4.6.2 Block Diagram

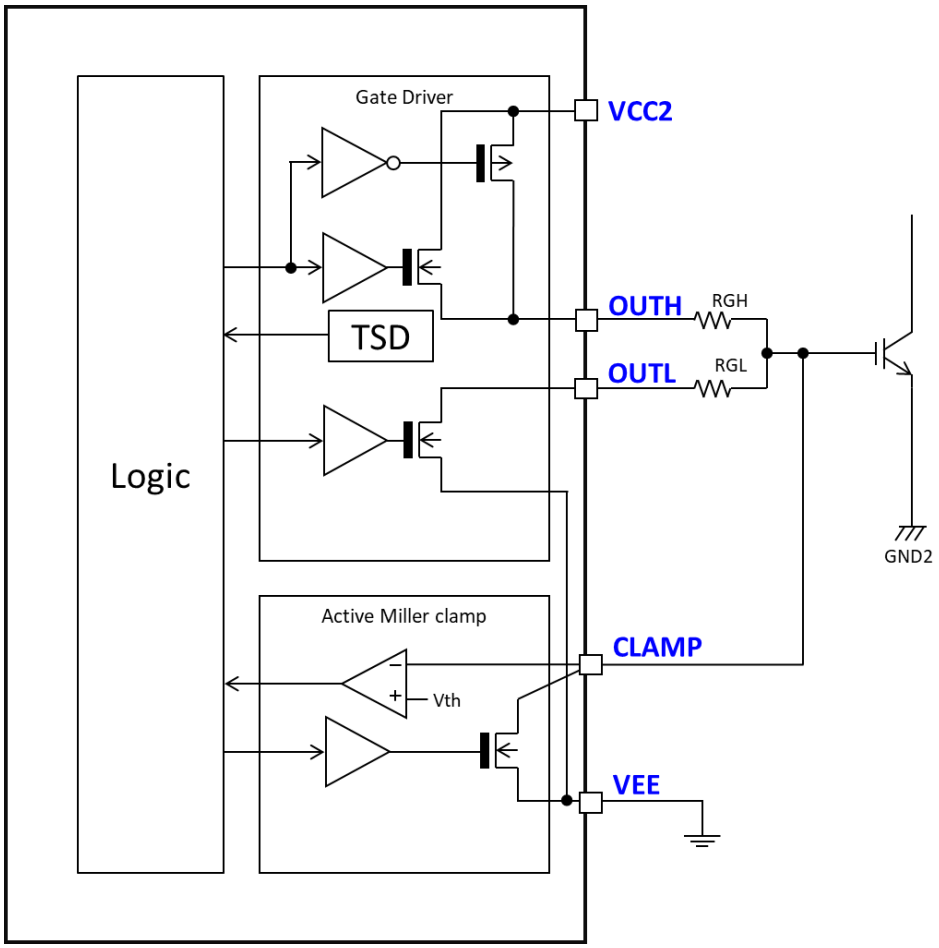


Figure 45. Block Diagram of Thermal Shut Down

4.7 Internal Regulator, Reference Voltage

4.7.1 Features

For primary chip, the supply voltage of internal circuit is supplied from an external pin. For secondary chip, the supply voltage of internal circuit is supplied from on-chip 5 V regulator.

4.7.2 Block Diagram

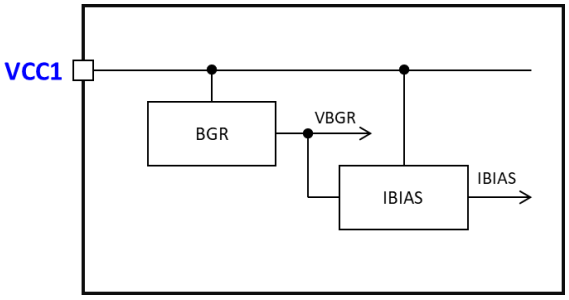


Figure 46. Block Diagram of Reference Voltage on Primary Chip

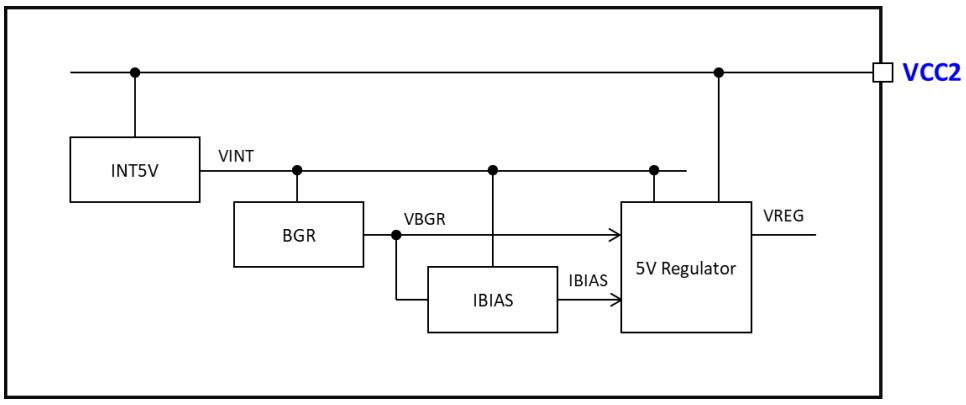


Figure 47. Block Diagram of Internal Regulator and Reference Voltage on Secondary Chip

5. Application Diagram Examples

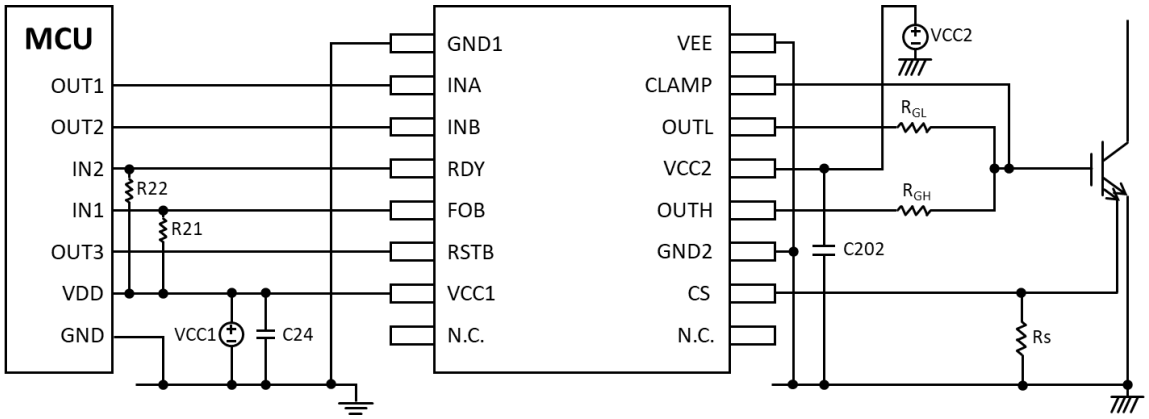


Figure 48. Simplified Application Diagram for IGBT

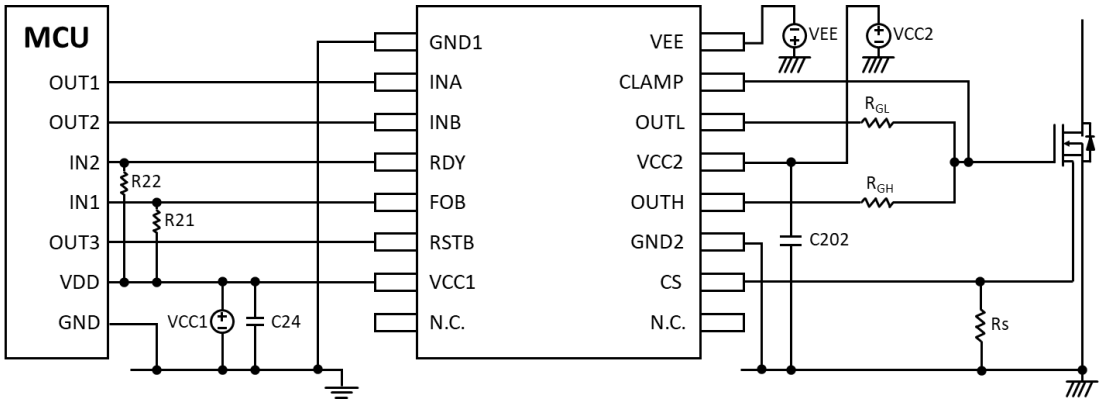


Figure 49. Simplified Application Diagram for SiC MOSFET

Table 14. Specifications of External Components

Component	Specification
R21	5 kΩ/5%
R22	5 kΩ/5%
C24	0.1 µF/10%
C202	1 µF/10%
RGL(1)	5.1 Ω/5%
RGH(1)	5.1 Ω/5%
RS	2.0 Ω/5%

The type and unit price of the component (resistor RG) may differ depending on the specifications of the IGBT (for example, gate charge, gate-emitter peak voltage). The rated power PG of the resistor RG connected to the IGBT can be calculated by equations 1 and 2.

$$P_G = I_G^2 R \quad \textbf{(1)}$$

$$I_G = f_C \times \left(\left|+Q_g\right| + \left|-Q_g\right|\right) \quad \textbf{(2)}$$

fc: Switching Frequency

$+Q_g$: Charge amount from 0 V to + V_{GE}

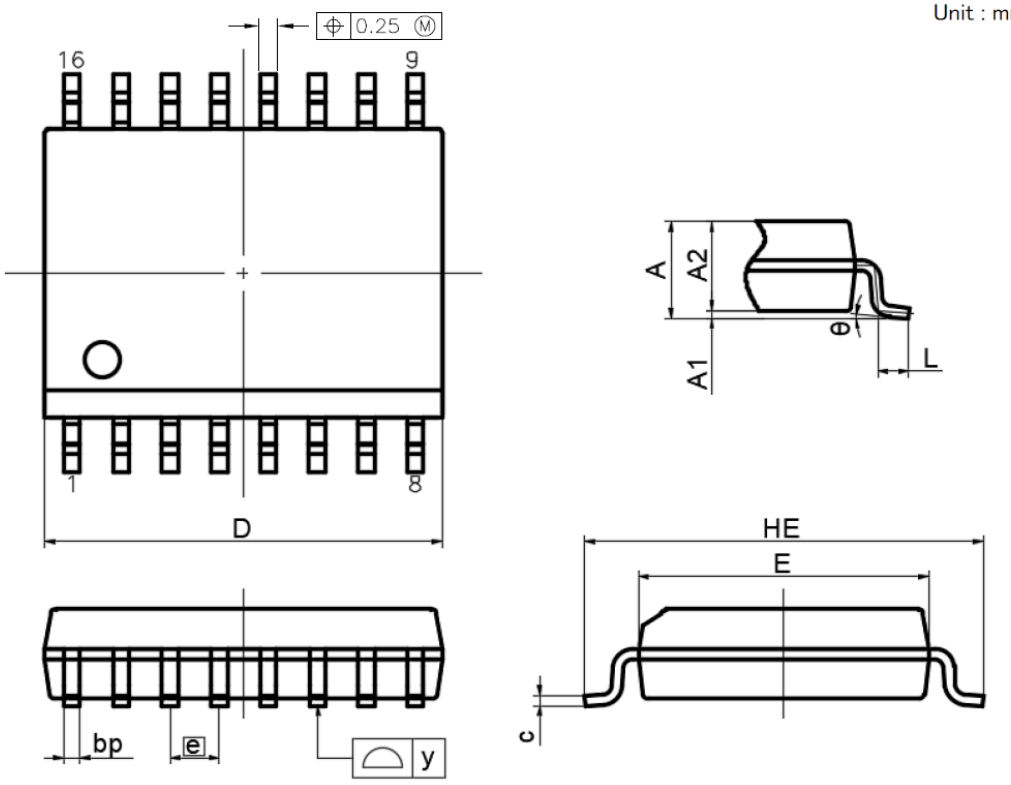
$-Q_g$: Charge amount from -V_{GE} to 0 V

6. Package Outline Drawings

Outline drawing SOP (PRSP0016DR-A)	RDK-G-001717-2
	Renesas Electronics Corporation

JEITA Package code	RENESAS code	MASS(TYP.) [g]
P-SOP16 7.5×10.3-1.27	PRSP0016DR-A	0.44[g]

Unit : mm



Reference Symbol	Dimension Millimeters		
	Min	Non	Max
D	10.15	—	10.41
E	7.44	—	7.59
A2	2.24	—	—
HE	10.01	—	10.63
A2	—	—	2.64
A1	0.10	—	0.29
bp	0.33	—	0.51
c	0.23	—	0.32
θ	0°	—	8°
e	—	1.27	—
y	—	—	0.10
L	0.51	—	1.02

7. Revision History

Revision	Date	Description
1.02	Oct 2, 2026	Removed preliminary status.
1.01	Jan 26.2026	Applied unified Renesas format.
1.00	Jun 8. 2024	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2026 Renesas Electronics Corporation. All rights reserved.