RAJ306102

General Purpose Motor Control IC

Rev.1.00
Oct 5, 2023

1 Description

The RAJ306102 is a general-purpose motor control IC for 3-phase brushless DC (BLDC) motor applications. RAJ306102 combines a smart gate driver and MCU (RL78/G1F) in a single package.

The smart gate driver includes three half-bridge gate drivers, a buck switching regulator and a charge pump for the gate drive voltage, two LDOs for the internal analog and logic circuitry and MCU, three accurate differential amplifiers, a BEMF sense amplifier, three general purpose comparators, and extensive protection functions.

The three half-bridge gate drivers are capable of driving up to three N-channel MOSFET bridges and support bridge voltages from 6V to 65V. Each gate driver supports up to 0.64A source and 1.28A sink peak drive current with adjustable drive strength control. Adaptive and adjustable dead-times are implemented to ensure robustness and flexibility. The active gate holding mechanism prevents miller effect induced cross-conduction and further enhances robustness.

Three accurate differential amplifiers with adjustable gain support ground-side shunt current sensing for each bridge. The device can also support both BLDC sensor/sensorless motor drive by the three general purpose comparators or a BEMF sense amplifier.

The protection functions include supply voltage OV/UV protection, buck regulator OV/UV/OC protection, charge pump UV protection, MOSFET V_{DS} OC protection, current sense OC protection, MOSFET V_{GS} fault, thermal warning, and thermal shutdown.

The smart gate driver can be configured to use SPI interface by the internal connection with MCU. All the parameters can be set through the SPI interface, and allows better monitoring. Fault conditions are reported on the nFAULT signal and each status bit in the Fault Status registers.

MCU supports H/W of the safe standard of IEC60730 and IEC61508. The development tools of the RL78 family are available.

2 Features

- Operating power supply voltage:
  - VBRIDGE: 6V to 65V (78V abs max)
  - VM: 6V to 60V (65V abs max)
- Operating ambient temperature: -40°C to 105°C
- Supply current:
  - MCU, VDD current:
    (HS mode, f_{IH}=32MHz: 5.2mA)
  - Smart gate driver, VM current:
    Operating Mode: 2mA, Sleep Mode: 28µA
- 8mm×8mm 64 Ld QFN package (0.4mm pitch)

Smart Gate Driver function

- 3-Phase drive for BLDC application
  - Peak 0.64A/1.28A source/sink current with 16 adjustable drive strength through SPI interface
  - Adaptive and adjustable dead time
  - 3-phase HI/LI mode and 3-phase PWM mode
  - Input control signal configuration
- Fully integrated power supply architecture
  - Two 5V LDOs allow for Sleep Mode low I_Q
  - 500mA buck switching regulator for the gate drive voltage (5V to 15V adjustable)
  - 100mA adjustable output LDO for MCU supplies
- Three differential amplifiers with configurable gain for current sensing (5, 10, 20, 40V/V)
- BEMF sense amplifier for sensorless motor drive
- Three comparators for hall sensor motor drive
- Extensive protection functions

MCU (RL78/G1F) function

- CPU: 16bit CISC CPU
- Code flash: 64KB, Data flash: 4KB, RAM: 5.5KB
- Serial array unit: 2 units
  (CSI:2ch, UART:1ch, I^2C:2ch)
- GPIO: 29 channels: I/O: 27ch, Input: 2ch
- Timer: Timer array unit: 1unit : 16bit, 4ch
  - Timer RJ/RG: 16bit, 1ch/1ch
  - Timer RD for motor control: 16bit, 2ch
  - Timer RX: 16bit, 1ch
- 10-bit resolution A/D converter input: 11ch
- External interrupt input: 10ch

3 Applications

- Power tools and Garden tools
- Vacuum cleaners, Fans, Pumps, and Robotics

1. Please refer to not only this datasheet but also *"RAJ306102 User's Manual: Hardware (R18UZ0082EJ)"* to understand this IC.
2. About detail specifications of RL78/G1F, please see *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.
3. This product has some restrictions on function.
   Please check them on *"CHAPTER2 MCU: RL78/G1F"* in *"RAJ306102 User's Manual: Hardware (R18UZ0082EJ)"*.
4. About the electrical characteristics of RL78/G1F, please substitute EVDD0/VDD condition to 3.135V<=EVDD0/VDD<=5.25V.

4 Overview

4.1 Typical Application Circuits

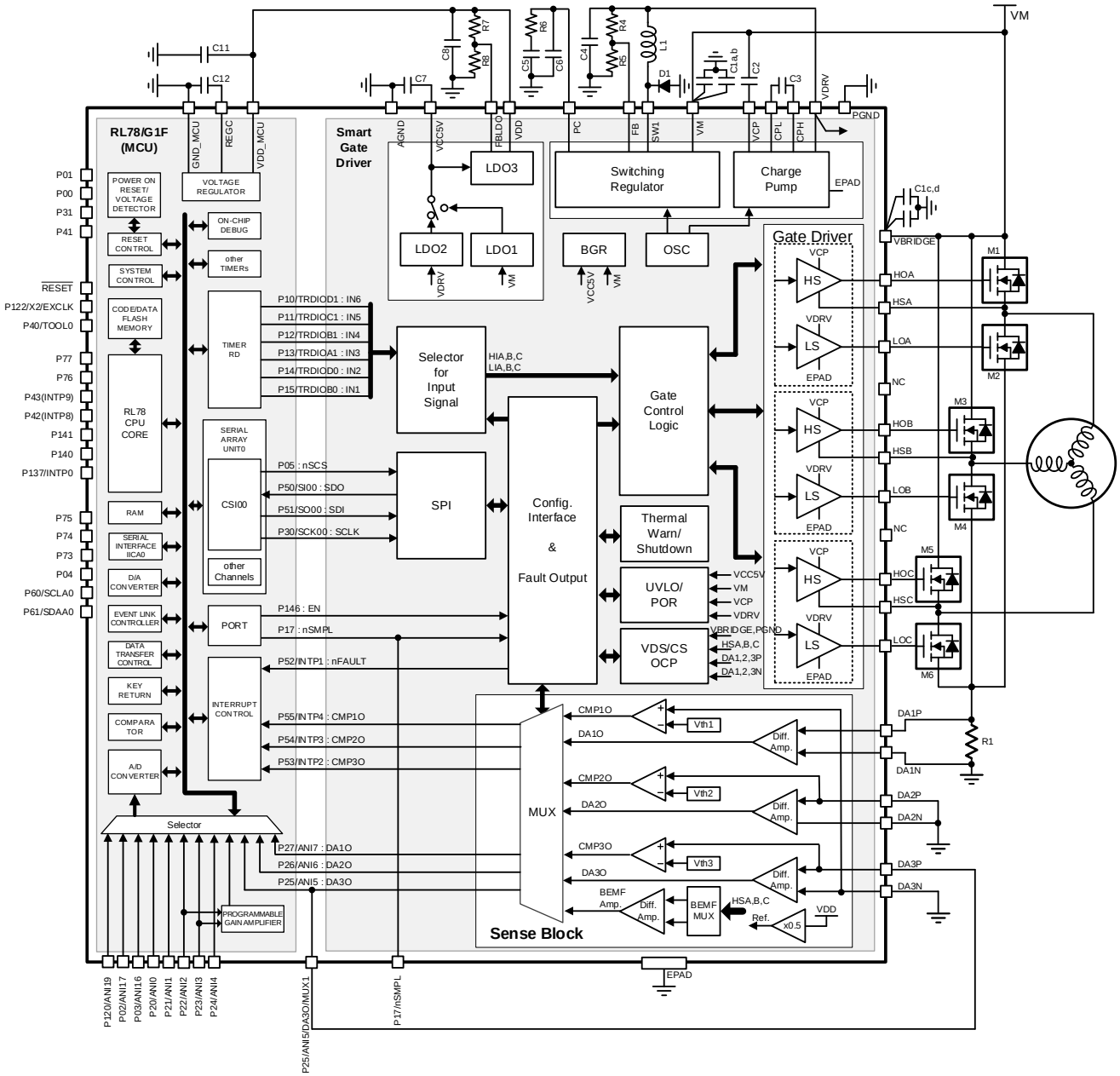


Figure 4.1-1 Simplified Block Diagram and Application – Sensorless Motor Drive by BEMF Sensing Comparator

4.1 Typical Application Circuits (continued)

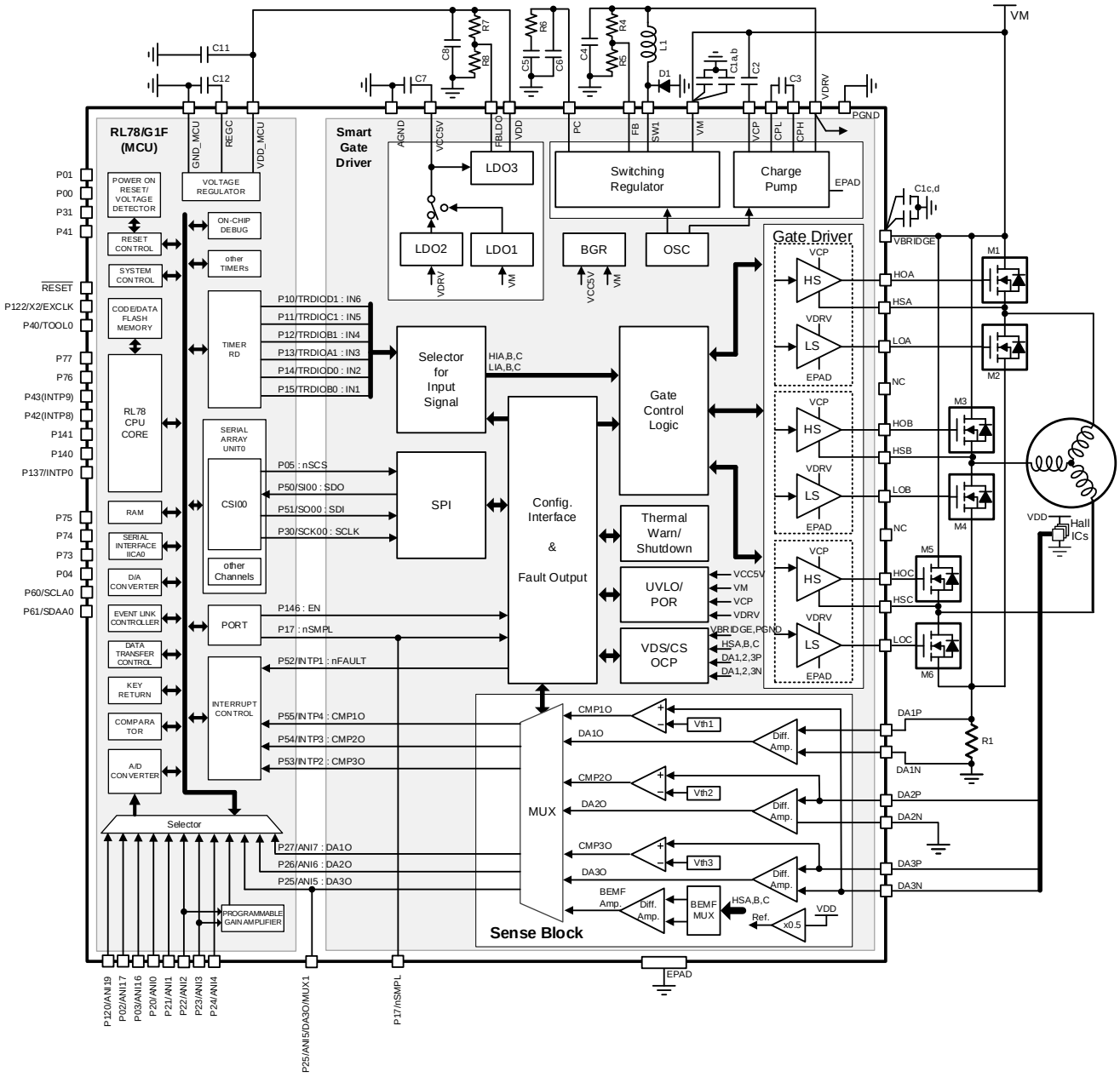


Figure 4.1-2 Simplified Block Diagram and Application – Hall Sensor Motor Drive by Using 3 Comparators

4.1 Typical Application Circuits (continued)

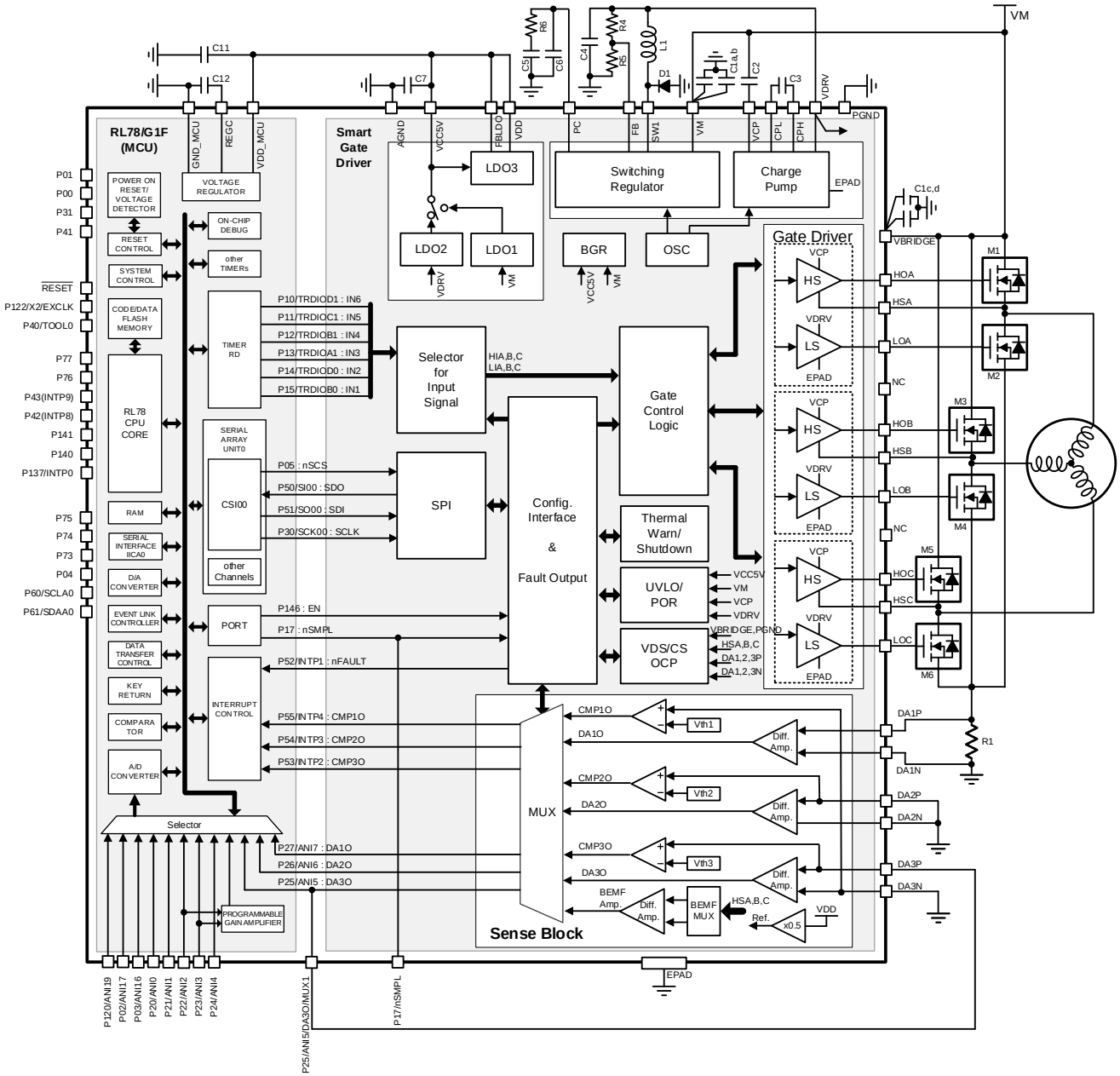


Figure 4.1-3 Simplified Block Diagram and Application – Sensorless Motor Drive by BEMF Sensing Comparator with 5V MCU Supply

4.2 Pin Configurations

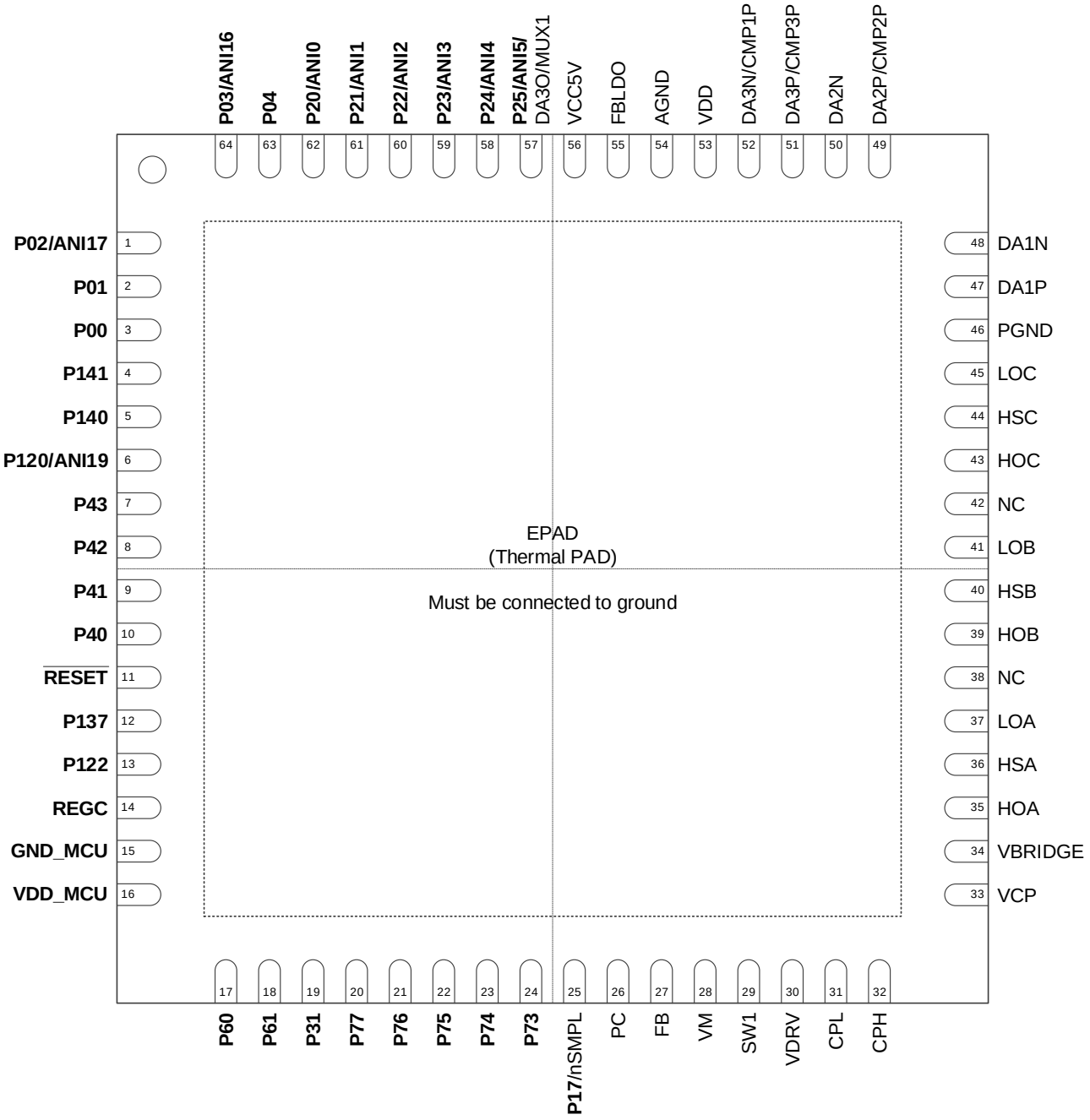


Figure 4.2-1 Pin Configuration Diagram Top View

4.3 Pin Descriptions

Table 4.3-1 Pin Descriptions

PIN		Alternate	I/O				
Number	Name	Function	level	type	Initial	Function	Note
1	**P02**	**ANI17/SO10/ TxD1/IVCMP10**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Serial data output of CSI10 / Serial data output of UART / Comparator 1 analog voltage input/reference voltage input	1
2	**P01**	**TO00/TRGCLKB/ TRJIO0/(INTP10)**	VDD	IN/OUT	IN	Digital input/output / Timer 00 output / Timer RG external clock input / Timer RJ input/output / (INTP10 interrupt request input)	1
3	**P00**	**TI00/TRGCLKA/ (TRJO0)/(INTP8)**	VDD	IN/OUT	IN	Digital input/output / Timer 00 input / Timer RG external clock input / (Timer RJ output) / (INTP8 interrupt request input)	1
4	**P141**	**PCLBUZ1/ INTP7**	VDD	IN/OUT	IN	Digital input/output / Programmable clock output/Buzzer output / INTP7 interrupt request input	1
5	**P140**	**PCLBUZ0/ INTP6**	VDD	IN/OUT	IN	Digital input/output / Programmable clock output/Buzzer output / INTP6 interrupt request input	1
6	**P120**	**ANI19/VCOUT0**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Comparator 0 output	1
7	**P43**	**INTP9**	VDD	IN/OUT	IN	Digital input/output / INTP9 interrupt request input	1
8	**P42**	**INTP8**	VDD	IN/OUT	IN	Digital input/output / INTP8 interrupt request input	1
9	**P41**	**(TRJIO0)**	VDD	IN/OUT	IN	Digital input/output / (Timer RJ input/output)	1
10	**P40**	**TOOL0**	VDD	IN/OUT	IN	Digital input/output / Data I/O for flash memory programmer/debugger	1
11	**/RESET**	**-**	VDD	IN	-	The active-low system reset input for RL78/G1F	1
12	**P137**	**INTP0**	VDD	IN	IN	Digital input / INTP0 interrupt request input	1
13	**P122**	**EXCLK**	VDD	IN	IN	Digital input / External clock input for main system clock	1
14	**REGC**	**-**	VDD	-	-	Connect regulator output stabilization capacitor between REGC and GND_MCU for internal operation of RL78/G1F.	1
15	**GND_MCU**	**-**	VDD	GND	-	Ground for RL78/G1F	1
16	**VDD_MCU**	**-**	VDD	POWER	-	Positive power supply input for RL78/G1F Connect to bypass capacitors between VDD_MCU and GND_MCU.	1
17	**P60**	**SCLA0**	VDD	IN/OUT	IN	Digital input/output / Serial clock I/O of serial interface IICA0	1
18	**P61**	**SDAA0**	VDD	IN/OUT	IN	Digital input/output / Serial data I/O of serial interface IICA0	1
19	**P31**	**TI03/TO03/ (PCLBUZ0)/ (TRJIO0)/VCOUT1**	VDD	IN/OUT	IN	Digital input/output / Timer 03 input / Timer 03 output / (Programmable clock output/Buzzer output) / (Timer RJ output) / Comparator 1 output	1
20	**P77**	**KR7/INTP11**	VDD	IN/OUT	IN	Digital input/output / KR7 key interrupt input / INTP11 interrupt request input	1
21	**P76**	**KR6/INTP10**	VDD	IN/OUT	IN	Digital input/output / KR6 key interrupt input / INTP10 interrupt request input	1
22	**P75**	**KR5/SCK01/ SCL01**	VDD	IN/OUT	IN	Digital input/output / KR5 key interrupt input / Serial clock I/O of CSI01 / Serial clock output of IIC01	1
23	**P74**	**KR4/SI01/ SDA01**	VDD	IN/OUT	IN	Digital input/output / KR4 key interrupt input / Serial data input of CSI01 / Serial data I/O of IIC01	1
24	**P73**	**KR3/SO01**	VDD	IN/OUT	IN	Digital input/output / KR3 key interrupt input / Serial data output of CSI01	1
25	**P17**	**TI02/TO02/** nSMPL	VDD	IN/OUT	IN	Digital input/output / Timer 02 input / Timer 02 output / Sample and Hold control input for smart gate driver	1,2
26	PC	-	VCC5V	OUT	OUT	gm amplifier output for phase compensation of buck switching regulator.	
27	FB	-	VCC5V	IN	IN	Voltage feedback input of buck switching regulator (Ref.=0.8V).	
28	VM	-	VM	POWER	-	Power supply input. Connect bypass capacitors between VM and analog ground.	
29	SW1	-	VM	OUT	OUT	Switch node of buck switching regulator.	
30	VDRV	-	VDRV	POWER	-	Output of buck switching regulator, Low-side gate driver supply. Connect to bypass capacitors between VDRV and analog ground.	
31	CPL	-	VDRV	OUT	OUT	Charge pump low-side switch node. Connect a flying capacitor between CPH and CPL pins.	
32	CPH	-	VCP	OUT	OUT	Charge pump high-side switch node. Connect a flying capacitor between CPH and CPL pins.	

Note1: RL78/G1F terminal. Please refer to *"RL78/G1F User's Manual: Hardware" (R01UH0516EJ)* about port functions of RL78/G1F.

Note2: When this pin is used as P17(Digital input/output), TI02, or TO02 function, the S/H function of the differential amplifier in the smart gate driver is not available.
Please set all of BEMF_SH, DA1_SH, DA2_SH, and DA3_SH bit in SNSCTL2 register of the smart gate driver to "0".
Please refer to the control register information on section 6.7.15, Sense Block Control 2 register.

4.3 Pin Descriptions (continued)

Table 4.3-2 Pin Descriptions (continued)

PIN		Alternate	I/O				
Number	Name	Function	level	type	Initial	Function	Note
33	VCP	-	VCP	POWER	-	Charge pump output. Connect a bypass capacitor between VCP and VBRIDGE pins.	
34	VBRIDGE	-	VBRIDGE	IN	IN	Charge pump output reference and high-side MOSFET drain sense Input. Connect a bypass capacitor between VBRIDGE pin and power ground.	
35	HOA	-	VCP	OUT	OUT	Phase A high-side gate driver output. Connect to the high-side MOSFET gate.	
36	HSA	-	VBRIDGE	IN	IN	Phase A high-side source sense input. Connect to the high-side MOSFET source.	
37	LOA	-	VDRV	OUT	OUT	Phase A low-side gate driver output. Connect to the low-side MOSFET gate.	
38	NC	-	-	-	-	No connection (Keep open state)	
39	HOB	-	VCP	OUT	OUT	Phase B high-side gate driver output. Connect to the high-side MOSFET gate.	
40	HSB	-	VBRIDGE	IN	IN	Phase B high-side source sense input. Connect to the high-side MOSFET source.	
41	LOB	-	VDRV	OUT	OUT	Phase B low-side gate driver output. Connect to the low-side MOSFET gate.	
42	NC	-	-	-	-	No connection (Keep open state)	
43	HOC	-	VCP	OUT	OUT	Phase C high-side gate driver output. Connect to the high-side MOSFET gate.	
44	HSC	-	VBRIDGE	IN	IN	Phase C high-side source sense input. Connect to the high-side MOSFET source.	
45	LOC	-	VDRV	OUT	OUT	Phase C low-side gate driver output. Connect to the low-side MOSFET gate.	
46	PGND	-	GND	GND	-	Ground sense input of external power stage.	
47	DA1P	-	VDD	IN	IN	Positive input of differential amplifier 1.	
48	DA1N	-	VDD	IN	IN	Negative input of differential amplifier 1.	
49	DA2P	CMP2P	VDD	IN	IN	Positive input of differential amplifier 2 and positive input of comparator 2.	
50	DA2N	-	VDD	IN	IN	Negative input of differential amplifier 2.	
51	DA3P	CMP3P	VDD	IN	IN	Positive input of differential amplifier 3 and positive input of comparator 3.	
52	DA3N	CMP1P	VDD	IN	IN	Negative input of differential amplifier 3 and positive input of comparator 1.	
53	VDD	-	VDD	POWER	-	Internal series regulator output and power supply of output buffers. Connect to a bypass capacitor between VDD and AGND.	
54	AGND	-	GND	GND	-	Device analog ground.	
55	FBLDO	-	VCC5V	IN	IN	Voltage feedback input of internal series regulator (Ref.=1.2V).	
56	VCC5V	-	VCC5V	POWER	-	Internal series regulator output(5V). Connect to a bypass capacitor between VCC5V and AGND.	
57	**P25**	**ANI5**/DA3O/MUX1	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Output of differential amplifier 3, BEMF sense amplifier, and multiplexer.	1,3
58	**P24**	**ANI4**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input	1
59	**P23**	**ANI3/ANO1/ PGAGND**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / DAC output / PGA reference voltage input	1
60	**P22**	**ANI2/ANO0/ PGAI/IVCMP0**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / DAC output / PGA voltage input / Comparator 0 analog voltage input	1
61	**P21**	**ANI1/AVREFM/ IVCMP13**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / ADC reference(- side) input	1
62	**P20**	**ANI0/AVREFP/ IVCMP12/(INTP11)**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / ADC reference (+ side) input / Comparator 1 analog voltage input/reference voltage input / (External interrupt request input)	1
63	**P04**	**SCK10/SCL10**	VDD	IN/OUT	ANALOG	Digital input/output / Serial clock I/O of CSI10 / Serial clock output of IIC10	1
64	**P03**	**ANI16/SI10/RxD1/ SDA10/IVCMP11**	VDD	IN/OUT	ANALOG	Digital input/output / ADC analog input / Serial data input of CSI10 / Serial data input of UART / Serial data I/O of IIC10 / Comparator 1 analog voltage input/reference voltage input	1
-	EPAD (Thermal PAD)	-	GND	GND	-	Power ground for gate driver and charge pump. Must be connected to power ground.	

Note1: RL78/G1F terminal. Please refer to *"RL78/G1F User's Manual: Hardware" (R01UH0516EJ)* about port functions of RL78/G1F.

Note3: When this pin is used as P25 or ANI5 pin, please set MUX bits in SNSCTL5 register of the smart gate driver to "000b".
This pin has 330kohm pulldown resistance. Please refer to the control register information on section 6.5.5, MUX1 Output Control, and section 6.7.18, Sense Block Control 5 register.

5 Specifications

5.1 Absolute Maximum Ratings

Table 5.1-1 Absolute Maximum Ratings Note1

Item		Symbol	Minimum	Maximum	unit
VBRIDGE to GND Note2		VBRIDGEabs	-0.3	78	V
VM to GND Note2		VMabs	-0.3	65	V
Voltage difference between ground pins (AGND, PGND, EPAD)		DGNDabs	-0.3	0.3	V
VCP to GND, CPH to GND, VCP to HSx, VCP to HOx (x=A,B,C)		VCPabs	-0.3	VBRIDGE + 15 Note3	V
CPL to GND		VCPLabs	-0.3	VDRV + 0.3	V
Continuous HOx (x=A,B,C) to GND		VHOxabs	-5	VCP + 0.5	V
Transient 200ns HOx (x=A,B,C) to GND		VHOxtran	-7	VCP + 0.5	V
HOx to HSx (x=A,B,C)		VGSHxabs	-0.3	15	V
Continuous HSx (x=A,B,C) to GND		VHSxabs	-5	VBRIDGE + 5 Note4	V
Transient 200ns HSx (x=A,B,C) to GND		VHSxtran	-7	VBRIDGE + 7 Note4	V
VDRV to AGND		VDRVabs	-0.3	17	V
Continuous LOx (x=A,B,C) to GND		VLOabs	-1	VDRV + 0.5	V
SW1 to GND		VSWabs	-1	VM + 0.5	V
VCC5V to GND		VCCabs	-0.3	5.5	V
FB, PC, FBLDO to GND		VFBabs	-0.3	VCC5V + 0.3	V
DAzP (z=1,2,3) to GND, DAzN (z=1,2,3) to GND		VDAINabs	-1	VDD + 0.6	V
VDD, VDD_MCU to GND		VDDabs	-0.3	5.5	V
REGC input voltage to GND		V_{IREGC}	-0.3	2.8 Note5	V
Digital input voltage	P00 to P04, P17, P20 to P25, P31, P40 to P43, P73 to P77, P120, P122, P137, P140, P141, /RESET, TEST	V_{DI1}	-0.3	VDD + 0.3	V
	P60, P61 (Nch open-drain)	V_{DI2}	-0.3	6.5	V
Output voltage	P00 to P04, P17, P20 to P25, P31, P40 to P43, P60, P61, P73 to P77, P120, P140, P141, DA3O	V_{OUT}	-0.3	VDD + 0.3	V
Analog input voltage	ANI0 to ANI5, ANI16, ANI17, ANI19	V_{AI1}	-0.3	VDD + 0.3 and AVREFP + 0.3 Note6	V

Note1: Not subject to production test, specified at Ta=25°C by design

Note2: Power supply can be applied to VBRIDGE and VM pin independently.

Note3: VCP pin voltage with respect to HOx and HSx pins should be limited to 86V maximum.
This will limit the maximum VCPabs, minimum VHOxabs, VHSxabs, and maximum VGSHxabs when VBRIDGE is greater than 66V.
For example, when VBRIDGE=78V, VCPabs=84V, and VHOxabs=VHSxabs=-2V, VGSHxabs should be limited to (84V - 78V) = 6V.
In this example, VDRV pin voltage will be also limited to about 7V in consideration of the step-up voltage of the charge pump.

Note4: In case of VDRV<=7V, the maximum VHSxabs is limited to VBRIDGE + (VDRV-2V).
The maximum VHSxtran is also limited to VBRIDGE + VDRV.

Note5: Connect the REGC pin to GND_MCU via a capacitor (0.47 to 1μF). This value regulates the absolute maximum rating of REGC pin.
Do not use this pin with voltage applied to it.

Note6: Do not exceed AVREFP + 0.3V in case of A/D conversion target pin.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter
That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage,
and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark1: Unless specified otherwise, the characteristics of alternate-function pins are same as those of the port pins.

Remark2: AVREFP: positive side reference voltage of the A/D converter.

Remark3: The GND pin of each block is the followings.
Gate driver block: EPAD, Charge pump: EPAD, Analog blocks: AGND, MCU: GND_MCU

5.1 Absolute Maximum Ratings (continued)

Table 5.1-2 Absolute Maximum Ratings (continued) Note1

Item		Symbol	Minimum	Maximum	unit
Output current, high	P00 to P04, P40 to P43, P120, P140, P141	I_{DOH1}	-40	-	mA/pin
		I_{DOH1A}	-70	-	mA total
	P17, P31, P73 to P77	I_{DOH2}	-40	-	mA/pin
		I_{DOH2A}	-100	-	mA total
	P20 to P25	I_{DOH3}	-0.5	-	mA/pin
		I_{DOH3A}	-2	-	mA total
Output current, low	P00 to P04, P40 to P43, P120, P140, P141	I_{DOL1}	-	40	mA/pin
		I_{DOL1A}	-	70	mA total
	P17, P31, P73 to P77	I_{DOL2}	-	40	mA/pin
		I_{DOL2A}	-	100	mA total
	P20 to P25	I_{DOL3}	-	1	mA/pin
		I_{DOL3A}	-	5	mA total
Ambient temperature		TA	-40	105	°C
Junction temperature for smart gate driver (RAA306012)		TJ	-40	150	°C
Storage temperature		Tstg	-65	150	°C

Note1: Not subject to production test, specified at Ta=25°C by design

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter
That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark1: Unless specified otherwise, the characteristics of alternate-function pins are same as those of the port pins.

Remark2: AVREFP: positive side reference voltage of the A/D converter.

Remark3: The GND pin of each block is the followings.
Gate driver block: EPAD, Charge pump: EPAD, Analog blocks: AGND, MCU: GND_MCU

5.2 Thermal Information

Table 5.2-1 Thermal Information

Thermal resistance (Typical)	θ_{JA}[°C/W]	Ψ_{JT}[°C/W]
8mm x 8mm 64Ld QFN Package Note1,2	21.4	1.69

Note1: θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.

Note2: For Ψ_{JT}, the "case temp" location is the center of the exposed metal pad on the package underside.

5.3 Recommended Operating Conditions

Table 5.3-1 Recommended Operating Conditions

Item		Symbol	Minimum	Maximum	unit
VBRIDGE to GND		VBRIDGEope	6	65	V
VM to GND		VMope	6	60	V
VCC5V to GND		VCCope	4.75	5.25	V
VDRV to GND		VDRVope Note4	5	16	V
VDD to GND		VDDope	3.135	5.25	V
VDD_MCU to GND	supplied from VCC5V	VMCUope1	4.75	5.25	V
	supplied from VDD	VMCUope2	3.135	3.465	V
External load current (VDD & VCC5V), Sleep Mode		$I_{VDD}0$	0	50 Note3	mA
External load current (VDD & VCC5V), during start-up, LDO1=On		$I_{VDD}1_0$	0	70 Note3	mA
External load current (VDD & VCC5V), Operating Mode		$I_{VDD}1_1$	0	90 Note3	mA
Operating junction temperature		Tjope	-40	125	°C

Note3: Power dissipation and thermal limits must be observed.
External load current is defined as the total of VCC5V and VDD load current including MCU supply current.

Note4: VDRV voltage must be set so that VCC5V voltage doesn't deviate from the recommended operating condition.

5.4 Electrical Characteristics

Regarding the electrical characteristics of the function implemented in RL78/G1F, please refer to *"RL78/G1F User's Manual: Hardware" (R01UH0516EJ)*.

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Power supply (VM)						
VM Sleep Mode current	$I_{VM}0$	HOx/LOx=Low/Low, No load on VDD	-	28	44	µA
VM, VBRIDGE operating current (combined)	$I_{VM}1$	Operating Mode, HOx/LOx=Low/Low, excluding MCU supply current	-	2	-	mA
VDRV operating current	$I_{VDRV}1$	Operating Mode, HOx/LOx=Low/Low	-	3.8	-	mA
Sleep Mode entry time delay	tsleep	From internal EN trigger to Sleep Mode	-	0.55	0.85	ms
Wake-up time delay	twake	From internal EN trigger to All power rails ready, C2=2.2µF, C3=0.22µF	-	6.5	-	ms
Power supply (VCC5V)						
Output voltage	$V_{VCC}0_1$	VM=60V, Sleep Mode, load=0mA	-	5	-	V
	$V_{VCC}0_2$	VM=36V, Sleep Mode, load=10mA	-	5	-	V
	$V_{VCC}0_3$	VM=6V, Sleep Mode, load=50mA	4.75	5	-	V
	$V_{VCC}1_1$	VDRV=15V, Operating Mode, load=0.1mA	-	5	-	V
	$V_{VCC}1_2$	VDRV=12V, Operating Mode, load=40mA	4.85	5	5.15	V
	$V_{VCC}1_3$	VDRV=8V, Operating Mode, load=100mA	-	5	-	V
Current limit	$I_{LMTCC}0_0$	VM=6V, Sleep Mode	50	80	-	mA
	$I_{LMTCC}0_1$	VM=36V, during start up, LDO1=On	80	130	-	mA
	$I_{LMTCC}1$	VDRV=12V, Operating Mode	100	160	-	mA
Power supply (VDD)						
Output voltage [Note2]	$V_{VDD}0_1$	VM=60V, Sleep Mode, load=0mA	-	3.3	-	V
	$V_{VDD}0_2$	VM=36V, Sleep Mode, load=10mA	-	3.3	-	V
	$V_{VDD}0_3$	VM=6V, Sleep Mode, load=50mA	3.0	3.3	-	V
	$V_{VDD}1_1$	VDRV=15V, Operating Mode, load=0.1mA	-	3.3	-	V
	$V_{VDD}1_2$	VDRV=12V, Operating Mode, load=40mA	3.201	3.3	3.399	V
	$V_{VDD}1_3$	VDRV=8V, Operating Mode, load=100mA	-	3.3	-	V
Current limit [Note3]	$I_{LMTDD}0$	VM=6V, Sleep Mode	50	80	-	mA
	$I_{LMTDD}1_0$	VM=36V, during start-up, LDO1=On	80	130	-	mA
	$I_{LMTDD}1_1$	VDRV=12V, Operating Mode	100	160	-	mA

Note2: VDD specification does not apply when VDD LDO is not used by connecting FBLDO to VCC5V or VDD pin.

Note3: VDD current is limited by VCC5V current limit. These items are not tested.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Buck switching regulator (VDRV)						
Output voltage adjustment range Note1	V_{DRV}		5	-	15	V
Reference voltage	V_{REF_SR}		0.776	0.8	0.824	V
gm amplifier gain	$gm_{_SR}$		-	200	-	µA/V
gm amplifier output capability	I_{gmSRC_SR}		-	18	-	µA
	I_{gmSNK_SR}		-	-18	-	µA
gm amplifier maximum output voltage	V_{gmH_SR}	FB=0V	-	3.95	-	V
gm amplifier minimum output voltage	V_{gmL_SR}	FB=1V	-	0.02	-	V
Ramp offset voltage	V_{ramp_SR}		-	870	-	mV
Oscillator frequency	f_{SW_SR}		400	500	575	kHz
Soft-start time	t_{SS_SR}	Time to FB=0.8V	-	2.2	-	ms
Cycle-by-cycle current limit Note1	I_{OC1_SR}		-	1.2	-	A
Hiccup current limit threshold Note1	I_{OC2_SR}		-	1.4	-	A
Charge pump (VCP)						
Output voltage with respect to VBRIDGE	V_{VCP}_1	VM=60V, VDRV=12V, load=15mA	-	11	-	V
	V_{VCP}_2	VM=36V, VDRV=12V, load=15mA	-	11	-	V
	V_{VCP}_3	VM=6V, VDRV=6V, load=15mA	5.0	5.3	-	V
Oscillator frequency	f_{SW_CP}		-	250	-	kHz
Maximum load current Note1	I_{load_CP}		28	-	-	mA
Gate driver block (HOx, LOx (x=A,B,C))						
High-side gate driver Output high voltage	V_{GSHH}	Io=1mA, VDRV=12V, VM=HSx=24V, with respect to HSx	-	11.45	-	V
High-side gate driver Output low voltage	V_{GSHL}	Io=-1mA, VDRV=12V, VM=HSx=24V, with respect to HSx	-	0.05	-	V
Low-side gate driver Output high voltage	V_{GSLH}	Io=1mA, VDRV=12V, VM=HSx=24V, with respect to GND	-	11.95	-	V
Low-side gate driver Output low voltage	V_{GSLL}	Io=-1mA, VDRV=12V, VM=HSx=24V, with respect to GND	-	0.05	-	V
High-side gate clamp voltage Note1	V_{CLMP}	Io=-1mA, with respect to HSx	16.0	17.2	18.4	V
Gate pulldown resistance	R_{PD}		-	200	-	kΩ
Strong sink current Note1	I_{SNK_STG}		-	1280	-	mA
Pullup source current	I_{SRC_PU}		-	50	-	mA
Pulldown sink current	I_{SNK_PD}		-	100	-	mA

Note1: This specification is not tested in production. Only functional test.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Gate driver block (HOx (x=A,B,C))						
High-side peak source current [Note1]	I_{SRCH0}	ISRC_HS[3:0]=0h	-	50	-	mA
	I_{SRCH1}	ISRC_HS[3:0]=1h	-	60	-	mA
	I_{SRCH2}	ISRC_HS[3:0]=2h	-	70	-	mA
	I_{SRCH3}	ISRC_HS[3:0]=3h	-	80	-	mA
	I_{SRCH4}	ISRC_HS[3:0]=4h	-	100	-	mA
	I_{SRCH5}	ISRC_HS[3:0]=5h	-	120	-	mA
	I_{SRCH6}	ISRC_HS[3:0]=6h	-	140	-	mA
	I_{SRCH7}	ISRC_HS[3:0]=7h	-	160	-	mA
	I_{SRCH8}	ISRC_HS[3:0]=8h	-	200	-	mA
	I_{SRCH9}	ISRC_HS[3:0]=9h	-	240	-	mA
	I_{SRCH10}	ISRC_HS[3:0]=Ah	-	280	-	mA
	I_{SRCH11}	ISRC_HS[3:0]=Bh	-	320	-	mA
	I_{SRCH12}	ISRC_HS[3:0]=Ch	-	400	-	mA
	I_{SRCH13}	ISRC_HS[3:0]=Dh	-	480	-	mA
	I_{SRCH14}	ISRC_HS[3:0]=Eh	-	560	-	mA
	I_{SRCH15}	ISRC_HS[3:0]=Fh	-	640	-	mA
High-side peak sink current [Note1]	I_{SNKH0}	ISRC_HS[3:0]=0h	-	100	-	mA
	I_{SNKH1}	ISRC_HS[3:0]=1h	-	120	-	mA
	I_{SNKH2}	ISRC_HS[3:0]=2h	-	140	-	mA
	I_{SNKH3}	ISRC_HS[3:0]=3h	-	160	-	mA
	I_{SNKH4}	ISRC_HS[3:0]=4h	-	200	-	mA
	I_{SNKH5}	ISRC_HS[3:0]=5h	-	240	-	mA
	I_{SNKH6}	ISRC_HS[3:0]=6h	-	280	-	mA
	I_{SNKH7}	ISRC_HS[3:0]=7h	-	320	-	mA
	I_{SNKH8}	ISRC_HS[3:0]=8h	-	400	-	mA
	I_{SNKH9}	ISRC_HS[3:0]=9h	-	480	-	mA
	I_{SNKH10}	ISRC_HS[3:0]=Ah	-	560	-	mA
	I_{SNKH11}	ISRC_HS[3:0]=Bh	-	640	-	mA
	I_{SNKH12}	ISRC_HS[3:0]=Ch	-	800	-	mA
	I_{SNKH13}	ISRC_HS[3:0]=Dh	-	960	-	mA
	I_{SNKH14}	ISRC_HS[3:0]=Eh	-	1120	-	mA
	I_{SNKH15}	ISRC_HS[3:0]=Fh	-	1280	-	mA

Note1: This specification is not tested in production. Only functional test.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Gate driver block (LOx (x=A,B,C))						
Low-side peak source current Note1	I_{SRCL0}	ISRC_LS[3:0]=0h	-	50	-	mA
	I_{SRCL1}	ISRC_LS[3:0]=1h	-	60	-	mA
	I_{SRCL2}	ISRC_LS[3:0]=2h	-	70	-	mA
	I_{SRCL3}	ISRC_LS[3:0]=3h	-	80	-	mA
	I_{SRCL4}	ISRC_LS[3:0]=4h	-	100	-	mA
	I_{SRCL5}	ISRC_LS[3:0]=5h	-	120	-	mA
	I_{SRCL6}	ISRC_LS[3:0]=6h	-	140	-	mA
	I_{SRCL7}	ISRC_LS[3:0]=7h	-	160	-	mA
	I_{SRCL8}	ISRC_LS[3:0]=8h	-	200	-	mA
	I_{SRCL9}	ISRC_LS[3:0]=9h	-	240	-	mA
	I_{SRCL10}	ISRC_LS[3:0]=Ah	-	280	-	mA
	I_{SRCL11}	ISRC_LS[3:0]=Bh	-	320	-	mA
	I_{SRCL12}	ISRC_LS[3:0]=Ch	-	400	-	mA
	I_{SRCL13}	ISRC_LS[3:0]=Dh	-	480	-	mA
	I_{SRCL14}	ISRC_LS[3:0]=Eh	-	560	-	mA
	I_{SRCL15}	ISRC_LS[3:0]=Fh	-	640	-	mA
Low-side peak sink current Note1	I_{SNKL0}	ISRC_LS[3:0]=0h	-	100	-	mA
	I_{SNKL1}	ISRC_LS[3:0]=1h	-	120	-	mA
	I_{SNKL2}	ISRC_LS[3:0]=2h	-	140	-	mA
	I_{SNKL3}	ISRC_LS[3:0]=3h	-	160	-	mA
	I_{SNKL4}	ISRC_LS[3:0]=4h	-	200	-	mA
	I_{SNKL5}	ISRC_LS[3:0]=5h	-	240	-	mA
	I_{SNKL6}	ISRC_LS[3:0]=6h	-	280	-	mA
	I_{SNKL7}	ISRC_LS[3:0]=7h	-	320	-	mA
	I_{SNKL8}	ISRC_LS[3:0]=8h	-	400	-	mA
	I_{SNKL9}	ISRC_LS[3:0]=9h	-	480	-	mA
	I_{SNKL10}	ISRC_LS[3:0]=Ah	-	560	-	mA
	I_{SNKL11}	ISRC_LS[3:0]=Bh	-	640	-	mA
	I_{SNKL12}	ISRC_LS[3:0]=Ch	-	800	-	mA
	I_{SNKL13}	ISRC_LS[3:0]=Dh	-	960	-	mA
	I_{SNKL14}	ISRC_LS[3:0]=Eh	-	1120	-	mA
	I_{SNKL15}	ISRC_LS[3:0]=Fh	-	1280	-	mA

Note1: This specification is not tested in production. Only functional test.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Gate driver block (HOx, LOx (x=A,B,C))						
Adaptive dead time V_{GS} falling threshold Note1	V_{TH_VGS}		-	1	-	V
Adaptive dead time V_{GS} threshold hysteresis Note1	V_{HYS_VGS}		-	2	-	V
Gate drive dead time	t_{DT0}	DEAD_TIME[1:0]=0h from VTH_VGS to other-side ON	-	50	-	ns
	t_{DT1}	DEAD_TIME[1:0]=1h from VTH_VGS to other-side ON	-	100	-	ns
	t_{DT2}	DEAD_TIME[1:0]=2h from VTH_VGS to other-side ON	-	200	-	ns
	t_{DT3}	DEAD_TIME[1:0]=3h from VTH_VGS to other-side ON	-	400	-	ns
Maximum gate transition time	t_{GT0}	T_GT[1:0]=0h from Source/Sink start to Pullup/down start	-	500	-	ns
	t_{GT1}	T_GT[1:0]=1h from Source/Sink start to Pullup/down start	-	1000	-	ns
	t_{GT2}	T_GT[1:0]=2h from Source/Sink start to Pullup/down start	-	2000	-	ns
	t_{GT3}	T_GT[1:0]=3h from Source/Sink start to Pullup/down start	-	4000	-	ns
Propagation delay Note1	t_{PROP}	from PWM input trigger to HOx/LOx start	-	40	-	ns
Differential amplifier (DAzP, DAzN, DAzO (z=1,2,3))						
Common mode input voltage range	V_{IC_CSA}	DAzP, DAzN pin	-0.5	-	2.8	V
Differential mode input voltage range	V_{ID_CSA}	DAzP - DAzN	-0.5	-	0.5	V
Input offset voltage	V_{IO_CSA}	CAL_CONN=1	-5	-	5	mV
Output voltage linear range Note1	V_{O_CSA}		0.4	-	VDD-0.4	V
Amplifier gain	G_{CSA0}	DAz_GAIN[1:0]=0h	4.85	5	5.15	V/V
	G_{CSA1}	DAz_GAIN[1:0]=1h	9.7	10	10.3	V/V
	G_{CSA2}	DAz_GAIN[1:0]=2h	19.4	20	20.6	V/V
	G_{CSA3}	DAz_GAIN[1:0]=3h	38.8	40	41.2	V/V
Settling time to +/-1% Note1	t_{SET_CSA0}	DAz_GAIN[1:0]=0h	-	250	-	ns
	t_{SET_CSA1}	DAz_GAIN[1:0]=1h	-	300	-	ns
	t_{SET_CSA2}	DAz_GAIN[1:0]=2h	-	400	-	ns
	t_{SET_CSA3}	DAz_GAIN[1:0]=3h	-	500	-	ns

Note1: This specification is not tested in production. Only functional test.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
BEMF sense amplifier (HSA, HSB, HSC, DA3O)						
Common mode input voltage range	V_{IC_EMF}	HSA, HSB, HSC pin	-2.5	-	VM+2.5	V
Differential mode input voltage range0	V_{ID_EMF0}	HSA, HSB, HSC pin - VBRIDGE/2 BEMF_GAIN[1:0]=0h	-24	-	24	V
Differential mode input voltage range3	V_{ID_EMF3}	HSA, HSB, HSC pin - VBRIDGE/2 BEMF_GAIN[1:0]=3h	-1.2	-	1.2	V
Output offset voltage0	V_{IO_EMF0}	DA3O pin with respect to VDD/2 BEMF_GAIN[1:0]=0h	-0.2	-	0.2	V
Output offset voltage3	V_{IO_EMF3}	DA3O pin with respect to VDD/2 BEMF_GAIN[1:0]=3h	-0.3	-	0.3	V
Amplifier output voltage bias	V_{REF_EMF}		-	VDD/2	-	V
BEMF sense amplifier gain	G_{EMF0}	BEMF_GAIN[1:0]=0h	0.0475	0.05	0.0525	V/V
	G_{EMF1}	BEMF_GAIN[1:0]=1h	0.095	0.1	0.105	V/V
	G_{EMF2}	BEMF_GAIN[1:0]=2h	0.475	0.5	0.525	V/V
	G_{EMF3}	BEMF_GAIN[1:0]=3h	0.95	1	1.05	V/V
Settling time to +/-1% Note1	t_{SET_EMF0}	BEMF_GAIN[1:0]=0h	-	350	-	ns
	t_{SET_EMF1}	BEMF_GAIN[1:0]=1h	-	400	-	ns
	t_{SET_EMF2}	BEMF_GAIN[1:0]=2h	-	500	-	ns
	t_{SET_EMF3}	BEMF_GAIN[1:0]=3h	-	1000	-	ns
Comparator (CMPzO (z=1,2,3))						
Threshold voltage for VDD=3.3V setting	V_{TH_CMP1}	CMPz_VTH[3:0] =1h	0.173	0.206	0.221	V
	V_{TH_CMP2}	CMPz_VTH[3:0] =2h	0.380	0.413	0.433	V
	V_{TH_CMP3}	CMPz_VTH[3:0] =3h	0.589	0.619	0.650	V
	V_{TH_CMP4}	CMPz_VTH[3:0] =4h	0.784	0.825	0.866	V
	V_{TH_CMP5}	CMPz_VTH[3:0] =5h	0.980	1.031	1.083	V
	V_{TH_CMP6}	CMPz_VTH[3:0] =6h	1.176	1.238	1.299	V
	V_{TH_CMP7}	CMPz_VTH[3:0] =7h	1.372	1.444	1.516	V
	V_{TH_CMP8}	CMPz_VTH[3:0] =8h	1.568	1.650	1.733	V
	V_{TH_CMP9}	CMPz_VTH[3:0] =9h	1.763	1.856	1.949	V
	V_{TH_CMP10}	CMPz_VTH[3:0] =Ah	1.959	2.063	2.166	V
	V_{TH_CMP11}	CMPz_VTH[3:0] =Bh	2.155	2.269	2.382	V
	V_{TH_CMP12}	CMPz_VTH[3:0] =Ch	2.351	2.475	2.599	V
	V_{TH_CMP13}	CMPz_VTH[3:0] =Dh	2.547	2.681	2.815	V
	V_{TH_CMP14}	CMPz_VTH[3:0] =Eh	2.743	2.888	3.032	V
	V_{TH_CMP15}	CMPz_VTH[3:0] =Fh	2.939	3.094	3.248	V
Hysteresis	V_{HYS_CMP0}	CMPz_HYS=0	-	+/-44	-	mV
	V_{HYS_CMP1}	CMPz_HYS=1	-	0	-	mV
Comparator delay	t_{DLY_CMP}		-	-	1	µs

Note1: This specification is not tested in production. Only functional test.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Fault management						
VCC5V power-on-reset rising	V_{CCUVR}		-	4.00	-	V
VCC5V power-on-reset falling	V_{CCUV}		-	3.63	-	V
VM under voltage rising0	$V_{VMUVR}0$	VMUV_TH=0	5.2	5.5	5.8	V
VM under voltage falling0	$V_{VMUV}0$	VMUV_TH=0	5.0	5.3	5.6	V
VM under voltage rising1	$V_{VMUVR}1$	VMUV_TH=1	7.38	7.78	8.18	V
VM under voltage falling1	$V_{VMUV}1$	VMUV_TH=1	7.1	7.5	7.9	V
VM over voltage rising	V_{VMOV}		-	63	-	V
VM over voltage falling	V_{VMOVR}		-	60	-	V
VDRV under voltage fault rising	V_{DRVUVR}		4.2	4.4	4.6	V
VDRV under voltage fault falling	V_{DRVUV}		4.0	4.2	4.4	V
VDRV over voltage rising	V_{DRVOV}	FB pin voltage	0.92	0.95	0.98	V
VDRV over voltage falling	V_{DRVOVR}	FB pin voltage	0.80	0.825	0.85	V
VCP under voltage fault falling0	$V_{CPUV}0$	with respect to VBRIDGE, CPUV_TH=0	-	0.58*VDRV	-	V
VCP under voltage fault hysteresis0	$V_{CPUVHYS}0$	CPUV_TH=0	-	0.07*VDRV	-	V
VCP under voltage fault falling1	$V_{CPUV}1$	with respect to VBRIDGE, CPUV_TH=1	-	0.8*VDRV	-	V
VCP under voltage fault hysteresis1	$V_{CPUVHYS}1$	CPUV_TH=1	-	0.09*VDRV	-	V
Thermal warning threshold [Note1]	T_{WARN}		-	140	-	°C
Thermal shutdown threshold [Note1]	T_{SD}		-	160	-	°C
Thermal hysteresis [Note1]	T_{HYS}		-	15	-	°C

Note1: This specification is not tested in production. Only functional test.

5.4 Electrical Characteristics (continued)

Note: All specifications are for Ta=25°C, VM=48V unless otherwise noted.

Parameter	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Fault management						
MOSFET V_{DS} OCP threshold	V_{DSOCP}	VDS_TH[3:0]=0h	-	40	-	mV
		VDS_TH[3:0]=1h	-	60	-	mV
		VDS_TH[3:0]=2h	-	80	-	mV
		VDS_TH[3:0]=3h	-	120	-	mV
		VDS_TH[3:0]=4h	-	160	-	mV
		VDS_TH[3:0]=5h	-	200	-	mV
		VDS_TH[3:0]=6h	-	240	-	mV
		VDS_TH[3:0]=7h	-	320	-	mV
		VDS_TH[3:0]=8h	-	400	-	mV
		VDS_TH[3:0]=9h	-	480	-	mV
		VDS_TH[3:0]=Ah	-	600	-	mV
		VDS_TH[3:0]=Bh	-	720	-	mV
		VDS_TH[3:0]=Ch	-	960	-	mV
		VDS_TH[3:0]=Dh	-	1200	-	mV
		VDS_TH[3:0]=Eh	-	1600	-	mV
		VDS_TH[3:0]=Fh	-	2000	-	mV
Shunt current sense OCP threshold	V_{CSOCP}	CSOCP_TH[2:0]=0h	37	51	65	mV
		CSOCP_TH[2:0]=1h	87	105	120	mV
		CSOCP_TH[2:0]=2h	131	157	175	mV
		CSOCP_TH[2:0]=3h	179	208	234	mV
		CSOCP_TH[2:0]=4h	224	260	290	mV
		CSOCP_TH[2:0]=5h	456	516	572	mV
		CSOCP_TH[2:0]=6h	686	773	857	mV
		CSOCP_TH[2:0]=7h	917	1029	1140	mV
OCP Deglitch time	t_{DEG_OCP}	DEG_TIME[1:0]=0h	1.10	1.57	2.04	µs
		DEG_TIME[1:0]=1h	1.67	2.38	3.09	µs
		DEG_TIME[1:0]=2h	2.44	3.49	4.54	µs
		DEG_TIME[1:0]=3h	4.01	5.73	7.45	µs
OCP Retry time	t_{RETRY_OCP}	TRETRY_CSOCP, VDSOCP=0	-	4000	-	µs
		TRETRY_CSOCP, VDSOCP=1	-	70	-	µs

5.5 SPI Timing Specification for Smart Gate Driver

The communication between MCU and smart gate driver is executed by 4-wire serial peripheral interface. These signals have to keep the following specifications. Please construct the suitable F/W to get the certain communication.

Table 5.5-1 SPI Timing Specification

Item	Symbol	Condition	Rated level			Unit
			MIN	TYP	MAX	
Sleep mode to SPI interface ready	t_{ready}	VCC5V > V_{CCUVR}, EN from low to high	-	2	-	ms
SCLK period	t_{CLK}		500	-	-	ns
SCLK high time	t_{CLKH}		200	-	-	ns
SCLK low time	t_{CLKL}		200	-	-	ns
SDI input data setup time	t_{SSDI}		40	-	-	ns
SDI input data hold time	t_{HSDI}		60	-	-	ns
SDO output data delay time	t_{dSDO}		-	-	120	ns
nSCS input setup time	t_{SnSCS}		200	-	-	ns
nSCS input hold time	t_{HnSCS}		200	-	-	ns
nSCS high time before pulling low	t_{nSCSH}		1000	-	-	ns
Chip de-select off time	$t_{OFFnSCS}$		-	20	-	ns

Note: These specifications are not tested in production. Only functional test.

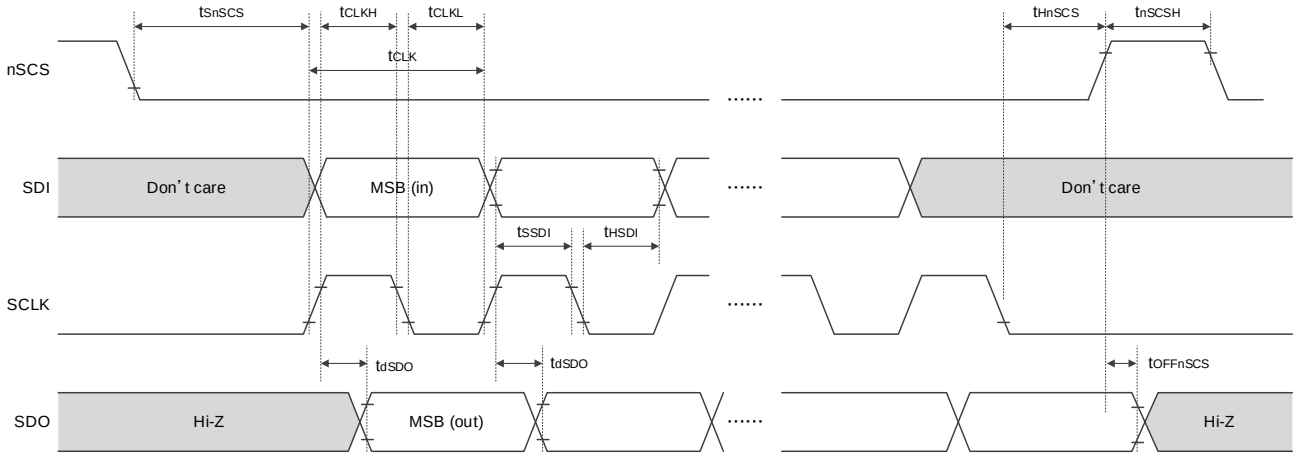


Figure 5.5-1 SPI Timing Diagram

6 Smart Gate Driver Description

6.1 Power-On Sequence and Functional Modes

6.1.1 Power-On Sequence

Figure 6.1-1 shows the example of Power-On sequence. The mode of operation and nFAULT signal in the smart gate driver chip work according to EN signal from MCU (RL78/G1F) and supply voltages including the output of the internal regulators. Refer to section 6.1.2, 6.1.3, and 6.2.

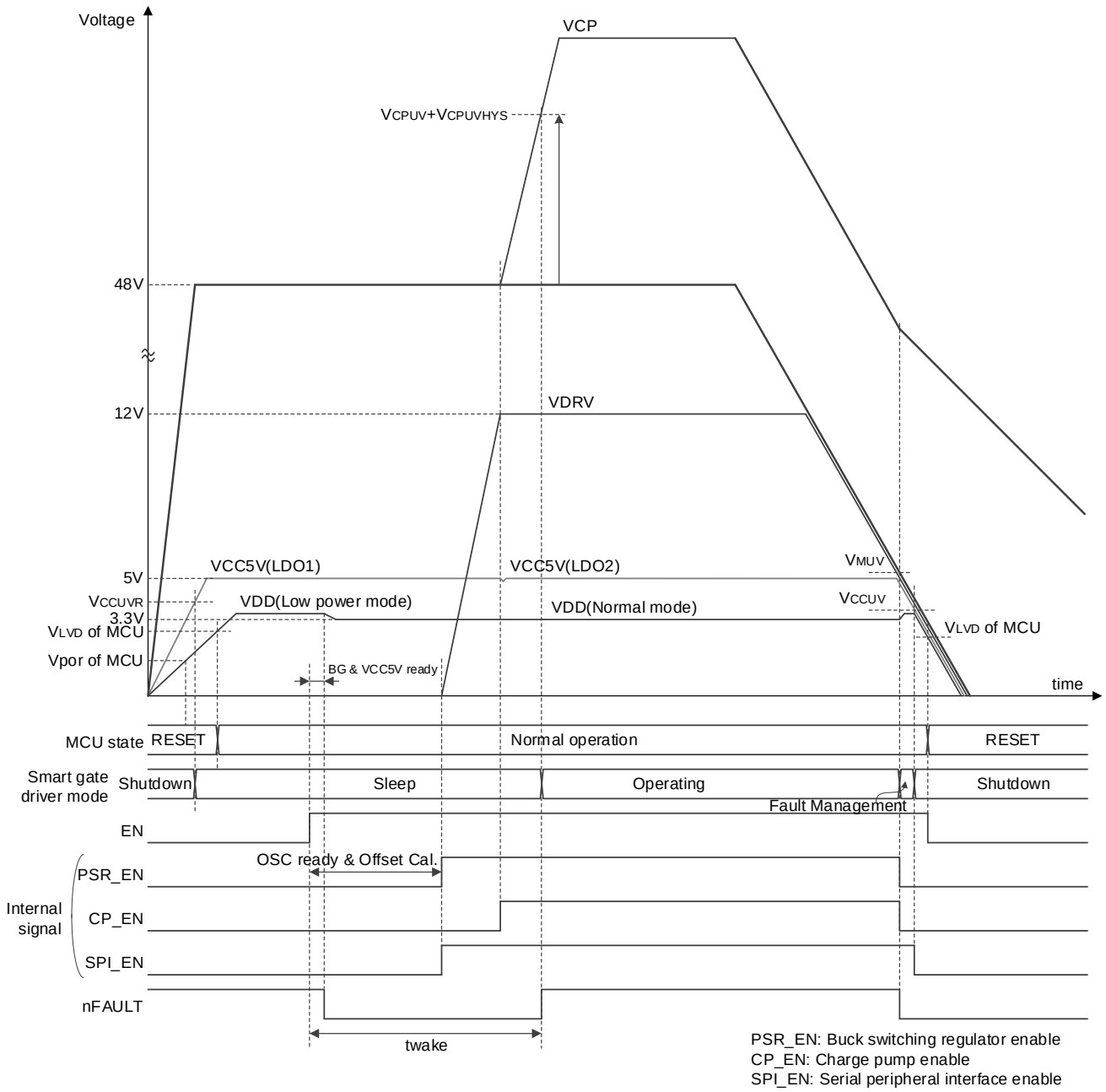


Figure 6.1-1 Power-On Sequence

6.1.2 Definitions of State of Different Modes

The smart gate driver contains four modes of operation:

Shutdown Mode:

This mode represents the state where VCC5V pin voltage is below the POR falling threshold (typical 3.63V). In this mode, most of internal functional blocks are disabled except for LDO1 and LDO3. LDO1 keeps powering the VCC5V rail until VM drops further below 1.2V. LDO3 is enabled in low power mode. Refer to section 6.3.3.

Sleep Mode:

The smart gate driver is in low-power Sleep Mode when VCC5V pin voltage is above the POR rising threshold (typical 4.0V) and EN is low. In this mode, the driver output is disabled and ignores any control input on HIx/LIx (x=A,B,C) selected from INz (z=1,2,3,4,5,6) signals. The power chain associated with the buck regulator (buck, charge pump, LDO2) is disabled. LDO1 and LDO3 are kept alive. LDO3 is enabled in low power mode. This minimizes the IC power consumption in Sleep Mode.

Operating Mode:

This mode represents the state when VCC5V pin voltage is above the POR rising threshold (typical 4.0V) and EN is pulled high. The smart gate driver is put into normal operation, high-efficiency buck regulator power chain (buck, charge pump, LDO2) and LDO3 are enabled in normal mode, and LDO1 is disabled. Driver output is enabled in response to control inputs on the HIx/LIx (x=A,B,C) selected from INz (z=1,2,3,4,5,6) signals. No occurrence of any fault is required in this mode.

Fault Management Mode:

This mode represents the state after any fault occurs. The smart gate driver reacts to fault conditions (see section 6.2 for detailed responses) and reports the fault status to the MCU using the nFAULT terminal and through the SPI interface. In this mode, the functioning of blocks depends on the fault source and control settings.

6.1.3 Mode Transition

The mode transition conditions (A to J) are summarized in Table 6.1-1.

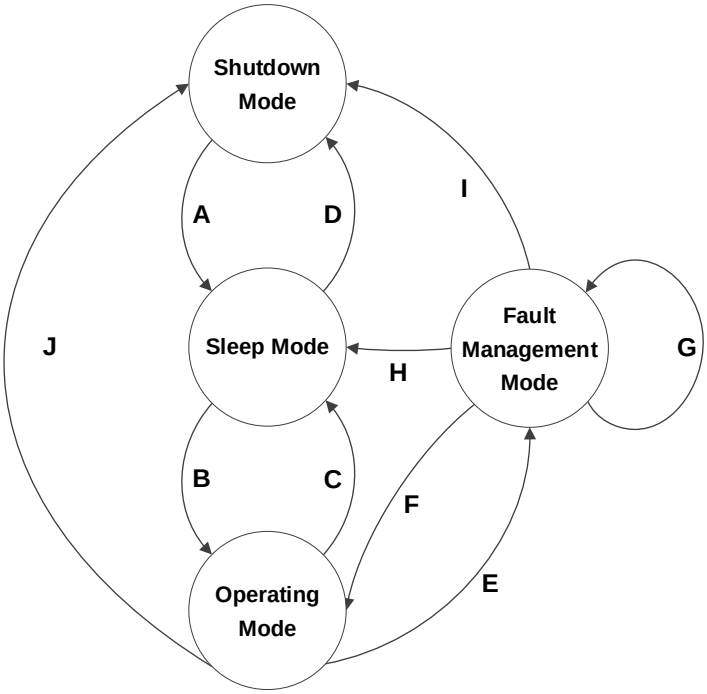


Figure 6.1-2 Mode Transition State Machine

6.1.3 Mode Transition (continued)

Table 6.1-1 Mode Transition Condition of State Machine

Transition	Exiting Mode	Entering Mode	Conditions	Actions
A	Shutdown	Sleep	VM rising, VCC5V > V_{CCUVR}	Disable most of the function blocks except for 5V LDO1 and VDD LDO3 [Note2]. Entering Sleep Mode after device start-up delay.
B	Sleep	Operating	EN goes high and stays.	Enable all function blocks except for 5V LDO1. Entering Operating Mode after Wake-up time delay "twake".
C	Operating	Sleep	EN goes low and stays. [Note1]	Disable most of the function blocks except for 5V LDO1 and VDD LDO3 [Note2]. The control registers are reset. Entering Sleep Mode after Entry time delay "tsleep".
D	Sleep	Shutdown	VM falling, and VCC5V < V_{CCUV}	Disable most of the function blocks except for 5V LDO1 and VDD LDO3 [Note2]. Entering Shutdown Mode after shutdown time delay.
E	Operating	Fault Management	Any fault condition occurs.	Respond based on fault management matrix.
F	Fault Management	Operating	Fault condition clears and operating recovers based on recovery action.	Enable all function blocks except for 5V LDO1. Entering Operating Mode after fault recovery delay.
G	Fault Management	Fault Management	Any other fault condition occurs.	Respond based on fault management matrix. Each function block disabling signal (active low) from multiple fault sources are ANDed together.
H	Fault Management	Sleep	EN goes low and stays. [Note1]	Disable most of the function blocks except for 5V LDO1 and VDD LDO3 [Note2]. The control registers are reset. Entering Sleep Mode after fault recovery delay.
I	Fault Management	Shutdown	VCC5V < V_{CCUV}	Disable most of the function blocks except for 5V LDO1 and VDD LDO3 [Note2]. The control registers are reset. Entering Shutdown Mode after shutdown time delay.
J	Operating	Shutdown	VCC5V < V_{CCUV}	Disable most of the function blocks except for 5V LDO1 and VDD LDO3 [Note2]. The control registers are reset. Entering Shutdown Mode after shutdown time delay.

Note1: EN low pulse shorter than "tsleep" maximum (0.85ms) must NOT be input to avoid the unexpected behavior.

Note2: LDO3 enters a low-power mode when the EN terminal is pulled low.

6.2 Fault Management

The smart gate driver has the protect function against VM undervoltage, VM overvoltage, Charge pump undervoltage, MOSFET V_{DS} overcurrent, Current sense overcurrent, MOSFET V_{GS} fault, Thermal warning, Thermal shutdown, Buck regulator overcurrent, Buck regulator undervoltage, and Buck regulator overvoltage events. When a fault occurs, the individual fault bit is set high along with the global FAULT bit in FAULT status register. The FAULT bit is OR'ed with all the other individual status bits. The fault and recovery action of each function is shown in Table 6.2-1 and Table 6.2-2.

6.2 Fault Management (continued)

Table 6.2-1 Fault Management Matrix

Fault type	Condition	Configuration	Reports	Gate driver Input / Output	Regulator in Fault Management Mode	Recovery condition	Recovery action
VCC5V undervoltage (VCC_UV)	VCC5V < V_{CCUV} (3.63V)	-	None	Blocked / Hi-Z pulldown	LDO1, LDO3 enable, others disable	VCC5V > V_{CCUVR} (4.0V)	Enter Sleep Mode
VM undervoltage (VM_UV)	VM < V_{VMUV} (5.3V or 7.5V)	DIS_VMUV=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-Z pulldown	LDO1, LDO3 enable, others disable	VM > V_{VMUVR} (5.5V or 7.78V)	RA1
		DIS_VMUV=1b		Active	Keep state in original mode		RA0
VM overvoltage (VM_OV)	VM > V_{VMOV} (63V)	DIS_VMOV=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-Z pulldown	LDO1, LDO3 enable, others disable	VM < V_{VMOVR} (60V)	RA2
		DIS_VMOV=1b		Active	Keep state in original mode		RA0
VCP undervoltage (VCP_UV)	VCP < V_{CPUV} (0.58*VDRV)	DIS_VCPUV=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-Z pulldown	All reg. except LDO1 enable	VCP > V_{CPUV}+ $V_{CPUVHYS}$ (0.58*VDRV +0.07*VDRV)	RA3
		DIS_VCPUV=1b		Active	Keep state in original mode		RA0
V_{DS} overcurrent (VDS_OCP)	V_{DSX} > V_{DSOCP} (x=A,B,C)	VDSOCP_MODE=00b	nFAULT=Lo (Latched) Status bit=1b	Blocked / Depends on PDMODE	All reg. except LDO1 enable	V_{DSX} < V_{DSOCP} (x=A,B,C) & clear latch	RA4
		VDSOCP_MODE=01b				Retry after t_{RETRY_OCP}	RA5
		VDSOCP_MODE=10b		Active	Keep state in original mode	V_{DSX} < V_{DSOCP} (x=A,B,C) & clear latch	RA6
		VDSOCP_MODE=11b	None			None	No action is necessary.
Current sense overcurrent (CS_OCP)	DAzP > V_{CSOCP} (z=1,2,3)	CSOCP_MODE=00b	nFAULT=Lo (Latched) Status bit=1b	Blocked / Depends on PDMODE	All reg. except LDO1 enable	DAzP < V_{CSOCP} (z=1,2,3) & clear latch	RA4
		CSOCP_MODE=01b				Retry after t_{RETRY_OCP}	RA5
		CSOCP_MODE=10b		Active	Keep state in original mode	DAzP < V_{CSOCP} (z=1,2,3) & clear latch	RA6
		CSOCP_MODE=11b	None			None	No action is necessary.
MOSFET V_{GS} fault (VGS_FAULT)	V_{GS} stuck > t_{GT}	DIS_VGSFLT=0b	nFAULT=Lo (Latched) Status bit=1b	Blocked / Hi-Z pulldown	All reg. except LDO1 enable	V_{GS} stuck < t_{GT} & clear latch	RA4
		DIS_VGSFLT=1b	None	Active	Keep state in original mode	None	No action is necessary.
Thermal warning (TWARN)	Tj > T_{WARN} (140°C)	TWARN_REP=0b	only Status bit=1b	Active	Keep state in original mode	Tj < T_{WARN} - T_{HYS} (125°C)	Status bit is reset, nFAULT pin is released high automatically.
		TWARN_REP=1b	nFAULT=Lo Status bit=1b				
Thermal shutdown (OTSD)	Tj > T_{SD} (160°C)	DIS_OTSD=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-Z pulldown	LDO1, LDO3 enable, others disable	Tj < T_{SD} - T_{HYS} (145°C)	RA2
		DIS_OTSD=1b		Active	Keep state in original mode		RA0
Buck reg. overcurrent limit (SR_OC1)	IL peak > I_{OC1_SR} (1.2A)	DIS_SROC=0b	None	Active	Keep state in original mode, buck reg. w/ SR_OC	None	No action is necessary.
		DIS_SROC=1b			Keep state in original mode, buck reg. w/o SR_OC		
Buck reg. overcurrent protection (SR_OCP)	IL peak > I_{OC2_SR} (1.4A)	DIS_SROC=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-Z pulldown	LDO1, LDO3 enable, buck reg. hiccup mode	Buck reg. soft-start done & IL peak < I_{OC2_SR}	RA2
		DIS_SROC=1b		Active	Keep state in original mode, buck reg. w/o SR_OC	IL peak < I_{OC2_SR}	RA0
VDRV undervoltage (VDRV_UV)	VDRV < V_{DRVUV} (4.2V)	DIS_VDRVUV=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-z pulldown	LDO1, LDO3 enable, buck reg. hiccup mode	Buck reg. soft-start done & VDRV > V_{DRVUVR} (4.4V)	RA2
		DIS_VDRVUV=1b		Active	Keep state in original mode	VDRV > V_{DRVUVR} (4.4V)	RA0
VDRV overvoltage (VDRV_OV)	FB > V_{DRVOV} (0.95V)	DIS_VDRVOV=0b	nFAULT=Lo Status bit=1b	Blocked / Hi-Z pulldown	LDO2, LDO3 enable, charge pump, buck reg. Hi-Z	FB < V_{DRVOVR} (0.825V)	RA3
		DIS_VDRVOV=1b		Active	Keep state in original mode		RA0

6.2 Fault Management (continued)

Table 6.2-2 Fault Recovery Actions

Recovery action	Case	Release/Reset timing				
		Status register reset	nFAULT release	Device mode moves to Operating Mode	Gate driver Input / Output	Regulators soft-start
RA0	Only report status	EN low pulse rising edge or CLR_FLT	Fault condition clears.	Keep state in original mode		
RA1	VM_UV	EN low pulse rising edge or CLR_FLT	Fault condition clears.			
RA2	VM_OV, OTSD, SR_OCP, VDRV_UV	EN low pulse rising edge or CLR_FLT	Fault condition clears.		EN low pulse rising edge or CLR_FLT	Fault condition clears.
RA3	VCP_UV, VDRV_OV	EN low pulse rising edge or CLR_FLT	Fault condition clears.		EN low pulse rising edge or CLR_FLT	Keep enable *Note1
RA4	VDS_OCP, CS_OCP with OCP_MODE= 00b, or VGS_FAULT	EN low pulse rising edge or CLR_FLT				Keep enable
RA5	VDS_OCP, CS_OCP with OCP_MODE= 01b	Expiration of Retry delay time				Keep enable
RA6	VDS_OCP, CS_OCP with OCP_MODE= 10b	EN low pulse rising edge or CLR_FLT		Keep state in original mode		

Note1: Charge pump and buck regulator release Hi-Z after the recovery from VDRV_OV.

6.2.1 Fault Indicator nFAULT

The nFAULT terminal (open-drain configuration) is the fault indicator. It is pulled low if any of the fault conditions occur. It is pulled high when all the fault conditions are removed and all chip power rail start-ups are done. The nFAULT is latched only for MOSFET V_{DS} overcurrent, Current sense overcurrent, and MOSFET V_{GS} fault. Toggling the EN signal or setting CLR_FLT=1b in IC Control 1 register pulls the nFAULT high (if the fault is removed).

This signal notifies the MCU after any fault occurs, so the MCU can stop normal operation and enter the fault handling routine. It also informs the MCU when all fault conditions are removed and all necessary power rails are properly up, so the MCU can re-enter the normal operating routine.

6.2.2 Fault Condition Types

6.2.2.1 VCC5V Undervoltage (VCC_UV)

If the VCC5V pin voltage falls lower than the V_{CCUV} threshold at any time, the smart gate driver enters Shutdown Mode, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), and most of internal function blocks are disabled except for LDO1 and LDO3. Normal operation starts again (the smart gate driver enters Sleep Mode) when the VCC5V undervoltage condition is removed (V_{CCUVR}).

6.2.2.2 VM Undervoltage (VM_UV)

If the input supply voltage on the VM pin falls lower than the V_{VMUV} threshold at any time with DIS_VMUV=0b, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), LDO1 and LDO3 are enabled, other regulators (buck, charge pump, LDO2) are disabled, and the nFAULT terminal is pulled low. The FAULT bit and VM_UV bit are also latched high in the Fault Status registers.

The nFAULT terminal is released automatically and normal operation starts again (gate driver, buck, charge pump, LDO2, and LDO3 operation) when the VM undervoltage condition is removed (V_{VMUVR}). The FAULT bit and VM_UV bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

This fault detection can be disabled by setting DIS_VMUV=1b in the Fault Control registers. If the VM undervoltage condition occurs with DIS_VMUV=1b, the device keeps state in original mode but the nFAULT terminal is pulled low until the VM undervoltage condition is removed (V_{VMUVR}). The FAULT bit and VM_UV bit are set high in the Fault Status registers until cleared by the CLR_FLT bit or an EN terminal low pulse.

6.2.2.3 VM Overvoltage (VM_OV)

If the input supply voltage on the VM pin rises higher than the V_{VMOV} threshold at any time with DIS_VMOV=0b, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), LDO1 and LDO3 are enabled, other regulators (buck, charge pump, LDO2) are disabled, and the nFAULT terminal is pulled low. The FAULT bit and VM_OV bit are also latched high in the Fault Status registers.

The nFAULT terminal is released automatically and normal operation starts again (buck, charge pump, LDO2, and LDO3 operation) when the VM overvoltage condition is removed (V_{VMOVR}). The gate drivers are enabled and the FAULT bit and VM_OV bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

This fault detection can be disabled by setting DIS_VMOV=1b in the Fault Control registers. If the VM overvoltage condition occurs with DIS_VMOV=1b, the device keeps state in original mode but the nFAULT terminal is pulled low until the VM overvoltage condition is removed (V_{VMOVR}). The FAULT bit and VM_OV bit are set high in the Fault Status registers until cleared by the CLR_FLT bit or an EN terminal low pulse.

6.2.2.4 VCP Undervoltage (VCP_UV)

If the charge pump voltage on the VCP pin falls lower than the V_{CPUV} threshold at any time with DIS_VCPUV=0b, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), the nFAULT terminal is pulled low, the buck regulator power chain (buck, charge pump, LDO2) and LDO3 keep enabled (LDO1 disabled). The FAULT bit and VCP_UV bit are also latched high in the Fault Status registers.
The nFAULT terminal is released automatically when the VCP undervoltage condition is removed (V_{CPUV} + $V_{CPUVHYS}$). The gate drivers are enabled and the FAULT bit and VCP_UV bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.
This fault detection can be disabled by setting DIS_VCPUV=1b in the Fault Control registers. If the VCP undervoltage condition occurs with DIS_VCPUV=1b, the device keeps state in original mode but the nFAULT terminal is pulled low until the VCP undervoltage condition is removed (V_{CPUV} + $V_{CPUVHYS}$). The FAULT bit and VCP_UV bit are set high in the Fault Status registers until cleared by the CLR_FLT bit or an EN terminal low pulse.

6.2.2.5 MOSFET V_{DS} Overcurrent (VDS_OCP)

A MOSFET V_{DS} overcurrent is detected by monitoring the V_{DS} voltage drop across the external MOSFET r_{DS}(on). If the V_{DS} voltage across an enabled MOSFET exceeds the V_{DSOCP} threshold selected by the VDS_TH bits for longer than the t_{DEG_OCP} deglitch time selected by the DEG_TIME bits, the smart gate driver judges VDS_OCP occurs and the fault actions are executed according to the VDSOCP_MODE bits in the Fault Control registers. The smart gate driver has following 4 different response modes for VDS_OCP fault action.
Note: For low-side V_{DS} overcurrent, the voltage between HSx (x=A,B,C) and PGND is monitored, respectively. Therefore, this voltage includes the differential voltage across the shunt resistor.

Latch mode (VDSOCP_MODE=00b):
After a VDS_OCP in this mode, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs) or the outputs are pulled low according to the PDMODE bit, and the nFAULT terminal is pulled low. The FAULT bit, VDS_OCP bit, and corresponding VDSyx_OCP (y=H,L, x=A,B,C) bit are latched high in the Fault Status registers.
The nFAULT terminal is released, normal operation starts again, and the FAULT bit, VDS_OCP bit, and corresponding VDSyx_OCP (y=H,L, x=A,B,C) bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

Automatic Retry mode (VDSOCP_MODE=01b):
After a VDS_OCP in this mode, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs) or pulled low according to the PDMODE bit and the nFAULT terminal is pulled low. The FAULT bit, VDS_OCP bit, and corresponding VDSyx_OCP (y=H,L, x=A,B,C) bit are latched high in the Fault Status registers.
The nFAULT terminal is released and normal operation starts again automatically after the t_{RETRY_OCP} time passes. The FAULT bit, VDS_OCP bit, and corresponding VDSyx_OCP (y=H,L, x=A,B,C) bit keep latched until the retry starts.

Report Only mode (VDSOCP_MODE=10b):
No action takes place (the gate drivers keep active) after a VDS_OCP in this mode. The nFAULT terminal is pulled low and the FAULT, VDS_OCP, and corresponding VDSyx_OCP (y=H,L, x=A,B,C) bit are latched high in the Fault Status registers.
The controller handles the VDS_OCP appropriately by controlling INz (z=1,2,3,4,5,6) signals or EN signal.
The nFAULT terminal is released and the FAULT bit, VDS_OCP bit, and corresponding VDSyx_OCP (y=H,L, x=A,B,C) bit are reset when the VDS_OCP condition is removed and the CLR_FLT bit or an EN terminal low pulse is set.

Disable mode (VDSOCP_MODE=11b):
No action and no report take place in this mode. The gate drivers keep active, the nFAULT terminal and the fault status bits keep state in original mode.

6.2.2.6 Current Sense Overcurrent (CS_OCP)

Current sense overcurrent is detected by monitoring the voltage drop across the external current sense resistor. If the differential voltage between DAzP and DAzN (z=1,2,3) exceeds the V_{CSOCP} threshold selected by the CSOCP_TH bits for longer than the t_{DEG_OCP} deglitch time selected by the DEG_TIME bits, the smart gate driver judges CS_OCP occurs and the fault actions are executed according to the CSOCP_MODE bits. The smart gate driver has following 4 different response modes for CS_OCP fault action. CSz_OCP (z=1,2,3) bits corresponding to each overcurrent can be disabled independently by setting DIS_CSzOCP (z=1,2,3) bits in the Fault Control registers to high. No action and no report take place in the case of DIS_CSzOCP (z=1,2,3)=1. If some differential amplifiers or DAzP, DAzN (z=1,2,3) pins are not used for shunt current sensing, corresponding DIS_CSzOCP (z=1,2,3) bits should be set to high.

Latch mode (CSOCP_MODE=00b):

After a CS_OCP in this mode, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs) or the outputs are pulled low according to the PDMODE bit and the nFAULT terminal is pulled low. The FAULT bit, CS_OCP bit, and corresponding CSz_OCP (z=1,2,3) bit are latched high in the Fault Status registers.
The nFAULT terminal is released, normal operation starts again, and the FAULT bit, CS_OCP bit, and corresponding CSz_OCP (z=1,2,3) bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

Automatic Retry mode (CSOCP_MODE=01b):

After a CS_OCP in this mode, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs) or the outputs are pulled low according to the PDMODE bit and the nFAULT terminal is pulled low. The FAULT bit, CS_OCP bit, and corresponding CSz_OCP (z=1,2,3) bit are latched high in the Fault Status registers.
The nFAULT terminal is released and normal operation starts again automatically after the t_{RETRY_OCP} time passes. The FAULT bit, CS_OCP bit, and corresponding CSz_OCP (z=1,2,3) bit keep latched until the retry starts.

Report Only mode (CSOCP_MODE=10b):

No action takes place (the gate drivers keep active) after a CS_OCP in this mode. The nFAULT terminal is pulled low and the FAULT bit, CS_OCP bit, and corresponding CSz_OCP (z=1,2,3) bit are latched high in the Fault Status registers.
The controller handles the CS_OCP appropriately by controlling INz (z=1,2,3,4,5,6) signals or EN signal.
The nFAULT terminal is released and the FAULT bit, CS_OCP bit, and corresponding CSz_OCP (z=1,2,3) bit are reset when the CS_OCP condition is removed and the CLR_FLT bit or an EN terminal low pulse is set.

Disable mode (CSOCP_MODE=11b):

No action and no report take place in this mode. The gate drivers keep active, the nFAULT terminal and the fault status bits keep state in original mode.

6.2.2.7 MOSFET V_{GS} Fault (VGS_FAULT)

MOSFET V_{GS} fault is detected by monitoring the gate-source voltage V_{GS} of the external MOSFET after the maximum gate transition time (t_{GT}). If the V_{GS} does not rise (over 3V typical) or drop (below 1V typical) by the abnormality of HOx, or LOx pins (shorted to other pins), or the inappropriate settings of ISRC_HS, ISRC_LS, and T_GT bits, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs) and the nFAULT terminal is pulled low. The FAULT bit, VGS_FAULT bit, and corresponding VGSyx_FAULT (y=H,L, x=A,B,C) bit are latched high in the Fault Status registers.
The nFAULT terminal is released, normal operation starts again, and the FAULT bit, VGS_FAULT bit, and VGSyx_FAULT (y=H,L, x=A,B,C) bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.
This fault detection can be disabled by setting DIS_VGSFLT=1b in the Fault Control registers. If the VGS_FAULT condition occurs with DIS_VGSFLT=1b, no action and no report take place. The gate drivers keep active, the nFAULT pin and the fault status bits keep state in original mode.

6.2.2.8 Thermal Warning (TWARN)

If the die temperature exceeds the trip point of the thermal warning temperature (T_{WARN}), TWARN bit is set high in the Fault Status register. The device keeps state in original mode. When the die temperature falls lower than the recovery point of the thermal warning (T_{WARN} – T_{HYS}), TWARN bit is cleared automatically. TWARN bit can be output to the nFAULT terminal by setting TWARN_REP=1b through the SPI interface.

6.2.2.9 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown temperature (T_{SD}) with DIS_OTSD=0b, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), LDO1 and LDO3 are enabled, other regulators (buck, charge pump, LDO2) are disabled, and the nFAULT terminal is pulled low. The FAULT bit and OTSD bit are also latched high in the Fault Status registers.

The nFAULT terminal is released automatically and normal operation starts again (buck, charge pump, LDO2, and LDO3 operation) when the die temperature falls lower than the recovery point of the thermal shutdown (T_{SD} – T_{HYS}). The gate drivers are enabled and the FAULT bit and OTSD bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

The thermal shutdown can be disabled by setting DIS_OTSD=1b in the Fault Control registers. If the OTSD condition occurs with DIS_OTSD=1b, the device keeps state in original mode but the nFAULT terminal is pulled low until the OTSD condition is removed (T_{SD} – T_{HYS}). The FAULT bit and OTSD bit are set high in the Fault Status registers until cleared by the CLR_FLT bit or an EN terminal low pulse. The controller handles the OTSD appropriately by controlling INz (z=1,2,3,4,5,6) signals or EN signal to avoid the high die temperature.

6.2.2.10 Buck Regulator Overcurrent Limiting (SR_OC1)

The overcurrent function of the buck regulator protects against any overload condition and output short at worst case by monitoring the current flowing through the high-side MOSFET. The device has two overcurrent function. The overcurrent function SR_OC1 limits the high-side MOSFET peak current cycle-by-cycle. No action and no report take place by SR_OC1 event except for the buck regulator. The gate drivers keep active, the nFAULT terminal and the fault status bits keep state in original mode.

6.2.2.11 Buck Regulator Overcurrent Protection (SR_OCP)

The second overcurrent function SR_OCP has the higher overcurrent threshold I_{OC2_SR} than I_{OC1_SR}. If the high-side MOSFET current reaches I_{OC2_SR}, the PWM shut off after two-cycle delay and the buck regulator enters Hiccup mode. In Hiccup mode, the PWM is disabled for a dummy cycle (63ms). After this dummy cycle, the true soft-start cycle is attempted again.

When SR_OCP occurs, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), LDO1 and LDO3 are enabled, charge pump and LDO2 are disabled, and the nFAULT terminal is pulled low. The FAULT bit, SR_FAULT bit and SR_OCP bit are also latched high in the Fault Status registers.

The nFAULT terminal is released automatically when the overcurrent condition is removed (I_{OC2_SR}) and soft-start of power rails is done. The gate drivers are enabled and the FAULT bit, SR_FAULT bit and SR_OCP bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

6.2.2.12 Buck Regulator VDRV Undervoltage (VDRV_UV)

If the VDRV pin voltage of the buck regulator output falls lower than the V_{DRVUV} threshold, the buck regulator enters Hiccup mode. The gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), LDO1 and LDO3 are enabled, charge pump and LDO2 are disabled, and the nFAULT terminal is pulled low. The FAULT bit, SR_FAULT bit, and VDRV_UV bit are also latched high in the Fault Status registers.
The nFAULT terminal is released automatically when the undervoltage condition is removed (V_{DRVUV}) and soft-start of power rails is done. The gate drivers are enabled and the FAULT bit, SR_FAULT bit and VDRV_UV bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

6.2.2.13 Buck Regulator VDRV Overvoltage (VDRV_OV)

If the VDRV pin voltage of the buck regulator output rises higher than the V_{DRVOV} threshold by FB pin voltage, the gate drivers are disabled (blocked inputs, Hi-Z pulldown outputs), LDO2 and LDO3 keep enable, charge pump and buck regulator stop switching until the fault condition is removed, and the nFAULT terminal is pulled low. The FAULT bit, SR_FAULT bit, and VDRV_OV bit are also latched high in the Fault Status registers.
The nFAULT terminal is released automatically and normal operation starts again (buck, charge pump) when the overvoltage condition is removed (V_{DRVOVR}). The gate drivers are enabled and the FAULT bit, SR_FAULT bit and VDRV_OV bit are reset after setting the CLR_FLT bit or an EN terminal low pulse.

6.3 Power Architecture

6.3.1 Block Diagram and On/Off Table of Power Supply Blocks

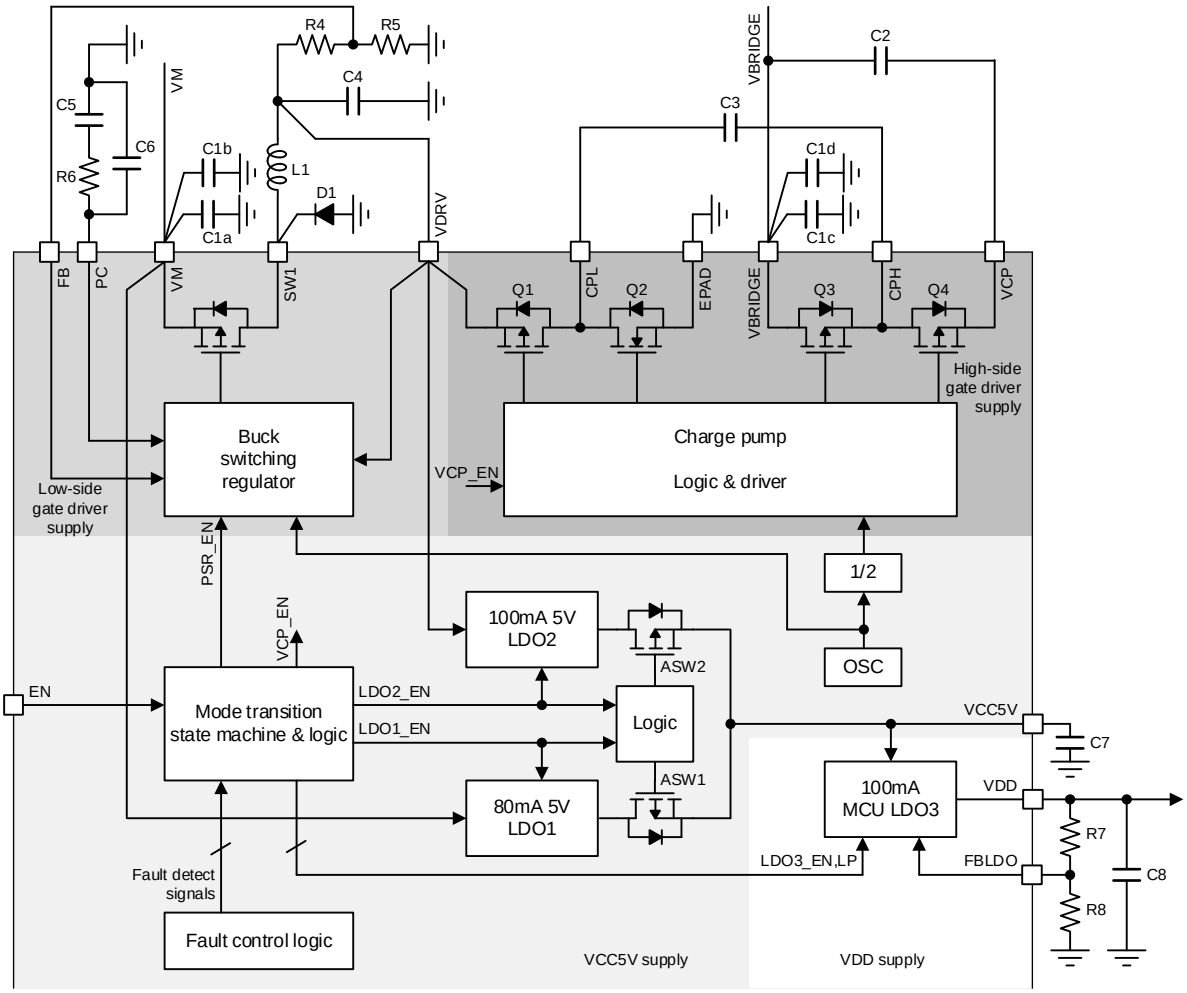


Figure 6.3-1 Block Diagram of Power Supply Blocks

Table 6.3-1 On/Off Table of Power Supply Blocks

Mode	80mA 5V LDO1	100mA MCU LDO3	100mA 5V LDO2	Buck switching regulator	Charge pump
Shutdown	On	On Note1	Off		
Sleep	On	On Note1	Off		
Operating	Off	On	On		
Fault Management	Reaction based on fault management matrix				

Note1: LDO3 enters a low-power mode when the EN terminal is pulled low.

6.3.2 VCC5V Supply

VCC5V supply consists of two LDOs and two analog switches for LDO output selection.

5V LDO1 for EN=Lo:

This LDO is a high voltage LDO fed from VM. It is enabled to generate VCC5V power upon device power-up (VCC5V reaches above rising POR) until the buck regulator soft-start is completed. Whenever LDO1 is enabled, ASW1 is also turned on.

Note: the bandgap reference used in LDO1 is untrimmed.

5V LDO2 for EN=Hi:

This LDO is a low voltage LDO fed from the buck regulator output. It supplies VCC5V in Operating Mode after the buck regulator soft-start is completed. ASW2 is on when LDO2 is used.

Note: the bandgap reference used in LDO2 is trimmed, to achieve better VCC5V accuracy in Operating Mode.

6.3.3 VDD Supply

VDD LDO is a low voltage LDO3 fed from VCC5V, designed to power the MCU and peripherals in applications as required. It has a dedicated feedback pin (FBLDO) that allows for fine adjustment of output voltage within the recommended operating condition. The internal reference is 1.2V. The output voltage is tightly regulated during normal Operating Mode. When the EN terminal is pulled low, LDO3 enters a low-power mode with not-so-tight regulation.

6.3.4 Low-side Gate Driver Supply (VDRV)

Low-side gate driver supply (VDRV) is generated by a 500mA buck switching regulator fed from VM. VDRV adjustable range is from 5V to 15V. The buck regulator integrates a 1.0Ω high voltage (65V) PMOS and the corresponding gate driver. It also integrates all the control circuitry and logic to achieve peak current mode control scheme. The freewheeling diode and inductor need to be placed externally. Regulator switching frequency is 500kHz, with two-level peak current limit at 1.2A (cycle-by-cycle current limit) and 1.4A (peak OCP threshold). Regulator output is monitored and protected from OV and UV conditions. Under medium or high load conditions, the regulator runs in continuous current mode (CCM). However, under light-load conditions, it can run in discontinuous current mode (DCM) due to the nature of asynchronous rectification. Moreover, in case of high VM low VDRV operation in light load, it can run in pulse skipping mode due to the minimum on-time limitation.

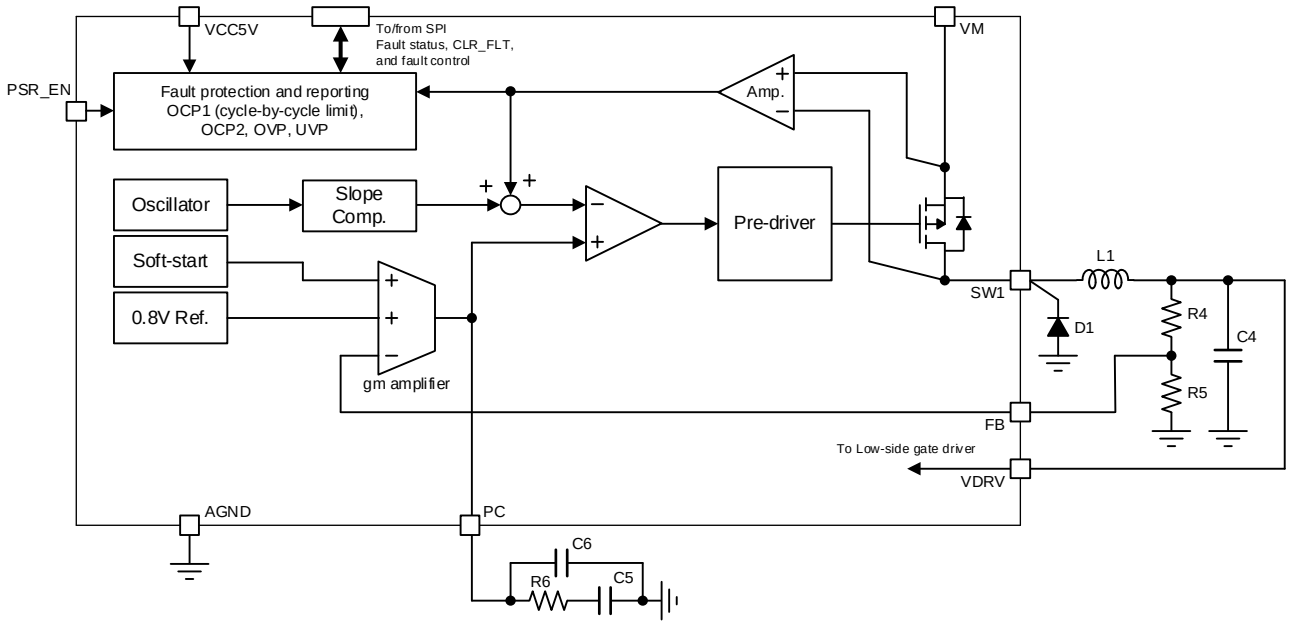


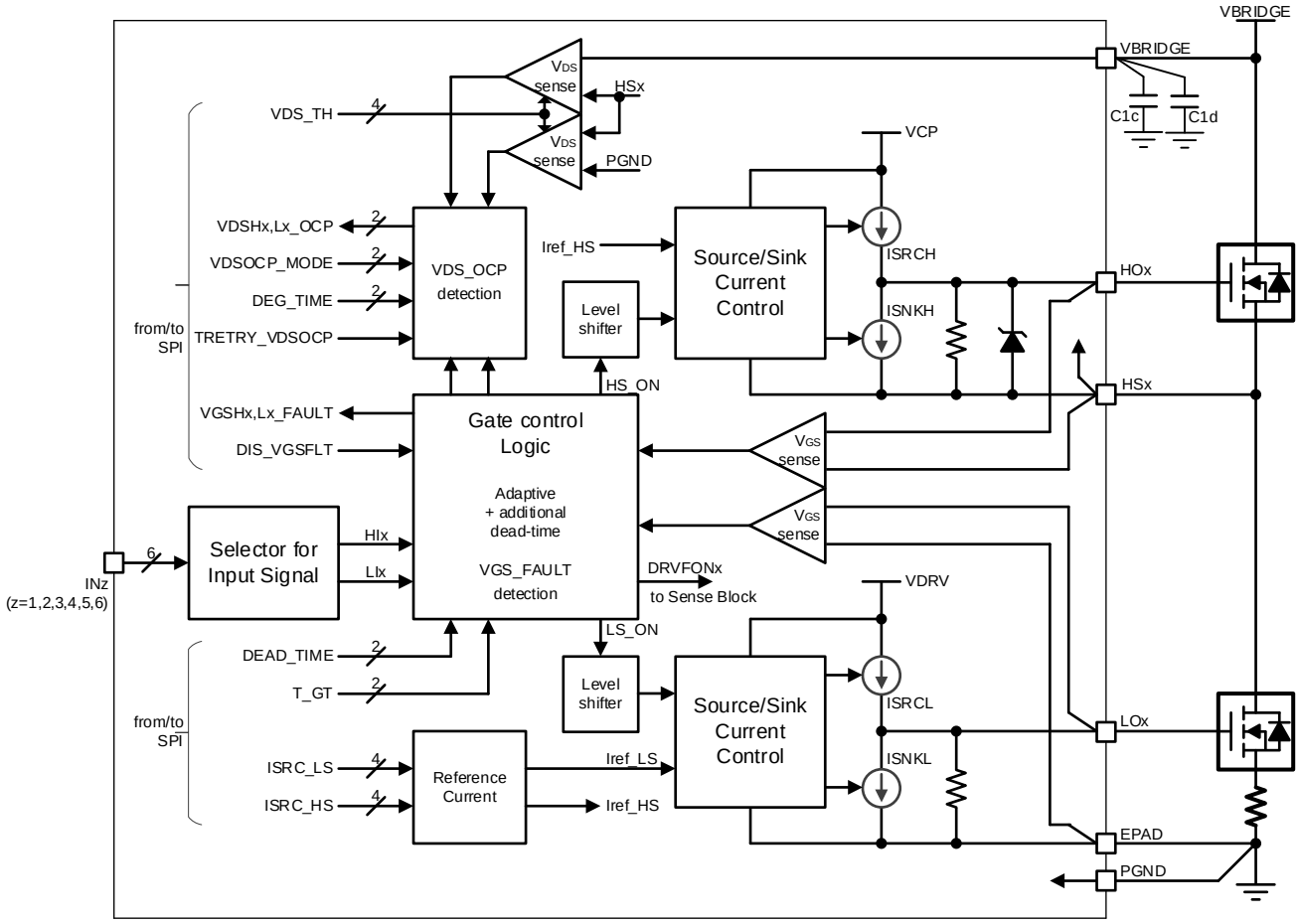
Figure 6.3-2 Buck regulator block diagram

6.3.5 High-side Gate Driver Supply (VCP)

This high voltage charge pump is to generate a steady high-side gate driver supply rail at the level VBRIDGE+VDRV. The CPL pin switches between VDRV and EPAD (Ground) by complementary switches Q1 and Q2. The CPH pin switches between VBRIDGE and VCP (VBRIDGE+VDRV) by complementary switches Q3 and Q4. Q1 and Q4 are turned on and off at the same time, while Q2 and Q3 are turned on and off at the same time. In this way, during on-time of Q2 and Q3 (off-time of Q1 and Q4), the flying capacitor C3 across CPH and CPL gets charged by VBRIDGE. During on-time of Q1 and Q4 (off-time of Q2 and Q3), C2 gets charged up towards VBRIDGE+VDRV by VDRV. From its operation it can be seen that this charge pump always runs in full mode with minimal power dissipation. The complementary switches operate at 250kHz, which is 1/2 the internal oscillator frequency used by the buck regulator, and the duty cycle is 50%. The maximum loading target is 28mA. The charge pump output is monitored and undervoltage protection is implemented.

6.4 Gate Driver

6.4.1 Block Diagram



Note1: "x" in this figure stands for A,B, and C.

Figure 6.4-1 Block Diagram of Gate Driver

6.4.2 Gate Driver Control Modes

When the device is put into Operating Mode, the gate driver sets its output state based on the control signal present on HIx and LIx (x=A,B,C) signals which is selected from INz (z=1,2,3,4,5,6) signals according to HOx_SEL and LOx_SEL (x=A,B,C) bits in the Gate Driver Input Selection registers. Two gate driver control modes are available:

- 3-Phase HI/LI Mode
- 3-Phase PWM Mode

Detailed descriptions and logic truth tables are listed in the following 3-Phase HI/LI Mode and 3-Phase PWM Mode sections.

6.4.2.1 3-Phase HI/LI Mode

This mode is enabled when PWMMODE=0b in the IC Control 1 register. In this mode, HIx and LIx (x=A,B,C) inputs serve as control inputs for each individual driver output, logic active high. For each phase, the HIx (x=A,B,C) input signal controls the high-side gate driver output HOx (x=A,B,C) directly, while the LIx (x=A,B,C) input signal controls the low-side gate driver output LOx (x=A,B,C) directly. See Table 6.4-1.

Table 6.4-1 3-Phase HI/LI Mode Truth Table (x=A,B,C)

LIx	HIx	LOx	HOx - HSx	HSx
0	0	Low	Low	Hi-Z
0	1	Low	High	High
1	0	High	Low	Low
1	1	Low	Low	Hi-Z

6.4.2.2 3-Phase PWM Mode

This mode is enabled when PWMMODE=1b in the IC Control 1 register. In this mode, LIx (x=A,B,C) serves as the enable (logic high)/disable (logic low) of the driver output of each bridge. HIx (x=A,B,C) serves as control input for each bridge. See Table 6.4-2.

Table 6.4-2 3-Phase PWM Mode Truth Table (x=A,B,C)

LIx	HIx	LOx	HOx - HSx	HSx
0	0	Low	Low	Hi-Z
0	1	Low	Low	Hi-Z
1	0	High	Low	Low
1	1	Low	High	High

6.4.3 Adjustable Slew-Rate

The gate driver architecture allows for the accurate setting of the gate drive source (I_{SRC}) and sink current (I_{SNK}). It is helpful to more accurately control and adjust the slew-rate of switch node voltage, which is beneficial for radiated emission optimization, controlling the reverse recovery of the body diode and avoiding CdV/dt induced cross-conduction. For all gate driver outputs, 16 levels of sourcing/sinking current can be supported by ISRC_HS or ISRC_LS bits through the SPI interface. The configurable range is from 50mA to 640mA for sourcing and 100mA to 1280mA for sinking.

Note: The driver sink current is automatically set to be double the source current.

The duration of driver peak source/sink current (maximum gate transition time (t_{GT})), can also be configured to ensure the MOSFET turns on fully. This maximum gate transition time (t_{GT}) can be configured to four levels of options (500ns, 1000ns, 2000ns, 4000ns) by T_GT bits through the SPI interface.

6.4.4 Gate Driver Robustness Enhancement

Strong sinking current to avoid CdV/dt induced cross-conduction

Additionally, within the same bridge phase, whenever one of the gate drivers is during gate transition of turning on or turning off the corresponding external MOSFET, the complementary gate driver performs a strong sinking current (I_{SNK_STG}) to avoid CdV/dt induced cross-conduction. The maximum duration of the strong sinking current is also equal to the maximum gate transition time (t_{GT}).

Active pullup/pulldown current to hold gate state

After the maximum gate transition time (t_{GT}), the driver actively imposes weaker current to hold the gate state. A pullup current (I_{SRC_PU}) is sourced out of the driver to maintain a high output voltage, whereas a pulldown sinking current (I_{SNK_PD}) is imposed to maintain nearly zero output voltage.

Adaptive dead time control plus configurable additional dead time

Adaptive dead time control is implemented by actively monitoring the gate of the MOSFET that is turning off first during the transition. The complementary MOSFET is allowed to start turning on only after it drops below the threshold (1V typical). In addition to adaptive dead time, you can add the extra dead time (t_{DT}) by setting DEAD_TIME bits through SPI interface.

Note: The t_{GT} value is defined as “maximum” gate transition time because in real applications, actual gate transition must be shorter than the t_{GT} setting in order to properly drive the MOSFETs. Therefore, the duration of driver peak source/sink current can get terminated before reaching the full t_{GT} duration. For example, during the turn off transition, after V_{GS} drops below the adaptive dead time threshold, peak sink current and the complementary MOSFET gate strong sinking current are terminated, which is earlier than the elapse of t_{GT}. For the turning-on transition, because there is no detection of V_{GS} reaching enough high level for the MOSFET, peak source current and complementary MOSFET gate strong sinking current sustain a full t_{GT} duration, assuming it is sufficiently long on time. Other instances involve the short on-time or off-time.

Adaptive dead time control disable function

Adaptive dead time control can be disabled by setting DIS_SADT=1b. In this case, the monitored result of the MOSFET gate voltage is ignored, and the complementary MOSFET is allowed to start turning on by the only the complementary HIx or LIx (x=A,B,C) input. After the complementary input changes to high, the extra dead time (t_{DT}) is started to avoid the shoot through current of the gate driver. After finishing the extra dead time (t_{DT}), the complementary MOSFET starts turning on. Refer to Figure 6.4-4.

Note: The inserted dead time should be shorter than the t_{GT} setting in order to properly drive the MOSFETs. The duration of driver peak source/sink current is terminated after reaching the full t_{GT} duration. Refer to Figure 6.4-5. And the inserted dead time must be longer than the MOSFET discharge time “tdchg” to avoid the shoot through current of the half-bridge MOSFET.

6.4.5 Gate Drive Timing Diagram in 3-Phase HI/LI Mode

Figure 6.4-2 shows the gate drive timing diagram if the HI/LI inserted dead time is relatively long (longer than maximum gate transition time (t_{GT}) plus extra dead time (t_{DT}) set). This case means:

- During high-side MOSFET turn-off/low-side MOSFET turn-on transition, if LIx (x=A,B,C) asserts high after the HOx-HSx (x=A,B,C) high-to-low transition time (t_{GT}) and extra dead time (t_{DT}) ends.
- During low-side MOSFET turn-off/high-side MOSFET turn-on transition, if HIx (x=A,B,C) asserts high after the LOx (x=A,B,C) high-to-low transition time (t_{GT}) and extra dead time (t_{DT}) ends.

Total effective dead time is adaptive dead time, plus extra dead time (t_{DT}) selected by DEAD_TIME bits, plus additional dead time introduced by the HIx/LIx (x=A,B,C) signals.

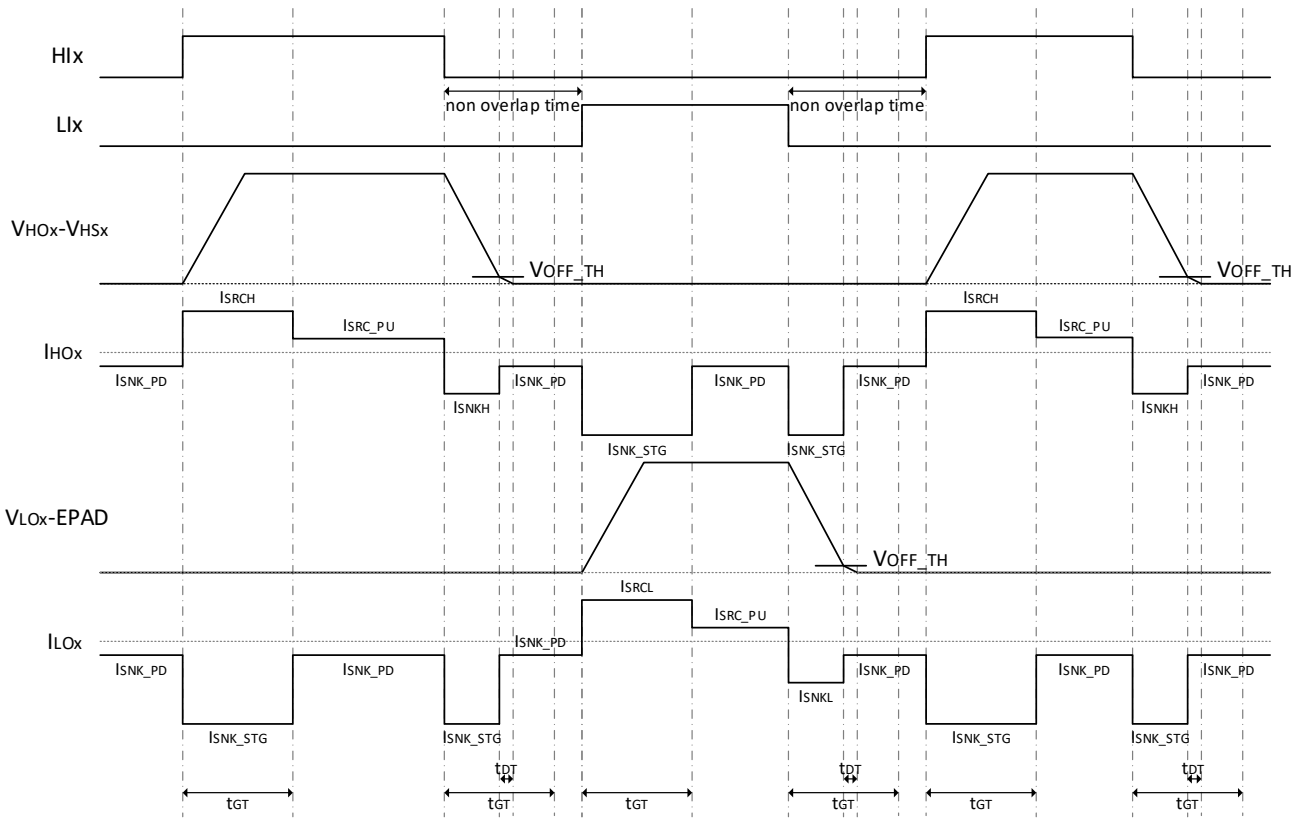


Figure 6.4-2 Gate Drive Timing Diagram in 3-Phase HI/LI Mode if the HI/LI Inserted Dead Time is Relatively Long

6.4.5 Gate Drive Timing Diagram in 3-Phase HI/LI Mode (continued)

Figure 6.4-3 shows the gate drive timing diagram if the HIx/LIx (x=A,B,C) inserted dead time is relatively short (shorter than maximum gate transition time (t_{GT}) plus extra dead time (t_{DT}) set). This case means:

- During high-side MOSFET turn-off/low-side MOSFET turn-on transition, if LIx (x=A,B,C) asserts high before the HOx-HSx (x=A,B,C) high-to-low transition time (t_{GT}) and extra dead time (t_{DT}) ends.
- During low-side MOSFET turn-off/high-side MOSFET turn-on transition, if HIx (x=A,B,C) asserts high before the LOx (x=A,B,C) high-to-low transition time (t_{GT}) and extra dead time (t_{DT}) ends.

Total effective dead time is adaptive dead time, plus extra dead time (t_{DT}) selected by DEAD_TIME bits.

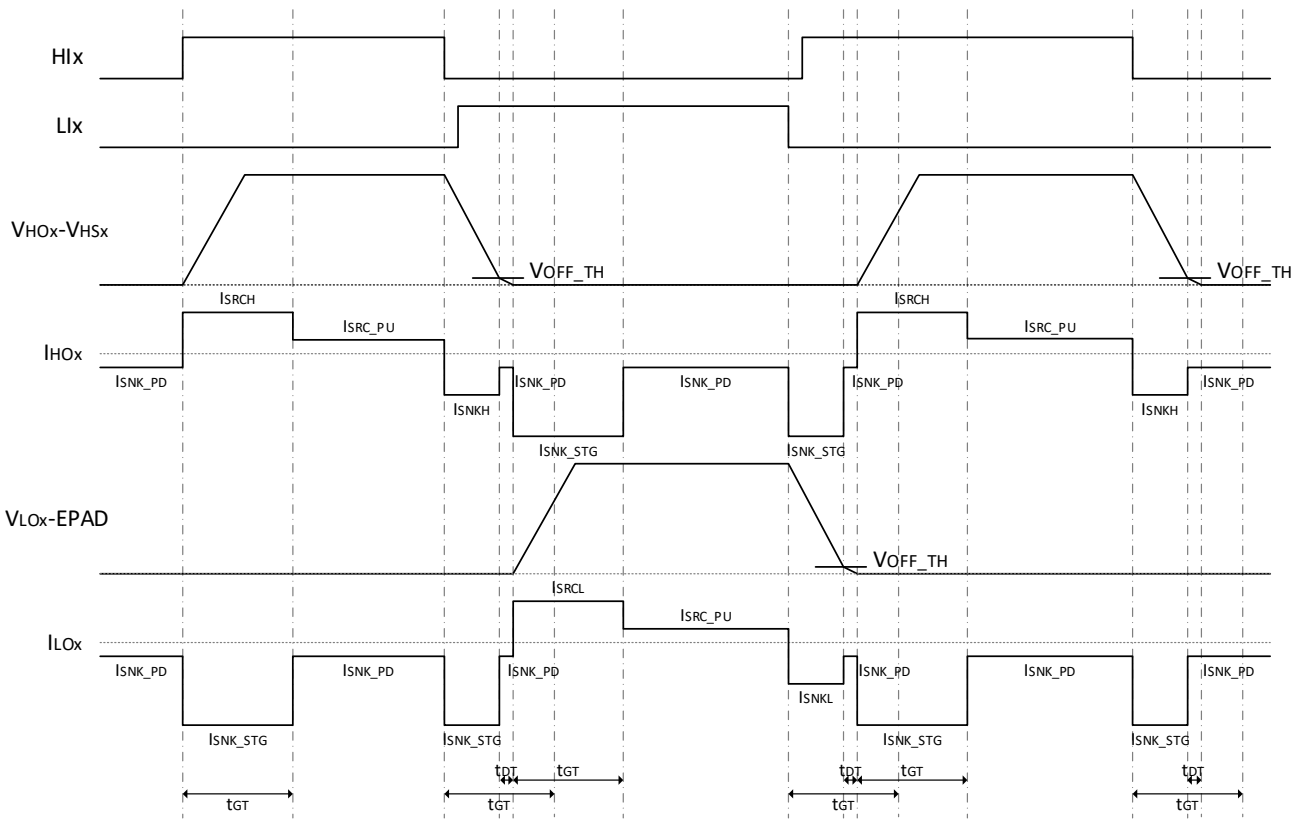


Figure 6.4-3 Gate Drive Timing Diagram in 3-Phase HI/LI Mode if the HI/LI Inserted Dead Time is Relatively Short

6.4.6 Gate Drive Timing Diagram with DIS_SADT=1b

Figure 6.4-4 shows the gate drive timing diagram with DIS_SADT=1b if the HIx/LIx (x=A,B,C) inserted dead time is shorter than maximum gate transition time (t_{GT}). This case means:

- During high-side MOSFET turn-off/low-side MOSFET turn-on transition, if LIx (x=A,B,C) asserts high after the high-side MOSFET turns off and before the HOx-HSx (x=A,B,C) high-to-low transition time (t_{GT}) ends.
- During low-side MOSFET turn-off/high-side MOSFET turn-on transition, if HIx (x=A,B,C) asserts high after the low-side MOSFET turns off and before the LOx (x=A,B,C) high-to-low transition time (t_{GT}) ends.

Total effective dead time is a non-overlap time, plus extra dead time (t_{DT}) selected by DEAD_TIME bits.

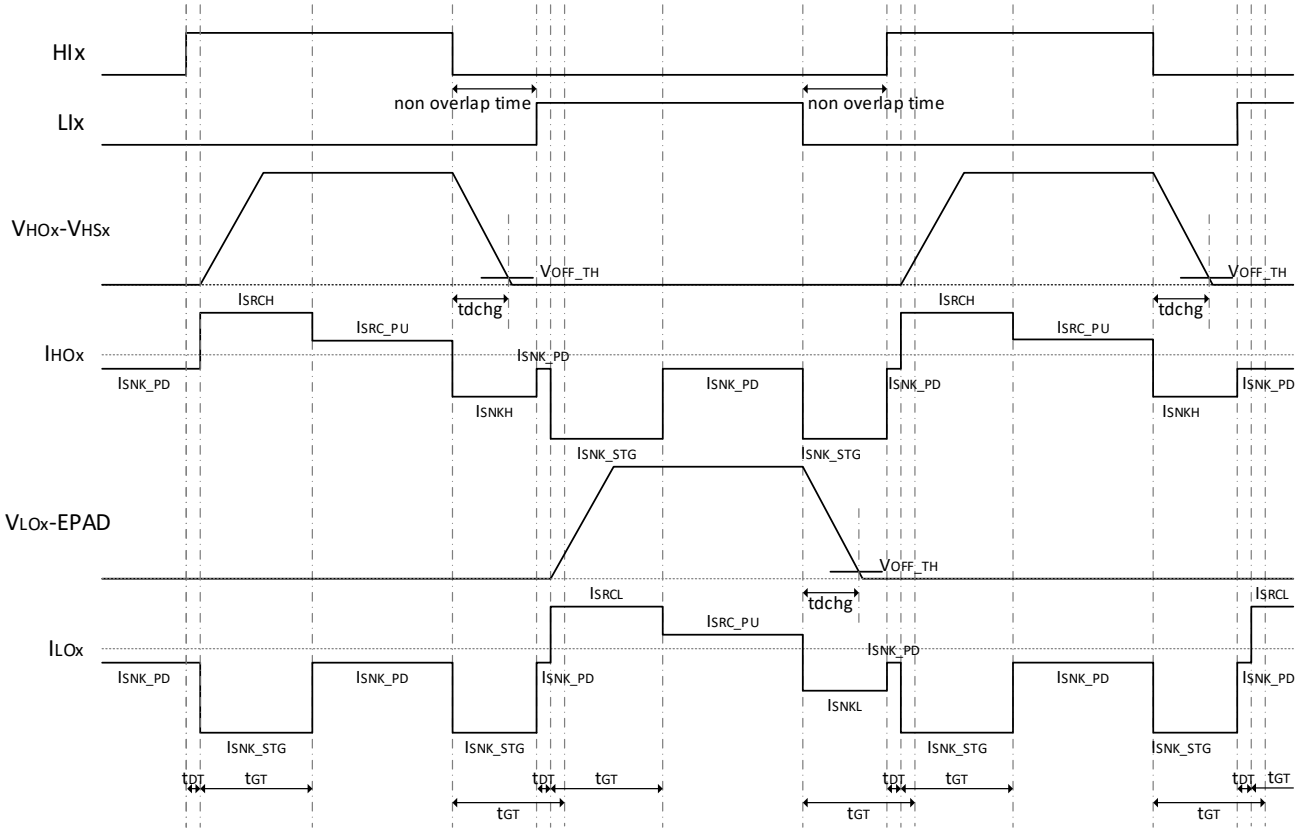


Figure 6.4-4 Gate Drive Timing Diagram with DIS_SADT=1b if the HI/LI Inserted Dead Time is Shorter than Maximum Gate Transition Time

6.4.6 Gate Drive Timing Diagram with DIS_SADT=1b (continued)

Figure 6.4-5 shows the gate drive timing diagram with DIS_SADT=1b if the HIx/LIx (x=A,B,C) inserted dead time is longer than maximum gate transition time (t_{GT}). This case means:

- During high-side MOSFET turn-off/low-side MOSFET turn-on transition, if LIx (x=A,B,C) asserts high after the HOx-HSx (x=A,B,C) high-to-low transition time (t_{GT}) ends.
- During low-side MOSFET turn-off/high-side MOSFET turn-on transition, if HIx (x=A,B,C) asserts high after the LOx (x=A,B,C) high-to-low transition time (t_{GT}) ends.

Total effective dead time is a non-overlap time, plus extra dead time (t_{DT}) selected by DEAD_TIME bits.

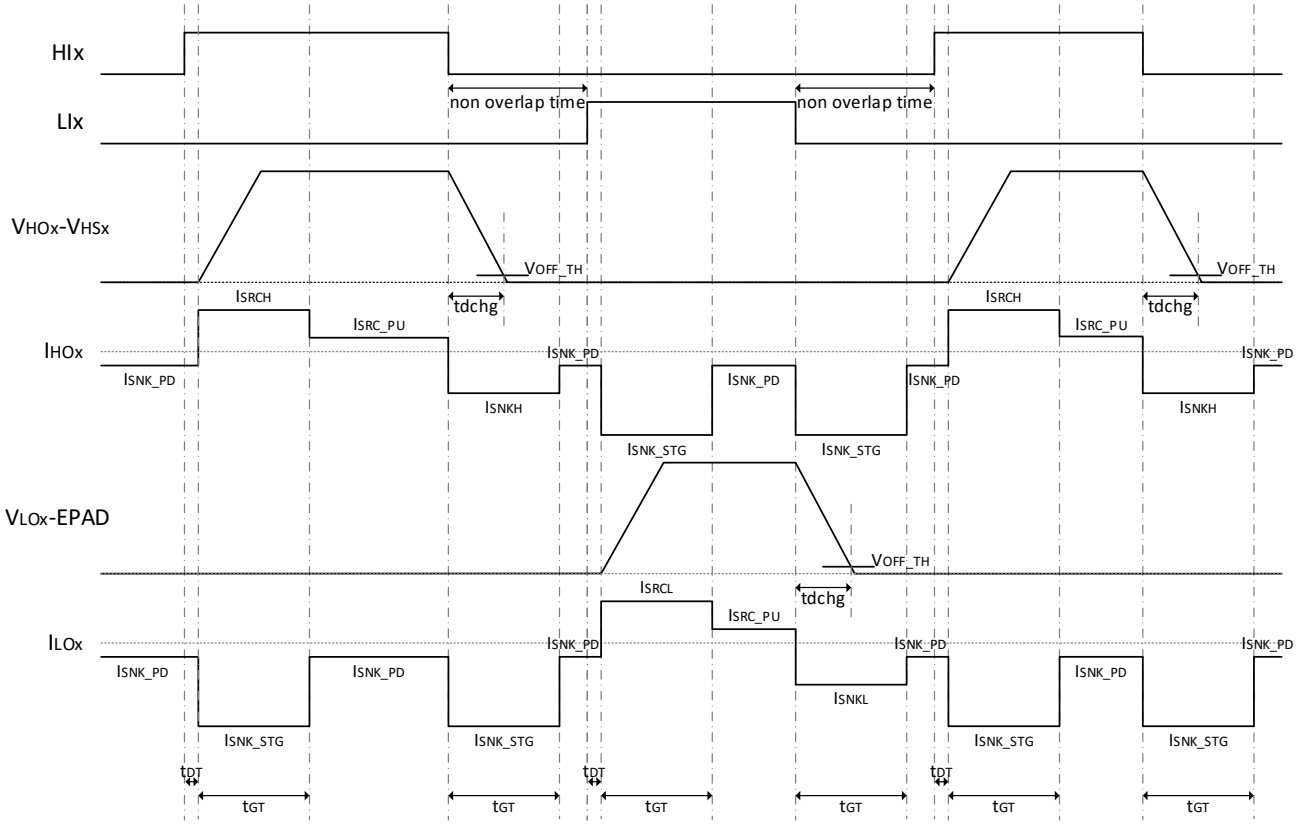


Figure 6.4-5 Gate Drive Timing Diagram with DIS_SADT=1b if the HI/LI Inserted Dead Time is Longer than Maximum Gate Transition Time

6.4.7 Gate Drive Timing Diagram in 3-Phase PWM Mode

Figure 6.4-6 shows the gate drive timing diagram when the gate driver control mode is 3-Phase PWM Mode. In this mode, the timing diagram is similar to 3-phase HI/LI Mode if the HIx/LIx (x=A,B,C) inserted dead time is zero.

Total effective dead time is adaptive dead time, plus extra dead time (t_{DT}) selected by DEAD_TIME bits.

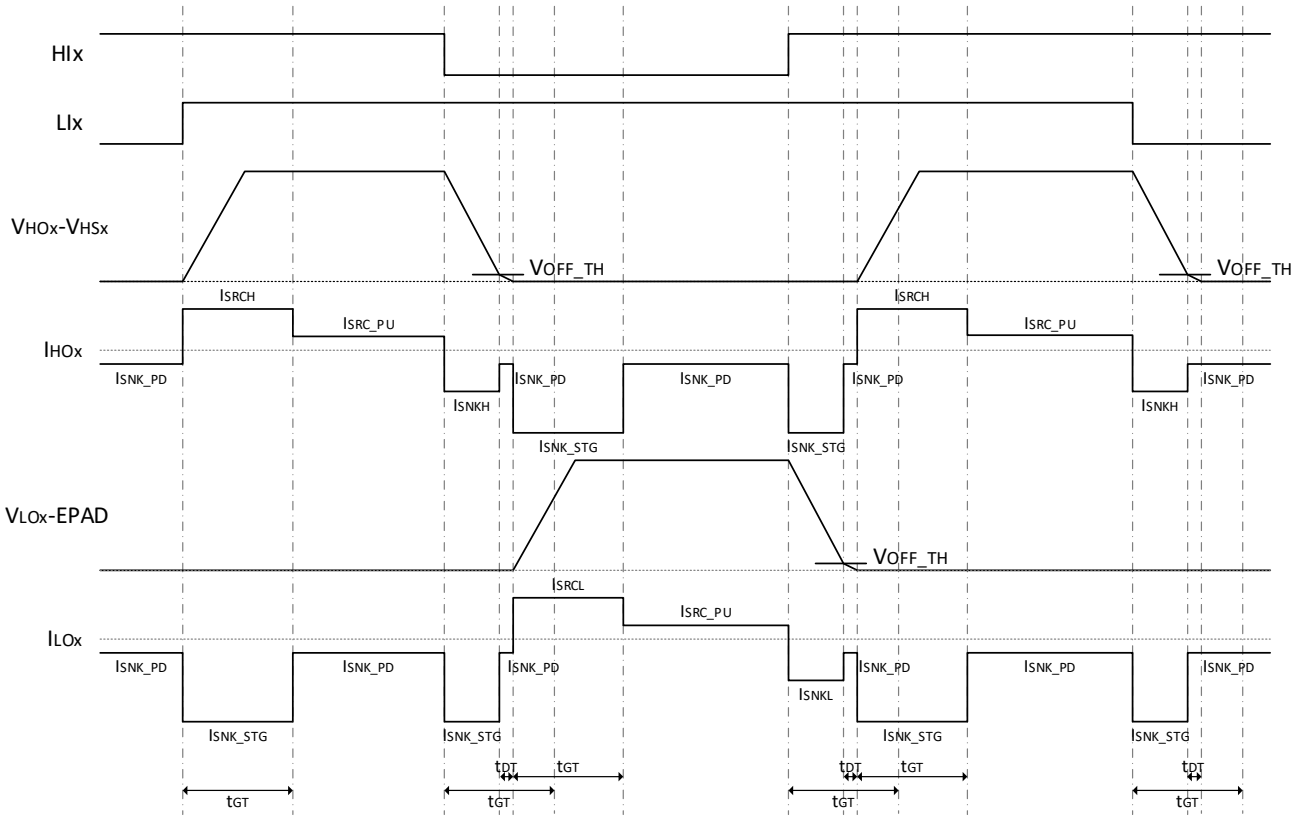


Figure 6.4-6 Gate Drive Timing Diagram in 3-Phase PWM Mode

6.5 Sense Block

6.5.1 Overview

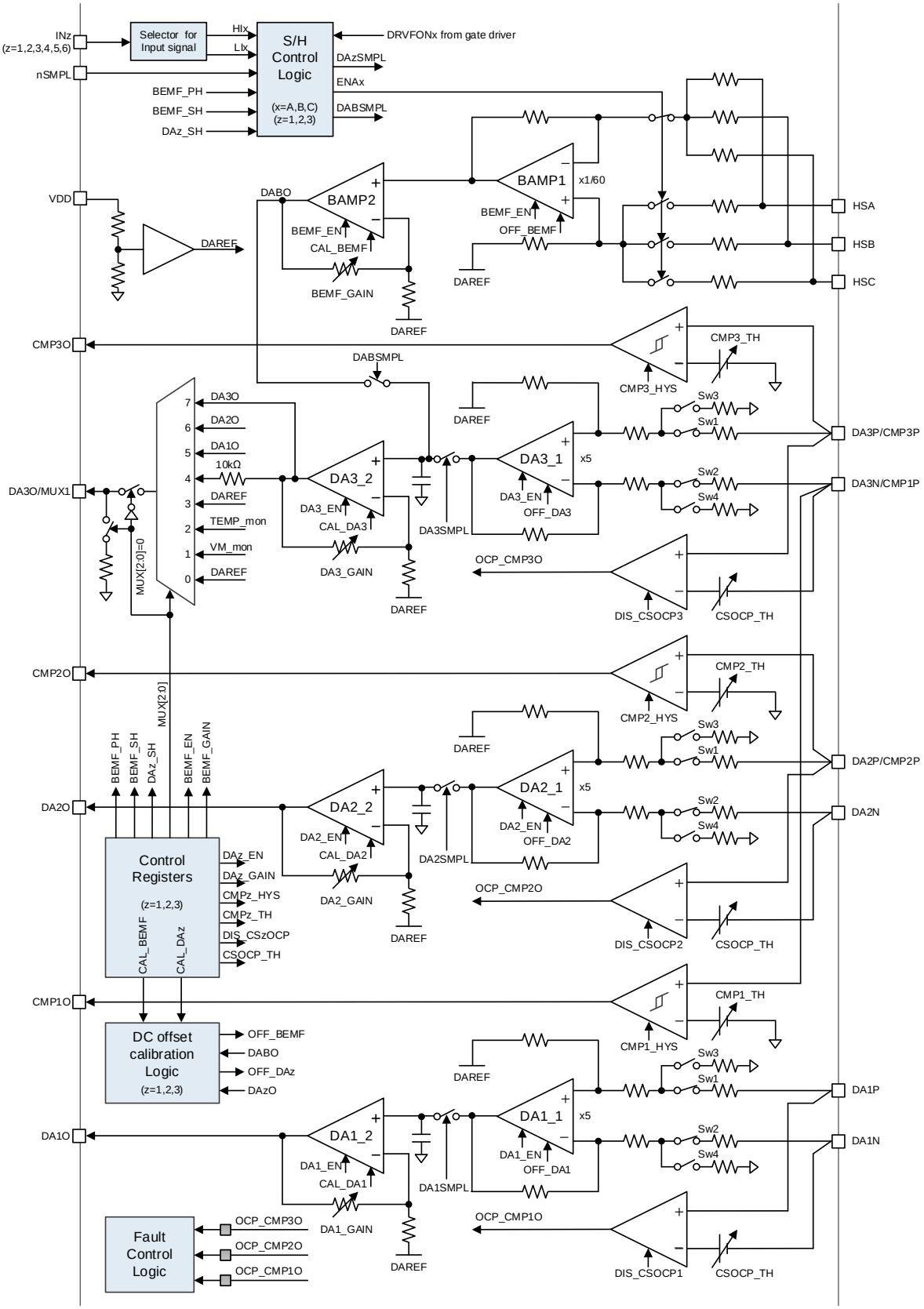


Figure 6.5-1 Block Diagram of Sense Block

6.5.1 Overview (continued)

Figure 6.5-1 shows the block diagram of sense block. The smart gate driver comprises three differential programmable gain amplifiers, three general-purpose comparators, three current sense overcurrent comparators, a BEMF sense amplifier, and an analog multiplexer. The three differential amplifiers can separately support current sensing up to three phases by using low-side shunt resistors in the external half-bridges. The general-purpose comparator has 0V to VDD input common mode range. The inputs of general-purpose comparators are DA2P, DA3P, and DA3N. The user can select these pins usage by changing the input signal only. The differential amplifiers and general-purpose comparators can be disabled individually by setting DAz_EN in the IC Control registers or CMPz_VTH (z=1,2,3) bits in the Sense Block Control registers to reduce the quiescent current. The current sense overcurrent comparator monitors the input of the differential amplifier continuously. The current sense overcurrent threshold V_{CSOCP} is selectable through the CSOCP_TH bits. Regarding BEMF (back electromotive force) sensing, two dedicated amplifiers form the BEMF sensing signal chain. The first differential amplifier outputs the voltage between high impedance phase and the virtual center tap. The high impedance phase is selected automatically at nSMPL falling edge, or selected by CMP1O/2O or CMP1O/3O inputs. The second programmable gain amplifier can adjust the output range suitably for the position detection by BEMF sensing. The output of BEMF sensing can be monitored through the analog multiplexer on DA3O/MUX1 pin. The analog multiplexer can output the VM voltage and die temperature by setting MUX bits in the Sense Block Control registers.

6.5.2 Differential Amplifiers for Current Sensing

The differential amplifier has the following functions.

Enable control:

Each differential amplifier can be disabled by DAz_EN (z=1,2,3)=0b according to the actual application.

Programmable gain:

The gain of differential amplifier is programmable by DAz_GAIN (z=1,2,3) bits. The gain settings are 5V/V, 10V/V, 20V/V, 40V/V.

Reference:

The output reference voltage of differential amplifier is 0.5*V_{DD}.

Sample and hold (S/H) function:

When DAz_SH (z=1,2,3) bit is set “1”, S/H function of the differential amplifier is enabled individually. Three differential amplifier outputs are sampled during nSMPL signal=L simultaneously. This function helps 3 shunt current sensing. Refer to Figure 6.5-2.

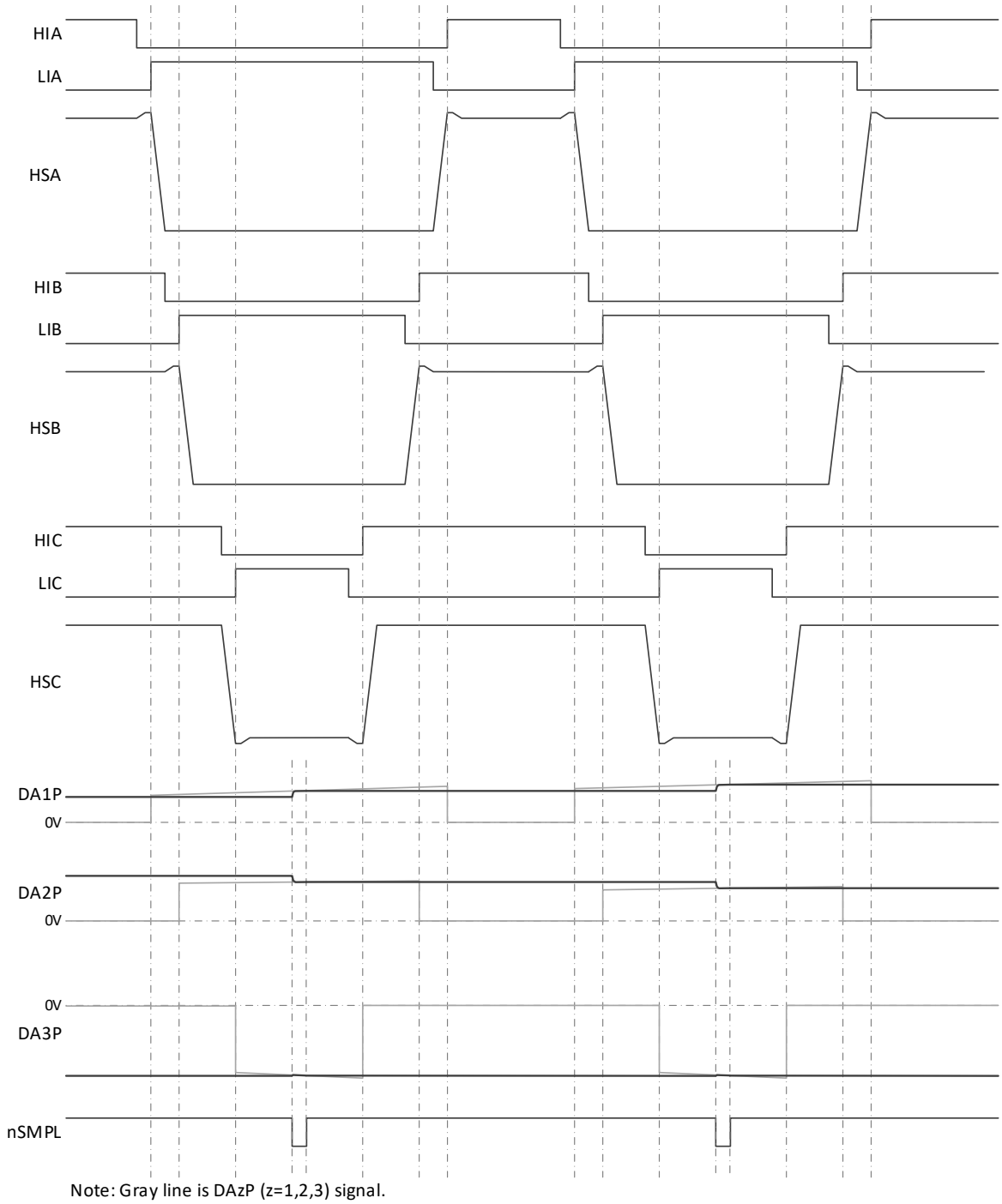
Note: The DA3O output is controlled by MUX[2:0] bits and BEMF_EN bit. When BEMF_EN bit is set to “1”, S/H switch of the differential amplifier 3 keeps turn off to avoid the conflict with BEMF sense amplifier output. When BEMF_EN bit is set to “0”, the output of the differential amplifier 3 can be monitored by MUX[2:0]=100b or 111b. Refer to section 6.5.5.

DC offset calibration:

DC offset calibration is automatically conducted upon device power up. It can also be initiated by setting CAL_DAz (z=1,2,3) bit in the Sense Block Control registers. When CAL_CONN bit is set to “0”, it is done by turning off Sw1 and Sw2, turning on Sw3 and Sw4 (connecting differential amplifier inputs to GND), and setting gain depending on DAz_GAIN (z=1,2,3) bits, and then going through an auto-zero routine to minimize amplifier input offset. When CAL_CONN bit is set to “1”, it is done by keeping Sw1 and Sw2 turn on (connecting differential amplifier inputs to the external shunt).

Note: If initiating calibration by CAL_DAz (z=1,2,3) bit, each amplifier can be calibrated individually. It takes approximately 288µs to finish calibration on each amplifier. Renesas recommends allowing 400µs per one amplifier for the calibration to complete in actual application. Although the calibration can be initiated by SPI interface even on the fly, Renesas recommends conducting the calibration when no MOSFETs are switching and with all driver output pulled low to avoid any impact of noise on calibration accuracy.

6.5.2 Differential Amplifiers for Current Sensing (continued)



Note: Gray line is DAzP (z=1,2,3) signal.
Black line is the virtual signal which sampled DAzP (z=1,2,3) by nSMPL.

Figure 6.5-2 S/H Function of Current Sensing

6.5.3 BEMF Sense Amplifier

The BEMF sense amplifier has the following functions.

Enable control:

BEMF sense amplifier can be disabled by BEMF_EN=0b according to the actual application.

Programmable gain:

The gain of BEMF sense amplifier is programmable by BEMF_GAIN bits. The gain settings are 0.05V/V, 0.1V/V, 0.5V/V, 1.0V/V with DA3_GAIN=00b.

Reference:

The output reference voltage of BEMF sense amplifier is 0.5*V_{DD}.

High impedance phase selection:

In typical trapezoidal BLDC operation, only 2-phase bridges are energized at a given time. The 3rd phase is in high impedance state (both high-side and low-side MOSFETs are turned off). By sensing the differential voltage between this high impedance phase and the virtual center tap, provides you the BEMF induced in this 3rd phase stator coil, which allows you to know/estimate the rotor position relative to this 3rd phase. This device has three methods for the high impedance phase selection according to the BEMF_PH bits. When BEMF_PH bits are set to 00xb, the 3rd phase is detected by checking the state of HIx/LIx (x=A,B,C) signals in S/H control logic. The check timing is the falling edge of nSMPL signal. When BEMF_PH bits are set to 010b or 011b, the 3rd phase is selected according to CMP1O/2O or CMP1O/3O terminals. When BEMF_PH bits are set to 1xxb, the 3rd phase is selected according to BEMF_PH1,0 bits directly. These functions help to achieve the position sensorless trapezoidal BLDC operation without the additional external circuits. Refer to Figure 6.5-3 and section 6.7.15.

Sample and hold (S/H) function:

BEMF sense amplifier also has S/H function. S/H capacitance and amplifier are common use with the differential amplifier 3. S/H switch becomes active only when BEMF_EN bit is set to “1”. The actual turning on timing of the S/H switch needs to occur after any possible transition is over. That requires to turn on after a reasonable delay relative to the HIx/LIx (x=A,B,C) rising edge. The delay time is realized by waiting for LS_ON (or HS_ON if it’s high-side turning on transition of HSx (x=A,B,C)) going high plus the configured gate driver transition time tGT. The actual turning off timing of the S/H switch aligns to the falling edge of the internal gate-off logic signal (which is issued shortly after HIx/LIx (x=A,B,C) falling edge). This ensures the hold value is not affected by the off transition.

The turn on/off timing of the S/H switch is adjustable by nSMPL signal. The S/H switch keeps turn off during nSMPL=H. If any possible transition remains after the internal S/H delay time, the adjustment of turn on timing by nSMPL signal is necessary. Refer to Figure 6.5-4.

DC offset calibration:

DC offset calibration can be initiated by setting CAL_DA3/BEMF bit with BEMF_EN=1b. The calibration phase is selectable by the combination of CAL_BCONN bit and BEMF_PH bits in the Sense Block Control registers. The amplifier gain depends on BEMF_GAIN bits. The DC offset calibration goes through an auto-zero routine to minimize amplifier input offset.

Note: If initiating calibration by CAL_DA3/BEMF bit with BEMF_EN=1b, it takes approximately 288μs to finish calibration. Renesas recommends allowing 400μs for the calibration to complete in actual application. Although the calibration can be initiated by SPI interface even on the fly, the motor has to be stop condition to avoid BEMF voltage input.

6.5.3 BEMF Sense Amplifier (continued)

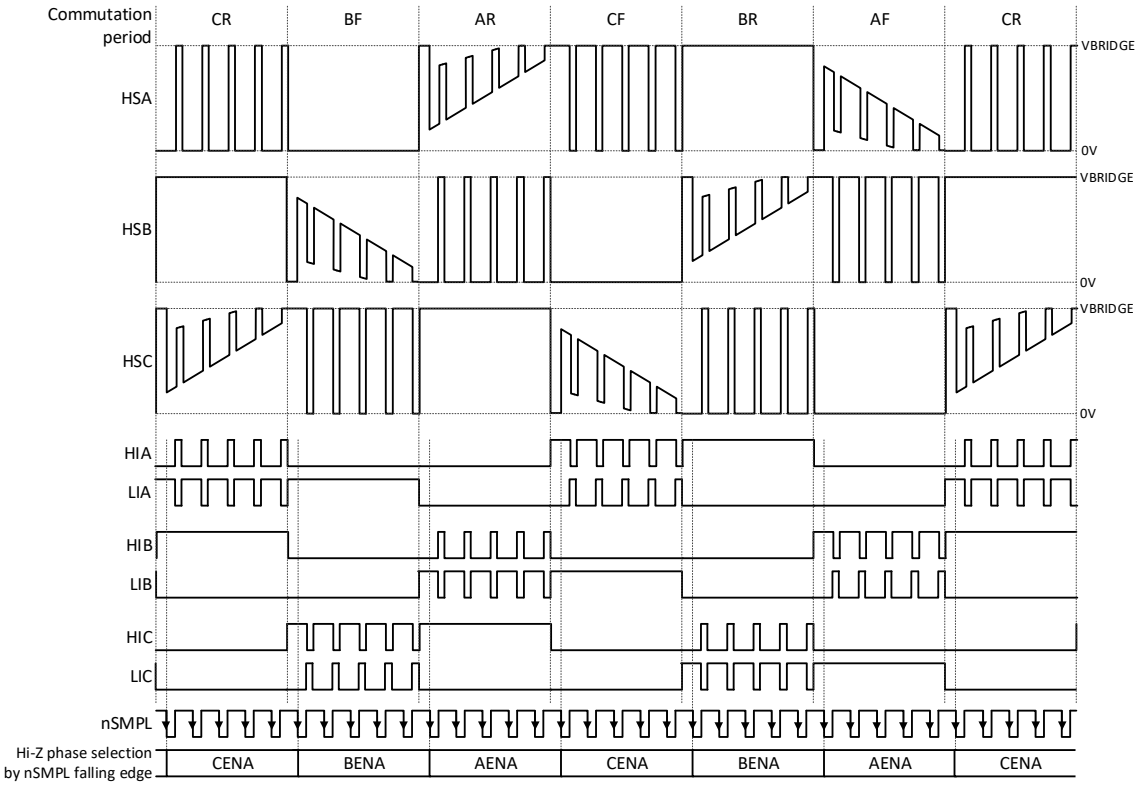


Figure 6.5-3 The Relation between Typical Six Step Trapezoidal Drive and BEMF Detect Phase

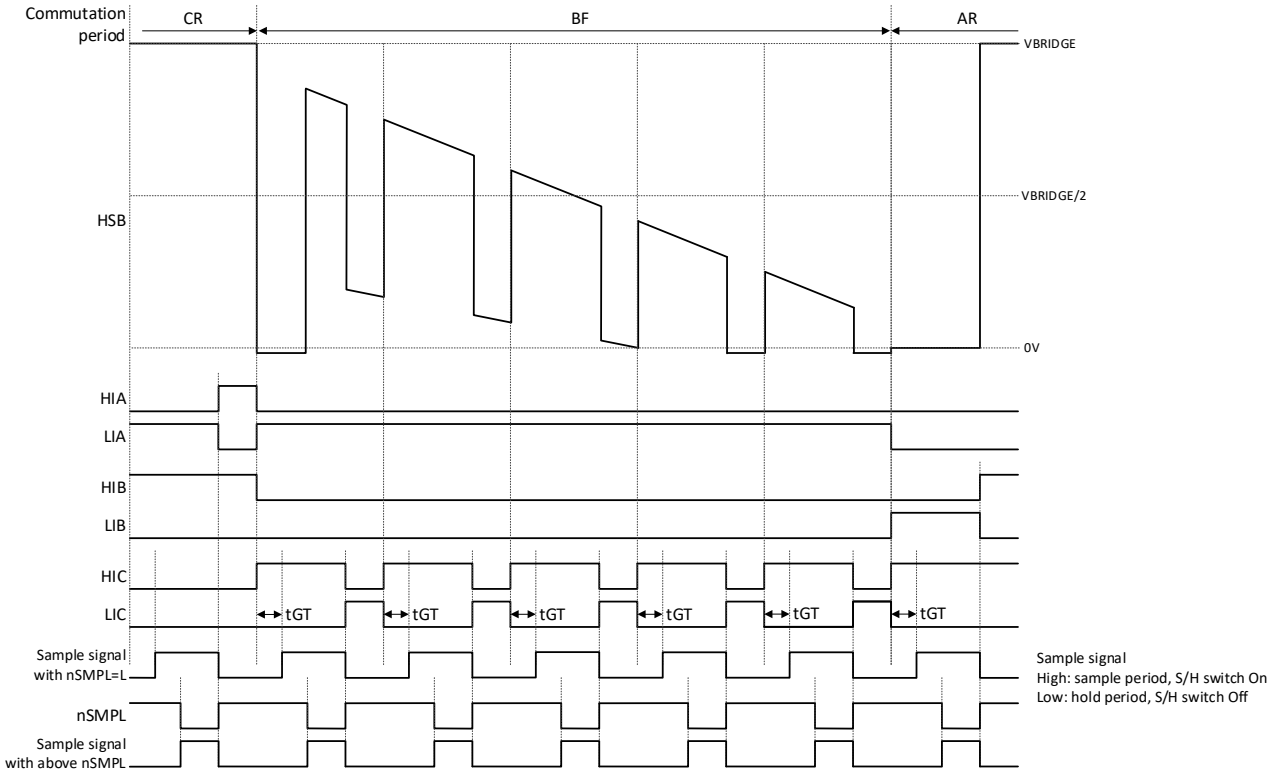


Figure 6.5-4 S/H Timing During Commutation Period BF

6.5.4 Comparators

The general-purpose comparator has the following functions.

Enable control:

Each comparator can be disabled by setting CMPz_VTH (z=1,2,3) bits to 0000b according to the actual application.

Programmable threshold voltage and hysteresis:

The threshold voltage of general-purpose comparator is programmable by CMPz_VTH (z=1,2,3) bits individually. The threshold setting including the hysteresis voltage is following equation.

- Falling: V_{TH_CMP}= V_{DD} / 16 x CMPz_VTH – 44mV x (1 – CMPz_HYS)
- Rising: V_{TH_CMP}= V_{DD} / 16 x CMPz_VTH + 44mV x (1 – CMPz_HYS)

Pin usage limitation:

The inputs of the general-purpose comparators are common use with the inputs of the differential amplifiers. When all of the differential amplifiers are used, the general-purpose comparators can be used for ONLY same inputs as the differential amplifiers.

6.5.5 MUX1 Output Control

DA3O/MUX1 pin has the analog multiplexer function. The following analog signals can be monitored depending on MUX bits in the Sense Block Control registers. After changing DA3O/MUX1 pin output or BEMF_EN bit, it is necessary to wait more than 4μs for the settling time of DA3O/MUX1 pin output.

- MUX=000b: GND (330kΩ pulldown)
- MUX=001b: VM monitor
- MUX=010b: Die temperature monitor
- MUX=011b: Differential amplifier reference voltage
- MUX=100b, BEMF_EN=0b: Differential amplifier 3 output with 10kΩ
- MUX=100b, BEMF_EN=1b: BEMF sense amplifier output with 10kΩ
- MUX=101b: Differential amplifier 1 output
- MUX=110b: Differential amplifier 2 output
- MUX=111b, BEMF_EN=0b: Differential amplifier 3 output without 10kΩ
- MUX=111b, BEMF_EN=1b: BEMF sense amplifier output without 10kΩ

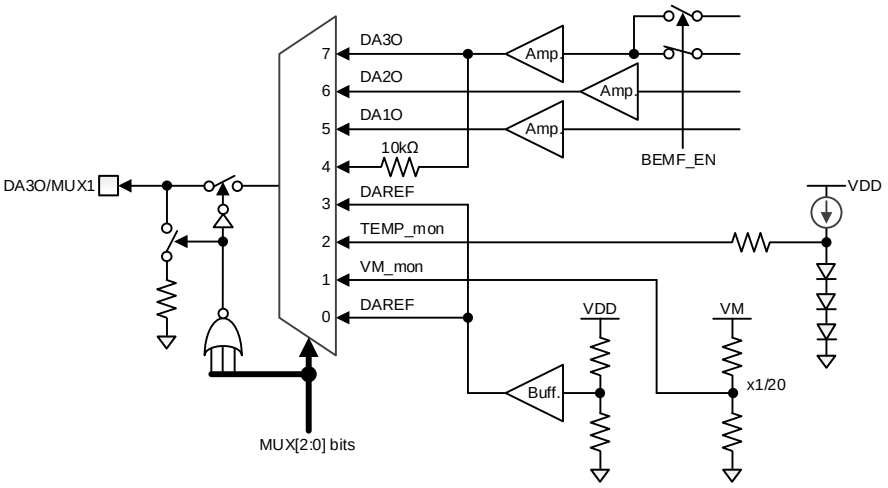


Figure 6.5-5 Block Diagram of Analog Multiplexer for DA3O/MUX1 Pin

6.5.6 VM Monitor

The output of VM attenuator can be monitored by setting 001b to MUX bits in SPI register. The relation between this monitored voltage (DA3O/MUX1 pin) and the VM voltage is shown in Figure 6.5-6.

The ratio of VM voltage and the monitored voltage (RVM) is 20.0 typical.

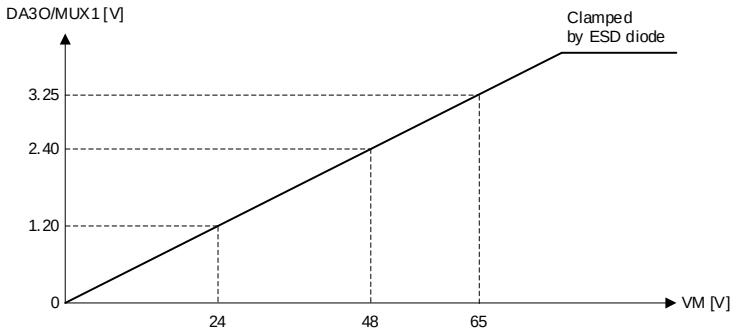


Figure 6.5-6 The Relation between DA3O/MUX1 and VM Voltage

6.5.7 Junction Temperature Monitor

The junction temperature of the die can be monitored by setting 010b to MUX bits in SPI register.
The relation between this monitored voltage (DA3O/MUX1 pin) and the junction temperature is shown in Figure 6.5-7.
The junction temperature (Tj) is calculated by the following equation.

Tj [°C]= 25[°C] + (2.000 – MUX1 voltage) [V] / 6.0 [mV/°C]

For example, in the case of ISENADIN=1.520[V]

Tj [°C]= 25[°C] + (2.000 – 1.520) [V] / 6.0 [mV/°C] =105[°C]

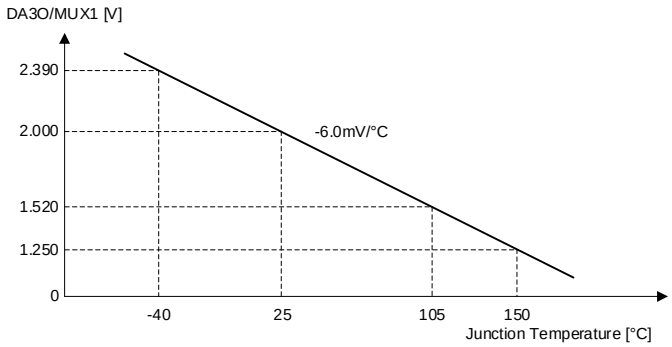


Figure 6.5-7 The Relation between DA3O/MUX1 and the Junction Temperature

6.6 SPI Communication Format

The SPI block of the smart gate driver only works in slave mode. Figure 6.6-1 shows SPI communication format of both write and read mode. If the communication format is different from Figure 6.6-1, its communication becomes invalid.

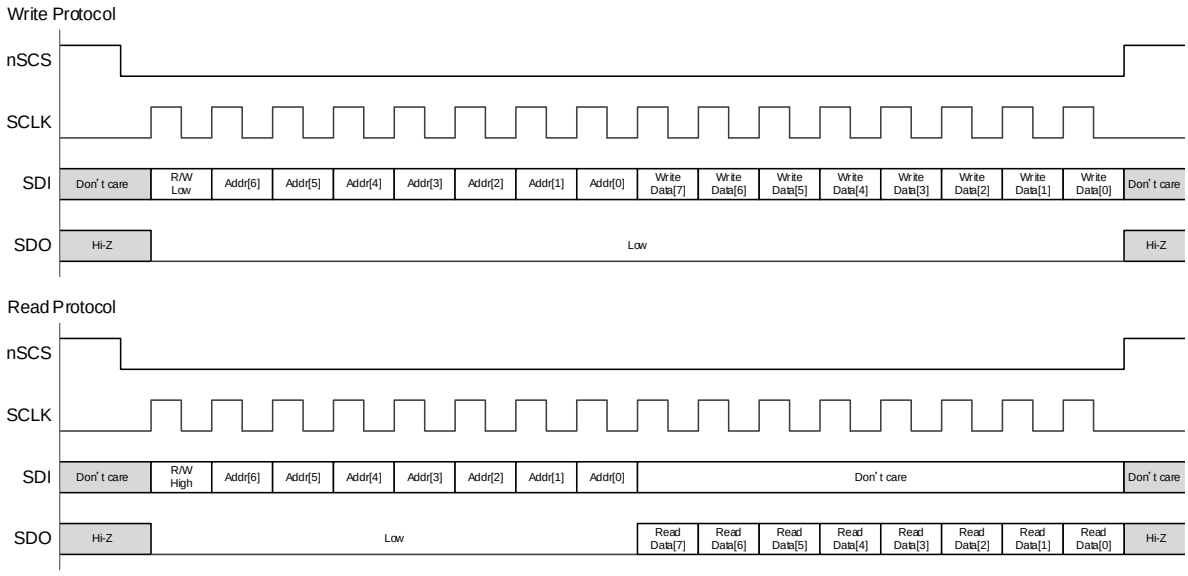


Figure 6.6-1 SPI Communication Format

6.7 Control Register Map

Table 6-7 shows the control register map of the smart gate driver. The control registers are reset by entering Sleep or Shutdown Mode. Refer to section 6.1.3 Mode Transition.

Table 6-7 Control Register Map

Address	Register Name	Symbol	Access Type	Initial value	7	6	5	4	3	2	1	0
0x00	Fault Status 0	FLTSTS0	R	00h	FAULT	SR_FAULT	OV_UVLO	VDS_OCP	VGS_FAULT	CS_OCP	OTSD	TWARN
0x01	Fault Status 1	FLTSTS1	R	00h	VDRV_UV	VDRV_OV	SR_OCP	VCP_UV	VM_UV	VM_OV	N/A	N/A
0x02	Fault Status 2	FLTSTS2	R	00h	VDSHA_OCP	VDSLA_OCP	VGSHA_FAULT	VGSLA_FAULT	VDSHB_OCP	VDSLB_OCP	VGSHB_FAULT	VGSLB_FAULT
0x03	Fault Status 3	FLTSTS3	R	00h	VDSHC_OCP	VDSLC_OCP	VGSHC_FAULT	VGSLC_FAULT	N/A	CS1_OCP	CS2_OCP	CS3_OCP
0x04	Fault Control 1	FLTCTL1	R/W	00h	DIS_VDRVUV	DIS_VDRVOV	DIS_SROC	DIS_VCPUV	DIS_VMUV	DIS_VMOV	DIS_OTSD	TWARN_REP
0x05	Fault Control 2	FLTCTL2	R/W	07h	CSOCP_MODE1	CSOCP_MODE0	VDSOCP_MODE1	VDSOCP_MODE0	DIS_VGSFLT	DIS_CS1OCP	DIS_CS2OCP	DIS_CS3OCP
0x06	IC Control 1	ICCTL1	R/W	35h	CLR_FLT	WRITE_LOCK2	WRITE_LOCK1	WRITE_LOCK0	PWMMODE	CSOCP_TH2	CSOCP_TH1	CSOCP_TH0
0x07	IC Control 2	ICCTL2	R/W	50h	DEAD_TIME1	DEAD_TIME0	T_GT1	T_GT0	BEMF_EN	DA1_EN	DA2_EN	DA3_EN
0x08	Gate Driver Control	GDCTL	R/W	FFh	ISRC_HS3	ISRC_HS2	ISRC_HS1	ISRC_HS0	ISRC_LS3	ISRC_LS2	ISRC_LS1	ISRC_LS0
0x09	Over Current Protection Control	OCPCTL	R/W	00h	VDS_TH3	VDS_TH2	VDS_TH1	VDS_TH0	TRETRY_CSOCP	TRETRY_VDSOCP	DEG_TIME1	DEG_TIME0
0x0A	Phase-A Gate Driver Input Selection	GDSELA	R/W	14h	CMP1_HYS	HOA_SEL2	HOA_SEL1	HOA_SEL0	VMUV_TH	LOA_SEL2	LOA_SEL1	LOA_SEL0
0x0B	Phase-B Gate Driver Input Selection	GDSELB	R/W	25h	CMP2_HYS	HOB_SEL2	HOB_SEL1	HOB_SEL0	PDMODE	LOB_SEL2	LOB_SEL1	LOB_SEL0
0x0C	Phase-C Gate Driver Input Selection	GDSELC	R/W	36h	CMP3_HYS	HOC_SEL2	HOC_SEL1	HOC_SEL0	CPUV_TH	LOC_SEL2	LOC_SEL1	LOC_SEL0
0x0D	Sense Block Control 1	SNSCTL1	R/W	AAh	BEMF_GAIN1	BEMF_GAIN0	DA1_GAIN1	DA1_GAIN0	DA2_GAIN1	DA2_GAIN0	DA3_GAIN1	DA3_GAIN0
0x0E	Sense Block Control 2	SNSCTL2	R/W	00h	CAL_BCONN	BEMF_PH2	BEMF_PH1	BEMF_PH0	BEMF_SH	DA1_SH	DA2_SH	DA3_SH
0x0F	Sense Block Control 3	SNSCTL3	R/W	88h	CMP1_VTH3	CMP1_VTH2	CMP1_VTH1	CMP1_VTH0	CMP2_VTH3	CMP2_VTH2	CMP2_VTH1	CMP2_VTH0
0x10	Sense Block Control 4	SNSCTL4	R/W	80h	CMP3_VTH3	CMP3_VTH2	CMP3_VTH1	CMP3_VTH0	CAL_CONN	CAL_DA1	CAL_DA2	CAL_DA3/BEMF
0x11	Sense Block Control 5	SNSCTL5	R/W	00h	DIS_SADT	RESERVED11_6	CTL6_UNLOCK	RESERVED11_4	RESERVED11_3	MUX2	MUX1	MUX0
0x12	Sense Block Control 6	SNSCTL6	R/W	40h	RESERVED12_7	BEMF_OFFSET	RESERVED12_5	RESERVED12_4	RESERVED12_3	RESERVED12_2	RESERVED12_1	GD_AOR

6.7.1 Fault Status 0 Register: FLTSTS0 (Address=0x00) [Default=0x00]

Figure 6.7-1 and Table 6.7-1 show the details of Fault Status 0 register.

Figure 6.7-1 Fault Status 0 Register FLTSTS0

7	6	5	4	3	2	1	0
FAULT	SR_FAULT	OV_UVLO	VDS_OCP	VGS_FAULT	CS_OCP	OTSD	TWARN
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 6.7-1 Fault Status 0 Register FLTSTS0 Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	Logic OR of all Fault Status bits
6	SR_FAULT	R	0b	Logic OR of the Fault Status bits for buck switching regulator: VDRV_UV, VDRV_OV, SR_OCP
5	OV_UVLO	R	0b	Logic OR of the Fault Status bits for undervoltage and overvoltage: VCP_UV, VM_UV, VM_OV
4	VDS_OCP	R	0b	Logic OR of the Fault Status bits for V_{DS} overcurrent: VDSHx_OCP, VDSLx_OCP
3	VGS_FAULT	R	0b	Logic OR of the Fault Status bits for V_{GS} fault : VGSHx_FAULT, VGSLx_FAULT
2	CS_OCP	R	0b	Logic OR of the Fault Status bits for current sense overcurrent: CS1_OCP, CS2_OCP, CS3_OCP
1	OTSD	R	0b	Indicator of thermal shutdown
0	TWARN	R	0b	Indicator of thermal warning

Note1: Fault status registers are reset by writing 1b to CLR_FLT, or recovery low pulse (>tsleep: 0.85ms) on EN pin.

6.7.2 Fault Status 1 Register: FLTSTS1 (Address=0x01) [Default=0x00]

Figure 6.7-2 and Table 6.7-2 show the details of Fault Status 1 register.

Figure 6.7-2 Fault Status 1 Register FLTSTS1

7	6	5	4	3	2	1	0
VDRV_UV	VDRV_OV	SR_OCP	VCP_UV	VM_UV	VM_OV	N/A	N/A
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 6.7-2 Fault Status 1 Register FLTSTS1 Descriptions

Bit	Field	Type	Default	Description
7	VDRV_UV	R	0b	Indicator of VDRV undervoltage (V_{DRVUV})
6	VDRV_OV	R	0b	Indicator of VDRV overvoltage (V_{DRVOV})
5	SR_OCP	R	0b	Indicator of buck switching regulator overcurrent (I_{OC2_SR})
4	VCP_UV	R	0b	Indicator of VCP undervoltage (V_{CPUV})
3	VM_UV	R	0b	Indicator of VM undervoltage (V_{VMUV})
2	VM_OV	R	0b	Indicator of VM overvoltage (V_{VMOV})
1	N/A	R	0b	Not assigned
0	N/A	R	0b	Not assigned

Note1: Fault status registers are reset by writing 1b to CLR_FLT, or recovery low pulse (>tsleep: 0.85ms) on EN pin.

6.7.3 Fault Status 2 Register: FLTSTS2 (Address=0x02) [Default=0x00]

Figure 6.7-3 and Table 6.7-3 show the details of Fault Status 2 register.

Figure 6.7-3 Fault Status 2 Register FLTSTS2

7	6	5	4	3	2	1	0
VDSHA_OCP	VDSLA_OCP	VGSHA_FAULT	VGSLA_FAULT	VDSHB_OCP	VDSLB_OCP	VGSHB_FAULT	VGSLB_FAULT
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 6.7-3 Fault Status 2 Register FLTSTS2 Descriptions

Bit	Field	Type	Default	Description
7	VDSHA_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-A high-side MOSFET
6	VDSLA_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-A low-side MOSFET
5	VGSHA_FAULT	R	0b	Indicator of V_{GS} fault on Phase-A high-side MOSFET
4	VGSLA_FAULT	R	0b	Indicator of V_{GS} fault on Phase-A low-side MOSFET
3	VDSHB_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-B high-side MOSFET
2	VDSLB_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-B low-side MOSFET
1	VGSHB_FAULT	R	0b	Indicator of V_{GS} fault on Phase-B high-side MOSFET
0	VGSLB_FAULT	R	0b	Indicator of V_{GS} fault on Phase-B low-side MOSFET

Note1: Fault status registers are reset by writing 1b to CLR_FLT, or recovery low pulse (>tsleep: 0.85ms) on EN pin.

6.7.4 Fault Status 3 Register: FLTSTS3 (Address=0x03) [Default=0x00]

Figure 6.7-4 and Table 6.7-4 show the details of Fault Status 3 register.

Figure 6.7-4 Fault Status 3 Register FLTSTS3

7	6	5	4	3	2	1	0
VDSHC_OCP	VDSLC_OCP	VGSHC_FAULT	VGSLC_FAULT	N/A	CS1_OCP	CS2_OCP	CS3_OCP
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 6.7-4 Fault Status 3 Register FLTSTS3 Descriptions

Bit	Field	Type	Default	Description
7	VDSHC_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-C high-side MOSFET
6	VDSLC_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-C low-side MOSFET
5	VGSHC_FAULT	R	0b	Indicator of V_{GS} fault on Phase-C high-side MOSFET
4	VGSLC_FAULT	R	0b	Indicator of V_{GS} fault on Phase-C low-side MOSFET
3	N/A	R	0b	Not assigned
2	CS1_OCP	R	0b	Indicator of current sense overcurrent by DA1P, DA1N inputs
1	CS2_OCP	R	0b	Indicator of current sense overcurrent by DA2P, DA2N inputs
0	CS3_OCP	R	0b	Indicator of current sense overcurrent by DA3P, DA3N inputs

Note1: Fault status registers are reset by writing 1b to CLR_FLT, or recovery low pulse (>tsleep: 0.85ms) on EN pin.

6.7.5 Fault Control 1 Register: FLTCTL1 (Address=0x04) [Default=0x00]

Figure 6.7-5 and Table 6.7-5 show the details of Fault Control 1 register.

Figure 6.7-5 Fault Control 1 Register FLTCTL1

7	6	5	4	3	2	1	0
DIS_VDRVUV	DIS_VDRVOV	DIS_SROC	DIS_VCPUV	DIS_VMUV	DIS_VMOV	DIS_OTSD	TWARN_REP
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-5 Fault Control 1 Register FLTCTL1 Descriptions

Bit	Field	Type	Default	Description
7	DIS_VDRVUV	R/W	0b	Write 1b to report status only for VDRV undervoltage (V_{DRVUV}) detection
6	DIS_VDRVOV	R/W	0b	Write 1b to report status only for VDRV overvoltage (V_{DRVOV}) detection
5	DIS_SROC	R/W	0b	Write 1b to report status only for buck switching regulator overcurrent (I_{OC2_SR}) protection
4	DIS_VCPUV	R/W	0b	Write 1b to report status only for VCP undervoltage (V_{CPUV}) detection
3	DIS_VMUV	R/W	0b	Write 1b to report status only for VM undervoltage (V_{VMUV}) detection
2	DIS_VMOV	R/W	0b	Write 1b to report status only for VM overvoltage fault (V_{VMOV}) detection
1	DIS_OTSD	R/W	0b	Write 1b to report status only for thermal shutdown
0	TWARN_REP	R/W	0b	0b: Thermal warning is reported on only TWARN bit. 1b: Thermal warning is reported on nFAULT pin, FAULT bit and TWARN bit.

6.7.6 Fault Control 2 Register: FLTCTL2 (Address=0x05) [Default=0x07]

Figure 6.7-6 and Table 6.7-6 show the details of Fault Control 2 register.

Figure 6.7-6 Fault Control 2 Register FLTCTL2

7	6	5	4	3	2	1	0
CSOCP_MODE1	CSOCP_MODE0	VDSOCP_MODE1	VDSOCP_MODE0	DIS_VGSFLT	DIS_CS1OCP	DIS_CS2OCP	DIS_CS3OCP
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 1b

Table 6.7-6 Fault Control 2 Register FLTCTL2 Descriptions

Bit	Field	Type	Default	Description
7	CSOCP_MODE1	R/W	0b	Response mode for current sense overcurrent 00b: Latch upon current sense overcurrent [Note2] 01b: Automatic retry upon current sense overcurrent 10b: Report on nFAULT pin, FAULT, CS_OCP and CS1/2/3_OCP bits only. No action takes place. 11b: Disable. No report and no action takes place.
6	CSOCP_MODE0	R/W	0b	
5	VDSOCP_MODE1	R/W	0b	Response mode for V_{DS} overcurrent 00b: Latch upon V_{DS} overcurrent [Note2] 01b: Automatic retry upon V_{DS} overcurrent 10b: Report on nFAULT pin, FAULT, VDS_OCP, VDSHx_OCP and VDSLx_OCP bits only. No action takes place. 11b: Disable, No report and no action takes place
4	VDSOCP_MODE0	R/W	0b	
3	DIS_VGSFLT	R/W	0b	Write 1b to disable V_{GS} fault detection
2	DIS_CS1OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA1P, DA1N inputs
1	DIS_CS2OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA2P, DA2N inputs
0	DIS_CS3OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA3P, DA3N inputs

Note2: Latch is recovered by writing 1b to CLR_FLT, or recovery low pulse (>tsleep: 0.85ms) on EN pin.

6.7.7 IC Control 1 Register: ICCTL1 (Address=0x06) [Default=0x35]

Figure 6.7-7 and Table 6.7-7 show the details of IC Control 1 register.

Figure 6.7-7 IC Control 1 Register ICCTL1

7	6	5	4	3	2	1	0
CLR_FLT	WRITE_LOCK2	WRITE_LOCK1	WRITE_LOCK0	PWMMODE	CSOCP_TH2	CSOCP_TH1	CSOCP_TH0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b

Table 6.7-7 IC Control 1 Register ICCTL1 Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write 1b to clear the all flagged fault status bits. This bit is reset to 0b automatically.
6	WRITE_LOCK2	R/W	0b	Write 110b to ignore all further register write except WRITE_LOCK[2:0]. Write 011b to unlock to allow register write. Writing other values takes no effect.
5	WRITE_LOCK1	R/W	1b	
4	WRITE_LOCK0	R/W	1b	
3	PWMMODE	R/W	0b	0b: 3-Phase HI/LI mode, 1b: 3-Phase PWM mode
2	CSOCP_TH2	R/W	1b	Threshold voltage setting of current sense overcurrent by DAzP, DAzN (z=1,2,3) inputs 000b: 51mV, 001b: 105mV, 010b: 157mV, 011b: 208mV, 100b: 260mV, 101b: 516mV, 110b: 773mV, 111b: 1029mV
1	CSOCP_TH1	R/W	0b	
0	CSOCP_TH0	R/W	1b	

6.7.8 IC Control 2 Register: ICCTL2 (Address=0x07) [Default=0x50]

Figure 6.7-8 and Table 6.7-8 show the details of IC Control 2 register.

Figure 6.7-8 IC Control 2 Register ICCTL2

7	6	5	4	3	2	1	0
DEAD_TIME1	DEAD_TIME0	T_GT1	T_GT0	BEMF_EN	DA1_EN	DA2_EN	DA3_EN
R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-8 IC Control 2 Register ICCTL2 Descriptions

Bit	Field	Type	Default	Description
7	DEAD_TIME1	R/W	0b	Dead time from V_{GS} voltage monitor output to start timing of another-side turn on 00b: 50ns, 01b: 100ns, 10b: 200ns, 11b: 400ns
6	DEAD_TIME0	R/W	1b	
5	T_GT1	R/W	0b	Maximum gate transition time 00b: 500ns, 01b: 1000ns, 10b: 2000ns, 11b: 4000ns
4	T_GT0	R/W	1b	
3	BEMF_EN	R/W	0b	Write 1b to enable BEMF sense amplifier.
2	DA1_EN	R/W	0b	Write 1b to enable differential amplifier 1.
1	DA2_EN	R/W	0b	Write 1b to enable differential amplifier 2.
0	DA3_EN	R/W	0b	Write 1b to enable differential amplifier 3.

6.7.9 Gate Drive Control Register: GDCTL (Address=0x08) [Default=0xFF]

Figure 6.7-9 and Table 6.7-9 show the details of Gate Drive Control register.

Figure 6.7-9 Gate Drive Control Register GDCTL

7	6	5	4	3	2	1	0
ISRC_HS3	ISRC_HS2	ISRC_HS1	ISRC_HS0	ISRC_LS3	ISRC_LS2	ISRC_LS1	ISRC_LS0
R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b

Table 6.7-9 Gate Drive Control Register GDCTL Descriptions

Bit	Field	Type	Default	Description
7	ISRC_HS3	R/W	1b	High-side gate driver output source current. Sink current is 2*(source current). 0000b: 50mA, 0001b: 60mA, 0010b: 70mA, 0011b: 80mA, 0100b: 100mA, 0101b: 120mA, 0110b: 140mA, 0111b: 160mA, 1000b: 200mA, 1001b: 240mA, 1010b: 280mA, 1011b: 320mA, 1100b: 400mA, 1101b: 480mA, 1110b: 560mA, 1111b: 640mA
6	ISRC_HS2	R/W	1b	
5	ISRC_HS1	R/W	1b	
4	ISRC_HS0	R/W	1b	
3	ISRC_LS3	R/W	1b	Low-side gate driver output source current. Sink current is 2*(source current). 0000b: 50mA, 0001b: 60mA, 0010b: 70mA, 0011b: 80mA, 0100b: 100mA, 0101b: 120mA, 0110b: 140mA, 0111b: 160mA, 1000b: 200mA, 1001b: 240mA, 1010b: 280mA, 1011b: 320mA, 1100b: 400mA, 1101b: 480mA, 1110b: 560mA, 1111b: 640mA
2	ISRC_LS2	R/W	1b	
1	ISRC_LS1	R/W	1b	
0	ISRC_LS0	R/W	1b	

6.7.10 Overcurrent Protection Control Register: OCPCTL (Address=0x09) [Default=0x00]

Figure 6.7-10 and Table 6.7-10 show the details of Overcurrent Protection Control register.

Figure 6.7-10 Overcurrent Protection Control Register OCPCTL

7	6	5	4	3	2	1	0
VDS_TH3	VDS_TH2	VDS_TH1	VDS_TH0	TRETRY_CSOCP	TRETRY_VDSOCP	DEG_TIME1	DEG_TIME0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-10 Overcurrent Protection Control Register OCPCTL Descriptions

Bit	Field	Type	Default	Description
7	VDS_TH3	R/W	0b	Threshold voltage setting of V_{DS} overcurrent fault 0000b: 40mV, 0001b: 60mV, 0010b: 80mV, 0011b: 120mV, 0100b: 160mV, 0101b: 200mV, 0110b: 240mV, 0111b: 320mV, 1000b: 400mV, 1001b: 480mV, 1010b: 600mV, 1011b: 720mV, 1100b: 960mV, 1101b: 1200mV, 1110b: 1600mV, 1111b: 2000mV
6	VDS_TH2	R/W	0b	
5	VDS_TH1	R/W	0b	
4	VDS_TH0	R/W	0b	
3	TRETRY_CSOCP	R/W	0b	Retry time for current sense overcurrent fault with CSOCP_MODE=01b, 0b: 4000µs, 1b: 70µs
2	TRETRY_VDSOCP	R/W	0b	Retry time for V_{DS} overcurrent fault with VDSOCP_MODE=01b, 0b: 4000µs, 1b: 70µs
1	DEG_TIME1	R/W	0b	Deglitch time for both current sense and V_{DS} overcurrent fault 00b: 1.57µs, 01b: 2.38µs, 10b: 3.49µs, 11b: 5.73µs
0	DEG_TIME0	R/W	0b	

6.7.11 Phase-A Gate Driver Input Selection Register: GDSELA (Address=0x0A) [Default=0x14]

Figure 6.7-11 and Table 6.7-11 show Phase-A Gate Driver Input Selection register.

Figure 6.7-11 Phase-A Gate Driver Input Selection Register GDSELA

7	6	5	4	3	2	1	0
CMP1_HYS	HOA_SEL2	HOA_SEL1	HOA_SEL0	VMUV_TH	LOA_SEL2	LOA_SEL1	LOA_SEL0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b

Table 6.7-11 Phase-A Gate Driver Input Selection Register GDSELA Descriptions

Bit	Field	Type	Default	Description
7	CMP1_HYS	R/W	0b	Comparator 1 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOA_SEL2	R/W	0b	Input selection for Phase-A high-side gate driver Note3 000b: Lo fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOA_SEL1	R/W	0b	
4	HOA_SEL0	R/W	1b	
3	VMUV_TH	R/W	0b	VM under voltage threshold setting, 0b: 5.3V, 1b: 7.5V
2	LOA_SEL2	R/W	1b	Input selection for Phase-A low-side gate driver Note3 000b: Lo fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOA_SEL1	R/W	0b	
0	LOA_SEL0	R/W	0b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

6.7.12 Phase-B Gate Driver Input Selection Register: GDSELB (Address=0x0B) [Default=0x25]

Figure 6.7-12 and Table 6.7-12 show Phase-B Gate Driver Input Selection register.

Figure 6.7-12 Phase-B Gate Driver Input Selection Register GDSELB

7	6	5	4	3	2	1	0
CMP2_HYS	HOB_SEL2	HOB_SEL1	HOB_SEL0	PDMODE	LOB_SEL2	LOB_SEL1	LOB_SEL0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b

Table 6.7-12 Phase-B Gate Driver Input Selection Register GDSELB Descriptions

Bit	Field	Type	Default	Description
7	CMP2_HYS	R/W	0b	Comparator 2 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOB_SEL2	R/W	0b	Input selection for Phase-B high-side gate driver Note3 000b: Lo fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOB_SEL1	R/W	1b	
4	HOB_SEL0	R/W	0b	
3	PDMODE	R/W	0b	Gate driver pulldown mode after VDS_OCP, CS_OCP, 0b: Hi-Z pulldown, 1b: driver output low
2	LOB_SEL2	R/W	1b	Input selection for Phase-B low-side gate driver Note3 000b: Lo fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOB_SEL1	R/W	0b	
0	LOB_SEL0	R/W	1b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

6.7.13 Phase-C Gate Driver Input Selection Register: GDSELC (Address=0x0C) [Default=0x36]

Figure 6.7-13 and Table 6.7-13 show Phase-C Gate Driver Input Selection register.

Figure 6.7-13 Phase-C Gate Driver Input Selection Register GDSELC

7	6	5	4	3	2	1	0
CMP3_HYS	HOC_SEL2	HOC_SEL1	HOC_SEL0	CPUV_TH	LOC_SEL2	LOC_SEL1	LOC_SEL0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b

Table 6.7-13 Phase-C Gate Driver Input Selection Register GDSELC Descriptions

Bit	Field	Type	Default	Description
7	CMP3_HYS	R/W	0b	Comparator 3 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOC_SEL2	R/W	0b	Input selection for Phase-C high-side gate driver Note3 000b: Lo fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOC_SEL1	R/W	1b	
4	HOC_SEL0	R/W	1b	
3	CPUV_TH	R/W	0b	VCP under voltage threshold setting, 0b: 0.58*VDRV, 1b: 0.8*VDRV
2	LOC_SEL2	R/W	1b	Input selection for Phase-C low-side gate driver Note3 000b: Lo fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOC_SEL1	R/W	1b	
0	LOC_SEL0	R/W	0b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

6.7.14 Sense Block Control 1 Register: SNSCTL1 (Address=0x0D) [Default=0xAA]

Figure 6.7-14 and Table 6.7-14 show Sense Block Control 1 register.

Figure 6.7-14 Sense Block Control 1 Register SNSCTL1

7	6	5	4	3	2	1	0
BEMF_GAIN1	BEMF_GAIN0	DA1_GAIN1	DA1_GAIN0	DA2_GAIN1	DA2_GAIN0	DA3_GAIN1	DA3_GAIN0
R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b

Table 6.7-14 Sense Block Control 1 Register SNSCTL1 Descriptions

Bit	Field	Type	Default	Description
7	BEMF_GAIN1	R/W	1b	Gain setting of BEMF sense amplifier with DA3_GAIN=00b 00b: 0.05V/V, 01b: 0.1V/V, 10b: 0.5V/V, 11b: 1.0V/V
6	BEMF_GAIN0	R/W	0b	
5	DA1_GAIN1	R/W	1b	Gain setting of differential amplifier 1 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
4	DA1_GAIN0	R/W	0b	
3	DA2_GAIN1	R/W	1b	Gain setting of differential amplifier 2 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
2	DA2_GAIN0	R/W	0b	
1	DA3_GAIN1	R/W	1b	Gain setting of differential amplifier 3 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
0	DA3_GAIN0	R/W	0b	

6.7.15 Sense Block Control 2 Register: SNSCTL2 (Address=0x0E) [Default=0x00]

Figure 6.7-15 and Table 6.7-15 show Sense Block Control 2 register.

Figure 6.7-15 Sense Block Control 2 Register SNSCTL2

7	6	5	4	3	2	1	0
CAL_BCONN	BEMF_PH2	BEMF_PH1	BEMF_PH0	BEMF_SH	DA1_SH	DA2_SH	DA3_SH
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-15 Sense Block Control 2 Register SNSCTL2 Descriptions

Bit	Field	Type	Default	Description
7	CAL_BCONN	R/W	0b	Input selection of BEMF sense amplifier during BEMF offset calibration 0b: The amplifier inputs are connected to the reference voltage of BEMF sense amplifier (DAREF) 1b: The amplifier inputs are connected to the phase selected by BEMF_PH bits
6	BEMF_PH2	R/W	0b	Detect phase selection of BEMF sense amplifier Note4 00xb: Select automatically from the input signals of the gate driver at every nSMPL falling edge 010b: Select by CMP1O and CMP2O pins (CMP1O, CMP2O)= (0,0): No selection, (0,1): Phase-A, (1,0): Phase-B, (1,1): Phase-C 011b: Select by CMP1O and CMP3O pins (CMP1O, CMP3O)= (0,0): No selection, (0,1): Phase-A, (1,0): Phase-B, (1,1): Phase-C 100b: No selection, 101b: Phase-A, 110b: Phase-B, 111b: Phase-C
5	BEMF_PH1	R/W	0b	
4	BEMF_PH0	R/W	0b	
3	BEMF_SH	R/W	0b	S/H control setting of BEMF sense amplifier Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Lo & PWM ON after tGT
2	DA1_SH	R/W	0b	S/H control setting of differential amplifier 1 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Lo
1	DA2_SH	R/W	0b	S/H control setting of differential amplifier 2 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Lo
0	DA3_SH	R/W	0b	S/H control setting of differential amplifier 3 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Lo

Note4: Refer to the detail description of Differential Amplifiers for Current Sensing and BEMF sense amplifier

6.7.16 Sense Block Control 3 Register: SNSCTL3 (Address=0x0F) [Default=0x88]

Figure 6.7-16 and Table 6.7-16 show Sense Block Control 3 register.

Figure 6.7-16 Sense Block Control 3 Register SNSCTL3

7	6	5	4	3	2	1	0
CMP1_VTH3	CMP1_VTH2	CMP1_VTH1	CMP1_VTH0	CMP2_VTH3	CMP2_VTH2	CMP2_VTH1	CMP2_VTH0
R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-16 Sense Block Control 3 Register SNSCTL3 Descriptions

Bit	Field	Type	Default	Description
7	CMP1_VTH3	R/W	1b	Threshold voltage setting of Comparator 1 0000b: Disable, 0001b to 1111b: Threshold voltage = VDD /16 x CMP1_VTH
6	CMP1_VTH2	R/W	0b	
5	CMP1_VTH1	R/W	0b	
4	CMP1_VTH0	R/W	0b	
3	CMP2_VTH3	R/W	1b	Threshold voltage setting of Comparator 2 0000b: Disable, 0001b to 1111b: Threshold voltage = VDD /16 x CMP2_VTH
2	CMP2_VTH2	R/W	0b	
1	CMP2_VTH1	R/W	0b	
0	CMP2_VTH0	R/W	0b	

6.7.17 Sense Block Control 4 Register: SNSCTL4 (Address=0x10) [Default=0x80]

Figure 6.7-17 and Table 6.7-17 show Sense Block Control 4 register.

Figure 6.7-17 Sense Block Control 4 Register SNSCTL4

7	6	5	4	3	2	1	0
CMP3_VTH3	CMP3_VTH2	CMP3_VTH1	CMP3_VTH0	CAL_CONN	CAL_DA1	CAL_DA2	CAL_DA3/BEMF
R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-17 Sense Block Control 4 Register SNSCTL4 Descriptions

Bit	Field	Type	Default	Description
7	CMP3_VTH3	R/W	1b	Threshold voltage setting of Comparator 3 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP3_VTH
6	CMP3_VTH2	R/W	0b	
5	CMP3_VTH1	R/W	0b	
4	CMP3_VTH0	R/W	0b	
3	CAL_CONN	R/W	0b	Input selection of differential amplifier during DC offset calibration 0b: The amplifier inputs are connected to GND. 1b: The amplifier inputs are connected to the external shunt.
2	CAL_DA1	R/W	0b	Write 1b to enable DC offset calibration for differential amplifier 1. This bit is automatically reset to 0 after calibration is done.
1	CAL_DA2	R/W	0b	Write 1b to enable DC offset calibration for differential amplifier 2. This bit is automatically reset to 0 after calibration is done.
0	CAL_DA3/BEMF	R/W	0b	Write 1b to this bit to enable DC offset calibration for differential amplifier 3 if BEMF sensing is disabled (BEMF_EN=0b). Write 1b to this bit to enable DC offset calibration for BEMF sensing amplifiers if BEMF sensing is enabled (BEMF_EN=1b). This bit automatically resets to 0 after calibration is done

6.7.18 Sense Block Control 5 Register: SNSCTL5 (Address=0x11) [Default=0x00]

Figure 6.7-18 and Table 6.7-18 show Sense Block Control 5 register.

Figure 6.7-18 Sense Block Control 5 Register SNSCTL5

7	6	5	4	3	2	1	0
DIS_SADT	RESERVED11_6	CTL6_UNLOCK	RESERVED11_4	RESERVED11_3	MUX2	MUX1	MUX0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-18 Sense Block Control 5 Register SNSCTL5 Descriptions

Bit	Field	Type	Default	Description
7	DIS_SADT	R/W	0b	Write 1b to disable the adaptive dead time control function
6	RESERVED11_6	R/W	0b	Reserved. The write value should be 0b.
5	CTL6_UNLOCK	R/W	0b	Write 0b to ignore SNSCTL6 register write. Write 1b to unlock to allow SNSCTL6 register write.
4	RESERVED11_4	R/W	0b	Reserved. The write value should be 0b.
3	RESERVED11_3	R/W	0b	Reserved. The write value should be 0b.
2	MUX2	R/W	0b	Output selection of DA3O/MUX1 pin 000b: GND (pulldown: 330kΩ) 001b: VM monitor 010b: TEMP monitor 011b: Differential amplifier reference voltage 101b: Differential amplifier 1 output 110b: Differential amplifier 2 output In case of BEMF_EN=0b, 100b: Differential amplifier 3 output w/ 10kΩ 111b: Differential amplifier 3 output w/o 10kΩ In case of BEMF_EN=1b, 100b: BEMF sense amplifier output w/ 10kΩ 111b: BEMF sense amplifier output w/o 10kΩ
1	MUX1	R/W	0b	
0	MUX0	R/W	0b	

6.7.19 Sense Block Control 6 Register: SNSCTL6 (Address=0x12) [Default=0x40]

Figure 6.7-19 and Table 6.7-19 show Sense Block Control 6 register. CTL6_UNLOCK=1b is necessary to allow SNSCTL6 register write. After writing SNSCTL6 register, CTL6_UNLOCK should be set to 0b.

Figure 6.7-19 Sense Block Control 6 Register SNSCTL6

7	6	5	4	3	2	1	0
RESERVED12_7	BEMF_OFFSET	RESERVED12_5	RESERVED12_4	RESERVED12_3	RESERVED12_2	RESERVED12_1	GD_AOR
R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 6.7-19 Sense Block Control 6 Register SNSCTL6 Descriptions

Bit	Field	Type	Default	Description
7	RESERVED12_7	R/W	0b	Reserved. The write value should be 0b.
6	BEMF_OFFSET	R/W	1b	Data selection of BEMF sense amplifier DC offset 0b: calibration data, 1b: trimming data by shipping test This bit automatically sets to 0 after DC offset calibration for BEMF sense amplifier is done.
5	RESERVED12_5	R/W	0b	Reserved. The write value should be 0b.
4	RESERVED12_4	R/W	0b	Reserved. The write value should be 0b.
3	RESERVED12_3	R/W	0b	Reserved. The write value should be 0b.
2	RESERVED12_2	R/W	0b	Reserved. The write value should be 0b.
1	RESERVED12_1	R/W	0b	Reserved. The write value should be 0b.
0	GD_AOR	R/W	0b	Write 1b to enable the active override mode of the gate driver logic.

7 MCU Description

7.1 Features

The integrated MCU is the RL78/G1F (R5F11BLE) with following features.

- **Ultra-low power consumption technology**
  - Operation from 3.135V to 5.5V supply
  - Three low power consumption modes (HALT, STOP, SNOOZE mode)
- **16-bit CISC CPU core**
  - CISC architecture with 3-stage pipeline
  - Minimum instruction execution time: Can be changed from high speed (0.03125 us: @ 32 MHz) to low speed (1.00000 us: @ 1 MHz) operation with high-speed on-chip oscillator
  - Multiply/divide/multiply & accumulate instructions are supported
  - Address space: 1 MB
  - General-purpose registers: (8-bit register x 8) x 4 banks
  - On-chip RAM: 5.5 KB
- **Code flash memory**
  - Code flash memory: 64 KB
  - Block size: 1 KB
  - Prohibition of block erase and rewriting (security function)
  - On-chip debug function
  - Self-programming (with boot swap function/flash shield window function)
- **Data flash memory**
  - Data flash memory: 4 KB
  - Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
  - Number of rewrites: 1,000,000 times (TYP.)
  - Voltage of rewrites: VDD = 3.135 to 5.5 V
- **High-speed on-chip oscillator**
  - Select from 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
  - High accuracy: ±1.0% (VDD = 1.8 to 5.5 V, TA = -20 to +85°C)
- **Operating ambient temperature**
  - TA = –40 to +105°C (G: Industrial applications)
- **Power management and reset function**
  - On-chip power-on-reset (POR) circuit
  - On-chip voltage detector (LVD)
- **Data transfer controller (DTC)**
  - Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
  - Activation sources: Activated by interrupt sources.
  - Chain transfer function
- **Event link controller (ELC)**
  - Event signals of 21 types can be linked to the specified peripheral function.
- **Serial interfaces**
  - CSI: 3 channels (CSI00 is only internal use)
  - UART: 1 channel
  - I^2C/simplified I^2C: 2 channels

7.1 Features (continued)

- **Timer**
  - 16-bit timer: 9 channels
    (Timer Array Unit (TAU): 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels (with PWMOPA, Timer RD is only internal use.),Timer RG: 1 channel, Timer RX: 1 channel)
  - 12-bit interval timer: 1 channel
  - Real-time clock: 1 channel (Constant-period interrupt function only)
  - Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)
- **A/D converter**
  - 8/10-bit resolution A/D converter (VDD = 1.6 to 5.5 V)
  - Analog input: 11 channels
    Sample and hold function: 3 channels (ANI5 to ANI7 through PGA in the smart gate driver)
    ANI0 to ANI4, ANI16, ANI17, and ANI19 (9ch) can be input from the external pin.
    ANI5 can be selectable input from the external pin or internally through PGA in the smart gate driver
  - Internal reference voltage (1.45 V) and temperature sensor
- **D/A converter**
  - 8-bit resolution D/A converter (VDD = 1.6 to 5.5 V)
  - Analog output: 2 channels
  - Output voltage: 0 V to VDD
  - Real-time output function
- **Comparator**
  - 2 channels (pin selector is provided for 1 channel)
  - Incorporates a function for the output of a timer window in combination with the timer array unit.
  - The external reference voltage or internal reference voltage can be selected as the reference voltage.
- **PGA**
  - 1 channel (x4, 8, 16, 32 from PGAI pin in the MCU)
  - 3 channels (x5, 10, 20, 40 from DAzP, DAzN (z=1,2,3) pins in the smart gate driver)
- **I/O port**
  - I/O port: 29 (N-ch open drain I/O [withstand voltage of 6 V]: 2, N-ch open drain I/O [VDD_MCU withstand voltage]: 6)
  - Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
  - On-chip key interrupt function
  - On-chip clock output/buzzer output controller
- **Useful functions for IEC60730 and IEC61508 compliance**
  - Flash memory CRC operation function (high-speed CRC, general-purpose CRC)
  - RAM parity error detection function
  - RAM guard function
  - SFR guard function
  - Invalid memory access detection function
  - Frequency detection function
  - A/D test function
  - Digital output signal level detection function for I/O pins
- **Others**
  - On-chip BCD (binary-coded decimal) correction circuit

For more details, refer to *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.

7.2 Reset Function

The following seven operations are available to generate a reset signal. External and internal resets start program execution from the address at 00000H and 00001H when the reset signal is generated.

(1) External reset input via /RESET pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
(4) Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
(5) Internal reset by execution of illegal instruction (code FFH)
(6) Internal reset by RAM parity error
(7) Internal reset by illegal-memory access

For more details, refer to chapter 27 RESET FUNCTION in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.
After MCU is reset, I/O port P146 connected to EN terminal for the smart gate driver internally becomes high impedance immediately. As the EN terminal has an internal pulldown resistance (100kΩ), the smart gate driver also enters Sleep Mode. Refer to section 6.1.3 Mode Transition.

7.3 Standby Function

The standby function reduces the operating current of the system, and the following three modes are available.

(1) HALT mode
HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode
STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current. Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

(3) SNOOZE mode
In the SNOOZE mode, the STOP mode is released by the CSI00 or UART0 data reception, an A/D conversion request by the timer trigger signal (the interrupt request signal (INTRTC/INTIT) or ELC event input), or DTC start source, and the CSI00 or UART0 data reception, A/D conversion, and DTC operation is performed without operating the CPU. This can only be specified when the high-speed on-chip oscillator is selected for the CPU/peripheral hardware clock (fCLK).
In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

For more details, refer to chapter 26 STANDBY FUNCTION in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.
This device can optimize the power consumption by these three modes of RL78/G1F, the modes of the smart gate driver operation, and the enable control for each block in the smart gate driver. For details, refer to section 6.1 Power-On Sequence and Functional Modes.

7.4 Port Functions

The RL78/G1F microcontrollers are provided with digital I/O ports, which enable variety of control operations. In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see chapter 2 PIN FUNCTIONS in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.

After a reset, all pins except for P02 and P03 function as input pins immediately, and P02 and P03 function as analog input ports. All pin functions are switched by register settings. The setting of each pin is specified by the registers for the corresponding I/O port and alternate functions. Table 7.4-1 lists the specifications of I/O ports. The port settings for not only the external I/O pins but also the internal connection ports including unused pins according to Table 7.4-1 are also necessary. For details of the I/O ports, see chapter 4 PORT FUNCTIONS in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.

Table 7.4-1 Specifications of I/O ports

Port symbol	I/O pins	Number of pins	Internal connect ports (terminals of smart gate driver)	Note
PORT0	P00 to P04	5	P05 (nSCS) P06 (Unused)	P05 is used as an output port for smart gate driver control. Need to set P06 to output port.
PORT1	P17	1	P10 to P15 (IN6 to IN1) P16 (Unused)	P10 to P15 are used as output ports for smart gate driver control. Need to set P16 to output port. P17 is common use with nSMPL terminal for S/H function.
PORT2	P20 to P25	6	P25 (DA3O) P26 (DA2O) P27 (DA1O)	P25 is common use with DA3O terminal for the differential amplifier. P26, P27 are available as the ADC input through the PGA.
PORT3	P31	1	P30 (SCLK)	P30 is used as an output port for smart gate driver control.
PORT4	P40 to P43	4	—	—
PORT5	—	—	P50 (SDO) P51 (SDI) P52 (nFAULT) P53 to P55 (CMP3,2,1O)	P50 is used as an output port for smart gate driver control. P51 and P52 are used as input ports for smart gate driver control. P53 to P55 port settings depend on the usage. P53 to P55 are available as the interrupt function through the comparator
PORT6	P60, P61	2	P62, P63 (Unused)	Need to set the port's output latch to 0.
PORT7	P73 to P77	5	P70 to P72 (Unused)	Need to set P70, P71, P72 to output port.
PORT12	P120, P122	2	P121 (Unused) P123, P124 (Unused)	Need to set P121 to input port. P121 is connected with P122 pin. Need to set P123, P124 to input port. P123,P124 are connected with /RESET pin.
PORT13	P137	1	P130 (Unused)	No port setting is necessary for P130.
PORT14	P140, P141	2	P146 (EN) P147 (Unused)	P146 is used as an output port for smart gate driver control. Need to set P147 to output port.
	Total of pins	29		

7.5 Serial Array Unit

RL78/G1F has two serial array units. Serial array unit 0 has four serial channels. Serial array unit 1 has two serial channels. Serial array unit 1 is NOT available as this device has no corresponding I/O pins. The serial channel has three modes (CSI, UART, and Simplified I^2C). The all three modes are available by using serial array unit 0. For more details of serial array unit, refer to chapter 19, SERIAL ARRAY UNIT in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)".*

Table 7.5-1 Functions of SCI Channels

Unit	Channel	Used as CSI	Used as UART	Used as simplified I^2C
0	0	CSI00 Note1 (Not support slave select input function)	Not available	Not available
	1	CSI01		IIC01
	2	CSI10	UART1	IIC10
	3	Not available		Not available
1	0	Not available	Not available	Not available
	1	Not available		Not available

Note1: CSI00 is used for the communication between RL78/G1F and the smart gate driver.
CSI00 is not available for the external communication interface.

P51(SO00), P50(SI00), and P30(SCK00) of RL78/G1F are connected internally with the smart gate driver. RL78/G1F can access the registers of the smart gate driver by CSI00.
Please set CSI00 settings as follows.

- To disable slave select input function (/SSI00 pin), setting of SSIE00 =0 in ISC register is required. Refer to Section 19.3.15, Input switch control register (ISC) in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.
- To use type2 (DAP00=0, and CPK00=1 in SCR00 register).
  Refer to Section 19.3.4, Serial communication operation setting register mn (SCRmn) in *"RL78/G1F User's Manual: Hardware (R01UH0516EJ)"*.

8 External Circuit

The external circuit in the case of sensorless motor drive by BEMF sensing comparator is shown as Figure 8-1. The recommended value of each external component is shown in Table 8-1.

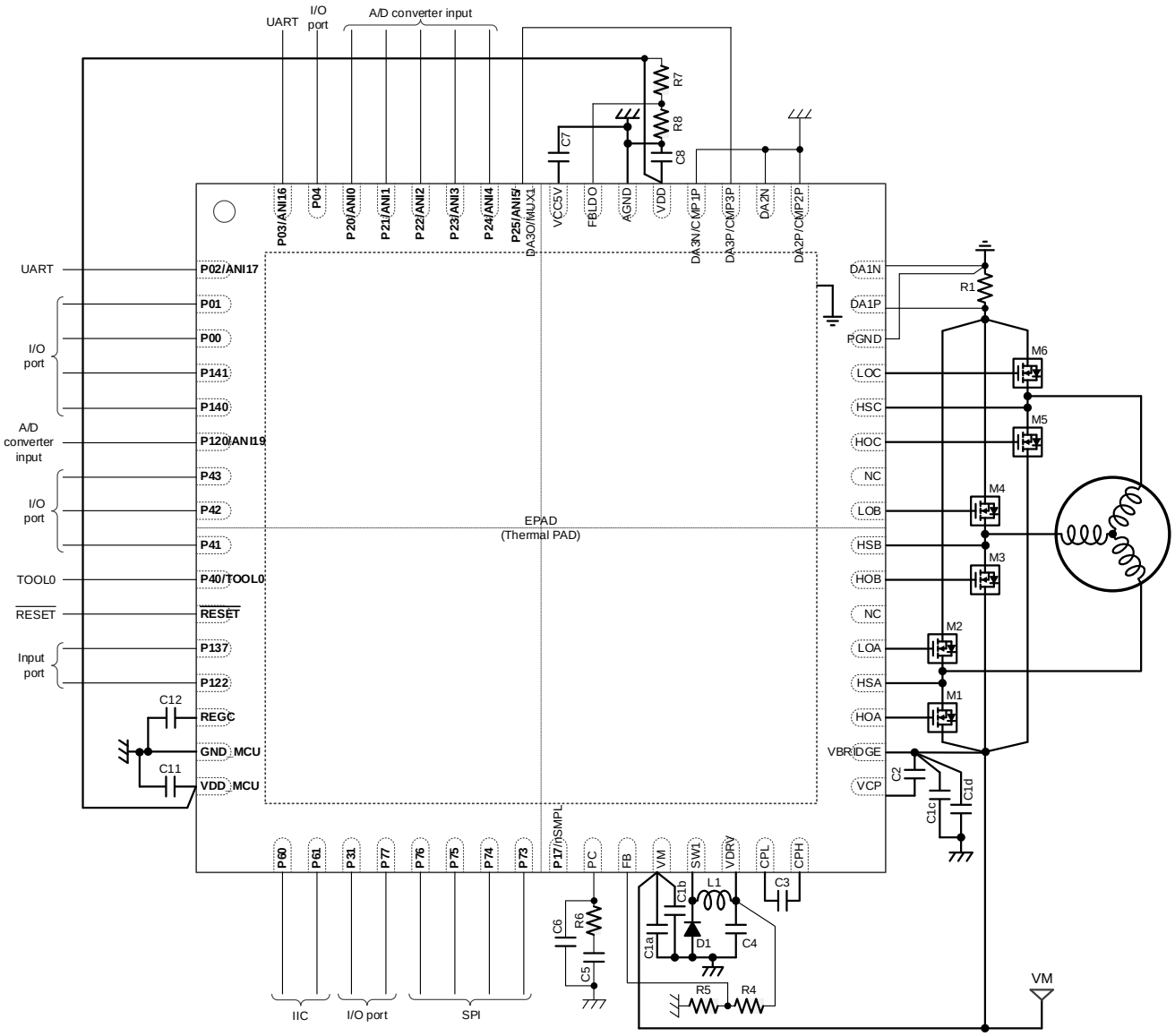


Figure 8-1 External Circuit Example – Sensorless Motor Drive by BEMF Sensing Comparator

8 External Circuit (continued)

Table 8-1 The External Component List

Part No.	Recommended value	Ratings	Purpose	Notes
R1	Depend on application	Depend on application	Shunt resistance for current sense	
R4	48.7kΩ	-	Bleeder resistance for VDRV output voltage setting	1
R5	3.48kΩ	-	Bleeder resistance for VDRV output voltage setting	1
R6	60.4kΩ	-	Phase compensation resistance for the switching regulator	4
R7	160kΩ	-	Bleeder resistance for VDD output voltage setting	2
R8	91kΩ	-	Bleeder resistance for VDD output voltage setting	2
C1a	3x 4.7μF	100V	Bypass capacitance for VM terminal	5
C1b	0.1μF	100V	Bypass capacitance for VM terminal	5
C1c	4.7μF	100V	Bypass capacitance for VBRIDGE terminal	5
C1d	0.1μF	100V	Bypass capacitance for VBRIDGE terminal	5
C2	2.2μF	25V	Bypass capacitance for VCP terminal	3
C3	0.22μF	100V	Pumping capacitance for the charge pump	3
C4	10μF	25V	Output capacitance for the switching regulator, VDRV terminal	4
C5	2200pF	10V	Phase compensation capacitance for the switching regulator	4
C6	DNP	10V	Phase compensation capacitance for the switching regulator	
C7	22μF	10V	Output capacitance for the linear regulator, VCC5V terminal	
C8	22μF	10V	Output capacitance for the linear regulator, VDD terminal	
C11	0.1μF	10V	Bypass capacitance for VDD_MCU terminal	
C12	0.47μF	10V	Regulator output stabilization capacitance	
M1 to M6	Depend on application	Depend on application	Power MOSFET for the motor drive	
L1	22μH or 33μH	>2A	Coil for the switching regulator	
D1	0.6V	100V, >2A	Schottky rectifier diode for the switching regulator	

Please refer to *"RAJ306102 User's Manual: Hardware (R18UZ0082EJ)"* for the details to select the parts.

Note1: VDRV output voltage is 12V with these resistors.

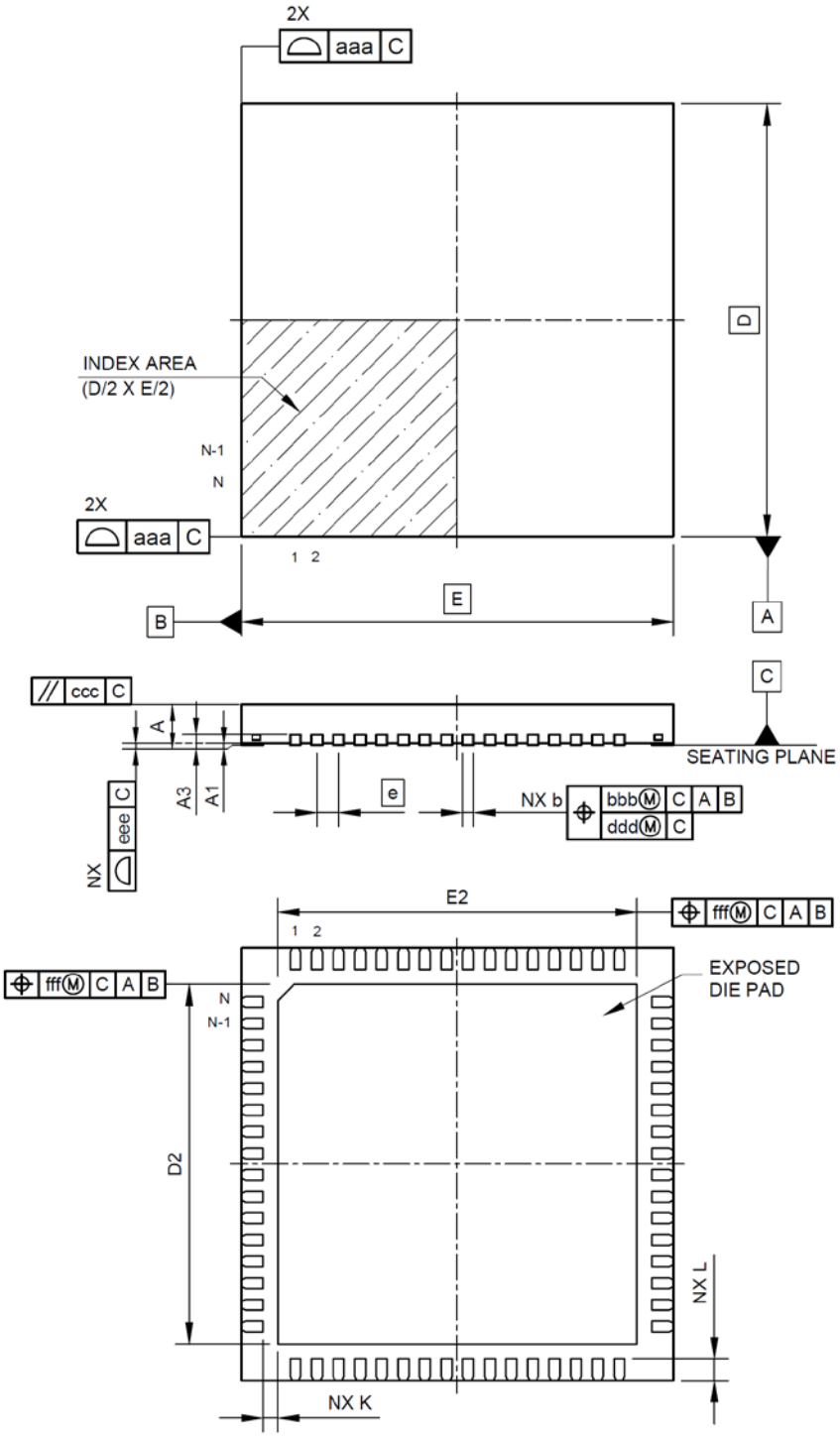
Note2: VDD output voltage is 3.310V with these resistors.

Note3: Please consider the effective capacitance. The smaller C3 causes the larger voltage drop of VCP.
The smaller C2 causes the larger voltage ripple of VCP.

Note4: Please select the suitable value of R6 and C5 depending on C4 effective capacitance.

Note5: The suitable capacitance depends on the constraints of the application and characteristic.

9 Package Specification



Symbols	Dimension in Millimeters		
	Min.	Typ.	Max.
A	-	-	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	-	8.00	-
E	-	8.00	-
e	-	0.40	-
N	64		
L	0.30	0.40	0.50
K	0.20	-	-
D2	6.40	6.50	6.75
E2	6.40	6.50	6.75
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

10 Revision History

Revision	Date	Description	Object Page
1.00	5-Oct-23	• Initial release.	• All

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.

© 2023 Renesas Electronics Corporation. All rights reserved.