

RBA190N15YANS-3UA04

REXFET-1 N-Channel [Power MOSFET](#)

150 V - 190 A - 3.9 mΩ - TOLL for Automotive

Description

The RBA190N15YANS-3UA04 N-channel power MOSFET features REXFET-1 split-gate technology and is offered in a TOLL package. The TOLL package features top-side cooling for ultra-compact and optimal thermal performance. Renesas' REXFET-1 split gate technology is suitable for applications requiring low $R_{DS(on)}$ and switching capability for high-power and high-frequency applications.

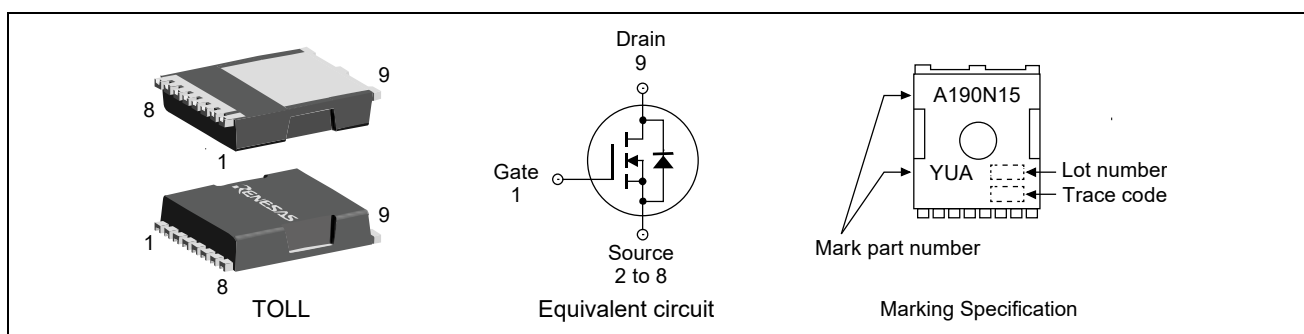
Features

- Standard level gate drive voltage: $V_{GS(th)} = 2.2$ to 3.7 V
- Super low on-state resistance: $R_{DS(on)} = 3.9$ mΩ MAX.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- AEC-Q101 qualified
- PPAP capable
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

Small Traction (2-wheel, 3-wheel vehicle), 72 to 96 V load, Onboard charger, Charging station, Low voltage DC/DC,

Outline



Absolute Maximum Ratings

($T_j = 25$ °C unless otherwise notice)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	150	V
Gate to Source Voltage	V_{GSS}	±20	V
Continuous Drain Current	$I_D(T_c = 25^\circ\text{C})$ Note 2,6	±190	A
	$I_D(T_c = 100^\circ\text{C})$ Note 2,6	±135	A
Pulsed Drain Current	$I_D(\text{pulse})$ Note 1,2,3,6	±760	A
Power Dissipation	P_D Note 1,6	319	W
Operating and Storage Temperature	T_j, T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Note 4	65	A
Single Avalanche Energy	E_{AS} Note 4	317	mJ

Thermal Resistance

Item	Symbol	Min	Typ	Max	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ ^{Note 6}	—	—	0.47	°C/W
Junction to Ambient Thermal Resistance	$R_{th(j-a)}$ ^{Note 5,6}	—	—	40	°C/W

Electrical Characteristics

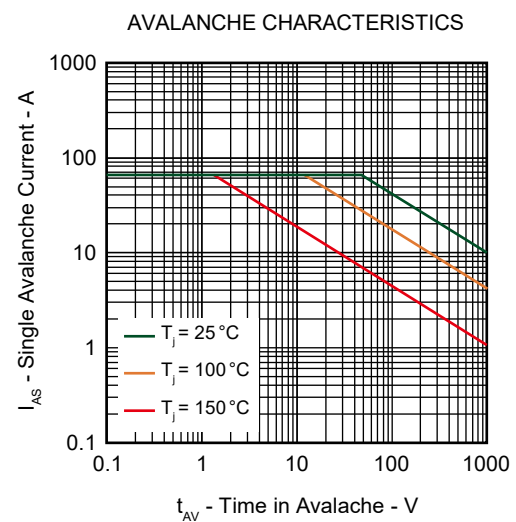
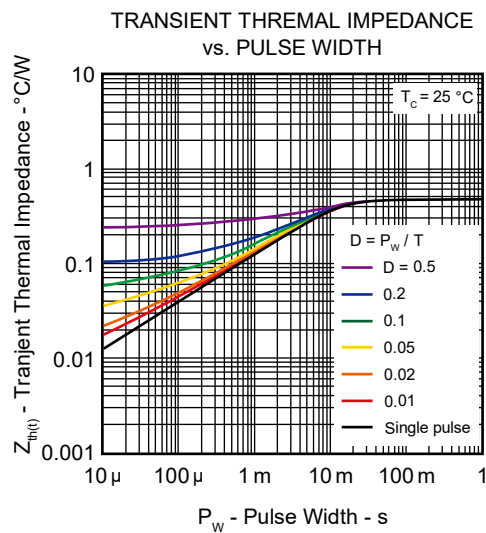
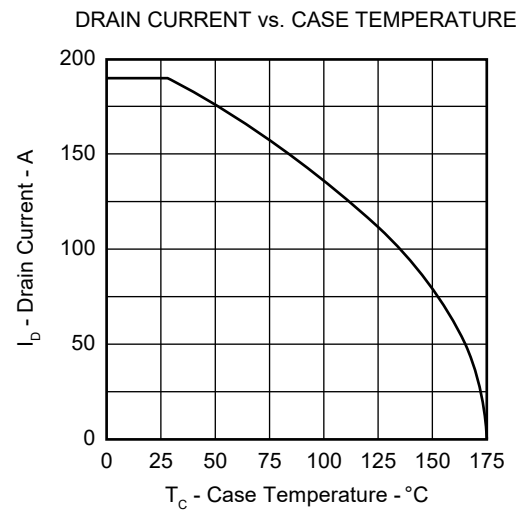
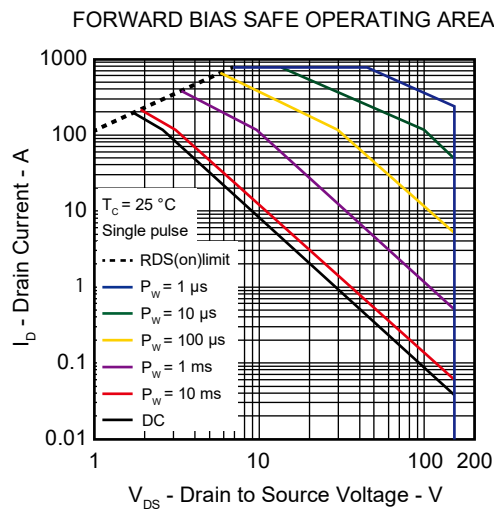
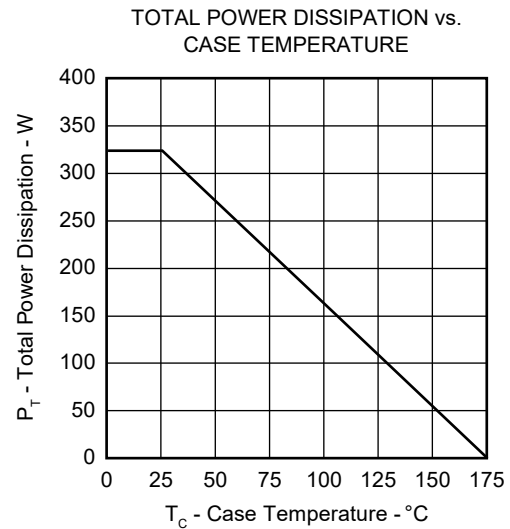
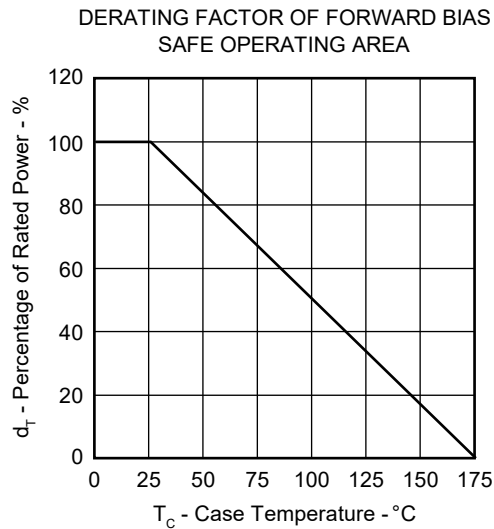
(T_j = 25 °C unless otherwise notice)

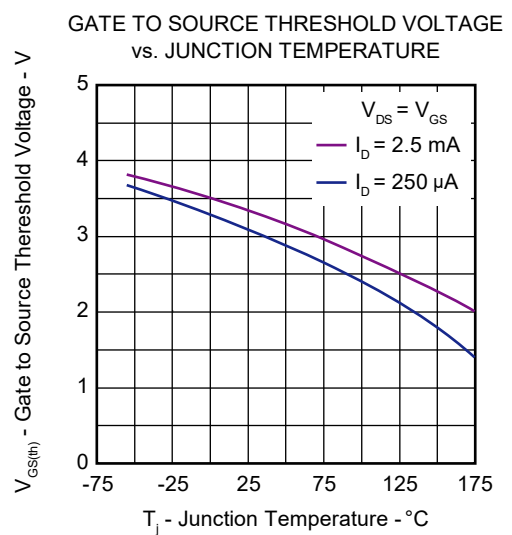
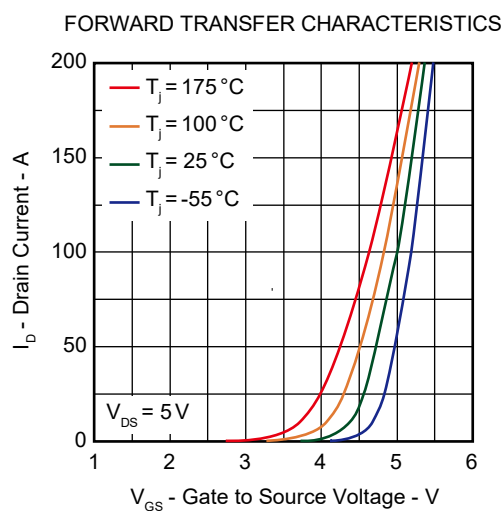
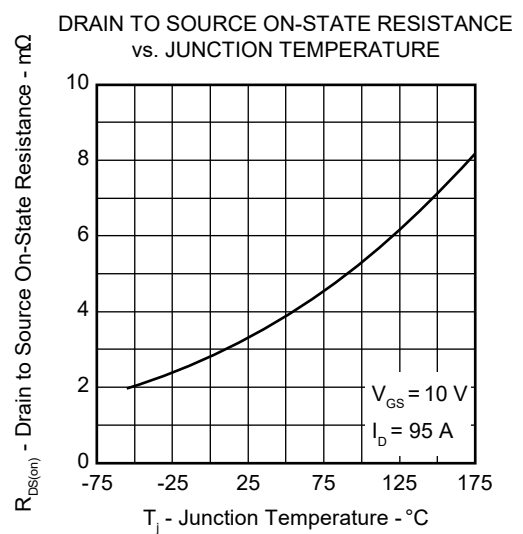
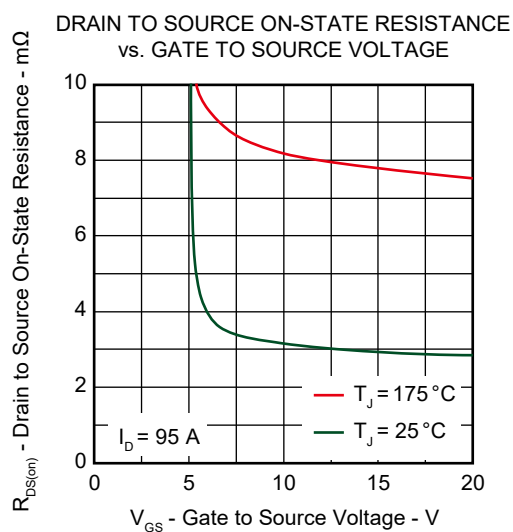
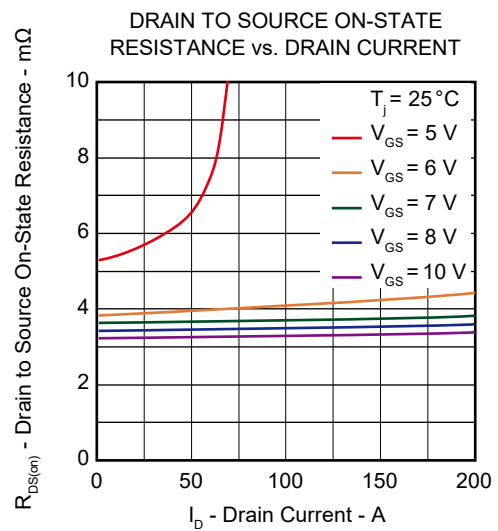
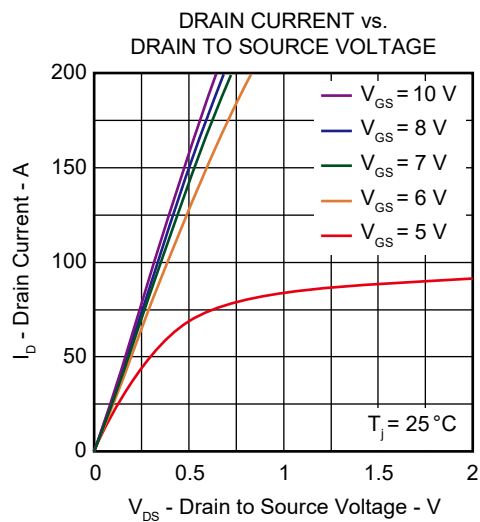
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 150 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	—	—	±100	nA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	2.2	—	3.7	V	V _{DS} = V _{GS} , I _D = 250 μA
Drain to Source On-state Resistance	R _{DS(on)}	—	3.2	3.9	mΩ	V _{GS} = 10 V, I _D = 95 A
Input Capacitance	C _{iss}	—	5500	—	pF	V _{DS} = 75 V, V _{GS} = 0 V f = 100 kHz
Output Capacitance	C _{oss}	—	1800	—	pF	
Reverse Transfer Capacitance	C _{rss}	—	33	—	pF	
Gate resistance	R _g	—	3.5	—	Ω	—
Turn-on Delay Time	t _{d(on)}	—	30	—	ns	V _{DD} = 75 V, I _D = 50 A V _{GS} = 10 V R _G = 5 Ω
Rise Time	t _r	—	15	—	ns	
Turn-off Delay Time	t _{d(off)}	—	75	—	ns	
Fall Time	t _f	—	15	—	ns	
Total Gate Charge	Q _g	—	76	—	nC	V _{DD} = 75 V, I _D = 50 A V _{GS} = 10 V
Gate to Source Charge	Q _{gs}	—	28	—	nC	
Gate to Drain Charge	Q _{gd}	—	13	—	nC	
Gate plateau voltage	V _{plateau}	—	5.0	—	V	
Output Charge	Q _{oss}	—	210	—	nC	V _{DS} = 75 V, V _{GS} = 0 V
Body Diode Forward Voltage	V _{F(S-D)}	—	0.87	1.5	V	I _F = 95 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	120	—	ns	I _F = 50 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	—	400	—	nC	dI/dt = 100 A/μs

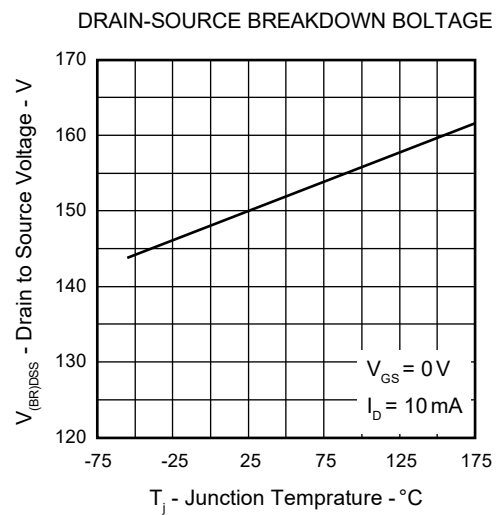
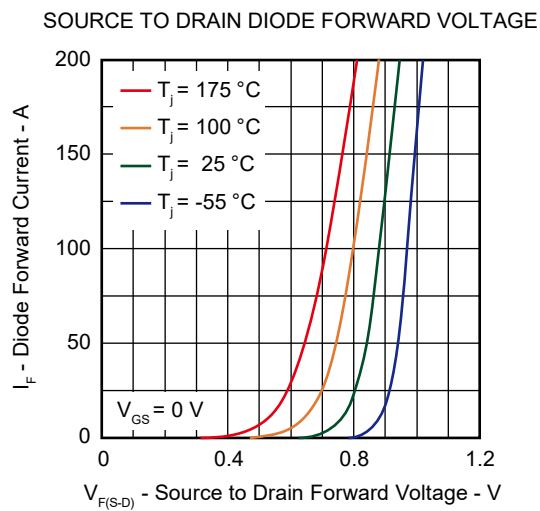
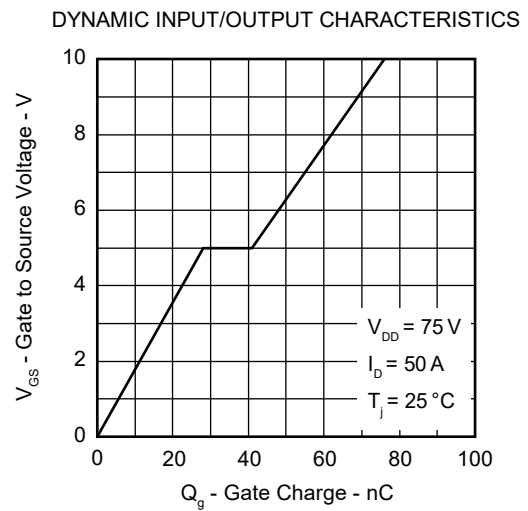
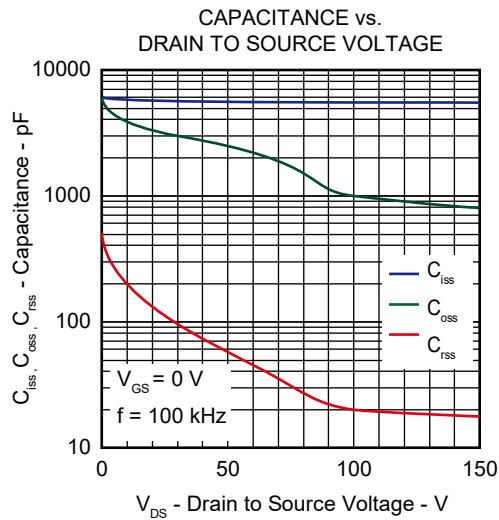
Note 1. T_c = 25 °C

2. Value is limited by overall system design including PCB.
3. PW ≤ 10 μs
4. L = 100 μH, V_{DD} = 50 V, R_G = 25 Ω
5. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)
6. Defined by design. Not subject to production test.

Typical Characteristics

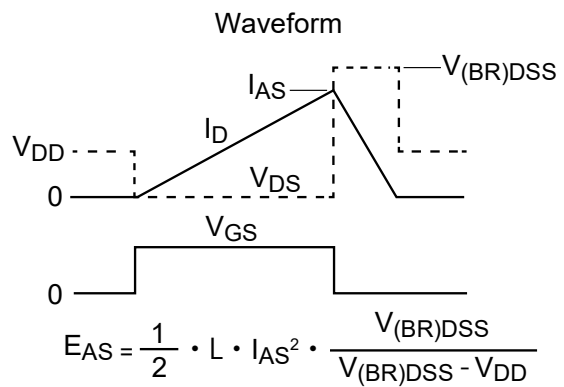
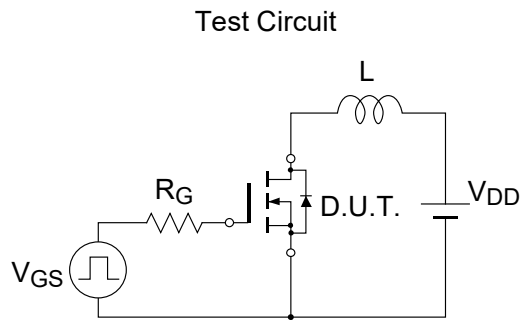




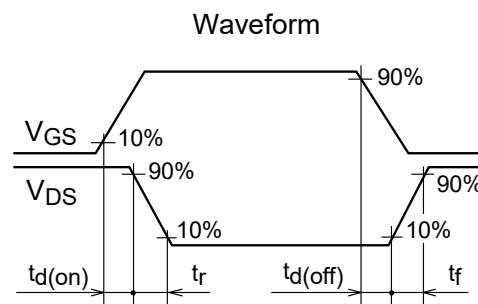
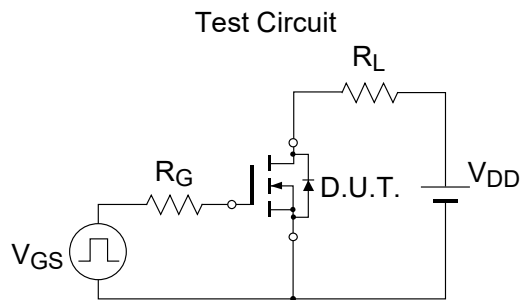


Test Circuit

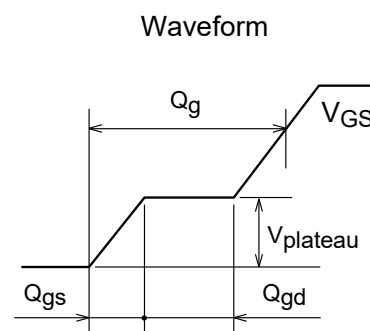
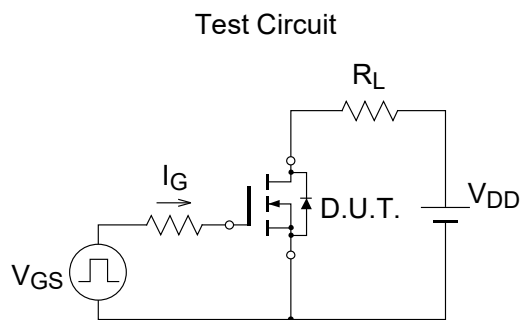
Avalanche



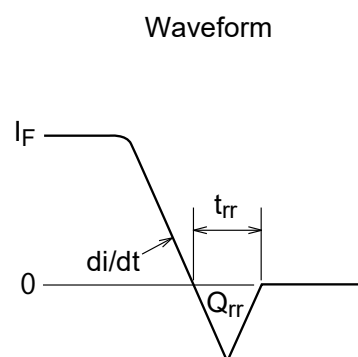
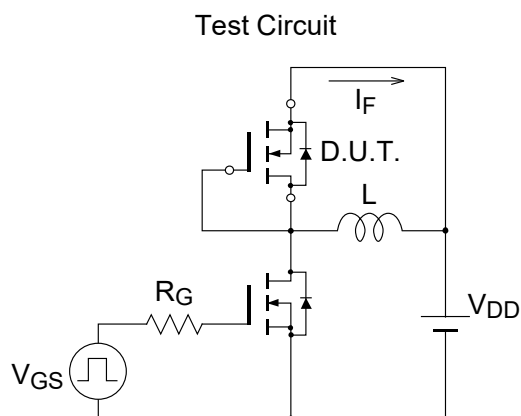
Switching Time



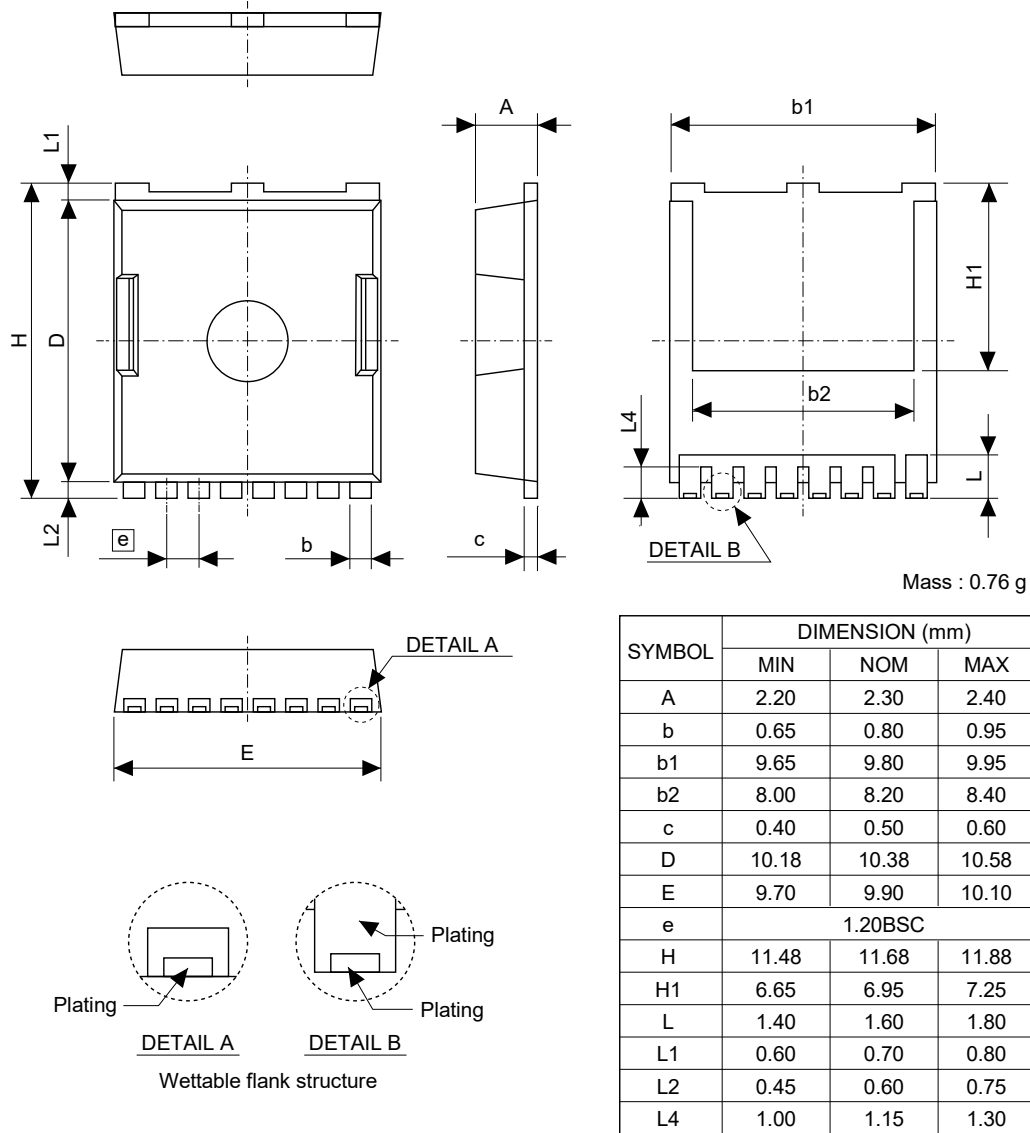
Gate Charge



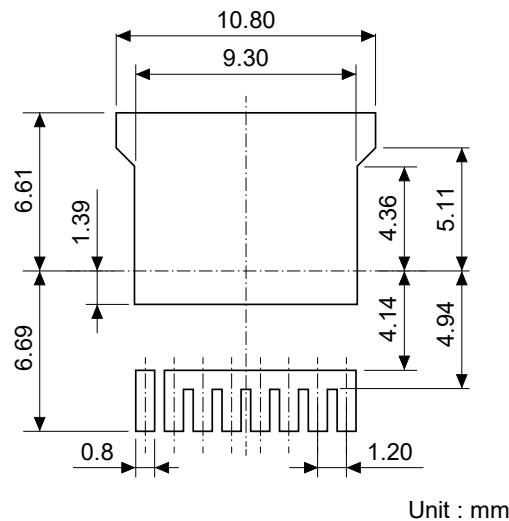
Reverse Recovery



Package Dimensions



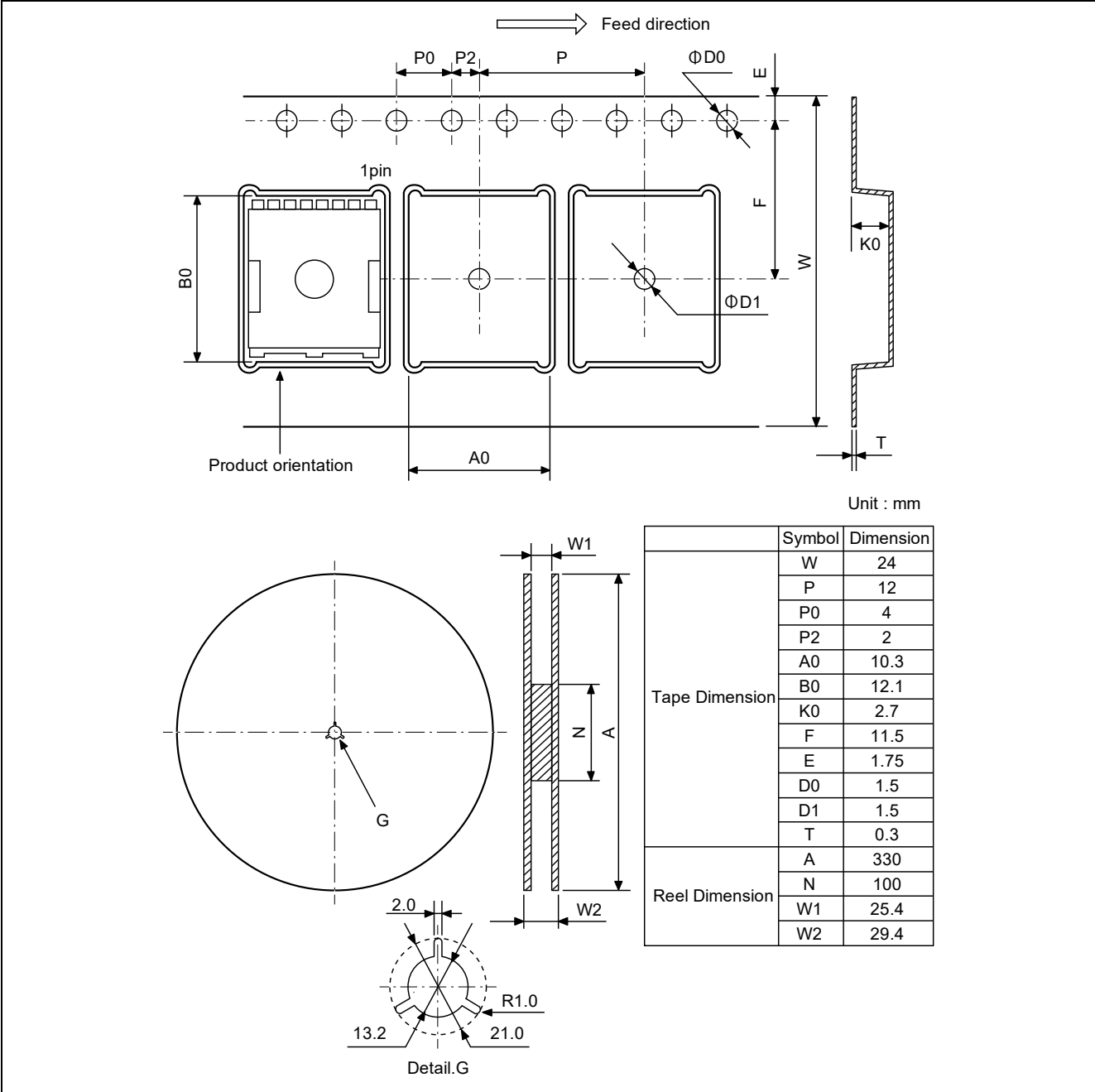
Mount pad



Ordering Information

Part No.	Packing	Quantity
RBA190N15YANS-3UA04#GB0	Taping	2000 pcs/reel

Packing Specification



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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