RBA50N04DANS-4UA06

N-Channel Power MOSFET

40V - 50A - 5.8mΩ

Description

Renesas SO8-FL technology in 5x6mm2 flat-lead package designed for supporting high current with copper clip-applied, compact & efficient designs and including optimal thermal performance. AEC-Q101 qualified MOSFET and PPAP capable suitable for automotive applications.

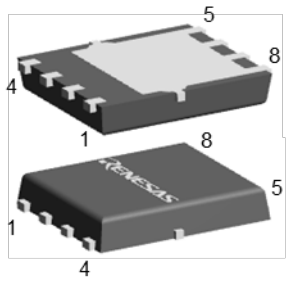
Features

- Standard level gate drive voltage: $V_{GS(th)}$ = 2.0~4.0V
- Low on-state resistance to minimize conduction losses: $R_{DS(on)}$ = 5.8mΩ Max.
- Low input capacitance to minimize driver losses
- Small footprint (5x6mm^2) with compact design
- AEC-Q101 qualified
- PPAP capable
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

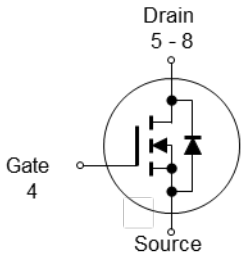
Application

- Automotive: 12V/24V load EPS, ABS, PSM, BMS, e-fuse, etc.
- Industrial: Micro inverter, DC-DC converter, Power-tool, battery powered application, etc.

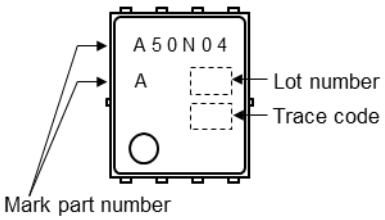
Outline



SO8-FL



Equivalent Circuit



Marking Specification

Absolute Maximum Ratings

(T_j=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	40	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$ Notes1,2,5	±50	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1,3,5	±150	A
Power Dissipation	P_D Notes1,5	47	W
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Notes4	20	A
Single Avalanche Energy	E_{AS} Notes4	40	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ Notes5	3.2	°C/W

Electrical Characteristics

(T_j=25°C unless otherwise notice.)

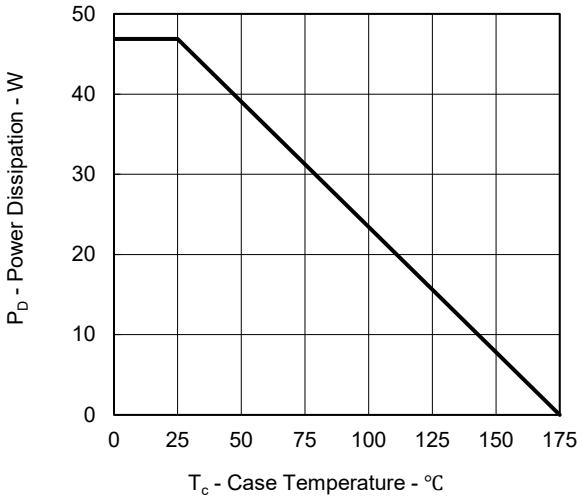
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±100	nA	V_{GS} = ± 20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Drain to Source On-state Resistance	$R_{DS(on)}$	—	4.98	5.8	mΩ	V_{GS} = 10 V, I_D = 25 A
Input Capacitance	C_{iss}	—	1200	—	pF	V_{DS} = 25 V
Output Capacitance	C_{oss}	—	150	—	pF	V_{GS} = 0 V
Reverse Transfer Capacitance	C_{rss}	—	95	—	pF	f = 1 MHz
Gate resistance	R_g	—	1.8	—	Ω	
Turn-on Delay Time	$t_{d(on)}$	—	22	—	ns	V_{DD} = 20 V, I_D = 25 A
Rise Time	t_r	—	30	—	ns	V_{GS} = 10 V
Turn-off Delay Time	$t_{d(off)}$	—	41	—	ns	R_G = 5 Ω
Fall Time	t_f	—	9	—	ns	
Total Gate Charge	Q_g	—	24	—	nC	V_{DD} = 20 V
Gate to Source Charge	Q_{gs}	—	7.2	—	nC	V_{GS} = 10 V
Gate to Drain Charge	Q_{gd}	—	6	—	nC	I_D = 25 A
Body Diode Forward Voltage	$V_{F(S-D)}$	—	0.83	1.5	V	I_F = 25 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	32	—	ns	I_F = 25 A, V_{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	25	—	nC	di/dt = 100 A/μs

Notes 1. T_c = 25°C

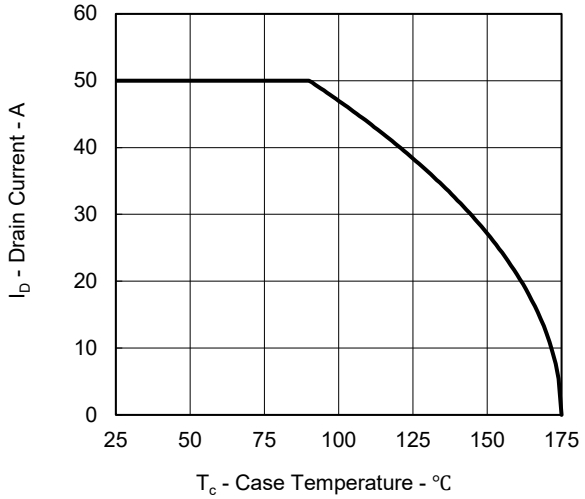
2. Value is limited by overall system design including PCB.
3. PW ≤ 10 μs , Duty Cycle ≤ 1%
4. L = 100μH , V_{DD} = 20V , V_{GS} = 20 → 0V , R_G = 25 Ω
5. Defined by design. Not subject to production test.

Typical Characteristics

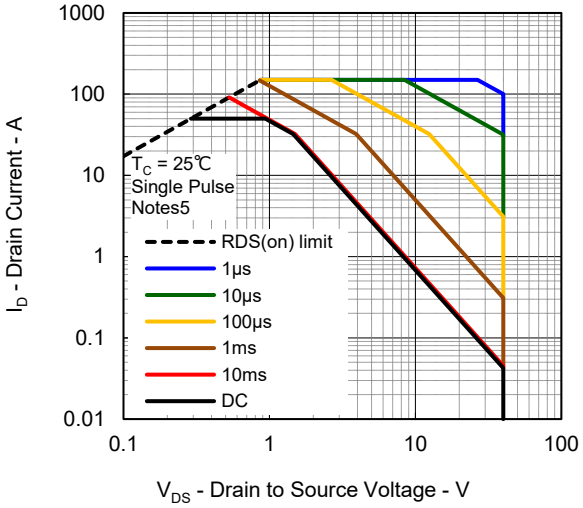
POWER DISSIPATION vs. CASE TEMPERATURE



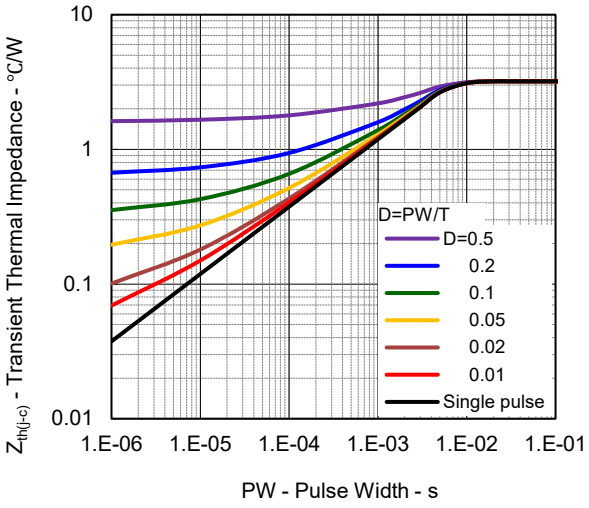
DRAIN CURRENT vs. CASE TEMPERATURE



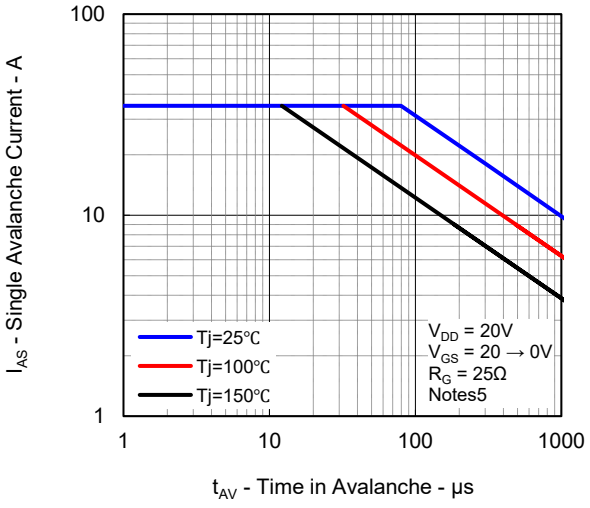
FORWARD BIAS SAFE OPERATING AREA



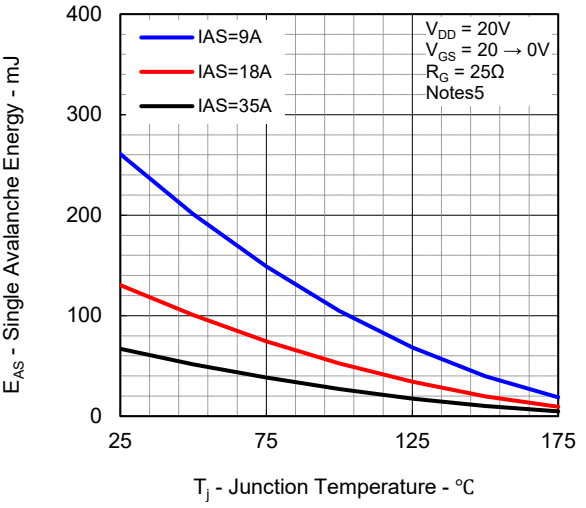
TRANSIENT THERMAL IMPEDANCE vs. PULSE WIDTH



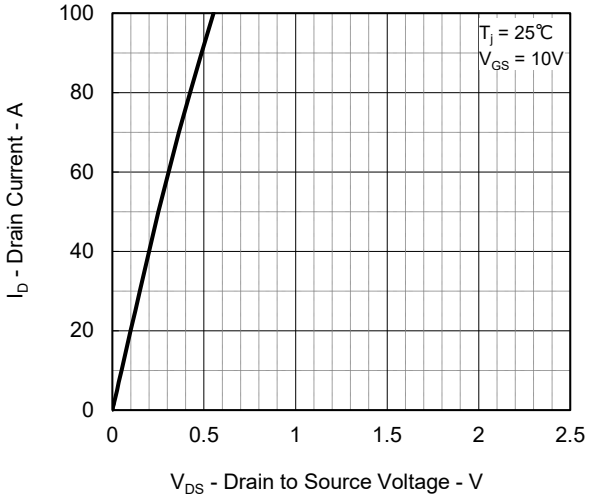
TYPICAL AVALANCHE CHARACTERISTICS



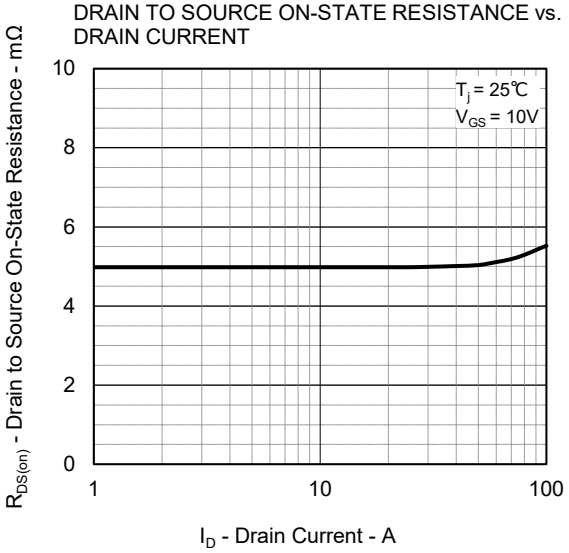
TYPICAL AVALANCHE ENERGY



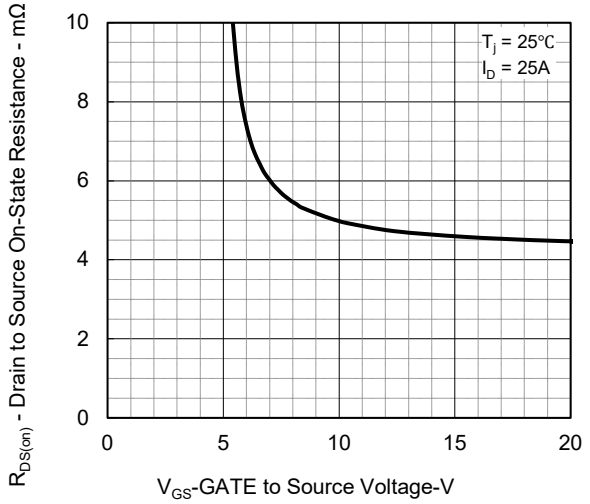
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



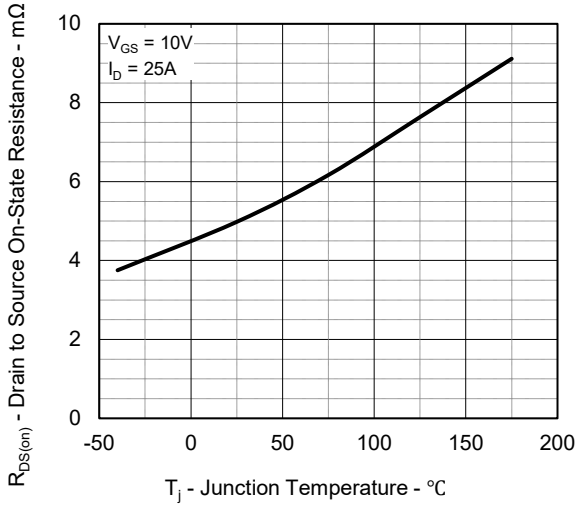
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



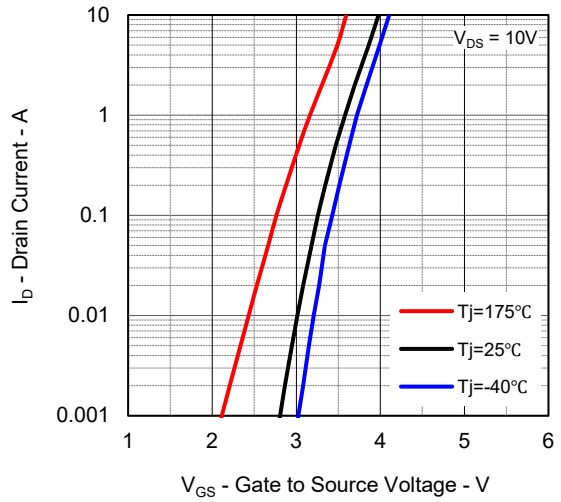
DRAIN TO SOURCE ON-STATERESISTANCE vs. GATE TO SOURCE VOLTAGE



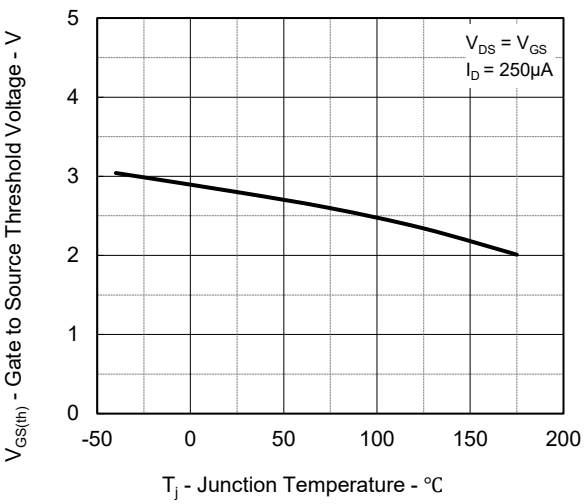
DRAIN TO SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURERE



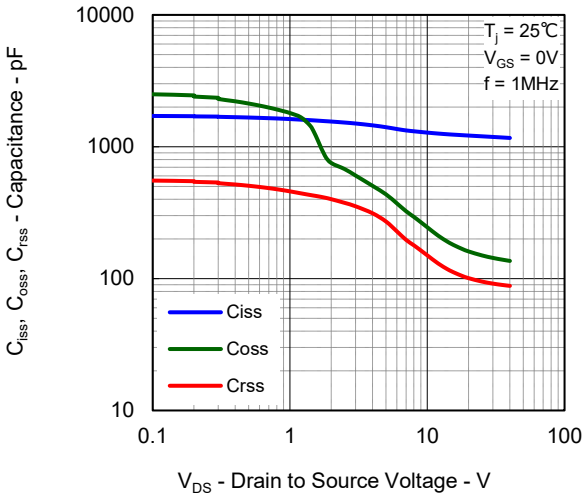
FORWARD TRANSFER CHARACTERISTICS



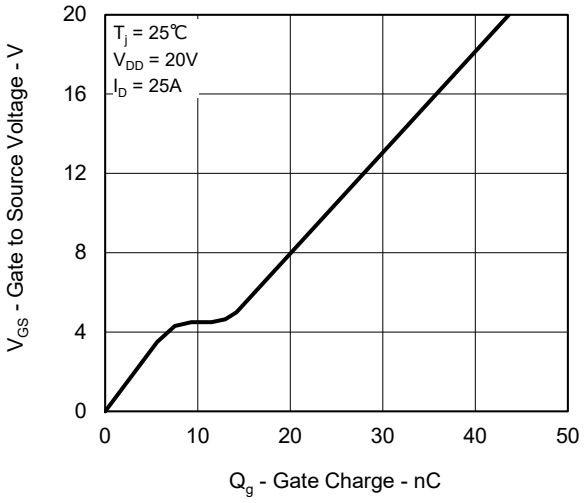
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



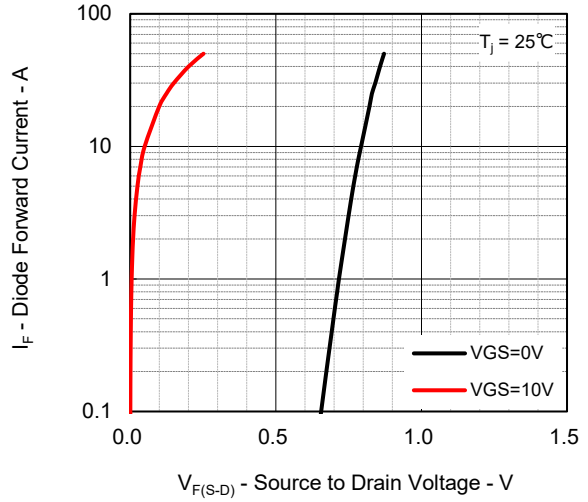
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



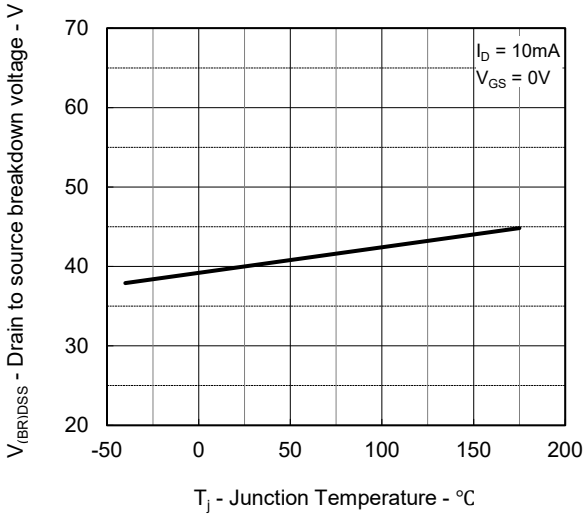
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



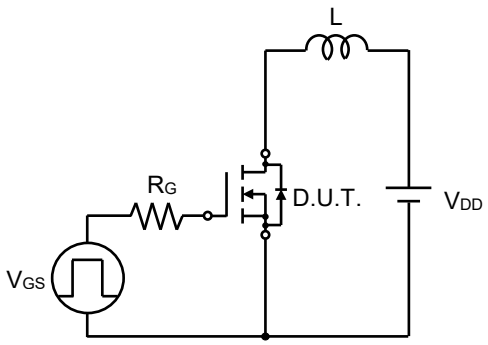
DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE



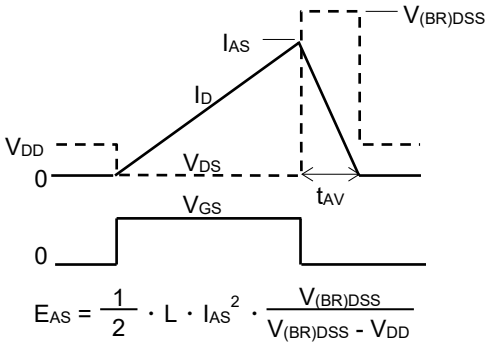
Test Circuit

Avalanche

Test Circuit



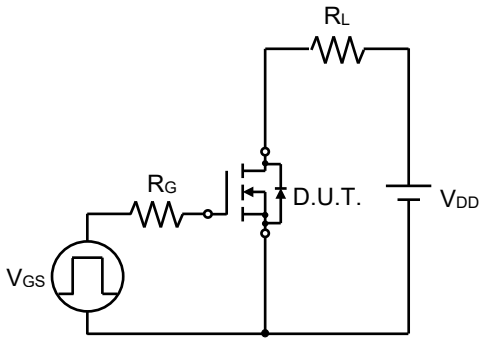
Waveform



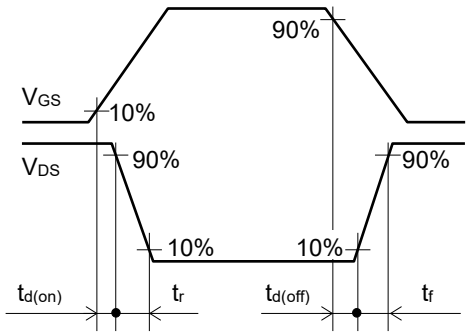
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^{2} \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

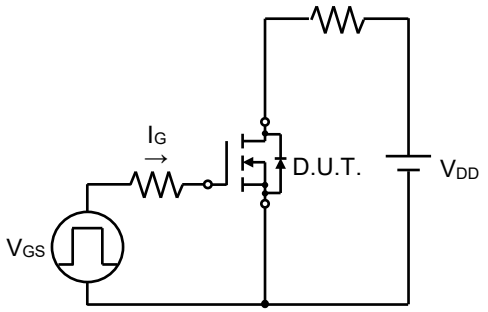


Waveform

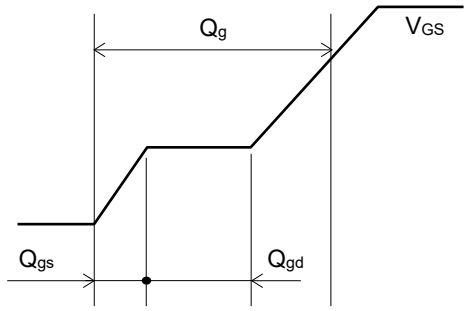


Gate Charge

Test Circuit

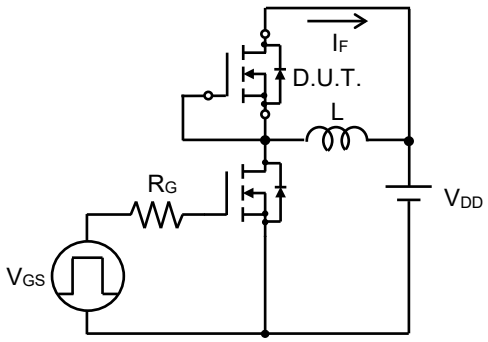


Waveform

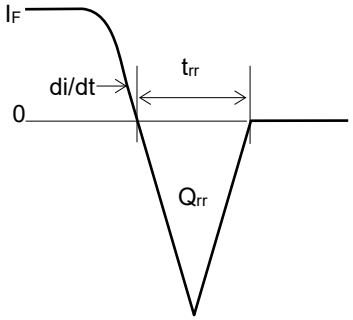


Reverse Recovery

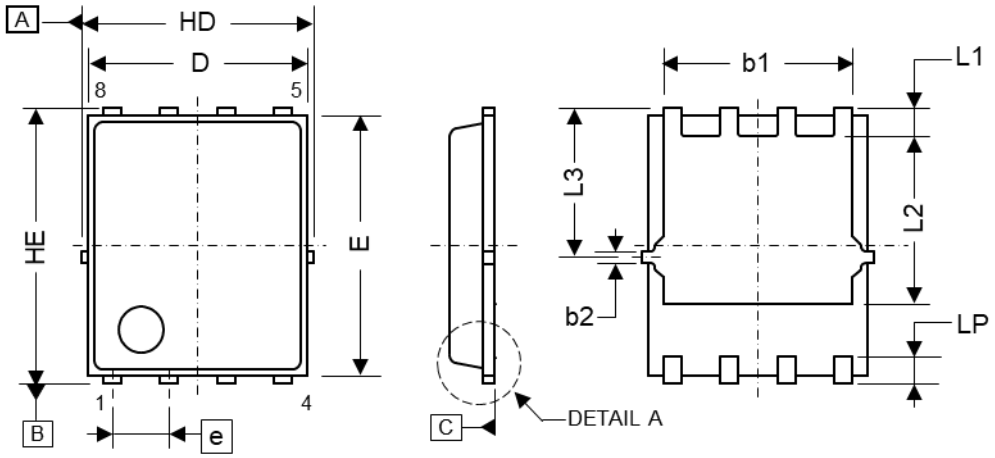
Test Circuit



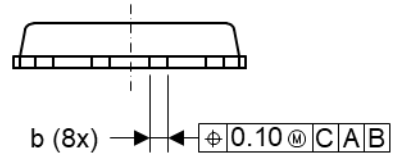
Waveform

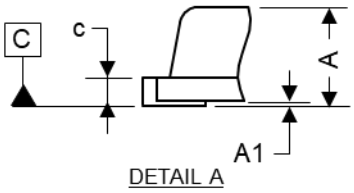


Package Dimensions



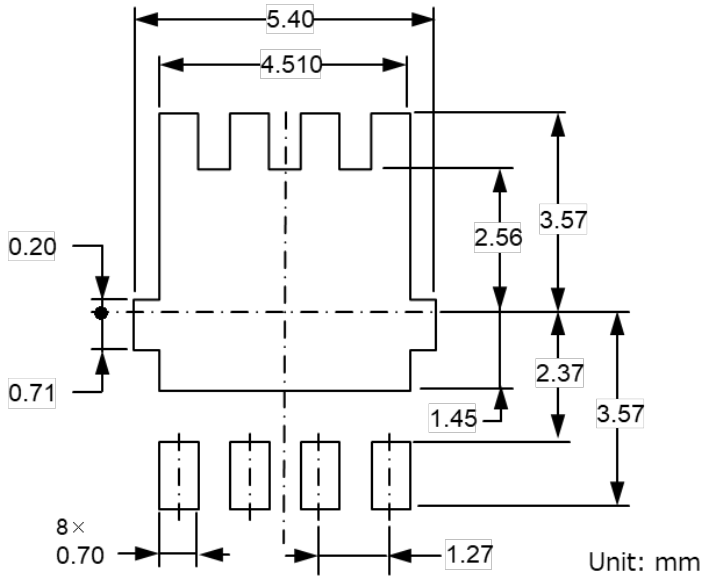
Mass : 0.1g





	DIMENSION (mm)		
SYMBOL	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	—	0.05
b	0.30	0.40	0.50
b1	4.11	4.21	4.31
b2	—	0.26	—
c	0.15	0.25	0.35
D	4.75	4.90	5.05
E	5.60	5.75	5.90
e	1.27BSC		
HD	4.95	5.15	5.35
HE	5.90	6.10	6.30
L1	0.45	0.65	0.85
L2	3.49	3.69	3.89
L3	3.10	3.30	3.50
LP	0.40	0.60	0.80

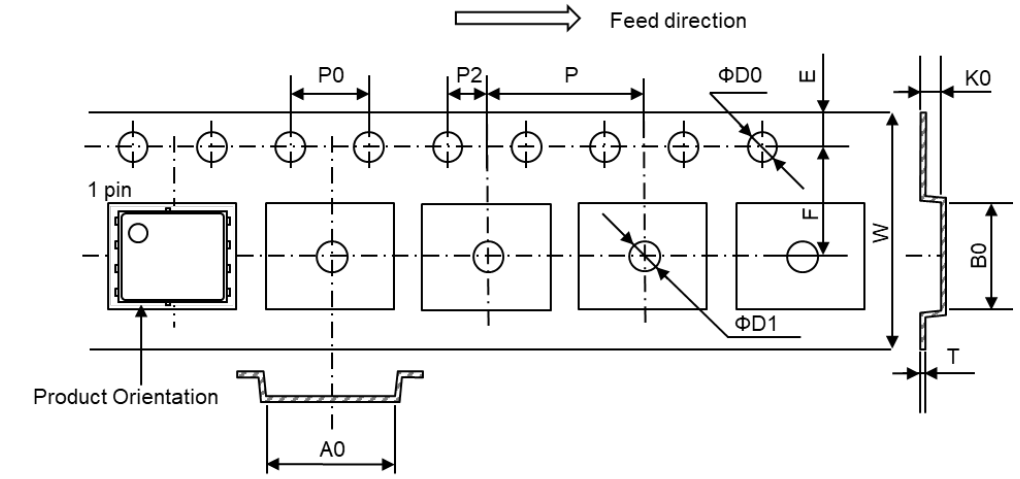
Mount pad

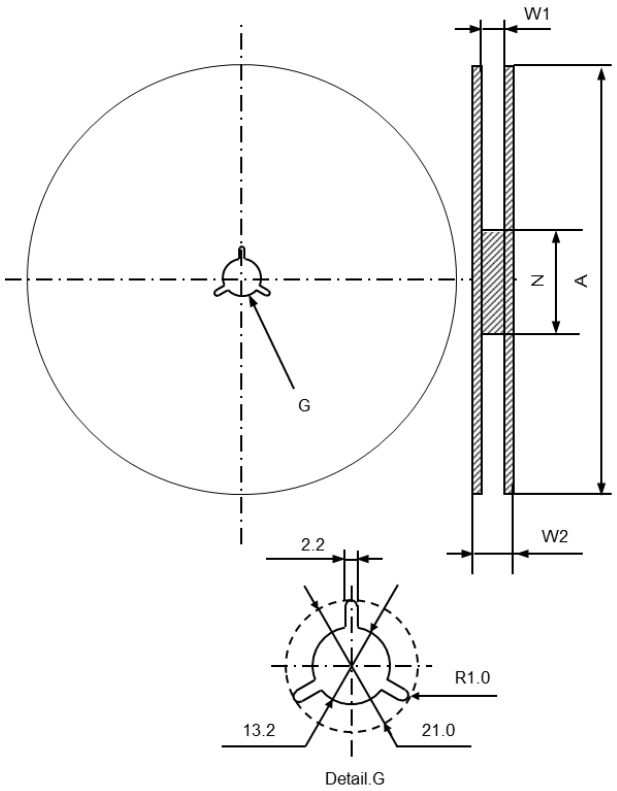


Ordering Information

Part No.	Packing	Quantity
RBA50N04DANS-4UA06#HB0	Taping	5000pcs/reel

Packing Specification





Unit : mm

	Symbol	Dimension
Tape Dimension	W	12
	P	8
	P0	4
	P2	2
	A0	6.35
	B0	5.35
	K0	1.2
	F	5.5
	E	1.75
	D0	1.5
	D1	1.5
	T	0.3
Reel Dimension	A	330
	N	100
	W1	13.5
	W2	17.4

Maximum storage	5000 pcs/Reel

Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.
Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook.

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