

# RBE011N08R1SZPW

REXFET-1 N-Channel [Power MOSFET](#)

80 V - 360 A - 1.06 mΩ - TOLT

## Description

The RBE011N08R1SZPW N-channel power MOSFET features REXFET-1 split-gate technology and is offered in a TOLT package. The TOLT package features top-side cooling for ultra-compact and optimal thermal performance. Renesas' REXFET-1 split gate technology is suitable for applications requiring low  $R_{DS(on)}$  and switching capability for high-power and high-frequency applications.

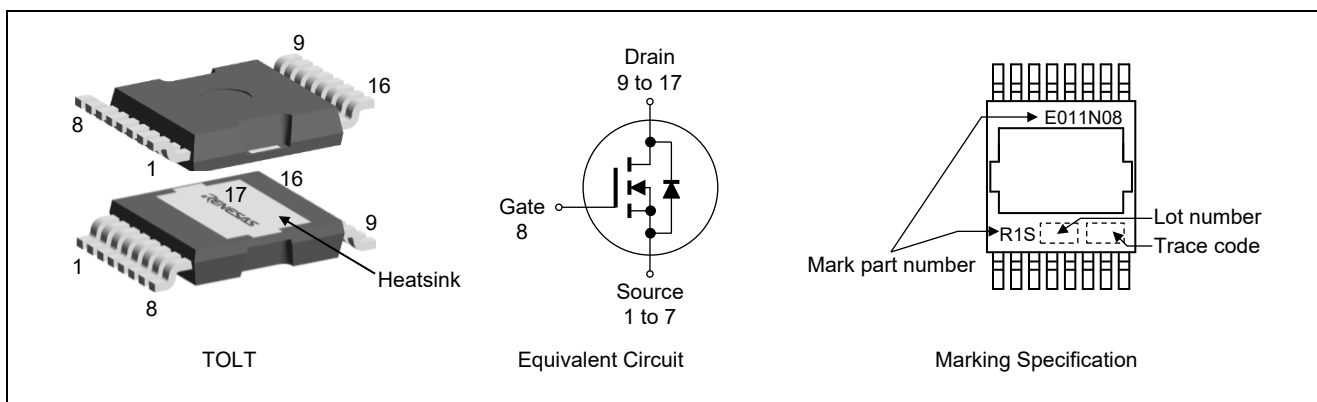
## Features

- Standard level gate drive voltage:  $V_{GS(th)} = 2.0$  to  $4.0$  V
- Super low on-state resistance:  $R_{DS(on)} = 1.06$  mΩ Max.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

## Application

Motor Control, Energy Infrastructure, Industrial Automation, DC-DC Power Conversion, Power Tools, Robotics

## Outline



## Absolute Maximum Ratings

( $T_j = 25$  °C unless otherwise notice.)

| Item                           | Symbol                                | Ratings    | Unit |
|--------------------------------|---------------------------------------|------------|------|
| Drain to Source Voltage        | $V_{DSS}$                             | 80         | V    |
| Gate to Source Voltage         | $V_{GSS}$                             | ±20        | V    |
| Drain Current (DC)             | $I_D(DC)$ $T_c=25^{\circ}C$ Note 2,6  | ±360       | A    |
|                                | $I_D(DC)$ $T_c=100^{\circ}C$ Note 2,6 | ±350       | A    |
| Drain Current (pulse)          | $I_D(pulse)$ Note 1,3,6               | ±1440      | A    |
| Power Dissipation              | $P_D$ Note 1,6                        | 535        | W    |
| Operating Junction Temperature | $T_j$                                 | -55 to 175 | °C   |
| Storage Temperature            | $T_{stg}$                             | -55 to 175 | °C   |
| Single Avalanche Current       | $I_{AS}$ Note 4                       | 85         | A    |
| Single Avalanche Energy        | $E_{AS}$ Note 4                       | 722        | mJ   |

## Thermal Resistance

| Item                                   | Symbol                            | Max. | Unit |
|----------------------------------------|-----------------------------------|------|------|
| Junction to Case Thermal Resistance    | $R_{th(j-c)}$ <sup>Note 6</sup>   | 0.28 | °C/W |
| Junction to Ambient Thermal Resistance | $R_{th(j-a)}$ <sup>Note 5,6</sup> | 40   | °C/W |

## Electrical Characteristics

(T<sub>j</sub> = 25 °C unless otherwise notice.)

| Item                                | Symbol               | Min | Typ   | Max  | Unit | Test Conditions                                             |
|-------------------------------------|----------------------|-----|-------|------|------|-------------------------------------------------------------|
| Zero Gate Voltage Drain Current     | $I_{DSS}$            | —   | —     | 10   | μA   | V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V               |
| Gate Leakage Current                | $I_{GSS}$            | —   | —     | ±100 | nA   | V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> = 0 V             |
| Gate to Source Threshold Voltage    | V <sub>GS(th)</sub>  | 2.0 | —     | 4.0  | V    | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA |
| Drain to Source On-state Resistance | R <sub>DS(on)</sub>  | —   | 0.95  | 1.06 | mΩ   | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 100 A              |
| Input Capacitance                   | C <sub>iss</sub>     | —   | 18000 | —    | pF   | V <sub>DS</sub> = 40 V                                      |
| Output Capacitance                  | C <sub>oss</sub>     | —   | 2800  | —    | pF   | V <sub>GS</sub> = 0 V                                       |
| Reverse Transfer Capacitance        | C <sub>rss</sub>     | —   | 90    | —    | pF   | f = 100 kHz                                                 |
| Gate resistance                     | R <sub>g</sub>       | —   | 1.8   | —    | Ω    | —                                                           |
| Turn-on Delay Time                  | t <sub>d(on)</sub>   | —   | 90    | —    | ns   | V <sub>DD</sub> = 40 V                                      |
| Rise Time                           | t <sub>r</sub>       | —   | 55    | —    | ns   | I <sub>D</sub> = 100 A                                      |
| Turn-off Delay Time                 | t <sub>d(off)</sub>  | —   | 170   | —    | ns   | V <sub>GS</sub> = 10 V                                      |
| Fall Time                           | t <sub>f</sub>       | —   | 70    | —    | ns   | R <sub>G</sub> = 5 Ω                                        |
| Total Gate Charge                   | Q <sub>g</sub>       | —   | 250   | —    | nC   | V <sub>DD</sub> = 40 V                                      |
| Gate to Source Charge               | Q <sub>gs</sub>      | —   | 100   | —    | nC   | V <sub>GS</sub> = 10 V                                      |
| Gate to Drain Charge                | Q <sub>gd</sub>      | —   | 43    | —    | nC   | I <sub>D</sub> = 100 A                                      |
| Gate plateau voltage                | V <sub>plateau</sub> | —   | 5.3   | —    | V    |                                                             |
| Output Charge                       | Q <sub>oss</sub>     | —   | 240   | —    | nC   | V <sub>DD</sub> = 40 V, V <sub>GS</sub> = 0 V               |
| Body Diode Forward Voltage          | V <sub>F(S-D)</sub>  | —   | 0.83  | 1.5  | V    | I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V               |
| Reverse Recovery Time               | t <sub>rr</sub>      | —   | 110   | —    | ns   | I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V               |
| Reverse Recovery Charge             | Q <sub>rr</sub>      | —   | 340   | —    | nC   | di/dt = 100 A/μs                                            |

Note 1. T<sub>c</sub> = 25 °C

2. Value is limited by overall system design including PCB.

3. PW ≤ 100 μs

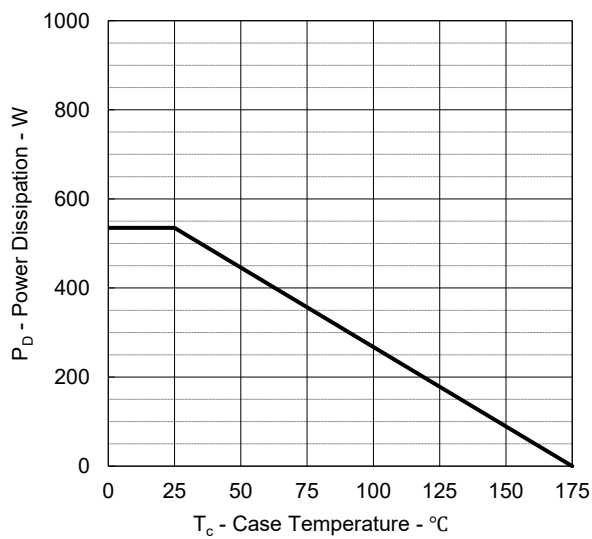
4. L = 100 μH, V<sub>DD</sub> = 40 V, R<sub>G</sub> = 25 Ω

5. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)

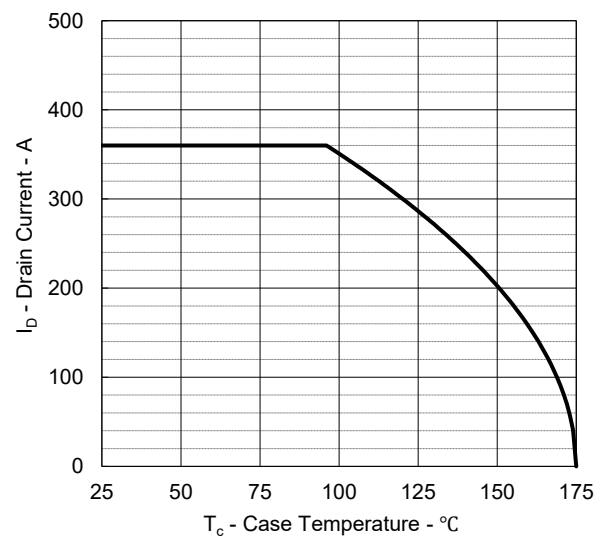
6. Defined by design. Not subject to production test.

## Typical Characteristics

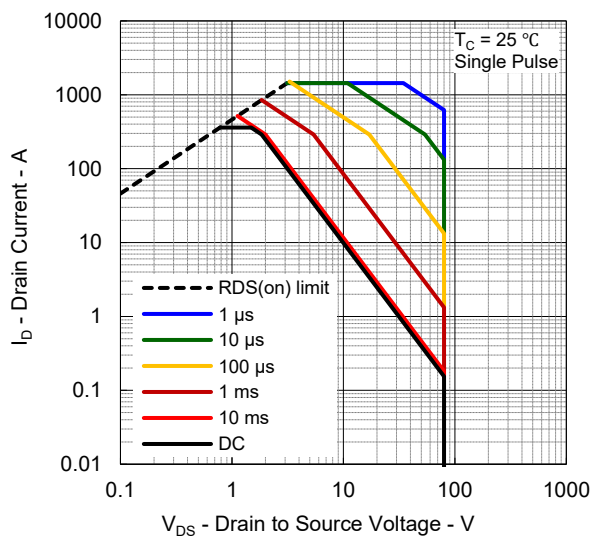
POWER DISSIPATION vs. CASE TEMPERATURE



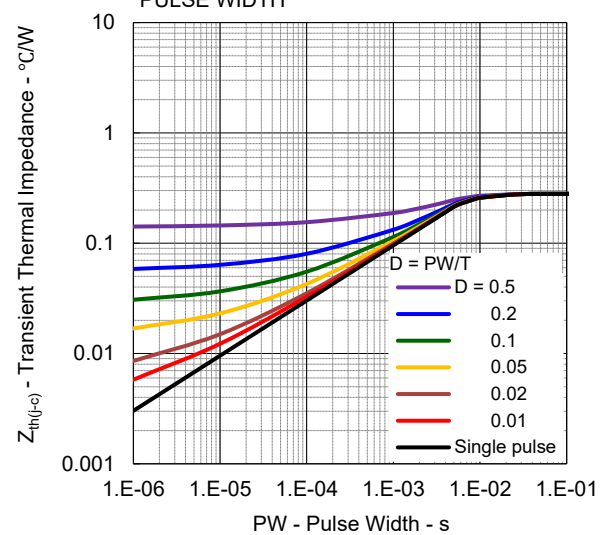
DRAIN CURRENT vs. CASE TEMPERATURE



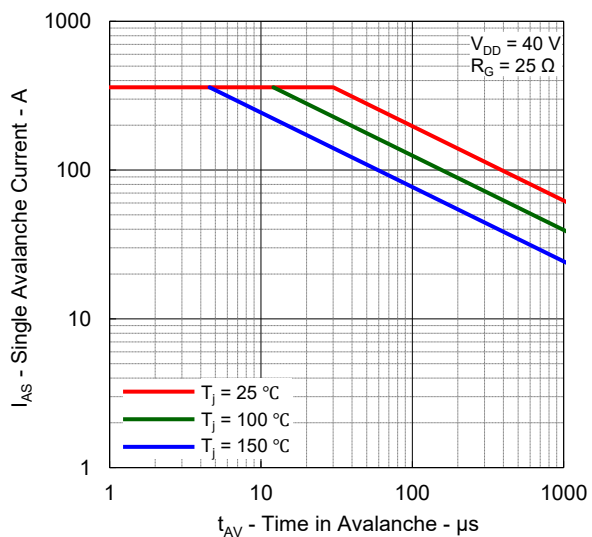
FORWARD BIAS SAFE OPERATING AREA



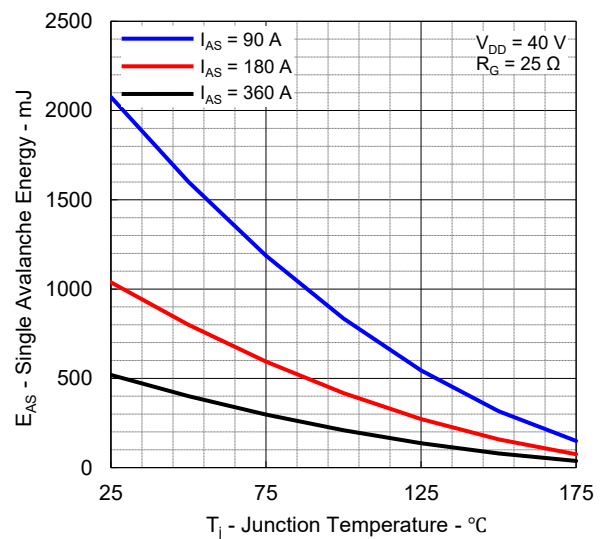
TRANSIENT THERMAL IMPEDANCE vs. PULSE WIDTH



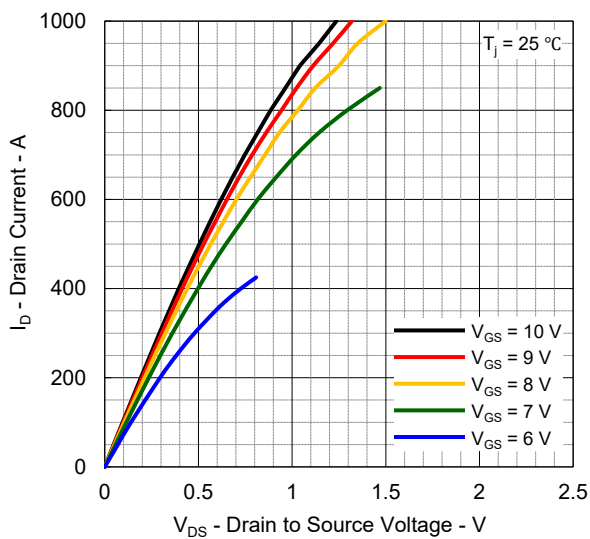
TYPICAL AVALANCHE CHARACTERISTICS



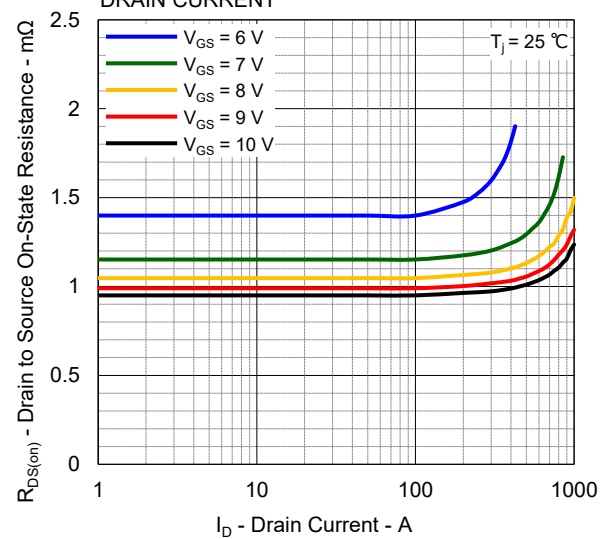
TYPICAL AVALANCHE ENERGY



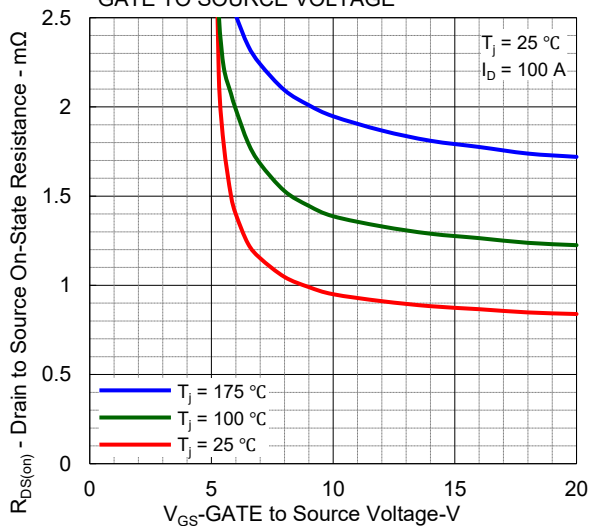
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



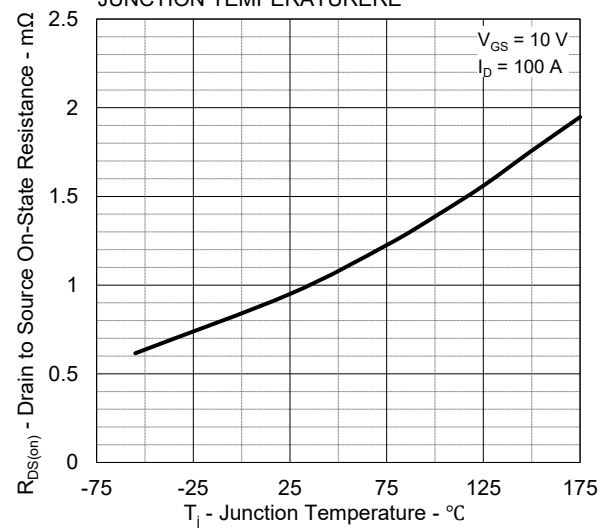
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



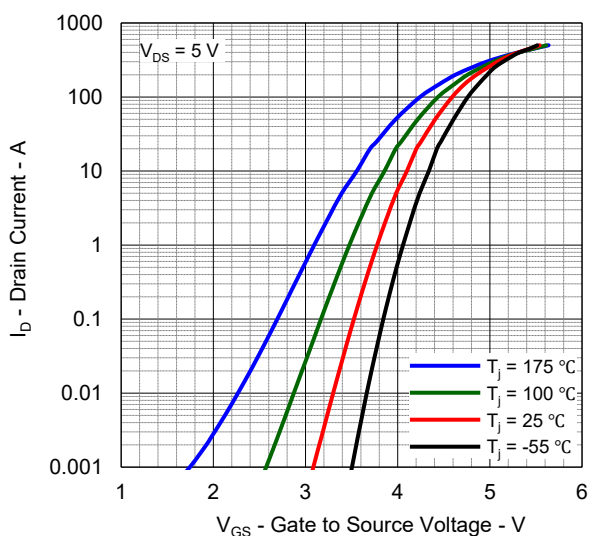
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



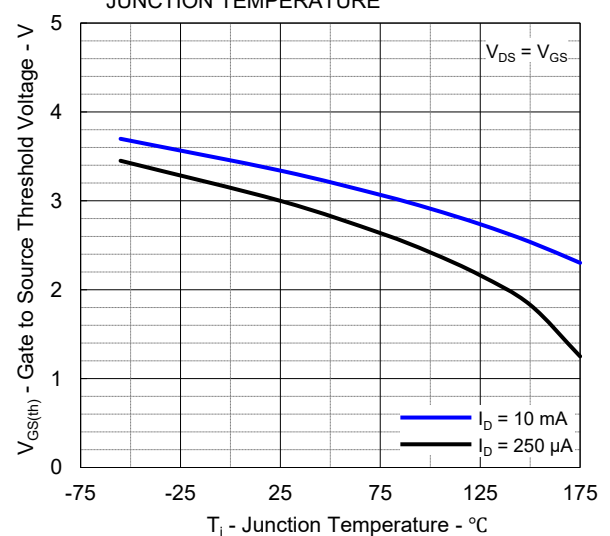
DRAIN TO SOURCE ON-STATE RESISTANCE vs. JUNCTION TEMPERATURE



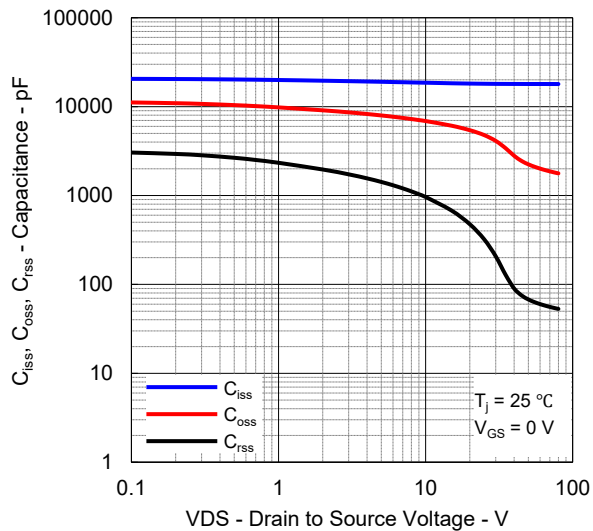
FORWARD TRANSFER CHARACTERISTICS



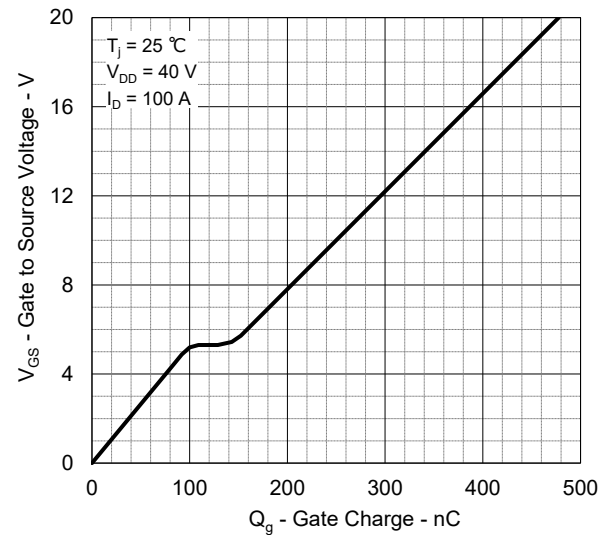
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



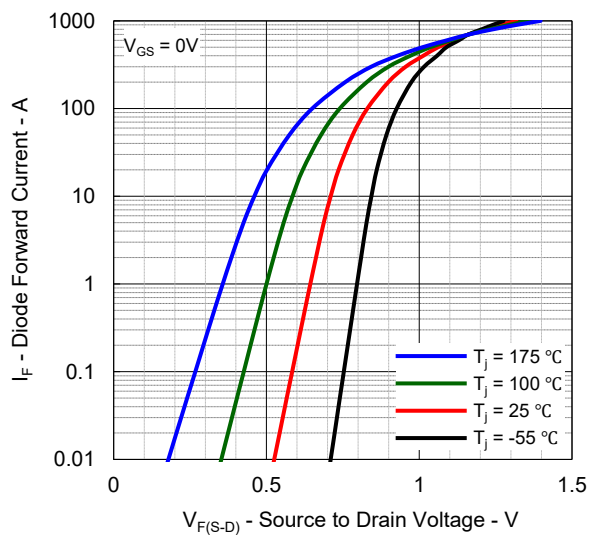
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



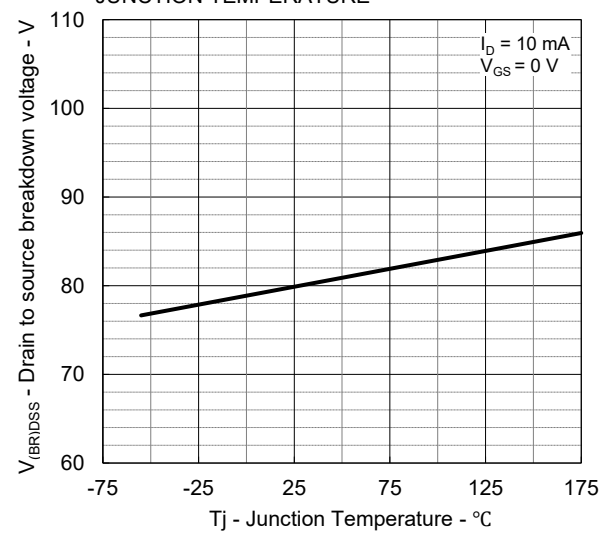
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

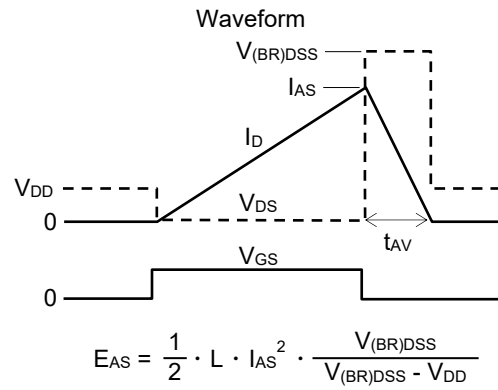
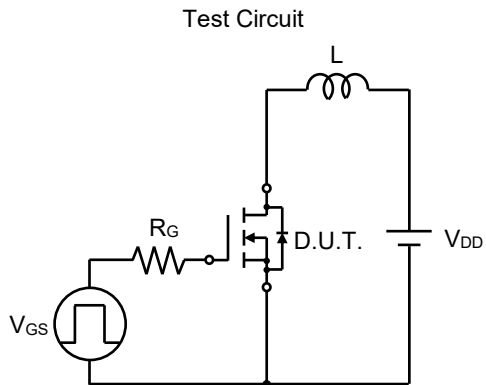


DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE

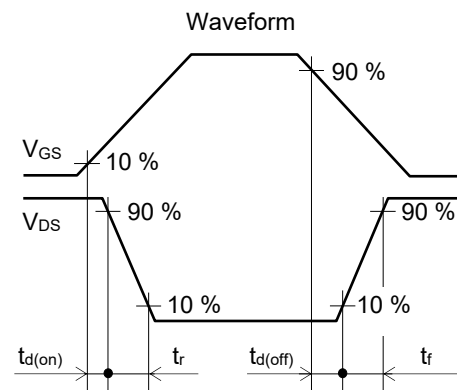
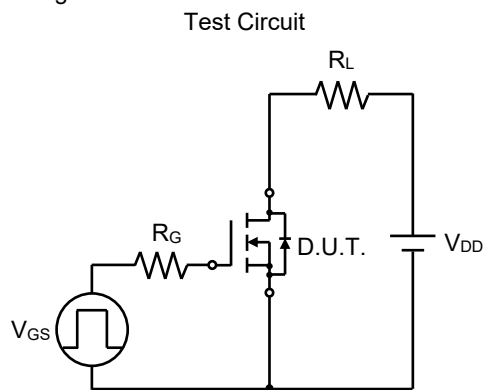


## Test Circuit

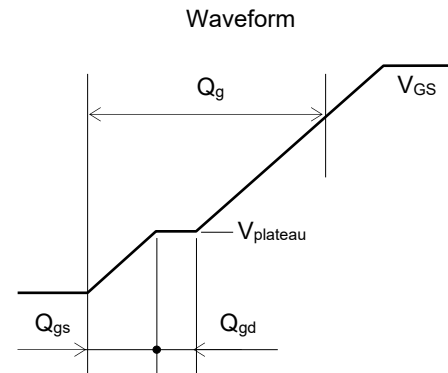
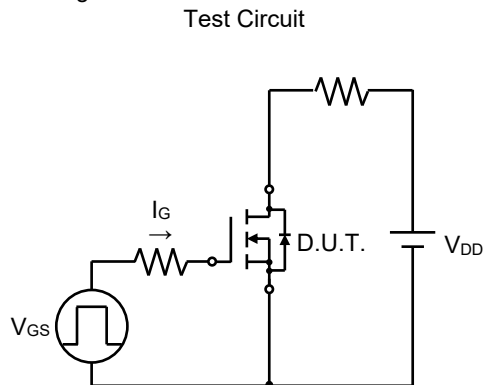
### Avalanche



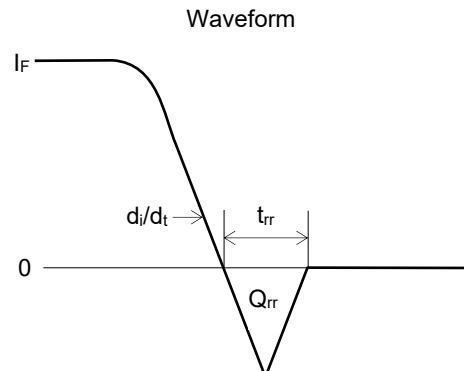
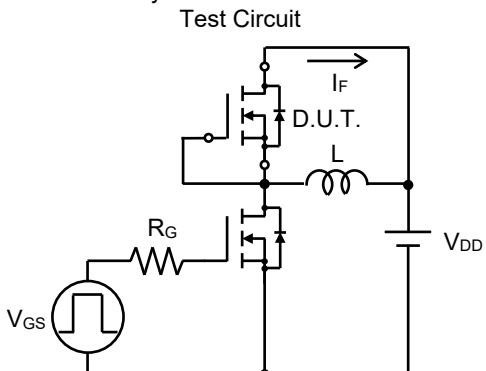
### Switching Time



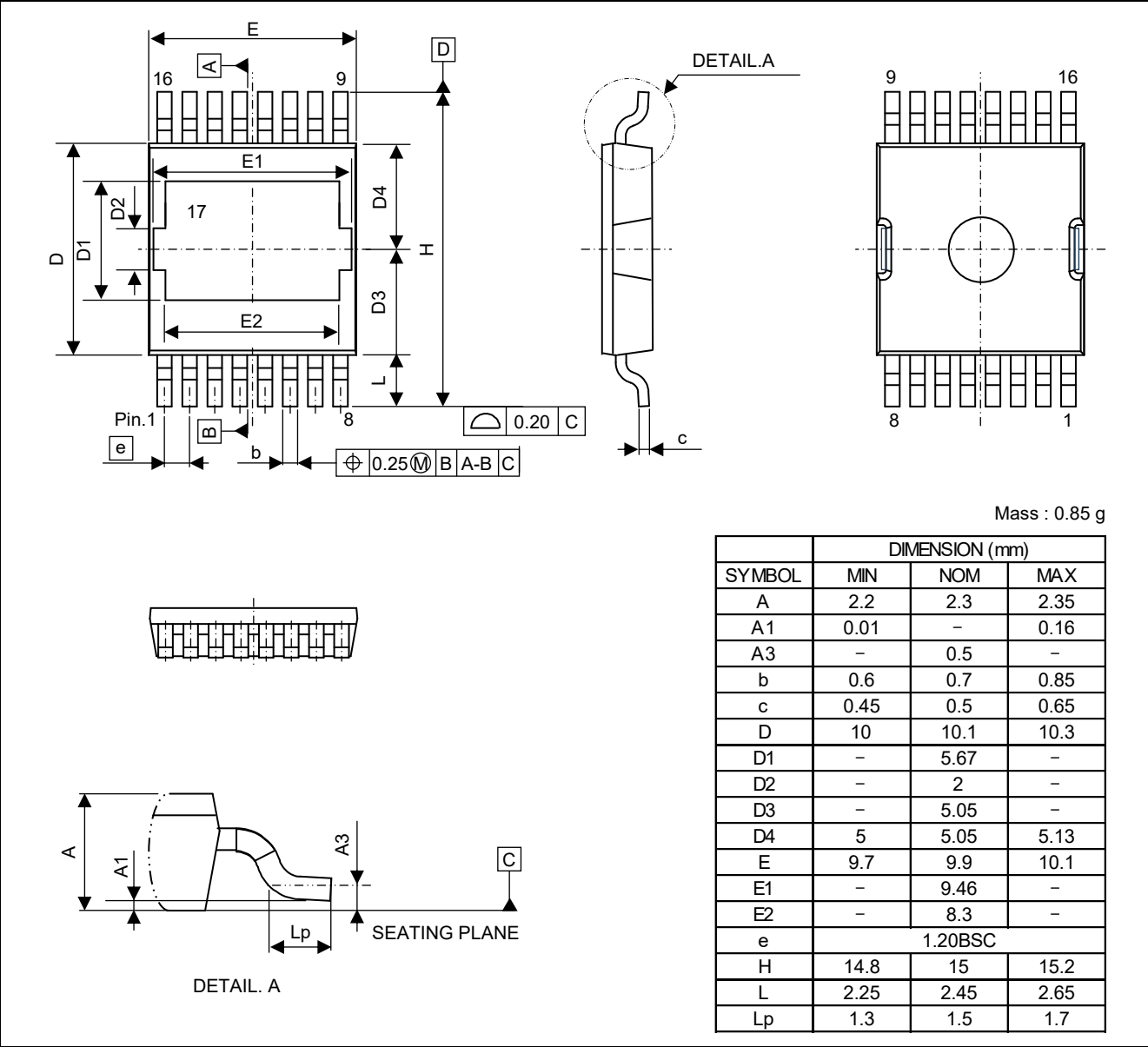
### Gate Charge



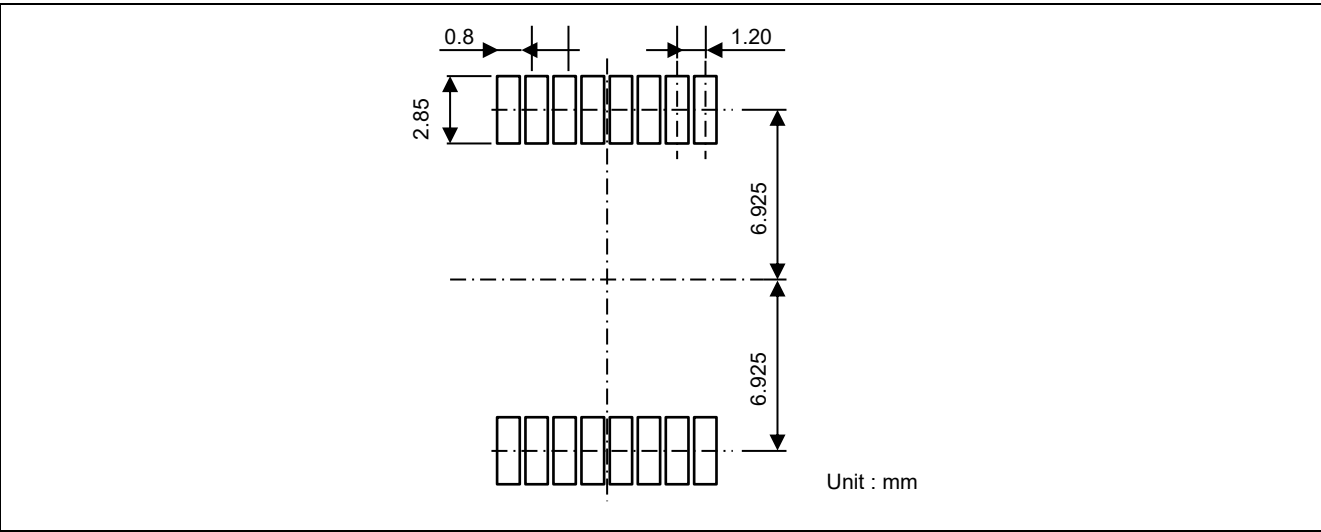
### Reverse Recovery



Package Dimensions



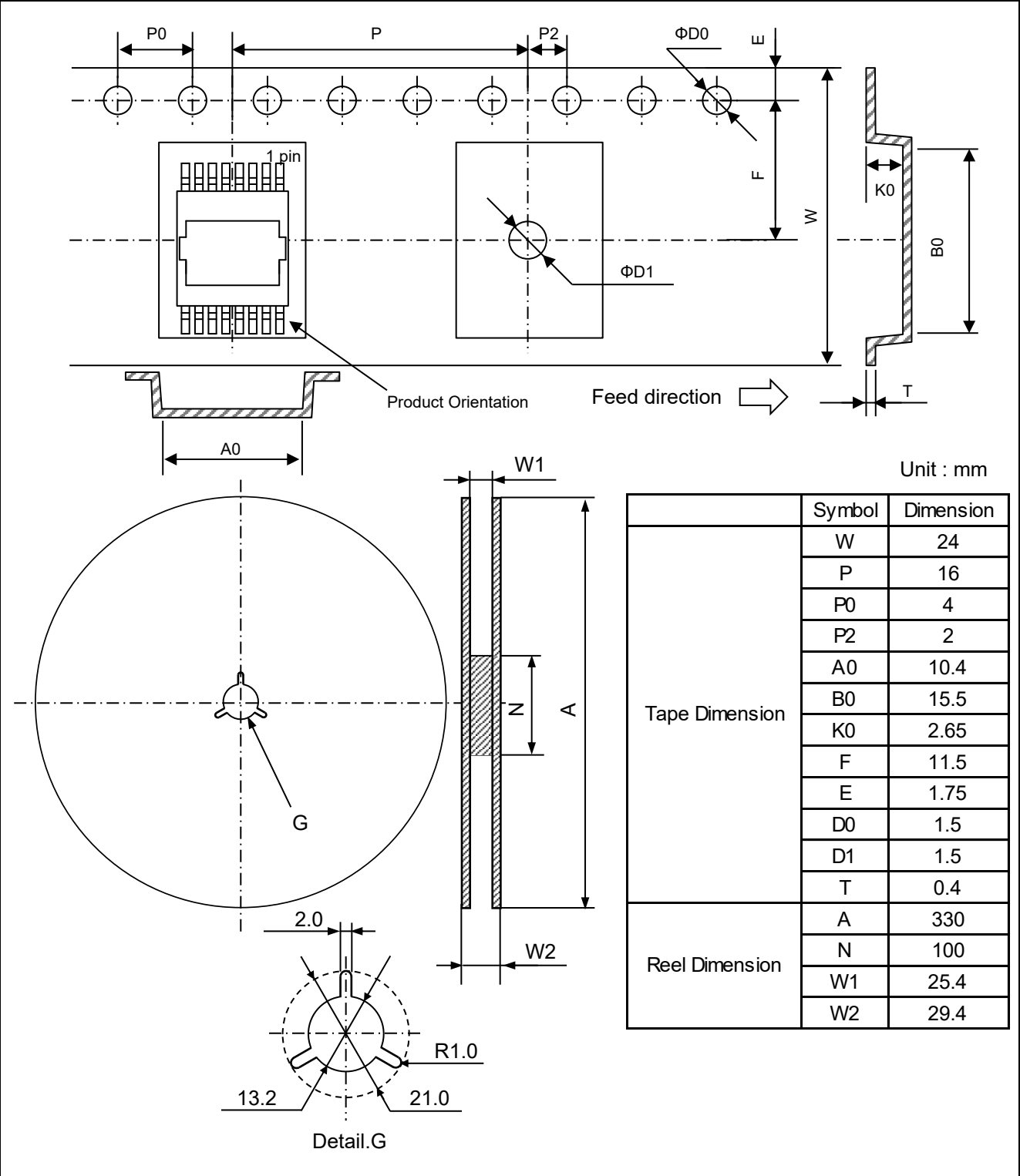
Mount pad



Ordering Information

| Part No.            | Packing | Quantity     |
|---------------------|---------|--------------|
| RBE011N08R1SZPW#KB0 | Taping  | 1300pcs/reel |

Packing Specification



Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



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