RBE015N10R1SZPW

REXFET-1 N-Channel Power MOSFET

100 V - 340 A - 1.5 mΩ - TOLT

Description

The RBE015N10R1SZPW N-channel power MOSFET features REXFET-1 split-gate technology and is offered in a TOLT package. The TOLT package features top-side cooling for ultra-compact and optimal thermal performance. Renesas' REXFET-1 split gate technology is suitable for applications requiring low RDS(on) and switching capability for high-power and high-frequency applications.

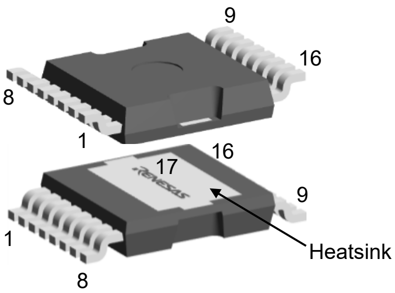
Features

- Standard level gate drive voltage: $V_{GS(th)}$ = 2.0 to 4.0 V
- Super low on-state resistance: $R_{DS(on)}$ = 1.5 mΩ Max.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

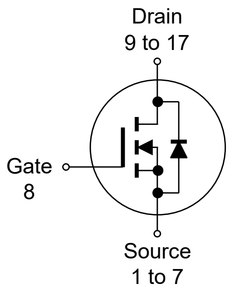
Application

Motor Control, Energy Infrastructure, Industrial Automation, DC-DC Power Conversion, Power Tools, Robotics

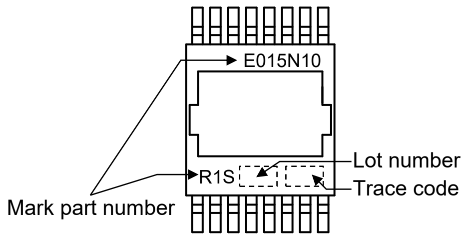
Outline



TOLT



Equivalent Circuit



Marking Specification

Absolute Maximum Ratings

(Tj = 25 °C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$ Tc=25°C Note 2,6	±340	A
	$I_{D(DC)}$ Tc=100°C Note 2,6	±272	A
Drain Current (pulse)	$I_{D(pulse)}$ Note 1,3,6	±1360	A
Power Dissipation	P_D Note 1,6	468	W
Operating Junction Temperature	T_j	-55 to 175	°C
Storage Temperature	T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Note 4	64	A
Single Avalanche Energy	E_{AS} Note 4	409	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ Note 6	0.32	°C/W
Junction to Ambient Thermal Resistance	$R_{th(j-a)}$ Note 5,6	40	°C/W

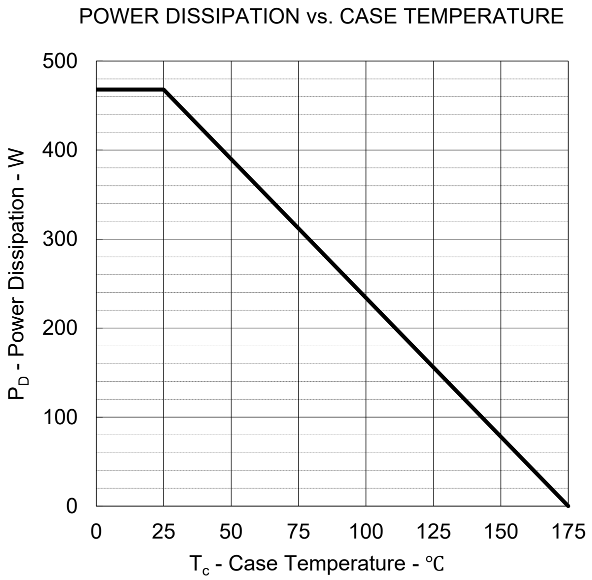
Electrical Characteristics

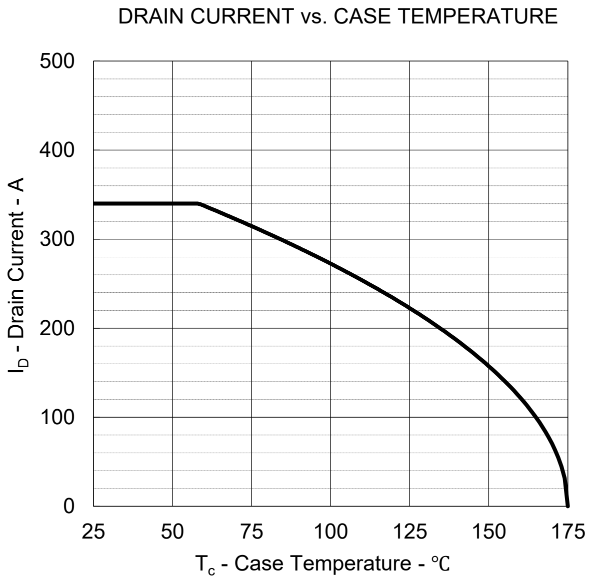
(T_j = 25 °C unless otherwise notice.)

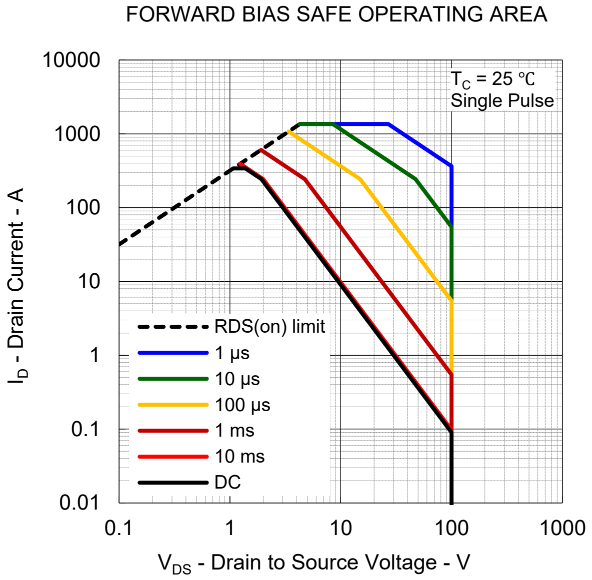
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	V_{DS} = 100 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±100	nA	V_{GS} = ± 20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
Drain to Source On-state Resistance	$R_{DS(on)}$	—	1.3	1.5	mΩ	V_{GS} = 10 V, I_D = 100 A
Input Capacitance	C_{iss}	—	13000	—	pF	V_{DS} = 50 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{oss}	—	3300	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	80	—	pF	
Gate resistance	R_g	—	1.8	—	Ω	—
Turn-on Delay Time	$t_{d(on)}$	—	75	—	ns	V_{DD} = 50 V I_D = 100 A V_{GS} = 10 V R_G = 5 Ω
Rise Time	t_r	—	60	—	ns	
Turn-off Delay Time	$t_{d(off)}$	—	130	—	ns	
Fall Time	t_f	—	55	—	ns	
Total Gate Charge	Q_g	—	170	—	nC	V_{DD} = 50 V V_{GS} = 10 V I_D = 100 A
Gate to Source Charge	Q_{gs}	—	75	—	nC	
Gate to Drain Charge	Q_{gd}	—	30	—	nC	
Gate plateau voltage	$V_{plateau}$	—	5.4	—	V	
Output Charge	Q_{oss}	—	280	—	nC	V_{DD} = 50 V, V_{GS} = 0 V
Body Diode Forward Voltage	$V_{F(S-D)}$	—	0.85	1.5	V	I_F = 100 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	110	—	ns	I_F = 100 A, V_{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q_{rr}	—	300	—	nC	

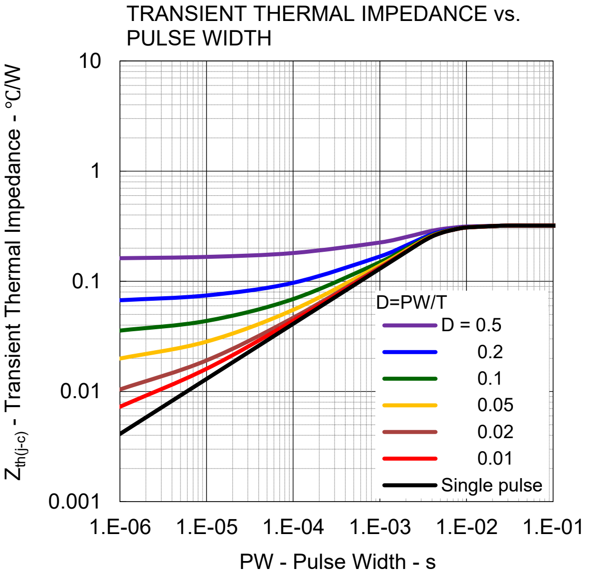
Note 1. T_c = 25 °C
2. Value is limited by overall system design including PCB.
3. PW ≤ 10 μs
4. L = 100 μH, V_{DD} = 50 V, R_G = 25 Ω
5. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)
6. Defined by design. Not subject to production test.

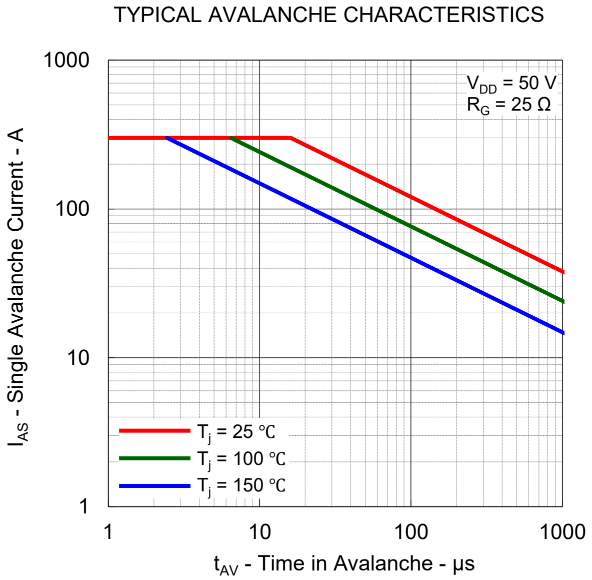
Typical Characteristics

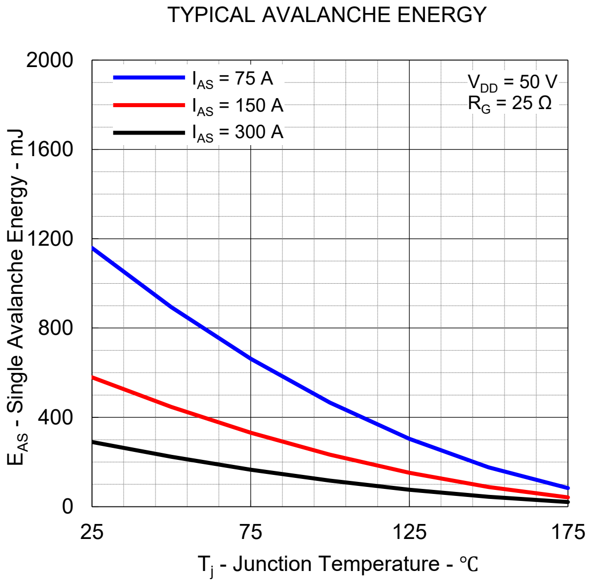




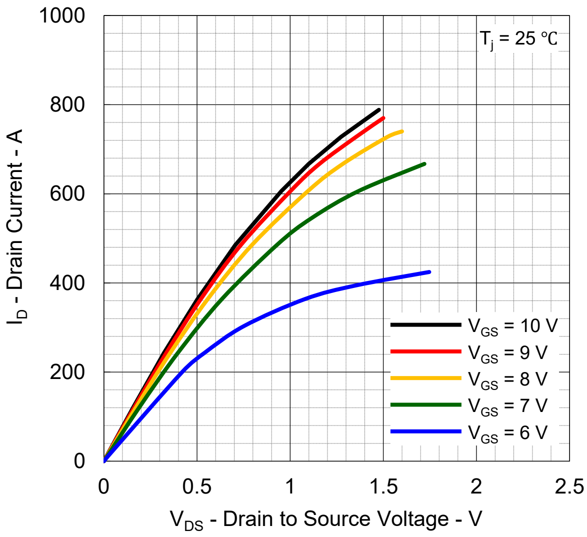




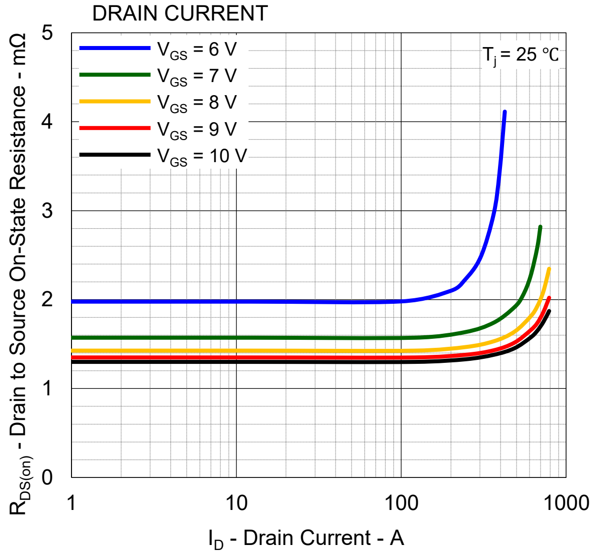




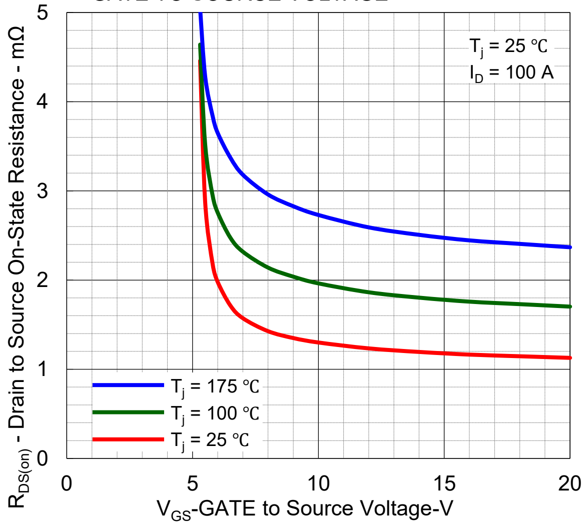
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



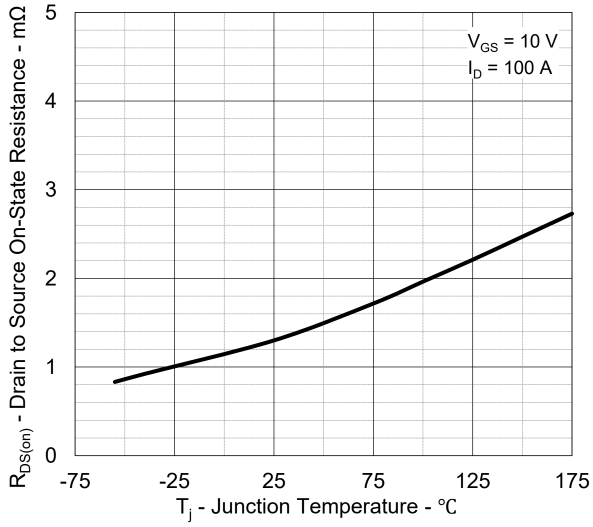
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



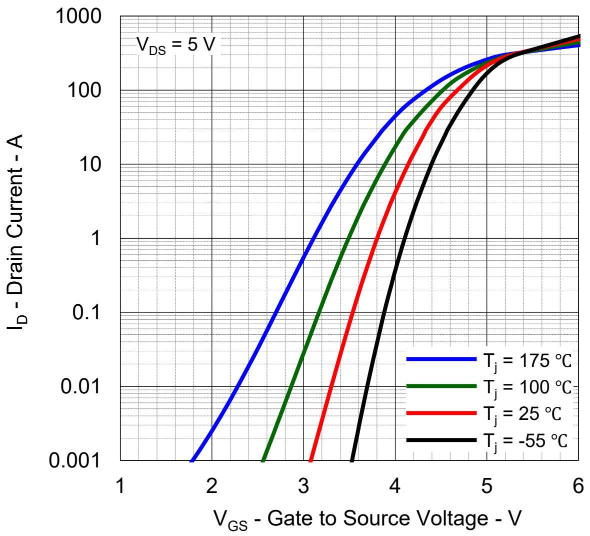
DRAIN TO SOURCE ON-STATERESISTANCE vs. GATE TO SOURCE VOLTAGE



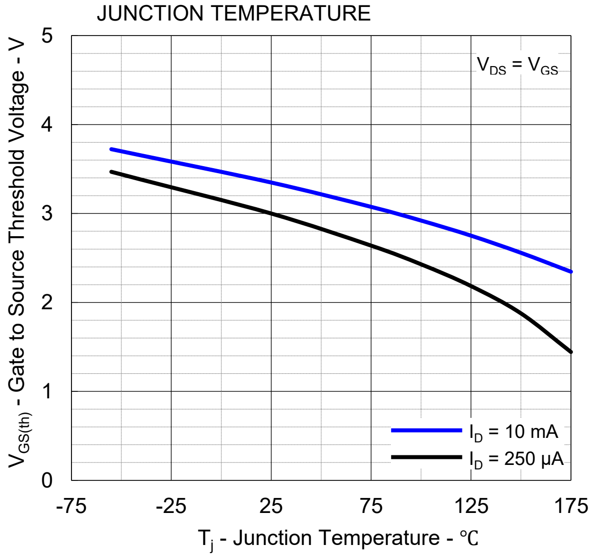
DRAIN TO SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURERE



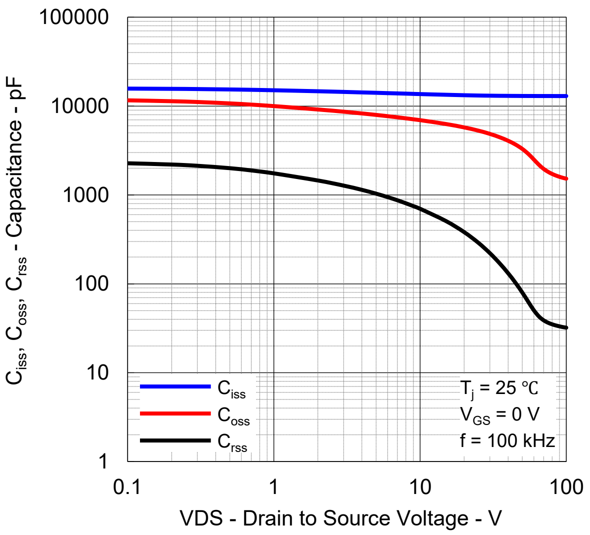
FORWARD TRANSFER CHARACTERISTICS



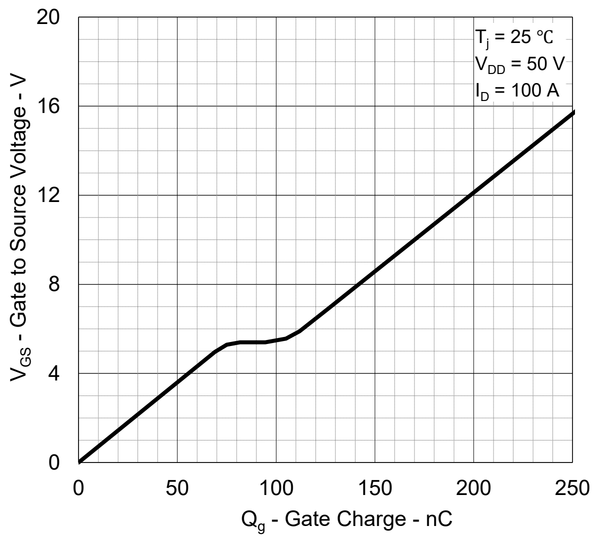
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



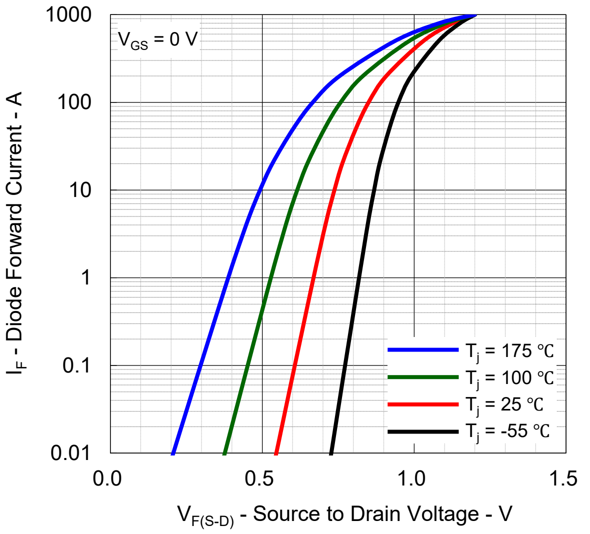
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



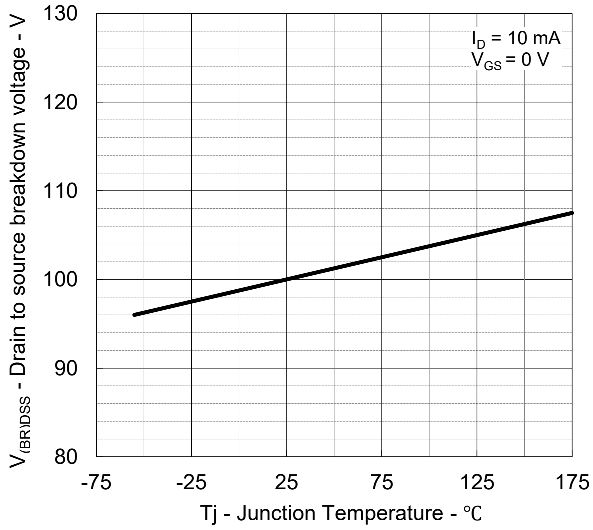
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



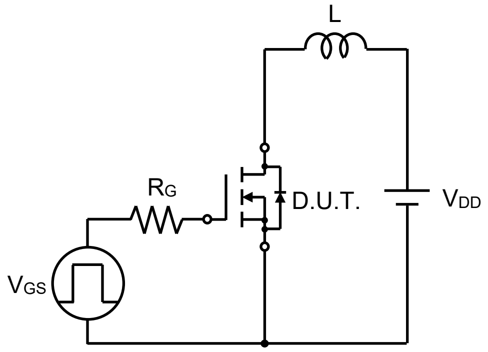
DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE



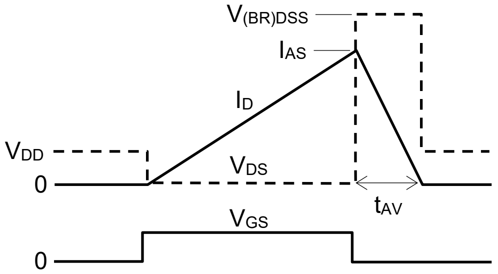
Test Circuit

Avalanche

Test Circuit



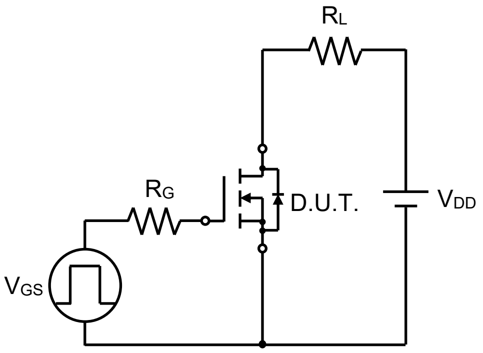
Waveform



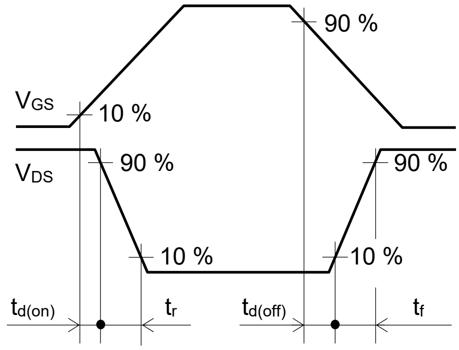
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^{2} \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

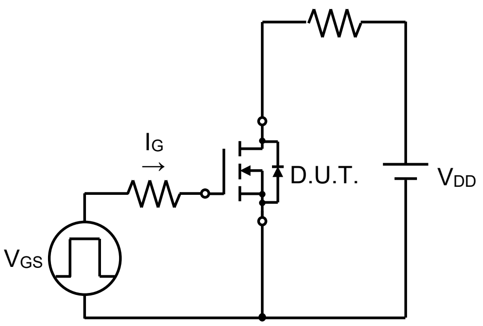


Waveform

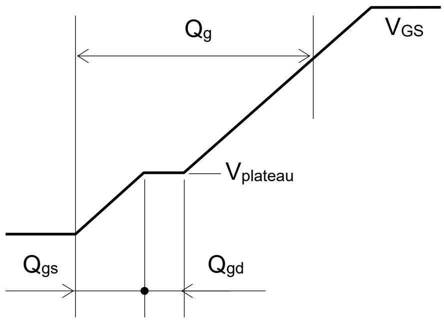


Gate Charge

Test Circuit

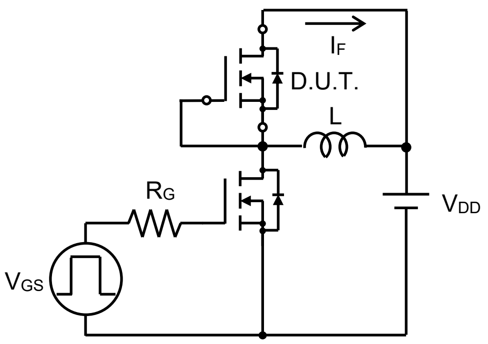


Waveform

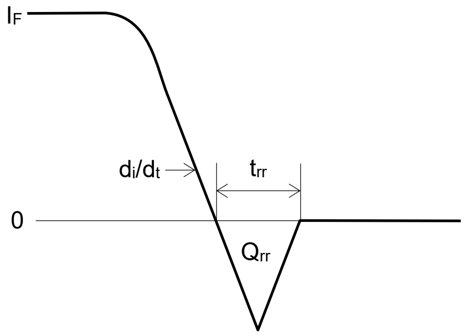


Reverse Recovery

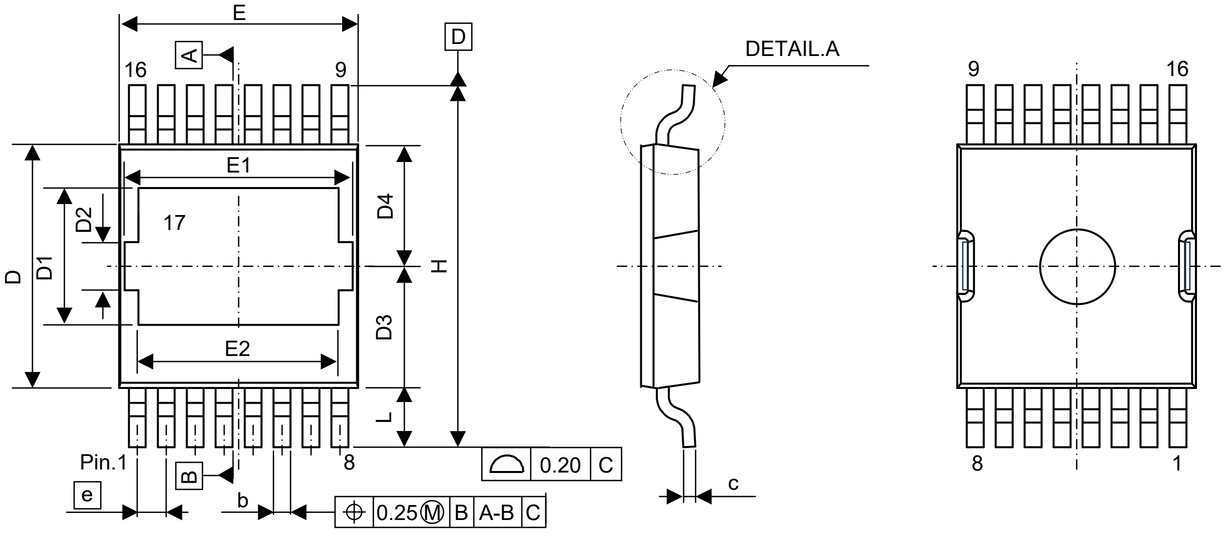
Test Circuit



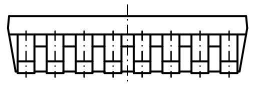
Waveform

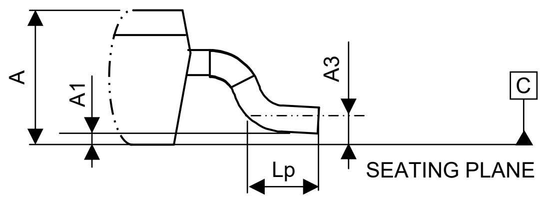


Package Dimensions



Mass : 0.85 g

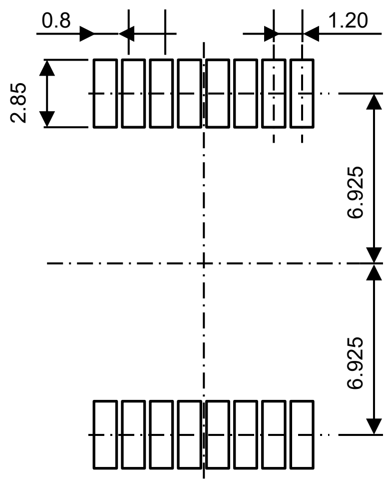




DETAIL. A

SYMBOL	DIMENSION (mm) MIN	NOM	MAX
A	2.2	2.3	2.35
A1	0.01	−	0.16
A3	−	0.5	−
b	0.6	0.7	0.85
c	0.45	0.5	0.65
D	10	10.1	10.3
D1	−	5.67	−
D2	−	2	−
D3	−	5.05	−
D4	5	5.05	5.13
E	9.7	9.9	10.1
E1	−	9.46	−
E2	−	8.3	−
e	1.20BSC		
H	14.8	15	15.2
L	2.25	2.45	2.65
Lp	1.3	1.5	1.7

Mount pad

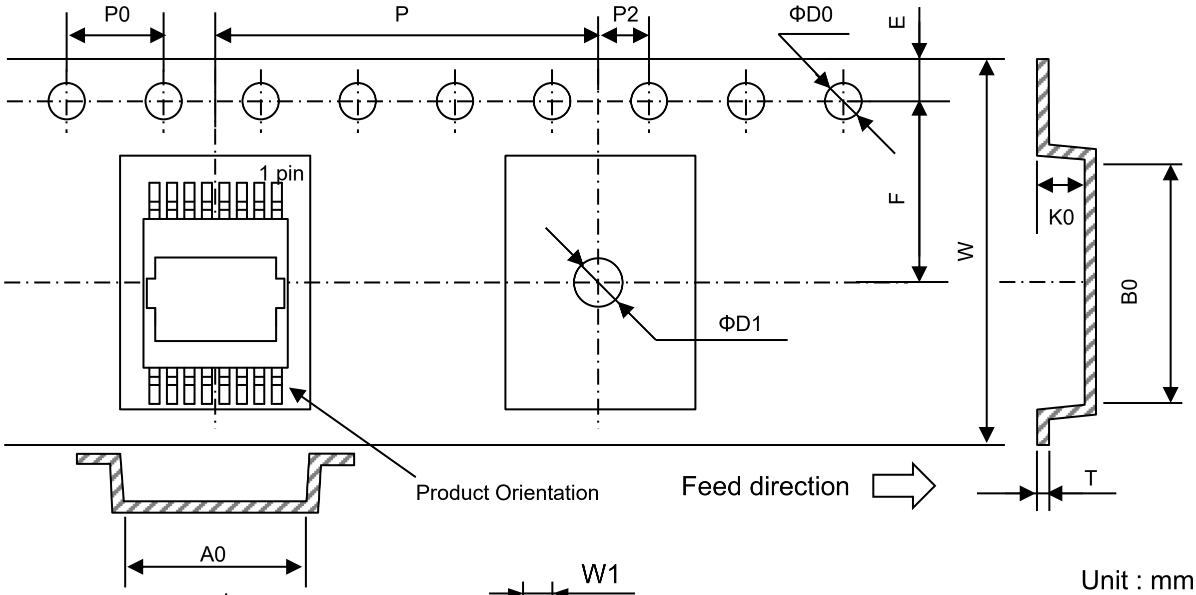


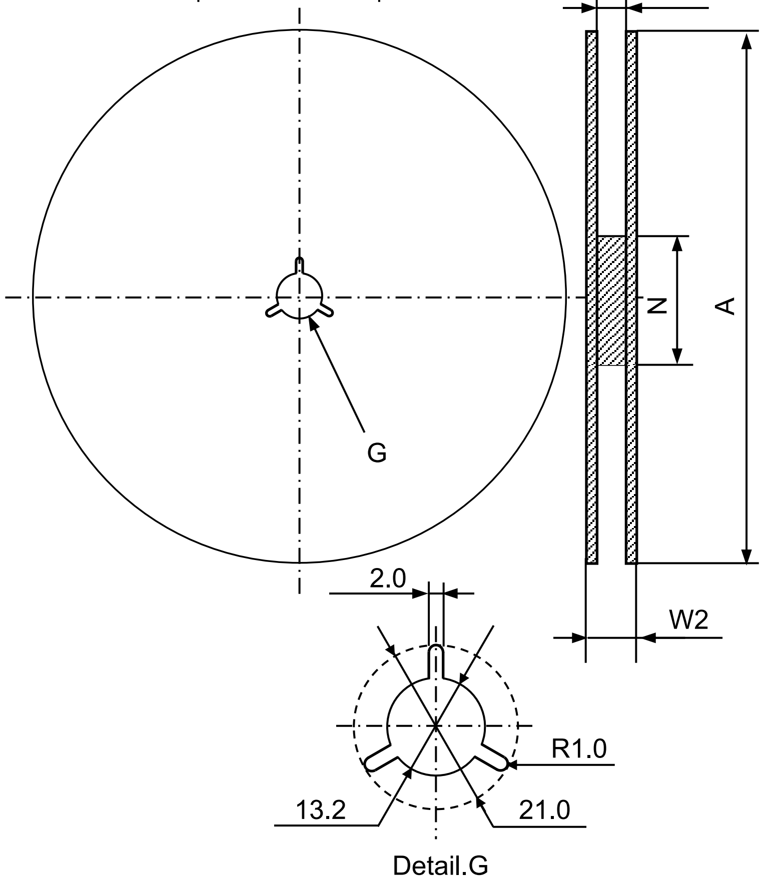
Unit : mm

Ordering Information

Part No.	Packing	Quantity
RBE015N10R1SZPW#KB0	Taping	1300pcs/reel

Packing Specification





Unit : mm

	Symbol	Dimension
Tape Dimension	W	24
	P	16
	P0	4
	P2	2
	A0	10.4
	B0	15.5
	K0	2.65
	F	11.5
	E	1.75
	D0	1.5
	D1	1.5
	T	0.4
Reel Dimension	A	330
	N	100
	W1	25.4
	W2	29.4

Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Corporate Headquarters

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Trademarks

Contact information

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