

RBE093N08R1SZN2

REXFET-1 N-Channel Power MOSFET

80 V - 50 A - 9.3 mΩ - μ SO8-FL(3×3)

Description

The RBE093N08R1SZN2 N-channel power MOSFET features REXFET-1 split-gate technology and is offered in a $3x3~\mu$ SO8-FL package. The μ SO8-FL package features ultra compact, leadless designs with Wettable Flanks to support enhanced thermal performance, reliability and ease of assembly. Renesas' split gate technology is suitable for applications requiring low RDS(on) and switching capability for high-power and high-frequency applications.

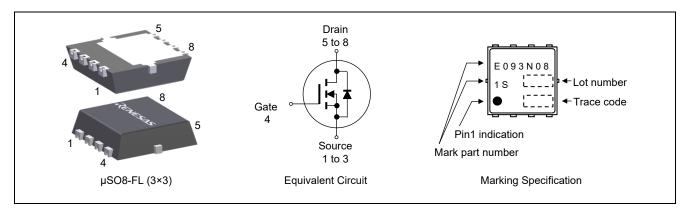
Features

- Standard level gate drive voltage: V_{GS(th)} = 2.0 to 4.0 V
- Super Low on-state resistance: $R_{DS(on)} = 9.3 \text{ m}\Omega$ Max.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

Motor Control, Energy Infrastructure, Industrial Automation, DC-DC Power Conversion, Power, Tools, Robotics

Outline



Absolute Maximum Ratings

(Tj = 25 °C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V _{DSS}	80	V
Gate to Source Voltage	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)} Note 1,2,6	±50	A
Drain Current (pulse)	I _{D(pulse)} Note 1,3,6	±150	A
Power Dissipation	P _D Note 1,6	57	W
Operating Junction Temperature	Tj	-55 to 175	°C
Storage Temperature	T _{stg}	-55 to 175	°C
Single Avalanche Current	IAS Note 4	18	A
Single Avalanche Energy	Eas Note 4	32.4	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	Rth(j-c) Note 6	2.6	°C/W
Junction to Ambient Thermal Resistance	Rth(j-a) Note 5,6	60	°C/W

Electrical Characteristics

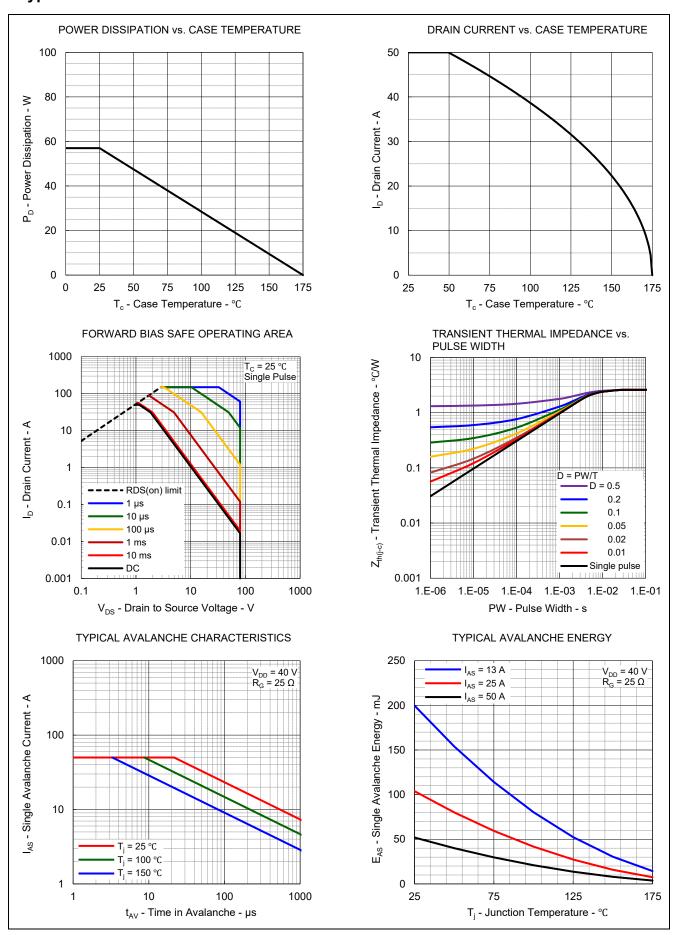
(T j= 25 °C unless otherwise notice.)

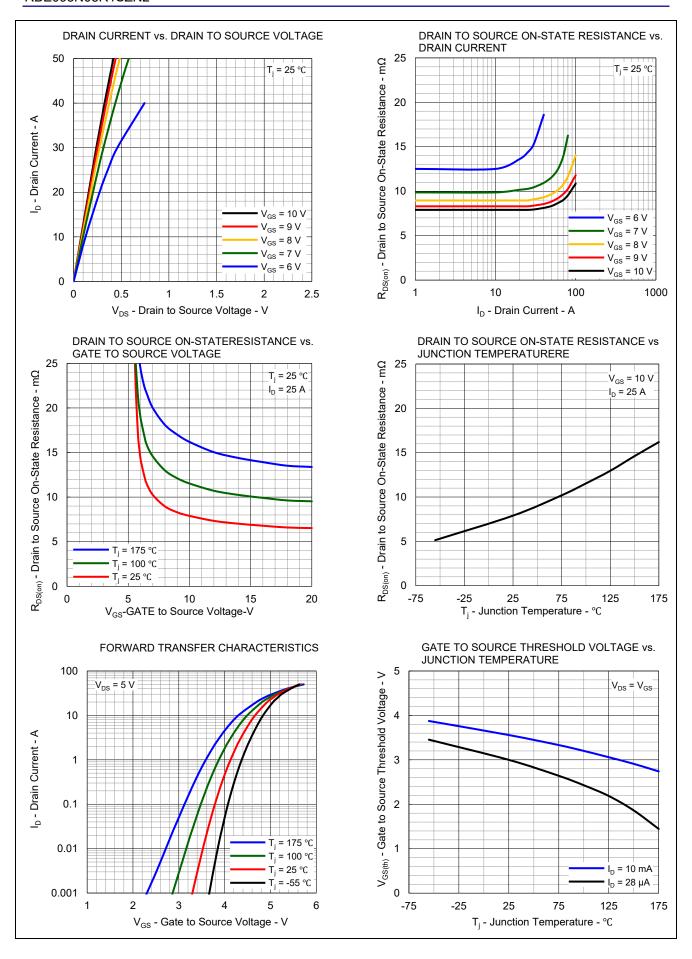
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}	_	_	10	μA	V _{DS} = 80 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}	_	_	±1	μA	V_{GS} = \pm 20 V , V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	_	4.0	V	$V_{DS} = V_{GS}$, $I_D = 28 \mu A$
Drain to Source On-state Resistance	R _{DS(on)}	_	7.9	9.3	mΩ	V _G s = 10 V, I _D = 25 A
Input Capacitance	C _{iss}	_	1800	_	pF	V _{DS} = 40 V
Output Capacitance	C _{oss}	_	290	_	pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}	_	14	_	pF	f = 100 kHz
Gate resistance	R _g	_	1.0	_	Ω	
Turn-on Delay Time	t _{d(on)}	_	17	_	ns	V _{DD} = 40 V
Rise Time	t _r	_	7.6	_	ns	I _D = 25 A
Turn-off Delay Time	t _{d(off)}	_	28	_	ns	V _{GS} = 10 V
Fall Time	t _f	_	9.5	_	ns	$R_G = 5 \Omega$
Total Gate Charge	Q _g	_	28	_	nC	V _{DD} = 40 V
Gate to Source Charge	Q_{gs}	_	12	_	nC	V _G s = 10 V
Gate to Drain Charge	Q_{gd}	_	5.0	_	nC	I _D = 25 A
Gate plateau voltage	V _{plateau}	_	5.7	_	V	
Output Charge	Q _{oss}	_	25	_	nC	V _{DD} = 40 V, V _{GS} = 0 V
Body Diode Forward Voltage	$V_{F(S-D)}$	_	0.88	1.5	V	I _F = 25 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	_	39	_	ns	I _F = 25 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	_	54	_	nC	di/dt = 100 A/μs

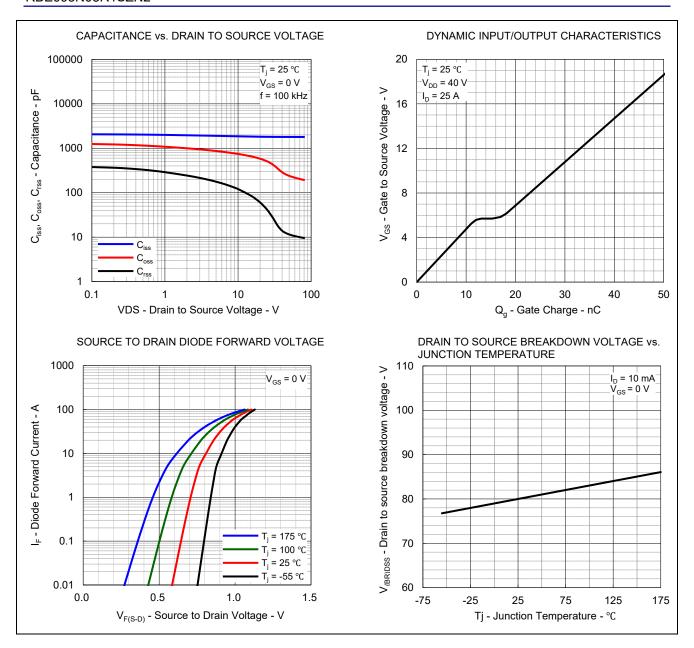
Note 1. T_c = 25 °C

- 2. Value is limited by overall system design including PCB.
- 3. PW \leq 100 μ s
- 4. L = 100 μ H, V_{DD} = 40 V, R_G = 25 Ω
- 5. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)
- 6. Defined by design. Not subject to production test.

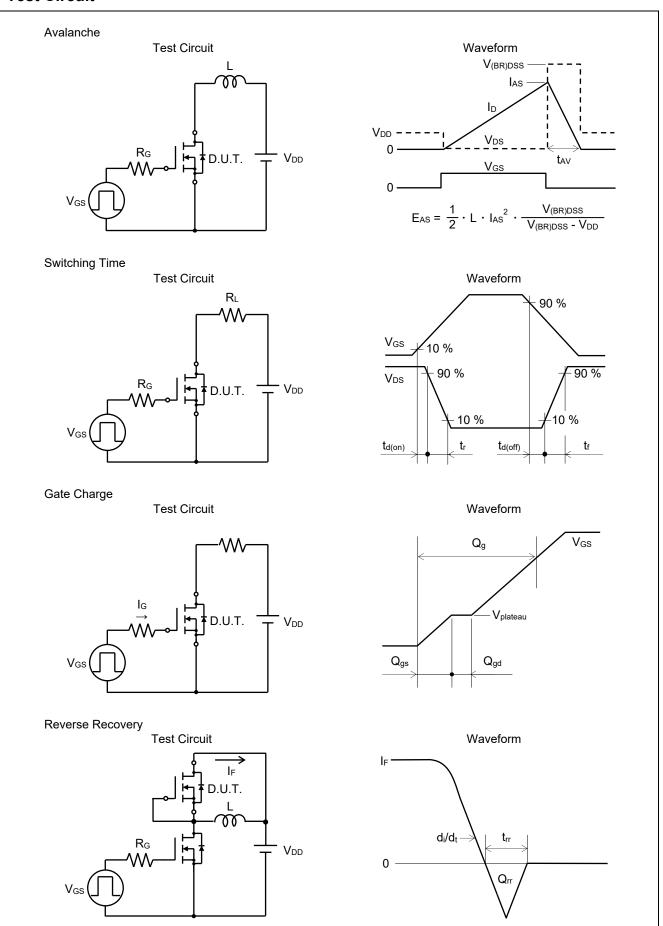
Typical Characteristics



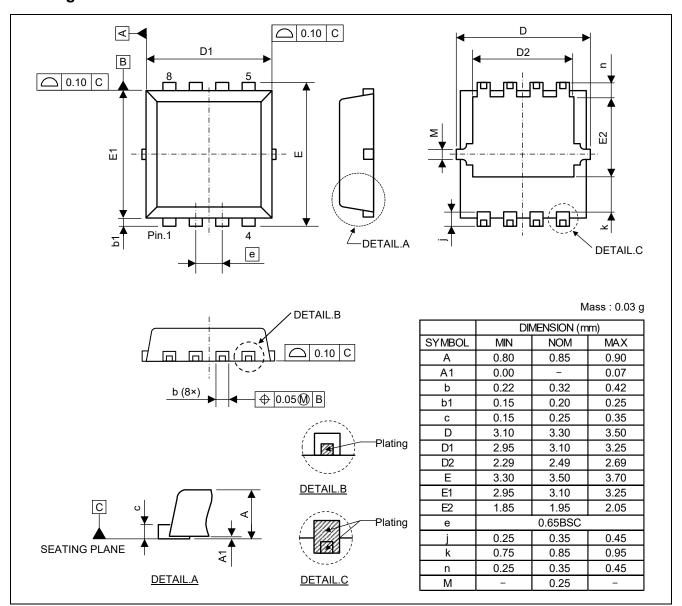




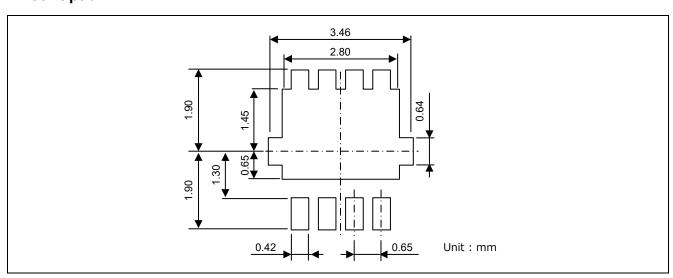
Test Circuit



Package Dimensions



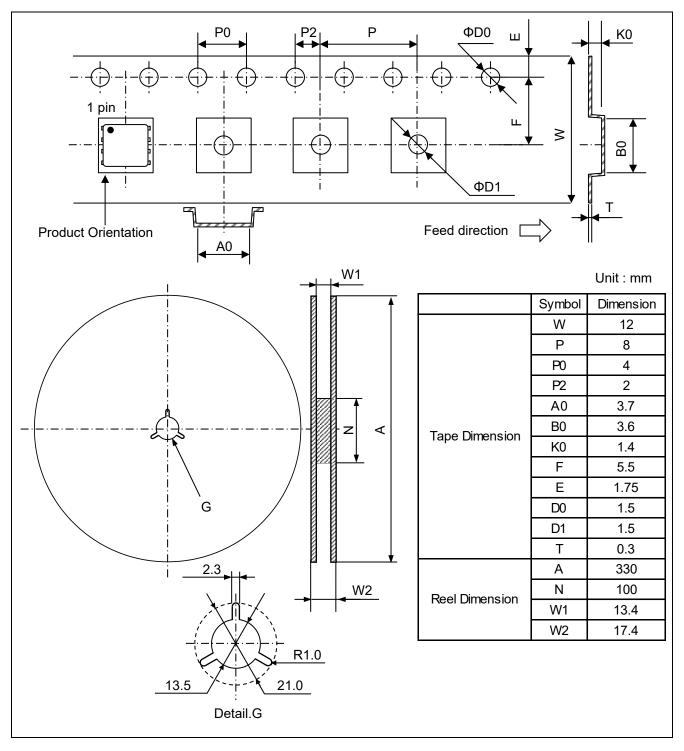
Mount pad



Ordering Information

Part No.	Packing	Quantity
RBE093N08R1SZN2#HB0	Taping	3000 pcs/reel

Packing Specification



Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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(Rev.5.0-1 October 2020)

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