

RBE111N10R1SZN2

REXFET-1 N-Channel [Power MOSFET](#)

100 V - 40 A - 11.1 mΩ - μSO8-FL(3×3)

Description

The RBE111N10R1SZN2 N-channel power MOSFET features REXFET-1 split-gate technology and is offered in a 3x3 μSO8-FL package. The μSO8-FL package features ultra compact, leadless designs with Wettable Flanks to support enhanced thermal performance, reliability and ease of assembly. Renesas' split gate technology is suitable for applications requiring low RDS(on) and switching capability for high-power and high-frequency applications.

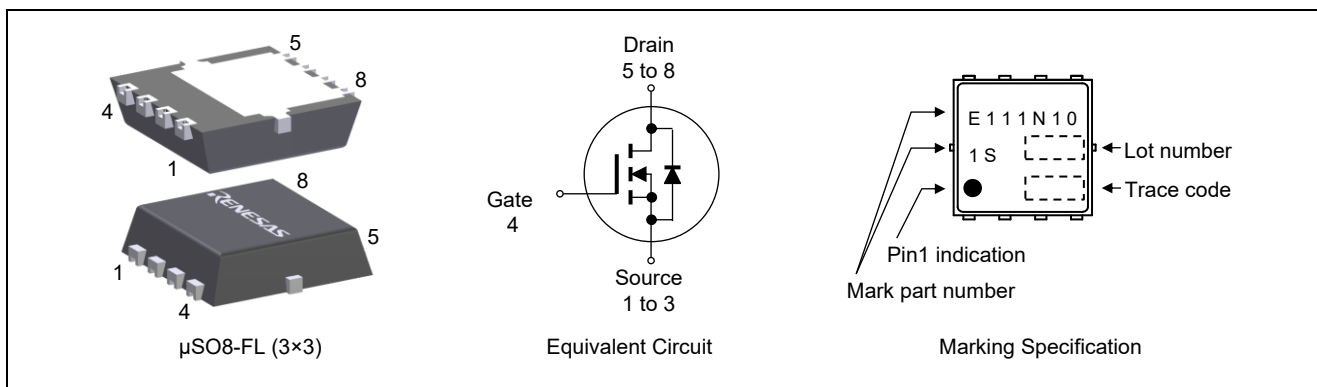
Features

- Standard level gate drive voltage: $V_{GS(th)} = 2.0$ to 4.0 V
- Low on-state resistance: $R_{DS(on)} = 11.1$ mΩ Max.
- Low input capacitance
- Low thermal resistance
- 100% Avalanche tested
- Pb-free lead plating: RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

Motor Control, Energy Infrastructure, Industrial Automation, DC-DC Power Conversion, Power, Tools, Robotics

Outline



Absolute Maximum Ratings

(Tj = 25 °C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$ <small>Note 1,2,6</small>	±40	A
Drain Current (pulse)	$I_{D(pulse)}$ <small>Note 1,3,6</small>	±120	A
Power Dissipation	P_D <small>Note 1,6</small>	57	W
Operating Junction Temperature	T_j	-55 to 175	°C
Storage Temperature	T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} <small>Note 4</small>	17	A
Single Avalanche Energy	E_{AS} <small>Note 4</small>	28.9	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ ^{Note 6}	2.6	°C/W
Junction to Ambient Thermal Resistance	$R_{th(j-a)}$ ^{Note 5,6}	60	°C/W

Electrical Characteristics

(T_j = 25 °C unless otherwise notice.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	V _{DS} = 100 V, V _{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±1	μA	V _{GS} = ± 20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	V _{GS(th)}	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 28 μA
Drain to Source On-state Resistance	R _{DS(on)}	—	9.7	11.1	mΩ	V _{GS} = 10 V, I _D = 20 A
Input Capacitance	C _{iss}	—	1700	—	pF	V _{DS} = 50 V
Output Capacitance	C _{oss}	—	390	—	pF	V _{GS} = 0 V
Reverse Transfer Capacitance	C _{rss}	—	18	—	pF	f = 100 kHz
Gate resistance	R _g	—	1.0	—	Ω	—
Turn-on Delay Time	t _{d(on)}	—	19	—	ns	V _{DD} = 50 V
Rise Time	t _r	—	9.6	—	ns	I _D = 20 A
Turn-off Delay Time	t _{d(off)}	—	28	—	ns	V _{GS} = 10 V
Fall Time	t _f	—	11	—	ns	R _G = 5 Ω
Total Gate Charge	Q _g	—	27	—	nC	V _{DD} = 50 V
Gate to Source Charge	Q _{gs}	—	11	—	nC	V _{GS} = 10 V
Gate to Drain Charge	Q _{gd}	—	5.7	—	nC	I _D = 20 A
Gate plateau voltage	V _{plateau}	—	5.5	—	V	
Output Charge	Q _{oss}	—	32	—	nC	V _{DD} = 50 V, V _{GS} = 0 V
Body Diode Forward Voltage	V _{F(S-D)}	—	0.87	1.5	V	I _F = 20 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}	—	45	—	ns	I _F = 20 A, V _{GS} = 0 V
Reverse Recovery Charge	Q _{rr}	—	62	—	nC	di/dt = 100 A/μs

Note 1. T_c = 25 °C

2. Value is limited by overall system design including PCB.

3. PW ≤ 100 μs

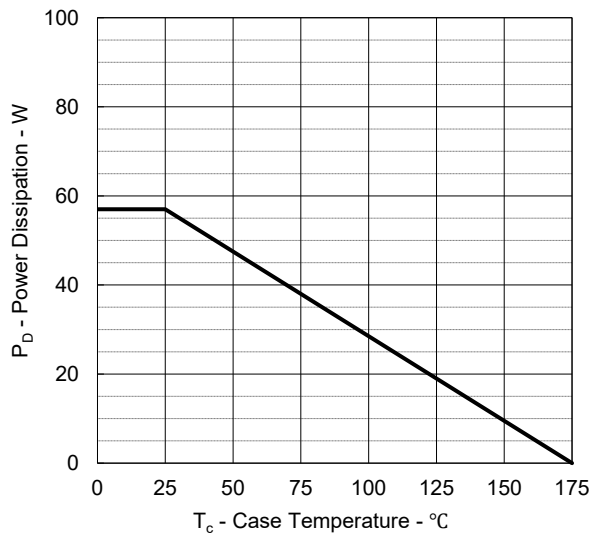
4. L = 100 μH, V_{DD} = 50 V, R_G = 25 Ω

5. Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4. (2 oz Cu pad.)

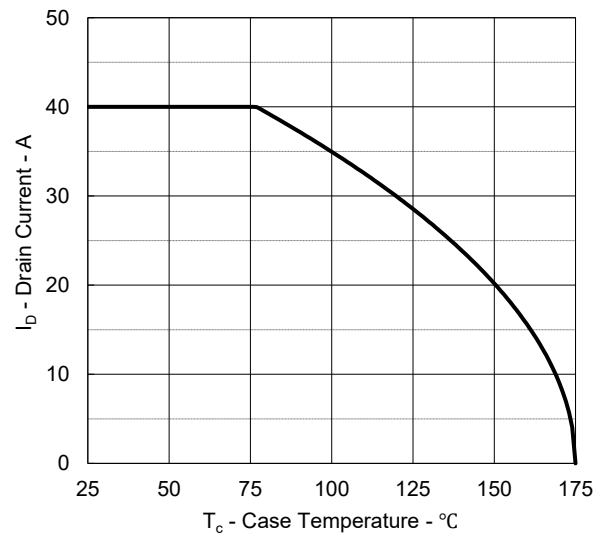
6. Defined by design. Not subject to production test.

Typical Characteristics

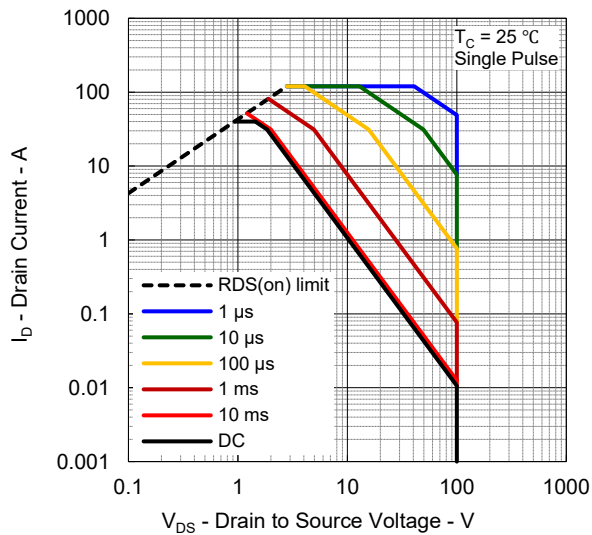
POWER DISSIPATION vs. CASE TEMPERATURE



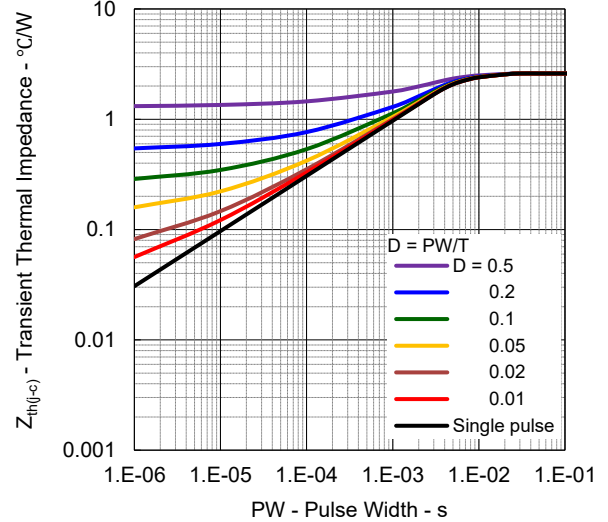
DRAIN CURRENT vs. CASE TEMPERATURE



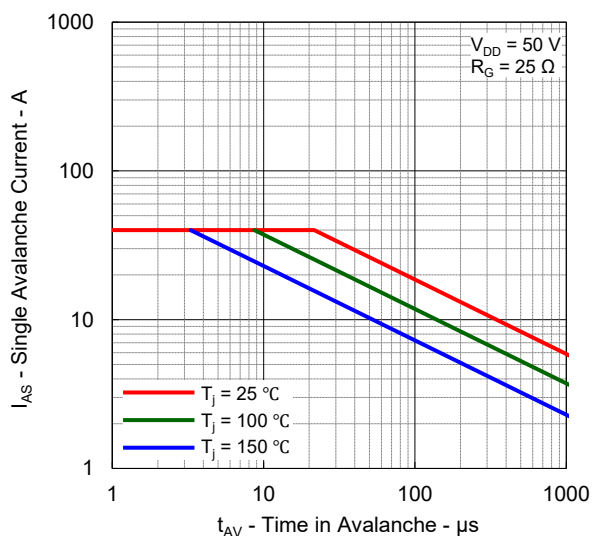
FORWARD BIAS SAFE OPERATING AREA



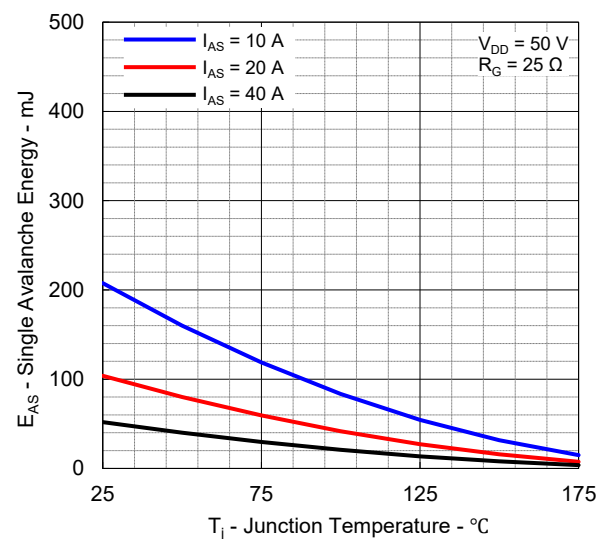
TRANSIENT THERMAL IMPEDANCE vs. PULSE WIDTH



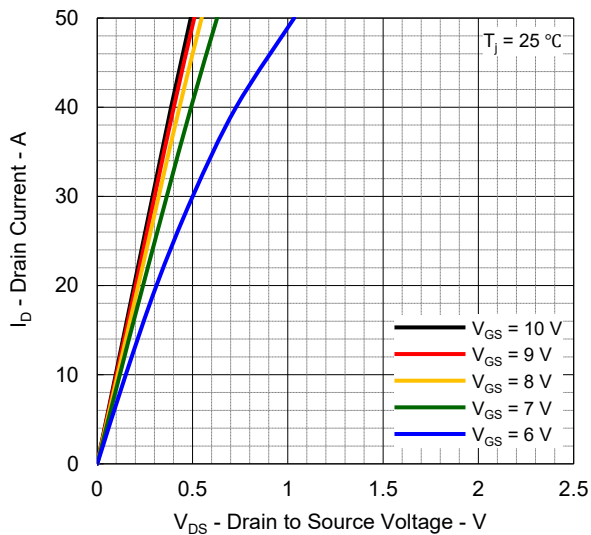
TYPICAL AVALANCHE CHARACTERISTICS



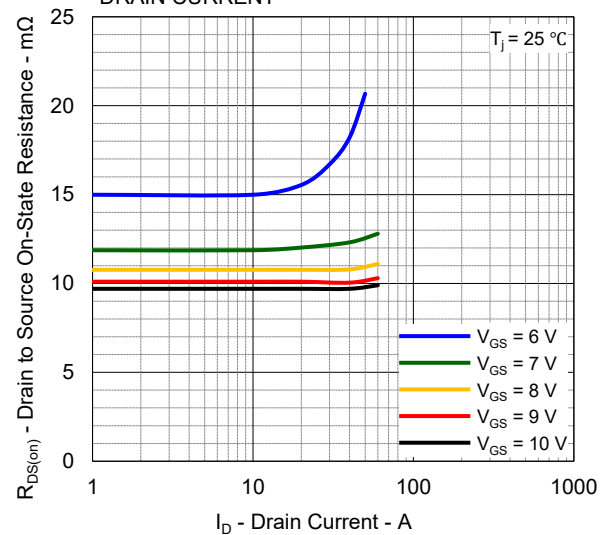
TYPICAL AVALANCHE ENERGY



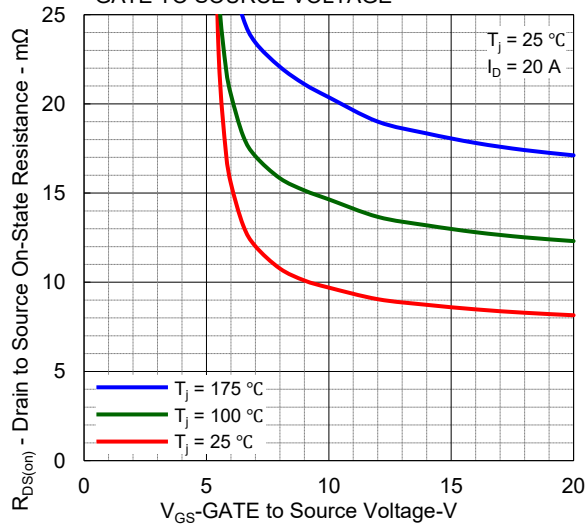
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



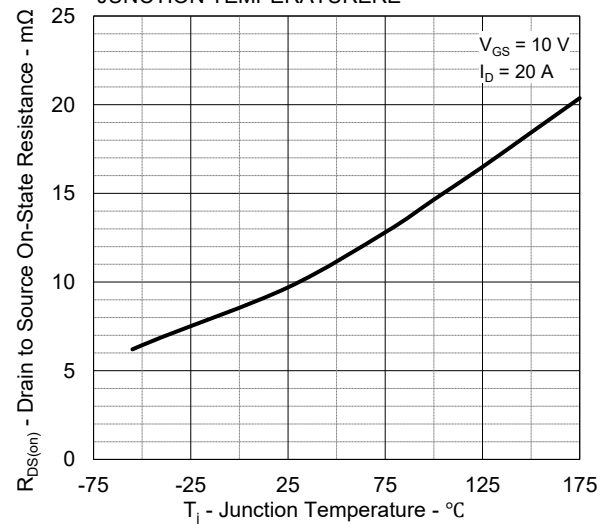
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



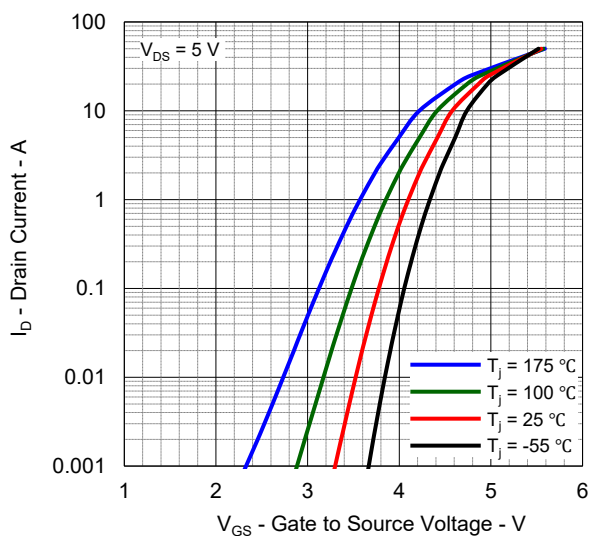
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



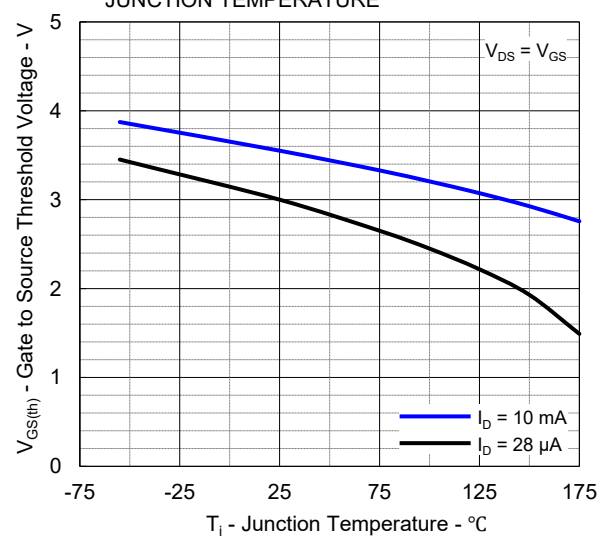
DRAIN TO SOURCE ON-STATE RESISTANCE vs. JUNCTION TEMPERATURE



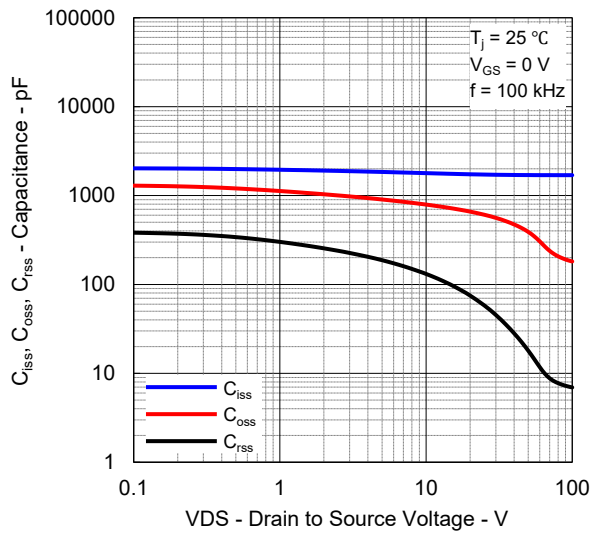
FORWARD TRANSFER CHARACTERISTICS



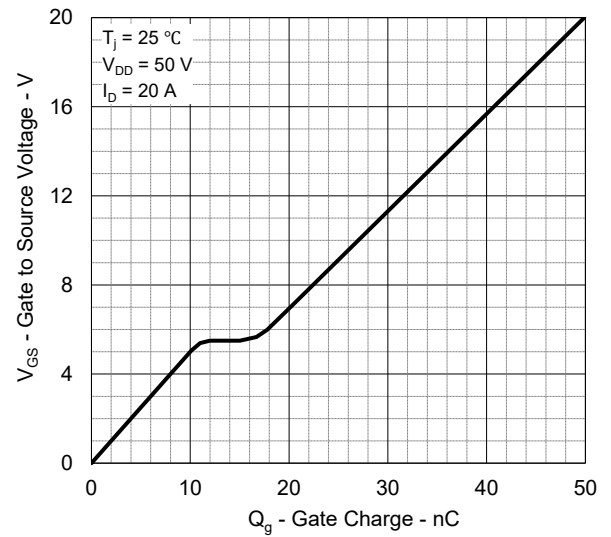
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



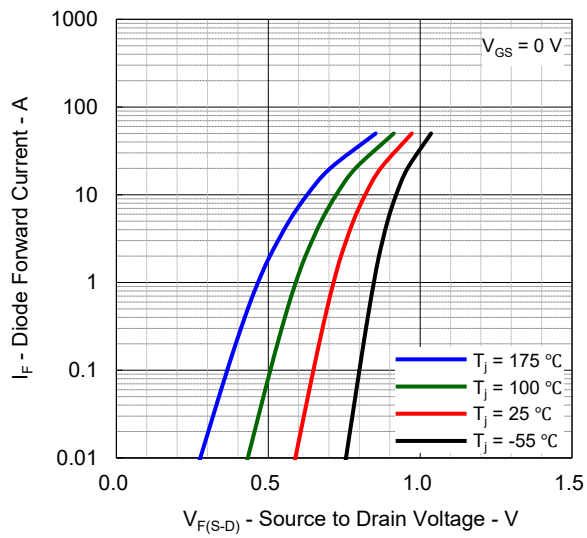
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



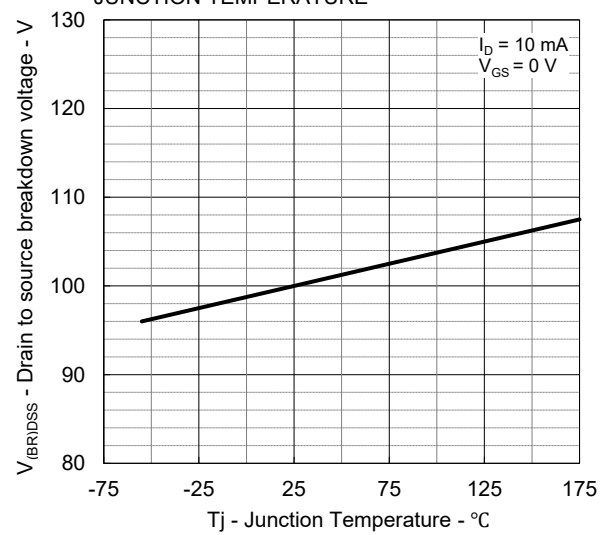
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

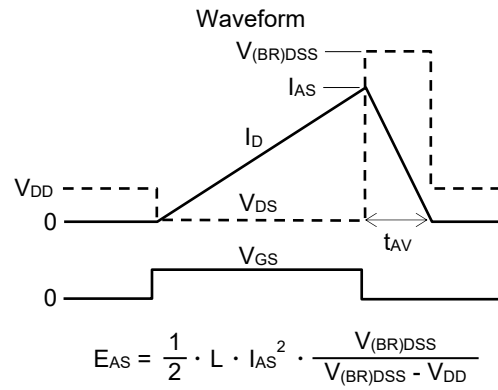
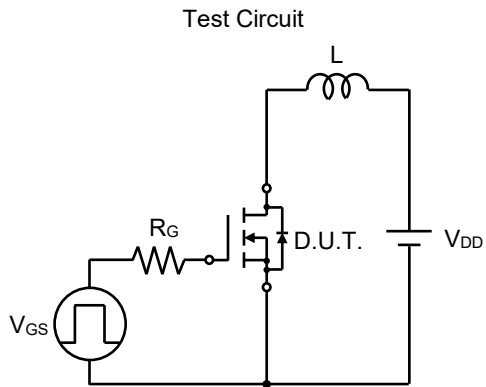


DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE

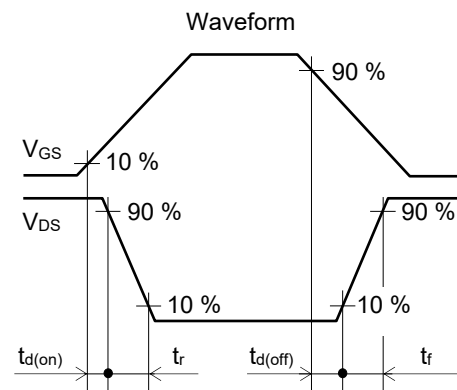
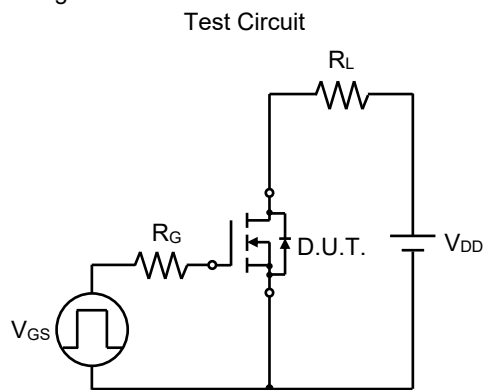


Test Circuit

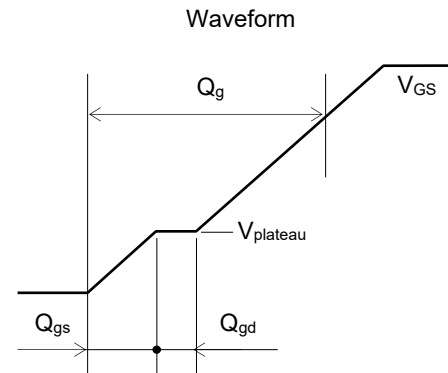
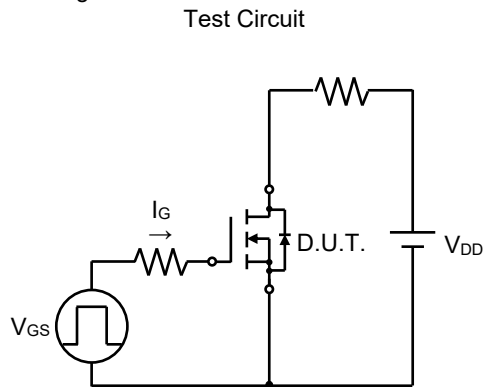
Avalanche



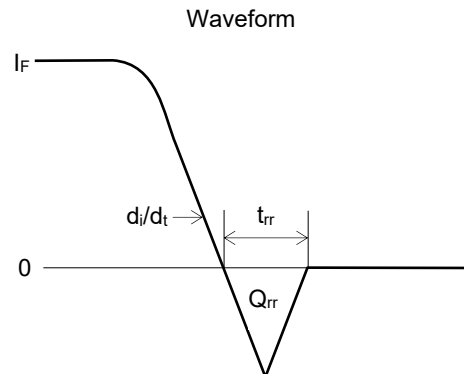
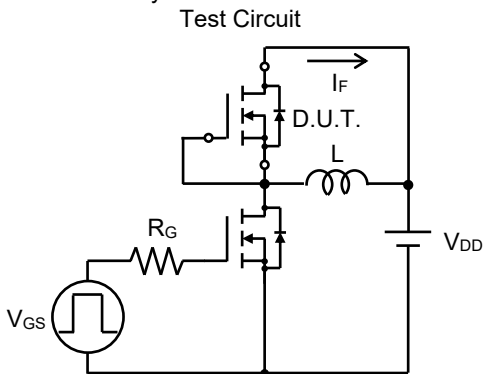
Switching Time



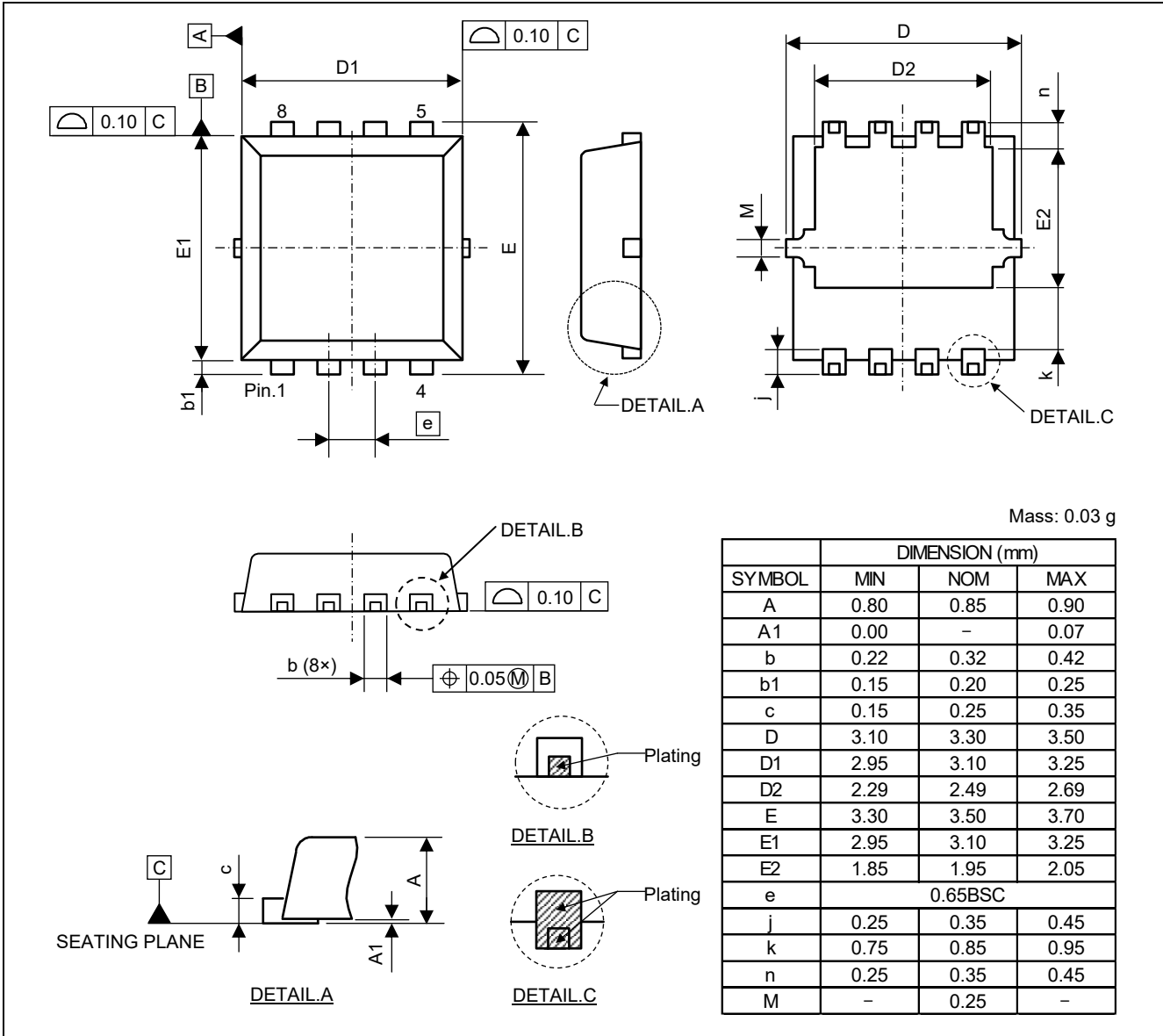
Gate Charge



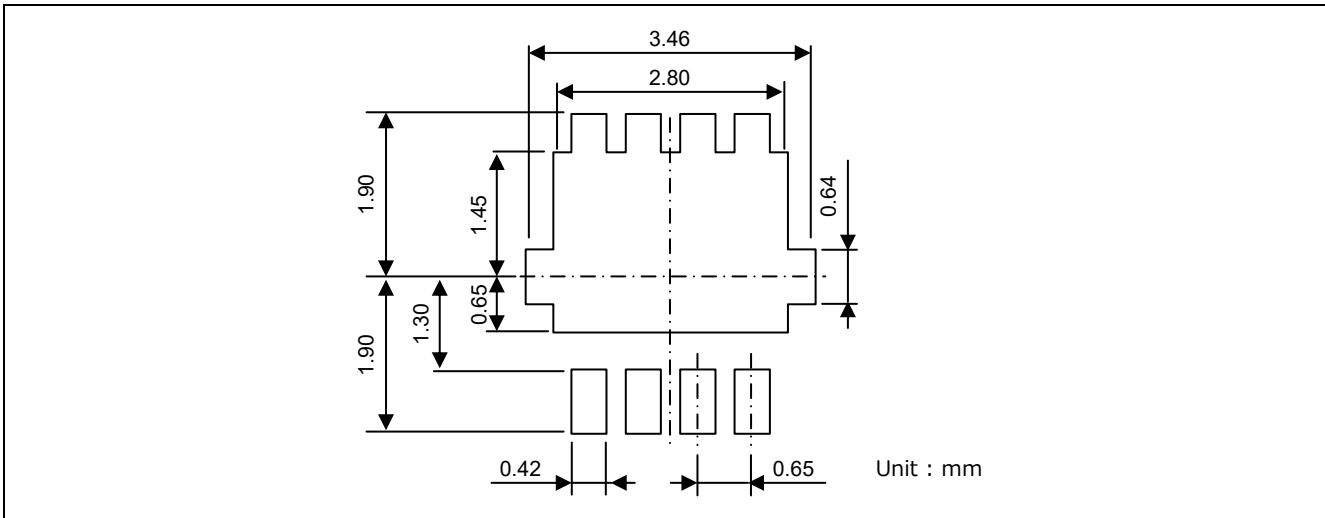
Reverse Recovery



Package Dimensions



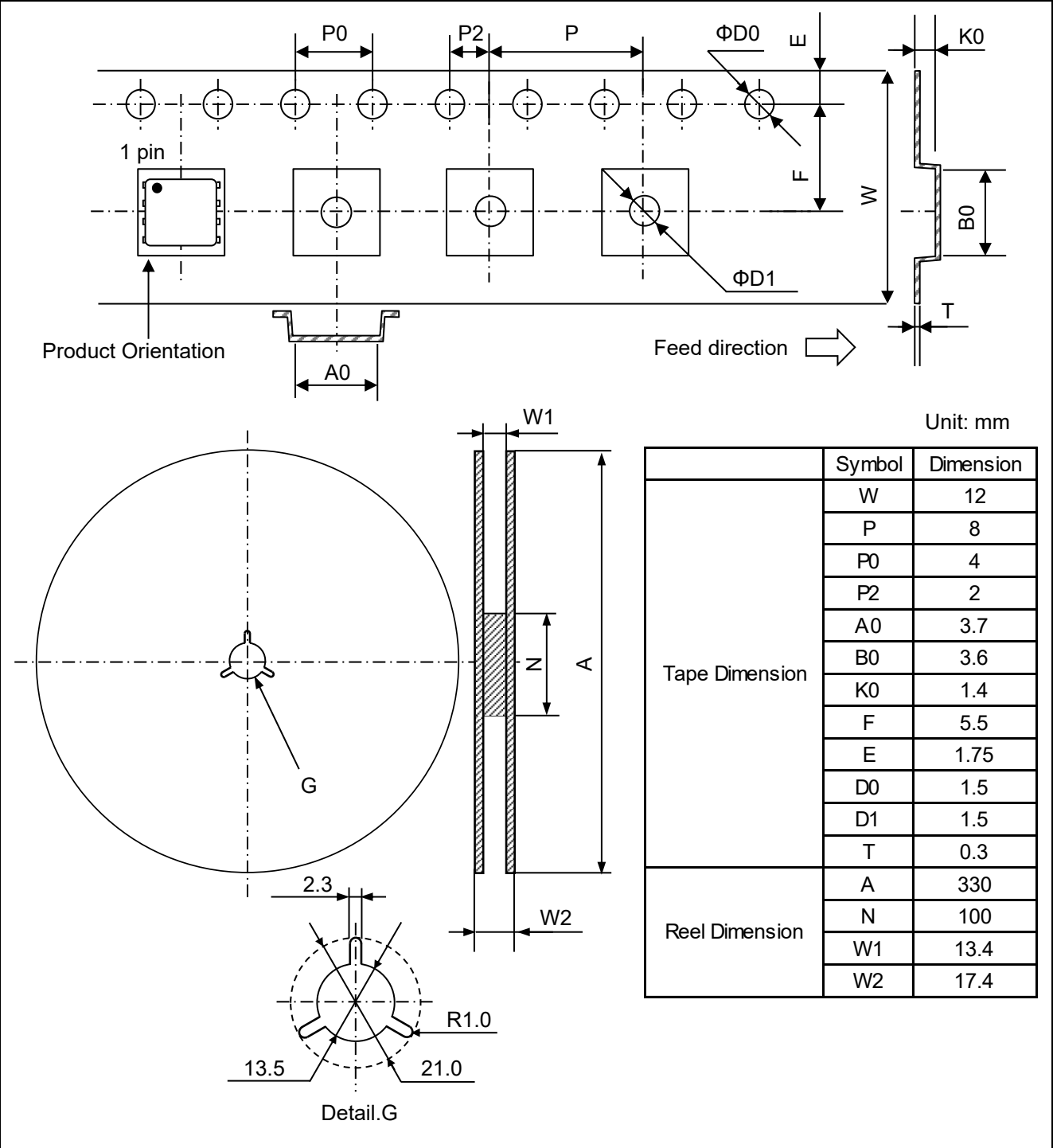
Mount pad



Ordering Information

Part No.	Packing	Quantity
RBE111N10R1SZN2#HB0	Taping	3000 pcs/reel

Packing Specification



Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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