Datasheet

RC193xx

PCIe Gen7 1.8V 2-Input Clock Mux Family with LOS

Description

The RC193xx (RC19302, RC19304, RC19308) ultra-high performance clock muxes support PCIe Gen 1-7. They provide a Loss-Of-Signal (LOS) output for system monitoring and redundancy. The devices also incorporate Power Down Tolerance (PDT), Flexible Power Sequencing (FPS), and Automatic Clock Parking (ACP) features, easing system design. They can drive both source-terminated and double-terminated loads, operating up to 400MHz.

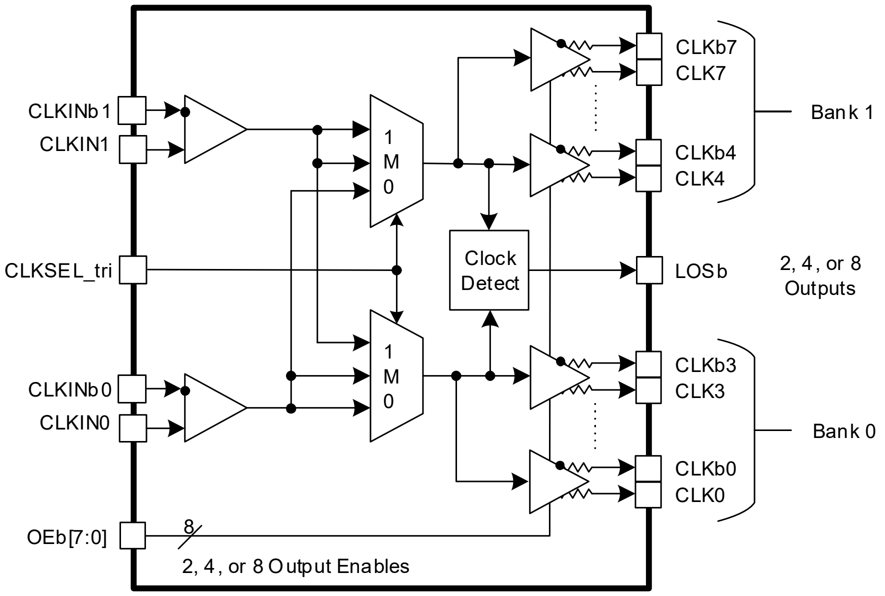
The family offers 2, 4, or 8 Low-Power (LP) HCSL output pairs in 3 × 3, 4 × 4, and 6 × 6 mm packages. The buffers support both Common Clock (CC) and Independent Reference (IR) PCIe clock architectures.

Applications

- Cloud/High-performance computing
- nVME storage
- Networking
- AI Accelerators

Features

- Very Low Additive Phase Jitter:
  - PCIe Gen5 CC: 6.9fs RMS (typ.)
  - PCIe Gen6 CC: 4.1fs RMS (typ.)
  - PCIe Gen7 CC: 2.9fs RMS (typ.)
  - DB2000Q: 11.5fs RMS (typ.)
  - 12kHz - 20MHz (156.25MHz): 42.8fs RMS (typ.)
- 2:N or dual x 1:N/2 modes (N is number of outputs)
- Power Down Tolerant (PDT) inputs
- Flexible Startup Sequencing (FSS)
- Automatic Clock Parking (ACP) upon loss of selected CLKIN
- Spread-spectrum tolerant
- CLKIN accepts HCSL or LVDS signal levels
- Dedicated OEb pin per output
- -40 to +105°C, 1.8V ± 5% operation
- Devices provide:
  - Pin or SMBus selectable 34Ω, 85Ω, or 100Ω differential output impedance
  - Pin or SMBus selectable output slew rate
  - Pin or SMBus selectable output amplitude
  - 9 SMBus addresses plus write protection



CLKSEL_tri	0	1	M
Bank 0	CLKIN0	CLKIN1	CLKIN0
Bank 1	CLKIN0	CLKIN1	CLKIN1

Figure 1. Simplified Block Diagram and Mux Logic

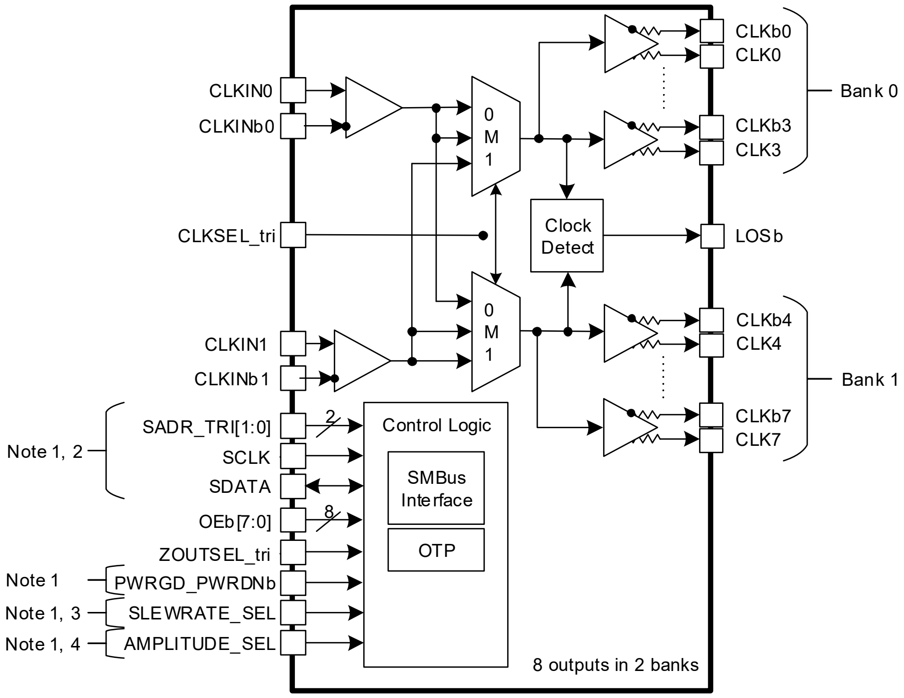
Contents

1. Pin Information

1.1 Signal Types

Term	Description
I	Input
O	Input
OD	Open Drain Output
I/O	Bi-Directional
PD	Pull-down
PU	Pull-up
Z	Tristate
D	Driven
X	Don't care
SE	Single-ended
DIF	Differential
PWR	3.3 V power
GND	Ground
PDT	Power Down Tolerant: These signals tolerate being driven when the device is powered down (VDD is not present).

1.2 Detailed Block Diagram



Note 1: RC19302 does not have these pins.
Note 2: RC19204, RC19304A100 do not have these pins
Note 3: RC19308, RC19304 only.
Note 4: RC19308A100, RC19304A100 only.

Figure 2. RC1930x Detailed Block Diagram

1.3 RC19308 Pin Information

1.3.1 RC19308 Pin Information

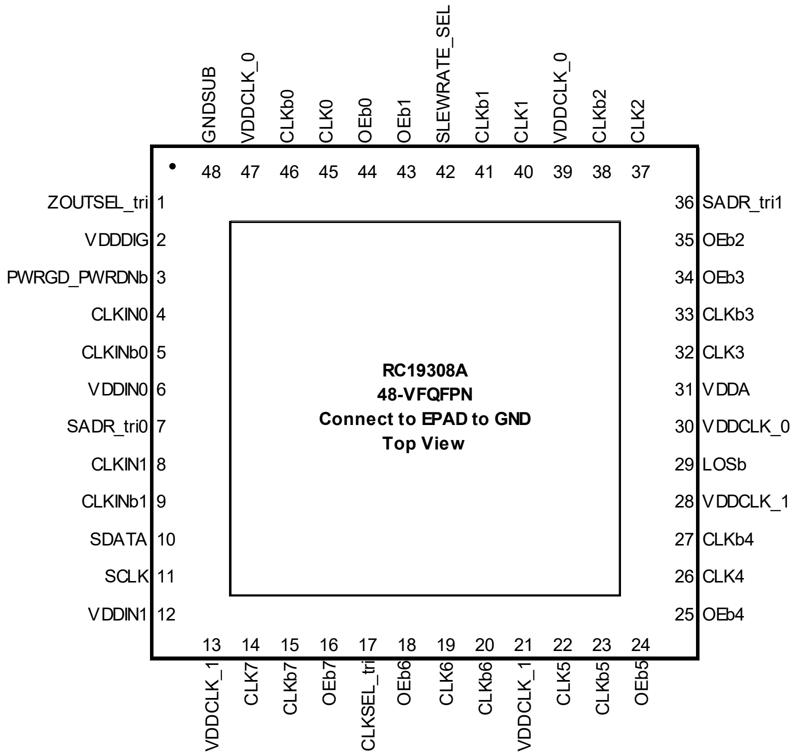


Figure 3. RC19308A Pin Assignments

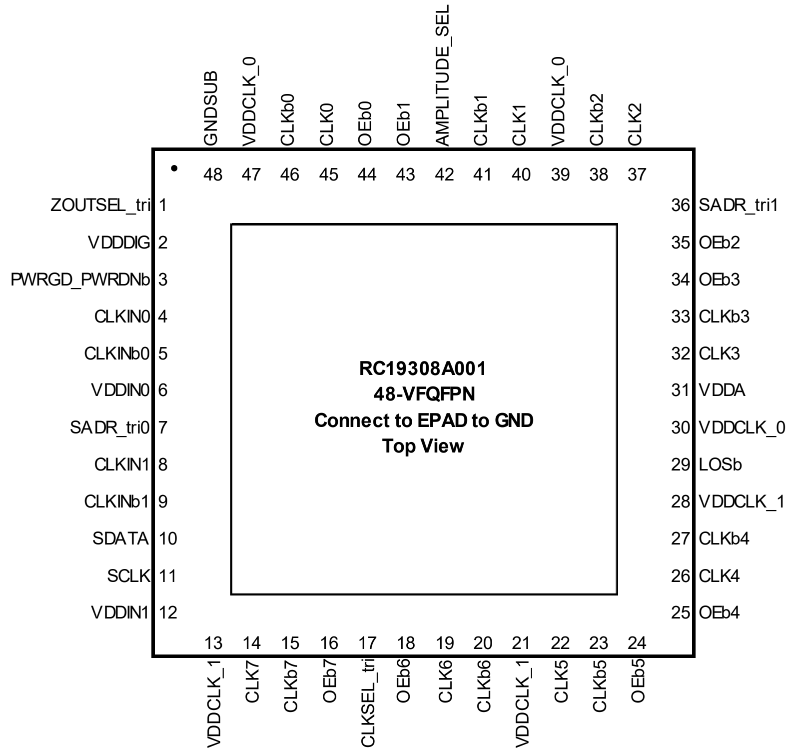


Figure 4. RC19308A001 Pin Assignments

1.3.2 RC19308 Pin Descriptions

Table 1. RC19308A/A001 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω, M = 34Ω,
2	VDDDIG	PWR	Digital power.
3	PWRGD_PWRDNb	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
4	CLKIN0	I, DIF	True clock input.
5	CLKINb0	I, DIF	Complementary clock input.
6	VDDIN0	PWR	Power supply for clock input 0.
7	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Selection (RC19308) table and refer to the tri-level input thresholds in the electrical tables.
8	CLKIN1	I, DIF	True clock input.
9	CLKINb1	I, DIF	Complementary clock input.
10	SDATA	I/O, SE, OD, PDT	Data pin for SMBus interface.
11	SCLK	I, SE, PDT	Clock pin of SMBus interface.
12	VDDIN1	PWR	Power supply for clock input 1.
13	VDDCLK_1	PWR	Power supply for clock output bank 1.
14	CLK7	O, DIF	True clock output.
15	CLKb7	O, DIF	Complementary clock output.
16	OEb7	I, SE, PU, PDT	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output.
17	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
18	OEb6	I, SE, PU, PDT	Active low input for enabling output 6. 0 = Enable output, 1 = Disable output.
19	CLK6	O, DIF	True clock output.
20	CLKb6	O, DIF	Complementary clock output.
21	VDDCLK_1	PWR	Power supply for clock output bank 1.
22	CLK5	O, DIF	True clock output.
23	CLKb5	O, DIF	Complementary clock output.
24	OEb5	I, SE, PU, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.
25	OEb4	I, SE, PU, PDT	Active low input for enabling output 4. 0 = Enable output, 1 = Disable output.
26	CLK4	O, DIF	True clock output.
27	CLKb4	O, DIF	Complementary clock output.
28	VDDCLK_1	PWR	Power supply for clock output bank 1.
29	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
30	VDDCLK_0	PWR	Power supply for clock output bank 0.
31	VDDA	PWR	Power supply for core multiplexer circuitry.
32	CLK3	O, DIF	True clock output.

Table 1. RC19308A/A001 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
33	CLKb3	O, DIF	Complementary clock output.
34	OEb3	I, SE, PU, PDT	Active low input for enabling output 3. 0 = Enable output, 1 = Disable output.
35	OEb2	I, SE, PU, PDT	Active low input for enabling output 2. 0 = Enable output, 1 = Disable output.
36	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Selection (RC19308) table and refer to the tri-level input thresholds in the electrical tables.
37	CLK2	O, DIF	True clock output.
38	CLKb2	O, DIF	Complementary clock output.
39	VDDCLK_0	PWR	Power supply for clock output bank 0.
40	CLK1	O, DIF	True clock output.
41	CLKb1	O, DIF	Complementary clock output.
42 (RC19308A)	SLEWRATE_SEL	I, SE, PU, PDT	Input to select default output slew rate. 0 = Slow slew rate. 1 = Fast slew rate.
42 (RC19308A001)	AMPLITUDE_SEL	I, SE, PD, PDT	Input to select output amplitude. The values are programmable with defaults listed below. See AMP_CTRL_DEF for default amplitude and AMP_CTRL_ALT for alternate amplitude. 0 = Select Default Amplitude (800mV), 1 = Select Alternate Amplitude (900mV)
43	OEb1	I, SE, PU, PDT	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output.
44	OEb0	I, SE, PU, PDT	Active low input for enabling output 0. 0 = Enable output, 1 = Disable output.
45	CLK0	O, DIF	True clock output.
46	CLKb0	O, DIF	Complementary clock output.
47	VDDCLK_0	PWR	Power supply for clock output bank 0.
48	GNDSUB	GND	Ground pin for substrate.
49	EPAD	PWR	Ground.

1.4 RC19304 Pin Information

1.4.1 RC19304 Pin Assignments

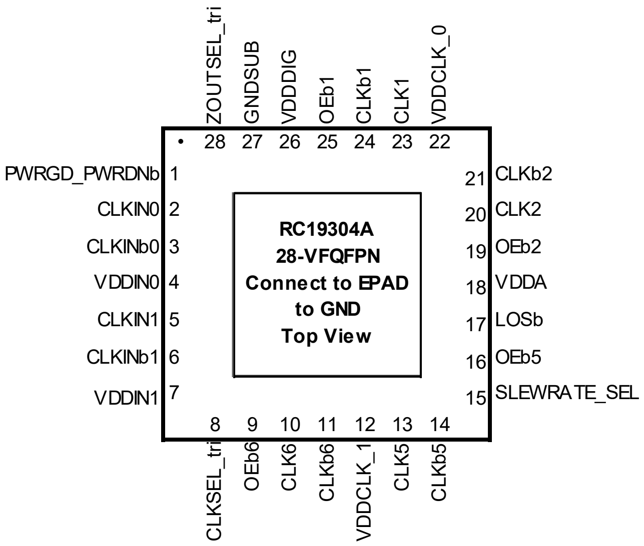


Figure 5. RC19304A Pin Assignments

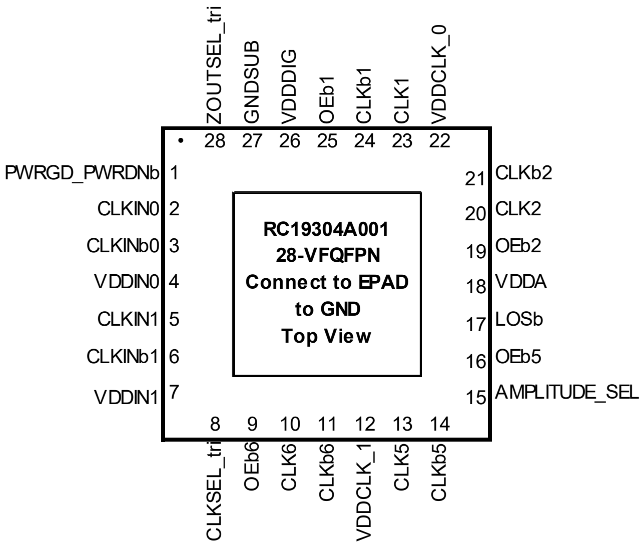


Figure 6. RC19304A001 Pin Assignments

1.4.2 RC19304 Pin Descriptions

Table 2. RC19304A/A001 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	PWRGD_PWRDNb	I, SE, PDT, PU	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
2	CLKIN0	I, DIF	True clock input.
3	CLKINb0	I, DIF	Complementary clock input.
4	VDDIN0	PWR	Power supply for clock input 0.
5	CLKIN1	I, DIF	True clock input.
6	CLKINb1	I, DIF	Complementary clock input.

Table 2. RC19304A/A001 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
7	VDDIN1	PWR	Power supply for clock input 1.
8	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
9	OEb6	I, SE, PU, PDT	Active low input for enabling output 6. 0 = Enable output, 1 = Disable output.
10	CLK6	O, DIF	True clock output.
11	CLKb6	O, DIF	Complementary clock output.
12	VDDCLK_1	PWR	Power supply for clock output bank 1.
13	CLK5	O, DIF	True clock output.
14	CLKb5	O, DIF	Complementary clock output.
15 (RC19304A)	SLEWRATE_SEL	I, SE, PU, PDT	Input to select default output slew rate. 0 = Slow slew rate. 1 = Fast slew rate.
15 (RC19304A001)	AMPLITUDE_SEL	I, SE, PD, PDT	Input to select output amplitude. The values are programmable with defaults listed below. See AMP_CTRL_DEF for default amplitude and AMP_CTRL_ALT for alternate amplitude. 0 = Select Default Amplitude (800mV), 1 = Select Alternate Amplitude (900mV)
16	OEb5	I, SE, PU, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.
17	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
18	VDDA	PWR	Power supply for analog circuitry.
19	OEb2	I, SE, PU, PDT	Active low input for enabling output 2. 0 = Enable output, 1 = Disable output.
20	CLK2	O, DIF	True clock output.
21	CLKb2	O, DIF	Complementary clock output.
22	VDDCLK_0	PWR	Power supply for clock output bank 0.
23	CLK1	O, DIF	True clock output.
24	CLKb1	O, DIF	Complementary clock output.
25	OEb1	I, SE, PU, PDT	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output.
26	VDDDIG	PWR	Digital power.
27	GNDSUB	GND	Ground pin for substrate.
28	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω, M = 34Ω,
29	EPAD	GND	Connect to ground.

1.5 RC19302 Pin Information

1.5.1 RC19302 Pin Assignments

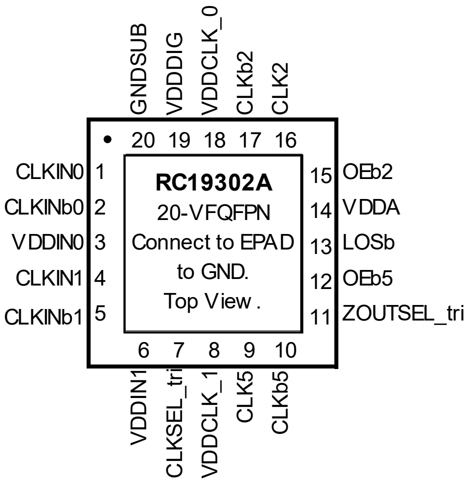


Figure 7. RC19302A Pin Assignments

1.5.2 RC19302 Pin Descriptions

Table 3. RC19302A Pin Descriptions

Pin Number	Pin Name	Type	Description
1	CLKIN0	I, DIF	True clock input.
2	CLKINb0	I, DIF	Complementary clock input.
3	VDDIN0	PWR	Power supply for clock input 0.
4	CLKIN1	I, DIF	True clock input.
5	CLKINb1	I, DIF	Complementary clock input.
6	VDDIN1	PWR	Power supply for clock input 1.
7	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
8	VDDCLK_1	PWR	Power supply for clock output bank 1.
9	CLK5	O, DIF	True clock output.
10	CLKb5	O, DIF	Complementary clock output.
11	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω, M = 34Ω,
12	OEb5	I, SE, PU, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.
13	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
14	VDDA	PWR	Power supply for analog circuitry.
15	OEb2	I, SE, PU, PDT	Active low input for enabling output 2. 0 = Enable output, 1 = Disable output.
16	CLK2	O, DIF	True clock output.
17	CLKb2	O, DIF	Complementary clock output.
18	VDDCLK_0	PWR	Power supply for clock output bank 0.
19	VDDDIG	PWR	Digital power.

Table 3. RC19302A Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
20	GNDSUB	GND	Ground pin for substrate.
21	EPAD	GND	Connect to ground.

2. Specifications

2.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin	-0.5	2.2	V
V_{IN}	Input Voltage for non-PDT inputs	Input pins not labeled as PDT [1]	-0.5	V_{DDx} + 0.3	V
V_{INPDT}	Input Voltage for PDT inputs	PDT input pins, see below for LOSb output pin [2]	-0.5	3.6	V
V_{PUPSMB}	Pull up resistor voltage for SMBus interface	SCLK, SDATA pins			V
V_{PUPLOS}	Pull up resistor voltage for LOSb pin	LOSb pin [3]	-0.5	1.9	V
I_{IN}	Input Current	All SE inputs and CLKIN [1]	-	±50	mA
I_{OUT}	Output Current – Continuous	CLK	-	30	mA
		SDATA	-	25	mA
	Output Current – Surge	CLK	-	60	mA
		SDATA	-	50	mA
T_J	Maximum Junction Temperature	-	-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
ESD	Human Body Model	JESD22-A114 (JS-001) Classification	-	2000	V
	Charged Device Model	JESD22-C101 Classification	-	500	V

1. Inputs not designated Power Down Tolerant (PDT) in the pin description tables.
2. Inputs designated Power Down Tolerant (PDT) in the pin description tables.
3. The V_{PUP} voltage may be applied before main VDD is applied. The LOSb pin is PDT to this voltage, not to 3.6V.

2.2 Recommended Operation Conditions

All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise. All conditions in this table must be met to guarantee device functionality and performance.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature		-	-	125	°C
T_A	Ambient Operating Temperature		-40	25	105	°C
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin, 1.8V ±5% supply.	1.7	1.8	1.9	V
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

2.3 Thermal Specifications

Table 6. Thermal Specifications

Package [1]	Symbol	Conditions	Typical Value (°C/W)
6 × 6 mm 48-VFQFPN (4.2 × 4.2 mm Epad)	θ_{Jc}	Junction to Case	28.5
	θ_{Jb}	Junction to Base	3.3
	θ_{JA0}	Junction to Air, still air	28.5
	θ_{JA1}	Junction to Air, 1 m/s air flow	25.4
	θ_{JA3}	Junction to Air, 3 m/s air flow	22.9
	θ_{JA5}	Junction to Air, 5 m/s air flow	21.8
4 × 4 mm 28-VFQFPN (2.6 × 2.6 mm Epad)	θ_{Jc}	Junction to Case	45.3
	θ_{Jb}	Junction to Base	2.2
	θ_{JA0}	Junction to Air, still air	36.3
	θ_{JA1}	Junction to Air, 1 m/s air flow	32.7
	θ_{JA3}	Junction to Air, 3 m/s air flow	31.0
	θ_{JA5}	Junction to Air, 5 m/s air flow	30.0
3 × 3 mm 20-VFQFPN (1.65 × 1.65 mm Epad)	θ_{Jc}	Junction to Case	96.3
	θ_{Jb}	Junction to Base	20.4
	θ_{JA0}	Junction to Air, still air	54.8
	θ_{JA1}	Junction to Air, 1 m/s air flow	51.1
	θ_{JA3}	Junction to Air, 3 m/s air flow	47.7
	θ_{JA5}	Junction to Air, 5 m/s air flow	46.2

1. Epad soldered to board.

2.4 Electrical Characteristics

2.4.1 Additive Phase Jitter

Table 7. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Unselected CLKIN Off) – Normal Conditions [1][2][3]

Symbol	Parameter	Condition	Typical	Maximum	Spec. Limit	Unit
$t_{\text{jphPCIeG1-CC}}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	418	658	86,000	fs p-p
$t_{\text{jphPCIeG2-CC}}$		PCIe Gen2 Hi Band (5.0 GT/s)	52	74	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	21	23	3,000	
$t_{\text{jphPCIeG3-CC}}$		PCIe Gen3 (8.0 GT/s)	18	25	1,000	
$t_{\text{jphPCIeG4-CC}}$		PCIe Gen4 (16.0 GT/s) [4][5]	18	25	500	
$t_{\text{jphPCIeG5-CC}}$		PCIe Gen5 (32.0 GT/s) [4] [6]	6.9	9.8	150	
$t_{\text{jphPCIeG6-CC}}$		PCIe Gen6 (64.0 GT/s) [4] [7]	4.1	5.8	100	
$t_{\text{jphPCIeG7-CC}}$		PCIe Gen7 (128 GT/s) [4][8]	2.9	4.0	67	
$t_{\text{jphPCIeG2-IR}}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	47	60	[9]	fs RMS
$t_{\text{jphPCIeG3-IR}}$		PCIe Gen3 (8.0 GT/s)	18	24		
$t_{\text{jphPCIeG4-IR}}$		PCIe Gen4 (16.0 GT/s) [3] [4]	19	25		
$t_{\text{jphPCIeG5-IR}}$		PCIe Gen5 (32.0 GT/s) [3] [5]	5.1	6.9		
$t_{\text{jphPCIeG6-IR}}$		PCIe Gen6 (64.0 GT/s) [3] [7]	3.7	4.9		
$t_{\text{jphPCIeG7-IR}}$		PCIe Gen7 (128 GT/s) [3][7]	2.6	3.4		

1. The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
5. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 8. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Unselected CLKIN Off) – Degraded Conditions [1][2][3]

Symbol	Parameter	Condition	Typical	Maximum	Spec. Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	358	669	86,000	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	50	79	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	18	24	3,000	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	17	27	1,000	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [4][5]	17	27	500	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [4] [6]	6.6	10.5	150	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [4] [7]	3.9	6.2	100	
$t_{jphPCIeG7\text{-}CC}$		PCIe Gen7 (128 GT/s) [4][8]	2.7	4.3	67	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	42	65	[9]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	16	26		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3] [4]	17	27		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3] [5]	4.8	7,5		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3] [7]	3.4	5.3		
$t_{jphPCIeG7\text{-}IR}$		PCIe Gen7 (128 GT/s) [3][7]	2.4	3.7		

1. The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 800mV and input slew rate ≥ 1.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
5. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 9. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Both CLKIN Running at Different Frequencies) – Normal Conditions [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Spec. Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	3268	7151	86,000	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	189	482	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	321	657	3,000	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	85	167	1,000	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [5][6]	85	167	500	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [4][7]	24	50	150	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [4][8]	18	35	100	
$t_{jphPCIeG7\text{-}CC}$		PCIe Gen7 (128 GT/s) [4][9]	13	25	67	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	384	757	[10]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	121	242		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	129	257		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	28	59		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][7]	26	50		
$t_{jphPCIeG7\text{-}IR}$		PCIe Gen7 (128 GT/s) [3][7]	18	36		

1. The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
4. One input clock at 100MHz, the other input clock at 99.75MHz, 100MHz clock measured.
5. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
6. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
10. The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 10. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Both CLKIN Running at Different Frequencies) – Degraded Conditions [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Spec. Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	3230	5491	86,000	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	159	343	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	345	546	3,000	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	86	131	1,000	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [5][6]	86	131	500	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [4][7]	24	39	150	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [4][8]	19	28	100	
$t_{jphPCIeG7\text{-}CC}$		PCIe Gen7 (128 GT/s) [4][9]	13	20	67	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	390	594	[10]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	123	190		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	131	202		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	28	46		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][7]	26	39		
$t_{jphPCIeG7\text{-}IR}$		PCIe Gen7 (128 GT/s) [3][7]	18	28		

1. The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 800mV and input slew rate ≥ 1.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
4. One input clock at 100MHz, the other input clock at 99.75MHz, 100MHz clock measured.
5. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
6. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
10. The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 11. PCIe Refclk Phase Jitter (CLKSEL_tri = M, Both CLKIN Running at Different Frequencies) – Normal Conditions [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Spec. Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	3804	7971	86,000	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	224	512	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	359	727	3,000	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	96	189	1,000	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [5][6]	96	189	500	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [4][7]	27	55	150	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [4][8]	21	39	100	
$t_{jphPCIeG7\text{-}CC}$		PCIe Gen7 (128 GT/s) [4][9]	15	28	67	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	436	853	[10]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	138	272		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	147	289		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	32	66		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][7]	29	56		
$t_{jphPCIeG7\text{-}IR}$		PCIe Gen7 (128 GT/s) [3][7]	21	40		

1. The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0 For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
4. One input clock at 100MHz, the other input clock at 99.75MHz, 100MHz clock measured.
5. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
6. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
10. The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 12. PCIe Refclk Phase Jitter (CLKSEL_tri = M, Both CLKIN Running at Different Frequencies) – Degraded Conditions [1][2][3][4]

Symbol	Parameter	Condition	Typical	Maximum	Spec. Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	3658	5827	86,000	fs p-p
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	199	327	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	375	609	3,000	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	96	141	1,000	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [5][6]	96	141	500	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [4][7]	27	41	150	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [4][8]	21	29	100	
$t_{jphPCIeG7\text{-}CC}$		PCIe Gen7 (128 GT/s) [4][9]	15	21	67	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	434	636	[10]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	137	202		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	145	215		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	32	49		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][7]	29	42		
$t_{jphPCIeG7\text{-}IR}$		PCIe Gen7 (128 GT/s) [3][7]	21	30		

1. The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 800mV and input slew rate ≥ 1.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
4. One input clock at 100MHz, the other input clock at 99.75MHz, 100MHz clock measured.
5. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
6. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
10. The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

2.4.2 Other Phase Jitter

Table 13. Non-PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Unselected CLKIN Off) [1][2][3]

Symbol	Parameter	Conditions	Typical	Maximum	Spec. Limit	Unit
$t_{jphDB2000Q}$	Additive Phase Jitter	100MHz, Intel-supplied filter [3][4]	11.5	12.8	80 [5]	fs RMS
		100MHz, Intel-supplied filter [3][6]		13.7	80 [5]	
$t_{jph12k\text{-}20M}$	Additive Phase Jitter	156.25MHz (12kHz to 20MHz) [4]	42.8	45.7	N/A	
		156.25MHz (12kHz to 20MHz) [6]		52.5	N/A	

1. See Test Loads for test configuration. Measured with one input at 100MHz and the other at 156.25MHz.
2. SMA100B used as signal source.
3. The RC19xxx devices meet all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
4. Differential input swing = 1600mV and input slew rate = 3.5V/ns
5. The rms sum of the source jitter and the additive jitter must be less than the jitter specification listed.
6. Differential input swing = 800mV and input slew rate = 1.5V/ns

Note: Dual-mode operation (CLKSEL_tri = M, both CLKIN running) is recommended only for PCIe applications.

2.4.3 Output Frequencies, Startup Time, and LOS Timing

Table 14. Output Frequencies, Startup Time, and LOS Timing

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{OP}	Operating Frequency	Automatic Clock Parking (ACP) Circuit disabled.	1	-	400	MHz
		Automatic Clock Parking (ACP) Circuit enabled.	25	-	400	
$t_{STARTUP}$	Start-up Time	[1]	-	0.5	1.6	ms
		[2]	-	70	85	ns
t_{LATOEb}	OEb Latency	OEb assertion/de-assertion CLK start/stop latency. Selected input clock must be running.	4	5	6	clks
$t_{LOSAssert}$	LOS Assert Time	Time from disappearance of selected input clock to LOS assert. [3][4]	-	244	289	ns
$t_{LOSDeassert}$	LOS De-assert Time	Time from appearance of selected input clock to LOS de-assert. [2][5]	6	-	7	clks

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. PWRGD_PGWRDNb tied to VDD in this case.
2. VDD stable, measured from de-assertion of PWRGD_PWRDNb.
3. The clock detect circuit does not qualify the accuracy of the input clock.
4. PWRGD_PWRDNb high. The clock detect circuit will park the outputs in a low/low state within this time.
5. PWRGD_PWRDNb high. The clock detect circuit will drive the outputs to a high/low state within this time and then begin clocking the outputs.

2.4.4 CLK (LP-HCSL) AC/DC Output Characteristics

Table 15. 85Ω CLK AC/DC Characteristics – Source-Terminated 100MHz PCIe Applications [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Spec. Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1066	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-216	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	703	837	960	-	mV
V_{LOW}	Voltage Low [3]		-200	-91	26	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 800mV, scope averaging off.	349	415	486	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		-	26	30	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.	1.9	2.8	3.9	1.8 to 4	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.	1.6	2.4	3.4	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Fast slew rate.	-	2.9	12.5	20	%
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Slow slew rate.	-	2.7	10.5		
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	774	920	1052	-	mV
V_{LOW}	Voltage Low [3]		-215	-98	28	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 900mV, scope averaging off.	371	445	526	300 to 600	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		-	26	31	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, Fast slew rate, scope averaging on.	2.0	3.0	4.1	2 to 5	V/ns
		V_{HIGH} set to 900mV, Slow slew rate, scope averaging on.	1.6	2.5	3.6	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Fast slew rate.	-	3.1	11.7	20	%
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Slow slew rate.	-	3.5	15.0	20	%
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	49.5	50.1	50.6	45 to 55	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. The specification limits are taken from either the PCI Express Base Specification 7.0 or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 16. 100 ohm CLK AC/DC Characteristics – Source-Terminated, PCIe Applications [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Spec. Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1075	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-170	-137	-101	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	811	871	926	-	mV
V_{LOW}	Voltage Low [3]		-140	-105	-64	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 800mV, scope averaging off.	346	443	543	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		21	25	30	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.	2.4	3.3	4.2	2 to 4	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.	1.8	2.6	3.4	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Fast slew rate.	-	8.2	18.6	20	%
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Slow slew rate.	-	14.2	19.7	20	%
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	896	967	1030	-	mV
V_{LOW}	Voltage Low [3]		-150	-113	-71	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 900mV, scope averaging off.	388	485	584	300 to 600	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		21	25	30	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, Fast slew rate, scope averaging on.	2.5	3.5	4.5	2 to 4	V/ns
		V_{HIGH} set to 900mV, Slow slew rate, scope averaging on.	1.9	2.7	3.6	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Fast slew rate.	-	8	17.8	20	%
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Slow slew rate.	-	12	19.5	20	%
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	49.5	50.0	50.5	45 to 55	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. The specification limits are taken from either the PCI Express Base Specification 7.0 or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 17. 85 ohm CLK AC/DC Characteristics – Source-Terminated, Non-PCIe Applications[1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	645	812	989	mV
V_{OL}	Output Low Voltage [2]		-220	-41	39	
V_{CROSS}	Crossing Voltage (abs) [3]		275	376	471	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	32	
t_R	Rise Time [2] VT = 20% to 80% of swing		290	429	601	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		271	422	623	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	739	872	1094	mV
V_{OL}	Output Low Voltage [2]		-236	-44	43	
V_{CROSS}	Crossing Voltage (abs) [3]		285	391	475	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	31	
t_R	Rise Time [2] VT = 20% to 80% of swing		308	524	729	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		311	476	625	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48.1	50.0	51.8	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 18. 100 ohm CLK AC/DC Characteristics - Source-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	636	837	958	mV
V_{OL}	Output Low Voltage [2]		-165	-52	49	
V_{CROSS}	Crossing Voltage (abs) [3]		285	420	571	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	32	
t_R	Rise Time [2] VT = 20% to 80% of swing		285	390	494	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		279	421	593	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	732	908	1070	mV
V_{OL}	Output Low Voltage [2]		-183	31	52	
V_{CROSS}	Crossing Voltage (abs) [3]		325	405	598	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	47	33	
t_R	Rise Time [2] VT = 20% to 80% of swing		383	491	592	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		334	462	579	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48.2	49.9	51.6	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. Measured from single-ended waveform.

3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 19. 85 ohm CLK AC/DC Characteristics – Double-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	382	410	436	mV
V_{OL}	Output Low Voltage [2]		-8	13	33	
V_{CROSS}	Crossing Voltage (abs) [3]		186	206	226	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-9	8	25	
t_R	Rise Time [2] VT = 20% to 80% of swing		256	368	491	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		225	307	417	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	415	448	480	mV
V_{OL}	Output Low Voltage [2]		-6	14	35	
V_{CROSS}	Crossing Voltage (abs) [3]		192	216	239	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-9	8	27	
t_R	Rise Time [2] VT = 20% to 80% of swing		289	418	558	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		227	302	406	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48.6	49.6	50.5	%

1. Both Tx and Rx are terminated (double-terminated) with CL= 2pF. This reduces amplitude by 50%. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 20. 100 ohm CLK AC/DC Characteristics – Double-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz)	399	428	456	mV
V_{OL}	Output Low Voltage [2]		-7	13	34	
V_{CROSS}	Crossing Voltage (abs) [3]		200	228	256	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-12	7	30	
t_R	Rise Time [2] VT = 20% to 80% of swing		196	272	358	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		214	293	388	ps

Table 20. 100 ohm CLK AC/DC Characteristics – Double-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	438	474	510	mV
V_{OL}	Output Low Voltage [2]		-7	14	36	
V_{CROSS}	Crossing Voltage (abs) [3]		218	247	276	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-13	7	31	
t_R	Rise Time [2] VT = 20% to 80% of swing		203	301	408	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		207	278	369	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48.6	49.6	50.6	%

1. Both Tx and Rx are terminated (double-terminated) with CL= 2pF. This reduces amplitude by 50%. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 21. 34ohm CLK AC/DC Characteristics – Rx-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz)	554	601	650	mV
V_{OL}	Output Low Voltage [2]		-3	19	40	
V_{CROSS}	Crossing Voltage (abs) [3]		281	316	352	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-21	11	42	
t_R	Rise Time [2] VT = 20% to 80% of swing		130	266	404	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		133	316	500	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	564	629	695	mV
V_{OL}	Output Low Voltage [2]		-3	19	40	
V_{CROSS}	Crossing Voltage (abs) [3]		290	331	372	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-22	11	45	
t_R	Rise Time [2] VT = 20% to 80% of swing		122	262	404	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		124	310	501	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48.6	49.5	50.4	%

1. ZOUTSEL_tri = M. This setting turns off the source termination, provided approximately 75% of the source-terminated amplitude at the receiver with C_L= 2pF. For more information, see Figure 10. This setting intends to provide >500mV single-ended swing into a receiver terminated load.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

2.4.5 CLKIN AC/DC Characteristics

Table 22. CLKIN AC/DC Characteristics for DC-Coupled Operation[1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IHMAX}	Maximum Input Voltage	Single-ended value.	-	-	1.2	V
V_{CROSS}	Input Crossover Voltage	LOW_LOW_DETECT enabled (default value). [2]	131	-	-	mV
		LOW_LOW_DETECT disabled.	100	-	-	mV
V_{SWING}	Input Swing [3]	LOW_LOW_DETECT enabled (default value). [2]	528	-	-	mV
		LOW_LOW_DETECT disabled.	200	-	-	mV
dv/dt	Input Slew Rate [3][4]	-	0.6	-	-	V/ns

1. See the Additive Phase Jitter tables for values required for performance. The CLKIN is designed for a ground-referenced differential input where the cross over voltage is approximately half of the swing. For example, a differential clock with a VOH of 1.2V would ideally have a crossover voltage of approximately 600mV. For applications where the input clock is not ground-referenced (LVPECL for example), the input clock needs to be AC-coupled and re-biased. Each RC193xx CLKIN has an internal bias circuit that may be enabled as well as internal terminations that may also be enabled. This reduces external components for such scenarios to a single external AC-coupling capacitor. See the RECEIVER_CONTROL register for details.
2. Low/Low is an invalid differential state. LOW_LOW_DETECT allows the receiver turn itself off when such a condition is detected
3. Differential value.
4. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

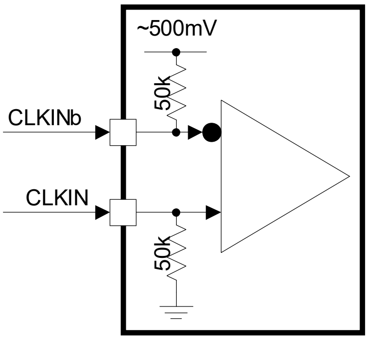


Figure 8. Clock Input Bias Network

2.4.6 Skew

Table 23. Output-to-Output and Input-to-Output Skew [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2]	Any two outputs in the same Bank.	-	14	50	ps
		Any two outputs regardless of Bank.[3]	-	25	60	ps
t_{PD}	Input-to-Output Delay [4]	Clock in to any output. Double-terminated.	0.9	1.1	1.3	ns
		Clock in to any output. Source-terminated.	0.9	1.1	1.7	ns
Δt_{PD}	Input-to-Output Delay Variation [3]	A single device, over temperature and voltage.	-	1.3	2	ps/°C

1. See Test Loads.
2. This parameter is defined in accordance with JEDEC Standard 65.
3. Output banks sourced from the same input. CLKSEL_tri = 0 or 1.
4. Defined as the time between to output rising edge and the input rising edge that caused it.

2.4.7 I/O Electrical Characteristics

Table 24. I/O Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage [1][2]	Single-ended inputs, unless otherwise listed.	0.65 × VDD	-	VDD + 0.3	V
V_{IL}	Input Low Voltage [1][2]		-0.3	-	0.35 × VDD	V
V_{IH}	Input High Voltage	SADR_tri[1:0].	0.75 × VDD	-	VDD + 0.3	V
V_{IM}	Input Mid Voltage		0.45 × VDD	0.5 × VDD	0.55 × VDD	V
V_{IL}	Input Low Voltage		-0.3	-	0.25 × VDD	V
V_{OL}	Output Low Voltage	LOSb, I_{OL} = 2mA.	-	0.1	0.4	V
I_{IH}	Input Leakage Current High, V_{IN} = VDD	CLKIN	5	-	15	µA
		CLKINb	-3	-	+3	
		PWRGD_PWRDNb	-35	-	-20	
		SADR_tri[1:0]	25	-	35	
		Single-ended inputs not otherwise listed	25	-	35	
I_{IL}	Input Leakage Current Low, V_{IN} = 0V	CLKIN	-3	-	+3	µA
		CLKINb	-12	-	-6	
		PWRGD_PWRDNb	-35	-	-20	
		SADR_tri[1:0]	-35	-	-20	
		Single-ended inputs not otherwise listed	-35	-	-20	
Rp	PD_CLKIN	Value of internal pull-down resistor to ground (CLKIN)	-	53	-	kΩ
	PU_CLKINb	Value of internal pull-up resistor to 0.5V (CLKINb).	-	57	-	
	Pull-up/Pull-down Resistor	Single-ended inputs.	-	125	-	
Zo	Output Impedance	CLK/CLKb single-ended impedance, 85Ω setting	-	34	-	Ω
		CLK/CLKb single-ended impedance, 100Ω setting	-	39	-	
		CLK/CLKb single-ended impedance, 34Ω setting	-	14	-	

1. For SCLK and SDATA, see Table 26.
2. These values are compliant with JESD8-7A 1.8V Normal Range.

2.4.8 Power Supply Current

Table 25. Power Supply Current [1][2][3]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDCLK_X}	V_{DDCLK_X} Operating Current per Output Pair, 100Ω impedance [4]	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	8.5	9.0	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	10.0	10.5	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	10.8	11.1	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	13.0	13.4	

Table 25. Power Supply Current [1][2][3] (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDCLK_X}	V_{DDCLK_X} Operating Current per Output Pair, 85Ω impedance [4]	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	9.8	10.4	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	11.5	12.1	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	12.4	12.8	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	15.0	15.4	
I_{DDCLK_X}	V_{DDCLK_X} Operating Current per Output Pair, 34Ω impedance [4]	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	9.2	10.1	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	14.5	15.5	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	15.4	16.3	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	21.2	21.6	
		Fast slew rate, receiver-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	21.2	21.6	
$I_{DDCLK\_CORE\_X}$	V_{DDCLK_X} Core Operating Current, per V_{DDCLK_X}, all Outputs Disabled	PWRGD_PWRDNb = 1, all outputs disabled, CLKIN = 100MHz.	-	2.2	2.7	mA
		PWRGD_PWRDNb = 1, all outputs disabled, CLKIN = maximum operating frequency.	-	5.8	7.2	
I_{DDINx}	V_{DDINx} Operating Current	Deselected input channel, per VDDIN pin. PWRGD_PWRDNb = 1.	-	1.7	2.1	mA
		Selected input channel, per VDDIN pin. PWRGD_PWRDNb = 1.	-	11.1	14.3	mA
I_{DDDIG}	V_{DDDIG} Current	PWRGD_PWRDNb = 0 or 1.	-	0.12	0.18	mA
I_{DDA}	V_{DDA} Current	Core logic supply, independent of either bank. PWRGD_PWRDNb = 0 or 1.	-	0.3	0.32	mA
$I_{DDINxPD}$	V_{DDINX} Power-down Current per I_{DDINX} pin.	PWRGD_PWRDNb = 0 (does not apply to RC19302).	-	1.6	2.1	mA
I_{DDCLK_xPD}	V_{DDCLK_x} Power-down Current per output bank [5]	PWRGD_PWRDNb = 0 (does not apply to RC19302).	-	1.8	2	mA

1. See Test Loads.
2. Output voltage set to 800mV. Slew rate has negligible effect on current consumption, so only fast is listed.
3. Total operating current is obtained by adding (I_{DDCLK} x number of outputs used) + $I_{DDCLK\_CORE\_0}$ + $I_{DDCLK\_CORE\_1}$ + I_{DDIN0} + I_{DDIN1} + I_{DDA} + I_{DDDIG}. For example, let's assume that the RC19308 is being used at 100MHz with 100ohm source terminated outputs and that only six outputs are used. CLKIN1 is selected. The typical operating current would be I_{DDCLK} x 6 + I_{DDCLK_CORE0} + I_{DDCLK_CORE0} + I_{DDIN0} + I_{DDIN1} + I_{DDA} + I_{DDDIG} or (8.5 x 6)mA + 2.2mA + 2.2mA + 1.7mA + 11.1mA + 0.3mA + 0.14mA = 68.6mA typical. *Note*: VDDCLK_0 serves CLK[3:0]. VDDCLK_1 serves CLK[7:4]. Total power down current is obtained by adding I_{DDCLK_0PD} + I_{DDCLK_1PD} + $I_{DDIN0PD}$ + $I_{DDIN1PD}$ + I_{DDDIG_PD} + I_{DDA}.
4. The value specified is for one output pair. Multiply this value by the number of outputs in use.
5. On the RC19308, bank 0 is powered by 3 VDDCLK_0 pins and bank 1 is powered by 3 VDDCLK_1 pins. This value is the total current per output bank, *not per VDDCLK pin.* This parameter needs to be counted only twice.

2.4.9 SMBus Electrical Characteristics

Table 26. SMBus DC Electrical Characteristics [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	High-level Input Voltage for SCLK and SDATA	VDD = 1.8V	0.8 VDD	-	3.6	V
V_{IL}	Low-level Input Voltage for SCLK and SDATA	VDD = 1.8V	-	-	0.3 VDD	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	-	0.05 VDD	-	-	
V_{OL}	Low-level Output Voltage for SCLK and SDATA	I_{OL} = 4mA	-	0.28	0.4	
I_{IN}	Input Leakage Current per Pin	-	[2]	-	[2]	µA
C_B	Capacitive Load for Each Bus Line	-	-	-	400	pF

1. V_{OH} is governed by the V_{PUP}, the voltage rail to which the pull-up resistors are connected. The maximum V_{PUP} voltage is 3.6V.
2. See I/O Electrical Characteristics.

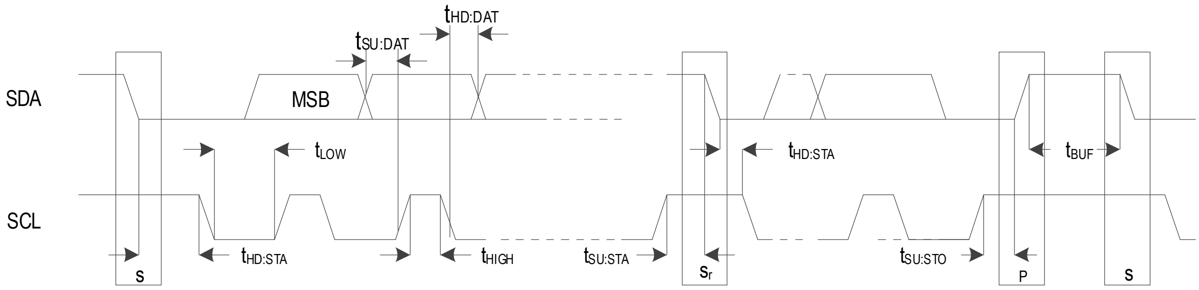


Figure 9. SMBus Target Timing Diagram

Table 27. SMBus AC Electrical Characteristics

Symbol	Parameter	Conditions	100kHz Class		Unit
			Minimum	Maximum	
f_{SMB}	SMBus Operating Frequency	[1]	10	100	kHz
t_{BUF}	Bus free time between STOP and START Condition	-	4.7	-	µs
$t_{HD:STA}$	Hold Time after (REPEATED) START Condition	[2]	4	-	µs
$t_{SU:STA}$	REPEATED START Condition Setup Time	-	4.7	-	µs
$t_{SU:STO}$	STOP Condition Setup Time	-	4	-	µs
$t_{HD:DAT}$	Data Hold Time	[3]	0	-	ns
$t_{SU:DAT}$	Data Setup Time	-	250	-	ns
$t_{TIMEOUT}$	Detect SCL_SCLK Low Timeout	[4]	25	35	ms
$t_{TIMEOUT}$	Detect SDA_nCS Low Timeout	[5]	25	35	ms
t_{LOW}	Clock Low Period	-	4.7	-	µs
t_{HIGH}	Clock High Period	[6]	4	50	µs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time (target [slave] device)	[7]	N/A. The RC193xx does not extend the clock.		ms
$t_{LOW:MEXT}$	Cumulative Clock Low Extend Time (host [master] device)	[8]	N/A. The RC193xx is not a host device.		ms
t_F	Clock/Data Fall Time	[9]	-	300	ns
t_R	Clock/Data Rise Time	[9]	-	1000	ns
t_{SPIKE}	Noise Spike Suppression Time	[10]	-	-	ns

1. Power must be applied and PWRGD_PWRDNb must be a 1 for the SMBus to be active.

2. A host should not drive the clock at a frequency below the minimum f_{SMB}. Further, the operating clock frequency should not be reduced below the minimum value of fSMB due to periodic clock extending by target devices as defined in Section 5.3.3 of System Management Bus (SMBus) Specification, Version 3.2, dated 12 Jan, 2022. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW: SEXT}$ and $t_{LOW: MEXT}$ limits. For example, if the SCLK is high for $t_{HIGH,MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB,MIN} – t_{HIGH,MAX}$. This requirement does not pertain to a device that extends the SCLK low for data processing of a received byte, data buffering and so forth for longer than 100 µs in a non-periodic way.
3. A device must internally provide sufficient hold time for the SDATA signal (with respect to the VIH,MIN of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.
4. Target devices may have caused other target devices to hold SDA low. This is the maximum time that a device can hold SDATA low after the host raises SCLK after the last bit of a transaction. A target device may detect how long SDA is held low and release SDA after the time out period.
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the host in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can host the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SCLK low for $t_{TIMEOUT,MAX}$ or longer.
6. The device has the option of detecting a timeout if the SDATAA pin is also low for this time.
7. $t_{HIGH,MAX}$ provides a simple guaranteed method for hosts to detect bus idle conditions. A host can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.
8. $t_{LOW:MEXT}$ is the cumulative time a host device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a target device or another host will also extend the clock causing the combined clock low time to be greater than tLOW:MEXT on a given byte. This parameter is measured with a full speed target device as the sole target of the host.
9. The rise and fall time measurement limits are defined as follows:
   - Rise Time Limits: ($V_{IL:MAX}$ - 0.15 V) to ($V_{IH:MIN}$ + 0.15 V)
   - Fall Time Limits: ($V_{IH:MIN}$ + 0.15 V) to ($V_{IL:MAX}$ - 0.15 V)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

3. Test Loads

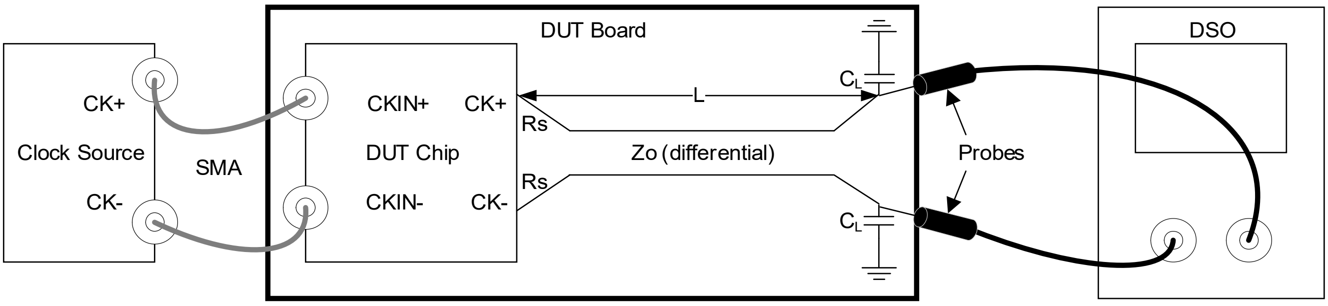


Figure 10. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

Table 28. Parameters for AC/DC Test Load (Standard PCIe Source-Terminated)

Clock Source	L (cm)	C_L (pF)	ZOUTSEL_tri pin	Zo (ohms)	Rs (ohms)
SMA100B	25.4	2	0 (85 ohms)	85	Internal
			1 (100 ohms)	100	Internal
			Mid (34 ohms)	85	External 25.5
				100	External 33.3

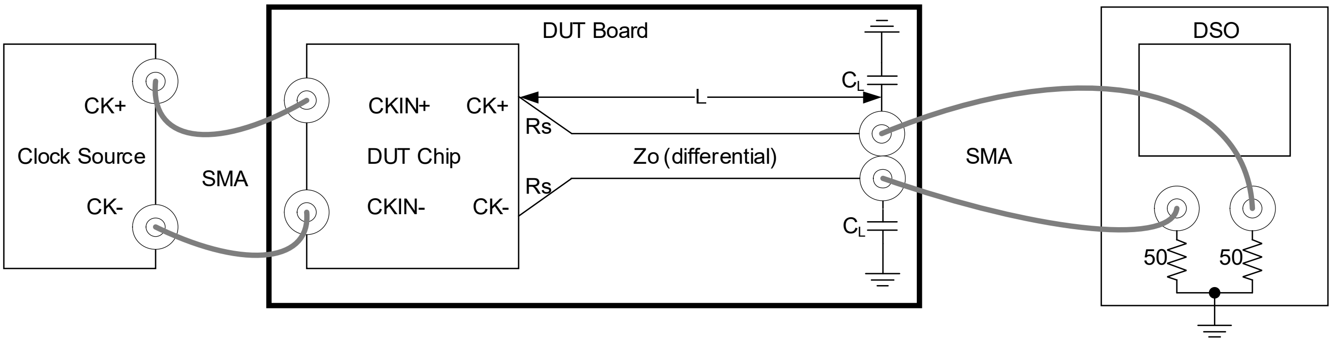


Figure 11. AC/DC Test Load for Differential Outputs (Double-Terminated or Receiver-Terminated)

Table 29. Parameters for AC/DC Test Load (Double-Terminated)

Clock Source	L (cm)	C_L (pF)	ZOUTSEL_tri pin	Zo (ohms)	Rs (ohms)
SMA100B	25.4	2	0 (85 ohms)	85	Internal
			1 (100 ohms)	100	Internal
			Mid (34 ohms)	85	None[1]
				100	

1. This setting is designed to provide additional amplitude for receiver-terminated loads by turning off the source termination in the output driver. There is no reflection with receiver terminated loads since the receiver termination absorbs the incident waveform.

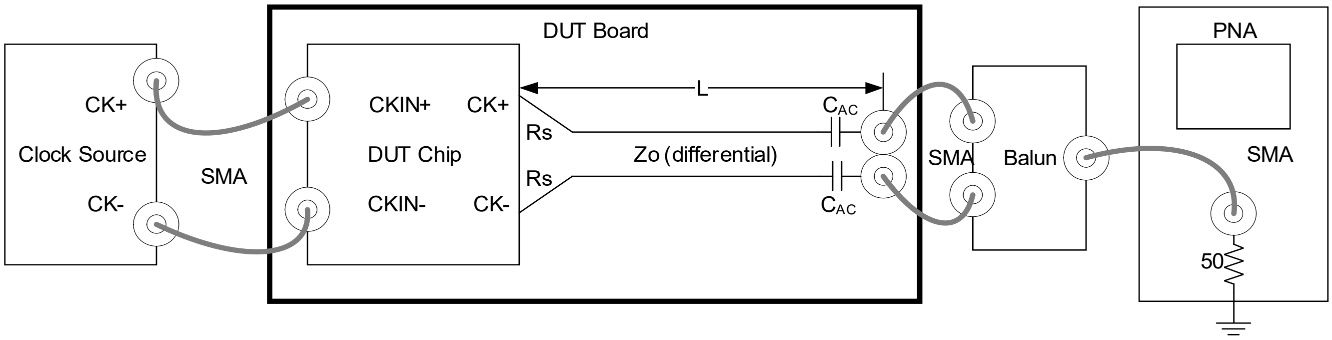


Figure 12. Test Load for PCIe Phase Jitter Measurements

Table 30. Parameters for PCIe Jitter Measurement

Clock Source	L (cm) [1]	C_{AC} (uF)	ZOUTSEL_tri pin	Zo (ohms)	Rs (ohms)
SMA100B	25.4	0.1	0 (85 ohms)	85	Internal
			1 (100 ohms)	100	Internal
			Mid (34 ohms)		None

1. PCIe Gen5-7 specify L = 0cm for 32, 64 and 128GT/s. L = 25.4cm is more conservative.

4. General SMBus Serial Interface Information

4.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte Location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte one at a time
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas**
T	starT bit		
Target Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

4.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte Location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte L through Byte X (if X(H) was written to Byte 7)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas**
T	starT bit		
Target Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Target Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not		
P	stoP bit		

4.3 Write Lock Functionality (RC19308)

WRITE_LOCK	WRITE_LOCK RW1C	SMBus Write Protect
0	0	No
0	1	Yes
1	0	Yes
1	1	Yes

4.4 SMBus Address Selection (RC19308)

Device	Address Selection		Binary Value								Hex Value	
	SADR_TRI1	SADR_TRI0	7	6	5	4	3	2	1	Rd/Wrt		
RC19308	0	0	1	1	0	1	0	1	1	0	D6	Standard Addresses
		M	1	1	0	1	1	0	0	0	D8	
		1	1	1	0	1	1	0	1	0	DA	
	M	0	1	1	0	0	0	1	1	0	C6	
		M	1	1	0	0	1	0	0	0	C8	
		1	1	1	0	0	1	0	1	0	CA	
	1	0	1	0	1	0	0	1	1	0	A6	
		M	1	0	1	0	1	0	0	0	A8	
		1	1	0	1	0	1	0	1	0	AA	

4.5 SMBus Registers

Table 31. Register Index

Offset (Hex)	Offset (Decimal)	Register Module Base Address: 0x0	
		Register Name	Register Description
0x0	0	OUTPUT_ENABLE	Output Enable Register
0x3	3	OEB_PIN_READBACK	OEb Pin Read-back Register
0x4	4	LOS_CONFIG	Loss of Signal and Async Mode Configuration Register
0x5	5	VENDOR_REVISION_ID	Vendor ID, Revision ID Register
0x6	6	DEVICE_ID	Device ID Register
0x7	7	BYTE_COUNT	Number of Bytes Returned on an SMBus Block Read
0xA	10	SLEW_AMP_SELECT	Multifunction Pin Configuration Register
0xE	14	INPUT_PULLUP_PULLDOWN_4	Internal Pull-up / Pull-down Configuration Register
0x10	16	AMP_CTRL_ALT	Alternate Amplitude Selection Register
0x11	17	AMP_CTRL_DEF	Default Amplitude Selection Register
0x12	18	PD_RESTORE_LOSb_CONFIG	Configuration and Status Register
0x14	20	OUTPUT_IMPEDANCE_7_0	Output Impedance Select Register 0
0x15	21	OUTPUT_REC_SEL_7_0	Output Impedance Select Register 1
0x16	22	OUTPUT_SLEW_RATE_7_0	Output Slew Rate Select Register
0x20	32	LOW_LOW_DETECT	CLKIN Low-Low Detect Enable Register
0x23	35	RECEIVER_CONTROL	CLKIN Configuration Register
0x26	38	WRITE_LOCK	Non-clearable SMBus Write Lock Register
0x27	39	WRITE_LOCK_LOS_EVT	Clearable SMBus Write Lock and LOS Event Register

4.5.1 OUTPUT_ENABLE

Output Enable Register.

OUTPUT_ENABLE Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	clk7_en	RW	0x1	CLK7 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
6	clk6_en	RW	0x1	CLK6 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
5	clk5_en	RW	0x1	CLK5 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
4	clk4_en	RW	0x1	CLK4 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
3	clk3_en	RW	0x1	CLK3 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
2	clk2_en	RW	0x1	CLK2 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
1	clk1_en	RW	0x1	CLK1 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
0	clk0_en	RW	0x1	CLK0 enable. 0 = Output is disabled (low/low) 1 = Output is enabled

4.5.2 OEB_PIN_READBACK

OEb Pin Read-back Register.

OEB_PIN_READBACK Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	rb_oeb_7	RO	0x0	State of OEb7 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
6	rb_oeb_6	RO	0x0	State of OEb6 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
5	rb_oeb_5	RO	0x0	State of OEb5 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
4	rb_oeb_4	RO	0x0	State of OEb4 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
3	rb_oeb_3	RO	0x0	State of OEb3 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
2	rb_oeb_2	RO	0x0	State of OEb2 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high

OEB_PIN_READBACK Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
1	rb_oeb_1	RO	0x0	State of OEb1 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
0	rb_oeb_0	RO	0x0	State of OEb0 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high

4.5.3 LOS_CONFIG

Loss of Signal and Async Mode Configuration Register.

LOS_CONFIG Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	los1b_rw1c_en	RW	0x1	LOS sticky bit enable for CLKIN1. Enables the CLKIN1 LOS sticky bit (B0x27[1]). This bit must be set to 1 if B0x4[2] is set to 0. 0 = Disable 1 = Enable
6	los0b_rw1c_en	RW	0x1	LOS sticky bit enable for CLKIN0. Enables the CLKIN0 LOS sticky bit (B0x27[1]). This bit must be set to 1 if B0x4[2] is set to 0. 0 = Disable 1 = Enable
5	los1b_acp1_enable	RW	0x1	Automatic clock parking enable for bank 1. Enables Automatic Clock Parking of bank 1 (CLK[7:4]) outputs to a low/low state when LOS condition occurs. 0 = Disable 1 = Enable
4	los0b_acp0_enable	RW	0x1	Automatic clock parking enable for bank 0. Enables Automatic Clock Parking of bank 0 (CLK[3:0]) outputs to a low/low state when LOS condition occurs. 0 = Disable 1 = Enable
3	los1b_config	RW	0x1	Configure LOSb pin operating mode for CLKIN1. Determines if the LOSb pin is real-time or sticky. If sticky, the LOSb pin is driven by the LOS1b RW1C sticky bit. 0 = LOSb from bank 1 RW1C sticky bit 1 = LOSb real-time
2	los0b_config	RW	0x1	Configure LOSb pin operating mode for CLKIN0. Determines if the LOSb pin is real-time or sticky. If sticky, the LOSb pin is driven by the LOS0b RW1C sticky bit. 0 = LOSb from bank 0 RW1C sticky bit 1 = LOSb real-time
1	reserved	RW	0x0	Reserved
0	async_mode	RW	0x0	Enable asynchronous operating mode. SYNC mode is the normal mode of operation, where the input clock is continuous. Outputs stop and start in a glitch free manner. ASYNC mode is used when the input is a pulse instead of a clock. All glitch-free synchronization circuits are bypassed, minimizing the latency through the device. ASYNC mode cannot be used with LOS or ACP. B0x4[6] and B0x4[4] must be set to 0 if ASYNC mode is used. 0 = SYNC mode, glitch-free outputs 1 = ASYNC mode, non-glitch-free outputs

4.5.4 VENDOR_REVISION_ID

Vendor ID, Revision ID Register.

VENDOR_REVISION_ID Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	rid	RO	0x0	Revision ID. Silicon revision. 0x0 = A revision
3:0	vid	RO	0x1	Vendor ID. Vendor ID. 0x1 = Renesas

4.5.5 DEVICE_ID

Device ID Register.

DEVICE_ID Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:0	device_id	RO	0x38	Device ID. RC19308 listed as default. 0x38 = RC19308 0x34 = RC19304 0x32 = RC19302

4.5.6 BYTE_COUNT

Number of Bytes Returned on an SMBus Block Read.

BYTE_COUNT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:5	reserved	RW	0x0	Reserved
4:0	byte_count	RW	0x7	Writing to this register configures how many bytes will be returned on an SMBus block read.

4.5.7 SLEW_AMP_SELECT

Multifunction Pin Configuration Register.

SLEW_AMP_SELECT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	slew_amp_sel	RW	0x0	Multifunction pin selection. The pin is defined as either Slew Rate Select or Amplitude Select. If Amplitude Select is chosen, refer to registers 0x10 and 0x11. 0 = Pin is Slew Rate Select pin (RC193xxA) 1 = Pin is Amplitude Select pin (RC193xxA001)
6	reserved	RW	0x0	Reserved
5:4	clksel_1_0	RW	0x0	Clock mux select. These bits allow software control of the input clock mux. 0 = Both bank from CLKIN0 1 = Bank0 from CLKIN0, bank1 from CLKIN1 2 = Invalid 3 = Both bank from CLKIN1
3:1	reserved	RW	0x0	Reserved
0	clksel_cntrl	RW	0x0	Select pin or software control of the clock mux. Pin control is the power up default. 0 = Use CLKSEL pin control 1 = Use software control (B0xA [5:4])

4.5.8 INPUT_PULLUP_PULLDOWN_4

Internal Pull-up / Pull-down Configuration Register.

INPUT_PULLUP_PULLDOWN_4 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	reserved	RW	0xb	Reserved
3	sdata_pullup	RW	0x0	Enable/disable internal pull-up. The default pin state is high when the internal pull-up is enabled. If the SMBus is not used, this bit may be set to hold the SDATA pin in an inactive state. It should not be set if the SMBus is used in the system. RC19308 and RC19304 only. 0 = Disable internal pull-up 1 = Enable internal pull-up
2	reserved	RW	0x0	Reserved
1	sclk_pullup	RW	0x0	Enable/disable internal pull-up. The default pin state is high when the internal pull-up is enabled. If the SMBus is not used, this bit may be set to hold the SDATA pin in an inactive state. It should not be set if the SMBus is used in the system. RC19308 and RC19304 only. 0 = Disable internal pull-up 1 = Enable internal pull-up
0	reserved	RW	0x0	Reserved

4.5.9 AMP_CTRL_ALT

Alternate Amplitude Selection Register.

AMP_CTRL_ALT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	amp_cntrl_alt_bnk1	RW	0xB	Alternate amplitude control for bank 1. When the multifunction pin is configured as Amplitude Select, this field defines the single-ended output amplitude of Bank 1 (CLK[7:4]) when the pin = 1. When the multifunction pin is configured as Slew Rate Selection, this field has no impact. 0x0 = 625mV 0x1 = 650mV 0x2 = 675mV 0x3 = 700mV 0x4 = 725mV 0x5 = 750mV 0x6 = 775mV 0x7 = 800mV 0x8 = 825mV 0x9 = 850mV
amp_cntrl_alt_bnk1 (continued)				0xA = 875mV 0xB = 900mV 0xC = 925mV 0xD = 950mV 0xE = 975mV 0xF = 1000mV

AMP_CTRL_ALT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
3:0	amp_cntrl_alt_bnk0	RW	0xB	Alternate amplitude control for bank 0. When the multifunction pin is configured as Amplitude Select, this field defines the single-ended output amplitude of the Bank 0 (CLK[3:0]) when the pin = 1. When the multifunction pin is configured as Slew Rate Selection, this field has no impact. 0x0 = 625mV 0x1 = 650mV 0x2 = 675mV 0x3 = 700mV 0x4 = 725mV 0x5 = 750mV 0x6 = 775mV 0x7 = 800mV 0x8 = 825mV 0x9 = 850mV 0xA = 875mV 0xB = 900mV 0xC = 925mV 0xD = 950mV 0xE = 975mV 0xF = 1000mV

4.5.10 AMP_CTRL_DEF

Default Amplitude Selection Register.

AMP_CTRL_DEF Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	amp_cntrl_def_bnk1	RW	0x7	Default amplitude control for bank 1. When the multifunction pin is configured as Amplitude Select, this field defines the single-ended output amplitude of the Bank 1 (CLK[7:4]) when the pin = 0. When the multifunction pin is configured as Slew Rate Selection, this field determines the amplitude of bank 1 (CLK[7:4]). 0x0 = 625mV 0x1 = 650mV 0x2 = 675mV 0x3 = 700mV 0x4 = 725mV 0x5 = 750mV 0x6 = 775mV 0x7 = 800mV 0x8 = 825mV 0x9 = 850mV 0xA = 875mV 0xB = 900mV 0xC = 925mV 0xD = 950mV 0xE = 975mV 0xF = 1000mV

AMP_CTRL_DEF Bit Field Descriptions

Bit Field	Field Name	Field Type	Default Value	Description
3:0	amp_cntrl_def_bnk0	RW	0x7	Default amplitude control for bank 0. When the multifunction pin is configured as Amplitude Select, this field defines the single-ended output amplitude of the Bank 0 (CLK[3:0]) when the pin = 0. When the multifunction pin is configured as Slew Rate Selection, this field determines the amplitude of bank 0 (CLK[3:0]). 0x0 = 625mV 0x1 = 650mV 0x2 = 675mV 0x3 = 700mV 0x4 = 725mV 0x5 = 750mV 0x6 = 775mV 0x7 = 800mV 0x8 = 825mV 0x9 = 850mV
amp_cntrl_def_bnk0 (continued)				0xA = 875mV 0xB = 900mV 0xC = 925mV 0xD = 950mV 0xE = 975mV 0xF = 1000mV

4.5.11 PD_RESTORE_LOSb_CONFIG

Configuration and Status Register.

PD_RESTORE_LOSb_CONFIG Bit Field Descriptions

Bit Field	Field Name	Field Type	Default Value	Description
7:5	reserved	RW	0x0	Reserved
4	ck_acquire_rb	RO	0x0	Clock acquired read-back. This bit indicates if a clock was ever detected (LOSb de-asserted) for the current power cycle. 0 = Clock never acquired 1 = Clock acquired once before
3	pd_restoreb	RW	0x1	Save configuration in power-down. This bit determines the behavior of the device when the PWRGD_PWRDNb pin is asserted low. This bit is automatically returned to 1 after PWRGD_PWRDNb is toggled 1-0-1 with the bit set to 0. 0 = Config Cleared 1 = Config Saved
2	sdata_time_out_enable	RW	0x1	Enable SMB time out monitoring SDATA. This bit enables a timeout for the SMBus data path. This timeout monitor is in addition to the mandatory SCLK timeout monitor. These monitors release a hung SMBus. 0 = Disable SDATA time out 1 = Enable SDATA time out
1	los1b_rb	RO	0x0	Real-time read back of CLKIN1 clock detect. This bit provides a real-time status of the CLKIN1 input. The default value assumes CLKIN1 is not present. 0 = LOS event detected (no CLKIN1 detected) 1 = No LOS event detected (CLKIN1 detected)
0	los0b_rb	RO	0x0	Real-time read back of CLKIN0 clock detect. This bit provides a real-time status of the CLKIN0 input. The default value assumes CLKIN0 is not present. 0 = LOS event detected (no CLKIN0 detected) 1 = No LOS event detected (CLKIN0 detected)

4.5.12 OUTPUT_IMPEDANCE_7_0

Output Impedance Select Register 0.

OUTPUT_IMPEDANCE_7_0 Bit Field Descriptions

Bit Field	Field Name	Field Type	Default Value	Description
7	clk7_impedance0	RW	0x0	CLK7 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When the pin is 0, this bit and B0x15[7] are set to 0. When the pin is M, this bit is set to 0 and B0x15[7] is set to 1. When the pin is 1, this bit is set to 1 and B0x15[7] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
6	clk6_impedance0	RW	0x0	CLK6 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[6] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[6] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[6] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
5	clk5_impedance0	RW	0x0	CLK5 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[5] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[5] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[5] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
4	clk4_impedance0	RW	0x0	CLK4 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[4] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[4] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[4] is set to 0. 0 = 85 ohm differential or 42.5 ohm single-ended 1 = 100 ohm differential or 50 ohm single-ended
3	clk3_impedance0	RW	0x0	CLK3 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[3] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[3] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[3] is set to 0. 0 = 85 ohm differential or 42.5 ohm single-ended 1 = 100 ohm differential or 50 ohm single-ended
2	clk2_impedance0	RW	0x0	CLK2 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[2] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[2] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[2] is set to 0. 0 = 85 ohm differential or 42.5 ohm single-ended 1 = 100 ohm differential or 50 ohm single-ended

OUTPUT_IMPEDANCE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
1	clk1_impedance0	RW	0x0	CLK1 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[1] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[1] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[1] is set to 0. 0 = 85 ohm differential or 42.5 ohm single-ended 1 = 100 ohm differential or 50 ohm single-ended
0	clk0_impedance0	RW	0x0	CLK0 impedance select bit 0. The default value of this bit is set by the ZOUTSEL_tri pin. When this pin is 0, this bit and B0x15[0] are set to 0. When this pin is M, this bit is set to 0, ignored, and B0x15[0] is set to 1. When this pin is 1, this bit is set to 1 and B0x15[0] is set to 0. 0 = 85 ohm differential or 42.5 ohm single-ended 1 = 100 ohm differential or 50 ohm single-ended

4.5.13 OUTPUT_REC_SEL_7_0

Output Impedance Select Register 1.

OUTPUT_REC_SEL_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	clk7_impedance1	RW	0x1	CLK7 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[7]. When this pin is M, this bit is set to 1 at power up, B0x14[7] is set to 0 and ignored. 0 = See B0x14[7] 1 = 34 ohm differential or 17 ohm single-ended
6	clk6_impedance1	RW	0x1	CLK6 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[6]. When this pin is M, this bit is set to 1 at power up, B0x14[6] is set to 0 and ignored. 0 = Source, see B0x14[6] 1 = 34 ohm differential or 17 ohm single-ended
5	clk5_impedance1	RW	0x1	CLK5 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[5]. When this pin is M, this bit is set to 1 at power up, B0x14[5] is set to 0 and ignored. 0 = Source, see B0x14[5] 1 = 34 ohm differential or 17 ohm single-ended
4	clk4_impedance1	RW	0x1	CLK4 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[4]. When this pin is M, this bit is set to 1 at power up, B0x14[4] is set to 0 and ignored. 0 = Source, see B0x14[4] 1 = 34 ohm differential or 17 ohm single-ended

OUTPUT_REC_SEL_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
3	clk3_impedance1	RW	0x1	CLK3 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[3]. When this pin is M, this bit is set to 1 at power up, B0x14[3] is set to 0 and ignored. 0 = Source, see B0x14[3] 1 = 34 ohm differential or 17 ohm single-ended
2	clk2_impedance1	RW	0x1	CLK2 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[2]. When this pin is M, this bit is set to 1 at power up, B0x14[2] is set to 0 and ignored. 0 = Source, see B0x14[2] 1 = 34 ohm differential or 17 ohm single-ended
1	clk1_impedance1	RW	0x1	CLK1 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, this bit is set to 0 at power up and the appropriate value is set in B0x14[1]. When this pin is M, this bit is set to 1 at power up, B0x14[1] is set to 0 and ignored. 0 = Source, see B0x14[1] 1 = 34 ohm differential or 17 ohm single-ended
0	clk0_impedance1	RW	0x1	CLK0 impedance select bit 1. The default state of this bit is set by the ZOUTSEL_tri pin. When this pin is 0 or 1, This bit is set to 0 at power up and the appropriate value is set in B0x14[0]. When this pin is M, This bit is set to 1 at power up, B0x14[0] is set to 0 and ignored. 0 = Source, see B0x14[0] 1 = 34 ohm differential or 17 ohm single-ended

4.5.14 OUTPUT_SLEW_RATE_7_0

Output Slew Rate Select Register.

OUTPUT_SLEW_RATE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	clk7_slewrate	RW	0x1	CLK7 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
6	clk6_slewrate	RW	0x1	CLK6 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
5	clk5_slewrate	RW	0x1	CLK5 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate

OUTPUT_SLEW_RATE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
4	clk4_slewrate	RW	0x1	CLK4 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
3	clk3_slewrate	RW	0x1	CLK3 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
2	clk2_slewrate	RW	0x1	CLK2 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
1	clk1_slewrate	RW	0x1	CLK1 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
0	clk0_slewrate	RW	0x1	CLK0 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate

4.5.15 LOW_LOW_DETECT

CLKIN Low-Low Detect Enable Register.

LOW_LOW_DETECT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:3	reserved	RW	0x12	Reserved
2	low_low_det_enable	RW	0x1	Enable low-low detect circuit on CLKIN0 and CLKIN1. Allows the device to detect a low-low condition on each CLKIN input and turn off the receiver. (Low-low is not a valid differential state). 0 = Disable 1 = Enable
1:0	reserved	RW	0x0	Reserved

4.5.16 RECEIVER_CONTROL

CLKIN Configuration Register.

RECEIVER_CONTROL Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	reserved	RW	0x0	Reserved
3	ac_in1	RW	0x0	AC-couple CLKIN1. When AC-coupling the input clock, set this bit to enable internal bias circuitry on the CLKIN1. This eliminates the need for external bias components on the CLKIN1 side of the AC-coupling capacitor. 0 = Disable internal bias (DC-coupled) 1 = Enable internal bias (AC-coupled)

RECEIVER_CONTROL Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
2	rx_term1	RW	0x0	Enable internal termination for CLKIN1. Applications requiring receiver terminations may set this bit to enable internal termination resistors to ground on both the CLKIN1 and CLKIN1b pins. PCIe applications generally require Rx_TERM to be 0. 0 = Disable internal termination (PCIe) 1 = Enable internal termination
1	ac_in0	RW	0x0	AC-couple CLKIN0. When AC-coupling the input clock, set this bit to enable internal bias circuitry on the CLKIN0. This eliminates the need for external bias components on the CLKIN0 side of the AC-coupling capacitor. 0 = Disable internal bias (DC-coupled) 1 = Enable internal bias (AC-coupled)
0	rx_term0	RW	0x0	Enable internal termination for CLKIN0. Applications requiring receiver terminations may set this bit to enable internal termination resistors to ground on both the CLKIN0 and CLKIN0b pins. PCIe applications generally require Rx_TERM to be 0. 0 = Disable internal termination (PCIe) 1 = Enable internal termination

4.5.17 WRITE_LOCK

Non-clearable SMBus Write Lock Register.

WRITE_LOCK Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:1	reserved	RW	0x0	Reserved
0	write_lock	RW	0x0	Non-clearable SMBus write lock bit. When written to one, the SMBus control registers cannot be written. They may be read. This bit can only be cleared by cycling power. 0 = SMBus writes are not prohibited by WRITE_LOCK 1 = SMBus locked for writing

4.5.18 WRITE_LOCK_LOS_EVT

Clearable SMBus Write Lock and LOS Event Register.

WRITE_LOCK_LOS_EVT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:3	reserved	RW1C	0x0	Reserved
2	los1_evt	RW1C	0x0	CLKIN1 LOS event sticky bit. When high, indicates that an LOS event was detected on CLKIN1. Can be cleared by writing a 1 to it. 0 = No LOS1 event detected 1 = LOS1 event detected.
1	los0_evt	RW1C	0x0	CLKIN0 LOS event sticky bit. When high, indicates that an LOS event was detected on CLKIN0. Can be cleared by writing a 1 to it. 0 = No LOS event detected 1 = LOS event detected.
0	write_lock_rw1c	RW1C	0x0	Clearable SMBus write lock bit. When written to one, the SMBus control registers cannot be written. They may be read. This bit can only be cleared by writing a 1 to it. 0 = SMBus writes are not prohibited by WRITE_LOCK_RW1C 1 = SMBus locked for writing

5. Applications Information

5.1 Inputs, Outputs, and Output Enable Control

The CLKIN/CLKINb inputs of the RC193xx devices have an internal bias network that prevents self-oscillation from a floating input clock condition.

5.1.1 Recommendations for Unused Inputs and Outputs

5.1.1.1 Unused Differential CLKIN Inputs

The CLKIN/CLKINb inputs of the RC19xxx devices have internal bias networks that protect the devices from a floating input clock condition. For RC193xx multiplexers that use only one input clock, the unused input can be left open. Renesas recommends that no trace be attached to unused CLKIN pins.

5.1.1.2 Unused Single-ended Control Inputs

The single-ended control pins have internal pull-up and/or internal pull-down resistors and do not require external resistors. They can be left floating if the default pin state is the desired state. If external resistors are needed to change the pin state or are desired for design robustness, 10kohm is the recommended value. Tri-level inputs are internally biased to VDD/2 and will indicate the mid (M) state if left floating.

5.1.1.3 Unused Differential CLK Outputs

All unused CLK outputs can be left floating. Renesas recommends that no trace be attached to unused CLK outputs. While not required (but highly recommended), the best design practice is to disable unused CLK outputs. This is easily accomplished with the dedicated OEb pin for each output.

5.1.1.4 Unused SMBus Clock and Data Pins

If the SMBus interface is not used, the clock and data pins must be pulled high with an external resistor. The two pins can share a resistor if there is no possibility of using the SMBus interface for debug purposes. If the interface might be used for debug, separate resistors should be used. Lightly loaded buses may use 10kohm pull-up resistors. Heavily loaded buses will require smaller pull-up resistor values. The SMBus pins are 3.3V tolerant and may be used with a 3.3V pull-up voltage

5.2 Differential CLKIN Configurations

The RC193xx input clock buffer supports four configurations:

- Direct connection to HCSL-level inputs
- Direct connection to LVDS-level inputs with *external* termination resistor
- Internal self-bias circuit for applications that *externally* AC-couple the input clock
  This feature is enabled by the **AC_IN** bit.
- Internal pull-down resistors (Rp) to terminate the clock input at the receiver.
  This feature is enabled by the **Rx_TERM** bit.

Devices with multiple input clocks have individual AC_IN and Rx_TERM configuration bits for each input. The internal input clock terminations prevent reflections and are useful for non-PCIe applications, where the frequency and transmission line length vary from the 100MHz PCIe standard. The following table summarizes the CLKIN configuration bit settings for the various configurations that are displayed in Figure 13 to Figure 16.

Table 32. CLKIN Configuration Bits

Configuration	CLKIN1 AC_IN1 B35[3]	CLKIN1 RX_TERM1 B35[2]	CLKIN0 AC_IN0 B35[1]	CLKIN0 RX_TERM0 B35[0]	Notes
HCSL Input Levels (PCIe Standard)	0	0	0	0	Default values
LVDS Input Levels	1	0	1	0	Eliminates need for external bias circuit. Must use external RT.
External AC-Coupling	1	0	1	0	Eliminates need for external bias circuit.
Receiver Termination	0	1	0	1	Prevents reflections for non-PCIe applications.

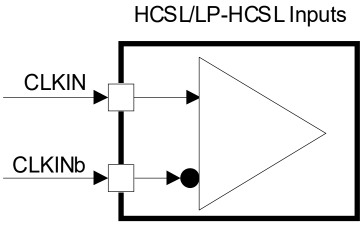


Figure 13. HCSL Input Levels (PCIe Standard)

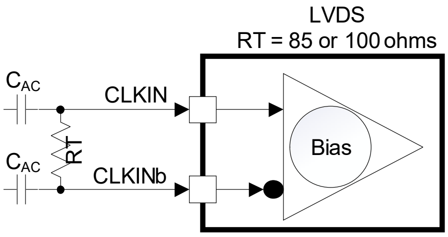


Figure 14. LVDS Input Levels

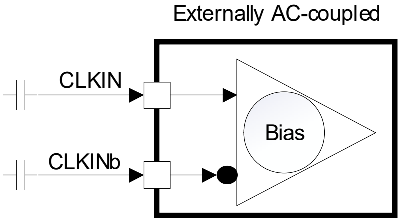


Figure 15. External AC-Coupling

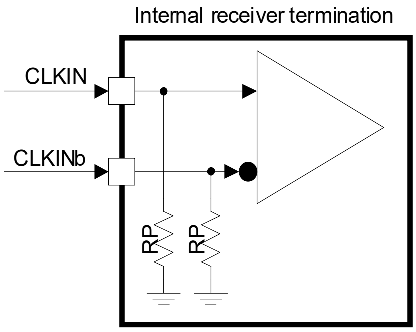


Figure 16. Receiver Termination

5.3 Differential CLK Output Configurations

5.3.1 Internal CLK Source Termination Enabled (ZOUT_SEL_tri = 0 or 1)

The RC193xx LP-HCSL CLK outputs have internal source terminations and directly drive industry-standard HCSL-level inputs with no external components. They support both 85 and 100 ohm differential impedances (Z_O = Z_{DIF} = 85 or 100 ohm) in Figure 17 through Figure 19. The combination of source termination and receiver termination results in a double-terminated load. The CLK outputs can drive double-terminated loads, however, when double-terminated, the CLK output swing will be half of the source-terminated values.

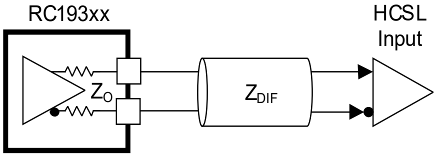


Figure 17. Direct-Coupled Source-Terminated HCSL (ZOUT_SEL_tri = 0 or 1)

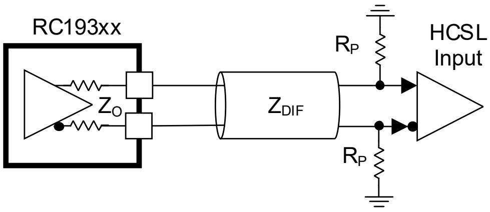


Figure 18. Direct-Coupled Double-Terminated HCSL

The RC193xx CLK outputs can directly drive AC-coupling capacitors without any source-termination components. The differential input will require an input-dependent bias network. This network may or may not be internal to the receiver. Refer to the receiver specification for detailed requirements. AC-coupling is used to connect the RC193xx to other logic families such as LVDS, LVPECL, or CML. See AN-891 for examples.

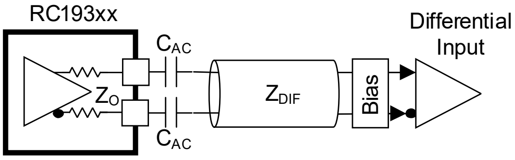


Figure 19. AC-Coupled Differential Input with Bias Network

Table 33 contains values for the items in the above figures.

Table 33. Parameters for Internal CLK Source Termination Enabled

ZOUT_SEL_tri	Z_O (ohms)	Z_{DIF} (ohms)	R_P (ohms)	C_{AC} (uF)
0	85	85	Z_{DIF} /2	0.1
1	100	100	Z_{DIF} /2	0.1

5.3.2 Internal CLK Source Termination Disabled (ZOUT_SEL_tri = M)

ZOUT_SEL_tri = M disables the internal source termination making the differential Z_O = 34ohms. This setting is used with receiver terminated loads to provide a higher CLK amplitude to the load than can be obtained with a double terminated configuration. The minimum single-ended amplitude in this configuration targets ~500mV. See Table 21 for detailed specifications. This setting is intended for Z_{DIF} =100 ohm systems.

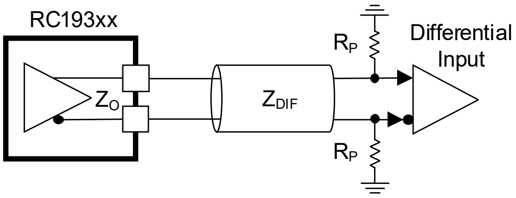


Figure 20. Direct-Coupled Receiver-Terminated HCSL

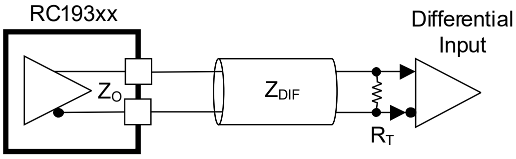


Figure 21. Alternate Direct-Coupled Receiver-Terminated Input

Table 34 contains values for the items in Figure 20 and Figure 21.

Table 34. Parameters for Direct-Coupled Receiver-Terminated Configurations

ZOUT_SEL_tri	Z_O (ohms)	Z_{DIF} (ohms)	R_P (ohms)	R_T (ohms)
M	34	100	Z_{DIF} /2	Z_{DIF}

5.4 Power Down Tolerant Pins

Pins labeled Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the RC193xx may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the RC193xx before it has received power. NOTE: The differential CLKIN pins are limited to 1.4V. Applying a voltage higher than this may damage the part.

5.5 Flexible Startup Sequencing

RC193xx devices support Flexible Startup Sequencing (FSS). FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table 35 shows the supported sequences; that is, the RC193xx devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

Note: The PWRGD_PWRDNb is synchronized with the selected CLKIN. If CLKIN is not present, the RC193xx will not sample the pin until CLKIN is present. This applies to both powering up and powering down. If powered up when the input clock stops, ACP (default enabled) will place the outputs into a low/low state even though the RC193xx will not be completely powered down.

Table 35. Flexible Startup Sequences

VDD	PWRGD_PWRDNb	CLKIN/CLKINb
Not present	X	Running
		Floating
		Low/Low
Present	0 or 1	Running
		Floating
		Low/Low

5.6 Loss of Signal and Automatic Clock Parking

The RC193xx devices have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOSb pin (the “b” suffix indicates “bar”, or active-low) and sets the LOS_EVT bit in the SMBus register space. Figure 22 shows the LOSb de-assertion timing for the RC193xx clock multiplexers. LOSb on the RC193xx multiplexers defaults to low at power up. CLKIN is represented differentially in Figure 22 and Figure 23.

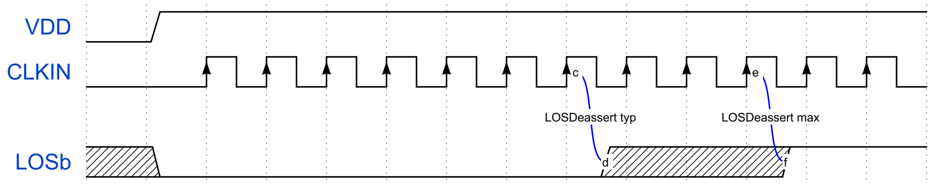


Figure 22. LOSb De-assert Timing RC193xx Devices

Note: The LOSb pin monitors the *selected* input clock in the RC193xx multiplexers.

The following diagram shows the LOSb assertion sequence when the *selected* CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the outputs to a Low/Low state after an LOS event. For exact timing, see Electrical Characteristics.

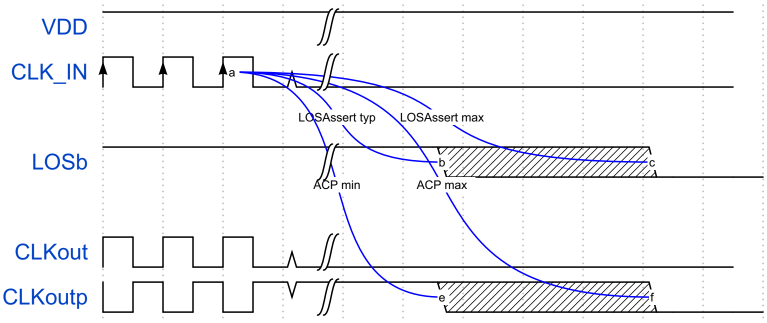


Figure 23. LOSb Assert Timing

5.7 Output Enable Control

The RC193xx buffer/mux family provides two mechanisms to enable or disable clock outputs. Both mechanisms start and stop the output clocks in a synchronous, glitch-free manner. A clock output is enabled only when both mechanisms indicate “enabled.” The following sections describe the two mechanisms.

5.7.1 SMBus Output Enable Bits

The RC193xx clock multiplexer family has a traditional SMBus output enable bit for each output. The power-up default is 1, or enabled. Changing this bit to a 0 disables the output to a low/low state. The transitions between the enable and disable states are glitch-free in both directions.

Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

5.7.2 Output Enable (OEb) Pins

The OEb (Note: the “b” suffix indicates “bar”, or active-low) pins on the RC193xx provide flexible CLKREQb functionality for PCIe slots and/or OE control for ‘motherboard-down’ devices. If the OEb pin is low the output is enabled. If the OEb pin is high, the output is disabled to a low/low state. All OEb pins enable and disable the controlled outputs in a glitch-free, synchronous manner.

Note: The glitch-free synchronization logic requires the *selected* CLKIN be running to enable or disable the outputs with this mechanism.

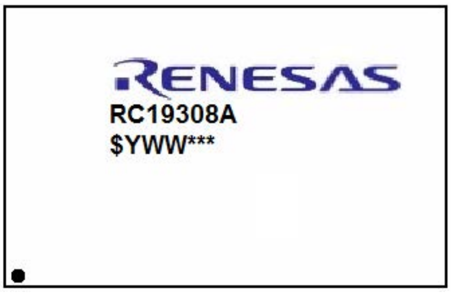
5.8 PCB Layout Recommendations

Proper layout is critical to achieving the full functionality and efficiency of the device. For information on how to support optimal electrical performance, effective thermal management, and overall system reliability, see the PCIe Buffer-Mux Layout Recommendations Application Note.

6. Package Outline Drawings

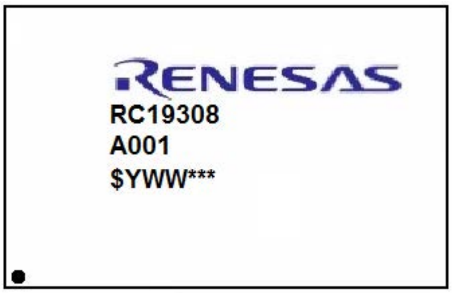
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagrams



RC19308A

- Lines 1 is the part number
- Line 2:
    - “$” indicates the mark code.
    - “YWW” indicates the last digit of the year and work week the part was assembled.
    - “***” indicates the assembly lot number.

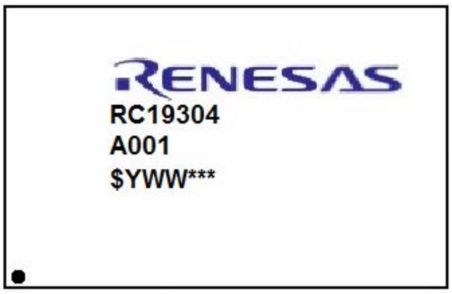


RC19308A001

- Lines 1 and 2 comprise the part number.
- Line 3:
    - “$” indicates the mark code.
    - “YWW” indicates the last digit of the year and work week the part was assembled.
    - “***” indicates the assembly lot number.

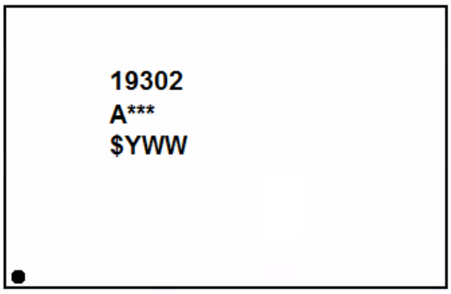
RC19304A

- Line 1 is the part number.
- Line 2:
    - “$” indicates the mark code.
    - “YWW” indicates the last digit of the year and work week the part was assembled.
    - “***” indicates the assembly lot number.



RC19304A001

- Lines 1 and 2 comprise the part number.
- Line 3:
    - “$” indicates the mark code.
    - “YWW” indicates the last digit of the year and work week the part was assembled.
    - “***” indicates the assembly lot number.



RC19302A

- Lines 1 and 2 comprise the part number (RC excluded).
- Line 2: “***” indicates the assembly lot number.
- Line 3:
  - “$” indicates the mark code.
  - “YWW” indicates the last digit of the year and work week the part was assembled.

8. Ordering Information

Part Number	Carrier Type	Pin Function Option	Number of Outputs	Package	Temperature Range
RC19308AGNA#BB0	Tray	Slew Rate Selection	8	6 × 6 mm, 0.4mm pitch 48-VFQFPN	-40 to +105°C
RC19308AGNA#KB0	Tape and Reel (EIA-481-D)				
RC19308A001GNA#BB0	Tray	Amplitude Selection			
RC19308A001GNA#KB0	Tape and Reel (EIA-481-D)				
RC19304AGNL#BB0	Tray	Slew Rate Selection	4	4 × 4 mm, 0.4mm pitch 28-VFQFPN	-40 to +105°C
RC19304AGNL#KB0	Tape and Reel (EIA-481-D)				
RC19304A001GNL#BB0	Tray	Amplitude Selection			
RC19304A001GNL#KB0	Tape and Reel (EIA-481-D)				
RC19302AGNT#BD0	Tray	N/A	2	3 × 3 mm, 0.4mm pitch 20-VFQFPN	-40 to +105°C
RC19302AGNT#KD0	Tape and Reel (EIA-481-D)				

9. Revision History

Revision	Date	Description
1.03	Nov 11, 2025	▪ Deleted non-applicable parameter description information from Table 7 to Table 12
1.02	Sep 12, 2025	▪ Added footnote 3 to Table 23 ▪ Added ECAD Design Information
1.01	Jun 28, 2025	Added PCB Layout Recommendations
1.00	Apr 4, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RC19308AGNA#BB0	48	VFQFPN	PSC-4212-02/NDG48P2
RC19308AGNA#KB0	48	VFQFPN	PSC-4212-02/NDG48P2
RC19308A001GNA#BB0	48	VFQFPN	PSC-4212-02/NDG48P2
RC19308A001GNA#KB0	48	VFQFPN	PSC-4212-02/NDG48P2
RC19304AGNL#BB0	28	VFQFPN	PSC-4249-01-02/NDG28P1
RC19304AGNL#KB0	28	VFQFPN	PSC-4249-01-02/NDG28P1
RC19304A001GNL#BB0	28	VFQFPN	PSC-4249-01-02/NDG28P1
RC19304A001GNL#KB0	28	VFQFPN	PSC-4249-01-02/NDG28P1
RC19302AGNT#BD0	20	VFQFPN	PSC-4179-02/NDG20P2
RC19302AGNT#KD0	20	VFQFPN	PSC-4179-02/NDG20P2

A.2 Symbol Pin Information

A.2.1 48-VFQFPN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	ZOUTSEL_tri	Input	-
2	VDDDIG	Power	-
3	PWRGD_PWRDNb	Input	-
4	CLKIN0	Input	-
5	CLKINb0	Input	-
6	VDDIN0	Power	-
7	SADR_tri0	Input	-
8	CLKIN1	Input	-
9	CLKINb1	Input	-
10	SDATA	I/O	-
11	SCLK	Input	-
12	VDDIN1	Power	-
13	VDDCLK_1	Power	-
14	CLK7	Output	-
15	CLKb7	Output	-
16	OEb7	Input	-
17	CLKSEL_tri	Input	-
18	OEb6	Input	-
19	CLK6	Output	-
20	CLKb6	Output	-
21	VDDCLK_1	Power	-
22	CLK5	Output	-
23	CLKb5	Output	-
24	OEb5	Input	-
25	OEb4	Input	-
26	CLK4	Output	-
27	CLKb4	Output	-
28	VDDCLK_1	Power	-
29	LOSb	Output	-
30	VDDCLK_0	Power	-
31	VDDA	Power	-
32	CLK3	Output	-
33	CLKb3	Output	-
34	OEb3	Input	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
35	OEb2	Input	-
36	SADR_tri1	Input	-
37	CLK2	Output	-
38	CLKb2	Output	-
39	VDDCLK_0	Power	-
40	CLK1	Output	-
41	CLKb1	Output	-
42	SLEWRATE_SEL [1]	Input	-
43	OEb1	Input	-
44	OEb0	Input	-
45	CLK0	Output	-
46	CLKb0	Output	-
47	VDDCLK_0	Power	-
48	GNDSUB	Power	-
EPAD49	GND	Power	-

1. This pin is AMPLITUDE_SEL for the RC19308A001.

A.2.2 28-VFQFPN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	PWRGD_PWRDNb	Input	-
2	CLKIN0	Input	-
3	CLKINb0	Input	-
4	VDDIN0	Power	-
5	CLKIN1	Input	-
6	CLKINb1	Input	-
7	VDDIN1	Power	-
8	CLKSEL_tri	Input	-
9	OEb6	Input	-
10	CLK6	Output	-
11	CLKb6	Output	-
12	VDDCLK_1	Power	-
13	CLK5	Output	-
14	CLKb5	Output	-
15	SLEWRATE_SEL [1]	Input	-
16	OEb5	Input	-
17	LOSb	Output	-
18	VDDA	Power	-
19	OEb2	Input	-
20	CLK2	Output	-
21	CLKb2	Output	-
22	VDDCLK_0	Power	-
23	CLK1	Output	-
24	CLKb1	Output	-
25	OEb1	Input	-
26	VDDDIG	Power	-
27	GNDSUB	Power	-
28	ZOUTSEL_tri	Input	-
EPAD29	GND	Power	-

1. This pin is AMPLITUDE_SEL for the RC19304A001.

A.2.3 20-VFQFPN

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	CLKIN0	Input	-
2	CLKINb0	Input	-
3	VDDIN0	Power	-
4	CLKIN1	Input	-
5	CLKINb1	Input	-
6	VDDIN1	Power	-
7	CLKSEL_tri	Input	-
8	VDDCLK_1	Power	-
9	CLK5	Output	-
10	CLKb5	Output	-
11	ZOUTSEL_tri	Input	-
12	OEb5	Input	-
13	LOSb	Output	-
14	VDDA	Power	-
15	OEb2	Input	-
16	CLK2	Output	-
17	CLKb2	Output	-
18	VDDCLK_0	Power	-
19	VDDDIG	Power	-
20	GNDSUB	Power	-
EPAD21	GND	Power	-

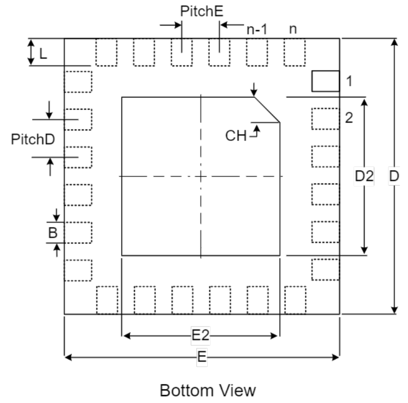
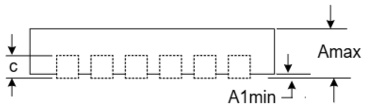
A.3 Symbol Parameters

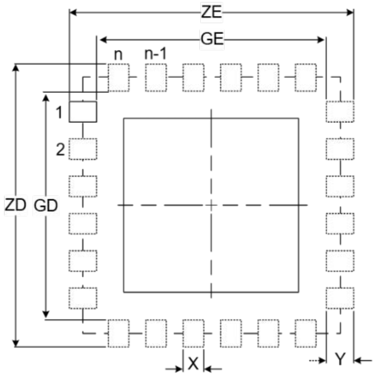
Orderable Part Number	Qualification	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	RoHS	Output Type	Number of Outputs	Interface	Max Output Frequency	Phase Jitter	Output Select Mode
RC19308AGNA#BB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	8	SMBus	400 MHz	42.8 fs	Slew Rate
RC19308AGNA#KB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	8	SMBus	400 MHz	42.8 fs	Slew Rate
RC19308A001GNA#BB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	8	SMBus	400 MHz	42.8 fs	Amplitude
RC19308A001GNA#KB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	8	SMBus	400 MHz	42.8 fs	Amplitude
RC19304AGNL#BB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	4	SMBus	400 MHz	42.8 fs	Slew Rate
RC19304AGNL#KB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	4	SMBus	400 MHz	42.8 fs	Slew Rate
RC19304A001GNL#BB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	4	SMBus	400 MHz	42.8 fs	Amplitude
RC19304A001GNL#KB0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	4	SMBus	400 MHz	42.8 fs	Amplitude
RC19302AGNT#BD0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	2	SMBus	400 MHz	42.8 fs	-
RC19302AGNT#KD0	Industrial	SMD	-40 °C	105 °C	1.7 V	1.9 V	Compliant	LP-HCSL	2	SMBus	400 MHz	42.8 fs	-

A.4 Footprint Design Information

A.4.1 48-VFQFPN

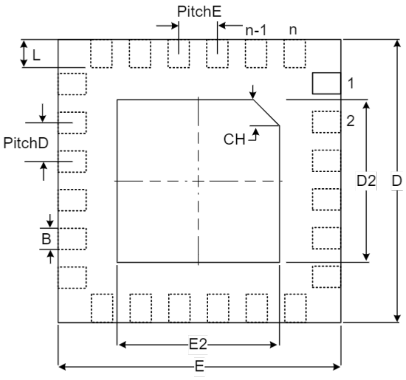
IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	PSC-4212-02/NDG48P2	48

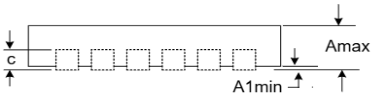
Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	5.90	 Bottom View
Maximum body span (vertical side)	Dmax	6.10	
Minimum body span (horizontal side)	Emin	5.90	
Maximum body span (horizontal side)	Emax	6.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.30	
Maximum Lead Length	Lmax	0.50	
Number of pins (vertical side)	PinCountD	12	
Number of pins (horizontal side)	PinCountE	12	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	 Side View
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side (center).	Pin1	S2	
Thermal pad Chamfer. If not present give hyphen (-).	CH	0.35	
Minimum thermal pad size (vertical side)	D2min	4.10	
Maximum thermal pad size (vertical side)	D2max	4.30	
Minimum thermal pad size (horizontal side)	E2min	4.10	
Maximum thermal pad size (horizontal side)	E2max	4.30	
Maximum Height	Amax	1.00	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	6.30	 PCB Top View
Distance between top pad toe to bottom pad toe (vertical side)	ZD	6.30	
Distance between left pad heel to right pad heel (horizontal side)	GE	5.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	5.20	
Pad Width	X	0.20	
Pad Length	Y	0.55	

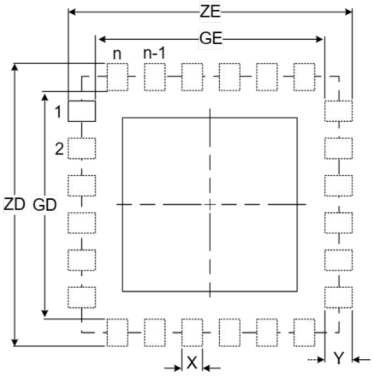
A.4.2 28-VFQFPN

IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	PSC-4249-01-02/NDG28P1	28

<table>
<tr><th>Description</th><th>Dimension</th><th>Value (mm)</th><th>Diagram</th></tr>
<tr><td>Minimum body span (vertical side)</td><td>Dmin</td><td>3.90</td><td rowspan="12">

Bottom View</td></tr>
<tr><td>Maximum body span (vertical side)</td><td>Dmax</td><td>4.10</td></tr>
<tr><td>Minimum body span (horizontal side)</td><td>Emin</td><td>3.90</td></tr>
<tr><td>Maximum body span (horizontal side)</td><td>Emax</td><td>4.10</td></tr>
<tr><td>Minimum Lead Width</td><td>Bmin</td><td>0.15</td></tr>
<tr><td>Maximum Lead Width</td><td>Bmax</td><td>0.25</td></tr>
<tr><td>Minimum Lead Length</td><td>Lmin</td><td>0.30</td></tr>
<tr><td>Maximum Lead Length</td><td>Lmax</td><td>0.50</td></tr>
<tr><td>Number of pins (vertical side)</td><td>PinCountD</td><td>7</td></tr>
<tr><td>Number of pins (horizontal side)</td><td>PinCountE</td><td>7</td></tr>
<tr><td>Distance between the center of any two adjacent pins (vertical side)</td><td>PitchD</td><td>0.40</td></tr>
<tr><td>Distance between the center of any two adjacent pins (horizontal side)</td><td>PitchE</td><td>0.40</td><td rowspan="12">

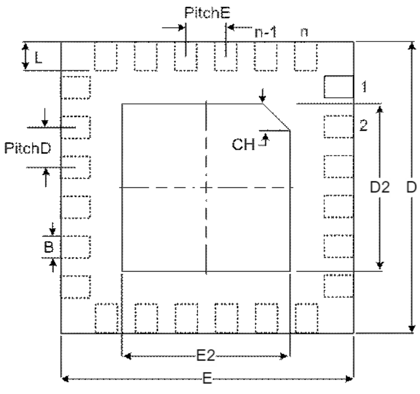
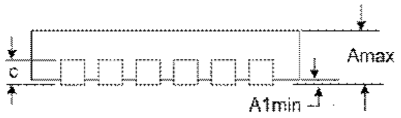
Side View</td></tr>
<tr><td>Location of pin 1; S2 = corner of D side (top left), C1 = center of E side (center).</td><td>Pin1</td><td>S2</td></tr>
<tr><td>Thermal pad Chamfer. If not present give hyphen (-).</td><td>CH</td><td>0.35</td></tr>
<tr><td>Minimum thermal pad size (vertical side)</td><td>D2min</td><td>2.50</td></tr>
<tr><td>Maximum thermal pad size (vertical side)</td><td>D2max</td><td>2.70</td></tr>
<tr><td>Minimum thermal pad size (horizontal side)</td><td>E2min</td><td>2.50</td></tr>
<tr><td>Maximum thermal pad size (horizontal side)</td><td>E2max</td><td>2.70</td></tr>
<tr><td>Maximum Height</td><td>Amax</td><td>1.00</td></tr>
<tr><td>Minimum Standoff Height</td><td>A1min</td><td>0.00</td></tr>
<tr><td>Minimum Lead Thickness</td><td>cmin</td><td>0.15</td></tr>
<tr><td>Maximum Lead Thickness</td><td>cmax</td><td>0.25</td></tr>
</table>

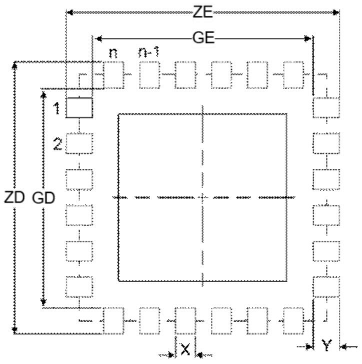
<table>
<tr><th colspan="4">Recommended Land Pattern</th></tr>
<tr><th>Description</th><th>Dimension</th><th>Value (mm)</th><th>Diagram</th></tr>
<tr><td>Distance between left pad toe to right pad toe (horizontal side)</td><td>ZE</td><td>4.30</td><td rowspan="6">

PCB Top View</td></tr>
<tr><td>Distance between top pad toe to bottom pad toe (vertical side)</td><td>ZD</td><td>4.30</td></tr>
<tr><td>Distance between left pad heel to right pad heel (horizontal side)</td><td>GE</td><td>3.20</td></tr>
<tr><td>Distance between top pad heel to bottom pad heel (vertical side)</td><td>GD</td><td>3.20</td></tr>
<tr><td>Pad Width</td><td>X</td><td>0.20</td></tr>
<tr><td>Pad Length</td><td>Y</td><td>0.55</td></tr>
</table>

A.4.3 20-VFQFPN

IPC Footprint Type	Package Code/POD Number	Number of Pins
QFN	PSC-4179-02/NDG20P2	20

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	2.90	
Maximum body span (vertical side)	Dmax	3.10	 Bottom View
Minimum body span (horizontal side)	Emin	2.90	
Maximum body span (horizontal side)	Emax	3.10	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.30	
Maximum Lead Length	Lmax	0.50	
Number of pins (vertical side)	PinCountD	5	
Number of pins (horizontal side)	PinCountE	5	
Distance between the center of any two adjacent pins (vertical side)	PitchD	0.40	
Distance between the center of any two adjacent pins (horizontal side)	PitchE	0.40	
Location of pin 1; S2 = corner of D side (top left), C1 = center of E side (center).	Pin1	S2	 Side View
Thermal pad Chamfer. If not present give hyphen (-).	CH	0.35	
Minimum thermal pad size (vertical side)	D2min	1.55	
Maximum thermal pad size (vertical side)	D2max	1.75	
Minimum thermal pad size (horizontal side)	E2min	1.55	
Maximum thermal pad size (horizontal side)	E2max	1.75	
Maximum Height	Amax	1.00	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.15	
Maximum Lead Thickness	cmax	0.25	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	3.30	 PCB Top View
Distance between top pad toe to bottom pad toe (vertical side)	ZD	3.30	
Distance between left pad heel to right pad heel (horizontal side)	GE	2.20	
Distance between top pad heel to bottom pad heel (vertical side)	GD	2.20	
Pad Width	X	0.20	
Pad Length	Y	0.55	