To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RD74VT1G00

2–input NAND Gate / Dual Supply Voltage Translator

REJ03D0512–0100
Rev.1.00
Jun. 01, 2005

Description

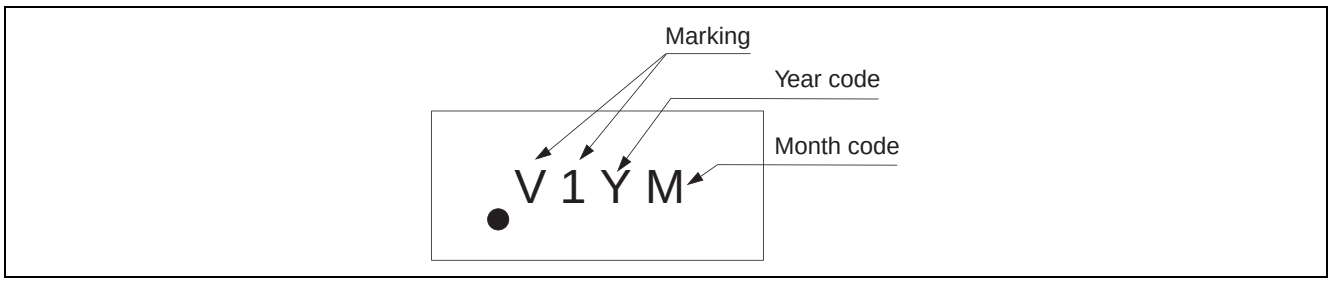
The RD74VT1G00 has two–input NAND gate in a 6 pin package. The input is designed to track V_{CC}IN, which accepts voltages from 1.2V to 3.6V, and the outputs are designed to track V_{CC}OUT, which operates at 1.2V to 3.6V. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- This product function as level shift that change V_{CC}IN input level to V_{CC}OUT output level by providing different supply voltage to V_{CC}IN and V_{CC}OUT.
- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- Supply voltage range: V_{CC}IN = 1.2 V to 3.6 V
  V_{CC}OUT = 1.2 V to 3.6 V
  Operating temperature range: –40 to +85°C
- All inputs V_{IH} (Max.) = 3.6 V (@V_{CC}IN = 0 V to 3.6 V)
  Outputs V_O (Max.) = 3.6 V (@V_{CC}OUT = 0 V)
- Output current ±2 mA (@V_{CC}OUT = 1.2 V)
  ±4 mA (@V_{CC}OUT = 1.4 V to 1.6 V)
  ±6 mA (@V_{CC}OUT = 1.65 V to 1.95 V)
  ±18 mA (@V_{CC}OUT = 2.3 V to 2.7 V)
  ±24 mA (@V_{CC}OUT = 3.0 V to 3.6 V)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
RD74VT1G00CLE	WCSP-6 pin	SXBG0006KB–A (TBS-6AV)	CL	E (3,000 pcs/reel)

Article Indication



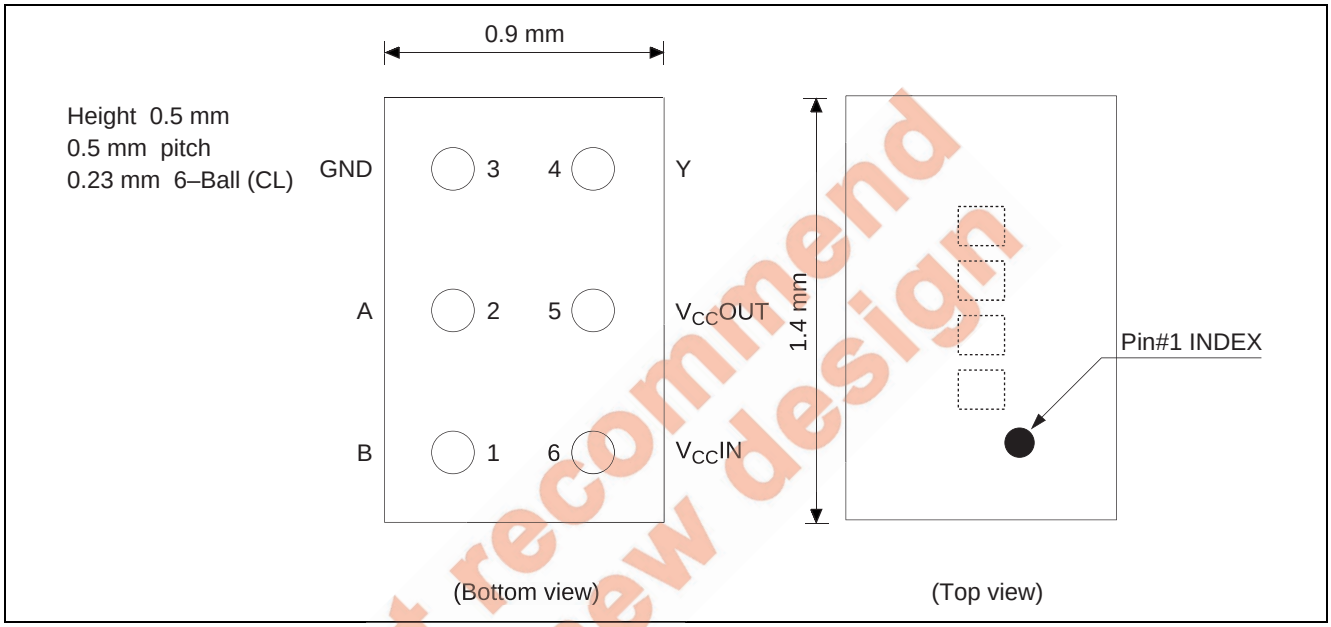
Function Table

Inputs		Output Y
A	B	
L	L	H
L	H	H
H	L	H
H	H	L

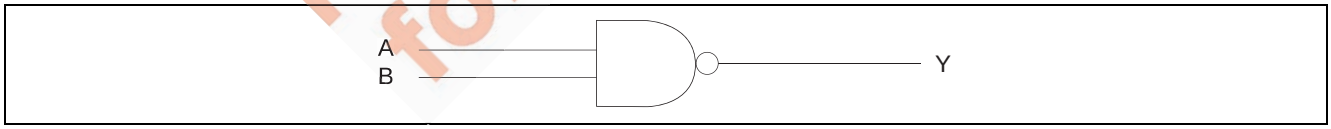
H: High level

L: Low level

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}IN, V_{CC}OUT	–0.5 to 4.6	V	
Input voltage range [*1]	V_I	–0.5 to 4.6	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC}OUT+0.5	V	Output: “H” or “L”
		–0.5 to 4.6		V_{CC}OUT: OFF
Input clamp current	I_{IK}	–50	mA	V_I < 0
Output clamp current	I_{OK}	–50	mA	V_O < 0
		50		V_O > V_{CC}+0.5
Continuous output current	I_O	±50	mA	
Continuous output current V_{CC} or GND	I_{CC}IN, I_{CC}OUT, I_{GND}	±100	mA	
Package Thermal impedance	θ_{ja}	123	°C/W	
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}IN	1.2 to 3.6	V	
	V_{CC}OUT	1.2 to 3.6		
Input/Output voltage	V_I	0 to 3.6	V	
	V_O	0 to V_{CC}OUT	V	Output: “H” or “L”
		0 to 3.6		V_{CC}OUT: OFF
Output current	I_{OH}	–2	mA	V_{CC}OUT = 1.2 V
		–4		V_{CC}OUT = 1.5±0.1 V
		–6		V_{CC}OUT = 1.8±0.15 V
		–18		V_{CC}OUT = 2.5±0.2 V
		–24		V_{CC}OUT = 3.3±0.3 V
	I_{OL}	2	mA	V_{CC}OUT = 1.2 V
		4		V_{CC}OUT = 1.5±0.1 V
		6		V_{CC}OUT = 1.8±0.15 V
		18		V_{CC}OUT = 2.5±0.2 V
		24		V_{CC}OUT = 3.3±0.3 V
Input transition rise or fall time	$\Delta t / \Delta v$	10	ns / V	
Operation free-air temperature	Ta	–40 to 85	°C	

Electrical Characteristics

(Ta = –40 to 85°C)

Item	Symbol	$V_{CC}IN$ (V) *	$V_{CC}OUT$ (V) *	Min	Typ	Max	Unit	Test conditions
Input voltage	V_{IH}	1.2	1.2 to 3.6	$V_{CC}IN \times 0.75$	—	—	V	
		1.5±0.1		$V_{CC}IN \times 0.70$	—	—		
		1.8±0.15		$V_{CC}IN \times 0.65$	—	—		
		2.5±0.2		1.6	—	—		
		3.3±0.3		2.0	—	—		
	V_{IL}	1.2	1.2 to 3.6	—	—	$V_{CC}IN \times 0.25$	V	
		1.5±0.1		—	—	$V_{CC}IN \times 0.30$		
		1.8±0.15		—	—	$V_{CC}IN \times 0.35$		
		2.5±0.2		—	—	0.7		
		3.3±0.3		—	—	0.8		
Output voltage	V_{OH}	1.2 to 3.6	1.2 to 3.6	$V_{CC}OUT$–0.2	—	—	V	I_{OH} = –100 µA
			1.2	0.9	—	—		I_{OH} = –2 mA
			1.5±0.1	1.1	—	—		I_{OH} = –4 mA
			1.8±0.15	1.25	—	—		I_{OH} = –6 mA
			2.5±0.2	1.7	—	—		I_{OH} = –18 mA
			3.3±0.3	2.2	—	—		I_{OH} = –24 mA
	V_{OL}	1.2 to 3.6	1.2 to 3.6	—	—	0.2	V	I_{OL} = 100 µA
			1.2	—	—	0.3		I_{OL} = 2 mA
			1.5±0.1	—	—	0.3		I_{OL} = 4 mA
			1.8±0.15	—	—	0.3		I_{OL} = 6 mA
			2.5±0.2	—	—	0.6		I_{OL} = 18 mA
			3.3±0.3	—	—	0.55		I_{OL} = 24 mA
Input current	I_{IN}	3.6	3.6	–1.0	—	1.0	µA	V_{IN} = GND or $V_{CC}IN$
Output leakage current	I_{OFF}	0	0	—	—	1.5	µA	V_{IN}, V_{OUT} = 0 to 3.6 V
Quiescent supply current	$I_{CC}IN$	1.2 to 3.6	1.2 to 3.6	–3.0	—	3.0	µA	$I_{O(Y\ port)}$ = 0 V_{IN} = $V_{CC}IN$ or GND
	$I_{CC}OUT$	1.2 to 3.6	1.2 to 3.6	–3.0	—	3.0		$I_{O(Y\ port)}$ = 0 V_{IN} = $V_{CC}IN$ or GND
Increase in I_{CC} per input	ΔI_{CC}	3.6	3.6	—	—	250	µA	A or B port $V_{CC}IN$–0.6 (1 input)
Input capacitance	C_{IN}	3.3	3.3	—	3.5	—	pF	V_{IN} = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$V_{CC}IN$ = 3.3±0.3 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				$V_{CC}OUT$= 1.2 V	$V_{CC}OUT$= 1.5±0.1 V		$V_{CC}OUT$= 1.8±0.15 V		$V_{CC}OUT$= 2.5±0.2 V		$V_{CC}OUT$= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A or B	Y	8.0	2.0	7.4	1.5	5.2	1.0	3.5	1.0	3.3	ns	C_L = 15pF R_L = 2.0kΩ
	t_{PHL}			8.0	2.0	7.4	1.5	5.2	1.0	3.5	1.0	3.3		

Switching Characteristics (Cont)

$V_{CC}IN$ = 2.5±0.2 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				$V_{CC}OUT$= 1.2 V	$V_{CC}OUT$= 1.5±0.1 V		$V_{CC}OUT$= 1.8±0.15 V		$V_{CC}OUT$= 2.5±0.2 V		$V_{CC}OUT$= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A or B	Y	8.0	2.0	8.0	1.5	5.5	1.0	3.9	1.0	3.5	ns	C_L = 15pF, R_L = 2.0kΩ
	t_{PHL}			8.0	2.0	8.0	1.5	5.5	1.0	3.9	1.0	3.5		

$V_{CC}IN$ = 1.8±0.15 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				$V_{CC}OUT$= 1.2 V	$V_{CC}OUT$= 1.5±0.1 V		$V_{CC}OUT$= 1.8±0.15 V		$V_{CC}OUT$= 2.5±0.2 V		$V_{CC}OUT$= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A or B	Y	8.2	2.0	8.6	1.5	6.2	1.0	4.6	1.0	4.0	ns	C_L = 15pF, R_L = 2.0kΩ
	t_{PHL}			8.2	2.0	8.6	1.5	6.2	1.0	4.6	1.0	4.0		

$V_{CC}IN$ = 1.5±0.1 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C									Unit	Test conditions
				$V_{CC}OUT$= 1.2 V	$V_{CC}OUT$= 1.5±0.1 V		$V_{CC}OUT$= 1.8±0.15 V		$V_{CC}OUT$= 2.5±0.2 V		$V_{CC}OUT$= 3.3±0.3 V			
				Typ	Min	Max	Min	Max	Min	Max	Min	Max		
Propagation delay time	t_{PLH}	A or B	Y	9.0	2.0	9.5	1.5	7.2	1.0	5.2	1.0	5.4	ns	C_L = 15pF, R_L = 2.0kΩ
	t_{PHL}			9.0	2.0	9.5	1.5	7.2	1.0	5.2	1.0	5.4		

$V_{CC}IN$ = 1.2 V

Item	Symbol	From (input)	To (output)	Ta = –40 to 85°C					Unit	Test conditions
				$V_{CC}OUT$= 1.2 V	$V_{CC}OUT$= 1.5±0.1 V	$V_{CC}OUT$= 1.8±0.15 V	$V_{CC}OUT$= 2.5±0.2 V	$V_{CC}OUT$= 3.3±0.3 V		
				Typ	Typ	Typ	Typ	Typ		
Propagation delay time	t_{PLH}	A or B	Y	9.8	7.6	6.2	5.0	4.5	ns	C_L = 15pF, R_L = 2.0kΩ
	t_{PHL}			9.8	7.6	6.2	5.0	4.5		

Operating Characteristics

Ta = 25°C

Item	Symbol	$V_{CC}IN$ (V)	$V_{CC}OUT$ (V)	Min	Typ	Max	Unit	Test conditions
Power dissipation capacitance	C_{PD}	3.3	3.3	—	12	—	pF	f = 10 MHz, C_L = 0

Power-up Considerations

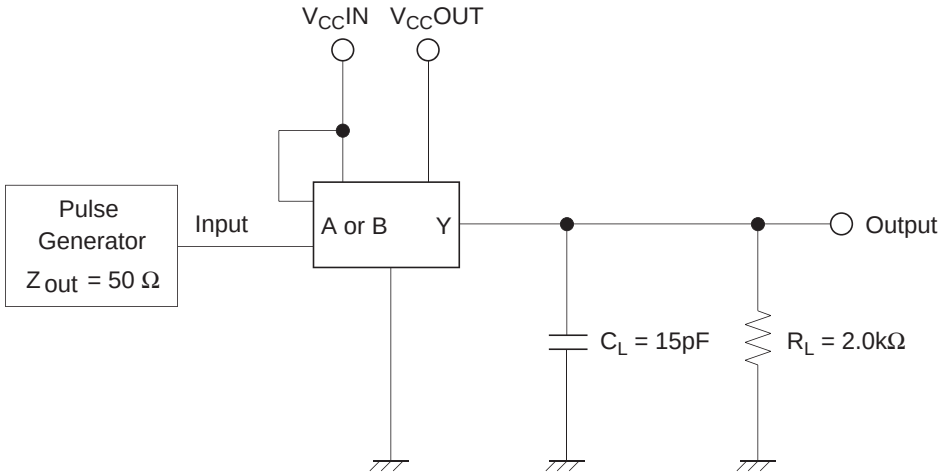
Level-translation devices offer an opportunity for successful mixed-voltage signal design.

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins.

Take these precautions to guard against such power-up problems.

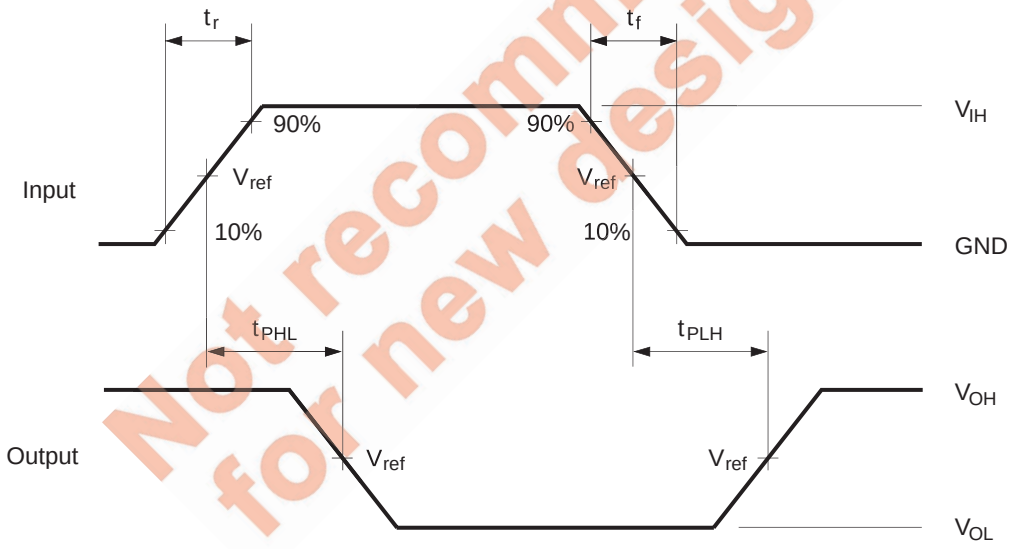
1. Connect ground before any supply voltage is applied.
2. Next, power-up the input side of the device.
   (Power up of $V_{CC}IN$ is first. Next power up is $V_{CC}OUT$)

Test Circuit



Note: C_L includes probe and jig capacitance.

• **Waveforms**

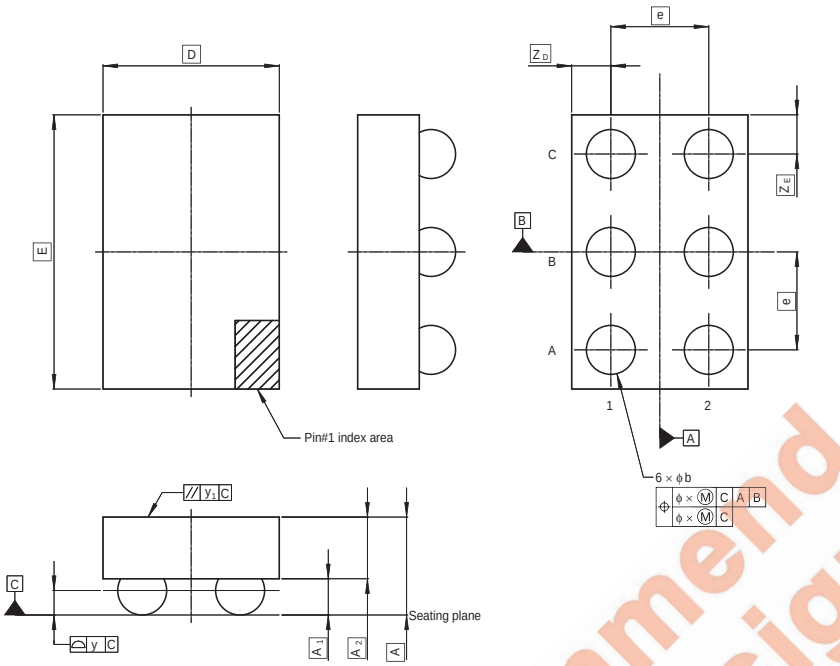


Symbol	V_{CC} = 1.2V to 3.6V
t_r / t_f	2.0 ns
V_{IH}	V_{CC}
V_{ref}	1/2 V_{CC}

Note: Input waveform : PRR ≤ 10 MHz, Z_O = 50 Ω, duty cycle 50%

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
S-XFBGA6-0.9x1.4-0.50	SXBG0006KB-A	TBS-6AV	0.001g



* Reference value.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	0.50
A_1	0.155	—	0.185
A_2	—	—	(0.315) *
b	0.20	—	0.25
D	—	0.90	—
E	—	1.40	—
e	—	0.50	—
x	—	—	0.05
y	—	—	0.05
y_1	—	—	0.20
Z_D	—	0.20	—
Z_E	—	0.20	—

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