

READ4656J

High Drivability & High Slew Rate, Output Full Range

High Voltage, Low Power Consumption

CMOS Quad Operational Amplifier

Description

The READ4656J is quad CMOS Operational Amplifier with AEC-Q100 compliant, which is the features the same performance as the Bipolar products (UPC844) about the voltage resistance (power supply voltage: 36V Max.) and high slew rate (8V/μs Typ.). This IC is the output full-range product with greatly reduced power consumption and input bias current compared to bipolar products.

Features

- AEC-Q100 Compliant
- Output full range (Rail-to-Rail output)
- Absolute Maximum Ratings
 - Power Supply Voltage $V_{DD} = -0.1 \text{ to } +36\text{V}$
 - Operating Ambient Temperature Range $T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$
- Electrical Characteristics
 - Power Supply Voltage $V_{DD} = +4.5\text{V to } +32\text{V}$
 - Input Offset Voltage $V_{IO} \leq \pm 9\text{mV}$
 - Input Bias Current $I_B \leq (1\text{pA})$
 - Supply current (per channel) $I_{DD} = 0.7 \text{ mA Typ.}, 1.0 \text{ mA Max.}$
(@ $V_{DD}=5.0\text{V}$ $T_A=-40^\circ\text{C}$ to $+125^\circ\text{C}$)
 - Slew Rate $SR = 8 \text{ V}/\mu\text{s Typ.}$

() reference value of design

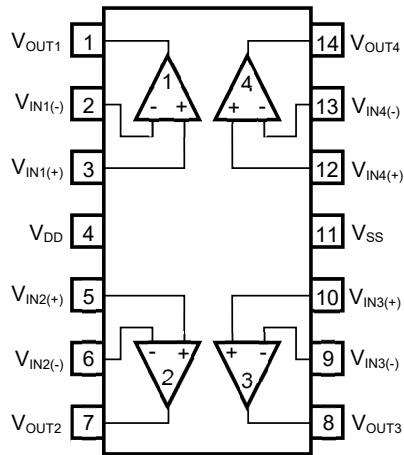
Product Line-up

Package	TSSOP
Product Name ⁽¹⁾	READ4656JSP#GC1 READ4656JSP#HC1
Quality Level	High Quality Level
Outline	Unit : mm

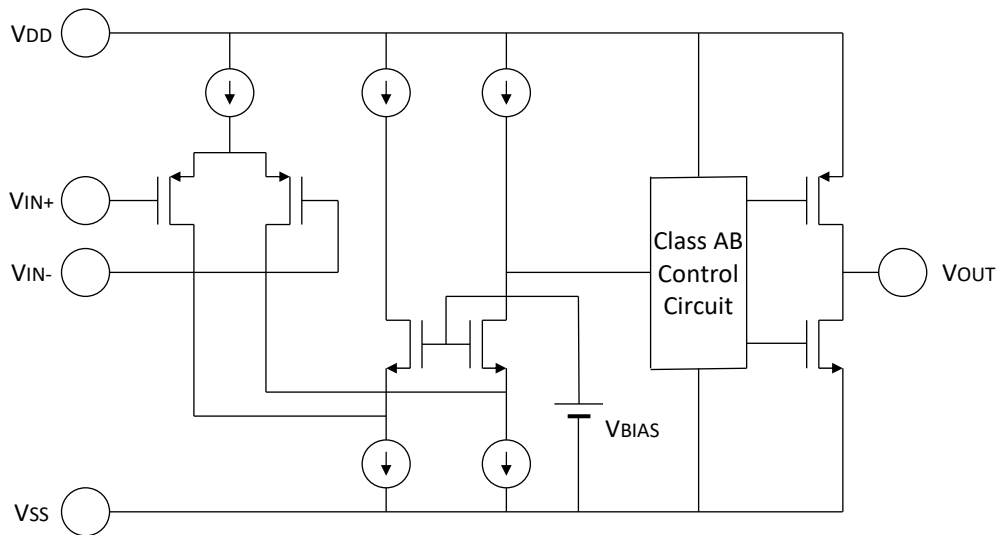
The diagram shows a top-down view of a TSSOP package. It is a rectangular component with 14 pins (7 on each long side). The overall width is 5.15 mm, the overall height is 6.40 mm, and the pin pitch is 0.65 mm. A small circle is visible on the top surface of the package.

(1). The taping direction is different for GC and HC.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<T_A=-40 to +125 °C >

Items	Symbol	Ratings	Unit
Supply voltage ^{Note.1}	V _{DD}	-0.1 to +36	V
Differential input voltage	V _{ID}	±2	V
Input voltage ^{Note.2}	V _I	V _{SS} -0.1 to V _{DD} +0.1	V
Maximum output current	I _o	20	mA
Power dissipation ^{Note.3}	P _T	550	mW
Junction temperature	T _j	-40 to +150	°C
Operating temp. range	T _A	-40 to +125	°C
Storage temp. range	T _{stg}	-55 to +150	°C

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of V_{SS} (GND)-0.1V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm x 100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern).

Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.

READ4656JSP: Derate at -7.0 mW/°C when T_A > 71 °C

(Junction – ambient thermal resistance R_{th(J-A)} = 144 °C/W)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (V _{SS} = GND)	V _{DD}	+4.5		+32	V
Power Supply Voltage (Dual Supply)	V _{DD} – V _{SS}	±2.25		±16	V

Electrical Characteristics

< T_A=25°C, V_{DD}=5.0V, V_{SS}=GND >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V _{IO}		±3	±9	mV	
Input offset current	I _{IO}			(±1)	pA	
Input bias current	I _B			(±1)	pA	
Output high voltage	V _{OH}	V _{DD} -0.3			V	I _L = 10mA
Output low voltage	V _{OL}			V _{SS} +0.3	V	I _L = 10mA
Voltage gain	A _v	60	90		dB	R _L ≥100kΩ
Channel supply current	I _{DD} /ch		0.7	1.0	mA	R _L =∞, I _o =0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V _{ICM}	V _{SS}		V _{DD} -2	V	
Gain bandwidth product	GBW		6		MHz	C _L =20pF
Slew rate	SR		8		V/μs	C _L =20pF
Channel Separation			80		dB	f = 20 Hz to 20 kHz

< T_A=25°C, V_{DD,SS}=±15 V >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V _{IO}		±3	±12	mV	
Input offset current	I _{IO}			(±1)	pA	
Input bias current	I _B			(±1)	pA	
Output high voltage	V _{OH}	V _{DD} -0.3			V	I _L = 10mA
Output low voltage	V _{OL}			V _{SS} +0.3	V	I _L = 10mA
Voltage gain	A _v	60	90		dB	R _L ≥100kΩ
Channel supply current	I _{DD} /ch		0.7	1.0	mA	R _L =∞, I _o =0
Common mode rejection ratio	CMRR	55	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V _{ICM}	V _{SS}		V _{DD} -2	V	
Gain bandwidth product	GBW		6		MHz	C _L =20pF
Slew rate	SR		8		V/μs	C _L =20pF
Channel Separation			80		dB	f = 20 Hz to 20 kHz

< T_A= -40 to +125°C, V_{DD}=5.0V, V_{SS}=GND >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input offset voltage	V _{IO}		±3	±9	mV	
Input offset current	I _{IO}		±3	±20	nA	
Input bias current	I _B		±3	±20	nA	
Output high voltage	V _{OH}	V _{DD} -0.45			V	I _L = 10 mA
Output low voltage	V _{OL}			V _{SS} +0.45	V	I _L = 10 mA
Voltage gain	A _V	60	90		dB	R _L ≥100kΩ
Channel supply current	I _{DD} /ch		0.7	1.0	mA	R _L =∞, I _O =0
Common mode rejection ratio	CMRR	50	80		dB	
Supply voltage rejection ratio	SVRR	50	80		dB	
Common mode input voltage range	V _{ICM}	V _{SS}		V _{DD} -2	V	
Gain bandwidth product	GBW		6		MHz	C _L =20pF
Slew rate	SR		8		V/μs	C _L =20pF
Channel Separation			80		dB	f = 20 Hz to 20 kHz

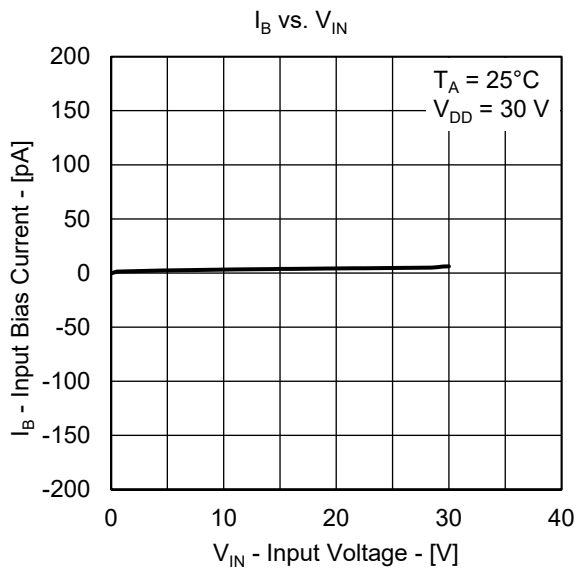
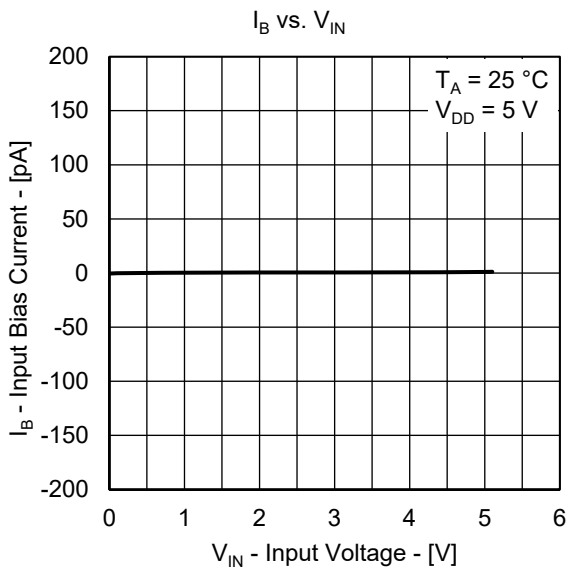
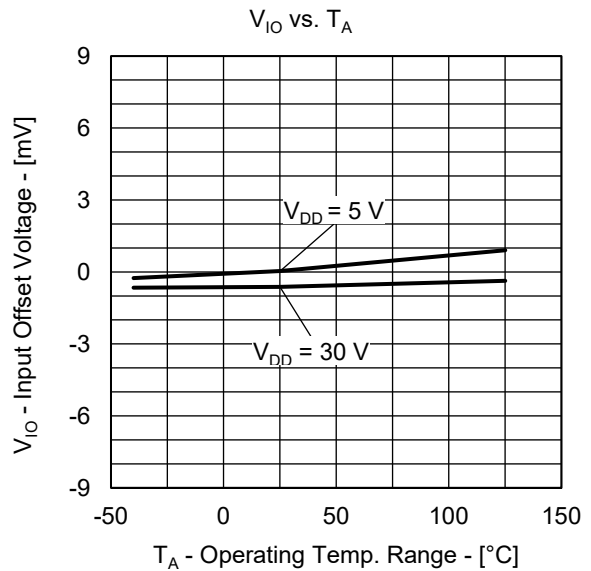
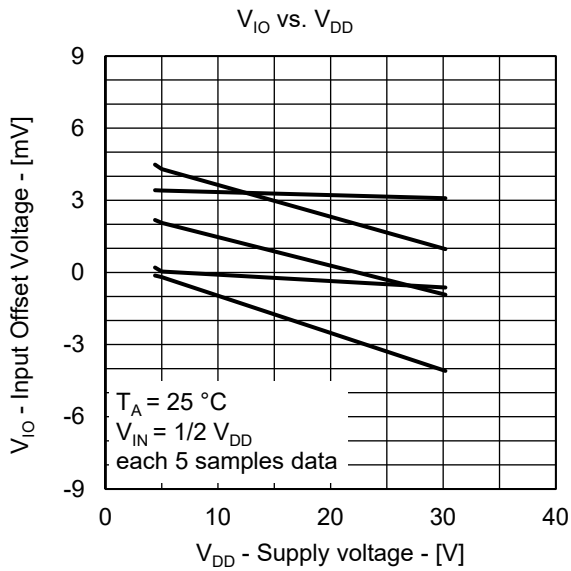
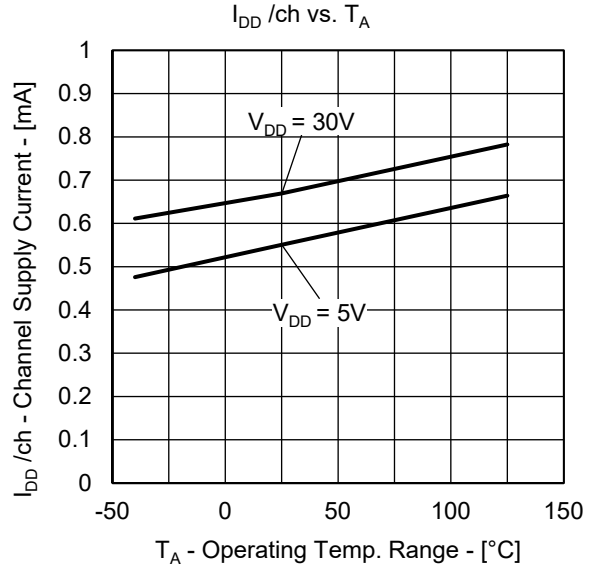
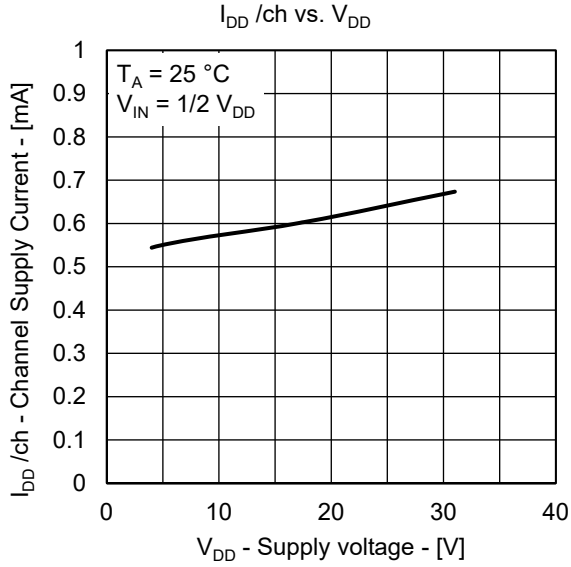
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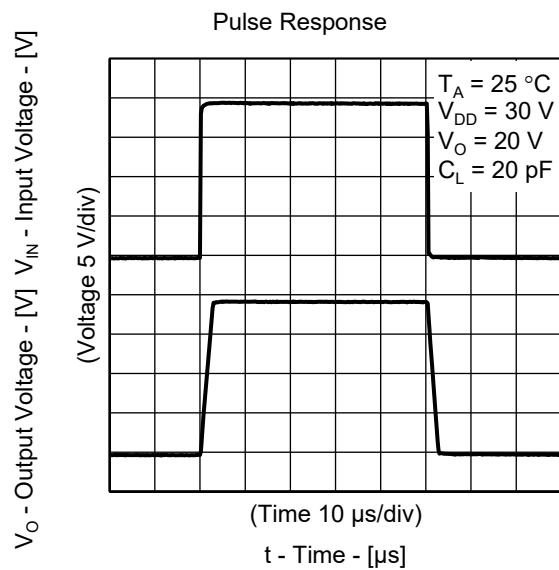
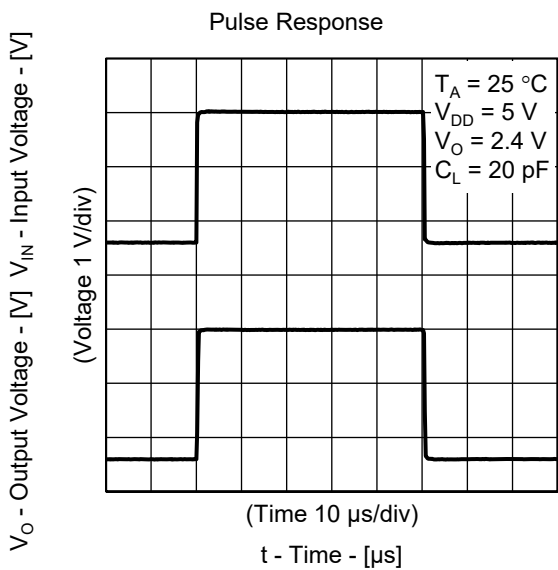
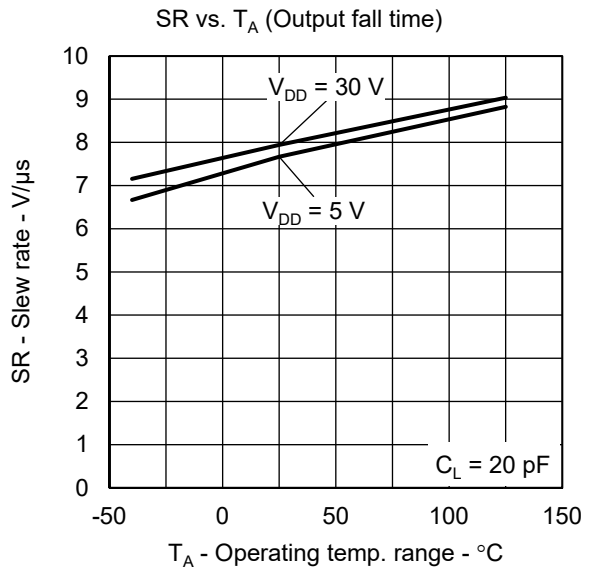
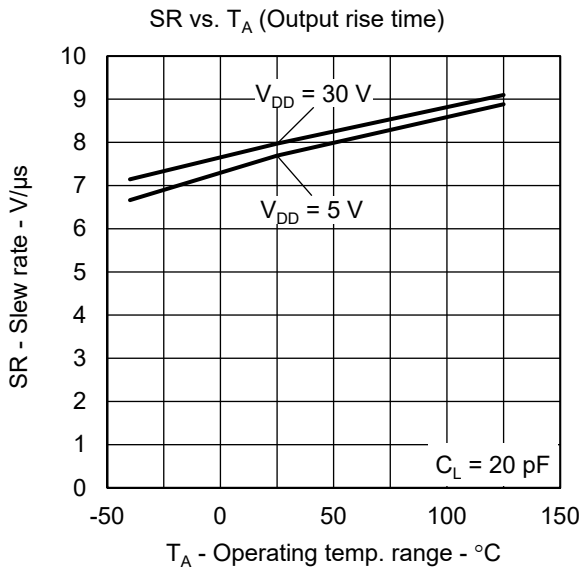
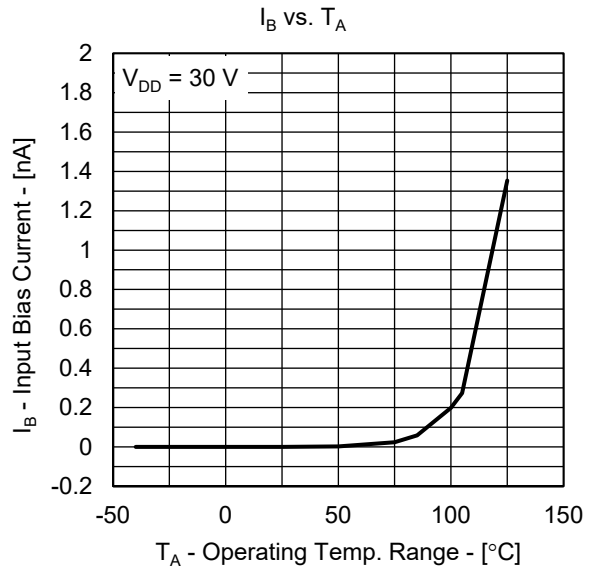
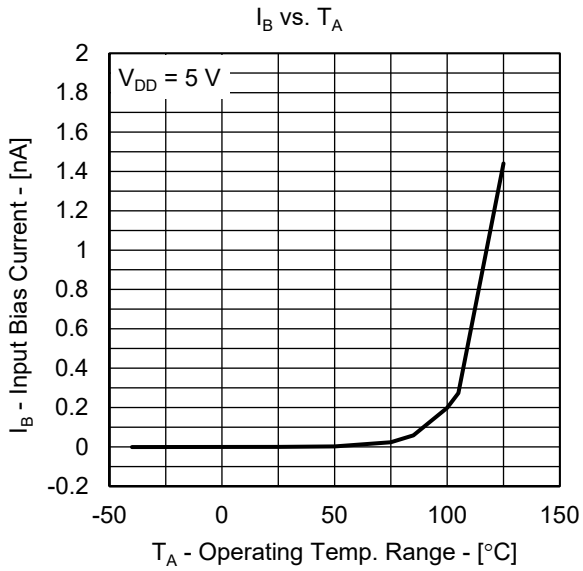
Notes

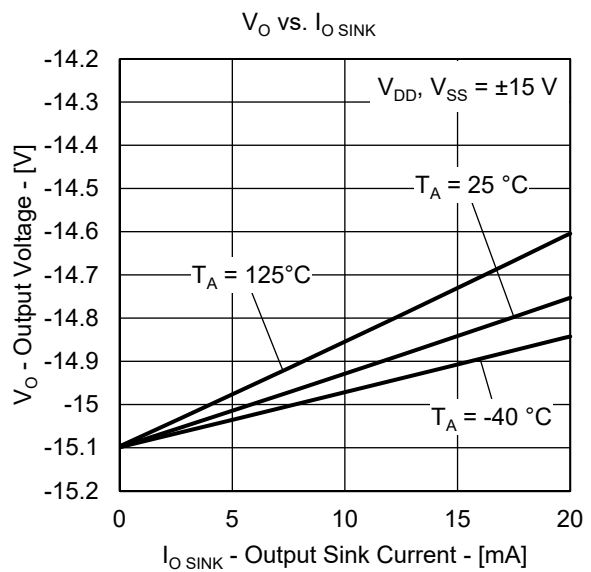
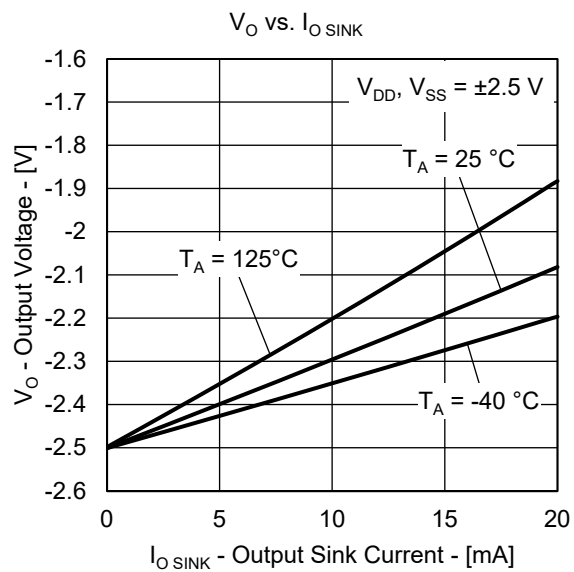
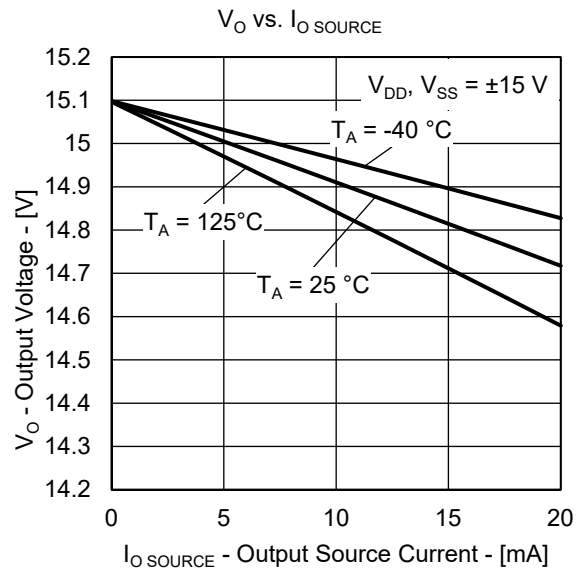
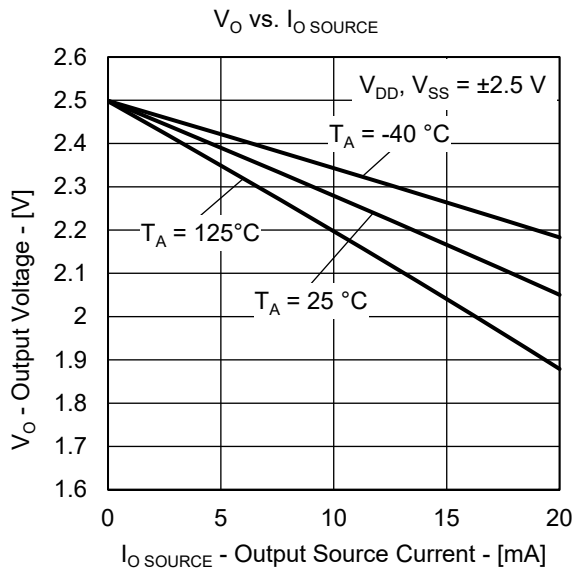
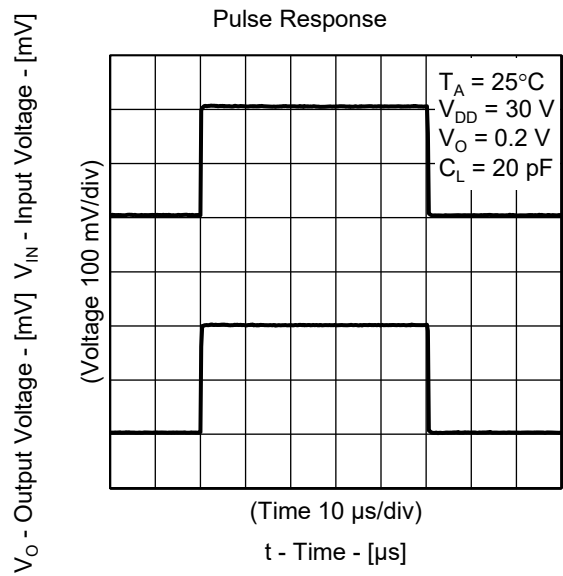
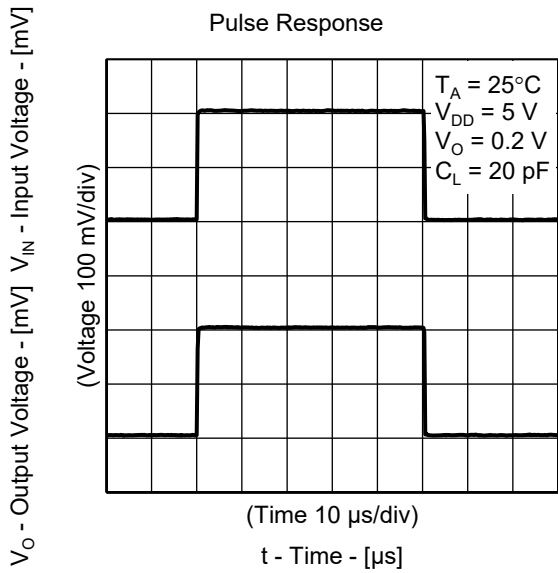
Output terminal: The over-current protection feature is not built in the output terminal of this product. Therefore, if the output is short circuit (from output to V_{DD} or from output to V_{SS}) or the forward clamp circuit using the diode at the output pin, the excessive output current may flow. Please insert the series resistor in the output pin to limit the current.

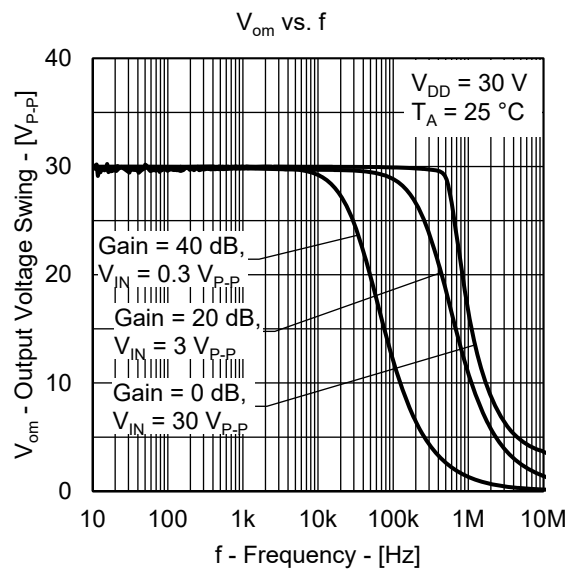
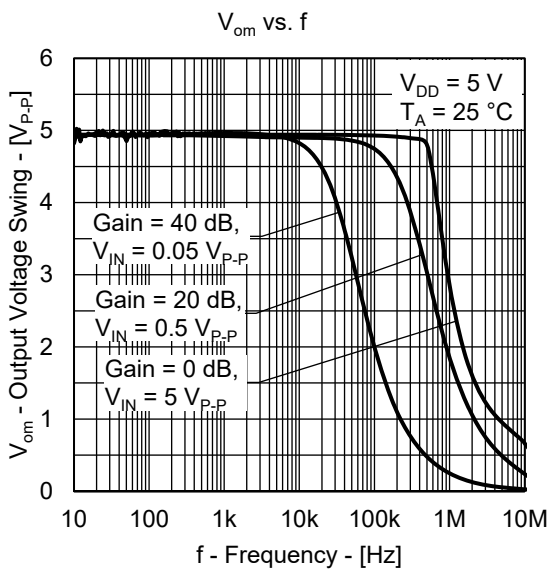
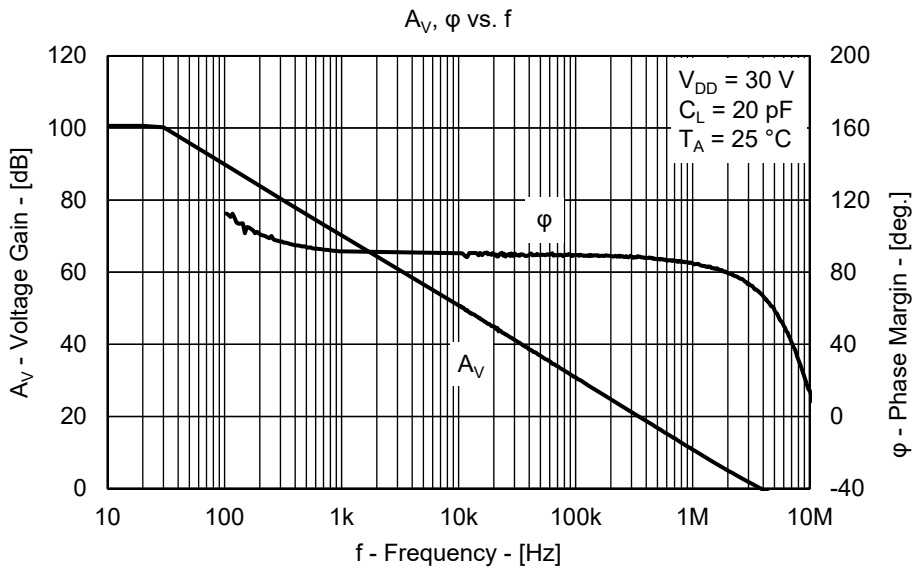
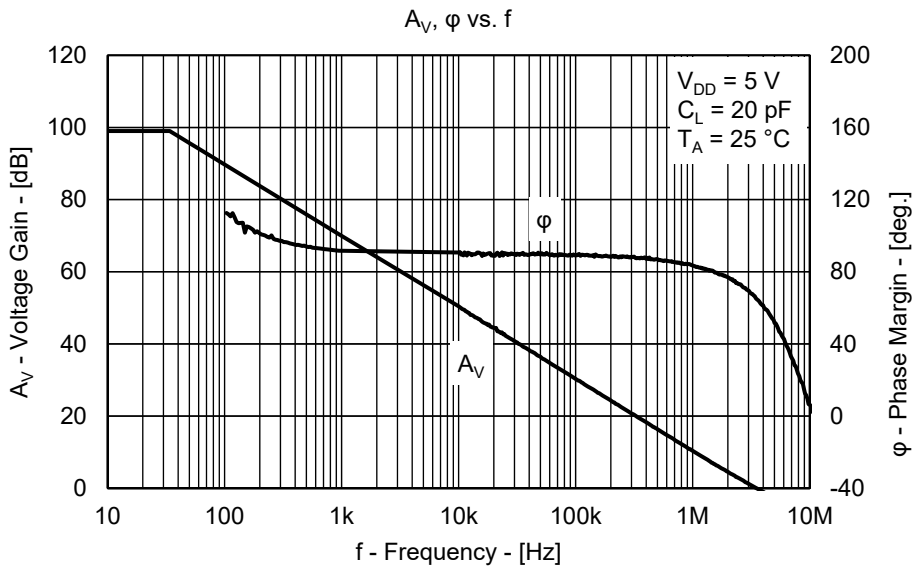
Application circuit: Please keep V_{ID} within ±2V during stationary operation and design the closed-loop operation composed feedback system: Voltage Follower, Inverting Amplifier and Non-inverting Amplifier.

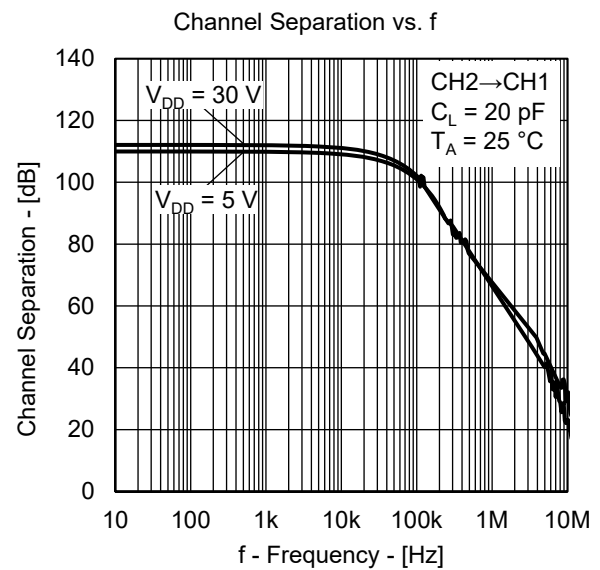
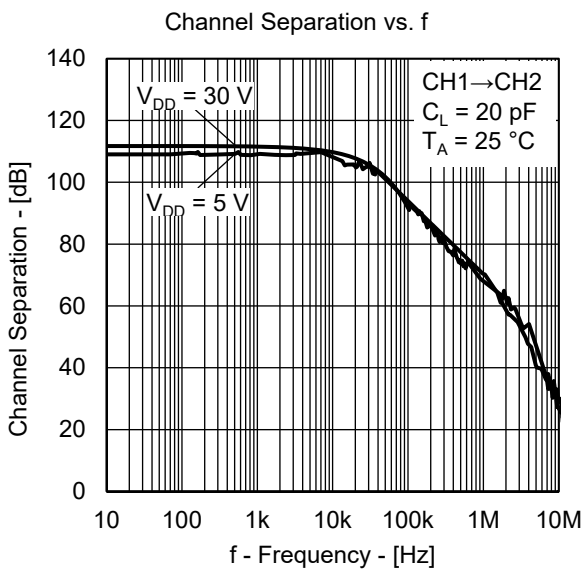
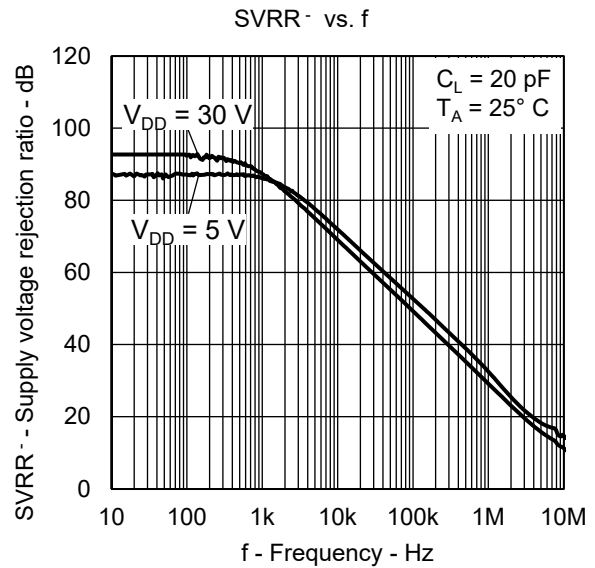
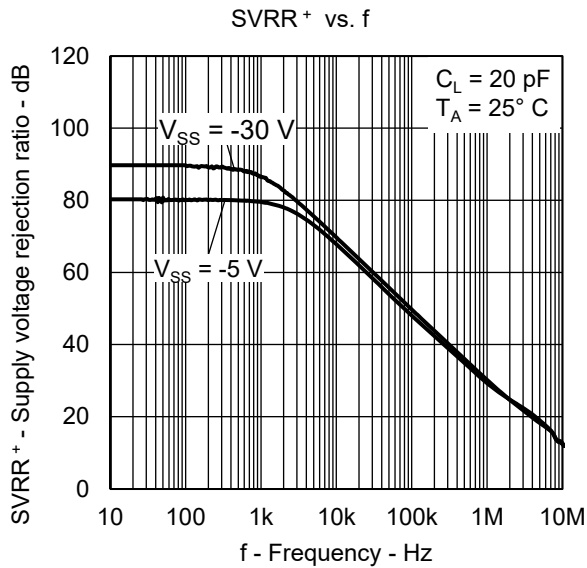
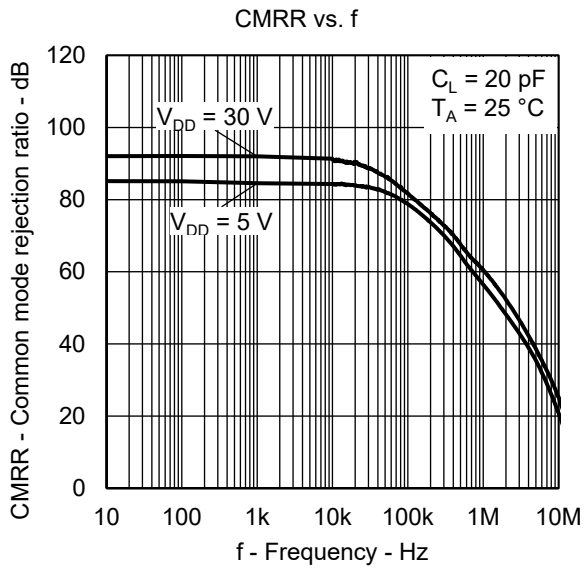
Characteristics Curve ($T_A = 25\text{ }^\circ\text{C}$) (Reference Value)

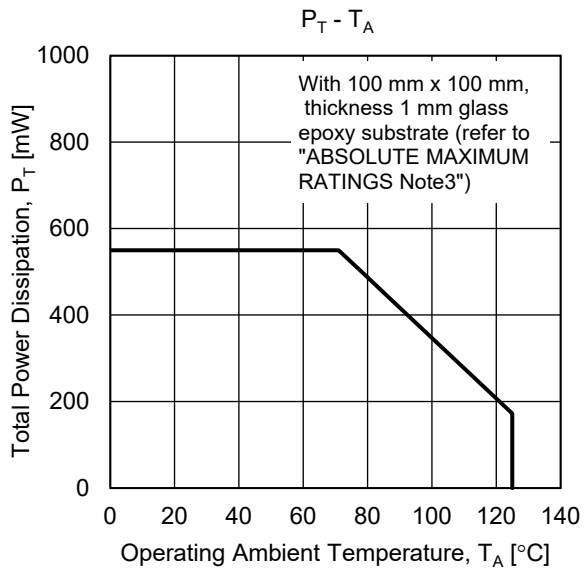










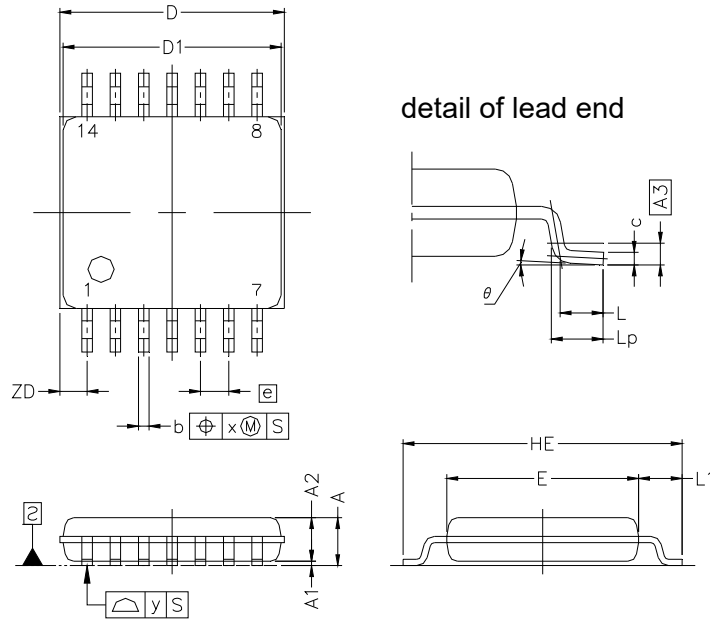


Package Dimensions

14-PIN PLASTIC TSSOP

JEITA Package Code	RENESAS Code	Previous Code	MASS(TYP.)[g]
P-TSSOP14-0225-0.65	PTSP0014JB-A	P14GR-65-9LG-1	—

Unit:mm



NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	5.15 ±0.15
D1	5.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} / _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} / _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.625

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