REAR56953A, REAR56953B

Voltage Detecting, System Resetting IC Series

DESCRIPTION

REAR56953A,B are semiconductor integrated circuits designed for detecting supply voltage and resetting all types of logic circuits such as CPUs.

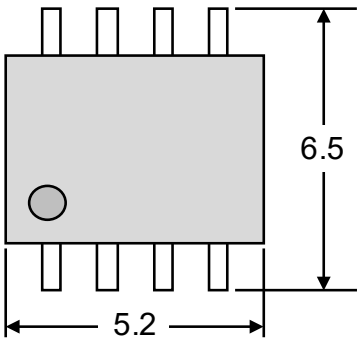
They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor.

They found extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

FEATURES

- Few external parts
- Large delay time with a capacitor of small capacitance (td ≈ 100ms, at 0.33μF)
- Low threshold operating voltage (Supply voltage to keep low-state at low supply voltage): 0.6V (Typ.) at R_L = 22kΩ
- Wide supply voltage range: 2V to 17V
- Wide application range

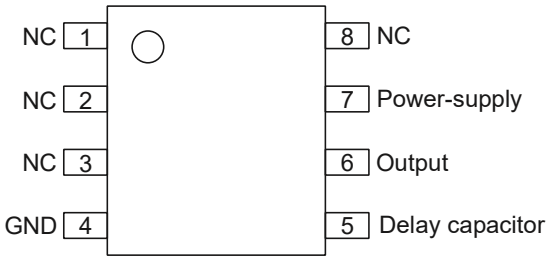
PRODUCT LINEUP

Package Type	SOP	
Part Name	REAR56953AGSM	REAR56953BGSM
Outline	Unit : mm 	

ORDERING INFORMATION

Order Name	Quality Level	Package
REAR56953AGSM#HCA	Normal Quality Level	8-Pin plastic SOP (5.72 mm (225))
REAR56953BGSM#HCA	Normal Quality Level	8-Pin plastic SOP (5.72 mm (225))

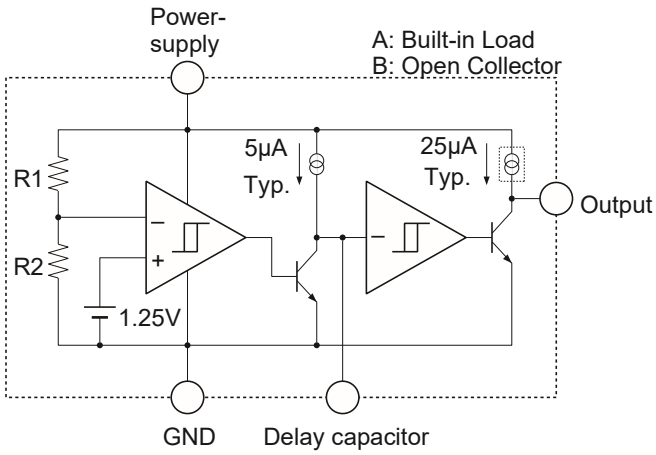
Pin Arrangement



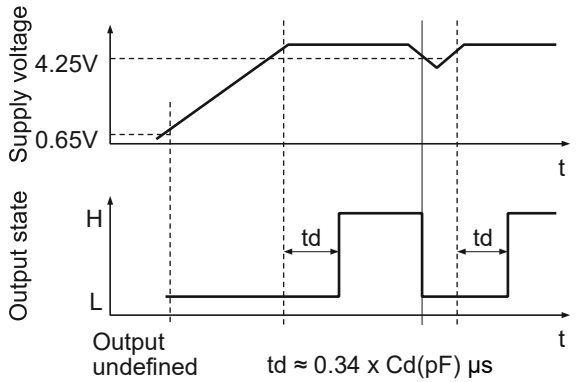
(Top view)

NC: No Connection

Block Diagram



Operating Waveform



ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply Voltage	V_{CC}	-0.3 to +18	V	
Output Sink Current	I_{SINK}	6	mA	
Output Applied Voltage	V_O	-0.3 to V_{CC}	V	Type A (Output with constant current load)
		-0.3 to +18		Type B (Open collector output)
Total Power Dissipation	Pd	440	mW	
Thermal Derating	Kθ	4.4	mW/°C	Refer to the thermal derating curve.
Operating Temperature	Topr	-40 to +85	°C	
Storage Temperature	Tstg	-55 to +125	°C	

RECOMMENDED OPERATING CONDITION

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2		17	V

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, unless otherwise noted)

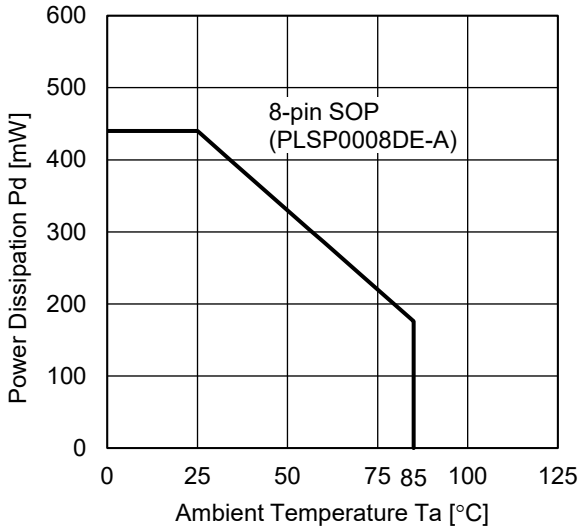
"L" Reset Type

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Detecting Voltage	V_S	4.05	4.25	4.45	V		
Hysteresis Voltage	ΔV_S	30	50	80	mV		
Detecting Voltage Temperature Coefficient	$V_S/\Delta T$		0.01		%/°C		
Circuit Current	I_{CC}		450	680	μA	Type A, V_{CC} = 5V	
			420	630		Type B, V_{CC} = 5V	
Delay Time	t_{pd}	1.6	3.4	7.0	ms	Cd = 0.01μF Note.1	
Constant Current	I_{pd}	-8	-5	-3	μA	V_{CC} = 5V	
Output Saturation Voltage	V_{sat}		0.2	0.4	V	V_{CC} = 4V, I_{SINK} = 4mA	
Threshold Operating Voltage	V_{OPL}		0.67	0.9	V	L reset type minimum supply voltage for IC operation	R_L = 2.2kΩ, V_{sat} ≤ 0.4V
			0.55	0.8			R_L = 100kΩ, V_{sat} ≤ 0.4V
Output Leakage Current	I_{OH}			30	nA	Type B, V_{out} ≤ 17V	
Output Load Current	I_{OC}	-40	-25	-17	μA	Type A, V_{CC} = 5V, V_O = 1/2 × V_{CC}	
Output High Voltage	V_{OH}	V_{CC}-0.2	V_{CC}-0.06		V	Type A	

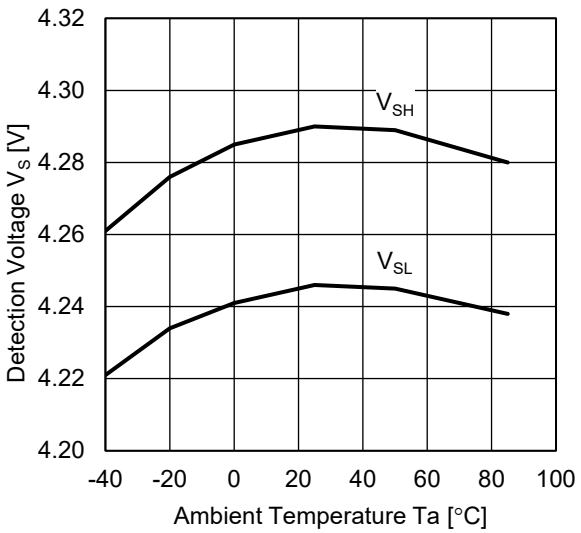
【Note】1. Please set the desired delay time by attaching capacitor of the range between 4700pF and 10μF.

TYPICAL CHARACTERISTICS

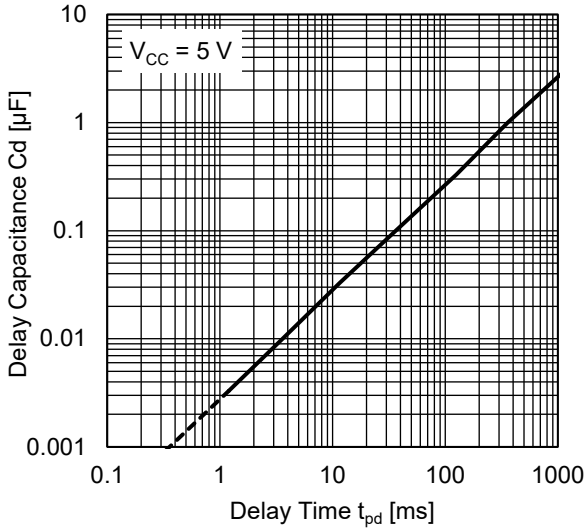
Thermal Derating



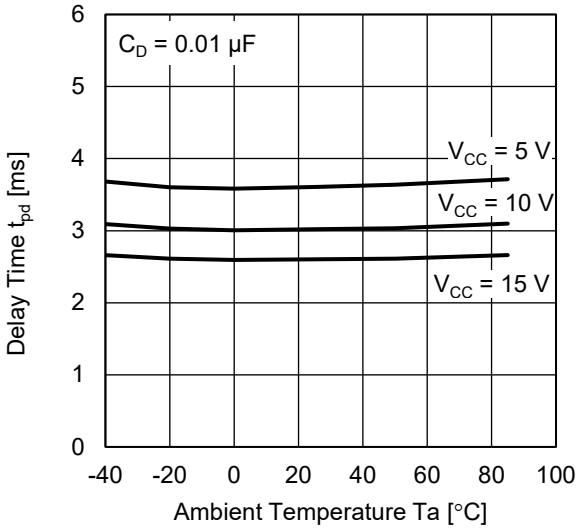
Detection Voltage vs. Ambient Temperature



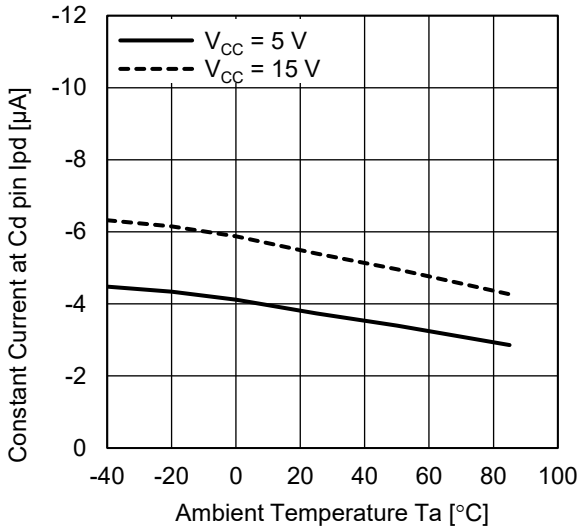
Delay Capacitance vs. Delay Time



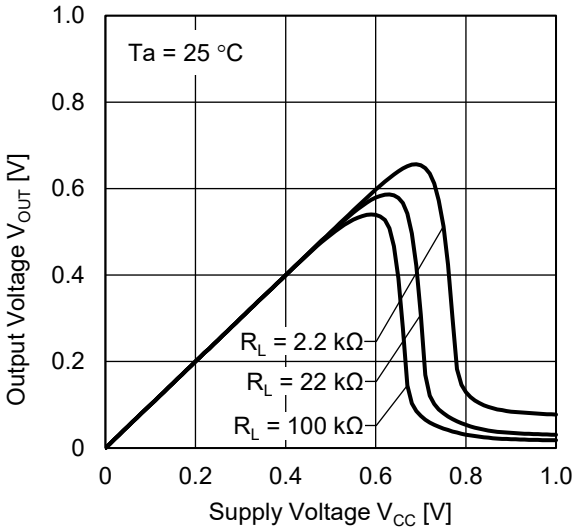
Delay Time vs. Ambient Temperature



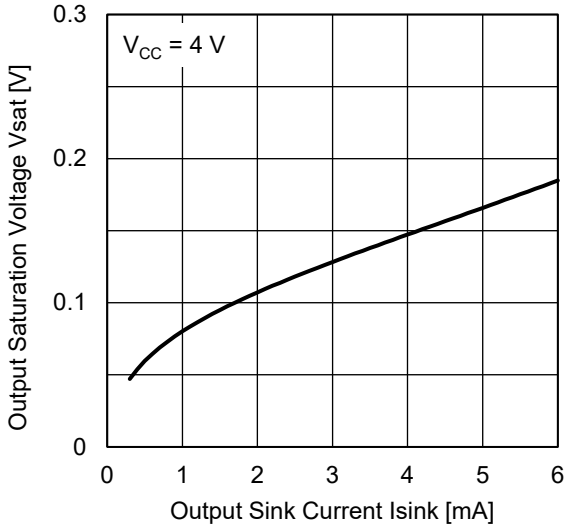
Constant Current at Cd pin vs. Ambient Temperature



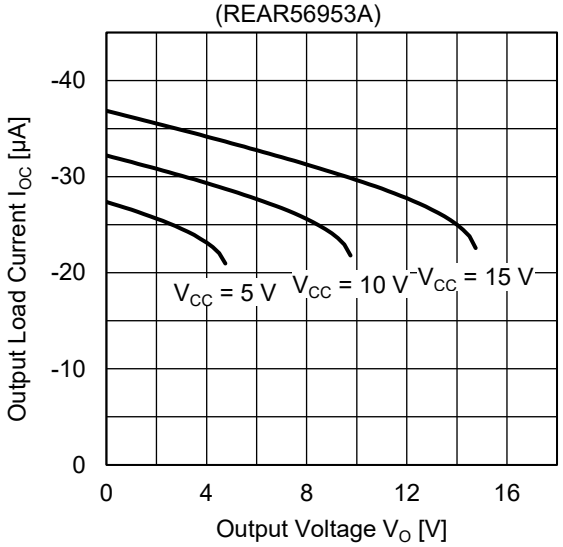
Threshold Operating Voltage



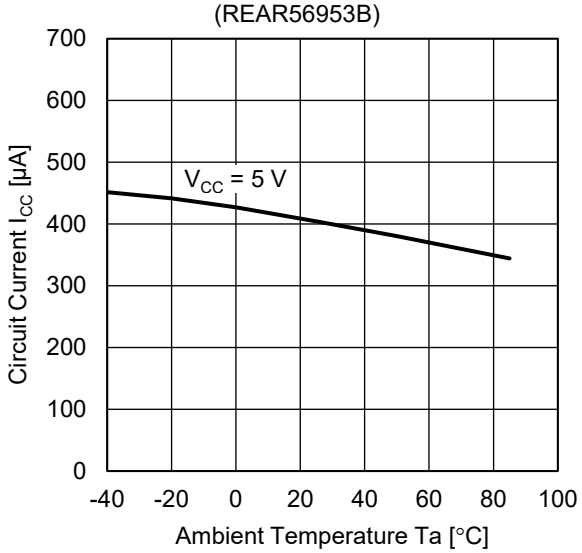
Output Saturation Voltage vs. Output Sink Current



Output Load Current vs. Output Voltage
(REAR56953A)



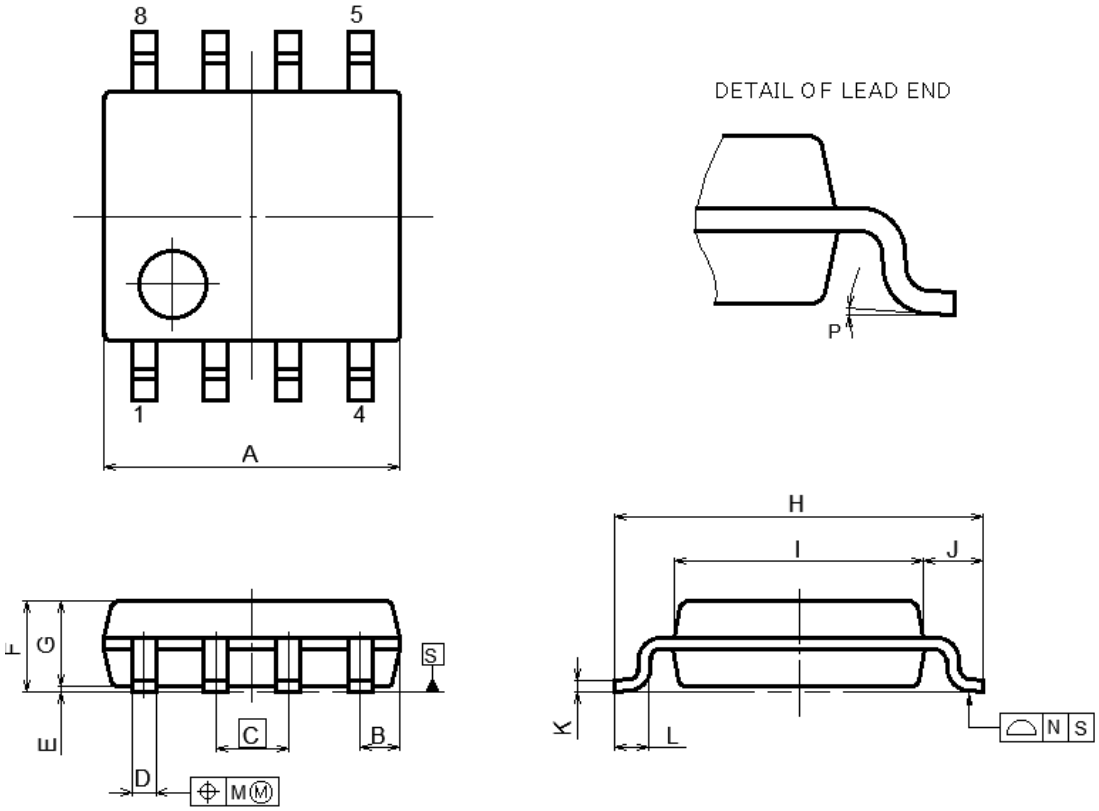
Circuit Current vs. Ambient Temperature
(REAR56953B)



PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4×5.2-1.27	PLSP0008DE-A	0.09[g]



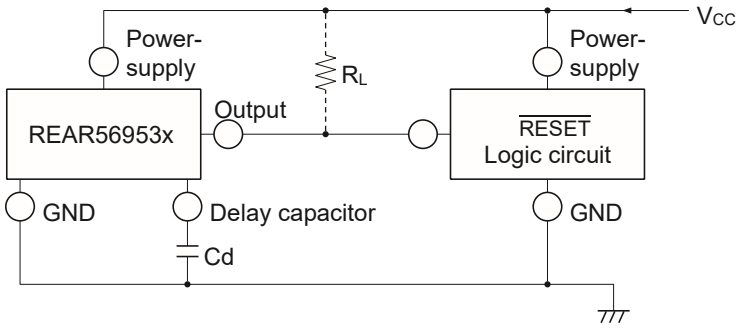
NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

EXAMPLE OF APPLICATION CIRCUIT

Reset Circuit of REAR56953

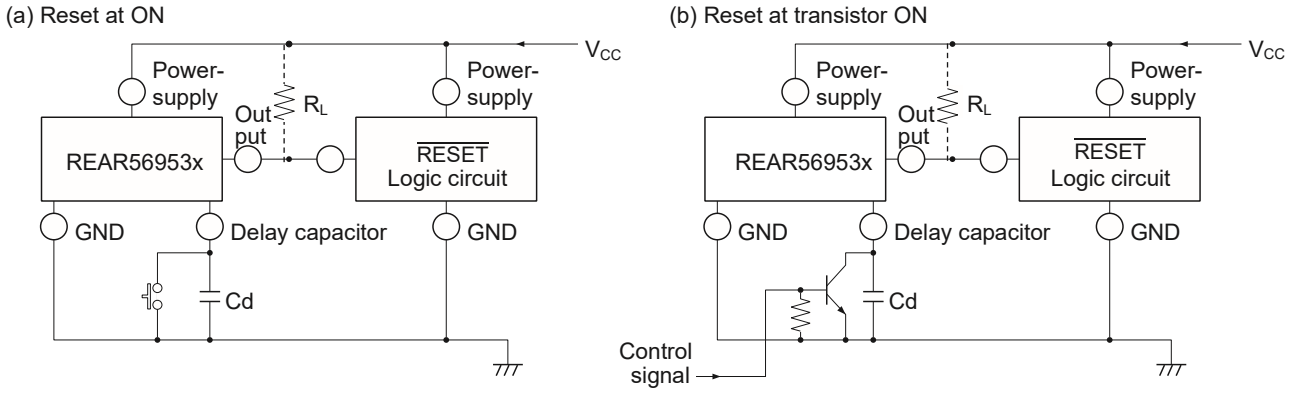


Reset Circuit of REAR56953

Notes:1. The delay time is about 0.34 × Cd (pF) μs.

2. If the REAR56953 and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
3. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor R_L to overcome the pull-down resistor.
4. When a negative supply voltage is used, the supply voltage side of REAR56953 and the GND side are connected to negative supply voltage respectively.

Case of Using Reset Signal except Supply Voltage in the REAR56953



Case of Using Reset Signal except Supply Voltage in the REAR56953

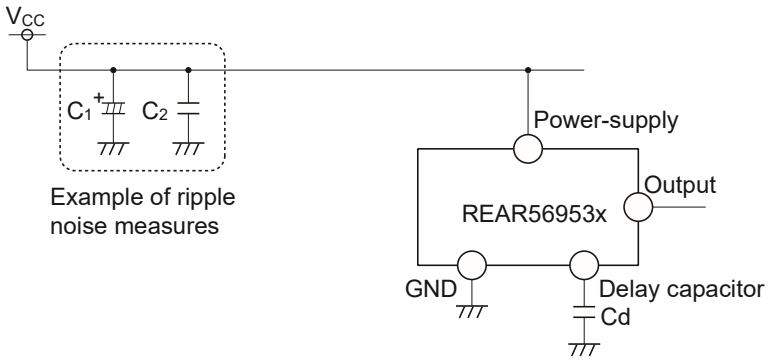
NOTICE FOR USE

About the Power Supply Line

1. About bypass capacitor

Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.

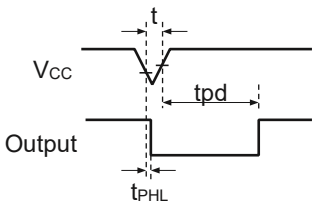
Therefore, please install C_1 and C_2 for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure.



Example of Ripple Noise Measures

Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 µF or less.
When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.



Time Chart at Momentary Voltage-Decrease

(1) The difference at delay time becomes remarkable.

A long delay setting of tens of seconds is fundamentally possible. However, when set delay time is lengthened, the range of the difference relatively grows, too. When a set value is assumed to be 'tpd', the difference occurs in the range from 0.47 × tpd to 2.05 × tpd. For instance, 34 seconds can be calculated at 100 µF. However, it is likely to vary within the ranges of 16-70 seconds.

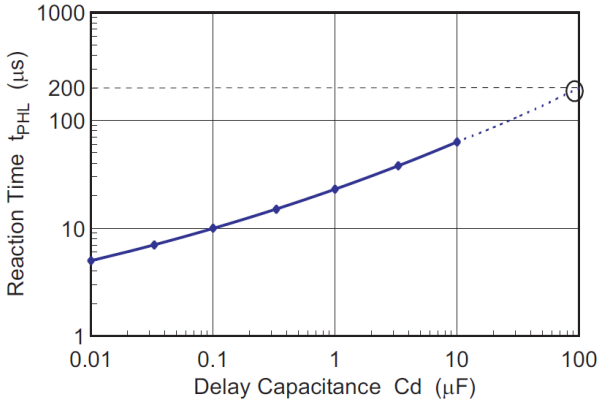
(2) Difficulty to react to a momentary voltage decrease.

For example, the reaction time t_{PHL} is 10 µs when delay capacitor Cd = 0.1 µF.
The momentary voltage-decrease that is longer than such t_{PHL} are occurs, the detection becomes possible. When the delay capacitance is enlarged, t_{PHL} also becomes long. For instance, it becomes about 100 to 200 µs in case of circuit constant C_1 = 100 µF.
(Characteristic graph 1 is used and extrapolation in case of Cd = 100µF.)
Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

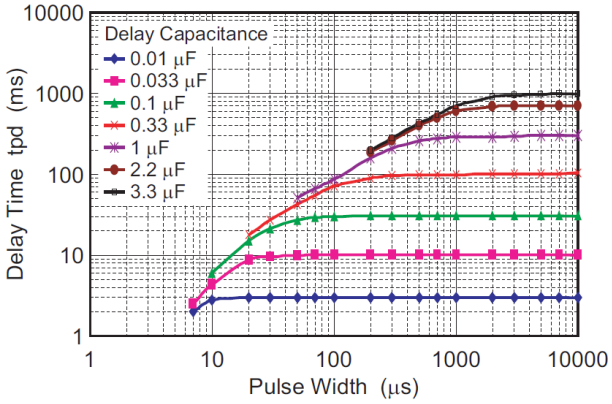
(3) Original delay time is not obtained.

When the momentary voltage-decrease time 't' is equivalent to t_{PHL}, the discharge becomes insufficient and the charge starts at that state. This phenomenon occurs at large capacitance. And, original delay time tpd is not obtained.
Please refer to characteristic graph 2. (Delay time versus input pulse width)

Characteristic Graph 1
Reaction Time vs. Delay Capacitance
(Example data)



Characteristic Graph 2
Delay Time vs. Momentary Voltage Decrease Pulse Width
(Example data)

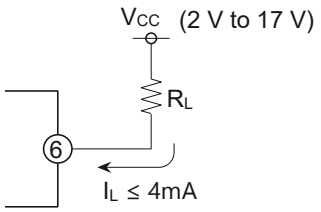


Characteristic Graph

Setting of Output Load Resistance (REAR56953B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation. Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance) R_L so that the output current (output inflow current I_L) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).



Output Load Resistance R_L

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