RH850/P1x-C

Renesas microcontroller

Section 1 Overview

RH850/P1x-C is a product series of Renesas Electronics' single-chip microcontroller RH850 family. This section describes the overview of RH850/P1x-C.

1.1 Outline

RH850/P1x-C is a 32-bit single-chip microcontroller with multiple CPUs, Code Flash, Data Flash, RAM modules, DMA controllers, many communication interfaces that are used in the automotive applications, A/D converters, timer units, etc. This chip is oriented to the automotive applications which comply with functional safety standard (ISO26262).

The main features are as below.

(1) RH850 multi-core CPU
This chip equips one or two RH850 G3M unit(s) as main CPU(s) depending on the product type, and each CPU unit has Lock-Step Dual Core feature for the functional safety. In addition to that, the chip equips one RH850 G3K unit as a sub CPU which controls security functionality (depending on product type).
The architecture of these CPUs realizes the compact footprint of the programs by 2-byte basic instructions and high-level language compiler oriented instruction sets. These CPUs have very quick interrupt response time so that they can support hard real-time applications.

(2) On-Chip Code Flash and Data Flash
This chip has high-speed Code Flash from which the CPU can fetch the instructions and the constant data. Its capacity is up to 8MB for the Production Device and 10MB for the Emulation Device. This Code Flash can be reprogrammed in the situation that the chip is mounted in the application systems.
This chip also has Data Flash with EEPROM emulation capability. Its capacity is up to 224KB.

(3) Rich peripheral functionality
This chip equips not only common communication interfaces such as SPI and HS-USRT but also automotive oriented ones such as MCAN, FlexRay, RLIN, SENT. In addition, it also supports Ethernet (depending on product type). As internal peripheral modules, the chip has A/D Converter, System Timer, Generic Timer Module, and dedicated Peripheral Interconnect module which connects the functionalities of these peripherals.

(4) Functional Safety support
This chip equips several dedicated functionalities including the Lock-Step Dual Core configuration for the CPU, the memory protection with ECC, the bus protection with ECC, the peripheral module protection, and voltage / clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(5) Security support
This chip supports various security features (depending on product type). The Intelligent Cryptographic Unit – Master (ICUMC) has a dedicated secure CPU (RH850G3K) and some secure peripherals such as AES engine and Random Number Generator (RNG). The chip also realizes the HW-level domain separation between non-secure and secure domains. The internal resources such as Code- and Data-Flash can be assigned to either domain and the secure domain is protected against non-secure accesses by the HW mechanism. The chip also has the protection scheme for a malicious access from external.

1.2 Product List

Table 1.1 Product list and package

Product Name	Product type	Package	Package Name	Note
R7F701370A	P1H-CE	BGA404	R7F701370AEEBG	
R7F701370B	P1H-CE	BGA404	R7F701370BEEBG	CAN-FD
R7F701371	P1H-C (8MB)	BGA292	R7F701371EABG	CAN-FD
R7F701372	P1H-C (4MB)	BGA292	R7F701372EABG	
R7F701372A	P1H-C (4MB)	BGA292	R7F701372AEABG	CAN-FD
R7F701396A	P1H-C (4MB)	BGA156	R7F701396AEABG	CAN-FD
R7F701373	P1M-C	BGA292	R7F701373EABG	
R7F701373A	P1M-C	BGA292	R7F701373AEABG	CAN-FD
R7F701374	P1M-C	LQFP144	R7F701374EAFP	
R7F701374A	P1M-C	LQFP144	R7F701374AEAFP	CAN-FD
R7F701397A	P1M-C	BGA156	R7F701397AEABG	CAN-FD

For better readability common Product Short Names will be used in this manual.

Wherever a more detailed distinction of the device is required either the specific Product Name (R7Fxxxx) or the nickname followed by further information in brackets (e.g. “P1M-C (BGA-292)”) will be used.

Product		RH850/P1x-C						
Product Short Name		P1M-C			P1H-C (4MB)		P1H-C (8MB)	P1H-CE
Package		QFP-144	BGA		BGA		BGA-292	BGA-404
			BGA-156	BGA-292	BGA-156	BGA-292		
	Package Extension to Product Name	EAFP	EABG					EEBG
Product name	Non-CANFD	R7F701374	—	R7F701373	—	R7F701372	—	R7F701370A
	CANFD	R7F701374A	R7F701397A	R7F701373A	R7F701396A	R7F701372A	R7F701371	R7F701370B

- “P1x-C” refers to all products covered in this document.
- “P1M-C” refers to all P1M-C variants regardless of package (QFP, BGA).
- “P1M-C(BGA-292)” refers to a subset of P1M-C devices, i.e. all “P1M-C” in the BGA package with 292 balls

Table 1.2 Features in each product (1/2)

Category	Item	Sub-item	unit	P1M-C	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
CPU Subsystem	PE1	CPU Core	—	RH850 G3M	RH850 G3M	RH850 G3M	RH850 G3M
		LSDC	—	Yes	Yes	Yes	Yes
		Clock Freq.	MHz	120, 160, 240	160, 240	160, 240	120, 160, 240
		FPU	—	Yes	Yes	Yes	Yes
		I-Cache	KB	16	16	16	16
		MPU	ch	16	16	16	16
		INTC1	ch	32	32	32	32
		Local RAM	KB	128	64	64	128
	PE2	CPU Core	—	—	RH850 G3M	RH850 G3M	RH850 G3M
		LSDC	—	—	Yes	Yes	Yes
		Clock Freq.	MHz	—	160, 240	160, 240	120, 160, 240
		FPU	—	—	Yes	Yes	Yes
		I-Cache	KB	—	16	16	16
		MPU	ch	—	16	16	16
		INTC1	ch	—	32	32	32
		Local RAM	KB	—	64	64	64
	Global RAM		KB	320	960	960	1344
	Total RAM	LRAM + GRAM	KB	448	1088	1088	1536
	INTC2		ch	224	224	224	224
	DMA	DMAC	ch	16	16	16	16
		DTS	ch	128	128	128	128
Flash Memory	Code Flash		MB	2	4	8	8
	Extra Code Flash (ED only)		MB	—	—	—	2
	ERAM (Calibration RAM: ED only)		MB	—	—	—	2
	Data Flash	NonSecure	KB	64	128	192	192
		Secure	KB	32	32	32	32
Security	ICUMC	CPU Core	—	RH850 G3K	RH850 G3K	RH850 G3K	RH850 G3K
		Clock Freq.	MHz	60, 80	80	80	60, 80
	BasicHardwareProtecton		—	Yes	Yes	Yes	Yes
	Secure WDT		ch	1	1	1	1
External Bus			—	No	P1H-C (4MB, BGA-292): Yes P1H-C (4MB, BGA-156): No	Yes	Yes
A/D Converter	Module		instance	2	2	2	2
	Analog input		ch	P1M-C (QFP): 20 P1M-C (BGA-292): 24 P1M-C (BGA-156): 16	P1H-C (4MB, BGA-292): 32 P1H-C (4MB, BGA-156): 16	40	40
	Voltage		V	3.3	3.3	3.3	3.3
Timers	System Timer		instance	1	2	2	2
	WDT		instance	1	2	2	2
	PIC		—	Yes	Yes	Yes	Yes
	GTM		—	Config 2	Config 3	Config 3	Config 3

Table 1.2 Features in each product (2/2)

Category	Item	Sub-item	unit	P1M-C	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
Communication Interface	MCAN		ch	2	2	3	3
	M_TTCAN		ch	1	1	1	1
	FlexRay		ch	2	P1H-C (4MB, BGA-292): 4 P1H-C (4MB, BGA-156): 2	4	4
	Ethernet		port	1	P1H-C (4MB, BGA-292): 2 P1H-C (4MB, BGA-156): 1	2	2
	SENT		ch	P1M-C (QFP, BGA-292): 6 P1M-C (BGA-156): 4	P1H-C (4MB, BGA-292): 8 P1H-C (4MB, BGA-156): 4	8	10
	HS-USRT		ch	2	P1H-C (4MB, BGA-292): 4 P1H-C (4MB, BGA-156): 2	4	4
	RLIN		ch	2	P1H-C (4MB, BGA-292): 4 P1H-C (4MB, BGA-156): 2	4	4
	CSIH (SPI)	# of ch	ch	4	4	4	4
		# of CS	pin	P1M-C (QFP): 28 (8/8/8/4) P1M-C (BGA-292): 30 (8/8/8/6) P1M-C (BGA-156): 24 (8/8/6/2)	P1H-C (4MB, BGA-292): 32 (8/8/8/8) P1H-C (4MB, BGA-156): 24 (8/8/6/2)	32 (8/8/8/8)	32 (8/8/8/8)
Safety	ECM		—	Yes	Yes	Yes	Yes
	Data CRC		ch	4	8	8	8
Internal Monitors	Clock		—	Yes	Yes	Yes	Yes
	Core Voltage		—	Yes	Yes	Yes	Yes
	Temperature		—	Yes	Yes	Yes	Yes
Debug	Debug Control		—	JTAG, LPD	JTAG, LPD	JTAG, LPD	JTAG, LPD
	Branch Trace		—	—	—	—	Yes
	Data Trace		—	—	—	—	Yes
	Trace I/F		—	—	—	—	Aurora 2 lanes Max 6.25 Gbps (3.125 Gbps/ lane)
	Bypass I/F		—	—	—	—	AUD Max 200 Mbps
Power Supply	Core		V	P1M-C (QFP, BGA-292): 1.25 (DPS), eVR P1M-C (BGA-156): 1.25 (DPS)	1.25	1.25	1.25
	I/O		V	3.3	3.3	3.3	3.3
	ADC		V	3.3	3.3	3.3	3.3

Table 1.3 Abbreviation table

Full name	Abbreviation
External Memory Controller	MEMC
Interrupt Controller	INTC
Direct Memory Access Controller	DMAC
Data Transfer System	DTS
Clocked Serial Interface H	CSIH
High-Speed Universal Synchronous Receiver / Transmitter	HS-USRT
FlexRay	FLX
Ethernet Controller	ETNA
Window Watchdog Timer	WDTA
System Timer	STM
Generic Timer Module	GTM
Peripheral Interconnect	PIC
AD Converter	ADCF
Error Control Module	ECM
Data CRC Function	DCRB
Core Voltage Monitor	CVM
Clock Monitor	CLMA
Temperature Sensor	OTS
On-Chip Debug	OCD
Emulation Device	ED
Intelligent Cryptographic Unit – Master	ICUMC

1.3 Pin Connection Diagrams

1.3.1 P1M-C (QFP-144) (TOP View)

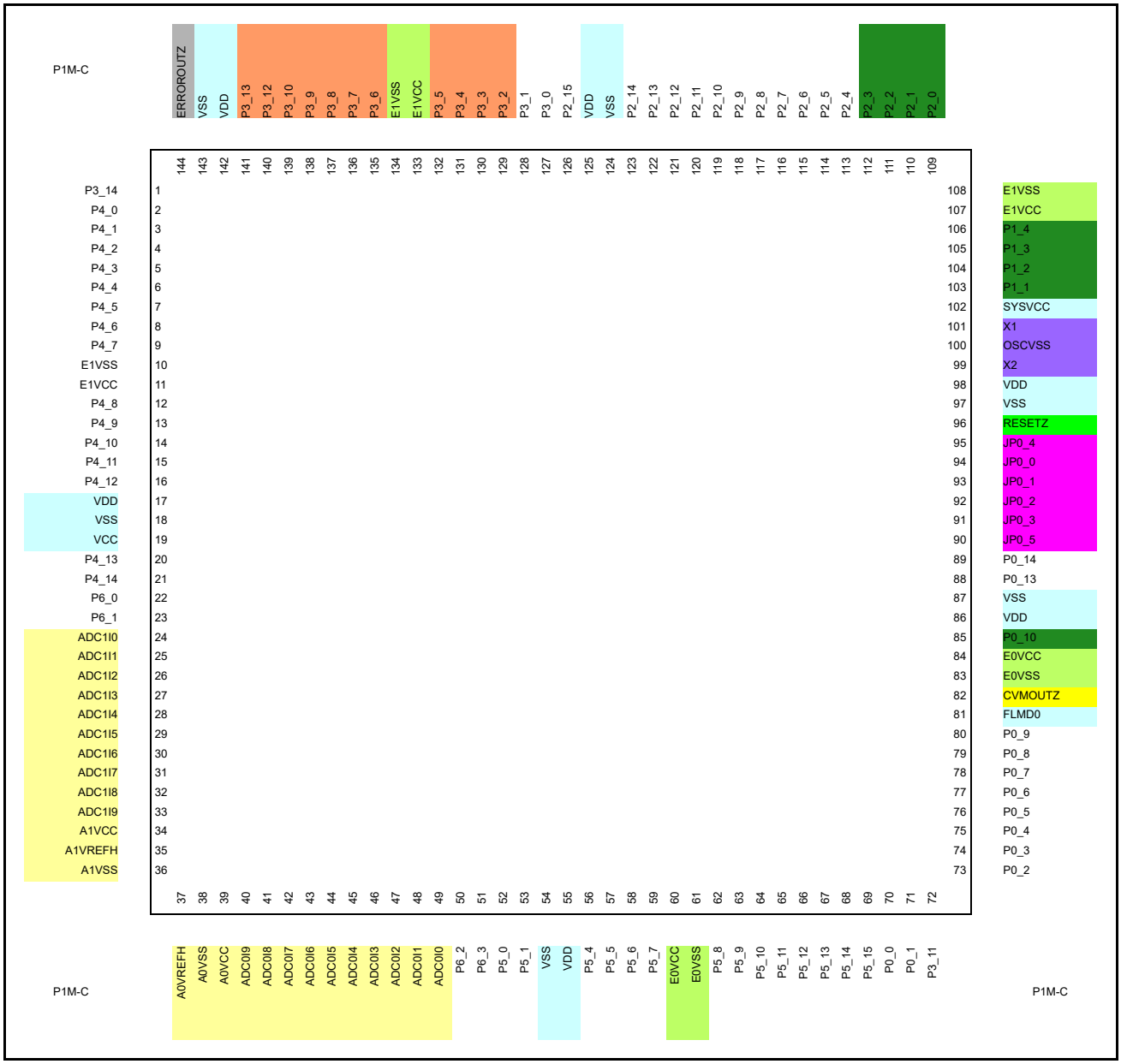
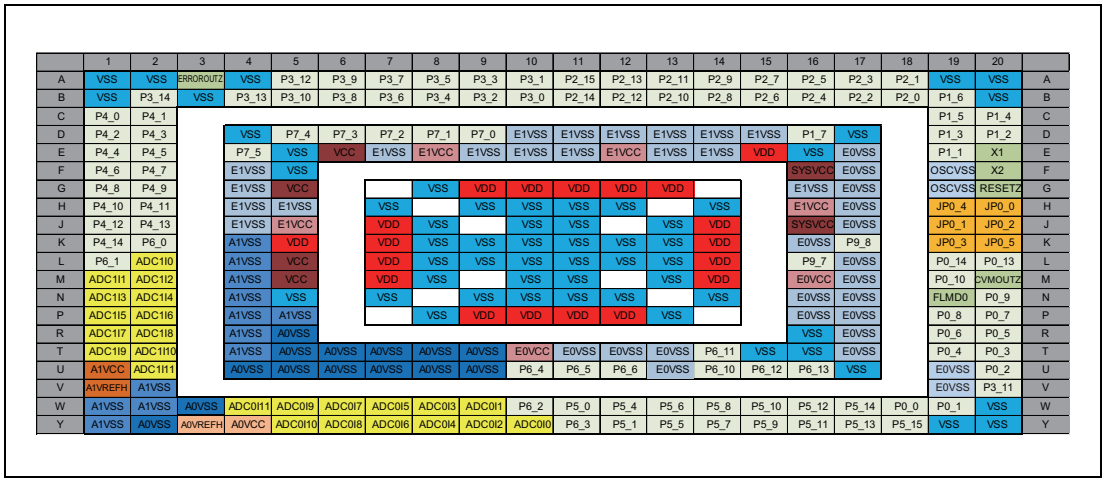


Figure 1.1 Pin Connection Diagram of P1M-C (QFP-144)

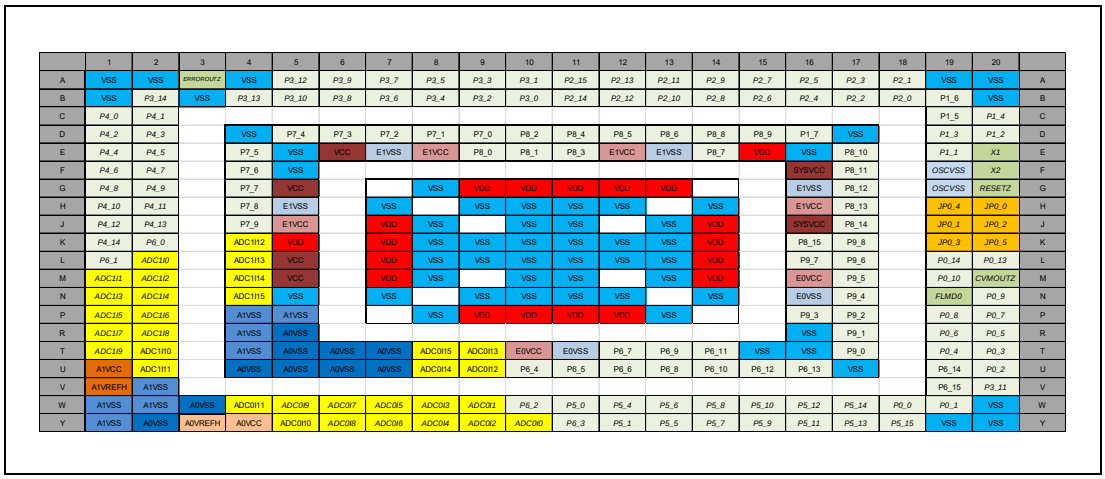
1.3.2 P1M-C (BGA-292) (TOP View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	ERROROUTZ	VSS	P3_12	P3_9	P3_7	P3_5	P3_3	P3_1	P2_15	P2_13	P2_11	P2_9	P2_7	P2_5	P2_3	P2_1	VSS	VSS	A
B	VSS	P3_14	VSS	P3_13	P3_10	P3_8	P3_6	P3_4	P3_2	P3_0	P2_14	P2_12	P2_10	P2_8	P2_6	P2_4	P2_2	P2_0	P1_6	VSS	B
C	P4_0	P4_1																	P1_5	P1_4	C
D	P4_2	P4_3		VSS	P7_4	P7_3	P7_2	P7_1	P7_0	E1VSS	E1VSS	E1VSS	E1VSS	E1VSS	E1VSS	P1_7	VSS		P1_3	P1_2	D
E	P4_4	P4_5		P7_5	VSS	VCC	E1VSS	E1VCC	E1VSS	E1VSS	E1VSS	E1VCC	E1VSS	E1VSS	VDD	VSS	E0VSS		P1_1	X1	E
F	P4_6	P4_7		E1VSS	VSS											SYSVCC	E0VSS		OSCVSS	X2	F
G	P4_8	P4_9		E1VSS	VCC			VSS	VDD	VDD	VDD	VDD	VDD			E1VSS	E0VSS		OSCVSS	RESETZ	G
H	P4_10	P4_11		E1VSS	E1VSS		VSS		VSS	VSS	VSS	VSS		VSS		E1VCC	E0VSS		JP0_4	JP0_0	H
J	P4_12	P4_13		E1VSS	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		SYSVCC	E0VSS		JP0_1	JP0_2	J
K	P4_14	P6_0		A1VSS	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		E0VSS	P9_8		JP0_3	JP0_5	K
L	P6_1	ADC1I0		A1VSS	VCC		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P9_7	E0VSS		P0_14	P0_13	L
M	ADC1I1	ADC1I2		A1VSS	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	E0VSS		P0_10	CVMOUTZ	M
N	ADC1I3	ADC1I4		A1VSS	VSS		VSS		VSS	VSS	VSS	VSS		VSS		E0VSS	E0VSS		FLMD0	P0_9	N
P	ADC1I5	ADC1I6		A1VSS	A1VSS			VSS	VDD	VDD	VDD	VDD	VSS			E0VSS	E0VSS		P0_8	P0_7	P
R	ADC1I7	ADC1I8		A1VSS	A0VSS											VSS	E0VSS		P0_6	P0_5	R
T	ADC1I9	ADC1I10		A1VSS	A0VSS	A0VSS	A0VSS	A0VSS	A0VSS	E0VCC	E0VSS	E0VSS	E0VSS	P6_11	VSS	VSS	E0VSS		P0_4	P0_3	T
U	A1VCC	ADC1I11		A0VSS	A0VSS	A0VSS	A0VSS	A0VSS	A0VSS	P6_4	P6_5	P6_6	E0VSS	P6_10	P6_12	P6_13	VSS		E0VSS	P0_2	U
V	A1VREFH	A1VSS																	E0VSS	P3_11	V
W	A1VSS	A1VSS	A0VSS	ADC0I11	ADC0I9	ADC0I7	ADC0I5	ADC0I3	ADC0I1	P6_2	P5_0	P5_4	P5_6	P5_8	P5_10	P5_12	P5_14	P0_0	P0_1	VSS	W
Y	A1VSS	A0VSS	A0VREFH	A0VCC	ADC0I10	ADC0I8	ADC0I6	ADC0I4	ADC0I2	ADC0I0	P6_3	P5_1	P5_5	P5_7	P5_9	P5_11	P5_13	P5_15	VSS	VSS	Y

Figure 1.2 Pin Connection Diagram of P1M-C (BGA-292)

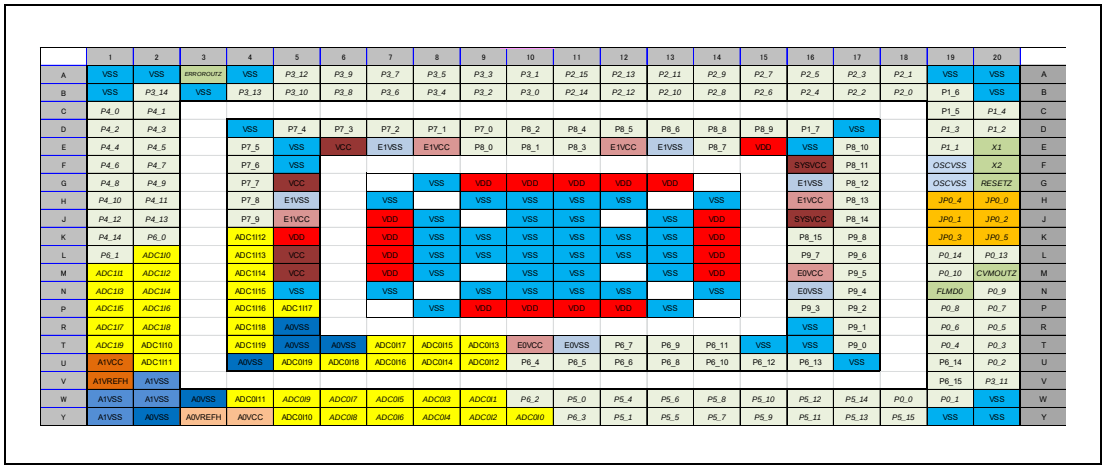
1.3.3 P1H-C (4MB) (BGA-292) (TOP View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	ERROROUTZ	VSS	P3_12	P3_9	P3_7	P3_5	P3_3	P3_1	P2_15	P2_13	P2_11	P2_9	P2_7	P2_5	P2_3	P2_1	VSS	VSS	A
B	VSS	P3_14	VSS	P3_13	P3_10	P3_8	P3_6	P3_4	P3_2	P3_0	P2_14	P2_12	P2_10	P2_8	P2_6	P2_4	P2_2	P2_0	P1_6	VSS	B
C	P4_0	P4_1																	P1_5	P1_4	C
D	P4_2	P4_3		VSS	P7_4	P7_3	P7_2	P7_1	P7_0	P8_2	P8_4	P8_5	P8_6	P8_8	P8_9	P1_7	VSS		P1_3	P1_2	D
E	P4_4	P4_5		P7_5	VSS	VCC	E1VSS	E1VCC	P8_0	P8_1	P8_3	E1VCC	E1VSS	P8_7	VDD	VSS	P8_10		P1_1	X1	E
F	P4_6	P4_7		P7_6	VSS											SYSVCC	P8_11		OSCVSS	X2	F
G	P4_8	P4_9		P7_7	VCC			VSS	VDD	VDD	VDD	VDD	VDD			E1VSS	P8_12		OSCVSS	RESETZ	G
H	P4_10	P4_11		P7_8	E1VSS		VSS		VSS	VSS	VSS	VSS		VSS		E1VCC	P8_13		JP0_4	JP0_0	H
J	P4_12	P4_13		P7_9	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		SYSVCC	P8_14		JP0_1	JP0_2	J
K	P4_14	P6_0		ADC1I12	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P8_15	P9_8		JP0_3	JP0_5	K
L	P6_1	ADC1I0		ADC1I13	VCC		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P9_7	P9_6		P0_14	P0_13	L
M	ADC1I1	ADC1I2		ADC1I14	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P9_5		P0_10	CVMOUTZ	M
N	ADC1I3	ADC1I4		ADC1I15	VSS		VSS		VSS	VSS	VSS	VSS		VSS		E0VSS	P9_4		FLMD0	P0_9	N
P	ADC1I5	ADC1I6		A1VSS	A1VSS			VSS	VDD	VDD	VDD	VDD	VSS			P9_3	P9_2		P0_8	P0_7	P
R	ADC1I7	ADC1I8		A1VSS	A0VSS											VSS	P9_1		P0_6	P0_5	R
T	ADC1I9	ADC1I10		A1VSS	A0VSS	A0VSS	A0VSS	ADC0I15	ADC0I13	E0VCC	E0VSS	P6_7	P6_9	P6_11	VSS	VSS	P9_0		P0_4	P0_3	T
U	A1VCC	ADC1I11		A0VSS	A0VSS	A0VSS	A0VSS	ADC0I14	ADC0I12	P6_4	P6_5	P6_6	P6_8	P6_10	P6_12	P6_13	VSS		P6_14	P0_2	U
V	A1VREFH	A1VSS																	P6_15	P3_11	V
W	A1VSS	A1VSS	A0VSS	ADC0I11	ADC0I9	ADC0I7	ADC0I5	ADC0I3	ADC0I1	P6_2	P5_0	P5_4	P5_6	P5_8	P5_10	P5_12	P5_14	P0_0	P0_1	VSS	W
Y	A1VSS	A0VSS	A0VREFH	A0VCC	ADC0I10	ADC0I8	ADC0I6	ADC0I4	ADC0I2	ADC0I0	P6_3	P5_1	P5_5	P5_7	P5_9	P5_11	P5_13	P5_15	VSS	VSS	Y

Figure 1.3 Pin Connection Diagram of P1H-C (4MB) (BGA-292)

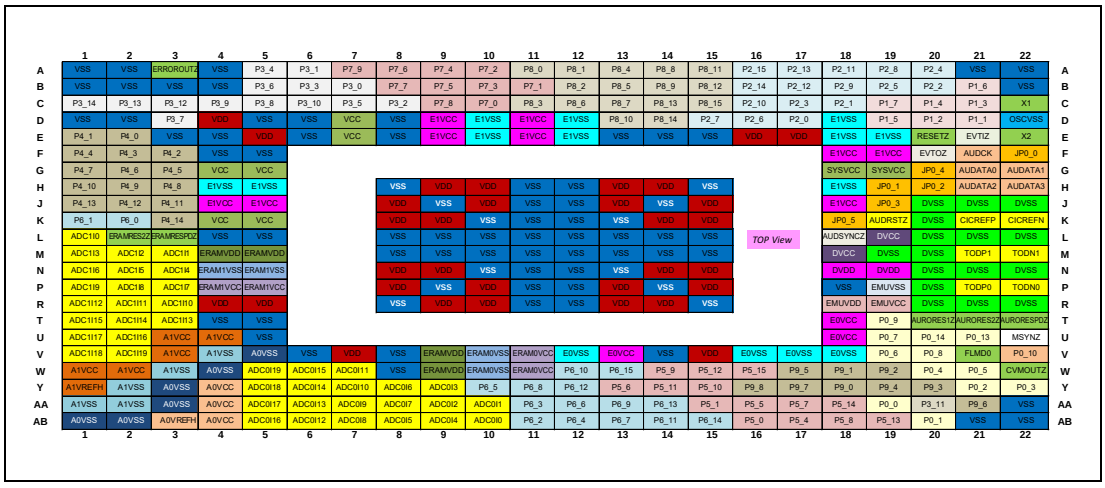
1.3.4 P1H-C (8MB) (BGA-292) (TOP View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	ERROROUTZ	VSS	P3_12	P3_9	P3_7	P3_5	P3_3	P3_1	P2_15	P2_13	P2_11	P2_9	P2_7	P2_5	P2_3	P2_1	VSS	VSS	A
B	VSS	P3_14	VSS	P3_13	P3_10	P3_8	P3_6	P3_4	P3_2	P3_0	P2_14	P2_12	P2_10	P2_8	P2_6	P2_4	P2_2	P2_0	P1_6	VSS	B
C	P4_0	P4_1																	P1_5	P1_4	C
D	P4_2	P4_3		VSS	P7_4	P7_3	P7_2	P7_1	P7_0	P8_2	P8_4	P8_5	P8_6	P8_8	P8_9	P1_7	VSS		P1_3	P1_2	D
E	P4_4	P4_5		P7_5	VSS	VCC	E1VSS	E1VCC	P8_0	P8_1	P8_3	E1VCC	E1VSS	P8_7	VDD	VSS	P8_10		P1_1	X1	E
F	P4_6	P4_7		P7_6	VSS											SYSVCC	P8_11		OSCVSS	X2	F
G	P4_8	P4_9		P7_7	VCC			VSS	VDD	VDD	VDD	VDD	VDD			E1VSS	P8_12		OSCVSS	RESETZ	G
H	P4_10	P4_11		P7_8	E1VSS		VSS		VSS	VSS	VSS	VSS		VSS		E1VCC	P8_13		JP0_4	JP0_0	H
J	P4_12	P4_13		P7_9	E1VCC		VDD	VSS		VSS	VSS		VSS	VDD		SYSVCC	P8_14		JP0_1	JP0_2	J
K	P4_14	P6_0		ADC1I12	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P8_15	P9_8		JP0_3	JP0_5	K
L	P6_1	ADC1I0		ADC1I13	VCC		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		P9_7	P9_6		P0_14	P0_13	L
M	ADC1I1	ADC1I2		ADC1I14	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P9_5		P0_10	CVMOUTZ	M
N	ADC1I3	ADC1I4		ADC1I15	VSS		VSS		VSS	VSS	VSS	VSS		VSS		E0VSS	P9_4		FLMD0	P0_9	N
P	ADC1I5	ADC1I6		ADC1I16	ADC1I17			VSS	VDD	VDD	VDD	VDD	VSS			P9_3	P9_2		P0_8	P0_7	P
R	ADC1I7	ADC1I8		ADC1I18	A0VSS											VSS	P9_1		P0_6	P0_5	R
T	ADC1I9	ADC1I10		ADC1I19	A0VSS	A0VSS	ADC0I17	ADC0I15	ADC0I13	E0VCC	E0VSS	P6_7	P6_9	P6_11	VSS	VSS	P9_0		P0_4	P0_3	T
U	A1VCC	ADC1I11		A0VSS	ADC0I19	ADC0I18	ADC0I16	ADC0I14	ADC0I12	P6_4	P6_5	P6_6	P6_8	P6_10	P6_12	P6_13	VSS		P6_14	P0_2	U
V	A1VREFH	A1VSS																	P6_15	P3_11	V
W	A1VSS	A1VSS	A0VSS	ADC0I11	ADC0I9	ADC0I7	ADC0I5	ADC0I3	ADC0I1	P6_2	P5_0	P5_4	P5_6	P5_8	P5_10	P5_12	P5_14	P0_0	P0_1	VSS	W
Y	A1VSS	A0VSS	A0VREFH	A0VCC	ADC0I10	ADC0I8	ADC0I6	ADC0I4	ADC0I2	ADC0I0	P6_3	P5_1	P5_5	P5_7	P5_9	P5_11	P5_13	P5_15	VSS	VSS	Y

Figure 1.4 Pin Connection Diagram of P1H-C (8MB) (BGA-292)

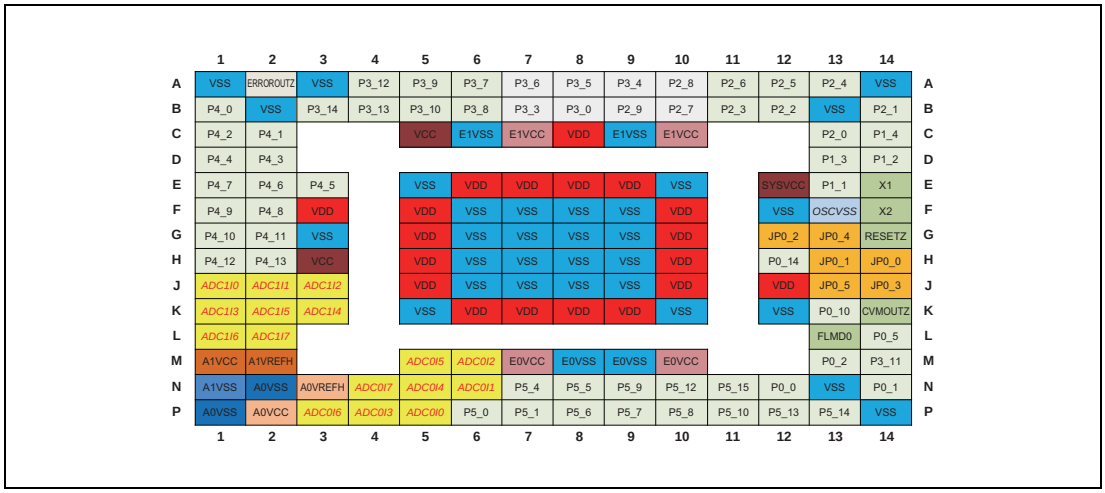
1.3.5 P1H-CE (BGA-404) (TOP View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VSS	ERROROUTZ	VSS	P3_4	P3_1	P7_9	P7_6	P7_4	P7_2	P8_0	P8_1	P8_4	P8_8	P8_11	P2_15	P2_13	P2_11	P2_8	P2_4	VSS	VSS	A
B	VSS	VSS	VSS	VSS	P3_6	P3_3	P3_0	P7_7	P7_5	P7_3	P7_1	P8_2	P8_5	P8_9	P8_12	P2_14	P2_12	P2_9	P2_5	P2_2	P1_6	VSS	B
C	P3_14	P3_13	P3_12	P3_9	P3_8	P3_10	P3_5	P3_2	P7_8	P7_0	P8_3	P8_6	P8_7	P8_13	P8_15	P2_10	P2_3	P2_1	P1_7	P1_4	P1_3	X1	C
D	VSS	VSS	P3_7	VDD	VSS	VSS	VCC	VSS	E1VCC	E1VSS	E1VCC	E1VSS	P8_10	P8_14	P2_7	P2_8	P2_0	E1VSS	P1_5	P1_2	P1_1	OSCVSS	D
E	P4_1	P4_0	VSS	VSS	VDD	VSS	VCC	VSS	E1VCC	E1VSS	E1VCC	E1VSS	VSS	VSS	VSS	VDD	VDD	E1VSS	E1VSS	RESETZ	EVTIZ	X2	E
F	P4_4	P4_3	P4_2	VSS	VSS													E1VCC	E1VCC	EVTOZ	AUDCK	JP0_0	F
G	P4_7	P4_6	P4_5	VCC	VCC													SYSVCC	SYSVCC	JP0_4	AUDATA0	AUDATA1	G
H	P4_10	P4_9	P4_8	E1VSS	E1VSS			VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS			E1VSS	JP0_1	JP0_2	AUDATA2	AUDATA3	H
J	P4_13	P4_12	P4_11	E1VCC	E1VCC			VDD	VSS	VDD	VSS	VSS	VDD	VSS	VDD			E1VCC	JP0_3	DVSS	DVSS	DVSS	J
K	P6_1	P6_0	P4_14	VCC	VCC			VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD			JP0_5	AUDRSTZ	DVSS	CICREFP	CICREFN	K
L	ADC1I0	ERAMRESZ	ERAMRESPDZ	VSS	VSS			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TOP View		AUDSYNC2	DVCC	DVSS	DVSS	DVSS	L
M	ADC1I3	ADC1I2	ADC1I1	ERAMVDD	ERAMVDD			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS			DVCC	DVSS	DVSS	TODP1	TODN1	M
N	ADC1I6	ADC1I5	ADC1I4	ERAM1VSS	ERAM1VSS			VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD			DVDD	DVDD	DVSS	DVSS	DVSS	N
P	ADC1I9	ADC1I8	ADC1I7	ERAM1VCC	ERAM1VCC			VDD	VSS	VDD	VSS	VSS	VDD	VSS	VDD			VSS	EMUVSS	DVSS	TODP0	TODN0	P
R	ADC1I12	ADC1I11	ADC1I10	VDD	VDD			VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS			EMUVDD	EMUVCC	DVSS	DVSS	DVSS	R
T	ADC1I15	ADC1I14	ADC1I13	VSS	VSS													E0VCC	P0_9	AURORES1Z	AURORES2Z	AURORESPD2	T
U	ADC1I17	ADC1I16	A1VCC	A1VCC	VSS													E0VCC	P0_7	P0_14	P0_13	MSYNZ	U
V	ADC1I18	ADC1I19	A1VCC	A1VSS	A0VSS	VSS	VDD	VSS	ERAMVDD	ERAM0VSS	ERAM0VCC	E0VSS	E0VCC	VSS	VDD	E0VSS	E0VSS	E0VSS	P0_6	P0_8	FLMD0	P0_10	V
W	A1VCC	A1VCC	A1VSS	A0VSS	ADC0I19	ADC0I15	ADC0I11	VSS	ERAMVDD	ERAM0VSS	ERAM0VCC	P6_10	P6_15	P5_9	P5_12	P5_15	P9_5	P9_1	P9_2	P0_4	P0_5	CVMOUTZ	W
Y	A1VREFH	A1VSS	A0VSS	A0VCC	ADC0I18	ADC0I14	ADC0I10	ADC0I6	ADC0I3	P6_5	P6_8	P6_12	P5_6	P5_11	P5_10	P9_8	P9_7	P9_0	P9_4	P9_3	P0_2	P0_3	Y
AA	A1VSS	A1VSS	A0VSS	A0VCC	ADC0I17	ADC0I13	ADC0I9	ADC0I7	ADC0I2	ADC0I1	P6_3	P6_6	P6_9	P6_13	P5_1	P5_5	P5_7	P5_14	P0_0	P3_11	P9_6	VSS	AA
AB	A0VSS	A0VSS	A0VREFH	A0VCC	ADC0I16	ADC0I12	ADC0I8	ADC0I5	ADC0I4	ADC0I0	P6_2	P6_4	P6_7	P6_11	P6_14	P5_0	P5_4	P5_8	P5_13	P0_1	VSS	VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 1.5 Pin Connection Diagram of P1H-CE (BGA-404)

1.3.6 P1M-C/P1H-C (BGA-156) (TOP View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	ERROROUTZ	VSS	P3_12	P3_9	P3_7	P3_6	P3_5	P3_4	P2_8	P2_6	P2_5	P2_4	VSS	A
B	P4_0	VSS	P3_14	P3_13	P3_10	P3_8	P3_3	P3_0	P2_9	P2_7	P2_3	P2_2	VSS	P2_1	B
C	P4_2	P4_1			VCC	E1VSS	E1VCC	VDD	E1VSS	E1VCC			P2_0	P1_4	C
D	P4_4	P4_3											P1_3	P1_2	D
E	P4_7	P4_6	P4_5		VSS	VDD	VDD	VDD	VDD	VSS		SYSVCC	P1_1	X1	E
F	P4_9	P4_8	VDD		VDD	VSS	VSS	VSS	VSS	VDD		VSS	OSCVSS	X2	F
G	P4_10	P4_11	VSS		VDD	VSS	VSS	VSS	VSS	VDD		JP0_2	JP0_4	RESETZ	G
H	P4_12	P4_13	VCC		VDD	VSS	VSS	VSS	VSS	VDD		P0_14	JP0_1	JP0_0	H
J	ADC1I0	ADC1I1	ADC1I2		VDD	VSS	VSS	VSS	VSS	VDD		VDD	JP0_5	JP0_3	J
K	ADC1I3	ADC1I5	ADC1I4		VSS	VDD	VDD	VDD	VDD	VSS		VSS	P0_10	CVMOUTZ	K
L	ADC1I6	ADC1I7											FLMD0	P0_5	L
M	A1VCC	A1VREFH			ADC0I5	ADC0I2	E0VCC	E0VSS	E0VSS	E0VCC			P0_2	P3_11	M
N	A1VSS	A0VSS	A0VREFH	ADC0I7	ADC0I4	ADC0I1	P5_4	P5_5	P5_9	P5_12	P5_15	P0_0	VSS	P0_1	N
P	A0VSS	A0VCC	ADC0I6	ADC0I3	ADC0I0	P5_0	P5_1	P5_6	P5_7	P5_8	P5_10	P5_13	P5_14	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 1.6 Pin Connection Diagram of P1M-C/P1H-C (BGA-156)

1.4 Block Diagram

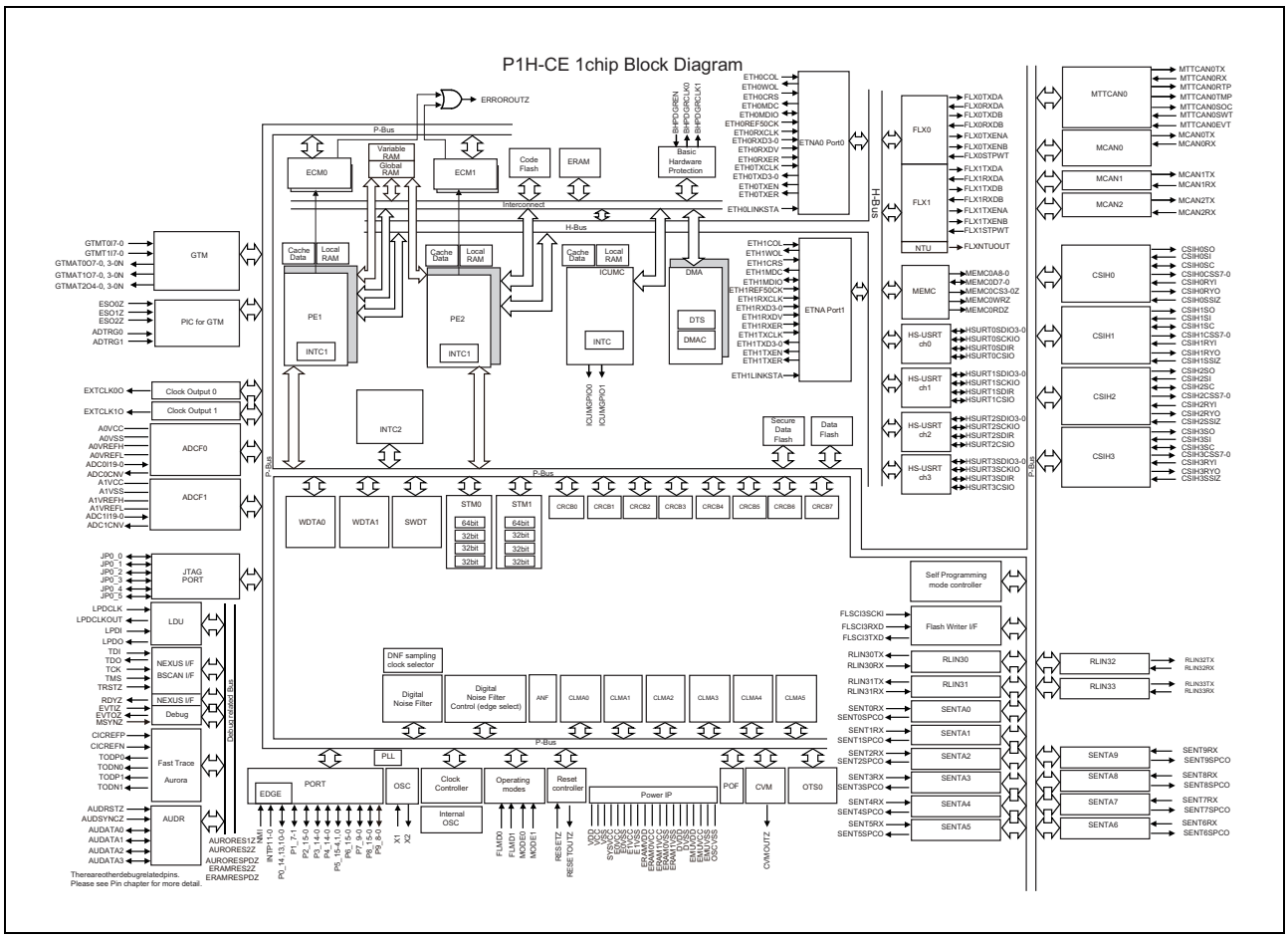


Figure 1.7 RH850/P1x-C chip block diagram (P1H-CE)

Section 2 Pin Functions

This section describes the pin and port functions.

Section 2.1 describes the pin connection and respective pins.

2.1 Pin List

2.1.1 Term Definition

The following terms are used in this section:

Pin

Denotes the physical pin. Every pin is denoted by a unique pin number.
A pin can be used in several modes. Each pin is assigned a name that reflects its function, which is determined by the selected mode.

Port group

Denotes a group of pins. All the pins of a specific port group are controlled by the same port control register.
The RH850/P1x-C provides the following port groups, indicated by the numbers in the table below.

	P1M-C/P1H-C (156)	P1M-C (144)	P1M-C (292)	P1H-C (4MB) (292)	P1H-C (8MB) (292)	P1H-C (8MB) ED (404)
Number of Group	7	8	10	11	11	11
Name of Group	P0 to P5, JP0	P0 to P6, JP0	P0 to P7, P9, JP0	P0 to P9, JP0	P0 to P9, JP0	P0 to P9, JP0

Port group index n

Each port group is identified by its own index “n” throughout this section; e.g.
PMCn for the port mode control register of the Pn port.

Port mode and ports

A pin in port mode works as a general purpose input/output pin. It is then called “port”.
The corresponding name is Pn_m. For example, P0_7 denotes port 7 of port group 0. It is referenced as “port P0_7”.

Alternative mode

In alternative mode, a pin can be used for various non-general-purpose input/output functions. It is such as CSI and INTP.

SHMT1/SHMT2/SHMT4

Denotes input buffer types. Each types have a different DC characteristics.
For detail, refer to the **Section 3, Electrical Specifications**.

GPIO/HSIO.

GPIO indicates General purpose I/O and HSIO indicates High speed I/O.
For detail, refer to the **Section 3, Electrical Specifications**.

2.1.2 Pin List and Function assignment

CAUTION

To prevent malfunction, secure reset value to registers that are not available for the individual product. For port availability of each product see Table 2.1.

Table 2.1 Pin List (1/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
															CMOS	SHMT1	SHMT4	SHMT2	
1													1						
2	1	P3_14	B3	P3_14	B2	P3_14	B2	P3_14	B2	P3_14	C1	P3_14	2	P3_14		SHMT1	SHMT4		HSIO
3	2	P4_0	B1	P4_0	C1	P4_0	C1	P4_0	C1	P4_0	E2	P4_0	3	P4_0		SHMT1	SHMT4		GPIO
4	3	P4_1	C2	P4_1	C2	P4_1	C2	P4_1	C2	P4_1	E1	P4_1	4	P4_1		SHMT1	SHMT4		GPIO
5	4	P4_2	C1	P4_2	D1	P4_2	D1	P4_2	D1	P4_2	F3	P4_2	5	P4_2		SHMT1	SHMT4		GPIO
6			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	6	VDD					
7	5	P4_3	D2	P4_3	D2	P4_3	D2	P4_3	D2	P4_3	F2	P4_3	7	P4_3		SHMT1	SHMT4		GPIO
8	6	P4_4	D1	P4_4	E1	P4_4	E1	P4_4	E1	P4_4	F1	P4_4	8	P4_4		SHMT1	SHMT4		GPIO
9	7	P4_5	E3	P4_5	E2	P4_5	E2	P4_5	E2	P4_5	G3	P4_5	9	P4_5		SHMT1	SHMT4		GPIO
10	8	P4_6	E2	P4_6	F1	P4_6	F1	P4_6	F1	P4_6	G2	P4_6	10	P4_6		SHMT1	SHMT4		GPIO
11	9	P4_7	E1	P4_7	F2	P4_7	F2	P4_7	F2	P4_7	G1	P4_7	11	P4_7		SHMT1	SHMT4		GPIO
12	10	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	12	E1VSS					
13	11	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	13	E1VCC					
14	12	P4_8	F2	P4_8	G1	P4_8	G1	P4_8	G1	P4_8	H3	P4_8	14	P4_8		SHMT1	SHMT4		GPIO
15	13	P4_9	F1	P4_9	G2	P4_9	G2	P4_9	G2	P4_9	H2	P4_9	15	P4_9		SHMT1	SHMT4		GPIO
16	14	P4_10	G1	P4_10	H1	P4_10	H1	P4_10	H1	P4_10	H1	P4_10	16	P4_10		SHMT1	SHMT4		GPIO
17	15	P4_11	G2	P4_11	H2	P4_11	H2	P4_11	H2	P4_11	J3	P4_11	17	P4_11		SHMT1	SHMT4		GPIO
18	16	P4_12	H1	P4_12	J1	P4_12	J1	P4_12	J1	P4_12	J2	P4_12	18	P4_12		SHMT1	SHMT4		GPIO
19	17	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	19	VDD					
20	18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	20	VSS					
21	19	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	21	VCC					
22	20	P4_13	H2	P4_13	J2	P4_13	J2	P4_13	J2	P4_13	J1	P4_13	22	P4_13		SHMT1	SHMT4		GPIO
23	21	P4_14			K1	P4_14	K1	P4_14	K1	P4_14	K3	P4_14	23	P4_14		SHMT1	SHMT4		GPIO
24	22	P6_0			K2	P6_0	K2	P6_0	K2	P6_0	K2	P6_0	24	P6_0		SHMT1	SHMT4		GPIO
25	23	P6_1			L1	P6_1	L1	P6_1	L1	P6_1	K1	P6_1	25	P6_1		SHMT1	SHMT4		GPIO
26											L3	ERAM RESPDZ	26	ERAM RESPDZ				SHMT2	
27											L2	ERAM RES2Z	27	ERAM RES2Z				SHMT2	
28	24	ADC1I0	J1	ADC1I0	L2	ADC1I0	L2	ADC1I0	L2	ADC1I0	L1	ADC1I0	28	ADC1I0					
29	25	ADC1I1	J2	ADC1I1	M1	ADC1I1	M1	ADC1I1	M1	ADC1I1	M3	ADC1I1	29	ADC1I1					
30	26	ADC1I2	J3	ADC1I2	M2	ADC1I2	M2	ADC1I2	M2	ADC1I2	M2	ADC1I2	30	ADC1I2					
31	27	ADC1I3	K1	ADC1I3	N1	ADC1I3	N1	ADC1I3	N1	ADC1I3	M1	ADC1I3	31	ADC1I3					
32	28	ADC1I4	K3	ADC1I4	N2	ADC1I4	N2	ADC1I4	N2	ADC1I4	N3	ADC1I4	32	ADC1I4					
33	29	ADC1I5	K2	ADC1I5	P1	ADC1I5	P1	ADC1I5	P1	ADC1I5	N2	ADC1I5	33	ADC1I5					
34	30	ADC1I6	L1	ADC1I6	P2	ADC1I6	P2	ADC1I6	P2	ADC1I6	N1	ADC1I6	34	ADC1I6					
35	31	ADC1I7	L2	ADC1I7	R1	ADC1I7	R1	ADC1I7	R1	ADC1I7	P3	ADC1I7	35	ADC1I7					
36	32	ADC1I8			R2	ADC1I8	R2	ADC1I8	R2	ADC1I8	P2	ADC1I8	36	ADC1I8					
37	33	ADC1I9			T1	ADC1I9	T1	ADC1I9	T1	ADC1I9	P1	ADC1I9	37	ADC1I9					
38					T2	ADC1I10	T2	ADC1I10	T2	ADC1I10	R3	ADC1I10	38	ADC1I10					
39					U2	ADC1I11	U2	ADC1I11	U2	ADC1I11	R2	ADC1I11	39	ADC1I11					
40					K4	A1VSS	K4	ADC1I12	K4	ADC1I12	R1	ADC1I12	40	ADC1I12					
41					L4	A1VSS	L4	ADC1I13	L4	ADC1I13	T3	ADC1I13	41	ADC1I13					
42					M4	A1VSS	M4	ADC1I14	M4	ADC1I14	T2	ADC1I14	42	ADC1I14					
43					N4	A1VSS	N4	ADC1I15	N4	ADC1I15	T1	ADC1I15	43	ADC1I15					
44					P4	A1VSS	P4	A1VSS	P4	ADC1I16	U2	ADC1I16	44	ADC1I16					
45					P5	A1VSS	P5	A1VSS	P5	ADC1I17	U1	ADC1I17	45	ADC1I17					

Table 2.1 Pin List (2/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
46					R4	A1VSS	R4	A1VSS	R4	ADC1I18	V1	ADC1I18	46	ADC1I18					
47					T4	A1VSS	T4	A1VSS	T4	ADC1I19	V2	ADC1I19	47	ADC1I19					
48	34	A1VCC	M1	A1VCC	U1	A1VCC	U1	A1VCC	U1	A1VCC	A1 VCC	A1VCC	48	A1VCC					
49	35	A1VREFH	M2	A1VREFH	V1	A1VREFH	V1	A1VREFH	V1	A1VREFH	Y1	A1VREFH	49	A1VREFH					
50	36	A1VSS	N1	A1VSS	V2	A1VSS	V2	A1VSS	V2	A1VSS	Y2	A1VSS	50	A1VSS					
51	36	A1VSS	A1 VSS	A1VSS	A1 VSS	A1VSS	A1 VSS	A1VSS	A1 VSS	A1VSS	A1 VSS	A1VSS	51	A1VSS					
52	48												52						
53	37	A0VREFH	N3	A0VREFH	Y3	A0VREFH	Y3	A0VREFH	Y3	A0VREFH	AB3	A0VREFH	53	A0VREFH					
54	38	A0VSS	N2	A0VSS	W3	A0VSS	W3	A0VSS	W3	A0VSS	AA3	A0VSS	54	A0VSS					
55	38	A0VSS	A0 VSS	A0VSS	A0 VSS	A0VSS	A0 VSS	A0VSS	A0 VSS	A0VSS	A0 VSS	A0VSS	55	A0VSS					
56	39	A0VCC	P2	A0VCC	Y4	A0VCC	Y4	A0VCC	Y4	A0VCC	A0 VCC	A0VCC	56	A0VCC					
57					U5	A0VSS	U5	A0VSS	U5	ADC0I19	W5	ADC0I19	57	ADC0I19					
58					U6	A0VSS	U6	A0VSS	U6	ADC0I18	Y5	ADC0I18	58	ADC0I18					
59					T7	A0VSS	T7	A0VSS	T7	ADC0I17	AA5	ADC0I17	59	ADC0I17					
60					U7	A0VSS	U7	A0VSS	U7	ADC0I16	AB5	ADC0I16	60	ADC0I16					
61					T8	A0VSS	T8	ADC0I15	T8	ADC0I15	W6	ADC0I15	61	ADC0I15					
62					U8	A0VSS	U8	ADC0I14	U8	ADC0I14	Y6	ADC0I14	62	ADC0I14					
63					T9	A0VSS	T9	ADC0I13	T9	ADC0I13	AA6	ADC0I13	63	ADC0I13					
64					U9	A0VSS	U9	ADC0I12	U9	ADC0I12	AB6	ADC0I12	64	ADC0I12					
65					W4	ADC0I11	W4	ADC0I11	W4	ADC0I11	W7	ADC0I11	65	ADC0I11					
66					Y5	ADC0I10	Y5	ADC0I10	Y5	ADC0I10	Y7	ADC0I10	66	ADC0I10					
67	40	ADC0I9			W5	ADC0I9	W5	ADC0I9	W5	ADC0I9	AA7	ADC0I9	67	ADC0I9					
68	41	ADC0I8			Y6	ADC0I8	Y6	ADC0I8	Y6	ADC0I8	AB7	ADC0I8	68	ADC0I8					
69	42	ADC0I7	N4	ADC0I7	W6	ADC0I7	W6	ADC0I7	W6	ADC0I7	AA8	ADC0I7	69	ADC0I7					
70	43	ADC0I6	P3	ADC0I6	Y7	ADC0I6	Y7	ADC0I6	Y7	ADC0I6	Y8	ADC0I6	70	ADC0I6					
71	44	ADC0I5	M5	ADC0I5	W7	ADC0I5	W7	ADC0I5	W7	ADC0I5	AB8	ADC0I5	71	ADC0I5					
72	45	ADC0I4	N5	ADC0I4	Y8	ADC0I4	Y8	ADC0I4	Y8	ADC0I4	AB9	ADC0I4	72	ADC0I4					
73	46	ADC0I3	P4	ADC0I3	W8	ADC0I3	W8	ADC0I3	W8	ADC0I3	Y9	ADC0I3	73	ADC0I3					
74	47	ADC0I2	M6	ADC0I2	Y9	ADC0I2	Y9	ADC0I2	Y9	ADC0I2	AA9	ADC0I2	74	ADC0I2					
75	48	ADC0I1	N6	ADC0I1	W9	ADC0I1	W9	ADC0I1	W9	ADC0I1	AA10	ADC0I1	75	ADC0I1					
76	49	ADC0I0	P5	ADC0I0	Y10	ADC0I0	Y10	ADC0I0	Y10	ADC0I0	AB10	ADC0I0	76	ADC0I0					
77			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	77	VDD					
78	50	P6_2			W10	P6_2	W10	P6_2	W10	P6_2	AB11	P6_2	78	P6_2		SHMT1	SHMT4		GPIO
79	51	P6_3			Y11	P6_3	Y11	P6_3	Y11	P6_3	AA11	P6_3	79	P6_3		SHMT1	SHMT4		GPIO
80					U10	P6_4	U10	P6_4	U10	P6_4	AB12	P6_4	80	P6_4		SHMT1	SHMT4		GPIO
81					U11	P6_5	U11	P6_5	U11	P6_5	Y10	P6_5	81	P6_5		SHMT1	SHMT4		GPIO
82					U12	P6_6	U12	P6_6	U12	P6_6	AA12	P6_6	82	P6_6		SHMT1	SHMT4		GPIO
83					E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	83	E0VCC					
84					E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	84	E0VSS					
85					T12	E0VSS	T12	P6_7	T12	P6_7	AB13	P6_7	85	P6_7		SHMT1	SHMT4		GPIO
86					U13	E0VSS	U13	P6_8	U13	P6_8	Y11	P6_8	86	P6_8		SHMT1	SHMT4		GPIO
87					T13	E0VSS	T13	P6_9	T13	P6_9	AA13	P6_9	87	P6_9		SHMT1	SHMT4		GPIO
88					U14	P6_10	U14	P6_10	U14	P6_10	W12	P6_10	88	P6_10		SHMT1	SHMT4		GPIO
89					T14	P6_11	T14	P6_11	T14	P6_11	AB14	P6_11	89	P6_11		SHMT1	SHMT4		GPIO
90					U15	P6_12	U15	P6_12	U15	P6_12	Y12	P6_12	90	P6_12		SHMT1	SHMT4		GPIO
91					U16	P6_13	U16	P6_13	U16	P6_13	AA14	P6_13	91	P6_13		SHMT1	SHMT4		GPIO
92					U19	E0VSS	U19	P6_14	U19	P6_14	AB15	P6_14	92	P6_14		SHMT1	SHMT4		GPIO
93					V19	E0VSS	V19	P6_15	V19	P6_15	W13	P6_15	93	P6_15		SHMT1	SHMT4		GPIO
94	52	P5_0	P6	P5_0	W11	P5_0	W11	P5_0	W11	P5_0	AB16	P5_0	94	P5_0		SHMT1	SHMT4		GPIO
95	53	P5_1	P7	P5_1	Y12	P5_1	Y12	P5_1	Y12	P5_1	AA15	P5_1	95	P5_1		SHMT1	SHMT4		GPIO
96	54	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	96	VSS					
97	55	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	97	VDD					
98	56	P5_4	N7	P5_4	W12	P5_4	W12	P5_4	W12	P5_4	AB17	P5_4	98	P5_4		SHMT1	SHMT4		GPIO
99	57	P5_5	N8	P5_5	Y13	P5_5	Y13	P5_5	Y13	P5_5	AA16	P5_5	99	P5_5		SHMT1	SHMT4		GPIO
100	58	P5_6	P8	P5_6	W13	P5_6	W13	P5_6	W13	P5_6	Y13	P5_6	100	P5_6		SHMT1	SHMT4		GPIO
101	59	P5_7	P9	P5_7	Y14	P5_7	Y14	P5_7	Y14	P5_7	AA17	P5_7	101	P5_7		SHMT1	SHMT4		GPIO

Table 2.1 Pin List (3/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings: Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
102	60	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	102	E0VCC					
103	61	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	103	E0VSS					
104	62	P5_8	P10	P5_8	W14	P5_8	W14	P5_8	W14	P5_8	AB18	P5_8	104	P5_8		SHMT1	SHMT4		GPIO
105	63	P5_9	N9	P5_9	Y15	P5_9	Y15	P5_9	Y15	P5_9	W14	P5_9	105	P5_9		SHMT1	SHMT4		GPIO
106	64	P5_10	P11	P5_10	W15	P5_10	W15	P5_10	W15	P5_10	Y15	P5_10	106	P5_10		SHMT1	SHMT4		GPIO
107	65	P5_11			Y16	P5_11	Y16	P5_11	Y16	P5_11	Y14	P5_11	107	P5_11		SHMT1	SHMT4		GPIO
108	66	P5_12	N10	P5_12	W16	P5_12	W16	P5_12	W16	P5_12	W15	P5_12	108	P5_12		SHMT1	SHMT4		GPIO
109	67	P5_13	P12	P5_13	Y17	P5_13	Y17	P5_13	Y17	P5_13	AB19	P5_13	109	P5_13		SHMT1	SHMT4		GPIO
110	68	P5_14	P13	P5_14	W17	P5_14	W17	P5_14	W17	P5_14	AA18	P5_14	110	P5_14		SHMT1	SHMT4		GPIO
111	69	P5_15	N11	P5_15	Y18	P5_15	Y18	P5_15	Y18	P5_15	W16	P5_15	111	P5_15		SHMT1	SHMT4		GPIO
112	70	P0_0	N12	P0_0	W18	P0_0	W18	P0_0	W18	P0_0	AA19	P0_0	112	P0_0		SHMT1	SHMT4		GPIO
113	71	P0_1	N14	P0_1	W19	P0_1	W19	P0_1	W19	P0_1	AB20	P0_1	113	P0_1		SHMT1	SHMT4		GPIO
114	72	P3_11	M14	P3_11	V20	P3_11	V20	P3_11	V20	P3_11	AA20	P3_11	114	P3_11		SHMT1	SHMT4		GPIO
115					T17	E0VSS	T17	P9_0	T17	P9_0	Y18	P9_0	115	P9_0		SHMT1	SHMT4		GPIO
116					R17	E0VSS	R17	P9_1	R17	P9_1	W18	P9_1	116	P9_1		SHMT1	SHMT4		GPIO
117					P17	E0VSS	P17	P9_2	P17	P9_2	W19	P9_2	117	P9_2		SHMT1	SHMT4		GPIO
118					P16	E0VSS	P16	P9_3	P16	P9_3	Y20	P9_3	118	P9_3		SHMT1	SHMT4		GPIO
119			E0 VCC	E0VCC	E0 VCC	E0VCC (see comment)	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	119	E0VCC					
120			E0 VSS	E0VSS	E0 VSS	E0VSS (see comment)	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	120	E0VSS					
121					N17	E0VSS	N17	P9_4	N17	P9_4	Y19	P9_4	121	P9_4		SHMT1	SHMT4		GPIO
122					M17	E0VSS	M17	P9_5	M17	P9_5	W17	P9_5	122	P9_5		SHMT1	SHMT4		GPIO
123					L17	E0VSS	L17	P9_6	L17	P9_6	AA21	P9_6	123	P9_6		SHMT1	SHMT4		GPIO
124					L16	P9_7 (see comment)	L16	P9_7	L16	P9_7	Y17	P9_7	124	P9_7		SHMT1	SHMT4		GPIO
125					K17	P9_8 (see comment)	K17	P9_8	K17	P9_8	Y16	P9_8	125	P9_8		SHMT1	SHMT4		GPIO
126						66							126						
127	73	P0_2	M13	P0_2	U20	P0_2	U20	P0_2	U20	P0_2	Y21	P0_2	127	P0_2		SHMT1	SHMT4		GPIO
128	74	P0_3			T20	P0_3	T20	P0_3	T20	P0_3	Y22	P0_3	128	P0_3		SHMT1	SHMT4		GPIO
129	75	P0_4			T19	P0_4	T19	P0_4	T19	P0_4	W20	P0_4	129	P0_4		SHMT1	SHMT4		GPIO
130	76	P0_5	L14	P0_5	R20	P0_5	R20	P0_5	R20	P0_5	W21	P0_5	130	P0_5		SHMT1	SHMT4		GPIO
131	77	P0_6			R19	P0_6	R19	P0_6	R19	P0_6	V19	P0_6	131	P0_6		SHMT1	SHMT4		GPIO
132	78	P0_7			P20	P0_7	P20	P0_7	P20	P0_7	U19	P0_7	132	P0_7		SHMT1	SHMT4		GPIO
133	79	P0_8			P19	P0_8	P19	P0_8	P19	P0_8	V20	P0_8	133	P0_8		SHMT1	SHMT4		GPIO
134	80	P0_9			N20	P0_9	N20	P0_9	N20	P0_9	T19	P0_9	134	P0_9		SHMT1	SHMT4		GPIO
135	81	FLMD0	L13	FLMD0	N19	FLMD0	N19	FLMD0	N19	FLMD0	V21	FLMD0	135	FLMD0				SHMT2	
136	82	CVM OUTZ	K14	CVM OUTZ	M20	CVM OUTZ	M20	CVMOUTZ	M20	CVMOUTZ	W22	CVM OUTZ	136	CVM OUTZ				SHMT2	GPIO50O hm (CVM OUT)
137	83	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	E0 VSS	E0VSS	137	E0VSS					
138	84	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	E0 VCC	E0VCC	138	E0VCC					
139	85	P0_10	K13	P0_10	M19	P0_10	M19	P0_10	M19	P0_10	V22	P0_10	139	P0_10		SHMT1	SHMT4		GPIO (RESETOUT)
140	86	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	140	VDD					
141	87	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	141	VSS					
142	88	P0_13			L20	P0_13	L20	P0_13	L20	P0_13	U21	P0_13	142	P0_13		SHMT1	SHMT4		GPIO
143	89	P0_14	H12	P0_14	L19	P0_14	L19	P0_14	L19	P0_14	U20	P0_14	143	P0_14		SHMT1	SHMT4		GPIO
144											U22	MSYNZ	144	MSYNZ		SHMT1			
145											R19	EMUVCC	145	EMUVCC					
146											P19	EMUVSS	146	EMUVSS					
147											T21	AURO RES2Z	147	AURO RES2Z				SHMT2	
148											T20	AURO RES1Z	148	AURO RES1Z				SHMT2	
149											T22	AURO RESPDZ	149	AURO RESPDZ				SHMT2	
150											R18	EMUVDD	150	EMUVDD					
151												EMUVDD	151	EMUVDD					
152											P18	VSS	152	VSS					
153												VSS	153	VSS					

Table 2.1 Pin List (4/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
154											N18	DVDD	154	DVDD					
155											P21	TODP0	155	TODP0					
156											P22	TODN0	156	TODN0					
157											R20	DVSS	157	DVSS					
158											M21	TODP1	158	TODP1					
159											M22	TODN1	159	TODN1					
160											N19	DVDD	160	DVDD					
161											N20	DVSS	161	DVSS					
162											M19	DVSS	162	DVSS					
164											K21	CICREFP	164	CICREFP					
165											K22	CICREFN	165	CICREFN					
166											L19	DVCC	166	DVCC					
167											M18	DVCC	167	DVCC					
168											M19	DVSS	168	DVSS					
169			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	169	VSS					
170	90	JP0_5	J13	JP0_5	K20	JP0_5	K20	JP0_5	K20	JP0_5	K18	JP0_5	170	JP0_5		SHMT1	SHMT4		GPIO
171	91	JP0_3	J14	JP0_3	K19	JP0_3	K19	JP0_3	K19	JP0_3	J19	JP0_3	171	JP0_3		SHMT1	SHMT4		GPIO
172	92	JP0_2	G12	JP0_2	J20	JP0_2	J20	JP0_2	J20	JP0_2	H20	JP0_2	172	JP0_2		SHMT1	SHMT4		GPIO
175	93	JP0_1	H13	JP0_1	J19	JP0_1	J19	JP0_1	J19	JP0_1	H19	JP0_1	175	JP0_1		SHMT1	SHMT4		GPIO
176	94	JP0_0	H14	JP0_0	H20	JP0_0	H20	JP0_0	H20	JP0_0	F22	JP0_0	176	JP0_0		SHMT1	SHMT4		GPIO
177	95	JP0_4	G13	JP0_4	H19	JP0_4	H19	JP0_4	H19	JP0_4	G20	JP0_4	177	JP0_4				SHMT2	
178											F20	EVTOZ	178	EVTOZ					GPIO50 Ohm
179											E21	EVTIZ	179	EVTIZ		SHMT1			
182											H22	AUDATA3	182	AUDATA3	CMOS				
183											H21	AUDATA2	183	AUDATA2	CMOS				
184											G22	AUDATA1	184	AUDATA1	CMOS				
185											G21	AUDATA0	185	AUDATA0	CMOS				
186											L18	AUD SYNCZ	186	AUD SYNCZ	CMOS				
187											F21	AUDCK	187	AUDCK	CMOS				
188											K19	AUDRSTZ	188	AUDRSTZ	CMOS				
189	96	RESETZ	G14	RESETZ	G20	RESETZ	G20	RESETZ	G20	RESETZ	E20	RESETZ	189	RESETZ				SHMT2	
190	97	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	190	VSS					
191	98	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	191	VDD					
192	99	X2	F14	X2	F20	X2	F20	X2	F20	X2	E22	X2	192	X2					
193	100	OSCVSS	F13	OSCVSS	F19	OSCVSS	F19	OSCVSS	F19	OSCVSS	D22	OSCVSS	193	OSCVSS					
194					G19	OSCVSS	G19	OSCVSS	G19	OSCVSS			194	OSCVSS					
195	101	X1	E14	X1	E20	X1	E20	X1	E20	X1	C22	X1	195	X1	Special				
196	102	SYSVCC	SYS VCC	SYSVCC	SYS VCC	SYSVCC	SYS VCC	SYSVCC	SYS VCC	SYSVCC	SYS VCC	SYSVCC	196	SYSVCC					
197	103	P1_1	E13	P1_1	E19	P1_1	E19	P1_1	E19	P1_1	D21	P1_1	197	P1_1		SHMT1	SHMT4		GPIO
198	104	P1_2	D14	P1_2	D20	P1_2	D20	P1_2	D20	P1_2	D20	P1_2	198	P1_2		SHMT1	SHMT4		GPIO
199	105	P1_3	D13	P1_3	D19	P1_3	D19	P1_3	D19	P1_3	C21	P1_3	199	P1_3		SHMT1	SHMT4		GPIO
200	106	P1_4	C14	P1_4	C20	P1_4	C20	P1_4	C20	P1_4	C20	P1_4	200	P1_4		SHMT1	SHMT4		GPIO
201	107	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	201	E1VCC					
202	108	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	202	E1VSS					
203	45												203						
204					C19	P1_5	C19	P1_5	C19	P1_5	D19	P1_5	204	P1_5		SHMT1	SHMT4		GPIO
205					B19	P1_6	B19	P1_6	B19	P1_6	B21	P1_6	205	P1_6		SHMT1	SHMT4		GPIO
206					D16	P1_7	D16	P1_7	D16	P1_7	C19	P1_7	206	P1_7		SHMT1	SHMT4		GPIO
207	109	P2_0	C13	P2_0	B18	P2_0	B18	P2_0	B18	P2_0	D17	P2_0	207	P2_0		SHMT1	SHMT4		GPIO
208	110	P2_1	B14	P2_1	A18	P2_1	A18	P2_1	A18	P2_1	C18	P2_1	208	P2_1		SHMT1	SHMT4		GPIO
209	111	P2_2	B12	P2_2	B17	P2_2	B17	P2_2	B17	P2_2	B20	P2_2	209	P2_2		SHMT1	SHMT4		GPIO
210	112	P2_3	B11	P2_3	A17	P2_3	A17	P2_3	A17	P2_3	C17	P2_3	210	P2_3		SHMT1	SHMT4		GPIO
211	113	P2_4	A13	P2_4	B16	P2_4	B16	P2_4	B16	P2_4	A20	P2_4	211	P2_4		SHMT1	SHMT4		GPIO
212	114	P2_5	A12	P2_5	A16	P2_5	A16	P2_5	A16	P2_5	B19	P2_5	212	P2_5		SHMT1	SHMT4		GPIO
213	115	P2_6	A11	P2_6	B15	P2_6	B15	P2_6	B15	P2_6	D16	P2_6	213	P2_6		SHMT1	SHMT4		GPIO
214	116	P2_7	B10	P2_7	A15	P2_7	A15	P2_7	A15	P2_7	D15	P2_7	214	P2_7		SHMT1	SHMT4		GPIO

Table 2.1 Pin List (5/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
215	117	P2_8	A10	P2_8	B14	P2_8	B14	P2_8	B14	P2_8	A19	P2_8	215	P2_8		SHMT1	SHMT4		GPIO
216	118	P2_9	B9	P2_9	A14	P2_9	A14	P2_9	A14	P2_9	B18	P2_9	216	P2_9		SHMT1	SHMT4		GPIO
217	119	P2_10			B13	P2_10	B13	P2_10	B13	P2_10	C16	P2_10	217	P2_10		SHMT1	SHMT4		GPIO
218	120	P2_11			A13	P2_11	A13	P2_11	A13	P2_11	A18	P2_11	218	P2_11		SHMT1	SHMT4		GPIO
219	121	P2_12			B12	P2_12	B12	P2_12	B12	P2_12	B17	P2_12	219	P2_12		SHMT1	SHMT4		GPIO
220	122	P2_13			A12	P2_13	A12	P2_13	A12	P2_13	A17	P2_13	220	P2_13		SHMT1	SHMT4		GPIO
221	123	P2_14			B11	P2_14	B11	P2_14	B11	P2_14	B16	P2_14	221	P2_14		SHMT1	SHMT4		GPIO
222	124	VSS			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	222	VSS					
223	125	VDD			VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	223	VDD					
224	126	P2_15			A11	P2_15	A11	P2_15	A11	P2_15	A16	P2_15	224	P2_15		SHMT1	SHMT4		GPIO
225					K16	E1VSS	K16	P8_15	K16	P8_15	C15	P8_15	225	P8_15		SHMT1	SHMT4		GPIO
226					J17	E1VSS	J17	P8_14	J17	P8_14	D14	P8_14	226	P8_14		SHMT1	SHMT4		GPIO
227					H17	E1VSS	H17	P8_13	H17	P8_13	C14	P8_13	227	P8_13		SHMT1	SHMT4		GPIO
228					G17	E1VSS	G17	P8_12	G17	P8_12	B15	P8_12	228	P8_12		SHMT1	SHMT4		GPIO
229					F17	E1VSS	F17	P8_11	F17	P8_11	A15	P8_11	229	P8_11		SHMT1	SHMT4		HSIO
230					E17	E1VSS	E17	P8_10	E17	P8_10	D13	P8_10	230	P8_10		SHMT1	SHMT4		HSIO
231					D15	E1VSS	D15	P8_9	D15	P8_9	B14	P8_9	231	P8_9		SHMT1	SHMT4		HSIO
232					D14	E1VSS	D14	P8_8	D14	P8_8	A14	P8_8	232	P8_8		SHMT1	SHMT4		GPIO
233					E14	E1VSS	E14	P8_7	E14	P8_7	C13	P8_7	233	P8_7		SHMT1	SHMT4		GPIO
234					D13	E1VSS	D13	P8_6	D13	P8_6	C12	P8_6	234	P8_6		SHMT1	SHMT4		GPIO
235					E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	235	E1VSS					
236					E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	236	E1VCC					
237					D12	E1VSS	D12	P8_5	D12	P8_5	B13	P8_5	237	P8_5		SHMT1	SHMT4		GPIO
238					D11	E1VSS	D11	P8_4	D11	P8_4	A13	P8_4	238	P8_4		SHMT1	SHMT4		GPIO
239					E11	E1VSS	E11	P8_3	E11	P8_3	C11	P8_3	239	P8_3		SHMT1	SHMT4		GPIO
240					D10	E1VSS	D10	P8_2	D10	P8_2	B12	P8_2	240	P8_2		SHMT1	SHMT4		GPIO
241					E10	E1VSS	E10	P8_1	E10	P8_1	A12	P8_1	241	P8_1		SHMT1	SHMT4		GPIO
242					E9	E1VSS	E9	P8_0	E9	P8_0	A11	P8_0	242	P8_0		SHMT1	SHMT4		GPIO
243					D9	P7_0	D9	P7_0	D9	P7_0	C10	P7_0	243	P7_0		SHMT1	SHMT4		GPIO
244					D8	P7_1	D8	P7_1	D8	P7_1	B11	P7_1	244	P7_1		SHMT1	SHMT4		GPIO
245					D7	P7_2	D7	P7_2	D7	P7_2	A10	P7_2	245	P7_2		SHMT1	SHMT4		GPIO
246					D6	P7_3	D6	P7_3	D6	P7_3	B10	P7_3	246	P7_3		SHMT1	SHMT4		GPIO
247					D5	P7_4	D5	P7_4	D5	P7_4	A9	P7_4	247	P7_4		SHMT1	SHMT4		GPIO
248					E4	P7_5	E4	P7_5	E4	P7_5	B9	P7_5	248	P7_5		SHMT1	SHMT4		GPIO
249					F4	E1VSS	F4	P7_6	F4	P7_6	A8	P7_6	249	P7_6		SHMT1	SHMT4		GPIO
250					G4	E1VSS	G4	P7_7	G4	P7_7	B8	P7_7	250	P7_7		SHMT1	SHMT4		GPIO
251					H4	E1VSS	H4	P7_8	H4	P7_8	C9	P7_8	251	P7_8		SHMT1	SHMT4		GPIO
252					J4	E1VSS	J4	P7_9	J4	P7_9	A7	P7_9	252	P7_9		SHMT1	SHMT4		GPIO
253	127	P3_0	B8	P3_0	B10	P3_0	B10	P3_0	B10	P3_0	B7	P3_0	253	P3_0		SHMT1	SHMT4		GPIO
254	128	P3_1			A10	P3_1	A10	P3_1	A10	P3_1	A6	P3_1	254	P3_1		SHMT1	SHMT4		GPIO
255	129	P3_2			B9	P3_2	B9	P3_2	B9	P3_2	C8	P3_2	255	P3_2		SHMT1	SHMT4		GPIO
256	130	P3_3	B7	P3_3	A9	P3_3	A9	P3_3	A9	P3_3	B6	P3_3	256	P3_3		SHMT1	SHMT4		GPIO
257	131	P3_4	A9	P3_4	B8	P3_4	B8	P3_4	B8	P3_4	A5	P3_4	257	P3_4		SHMT1	SHMT4		GPIO
258	132	P3_5	A8	P3_5	A8	P3_5	A8	P3_5	A8	P3_5	C7	P3_5	258	P3_5		SHMT1	SHMT4		GPIO
259	133	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	E1 VCC	E1VCC	259	E1VCC					
260	134	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	E1 VSS	E1VSS	260	E1VSS					
261	135	P3_6	A7	P3_6	B7	P3_6	B7	P3_6	B7	P3_6	B5	P3_6	261	P3_6		SHMT1	SHMT4		GPIO
262	136	P3_7	A6	P3_7	A7	P3_7	A7	P3_7	A7	P3_7	D3	P3_7	262	P3_7		SHMT1	SHMT4		GPIO
263	137	P3_8	B6	P3_8	B6	P3_8	B6	P3_8	B6	P3_8	C5	P3_8	263	P3_8		SHMT1	SHMT4		GPIO
264	138	P3_9	A5	P3_9	A6	P3_9	A6	P3_9	A6	P3_9	C4	P3_9	264	P3_9		SHMT1	SHMT4		HSIO
265	139	P3_10	B5	P3_10	B5	P3_10	B5	P3_10	B5	P3_10	C6	P3_10	265	P3_10		SHMT1	SHMT4		HSIO
266	140	P3_12	A4	P3_12	A5	P3_12	A5	P3_12	A5	P3_12	C3	P3_12	266	P3_12		SHMT1	SHMT4		GPIO
267	141	P3_13	B4	P3_13	B4	P3_13	B4	P3_13	B4	P3_13	C2	P3_13	267	P3_13		SHMT1	SHMT4		GPIO
268	142	VDD	VDD	VDD	VDD	VDD							268	VDD					
269	143	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	269	VSS					
270	144	ERROR OUTZ	A2	ERROR OUTZ	A3	ERROR OUTZ	A3	ERROR OUTZ	A3	ERROR OUTZ	A3	ERROR OUTZ	270	ERROR OUTZ				SHMT2	GPIO50 Ohm (ERROR OUT)

Table 2.1 Pin List (6/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
271													271						
272			E12	SYSVCC	F16	SYSVCC	F16	SYSVCC	F16	SYSVCC	G18	SYSVCC	272	SYSVCC					
273					J16	SYSVCC	J16	SYSVCC	J16	SYSVCC	G19	SYSVCC	273	SYSVCC					
274			C5	VCC	G5	VCC	G5	VCC	G5	VCC	D7	VCC	274	VCC					
275			H3	VCC	L5	VCC	L5	VCC	L5	VCC	E7	VCC	275	VCC					
276					M5	VCC	M5	VCC	M5	VCC	G4	VCC	276	VCC					
277					E6	VCC	E6	VCC	E6	VCC	G5	VCC	277	VCC					
278											K4	VCC	278	VCC					
279											K5	VCC	279	VCC					
280			C8	VDD	K5	VDD	K5	VDD	K5	VDD	D4	VDD	280	VDD					
281			E6	VDD	E15	VDD	E15	VDD	E15	VDD	E5	VDD	281	VDD					
282			E7	VDD	J7	VDD	J7	VDD	J7	VDD	E16	VDD	282	VDD					
283			E8	VDD	K7	VDD	K7	VDD	K7	VDD	E17	VDD	283	VDD					
284			E9	VDD	L7	VDD	L7	VDD	L7	VDD	H9	VDD	284	VDD					
285			F3	VDD	M7	VDD	M7	VDD	M7	VDD	H10	VDD	285	VDD					
286			F5	VDD	P9	VDD	P9	VDD	P9	VDD	H13	VDD	286	VDD					
287			F10	VDD	P10	VDD	P10	VDD	P10	VDD	H14	VDD	287	VDD					
288			G5	VDD	P11	VDD	P11	VDD	P11	VDD	J8	VDD	288	VDD					
289			G10	VDD	P12	VDD	P12	VDD	P12	VDD	J10	VDD	289	VDD					
290			H5	VDD	M14	VDD	M14	VDD	M14	VDD	J13	VDD	290	VDD					
291			H10	VDD	L14	VDD	L14	VDD	L14	VDD	J15	VDD	291	VDD					
292			J5	VDD	K14	VDD	K14	VDD	K14	VDD	K8	VDD	292	VDD					
293			J10	VDD	J14	VDD	J14	VDD	J14	VDD	K9	VDD	293	VDD					
294			J12	VDD	G13	VDD	G13	VDD	G13	VDD	K14	VDD	294	VDD					
295			K6	VDD	G12	VDD	G12	VDD	G12	VDD	K15	VDD	295	VDD					
296			K7	VDD	G11	VDD	G11	VDD	G11	VDD	N8	VDD	296	VDD					
297			K8	VDD	G10	VDD	G10	VDD	G10	VDD	N9	VDD	297	VDD					
298			K9	VDD	G9	VDD	G9	VDD	G9	VDD	N14	VDD	298	VDD					
299											N15	VDD	299	VDD					
300											P8	VDD	300	VDD					
301											P10	VDD	301	VDD					
302											P13	VDD	302	VDD					
303											P15	VDD	303	VDD					
304											R4	VDD	304	VDD					
305											R5	VDD	305	VDD					
306											R9	VDD	306	VDD					
307											R10	VDD	307	VDD					
308											R13	VDD	308	VDD					
309											R14	VDD	309	VDD					
310											V7	VDD	310	VDD					
311											V15	VDD	311	VDD					
312			A1	VSS	A1	VSS	A1	VSS	A1	VSS	A1	VSS	312	VSS					
313			A3	VSS	A2	VSS	A2	VSS	A2	VSS	A2	VSS	313	VSS					
314			B2	VSS	A4	VSS	A4	VSS	A4	VSS	A4	VSS	314	VSS					
315			P14	VSS	B1	VSS	B1	VSS	B1	VSS	A21	VSS	315	VSS					
316			N13	VSS	B3	VSS	B3	VSS	B3	VSS	A22	VSS	316	VSS					
317			A14	VSS	Y19	VSS	Y19	VSS	Y19	VSS	B1	VSS	317	VSS					
318			B13	VSS	Y20	VSS	Y20	VSS	Y20	VSS	B2	VSS	318	VSS					
319			E5	VSS	W20	VSS	W20	VSS	W20	VSS	B3	VSS	319	VSS					
320			E10	VSS	B20	VSS	B20	VSS	B20	VSS	B4	VSS	320	VSS					
321			F6	VSS	A20	VSS	A20	VSS	A20	VSS	B22	VSS	321	VSS					
322			F7	VSS	A19	VSS	A19	VSS	A19	VSS	D1	VSS	322	VSS					
323			F8	VSS	D4	VSS	D4	VSS	D4	VSS	D2	VSS	323	VSS					
324			F9	VSS	E5	VSS	E5	VSS	E5	VSS	D5	VSS	324	VSS					
325			F12	VSS	F5	VSS	F5	VSS	F5	VSS	D6	VSS	325	VSS					
326			G3	VSS	N5	VSS	N5	VSS	N5	VSS	D8	VSS	326	VSS					
327			G6	VSS	U17	VSS	U17	VSS	U17	VSS	E3	VSS	327	VSS					
328			G7	VSS	T16	VSS	T16	VSS	T16	VSS	E4	VSS	328	VSS					
329			G8	VSS	T15	VSS	T15	VSS	T15	VSS	E6	VSS	329	VSS					

Table 2.1 Pin List (7/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
330			G9	VSS	R16	VSS	R16	VSS	R16	VSS	E8	VSS	330	VSS					
331			H6	VSS	E16	VSS	E16	VSS	E16	VSS	E13	VSS	331	VSS					
332			H7	VSS	D17	VSS	D17	VSS	D17	VSS	E14	VSS	332	VSS					
333			H8	VSS	G8	VSS	G8	VSS	G8	VSS	E15	VSS	333	VSS					
334			H9	VSS	H7	VSS	H7	VSS	H7	VSS	F4	VSS	334	VSS					
335			J6	VSS	H9	VSS	H9	VSS	H9	VSS	F5	VSS	335	VSS					
336			J7	VSS	H10	VSS	H10	VSS	H10	VSS	H8	VSS	336	VSS					
337			J8	VSS	H11	VSS	H11	VSS	H11	VSS	H11	VSS	337	VSS					
338			J9	VSS	H12	VSS	H12	VSS	H12	VSS	H12	VSS	338	VSS					
339			K5	VSS	H14	VSS	H14	VSS	H14	VSS	H15	VSS	339	VSS					
340			K10	VSS	J8	VSS	J8	VSS	J8	VSS	J9	VSS	340	VSS					
341			K12	VSS	J10	VSS	J10	VSS	J10	VSS	J11	VSS	341	VSS					
342					J11	VSS	J11	VSS	J11	VSS	J12	VSS	342	VSS					
343					J13	VSS	J13	VSS	J13	VSS	J14	VSS	343	VSS					
344					K8	VSS	K8	VSS	K8	VSS	K10	VSS	344	VSS					
345					K9	VSS	K9	VSS	K9	VSS	K11	VSS	345	VSS					
346					K10	VSS	K10	VSS	K10	VSS	K12	VSS	346	VSS					
347					K11	VSS	K11	VSS	K11	VSS	K13	VSS	347	VSS					
348					K12	VSS	K12	VSS	K12	VSS	L8	VSS	348	VSS					
349					K13	VSS	K13	VSS	K13	VSS	L9	VSS	349	VSS					
350					L8	VSS	L8	VSS	L8	VSS	L10	VSS	350	VSS					
351					L9	VSS	L9	VSS	L9	VSS	L11	VSS	351	VSS					
352					L10	VSS	L10	VSS	L10	VSS	L12	VSS	352	VSS					
353					L11	VSS	L11	VSS	L11	VSS	L13	VSS	353	VSS					
354					L12	VSS	L12	VSS	L12	VSS	L14	VSS	354	VSS					
355					L13	VSS	L13	VSS	L13	VSS	L15	VSS	355	VSS					
356					M8	VSS	M8	VSS	M8	VSS	M8	VSS	356	VSS					
357					M10	VSS	M10	VSS	M10	VSS	M9	VSS	357	VSS					
358					M11	VSS	M11	VSS	M11	VSS	M10	VSS	358	VSS					
359					M13	VSS	M13	VSS	M13	VSS	M11	VSS	359	VSS					
360					N7	VSS	N7	VSS	N7	VSS	M12	VSS	360	VSS					
361					N9	VSS	N9	VSS	N9	VSS	M13	VSS	361	VSS					
362					N10	VSS	N10	VSS	N10	VSS	M14	VSS	362	VSS					
363					N11	VSS	N11	VSS	N11	VSS	M15	VSS	363	VSS					
364					N12	VSS	N12	VSS	N12	VSS	N10	VSS	364	VSS					
365					N14	VSS	N14	VSS	N14	VSS	N11	VSS	365	VSS					
366					P8	VSS	P8	VSS	P8	VSS	N12	VSS	366	VSS					
367					P13	VSS	P13	VSS	P13	VSS	N13	VSS	367	VSS					
368											P9	VSS	368	VSS					
369											P11	VSS	369	VSS					
370											P12	VSS	370	VSS					
371											P14	VSS	371	VSS					
372											R8	VSS	372	VSS					
373											R11	VSS	373	VSS					
374											R12	VSS	374	VSS					
375											R15	VSS	375	VSS					
376											T4	VSS	376	VSS					
377											T5	VSS	377	VSS					
378											U5	VSS	378	VSS					
379											V6	VSS	379	VSS					
380											V14	VSS	380	VSS					
381											AA22	VSS	381	VSS					
382											AB21	VSS	382	VSS					
383											AB22	VSS	383	VSS					
384			M7	E0VCC	T10	E0VCC	T10	E0VCC	T10	E0VCC	D9	E1VCC	384	E1VCC					
385			M10	E0VCC	M16	E0VCC	M16	E0VCC	M16	E0VCC	D11	E1VCC	385	E1VCC					
386			C7	E1VCC	H16	E1VCC	H16	E1VCC	H16	E1VCC	E9	E1VCC	386	E1VCC					
387			C10	E1VCC	J5	E1VCC	J5	E1VCC	J5	E1VCC	E11	E1VCC	387	E1VCC					
388					E12	E1VCC	E12	E1VCC	E12	E1VCC	F18	E1VCC	388	E1VCC					

Table 2.1 Pin List (8/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch		P1M-C/P1H-C Pkg 156 0.8mm ball pitch		P1M-C Pkg 292 0.8mm ball pitch		P1H-C (4MB) Pkg 292		P1H-C (8MB) Pkg 292		P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
389					E8	E1VCC	E8	E1VCC	E8	E1VCC	F19	E1VCC	389	E1VCC					
390											J4	E1VCC	390	E1VCC					
391											J5	E1VCC	391	E1VCC					
392											J18	E1VCC	392	E1VCC					
393											T18	E0VCC	393	E0VCC					
394											U18	E0VCC	394	E0VCC					
395											V13	E0VCC	395	E0VCC					
396			M8	E0VSS	T11	E0VSS	T11	E0VSS	T11	E0VSS	D10	E1VSS	396	E1VSS					
397			M9	E0VSS	N16	E0VSS	N16	E0VSS	N16	E0VSS	D12	E1VSS	397	E1VSS					
398			C6	E1VSS	G16	E1VSS	G16	E1VSS	G16	E1VSS	D18	E1VSS	398	E1VSS					
399			C9	E1VSS	H5	E1VSS	H5	E1VSS	H5	E1VSS	E10	E1VSS	399	E1VSS					
400					E13	E1VSS	E13	E1VSS	E13	E1VSS	E12	E1VSS	400	E1VSS					
401					E7	E1VSS	E7	E1VSS	E7	E1VSS	E18	E1VSS	401	E1VSS					
402											E19	E1VSS	402	E1VSS					
403											H4	E1VSS	403	E1VSS					
404											H5	E1VSS	404	E1VSS					
405											H18	E1VSS	405	E1VSS					
406											V12	E0VSS	406	E0VSS					
407											V16	E0VSS	407	E0VSS					
408											V17	E0VSS	408	E0VSS					
409											V18	E0VSS	409	E0VSS					
410											W1	A1VCC	410	A1VCC					
411											W2	A1VCC	411	A1VCC					
412											U3	A1VCC	412	A1VCC					
413											V3	A1VCC	413	A1VCC					
414											U4	A1VCC	414	A1VCC					
415					W1	A1VSS	W1	A1VSS	W1	A1VSS	AA1	A1VSS	415	A1VSS					
416					W2	A1VSS	W2	A1VSS	W2	A1VSS	AA2	A1VSS	416	A1VSS					
417					Y1	A1VSS	Y1	A1VSS	Y1	A1VSS	W3	A1VSS	417	A1VSS					
418											V4	A1VSS	418	A1VSS					
419											Y4	A0VCC	419	A0VCC					
420											AA4	A0VCC	420	A0VCC					
421											AB4	A0VCC	421	A0VCC					
422			P1	A0VSS	R5	A0VSS	R5	A0VSS	R5	A0VSS	AB1	A0VSS	422	A0VSS					
423					T5	A0VSS	T5	A0VSS	T5	A0VSS	AB2	A0VSS	423	A0VSS					
424					T6	A0VSS	T6	A0VSS	T6	A0VSS	Y3	A0VSS	424	A0VSS					
425					U4	A0VSS	U4	A0VSS	U4	A0VSS	W4	A0VSS	425	A0VSS					
426					Y2	A0VSS	Y2	A0VSS	Y2	A0VSS	V5	A0VSS	426	A0VSS					
427											L4	VSS	427	VSS					
428											L5	VSS	428	VSS					
429											V8	VSS	429	VSS					
430											W8	VSS	430	VSS					
431											M4	ERAM VDD	431	ERAM VDD					
432											M5	ERAMV DD	432	ERAM VDD					
433											V9	ERAM VDD	433	ERAM VDD					
434											W9	ERAM VDD	434	ERAM VDD					
435											N4	ERAM1 VSS	435	ERAM1 VSS					
436											N5	ERAM1 VSS	436	ERAM1 VSS					
437											V10	ERAM0 VSS	437	ERAM0 VSS					
438											W10	ERAM0 VSS	438	ERAM0 VSS					
439											P4	ERAM1 VCC	439	ERAM1 VCC					
440											P5	ERAM1 VCC	440	ERAM1 VCC					
441											V11	ERAM0 VCC	441	ERAM0 VCC					

Table 2.1 Pin List (9/9)

Ref. Nr.	P1M-C Pkg 144 0.4mm pin pitch	P1M-C/P1H-C Pkg 156 0.8mm ball pitch	P1M-C Pkg 292 0.8mm ball pitch	P1H-C (4MB) Pkg 292	P1H-C (8MB) Pkg 292	P1H-CE Pkg 404		Superset Ref.Nr.	Port name	Port buffer settings: Port Input Type	Port Input Type	Port Input Type	Port Input Type	Port Output Type
442						W11	ERAM0 VCC	442	ERAM0 VCC					
443						J20	DVSS	443	DVSS					
444						J21	DVSS	444	DVSS					
445						J22	DVSS	445	DVSS					
446						K20	DVSS	446	DVSS					
447						L20	DVSS	447	DVSS					
448						L21	DVSS	448	DVSS					
449						L22	DVSS	449	DVSS					
450						M19	DVSS	450	DVSS					
451						M20	DVSS	451	DVSS					
452						N20	DVSS	452	DVSS					
453						N21	DVSS	453	DVSS					
454						N22	DVSS	454	DVSS					
455						P20	DVSS	455	DVSS					
456						R20	DVSS	456	DVSS					
457						R21	DVSS	457	DVSS					
458						R22	DVSS	458	DVSS					

2.1.3 Pin Function assignments

Table 2.3 Pin Function assignments (1/6)

1st Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
1															
2	P3_14	GTM0I1	√	√	√	√	√	√	GTMAT0O1	√	√	√	√	√	√
3	P4_0	GTM1I0	√	√	√	√	√	√	GTMAT0O0	√	√	√	√	√	√
4	P4_1	GTM0I2	√	√	√	√	√	√	GTMAT0O2	√	√	√	√	√	√
5	P4_2 (MODE0)	GTM1I1	√	√	√	√	√	√	GTMAT0O1	√	√	√	√	√	√
6	VDD														
7	P4_3 (MODE1)	GTM0I3	√	√	√	√	√	√	GTMAT0O0N	√	√	√	√	√	√
8	P4_4	GTM0I6	√	√	√	√	√	√	GTMAT0O2	√	√	√	√	√	√
9	P4_5 (FLMD1)	GTM1I4	√	√	√	√	√	√	GTMAT0O0	√	√	√	√	√	√
10	P4_6	GTM1I5	√	√	√	√	√	√	GTMAT0O5	√	√	√	√	√	√
11	P4_7	GTM1I1	√	√	√	√	√	√	GTMAT0O5	√	√	√	√	√	√
12	E1VSS														
13	E1 VCC														
14	P4_8	GTM1I0	√	√	√	√	√	√	GTMAT0O0N	√	√	√	√	√	√
15	P4_9	GTM1I4	√	√	√	√	√	√	GTMAT0O4	√	√	√	√	√	√
16	P4_10	GTM0I3	√	√	√	√	√	√	GTMAT1O1N	√	√	√	√	√	√
17	P4_11	GTM0I2	√	√	√	√	√	√	GTMAT1O2N	√	√	√	√	√	√
18	P4_12	GTM0I1	√	√	√	√	√	√	GTMAT1O3N	√	√	√	√	√	√
19	VDD														
20	VSS														
21	VCC														
22	P4_13	GTM1I7	√	√	√	√	√	√	GTMAT1O0	√	√	√	√	√	√
23	P4_14	GTM1I7	√		√	√	√	√	GTMAT1O0N	√		√	√	√	√
24	P6_0	GTM1I6	√		√	√	√	√	GTMAT1O1	√		√	√	√	√
25	P6_1	GTM1I6	√		√	√	√	√	GTMAT1O1N	√		√	√	√	√
26	ERAMRESPDZ														
27	ERAMRES2Z														
28	ADC1I0														
29	ADC1I1														
30	ADC1I2														
31	ADC1I3														
32	ADC1I4														
33	ADC1I5														
34	ADC1I6														
35	ADC1I7														
36	ADC1I8														
37	ADC1I9														
38	ADC1I10														
39	ADC1I11														
40	ADC1I12														
41	ADC1I13														
42	ADC1I14														

2nd Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
1															
2	P3_14	RLIN30RX	√	√	√	√	√	√	ETH0TXEN	√	√	√	√	√	√
3	P4_0	ETH0RXER	√	√	√	√	√	√							
4	P4_1	ETH0TXCLK	√	√	√	√	√	√							
5	P4_2 (MODE0)	ETH0RXCLK	√	√	√	√	√	√							
6	VDD														
7	P4_3 (MODE1)	ETH0RXD0	√	√	√	√	√	√							
8	P4_4	ETH0RXD1	√	√	√	√	√	√	RLIN30TX	√	√	√	√	√	√
9	P4_5 (FLMD1)	ETH0RXD2	√	√	√	√	√	√							
10	P4_6	ETH0RXD3	√	√	√	√	√	√	RLIN30TX	√	√	√	√	√	√
11	P4_7	ETH0RXDV	√	√	√	√	√	√							
12	E1VSS														
13	E1 VCC														
14	P4_8								ETH0WOL	√	√	√	√	√	√
15	P4_9								EXTCLK1O	√	√	√	√	√	√
16	P4_10	MCAN1RX	√	√	√	√	√	√							
17	P4_11								MCAN1TX	√	√	√	√	√	√
18	P4_12	INTP1	√	√	√	√	√	√	FLXNTUOUT	√	√	√	√	√	√
19	VDD														
20	VSS														
21	VCC														
22	P4_13								CSIH0CSS5	√	√	√	√	√	√
23	P4_14								CSIH0CSS6	√		√	√	√	√
24	P6_0														
25	P6_1														
26	ERAMRESPDZ														
27	ERAMRES2Z														
28	ADC1I0														
29	ADC1I1														
30	ADC1I2														
31	ADC1I3														
32	ADC1I4														
33	ADC1I5														
34	ADC1I6														
35	ADC1I7														
36	ADC1I8														
37	ADC1I9														
38	ADC1I10														
39	ADC1I11														
40	ADC1I12														
41	ADC1I13														
42	ADC1I14														

3rd Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
1															
2	P3_14	MCAN0RX	√	√	√	√	√	√							
3	P4_0								MCAN0TX	√	√	√	√	√	√
4	P4_1	CSIH1SSIZ	√	√	√	√	√	√	CSIH1CSS0	√	√	√	√	√	√
5	P4_2 (MODE0)	CSIH1DCS	√	√	√	√	√	√	CSIH1SO0	√	√	√	√	√	√
6	VDD														
7	P4_3 (MODE1)	CSIH1SCI0	√	√	√	√	√	√	CSIH1SCO0	√	√	√	√	√	√
8	P4_4	CSIH1SI0	√	√	√	√	√	√							
9	P4_5 (FLMD1)	MTTCAN0RX	√	√	√	√	√	√							
10	P4_6								MTTCAN0TX	√	√	√	√	√	√
11	P4_7	INTP0	√	√	√	√	√	√	EXTCLK0O	√	√	√	√	√	√
12	E1VSS														
13	E1 VCC														
14	P4_8	RLIN30RX	√	√	√	√	√	√							
15	P4_9	CSIH2SSIZ	√	√	√	√	√	√	CSIH2CSS0	√	√	√	√	√	√
16	P4_10	CSIH2DCS	√	√	√	√	√	√	CSIH2SO2	√	√	√	√	√	√
17	P4_11	CSIH2SCI2	√	√	√	√	√	√	CSIH2SCO2	√	√	√	√	√	√
18	P4_12	CSIH2SI2	√	√	√	√	√	√							
19	VDD														
20	VSS														
21	VCC														
22	P4_13	SENT2RX	√	√	√	√	√	√							
23	P4_14	SENT3RX	√		√	√	√	√							
24	P6_0	SENT4RX	√		√	√	√	√							
25	P6_1	SENT5RX	√		√	√	√	√							
26	ERAMRESPDZ														
27	ERAMRES2Z														
28	ADC1I0														
29	ADC1I1														
30	ADC1I2														
31	ADC1I3														
32	ADC1I4														
33	ADC1I5														
34	ADC1I6														
35	ADC1I7														
36	ADC1I8														
37	ADC1I9														
38	ADC1I10														
39	ADC1I11														
40	ADC1I12														
41	ADC1I13														
42	ADC1I14														

4th Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
1															
2	P3_14	FLX0RXDA/ INTP10	√	√	√	√	√	√							
3	P4_0	FLX0RXDB	√	√	√	√	√	√	RLIN30TX	√	√	√	√	√	√
4	P4_1	FLX0STPWT	√	√	√	√	√	√							
5	P4_2 (MODE0)								FLX0TXENA	√	√	√	√	√	√
6	VDD														
7	P4_3 (MODE1)								FLX0TXDB	√	√	√	√	√	√
8	P4_4								FLX0TXDA	√	√	√	√	√	√
9	P4_5 (FLMD1)	RLIN30RX	√	√	√	√	√	√	FLX0TXENB	√	√	√	√	√	√
10	P4_6														
11	P4_7	SENT0RX	√	√	√	√	√	√	BHPDGRCLK0	√	√	√	√	√	√
12	E1VSS														
13	E1 VCC														
14	P4_8	SENT1RX	√	√	√	√	√	√	BHPDGRCLK1	√	√	√	√	√	√
15	P4_9								RLIN30TX	√	√	√	√	√	√
16	P4_10								CSIH0CSS3	√	√	√	√	√	√
17	P4_11								CSIH1CSS4	√	√	√	√	√	√
18	P4_12	ADC1TRG	√	√	√	√	√	√	CSIH1CSS5	√	√	√	√	√	√
19	VDD														
20	VSS														
21	VCC														
22	P4_13	ESO1Z	√	√	√	√	√	√	CSIH2CSS7	√	√	√	√	√	√
23	P4_14								EXTCLK1O	√		√	√	√	√
24	P6_0								CSIH1CSS6	√		√	√	√	√
25	P6_1								CSIH0CSS7	√		√	√	√	√
26	ERAMRESPDZ														
27	ERAMRES2Z														
28	ADC1I0														
29	ADC1I1														
30	ADC1I2														
31	ADC1I3														
32	ADC1I4														
33	ADC1I5														
34	ADC1I6														
35	ADC1I7														
36	ADC1I8														
37	ADC1I9														
38	ADC1I10														
39	ADC1I11														
40	ADC1I12														
41	ADC1I13														
42	ADC1I14														

Special Function

Superset Ref.Nr.	Port name	Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
1								
2	P3_14							
3	P4_0							
4	P4_1							
5	P4_2 (MODE0)	MODE0	√	√	√	√	√	√
6	VDD							
7	P4_3 (MODE1)	MODE1	√	√	√	√	√	√
8	P4_4							
9	P4_5 (FLMD1)	FLMD1	√	√	√	√	√	√
10	P4_6							
11	P4_7							
12	E1VSS							
13	E1 VCC							
14	P4_8							
15	P4_9							
16	P4_10							
17	P4_11							
18	P4_12							
19	VDD							
20	VSS							
21	VCC							
22	P4_13							
23	P4_14							
24	P6_0	ICUMGPIO0	√		√	√	√	√
25	P6_1	ICUMGPIO1	√		√	√	√	√
26	ERAMRESPDZ							√
27	ERAMRES2Z							√
28	ADC1I0		√	√	√	√	√	√
29	ADC1I1		√	√	√	√	√	√
30	ADC1I2		√	√	√	√	√	√
31	ADC1I3		√	√	√	√	√	√
32	ADC1I4		√	√	√	√	√	√
33	ADC1I5		√	√	√	√	√	√
34	ADC1I6		√	√	√	√	√	√
35	ADC1I7		√	√	√	√	√	√
36	ADC1I8		√	√	√	√	√	√
37	ADC1I9		√	√	√	√	√	√
38	ADC1I10		√	√	√	√	√	√
39	ADC1I11		√	√	√	√	√	√
40	ADC1I12					√	√	√
41	ADC1I13					√	√	√
42	ADC1I14					√	√	√

Table 2.3 Pin Function assignments (2/6)

Superset Ref.Nr.	Port name	1st Alternative In Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	1st Alternative Out Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	2nd Alternative In Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
43	ADC1I15																					
44	ADC1I16																					
45	ADC1I17																					
46	ADC1I18																					
47	ADC1I19																					
48	A1 VCC																					
49	A1 VREFH																					
50	A1VSS																					
51	A1VSS																					
52																						
53	A0 VREFH																					
54	A0VSS																					
55	A0VSS																					
56	A0 VCC																					
57	ADC0I19																					
58	ADC0I18																					
59	ADC0I17																					
60	ADC0I16																					
61	ADC0I15																					
62	ADC0I14																					
63	ADC0I13																					
64	ADC0I12																					
65	ADC0I11																					
66	ADC0I10																					
67	ADC0I9																					
68	ADC0I8																					
69	ADC0I7																					
70	ADC0I6																					
71	ADC0I5																					
72	ADC0I4																					
73	ADC0I3																					
74	ADC0I2																					
75	ADC0I1																					
76	ADC0I0																					
77	VDD																					
78	P6_2	GTM0I6	√		√	√	√	√	GTMAT0O6	√		√	√	√	√							
79	P6_3	GTM0I3	√		√	√	√	√	GTMAT0O7	√		√	√	√	√	HSURT2CSI				√	√	√
80	P6_4	GTM0I4			√	√	√	√	GTMAT2O3N				√	√	√	HSURT2SCKI				√	√	√
81	P6_5	GTM0I0			√	√	√	√	GTMAT2O3				√	√	√	HSURT2 SDIO3I				√	√	√
82	P6_6	GTM0I2			√	√	√	√	GTMAT2O2N				√	√	√	HSURT2 SDIO2I				√	√	√
83	E0 VCC																					
84	E0VSS																					
85	P6_7	GTM0I5				√	√	√	GTMAT2O2				√	√	√	HSURT2 SDIO1I				√	√	√
86	P6_8	GTM0I6				√	√	√	GTMAT2O1N				√	√	√	HSURT2 SDIO0I				√	√	√
87	P6_9	GTM1I2				√	√	√	GTMAT2O1				√	√	√							

Superset Ref.Nr.	Port name	2nd Alternative Out Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	3rd Alternative In Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	3rd Alternative Out Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
43	ADC1I15																					
44	ADC1I16																					
45	ADC1I17																					
46	ADC1I18																					
47	ADC1I19																					
48	A1 VCC																					
49	A1 VREFH																					
50	A1VSS																					
51	A1VSS																					
52																						
53	A0 VREFH																					
54	A0VSS																					
55	A0VSS																					
56	A0 VCC																					
57	ADC0I19																					
58	ADC0I18																					
59	ADC0I17																					
60	ADC0I16																					
61	ADC0I15																					
62	ADC0I14																					
63	ADC0I13																					
64	ADC0I12																					
65	ADC0I11																					
66	ADC0I10																					
67	ADC0I9																					
68	ADC0I8																					
69	ADC0I7																					
70	ADC0I6																					
71	ADC0I5																					
72	ADC0I4																					
73	ADC0I3																					
74	ADC0I2																					
75	ADC0I1																					
76	ADC0I0																					
77	VDD																					
78	P6_2	HSURT2 SDIR				√	√	√	SENT4RX	√		√	√	√	√							
79	P6_3	HSURT2CSO				√	√	√	SENT5RX	√		√	√	√	√							
80	P6_4	HSURT2 SCKO				√	√	√	SENT6RX				√	√	√							
81	P6_5	HSURT2 SDIO3O				√	√	√	SENT7RX				√	√	√							
82	P6_6	HSURT2 SDIO2O				√	√	√								SENT6SPCO				√	√	√
83	E0 VCC																					
84	E0VSS																					
85	P6_7	HSURT2 SDIO1O				√	√	√								SENT7SPCO				√	√	√
86	P6_8	HSURT2 SDIO0O				√	√	√														
87	P6_9																					

Superset Ref.Nr.	Port name	4th Alternative In Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	4th Alternative Out Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	Special Function Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
43	ADC1I15																			√	√	√
44	ADC1I16																				√	√
45	ADC1I17																				√	√
46	ADC1I18																				√	√
47	ADC1I19																				√	√
48	A1 VCC																√	√	√	√	√	√
49	A1 VREFH																√	√	√	√	√	√
50	A1VSS																√	√	√	√	√	√
51	A1VSS																√	√	√	√	√	√
52																						
53	A0 VREFH																√	√	√	√	√	√
54	A0VSS																√	√	√	√	√	√
55	A0VSS																√	√	√	√	√	√
56	A0 VCC																√	√	√	√	√	√
57	ADC0I19																				√	√
58	ADC0I18																				√	√
59	ADC0I17																				√	√
60	ADC0I16																				√	√
61	ADC0I15																			√	√	√
62	ADC0I14																			√	√	√
63	ADC0I13																			√	√	√
64	ADC0I12																			√	√	√
65	ADC0I11																	√	√	√	√	√
66	ADC0I10																	√	√	√	√	√
67	ADC0I9																√	√	√	√	√	√
68	ADC0I8																√	√	√	√	√	√
69	ADC0I7																√	√	√	√	√	√
70	ADC0I6																√	√	√	√	√	√
71	ADC0I5																√	√	√	√	√	√
72	ADC0I4																√	√	√	√	√	√
73	ADC0I3																√	√	√	√	√	√
74	ADC0I2																√	√	√	√	√	√
75	ADC0I1																√	√	√	√	√	√
76	ADC0I0																√	√	√	√	√	√
77	VDD																					
78	P6_2								CSIH1CSS7	√		√	√	√	√							
79	P6_3								MCAN0TX	√		√	√	√	√							
80	P6_4	INTP9			√	√	√	√														
81	P6_5																					
82	P6_6																					
83	E0 VCC																					
84	E0VSS																					
85	P6_7																					
86	P6_8																					
87	P6_9								HSURT3SDIR				√	√	√							

Table 2.3 Pin Function assignments (3/6)

Assignment columns (in each group, in order): P1M-C (QFP-144), P1M-C/P1H-C (BGA-156), P1M-C (BGA-292), P1H-C (4MB), P1H-C (8MB), P1H-CE

Superset Ref.Nr.	Port name	1st Alternative In: Function name	Assignment	1st Alternative Out: Function name	Assignment	2nd Alternative In: Function name	Assignment	2nd Alternative Out: Function name	Assignment	3rd Alternative In: Function name	Assignment	3rd Alternative Out: Function name	Assignment	4th Alternative In: Function name	Assignment	4th Alternative Out: Function name	Assignment	Special Function: Function name	Assignment
88	P6_10	GTM0I7	√ √ √ √	GTMAT2O0N	√ √ √	CSIH3SCI1	√ √ √ √	CSIH3SCO1	√ √ √ √					HSURT3CSI	√ √ √	HSURT3CSO	√ √ √		
89	P6_11	GTM0I3	√ √ √ √	GTMAT2O0	√ √ √			CSIH3CSS0	√ √ √ √					HSURT3SCKI	√ √ √	HSURT3 SCKO	√ √ √		
90	P6_12	GTM1I6	√ √ √ √	GTMAT1O7	√ √ √	CSIH3SI1	√ √ √ √							HSURT3 SDIO3I	√ √ √	HSURT3 SDIO3O	√ √ √		
91	P6_13	GTM1I7	√ √ √ √	GTMAT1O6	√ √ √	CSIH3DCS	√ √ √ √	CSIH3SO1	√ √ √ √					HSURT3 SDIO2I	√ √ √	HSURT3 SDIO2O	√ √ √		
92	P6_14	GTM1I1	√ √ √	GTMAT1O5	√ √ √									HSURT3 SDIO1I	√ √ √	HSURT3 SDIO1O	√ √ √		
93	P6_15	GTM1I0	√ √ √	GTMAT1O4	√ √ √									HSURT3 SDIO0I	√ √ √	HSURT3 SDIO0O	√ √ √		
94	P5_0	GTM0I0	√ √ √ √ √ √	GTMAT0O3	√ √ √ √ √ √					MCAN0RX	√ √ √ √ √ √					CSIH2CSS2	√ √ √ √ √ √		
95	P5_1	GTM1I3	√ √ √ √ √ √	GTMAT0O0N	√ √ √ √ √ √			CSIH0CSS1	√ √ √ √ √ √			MCAN0TX	√ √ √ √ √ √			CSIH2CSS3	√ √ √ √ √ √		
96	VSS																		
97	VDD																		
98	P5_4	GTM1I5	√ √ √ √ √ √	GTMAT0O1	√ √ √ √ √ √	CSIH0SSIZ	√ √ √ √ √ √	CSIH0CSS0	√ √ √ √ √ √	ADC0TRG	√ √ √ √ √ √	ADC1CNV	√ √ √ √ √ √	RLIN31RX	√ √ √ √ √ √				
99	P5_5	GTM1I0	√ √ √ √ √ √	GTMAT0O4	√ √ √ √ √ √	CSIH0DCS	√ √ √ √ √ √	CSIH0SO0	√ √ √ √ √ √			ADC0CNV	√ √ √ √ √ √			RLIN31TX	√ √ √ √ √ √		
100	P5_6	GTM0I3	√ √ √ √ √ √	GTMAT1O0	√ √ √ √ √ √	CSIH0SCI0	√ √ √ √ √ √	CSIH0SCO0	√ √ √ √ √ √			SENT4SPCO	√ √ √ √ √	CSIH2DCS	√ √ √ √ √ √	CSIH2SO1	√ √ √ √ √ √		
101	P5_7	GTM0I7	√ √ √ √ √ √	GTMAT1O0N	√ √ √ √ √ √	CSIH0SI0	√ √ √ √ √ √			NMI	√ √ √ √ √ √	SENT5SPCO	√ √ √ √ √	CSIH2SCI1	√ √ √ √ √ √	CSIH2SCO1	√ √ √ √ √ √		
102	E0 VCC																		
103	E0VSS																		
104	P5_8	GTM0I7	√ √ √ √ √ √	GTMAT0O3	√ √ √ √ √ √			RLIN30TX	√ √ √ √ √ √			EXTCLK1O	√ √ √ √ √ √	CSIH0RYI	√ √ √ √ √ √	CSIH0RYO	√ √ √ √ √ √		
105	P5_9	GTM1I3	√ √ √ √ √ √	GTMAT0O3N	√ √ √ √ √ √	RLIN30RX	√ √ √ √ √ √					MCAN1TX	√ √ √ √ √ √			CSIH1CSS3	√ √ √ √ √ √		
106	P5_10	GTM0I6	√ √ √ √ √ √	GTMAT1O1	√ √ √ √ √ √			EXTCLK0O	√ √ √ √ √ √	MCAN1RX	√ √ √ √ √ √			CSIH2SI1	√ √ √ √ √ √				
107	P5_11	GTM0I6	√ √ √ √ √	GTMAT1O1N	√ √ √ √ √														
108	P5_12	GTM1I1	√ √ √ √ √ √	GTMAT1O2	√ √ √ √ √ √			EXTCLK0O	√ √ √ √ √ √			CSIH2CSS3	√ √ √ √ √ √	SENT3RX	√ √ √ √ √ √				
109	P5_13	GTM1I2	√ √ √ √ √ √	GTMAT1O2N	√ √ √ √ √ √	SENT2RX	√ √ √ √ √ √			INTP2	√ √ √ √ √ √	CSIH0CSS2	√ √ √ √ √ √	RLIN30RX	√ √ √ √ √ √				
110	P5_14	GTM1I2	√ √ √ √ √ √	GTMAT0O2	√ √ √ √ √ √			MTTCAN0TX	√ √ √ √ √ √			RLIN30TX	√ √ √ √ √ √			CSIH2CSS0	√ √ √ √ √ √		
111	P5_15	GTM1I5	√ √ √ √ √ √	GTMAT0O2N	√ √ √ √ √ √	MTTCAN0RX	√ √ √ √ √ √			RLIN30RX	√ √ √ √ √ √					CSIH0CSS4	√ √ √ √ √ √		
112	P0_0	GTM0I6	√ √ √ √ √ √	GTMAT0O2	√ √ √ √ √ √					SENT0RX	√ √ √ √ √ √	CSIH0CSS1	√ √ √ √ √ √			CSIH0CSS5	√ √ √ √ √ √		
113	P0_1	GTM0I3	√ √ √ √ √ √	GTMAT0O3N	√ √ √ √ √ √					SENT1RX	√ √ √ √ √ √	CSIH1CSS6	√ √ √ √ √ √			CSIH0CSS6	√ √ √ √ √ √		
114	P3_11	GTM1I1	√ √ √ √ √ √	GTMAT0O1	√ √ √ √ √ √							CSIH1CSS7	√ √ √ √ √ √			CSIH0CSS7	√ √ √ √ √ √		
115	P9_0			GTMAT0O4	√ √ √											SENT8SPCO	√		
116	P9_1			GTMAT1O3N	√ √ √									SENT8RX	√	RLIN33TX	√ √ √		
117	P9_2			GTMAT1O3	√ √ √									RLIN33RX	√ √ √	SENT9SPCO	√		
118	P9_3			GTMAT1O2N	√ √ √									SENT9RX	√				
119	E0 VCC																		
120	E0VSS																		
121	P9_4			GTMAT1O2	√ √ √														
122	P9_5			GTMAT1O1N	√ √ √											CSIH1CSS5	√ √ √		
123	P9_6			GTMAT1O1	√ √ √											CSIH1CSS4	√ √ √		
124	P9_7			GTMAT1O0N	√ √ √ √			MCAN2TX	√ √										
125	P9_8			GTMAT1O0	√ √ √ √	MCAN2RX	√ √												
126																			
127	P0_2	GTM0I2	√ √ √ √ √ √	GTMAT1O1	√ √ √ √ √ √			CSIH2CSS2	√ √ √ √ √ √			CSIH0CSS4	√ √ √ √ √ √						
128	P0_3	GTM1I0	√ √ √ √ √	GTMAT0O0	√ √ √ √ √			CSIH2CSS4	√ √ √ √ √			CSIH0CSS3	√ √ √ √ √						
129	P0_4	GTM0I1	√ √ √ √ √	GTMAT1O2	√ √ √ √ √			CSIH2CSS5	√ √ √ √ √			CSIH1CSS2	√ √ √ √ √						
130	P0_5	GTM1I3	√ √ √ √ √ √	GTMAT1O0	√ √ √ √ √ √	INTP3	√ √ √ √ √ √	CSIH2CSS6	√ √ √ √ √ √							CSIH1CSS1	√ √ √ √ √ √		
131	P0_6	GTM0I0	√ √ √ √ √	GTMAT0O6	√ √ √ √ √			CSIH2CSS7	√ √ √ √ √							CSIH1CSS0	√ √ √ √ √		
132	P0_7	GTM0I4	√ √ √ √ √	GTMAT1O2	√ √ √ √ √	MCAN1RX	√ √ √ √ √			CSIH0SI2	√ √ √ √ √			CSIH1DCS	√ √ √ √ √	CSIH1SO2	√ √ √ √ √		

Table 2.3 Pin Function assignments (4/6)

1st Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
133	P0_8	GTM0I5	√		√	√	√	√	GTMAT1O3	√		√	√	√	√
134	P0_9	GTM1I4	√		√	√	√	√	GTMAT1O0N	√		√	√	√	√
135	FLMD0														
136	CVMOUTZ														
137	E0VSS														
138	E0 VCC														
139	P0_10 (RESETOUTZ)														
140	VDD														
141	VSS														
142	P0_13	GTM1I3	√		√	√	√	√	GTMAT1O1N	√		√	√	√	√
143	P0_14	GTM0I2	√	√	√	√	√	√	GTMAT0O4	√	√	√	√	√	√
144	MSYNZ														
145	EMU VCC														
146	EMU VSS														
147	AURORES2Z														
148	AURORES1Z														
149	AURORESPDZ														
150	EMU VDD														
151	EMU VDD														
152	VSS														
153	VSS														
154	DVDD														
155	TODP0														
156	TODN0														
157	DVSS														
158	TODP1														
159	TODN1														
160	DVDD														
161	DVSS														
162	DVSS														
164	CICREFP														
165	CICREFN														
166	DVCC														
167	DVCC														
168	DVSS														
169	VSS														
170	JP0_5 (RDYZ)														
171	JP0_3 (TMS)														
172	JP0_2 (TCK)														
175	JP0_1 (TDO)														
176	JP0_0 (TDI)														
177	JP0_4 (TRSTZ)														
178	EVTOZ														
179	EVTIZ														
182	AUDATA3														

2nd Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
133	P0_8								MCAN1TX	√		√	√	√	√
134	P0_9								EXTCLK1O	√		√	√	√	√
135	FLMD0														
136	CVMOUTZ														
137	E0VSS														
138	E0 VCC														
139	P0_10 (RESETOUTZ)														
140	VDD														
141	VSS														
142	P0_13	CSIH1RYI	√		√	√	√	√	CSIH1RYO	√		√	√	√	√
143	P0_14								EXTCLK1O	√	√	√	√	√	√
144	MSYNZ														
145	EMU VCC														
146	EMU VSS														
147	AURORES2Z														
148	AURORES1Z														
149	AURORESPDZ														
150	EMU VDD														
151	EMU VDD														
152	VSS														
153	VSS														
154	DVDD														
155	TODP0														
156	TODN0														
157	DVSS														
158	TODP1														
159	TODN1														
160	DVDD														
161	DVSS														
162	DVSS														
164	CICREFP														
165	CICREFN														
166	DVCC														
167	DVCC														
168	DVSS														
169	VSS														
170	JP0_5 (RDYZ)														
171	JP0_3 (TMS)														
172	JP0_2 (TCK)														
175	JP0_1 (TDO)														
176	JP0_0 (TDI)														
177	JP0_4 (TRSTZ)														
178	EVTOZ														
179	EVTIZ														
182	AUDATA3														

3rd Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
133	P0_8	CSIH0SCI2	√		√	√	√	√	CSIH0SCO2	√		√	√	√	√
134	P0_9	CSIH0DCS	√		√	√	√	√	CSIH0SO2	√		√	√	√	√
135	FLMD0														
136	CVMOUTZ														
137	E0VSS														
138	E0 VCC														
139	P0_10 (RESETOUTZ)														
140	VDD														
141	VSS														
142	P0_13	SENT4RX	√		√	√	√	√							
143	P0_14	SENT0RX	√	√	√	√	√	√							
144	MSYNZ														
145	EMU VCC														
146	EMU VSS														
147	AURORES2Z														
148	AURORES1Z														
149	AURORESPDZ														
150	EMU VDD														
151	EMU VDD														
152	VSS														
153	VSS														
154	DVDD														
155	TODP0														
156	TODN0														
157	DVSS														
158	TODP1														
159	TODN1														
160	DVDD														
161	DVSS														
162	DVSS														
164	CICREFP														
165	CICREFN														
166	DVCC														
167	DVCC														
168	DVSS														
169	VSS														
170	JP0_5 (RDYZ)														
171	JP0_3 (TMS)														
172	JP0_2 (TCK)	FLSCI3SCKI	√	√	√	√	√	√							
175	JP0_1 (TDO)								FLSCI3TXD	√	√	√	√	√	√
176	JP0_0 (TDI)	FLSCI3RXD	√	√	√	√	√	√	FLSCI3TXD	√	√	√	√	√	√
177	JP0_4 (TRSTZ)														
178	EVTOZ														
179	EVTIZ														
182	AUDATA3														

4th Alternative

Superset Ref.Nr.	Port name	In: Function name	In: P1M-C (QFP-144)	In: P1M-C/P1H-C (BGA-156)	In: P1M-C (BGA-292)	In: P1H-C (4MB)	In: P1H-C (8MB)	In: P1H-CE	Out: Function name	Out: P1M-C (QFP-144)	Out: P1M-C/P1H-C (BGA-156)	Out: P1M-C (BGA-292)	Out: P1H-C (4MB)	Out: P1H-C (8MB)	Out: P1H-CE
133	P0_8	CSIH1SCI2	√		√	√	√	√	CSIH1SCO2	√		√	√	√	√
134	P0_9	CSIH1SI2	√		√	√	√	√							
135	FLMD0														
136	CVMOUTZ														
137	E0VSS														
138	E0 VCC														
139	P0_10 (RESETOUTZ)														
140	VDD														
141	VSS														
142	P0_13	MCAN0RX	√		√	√	√	√							
143	P0_14								MCAN0TX	√	√	√	√	√	√
144	MSYNZ														
145	EMU VCC														
146	EMU VSS														
147	AURORES2Z														
148	AURORES1Z														
149	AURORESPDZ														
150	EMU VDD														
151	EMU VDD														
152	VSS														
153	VSS														
154	DVDD														
155	TODP0														
156	TODN0														
157	DVSS														
158	TODP1														
159	TODN1														
160	DVDD														
161	DVSS														
162	DVSS														
164	CICREFP														
165	CICREFN														
166	DVCC														
167	DVCC														
168	DVSS														
169	VSS														
170	JP0_5 (RDYZ)														
171	JP0_3 (TMS)														
172	JP0_2 (TCK)														
175	JP0_1 (TDO)														
176	JP0_0 (TDI)														
177	JP0_4 (TRSTZ)														
178	EVTOZ														
179	EVTIZ														
182	AUDATA3														

Special Function

Superset Ref.Nr.	Port name	Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
133	P0_8							
134	P0_9							
135	FLMD0							
136	CVMOUTZ							
137	E0VSS							
138	E0 VCC							
139	P0_10 (RESETOUTZ)	RESETOUTZ	√	√	√	√	√	√
140	VDD							
141	VSS							
142	P0_13							
143	P0_14	BHPDGREN	√	√	√	√	√	√
144	MSYNZ							√
145	EMU VCC							√
146	EMU VSS							√
147	AURORES2Z							√
148	AURORES1Z							√
149	AURORESPDZ							√
150	EMU VDD							√
151	EMU VDD							√
152	VSS	VSS						√
153	VSS	VSS						√
154	DVDD							√
155	TODP0							√
156	TODN0							√
157	DVSS							√
158	TODP1							√
159	TODN1							√
160	DVDD							√
161	DVSS							√
162	DVSS							√
164	CICREFP							√
165	CICREFN							√
166	DVCC							√
167	DVCC							√
168	DVSS							√
169	VSS	VSS	√	√	√	√	√	√
170	JP0_5 (RDYZ)	RDYZ	√	√	√	√	√	√
171	JP0_3 (TMS)	TMS	√	√	√	√	√	√
172	JP0_2 (TCK)	TCK	√	√	√	√	√	√
175	JP0_1 (TDO)	TDO	√	√	√	√	√	√
176	JP0_0 (TDI)	TDI	√	√	√	√	√	√
177	JP0_4 (TRSTZ)	TRSTZ	√	√	√	√	√	√
178	EVTOZ							√
179	EVTIZ							√
182	AUDATA3							√

Table 2.3 Pin Function assignments (5/6)

Superset Ref.Nr.	Port name	1st Alternative														2nd Alternative														3rd Alternative														4th Alternative														Special Function						
		In							Out							In							Out							In							Out							In							Out													
		Function name	Assignment						Function name	Assignment						Function name	Assignment						Function name	Assignment						Function name	Assignment						Function name	Assignment						Function name	Assignment						Function name	Assignment						Function name	Assignment					
			P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE		P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
183	AUDATA2																																																															√
184	AUDATA1																																																															√
185	AUDATA0																																																															√
186	AUDSYNCZ																																																															√
187	AUDCK																																																															√
188	AUDRSTZ																																																															√
189	RESETZ																																																															
190	VSS																																																															
191	VDD																																																															
192	X2																																																															
193	OSC VSS																																																															
194	OSC VSS																																																															
195	X1																																																															
196	SYS VCC																																																															
197	P1_1	GTM0I1	√	√	√	√	√	√	GTMAT0O5	√	√	√	√	√	√	INTP4	√	√	√	√	√	√	CSIH3CSS0	√	√	√	√	√	√	CSIH1SI1	√	√	√	√	√	√								HSURT0 SDIO0I	√	√	√	√	√	√	HSURT0 SDIO0O	√	√	√	√	√	√							
198	P1_2	GTM0I5	√	√	√	√	√	√	GTMAT0O2	√	√	√	√	√	√	CSIH3SCI0	√	√	√	√	√	√	CSIH3SCO0	√	√	√	√	√	√	CSIH1DCS	√	√	√	√	√	√	CSIH1SO1	√	√	√	√	√	√	HSURT0 SDIO1I	√	√	√	√	√	√	HSURT0 SDIO1O	√	√	√	√	√	√							
199	P1_3	GTM0I4	√	√	√	√	√	√	GTMAT0O3	√	√	√	√	√	√	CSIH3SI0	√	√	√	√	√	√																						HSURT0 SDIO2I	√	√	√	√	√	√	HSURT0 SDIO2O	√	√	√	√	√	√							
200	P1_4	GTM0I0	√	√	√	√	√	√	GTMAT1O3	√	√	√	√	√	√	CSIH3DCS	√	√	√	√	√	√	CSIH3SO0	√	√	√	√	√	√															HSURT0 SDIO3I	√	√	√	√	√	√	HSURT0 SDIO3O	√	√	√	√	√	√							
201	E1 VCC																																																															
202	E1VSS																																																															
203																																																																
204	P1_5	GTM1I6			√	√	√	√	GTMAT2O4				√	√	√								CSIH3CSS1			√	√	√	√																																			
205	P1_6	GTM1I3			√	√	√	√	GTMAT1O4				√	√	√								CSIH3CSS2			√	√	√	√	ESO2Z				√	√	√	CSIH1CSS7			√	√	√	√																					
206	P1_7	GTM1I4			√	√	√	√	GTMAT1O5				√	√	√								CSIH3CSS3			√	√	√	√								CSIH1CSS6			√	√	√	√																					
207	P2_0	GTM0I1	√	√	√	√	√	√	GTMAT0O1N	√	√	√	√	√	√	GTM0I0	√	√	√	√	√	√	CSIH1CSS0	√	√	√	√	√	√	CSIH2SCI0	√	√	√	√	√	√	CSIH2SCO0	√	√	√	√	√	√	HSURT0SCKI	√	√	√	√	√	√	HSURT0 SCKO	√	√	√	√	√	√							
208	P2_1	GTM1I0	√	√	√	√	√	√	GTMAT0O0	√	√	√	√	√	√								CSIH1CSS2	√	√	√	√	√	√	CSIH2DCS	√	√	√	√	√	√	CSIH2SO0	√	√	√	√	√	√	HSURT0CSI	√	√	√	√	√	√	HSURT0CSO	√	√	√	√	√	√							
209	P2_2	GTM0I2	√	√	√	√	√	√	GTMAT0O2N	√	√	√	√	√	√	GTM0I4	√	√	√	√	√	√	CSIH2CSS1	√	√	√	√	√	√	CSIH1SCI1	√	√	√	√	√	√	CSIH1SCO1	√	√	√	√	√	√								HSURT0SDIR	√	√	√	√	√	√							
210	P2_3	GTM1I1	√	√	√	√	√	√	GTMAT0O1	√	√	√	√	√	√	GTM0I5	√	√	√	√	√	√	GTMAT0O5	√	√	√	√	√	√	CSIH2SI0	√	√	√	√	√	√	CSIH0CSS0	√	√	√	√	√	√	HSURT1 SDIO0I	√	√	√	√	√	√	HSURT1 SDIO0O	√	√	√	√	√	√							
211	P2_4	GTM0I3	√	√	√	√	√	√	GTMAT0O3	√	√	√	√	√	√	ESO0Z	√	√	√	√	√	√	CSIH2CSS1	√	√	√	√	√	√	RLIN31RX	√	√	√	√	√	√	SENT0SPCO	√	√	√	√	√	√	HSURT1 SDIO1I	√	√	√	√	√	√	HSURT1 SDIO1O	√	√	√	√	√	√							
212	P2_5	GTM0I6	√	√	√	√	√	√	GTMAT0O2	√	√	√	√	√	√								CSIH2CSS2	√	√	√	√	√	√								RLIN31TX	√	√	√	√	√	√	HSURT1 SDIO2I	√	√	√	√	√	√	HSURT1 SDIO2O	√	√	√	√	√	√							
213	P2_6	GTM1I6	√	√	√	√	√	√	GTMAT0O2	√	√	√	√	√	√	RLIN30RX	√	√	√	√	√	√	CSIH2CSS3	√	√	√	√	√	√	MTTCAN0RX	√	√	√	√	√	√	CSIH1CSS1	√	√	√	√	√	√	HSURT1 SDIO3I	√	√	√	√	√	√	HSURT1 SDIO3O	√	√	√	√	√	√							
214	P2_7	GTM1I2	√	√	√	√	√	√	RLIN30TX	√	√	√	√	√	√	INTP5	√	√	√	√	√	√	CSIH0CSS2	√	√	√	√	√	√								MTTCAN0TX	√	√	√	√	√	√	HSURT1SCKI	√	√	√	√	√	√	HSURT1 SCKO	√	√	√	√	√	√							
215	P2_8	GTM1I1	√	√	√	√	√	√	GTMAT0O1N	√	√	√	√	√	√								CSIH0CSS3	√	√	√	√	√	√								EXTCLK0O	√	√	√	√	√	√	HSURT1CSI	√	√	√	√	√	√	HSURT1CSO	√	√	√	√	√	√							
216	P2_9	GTM1I4	√	√	√	√	√	√	GTMAT0O1N	√	√	√	√	√	√								CSIH0CSS4	√	√	√	√	√	√	RLIN30RX	√	√	√	√	√	√															HSURT1SDIR	√	√	√	√	√	√							
217	P2_10	GTM1I7	√		√	√	√	√	GTMAT1O3	√		√	√	√	√	CSIH2RYI	√		√	√	√	√	CSIH2RYO	√		√	√	√	√								RLIN30TX	√		√	√	√	√								CSIH3CSS3	√		√	√	√	√							
218	P2_11	GTM1I4	√		√	√	√	√	GTMAT1O3	√		√	√	√	√								CSIH2CSS4	√		√	√	√	√	CSIH0SI1	√		√	√	√	√																												
219	P2_12	GTM0I4	√		√	√	√	√	GTMAT1O3N	√		√	√	√	√								CSIH2CSS5	√		√	√	√	√	CSIH0SCI1	√		√	√	√	√	CSIH0SCO1	√		√	√	√	√																					
220	P2_13	GTM1I2	√		√	√	√	√	GTMAT1O1	√		√	√	√	√								CSIH2CSS6	√		√	√	√	√	CSIH0DCS	√		√	√	√	√	CSIH0SO1	√		√	√	√	√																					
221	P2_14	GTM1I4	√		√	√	√	√	GTMAT1O3N	√		√	√	√	√								CSIH2CSS7	√		√	√	√	√								CSIH0CSS0	√		√	√	√	√								CSIH0CSS7	√		√	√	√	√							
222	VSS																																																															
223	VDD																																																															
224	P2_15	GTM1I7	√		√	√	√	√	GTMAT0O3	√		√	√	√	√								EXTCLK0O	√		√	√	√	√																																			
225	P8_15	GTM1I0				√	√	√	GTMAT2O3				√	√	√	ETH1MDI				√	√	√	ETH1MDO				√	√	√	MEMC0D7I				√	√	√	MEMC0D7O				√	√	√																					
226	P8_14	GTM1I5				√	√	√	GTMAT2O2N				√	√	√								ETH1TXER				√	√	√	MEMC0D6I				√	√	√	MEMC0D6O				√	√	√																					
227	P8_13	GTM0I1				√	√	√	GTMAT2O2				√	√	√								ETH1TXD3				√	√	√	MEMC0D5I				√	√	√	MEMC0D5O				√	√	√																					

Table 2.3 Pin Function assignments (6/6)

1st Alternative

Superset Ref.Nr.	Port name	In: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	Out: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
228	P8_12	GTM0I3				√	√	√	GTMAT2O1N				√	√	√
229	P8_11	GTM0I6				√	√	√	GTMAT2O1				√	√	√
230	P8_10	GTM1I7				√	√	√	GTMAT2O0N				√	√	√
231	P8_9	GTM1I3				√	√	√	GTMAT2O0				√	√	√
232	P8_8	GTM0I7				√	√	√	GTMAT1O7				√	√	√
233	P8_7	GTM1I2				√	√	√	GTMAT1O6				√	√	√
234	P8_6	GTM1I5				√	√	√	GTMAT1O5				√	√	√
235	E1VSS														
236	E1 VCC														
237	P8_5	GTM1I4				√	√	√	GTMAT1O4				√	√	√
238	P8_4	GTM0I1				√	√	√	GTMAT2O4				√	√	√
239	P8_3	GTM0I4				√	√	√	GTMAT2O3N				√	√	√
240	P8_2	GTM0I0				√	√	√	GTMAT2O3				√	√	√
241	P8_1	GTM0I2				√	√	√	GTMAT2O2N				√	√	√
242	P8_0	GTM0I5				√	√	√	GTMAT2O2				√	√	√
243	P7_0	GTM0I6			√	√	√	√	GTMAT2O1N				√	√	√
244	P7_1	GTM1I2			√	√	√	√	GTMAT2O1				√	√	√
245	P7_2	GTM0I7			√	√	√	√	GTMAT2O0N				√	√	√
246	P7_3	GTM0I3			√	√	√	√	GTMAT2O0				√	√	√
247	P7_4	GTM1I6			√	√	√	√	GTMAT1O7				√	√	√
248	P7_5	GTM1I7			√	√	√	√	GTMAT1O6				√	√	√
249	P7_6	GTM1I1				√	√	√	GTMAT1O5				√	√	√
250	P7_7	GTM1I0				√	√	√	GTMAT1O4				√	√	√
251	P7_8														
252	P7_9														
253	P3_0	GTM1I2	√	√	√	√	√	√	GTMAT0O6	√	√	√	√	√	√
254	P3_1	GTM0I7	√		√	√	√	√	GTMAT0O7	√		√	√	√	√
255	P3_2	GTM1I0	√		√	√	√	√	GTMAT1O3	√		√	√	√	√
256	P3_3	GTM1I1	√	√	√	√	√	√	GTMAT1O3N	√	√	√	√	√	√
257	P3_4	GTM1I5	√	√	√	√	√	√	GTMAT1O2	√	√	√	√	√	√
258	P3_5	GTM1I5	√	√	√	√	√	√	GTMAT1O2N	√	√	√	√	√	√
259	E1VCC														
260	E1VSS														
261	P3_6	GTM0I6	√	√	√	√	√	√	GTMAT0O3N	√	√	√	√	√	√
262	P3_7	GTM0I4	√	√	√	√	√	√	GTMAT0O4	√	√	√	√	√	√
263	P3_8	GTM1I6	√	√	√	√	√	√	GTMAT0O3N	√	√	√	√	√	√
264	P3_9	GTM0I7	√	√	√	√	√	√	GTMAT1O0	√	√	√	√	√	√
265	P3_10	GTM0I5	√	√	√	√	√	√	GTMAT0O1	√	√	√	√	√	√
266	P3_12	GTM0I4	√	√	√	√	√	√	GTMAT0O0	√	√	√	√	√	√
267	P3_13	GTM0I0	√	√	√	√	√	√	GTMAT0O0	√	√	√	√	√	√
268	VDD														
269	VSS														
270	ERROROUT Z														

2nd Alternative

Superset Ref.Nr.	Port name	In: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	Out: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
228	P8_12								ETH1TXD2				√	√	√
229	P8_11								ETH1TXD1				√	√	√
230	P8_10								ETH1TXEN				√	√	√
231	P8_9								ETH1TXD0				√	√	√
232	P8_8	ETH1REF50CK				√	√	√							
233	P8_7	ETH1TXCLK				√	√	√							
234	P8_6	ETH1RXCLK				√	√	√							
235	E1VSS														
236	E1 VCC														
237	P8_5	ETH1RXD0				√	√	√							
238	P8_4	ETH1RXD1				√	√	√							
239	P8_3	ETH1RXER				√	√	√							
240	P8_2	ETH1CRS				√	√	√	FLXNTUOUT				√	√	√
241	P8_1	ETH1RXD2				√	√	√							
242	P8_0	ETH1RXD3				√	√	√							
243	P7_0														
244	P7_1								FLX1TXENB				√	√	√
245	P7_2	FLX1RXDB				√	√	√							
246	P7_3								FLX1TXDB				√	√	√
247	P7_4														
248	P7_5								FLX1TXDA				√	√	√
249	P7_6								FLX1TXENA				√	√	√
250	P7_7	FLX1RXDA				√	√	√							
251	P7_8								CSIH3CSS1				√	√	√
252	P7_9								CSIH3CSS2				√	√	√
253	P3_0														
254	P3_1	ETH0LINKSTA	√		√	√	√	√							
255	P3_2	RLIN30RX	√		√	√	√	√							
256	P3_3	ETH0MDI	√	√	√	√	√	√	ETH0MDO	√	√	√	√	√	√
257	P3_4								GTMAT0O6	√	√	√	√	√	√
258	P3_5	ETH0COL	√	√	√	√	√	√	GTMAT0O7	√	√	√	√	√	√
259	E1VCC														
260	E1VSS														
261	P3_6								ETH0MDC	√	√	√	√	√	√
262	P3_7	ETH0CRS	√	√	√	√	√	√	RLIN30TX	√	√	√	√	√	√
263	P3_8								ETH0TXER	√	√	√	√	√	√
264	P3_9								ETH0TXD0	√	√	√	√	√	√
265	P3_10								ETH0TXD1	√	√	√	√	√	√
266	P3_12								ETH0TXD2	√	√	√	√	√	√
267	P3_13	ETH0REF50CK	√	√	√	√	√	√	ETH0TXD3	√	√	√	√	√	√
268	VDD														
269	VSS														
270	ERROROUT Z														

3rd Alternative

Superset Ref.Nr.	Port name	In: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	Out: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
228	P8_12	MEMC0D4I				√	√	√	MEMC0D4O				√	√	√
229	P8_11	MEMC0D3I				√	√	√	MEMC0D3O				√	√	√
230	P8_10	MEMC0D2I				√	√	√	MEMC0D2O				√	√	√
231	P8_9	MEMC0D1I				√	√	√	MEMC0D1O				√	√	√
232	P8_8	MEMC0D0I				√	√	√	MEMC0D0O				√	√	√
233	P8_7								MEMC0A8				√	√	√
234	P8_6								MEMC0A7				√	√	√
235	E1VSS														
236	E1 VCC														
237	P8_5								MEMC0A6				√	√	√
238	P8_4								MEMC0A5				√	√	√
239	P8_3								MEMC0A4				√	√	√
240	P8_2								MEMC0A3				√	√	√
241	P8_1								MEMC0A2				√	√	√
242	P8_0	INTP8				√	√	√	MEMC0A1				√	√	√
243	P7_0	SENT7RX				√	√	√	MEMC0A0				√	√	√
244	P7_1	SENT6RX				√	√	√	ETH1MDC				√	√	√
245	P7_2	ETH1COL				√	√	√							
246	P7_3	ETH1LINKSTA				√	√	√							
247	P7_4	ETH1RXDV				√	√	√	CSIH3CSS7			√	√	√	√
248	P7_5								CSIH3CSS6			√	√	√	√
249	P7_6								CSIH3CSS5				√	√	√
250	P7_7	INTP11				√	√	√	CSIH3CSS4				√	√	√
251	P7_8								ETH1WOL				√	√	√
252	P7_9	FLX1STPWT				√	√	√							
253	P3_0								SENT3SPCO	√	√	√	√	√	√
254	P3_1								SENT4SPCO	√		√	√	√	√
255	P3_2	SENT0RX	√		√	√	√	√	CSIH3CSS1	√		√	√	√	√
256	P3_3	SENT1RX	√	√	√	√	√	√	CSIH3CSS2	√	√	√	√	√	√
257	P3_4								CSIH1CSS3	√	√	√	√	√	√
258	P3_5	INTP6	√	√	√	√	√	√							
259	E1VCC														
260	E1VSS														
261	P3_6								CSIH0CSS1	√	√	√	√	√	√
262	P3_7								CSIH0CSS2	√	√	√	√	√	√
263	P3_8	INTP7	√	√	√	√	√	√	CSIH1CSS1	√	√	√	√	√	√
264	P3_9								CSIH1CSS4	√	√	√	√	√	√
265	P3_10								CSIH1CSS5	√	√	√	√	√	√
266	P3_12								CSIH1CSS2	√	√	√	√	√	√
267	P3_13								CSIH1CSS3	√	√	√	√	√	√
268	VDD														
269	VSS														
270	ERROROUT Z														

4th Alternative / Special Function

Superset Ref.Nr.	Port name	In: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	Out: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE	Special Function: Function name	P1M-C (QFP-144)	P1M-C/P1H-C (BGA-156)	P1M-C (BGA-292)	P1H-C (4MB)	P1H-C (8MB)	P1H-CE
228	P8_12								MTTCAN0 RTP				√	√	√							
229	P8_11								MTTCAN0 TMP				√	√	√							
230	P8_10								MTTCAN0 SOC				√	√	√							
231	P8_9	MTTCAN0EVT				√	√	√														
232	P8_8	MTTCAN0 SWT				√	√	√														
233	P8_7																					
234	P8_6																					
235	E1VSS																					
236	E1 VCC																					
237	P8_5																					
238	P8_4																					
239	P8_3	CSIH3SCI2				√	√	√	CSIH3SCO2				√	√	√							
240	P8_2	CSIH3SSIZ				√	√	√	CSIH3CSS0				√	√	√							
241	P8_1	CSIH3SI2				√	√	√														
242	P8_0	CSIH3DCS				√	√	√	CSIH3SO2				√	√	√							
243	P7_0	CSIH3RYI			√	√	√	√	CSIH3RYO			√	√	√	√							
244	P7_1																					
245	P7_2								MEMC0RDZ				√	√	√							
246	P7_3								MEMC0WRZ				√	√	√							
247	P7_4	RLIN32RX				√	√	√														
248	P7_5								RLIN32TX				√	√	√							
249	P7_6								MEMC0CS0Z				√	√	√							
250	P7_7								MEMC0CS1Z				√	√	√							
251	P7_8								MEMC0CS2Z				√	√	√							
252	P7_9								MEMC0CS3Z				√	√	√							
253	P3_0								CSIH0CSS5	√	√	√	√	√	√							
254	P3_1								CSIH0CSS6	√		√	√	√	√							
255	P3_2	FLX0RXDA	√		√	√	√	√														
256	P3_3	FLX0RXDB	√	√	√	√	√	√														
257	P3_4	FLX0STPWT	√	√	√	√	√	√	SENT2SPCO	√	√	√	√	√	√							
258	P3_5								FLX0TXENA	√	√	√	√	√	√							
259	E1VCC																					
260	E1VSS																					
261	P3_6								FLX0TXDB	√	√	√	√	√	√							
262	P3_7								FLX0TXDA	√	√	√	√	√	√							
263	P3_8								FLX0TXENB	√	√	√	√	√	√							
264	P3_9								SENT1SPCO	√	√	√	√	√	√							
265	P3_10																					
266	P3_12	SENT2RX	√	√	√	√	√	√														
267	P3_13	SENT3RX	√	√	√	√	√	√	SENT1SPCO	√	√	√	√	√	√							
268	VDD																					
269	VSS																					
270	ERROROUT Z																					

2.1.4 Pin Function name

Table 2.4 Pin Function Name Definition (1/14)

Line	Function name	I/O	Category	Explanation
1	NMI	I	Pin (NMI)	non maskable interrupt
2	INTP0	I	Pin (INTP)	maskable external interrupt 0
3	INTP1	I		maskable external interrupt 1
4	INTP2	I		maskable external interrupt 2
5	INTP3	I		maskable external interrupt 3
6	INTP4	I		maskable external interrupt 4
7	INTP5	I		maskable external interrupt 5
8	INTP6	I		maskable external interrupt 6
9	INTP7	I		maskable external interrupt 7
10	INTP8	I		maskable external interrupt 8
11	INTP9	I		maskable external interrupt 9
12	INTP10	I		maskable external interrupt 10
13	INTP11	I		maskable external interrupt 11
14	EXTCLK0O	O	System Control	Clock controller output
15	EXTCLK1O	O		Clock controller output
16	CSIH0CSS0	O	CSIH0	CSIH0 serial peripheral chip select signal 0
17	CSIH0CSS1	O		CSIH0 serial peripheral chip select signal 1
18	CSIH0CSS2	O		CSIH0 serial peripheral chip select signal 2
19	CSIH0CSS3	O		CSIH0 serial peripheral chip select signal 3
20	CSIH0CSS4	O		CSIH0 serial peripheral chip select signal 4
21	CSIH0CSS5	O		CSIH0 serial peripheral chip select signal 5
22	CSIH0CSS6	O		CSIH0 serial peripheral chip select signal 6
23	CSIH0CSS7	O		CSIH0 serial peripheral chip select signal 7
24	CSIH0SSIZ	I		CSIH0 serial SS function control input signal
25	CSIH0RYI	I		CSIH0 ready (1) / busy (0) input signal
26	CSIH0RYO	O		CSIH0 ready (1) / busy (0) output signal
27	CSIH0SCIn	I		CSIH0 serial clock input signal n = 0 to 2
28	CSIH0SCOn	O		CSIH0 serial clock output signal n = 0 to 2
29	CSIH0SIn	I		CSIH0 serial data input n = 0 to 2
30	CSIH0SOn	O		CSIH0 serial data output n = 0 to 2
31	CSIH0DCSn	I		CSIH0 data consistency check signal n = 0 to 2
32	CSIH1CSS0	O	CSIH1	CSIH1 serial peripheral chip select signal 0
33	CSIH1CSS1	O		CSIH1 serial peripheral chip select signal 1
34	CSIH1CSS2	O		CSIH1 serial peripheral chip select signal 2
35	CSIH1CSS3	O		CSIH1 serial peripheral chip select signal 3
36	CSIH1CSS4	O		CSIH1 serial peripheral chip select signal 4
37	CSIH1CSS5	O		CSIH1 serial peripheral chip select signal 5
38	CSIH1CSS6	O		CSIH1 serial peripheral chip select signal 6
39	CSIH1CSS7	O		CSIH1 serial peripheral chip select signal 7
40	CSIH1SSIZ	I		CSIH1 serial SS function control input signal
41	CSIH1RYI	I		CSIH1 ready (1) / busy (0) input signal
42	CSIH1RYO	O		CSIH1 ready (1) / busy (0) output signal

Table 2.4 Pin Function Name Definition (2/14)

Line	Function name	I/O	Category	Explanation
43	CSIH1SCIn	I	CSIH1	CSIH1 serial clock input signal n = 0 to 2
44	CSIH1SCOn	O		CSIH1 serial clock output signal n = 0 to 2
45	CSIH1SIn	I		CSIH1 serial data input n = 0 to 2
46	CSIH1SOn	O		CSIH1 serial data output n = 0 to 2
47	CSIH1DCSn	I		CSIH1 data consistency check signal n = 0 to 2
48	CSIH2CSS0	O	CSIH2	CSIH2 serial peripheral chip select signal 0
49	CSIH2CSS1	O		CSIH2 serial peripheral chip select signal 1
50	CSIH2CSS2	O		CSIH2 serial peripheral chip select signal 2
51	CSIH2CSS3	O		CSIH2 serial peripheral chip select signal 3
52	CSIH2CSS4	O		CSIH2 serial peripheral chip select signal 4
53	CSIH2CSS5	O		CSIH2 serial peripheral chip select signal 5
54	CSIH2CSS6	O		CSIH2 serial peripheral chip select signal 6
55	CSIH2CSS7	O		CSIH2 serial peripheral chip select signal 7
56	CSIH2SSIZ	I		CSIH2 serial SS function control input signal
57	CSIH2RYI	I		CSIH2 ready (1) / busy (0) input signal
58	CSIH2RYO	O		CSIH2 ready (1) / busy (0) output signal
59	CSIH2SCIn	I		CSIH2 serial clock input signal n = 0 to 2
60	CSIH2SCOn	O		CSIH2 serial clock output signal n = 0 to 2
61	CSIH2SIn	I		CSIH2 serial data input n = 0 to 2
62	CSIH2SOn	O		CSIH2 serial data output n = 0 to 2
63	CSIH2DCSn	I		CSIH2 data consistency check signal n = 0 to 2
64	CSIH3CSS0	O	CSIH3	CSIH3 serial peripheral chip select signal 0
65	CSIH3CSS1	O		CSIH3 serial peripheral chip select signal 1
66	CSIH3CSS2	O		CSIH3 serial peripheral chip select signal 2
67	CSIH3CSS3	O		CSIH3 serial peripheral chip select signal 3
68	CSIH3CSS4	O		CSIH3 serial peripheral chip select signal 4
69	CSIH3CSS5	O		CSIH3 serial peripheral chip select signal 5
70	CSIH3CSS6	O		CSIH3 serial peripheral chip select signal 6
71	CSIH3CSS7	O		CSIH3 serial peripheral chip select signal 7
72	CSIH3SSIZ	I		CSIH3 serial SS function control input signal
73	CSIH3RYI	I		CSIH3 ready (1) / busy (0) input signal
74	CSIH3RYO	O		CSIH3 ready (1) / busy (0) output signal
75	CSIH3SCIn	I		CSIH3 serial clock input signal n = 0 to 2
76	CSIH3SCOn	O		CSIH3 serial clock output signal n = 0 to 2
77	CSIH3SIn	I		CSIH3 serial data input n = 0 to 2
78	CSIH3SOn	O		CSIH3 serial data output n = 0 to 2
79	CSIH3DCSn	I		CSIH3 data consistency check signal n = 0 to 2
80	RLIN30RX	I	RLIN30	RLIN30 data input
81	RLIN30TX	O		RLIN30 data output
82	RLIN31RX	I	RLIN31	RLIN31 data input
83	RLIN31TX	O		RLIN31 data output
84	RLIN32RX	I	RLIN32	RLIN32 data input
85	RLIN32TX	O		RLIN32 data output

Table 2.4 Pin Function Name Definition (3/14)

Line	Function name	I/O	Category	Explanation
86	RLIN33RX	I	RLIN33	RLIN33 data input
87	RLIN33TX	O		RLIN33 data output
88	HSURT0SDIO0I	I	HSURT0	HSURT0 data input 0
89	HSURT0SDIO0O	O		HSURT0 data output 0
90	HSURT0SDIO1I	I		HSURT0 data input 1
91	HSURT0SDIO1O	O		HSURT0 data output 1
92	HSURT0SDIO2I	I		HSURT0 data input 2
93	HSURT0SDIO2O	O		HSURT0 data output 2
94	HSURT0SDIO3I	I		HSURT0 data input 3
95	HSURT0SDIO3O	O		HSURT0 data output 3
96	HSURT0SCKI	I		HSURT0 serial clock input
97	HSURT0SCKO	O		HSURT0 serial clock output
98	HSURT0SDIR	O		HSURT0 direction indication output
99	HSURT0CSI	I		HSURT0 chip select input
100	HSURT0CSO	O		HSURT0 chip select output
101	HSURT1SDIO0I	I	HSURT1	HSURT1 data input 0
102	HSURT1SDIO0O	O		HSURT1 data output 0
103	HSURT1SDIO1I	I		HSURT1 data input 1
104	HSURT1SDIO1O	O		HSURT1 data output 1
105	HSURT1SDIO2I	I		HSURT1 data input 2
106	HSURT1SDIO2O	O		HSURT1 data output 2
107	HSURT1SDIO3I	I		HSURT1 data input 3
108	HSURT1SDIO3O	O		HSURT1 data output 3
109	HSURT1SCKI	I		HSURT1 serial clock input
110	HSURT1SCKO	O		HSURT1 serial clock output
111	HSURT1SDIR	O		HSURT1 direction indication output
112	HSURT1CSI	I		HSURT1 chip select input
113	HSURT1CSO	O		HSURT1 chip select output
114	HSURT2SDIO0I	I	HSURT2	HSURT2 data input 0
115	HSURT2SDIO0O	O		HSURT2 data output 0
116	HSURT2SDIO1I	I		HSURT2 data input 1
117	HSURT2SDIO1O	O		HSURT2 data output 1
118	HSURT2SDIO2I	I		HSURT2 data input 2
119	HSURT2SDIO2O	O		HSURT2 data output 2
120	HSURT2SDIO3I	I		HSURT2 data input 3
121	HSURT2SDIO3O	O		HSURT2 data output 3
122	HSURT2SCKI	I		HSURT2 serial clock input
123	HSURT2SCKO	O		HSURT2 serial clock output
124	HSURT2SDIR	O		HSURT2 direction indication output
125	HSURT2CSI	I		HSURT2 chip select input
126	HSURT2CSO	O		HSURT2 chip select output

Table 2.4 Pin Function Name Definition (4/14)

Line	Function name	I/O	Category	Explanation
127	HSURT3SDIO0I	I	HSURT3	HSURT3 data input 0
128	HSURT3SDIO0O	O		HSURT3 data output 0
129	HSURT3SDIO1I	I		HSURT3 data input 1
130	HSURT3SDIO1O	O		HSURT3 data output 1
131	HSURT3SDIO2I	I		HSURT3 data input 2
132	HSURT3SDIO2O	O		HSURT3 data output 2
133	HSURT3SDIO3I	I		HSURT3 data input 3
134	HSURT3SDIO3O	O		HSURT3 data output 3
135	HSURT3SCKI	I		HSURT3 serial clock input
136	HSURT3SCKO	O		HSURT3 serial clock output
137	HSURT3SDIR	O		HSURT3 direction indication output
138	HSURT3CSI	I		HSURT3 chip select input
139	HSURT3CSO	O		HSURT3 chip select output
140	MTTCAN0RX	I	MTTCAN0	MTTCAN0 receive data input
141	MTTCAN0TX	O		MTTCAN0 transmit data output
142	MTTCAN0EVT	I		MTTCAN0 event trigger
143	MTTCAN0RTP	O		MTTCAN0 register time mark interrupt pulse
144	MTTCAN0SOC	O		MTTCAN0 start of cycle
145	MTTCAN0SWT	I		MTTCAN0 stop watch trigger
146	MTTCAN0TMP	O		MTTCAN0 trigger time mark interrupt pulse
147	MCAN0RX	I	MCAN0	MCAN0 receive data input
148	MCAN0TX	O		MCAN0 transmit data output
149	MCAN1RX	I	MCAN1	MCAN1 receive data input
150	MCAN1TX	O		MCAN1 transmit data output
151	MCAN2RX	I	MCAN2	MCAN2 receive data input
152	MCAN2TX	O		MCAN2 transmit data output
154	FLXNTUOUT	O	FLX	NTU output
155	FLX0RXDA	I	FLX0	FLX0 channel A receive data input
156	FLX0RXDB	I		FLX0 channel B receive data input
157	FLX0STPWT	I		FLX0 stop watch trigger input
158	FLX0TXDA	O		FLX0 channel A transmit data output
159	FLX0TXDB	O		FLX0 channel B transmit data output
160	FLX0TXENA	O		FLX0 channel A transmit enable
161	FLX0TXENB	O		FLX0 channel B transmit enable
164	FLX1RXDA	I	FLX1	FLX1 channel A receive data input
165	FLX1RXDB	I		FLX1 channel B receive data input
166	FLX1STPWT	I		FLX1 stop watch trigger input
167	FLX1TXDA	O		FLX1 channel A transmit data output
168	FLX1TXDB	O		FLX1 channel B transmit data output
169	FLX1TXENA	O		FLX1 channel A transmit enable
170	FLX1TXENB	O		FLX1 channel B transmit enable
173	SENT0RX	I	SENT0	SENT ch0 sensor data input
174	SENT0SPCO	O		SENT ch0 SPC extension output

Table 2.4 Pin Function Name Definition (5/14)

Line	Function name	I/O	Category	Explanation
175	SENT1RX	I	SENT1	SENT ch1 sensor data input
176	SENT1SPCO	O		SENT ch1 SPC extension output
177	SENT2RX	I	SENT2	SENT ch2 sensor data input
178	SENT2SPCO	O		SENT ch2 SPC extension output
179	SENT3RX	I	SENT3	SENT ch3 sensor data input
180	SENT3SPCO	O		SENT ch3 SPC extension output
181	SENT4RX	I	SENT4	SENT ch4 sensor data input
182	SENT4SPCO	O		SENT ch4 SPC extension output
183	SENT5RX	I	SENT5	SENT ch5 sensor data input
184	SENT5SPCO	O		SENT ch5 SPC extension output
185	SENT6RX	I	SENT6	SENT ch6 sensor data input
186	SENT6SPCO	O		SENT ch6 SPC extension output
187	SENT7RX	I	SENT7	SENT ch7 sensor data input
188	SENT7SPCO	O		SENT ch7 SPC extension output
189	SENT8RX	I	SENT8	SENT ch8 sensor data input
190	SENT8SPCO	O		SENT ch8 SPC extension output
191	SENT9RX	I	SENT9	SENT ch9 sensor data input
192	SENT9SPCO	O		SENT ch9 SPC extension output
193	ETH0COL	I	ETH0	ETH0 Collision detection signal
194	ETH0WOL	O		ETH0 Wake on Lan signal (magic packet detection)
195	ETH0CRS	I		ETH0 Carrier detection signal
196	ETH0MDC	O		ETH0 Serial management interface transfer clock
197	ETH0MDI	I		ETH0 Serial management interface data Input
198	ETH0MDO	O		ETH0 Serial management interface data Output
199	ETH0REF50CK	I		ETH0 RMII reference clock
200	ETH0RXCLK	I		ETH0 Reception clock
201	ETH0RXD0	I		ETH0 Reception data 0
202	ETH0RXD1	I		ETH0 Reception data 1
203	ETH0RXD2	I		ETH0 Reception data 2
204	ETH0RXD3	I		ETH0 Reception data 3
205	ETH0RXDV	I		ETH0 Reception data valid
206	ETH0RXER	I		ETH0 Reception data error
207	ETH0TXCLK	I		ETH0 Transmission clock
208	ETH0TXD0	O	ETH0	ETH0 Transmission data 0
209	ETH0TXD1	O		ETH0 Transmission data 1
210	ETH0TXD2	O		ETH0 Transmission data 2
211	ETH0TXD3	O		ETH0 Transmission data 3
212	ETH0TXEN	O		ETH0 Transmission data enable
213	ETH0TXER	O		ETH0 Transmission data error
214	ETH0LINKSTA	I		ETH0 Link status from PHY

Table 2.4 Pin Function Name Definition (6/14)

Line	Function name	I/O	Category	Explanation
215	ETH1COL	I	ETH1	ETH1 Collision detection signal
216	ETH1WOL	O		ETH1 Wake on Lan signal (magic packet detection)
217	ETH1CRS	I		ETH1 Carrier detection signal
218	ETH1MDC	O		ETH1 Serial management interface transfer clock
219	ETH1MDI	I		ETH1 Serial management interface data Input
220	ETH1MDO	O		ETH1 Serial management interface data Output
221	ETH1REF50CK	I		ETH1 RMII reference clock
222	ETH1RXCLK	I		ETH1 Reception clock
223	ETH1RXD0	I		ETH1 Reception data 0
224	ETH1RXD1	I		ETH1 Reception data 1
225	ETH1RXD2	I		ETH1 Reception data 2
226	ETH1RXD3	I		ETH1 Reception data 3
227	ETH1RXDV	I		ETH1 Reception data valid
228	ETH1RXER	I		ETH1 Reception data error
229	ETH1TXCLK	I		ETH1 Transmission clock
230	ETH1TXD0	O		ETH1 Transmission data 0
231	ETH1TXD1	O		ETH1 Transmission data 1
232	ETH1TXD2	O		ETH1 Transmission data 2
233	ETH1TXD3	O		ETH1 Transmission data 3
234	ETH1TXEN	O		ETH1 Transmission data enable
235	ETH1TXER	O		ETH1 Transmission data error
236	ETH1LINKSTA	I		ETH1 Link status from PHY
237	MEMC0A0	O	External bus	External memory interface address bus bit0
238	MEMC0A1	O		External memory interface address bus bit1
239	MEMC0A2	O		External memory interface address bus bit2
240	MEMC0A3	O		External memory interface address bus bit3
241	MEMC0A4	O		External memory interface address bus bit4
242	MEMC0A5	O		External memory interface address bus bit5
243	MEMC0A6	O		External memory interface address bus bit6
244	MEMC0A7	O		External memory interface address bus bit7
245	MEMC0A8	O		External memory interface address bus bit8
246	MEMC0D0I	I		External memory interface data bus bit0 input
247	MEMC0D1I	I		External memory interface data bus bit1 input
248	MEMC0D2I	I		External memory interface data bus bit2 input
249	MEMC0D3I	I		External memory interface data bus bit3 input
250	MEMC0D4I	I		External memory interface data bus bit4 input
251	MEMC0D5I	I		External memory interface data bus bit5 input

Table 2.4 Pin Function Name Definition (7/14)

Line	Function name	I/O	Category	Explanation
252	MEMC0D6I	I	External bus	External memory interface data bus bit6 input
253	MEMC0D7I	I		External memory interface data bus bit7 input
254	MEMC0D0O	O		External memory interface data bus bit0 output
255	MEMC0D1O	O		External memory interface data bus bit1 output
256	MEMC0D2O	O		External memory interface data bus bit2 output
257	MEMC0D3O	O		External memory interface data bus bit3 output
258	MEMC0D4O	O		External memory interface data bus bit4 output
259	MEMC0D5O	O		External memory interface data bus bit5 output
260	MEMC0D6O	O		External memory interface data bus bit6 output
261	MEMC0D7O	O		External memory interface data bus bit7 output
262	MEMC0CS0Z	O		External memory interface chip select signals CS0
263	MEMC0CS1Z	O		External memory interface chip select signals CS1
264	MEMC0CS2Z	O		External memory interface chip select signals CS2
265	MEMC0CS3Z	O		External memory interface chip select signals CS3
266	MEMC0RDZ	O		External memory interface read strobe
267	MEMC0WRZ	O		External memory interface write strobe
268	ADC0CNV	O	ADC0	ADC0 AD conversion signal
269	ADC0TRG	I		ADC0 AD trigger input
270	ADC0I0	I		ADC0 input channel
271	ADC0I1	I		ADC0 input channel
272	ADC0I2	I		ADC0 input channel
273	ADC0I3	I		ADC0 input channel
274	ADC0I4	I		ADC0 input channel
275	ADC0I5	I		ADC0 input channel
276	ADC0I6	I		ADC0 input channel
277	ADC0I7	I		ADC0 input channel
278	ADC0I8	I		ADC0 input channel
279	ADC0I9	I		ADC0 input channel
280	ADC0I10	I		ADC0 input channel
281	ADC0I11	I		ADC0 input channel
282	ADC0I12	I		ADC0 input channel
283	ADC0I13	I		ADC0 input channel
284	ADC0I14	I		ADC0 input channel
285	ADC0I15	I		ADC0 input channel
286	ADC0I16	I		ADC0 input channel
287	ADC0I17	I		ADC0 input channel
288	ADC0I18	I		ADC0 input channel
289	ADC0I19	I		ADC0 input channel
290	ADC1CNV	O	ADC1	ADC1 AD conversion signal
291	ADC1TRG	I		ADC1 AD trigger input
292	ADC1I0	I		ADC1 input channel
293	ADC1I1	I		ADC1 input channel
294	ADC1I2	I		ADC1 input channel

Table 2.4 Pin Function Name Definition (8/14)

Line	Function name	I/O	Category	Explanation
295	ADC1I3	I	ADC1	ADC1 input channel
296	ADC1I4	I		ADC1 input channel
297	ADC1I5	I		ADC1 input channel
298	ADC1I6	I		ADC1 input channel
299	ADC1I7	I		ADC1 input channel
300	ADC1I8	I		ADC1 input channel
301	ADC1I9	I		ADC1 input channel
302	ADC1I10	I		ADC1 input channel
303	ADC1I11	I		ADC1 input channel
304	ADC1I12	I		ADC1 input channel
305	ADC1I13	I		ADC1 input channel
306	ADC1I14	I		ADC1 input channel
307	ADC1I15	I		ADC1 input channel
308	ADC1I16	I		ADC1 input channel
309	ADC1I17	I		ADC1 input channel
310	ADC1I18	I		ADC1 input channel
311	ADC1I19	I		ADC1 input channel
312	TCK	I	Debug	Debug clock
313	TDI	I		Debug data input
314	TDO	O		Debug data output
315	TMS	I		Debug mode select
316	RDYZ	O		Debug ready
317	TRSTZ	I		Debug reset
318	LPDCLK	I	Debug (LPD-4pin)	Debug clock for Low-pin count debug
319	LPDI	I		Debug data input for Low-pin count debug
320	LPDO	O		Debug data output for Low-pin count debug
321	LPDCLKOUT	O		Debug clock output for Low-pin count debug
322	LPDRSTZ	I		Debug reset for Low-pin count debug
323	EVTOZ	O	Nexus	Debug I/F event output signal
324	EVTIZ	I		Debug I/F event input signal
325	FLSCI3TXD	O	Flash Writer I/F	Flash Writer I/F TxD
326	FLSCI3RXD	I		Flash Writer I/F RxD
327	FLSCI3SCKI	I		Flash Writer I/F SCK
328	AUDRSTZ	I	AUDR	AUDR reset signal
329	AUDCK	I		AUDR clock signal
330	AUDSYNCZ	I		AUDR synchronous signal
331	AUDATA0	I/O		AUDR data signal
332	AUDATA1	I/O		AUDR data signal
333	AUDATA2	I/O		AUDR data signal
334	AUDATA3	I/O		AUDR data signal

Table 2.4 Pin Function Name Definition (9/14)

Line	Function name	I/O	Category	Explanation
335	CICREFP	I	Trace I/F	Trace I/F clock pos
336	CICREFN	I		Trace I/F clock neg
337	TODP0	O		Trace I/F data pos 0
338	TODN0	O		Trace I/F data neg 0
339	TODP1	O		Trace I/F data pos 1
340	TODN1	O		Trace I/F data neg 1
341	MSYNZ	I		Trace I/F Synchronization request
342	AURORES1Z	I		Aurora Domain Reset signal
343	AURORES2Z	I		Aurora domain signal Isolation
344	AURORESPDZ	I		Core domain Aurora signal Isolation
345	ERAMRESPDZ	I		Core domain ERAM signal Isolation
346	ERAMRES2Z	I		ERAM domain core signal Isolation
347	GTM0I0	I	GTM TIM	GTM TIM 0 input 0
348	GTM0I1	I		GTM TIM 0 input 1
349	GTM0I2	I		GTM TIM 0 input 2
350	GTM0I3	I		GTM TIM 0 input 3
351	GTM0I4	I		GTM TIM 0 input 4
352	GTM0I5	I		GTM TIM 0 input 5
353	GTM0I6	I		GTM TIM 0 input 6
354	GTM0I7	I		GTM TIM 0 input 7
355	GTM1I0	I		GTM TIM 1 input 0
356	GTM1I1	I		GTM TIM 1 input 1
357	GTM1I2	I		GTM TIM 1 input 2
358	GTM1I3	I		GTM TIM 1 input 3
359	GTM1I4	I		GTM TIM 1 input 4
360	GTM1I5	I		GTM TIM 1 input 5
361	GTM1I6	I		GTM TIM 1 input 6
362	GTM1I7	I		GTM TIM 1 input 7
363	GTMAT0O0	O	ATOM	GTM ATOM 0 output 0
364	GTMAT0O1	O		GTM ATOM 0 output 1
365	GTMAT0O2	O		GTM ATOM 0 output 2
366	GTMAT0O3	O		GTM ATOM 0 output 3
367	GTMAT0O4	O		GTM ATOM 0 output 4
368	GTMAT0O5	O		GTM ATOM 0 output 5
369	GTMAT0O6	O		GTM ATOM 0 output 6
370	GTMAT0O7	O		GTM ATOM 0 output 7
371	GTMAT1O0	O		GTM ATOM 1 output 0
372	GTMAT1O1	O		GTM ATOM 1 output 1
373	GTMAT1O2	O		GTM ATOM 1 output 2
374	GTMAT1O3	O		GTM ATOM 1 output 3
375	GTMAT1O4	O		GTM ATOM 1 output 4
376	GTMAT1O5	O		GTM ATOM 1 output 5
377	GTMAT1O6	O		GTM ATOM 1 output 6
378	GTMAT1O7	O		GTM ATOM 1 output 7

Table 2.4 Pin Function Name Definition (10/14)

Line	Function name	I/O	Category	Explanation
379	GTMAT2O0	O	ATOM	GTM ATOM 2 output 0
380	GTMAT2O1	O		GTM ATOM 2 output 1
381	GTMAT2O2	O		GTM ATOM 2 output 2
382	GTMAT2O3	O		GTM ATOM 2 output 3
383	GTMAT2O4	O		GTM ATOM 2 output 4
384	GTMAT0O0N	O	DTM	GTM ATOM 0 output 0 neg
385	GTMAT0O1N	O		GTM ATOM 0 output 1 neg
386	GTMAT0O2N	O		GTM ATOM 0 output 2 neg
387	GTMAT0O3N	O		GTM ATOM 0 output 3 neg
388	GTMAT1O0N	O		GTM ATOM 1 output 0 neg
389	GTMAT1O1N	O		GTM ATOM 1 output 1 neg
390	GTMAT1O2N	O		GTM ATOM 1 output 2 neg
391	GTMAT1O3N	O		GTM ATOM 1 output 3 neg
392	GTMAT2O0N	O		GTM ATOM 2 output 0 neg
393	GTMAT2O1N	O		GTM ATOM 2 output 1 neg
394	GTMAT2O2N	O		GTM ATOM 2 output 2 neg
395	GTMAT2O3N	O		GTM ATOM 2 output 3 neg
396	ESO0Z	I	GTM Hi-Z control	Emergency shut-off 0
397	ESO1Z	I		Emergency shut-off 1
398	ESO2Z	I		Emergency shut-off 2
399	ICUMGPIO0	O	ICUMC	ICUMC GPIO control 0
400	ICUMGPIO1	O		ICUMC GPIO control 1
401	BHPDGRCLK0	O	BHP	Degrading clock output for MCAN
402	BHPDGRCLK1	O		Degrading clock output for FlexRay
403	BHPDGREN	I		Degrading allowed pin
404	ERROROUTZ	O	ECM	Error output signal
405	CVMOUTZ	O	System Control	CVM internal voltage error detection output signal
406	FLMD0	I		Operating mode select pin
407	FLMD1	I		Operating mode select pin
408	MODE0	I		Operating mode select pin
409	MODE1	I		Operating mode select pin
410	RESETZ	I		Reset input
411	RESETOUTZ	O		Reset output
412	X1	I		Main oscillator resonator connections
413	X2	O		Main oscillator resonator connections
414	JP0_0	I/O	JP0	JTAG Port group 0 port0
415	JP0_1	I/O		JTAG Port group 0 port1
416	JP0_2	I/O		JTAG Port group 0 port2
417	JP0_3	I/O		JTAG Port group 0 port3
418	JP0_4	I		JTAG Port group 0 port4
419	JP0_5	I/O		JTAG Port group 0 port5

Table 2.4 Pin Function Name Definition (11/14)

Line	Function name	I/O	Category	Explanation
420	P0_0	I/O	P0	Port group 0 port0
421	P0_1	I/O		Port group 0 port1
422	P0_2	I/O		Port group 0 port2
423	P0_3	I/O		Port group 0 port3
424	P0_4	I/O		Port group 0 port4
425	P0_5	I/O		Port group 0 port5
426	P0_6	I/O		Port group 0 port6
427	P0_7	I/O		Port group 0 port7
428	P0_8	I/O		Port group 0 port8
429	P0_9	I/O		Port group 0 port9
430	P0_10	I/O		Port group 0 port10
431	P0_13	I/O		Port group 0 port13
432	P0_14	I/O		Port group 0 port14
433	P1_1	I/O	P1	Port group 1 port1
434	P1_2	I/O		Port group 1 port2
435	P1_3	I/O		Port group 1 port3
436	P1_4	I/O		Port group 1 port4
437	P1_5	I/O		Port group 1 port5
438	P1_6	I/O		Port group 1 port6
439	P1_7	I/O		Port group 1 port7
440	P2_0	I/O	P2	Port group 2 port0
441	P2_1	I/O		Port group 2 port1
442	P2_2	I/O		Port group 2 port2
443	P2_3	I/O		Port group 2 port3
444	P2_4	I/O		Port group 2 port4
445	P2_5	I/O		Port group 2 port5
446	P2_6	I/O		Port group 2 port6
447	P2_7	I/O		Port group 2 port7
448	P2_8	I/O		Port group 2 port8
449	P2_9	I/O		Port group 2 port9
450	P2_10	I/O		Port group 2 port10
451	P2_11	I/O		Port group 2 port11
452	P2_12	I/O		Port group 2 port12
453	P2_13	I/O		Port group 2 port13
454	P2_14	I/O		Port group 2 port14
455	P2_15	I/O		Port group 2 port15
456	P3_0	I/O	P3	Port group 3 port0
457	P3_1	I/O		Port group 3 port1
458	P3_2	I/O		Port group 3 port2
459	P3_3	I/O		Port group 3 port3
460	P3_4	I/O		Port group 3 port4
461	P3_5	I/O		Port group 3 port5
462	P3_6	I/O		Port group 3 port6
463	P3_7	I/O		Port group 3 port7

Table 2.4 Pin Function Name Definition (12/14)

Line	Function name	I/O	Category	Explanation
464	P3_8	I/O	P3	Port group 3 port8
465	P3_9	I/O		Port group 3 port9
466	P3_10	I/O		Port group 3 port10
467	P3_11	I/O		Port group 3 port11
468	P3_12	I/O		Port group 3 port12
469	P3_13	I/O		Port group 3 port13
470	P3_14	I/O		Port group 3 port14
471	P4_0	I/O	P4	Port group 4 port0
472	P4_1	I/O		Port group 4 port1
473	P4_2	I/O		Port group 4 port2
474	P4_3	I/O		Port group 4 port3
475	P4_4	I/O		Port group 4 port4
476	P4_5	I/O		Port group 4 port5
477	P4_6	I/O		Port group 4 port6
478	P4_7	I/O		Port group 4 port7
479	P4_8	I/O		Port group 4 port8
480	P4_9	I/O		Port group 4 port9
481	P4_10	I/O		Port group 4 port10
482	P4_11	I/O		Port group 4 port11
483	P4_12	I/O		Port group 4 port12
484	P4_13	I/O		Port group 4 port13
485	P4_14	I/O		Port group 4 port14
486	P5_0	I/O	P5	Port group 5 port0
487	P5_1	I/O		Port group 5 port1
488	P5_4	I/O		Port group 5 port4
489	P5_5	I/O		Port group 5 port5
490	P5_6	I/O		Port group 5 port6
491	P5_7	I/O		Port group 5 port7
492	P5_8	I/O		Port group 5 port8
493	P5_9	I/O		Port group 5 port9
494	P5_10	I/O		Port group 5 port10
495	P5_11	I/O		Port group 5 port11
496	P5_12	I/O		Port group 5 port12
497	P5_13	I/O		Port group 5 port13
498	P5_14	I/O		Port group 5 port14
499	P5_15	I/O		Port group 5 port15
500	P6_0	I/O	P6	Port group 6 port0
501	P6_1	I/O		Port group 6 port1
502	P6_2	I/O		Port group 6 port2
503	P6_3	I/O		Port group 6 port3
504	P6_4	I/O		Port group 6 port4
505	P6_5	I/O		Port group 6 port5
506	P6_6	I/O		Port group 6 port6
507	P6_7	I/O		Port group 6 port7

Table 2.4 Pin Function Name Definition (13/14)

Line	Function name	I/O	Category	Explanation
508	P6_8	I/O	P6	Port group 6 port8
509	P6_9	I/O		Port group 6 port9
510	P6_10	I/O		Port group 6 port10
511	P6_11	I/O		Port group 6 port11
512	P6_12	I/O		Port group 6 port12
513	P6_13	I/O		Port group 6 port13
514	P6_14	I/O		Port group 6 port14
515	P6_15	I/O		Port group 6 port15
516	P7_0	I/O	P7	Port group 7 port0
517	P7_1	I/O		Port group 7 port1
518	P7_2	I/O		Port group 7 port2
519	P7_3	I/O		Port group 7 port3
520	P7_4	I/O		Port group 7 port4
521	P7_5	I/O		Port group 7 port5
522	P7_6	I/O		Port group 7 port6
523	P7_7	I/O		Port group 7 port7
524	P7_8	I/O		Port group 7 port8
525	P7_9	I/O		Port group 7 port9
526	P8_0	I/O	P8	Port group 8 port0
527	P8_1	I/O		Port group 8 port1
528	P8_2	I/O		Port group 8 port2
529	P8_3	I/O		Port group 8 port3
530	P8_4	I/O		Port group 8 port4
531	P8_5	I/O		Port group 8 port5
532	P8_6	I/O		Port group 8 port6
533	P8_7	I/O		Port group 8 port7
534	P8_8	I/O		Port group 8 port8
535	P8_9	I/O		Port group 8 port9
536	P8_10	I/O		Port group 8 port10
537	P8_11	I/O		Port group 8 port11
538	P8_12	I/O		Port group 8 port12
539	P8_13	I/O		Port group 8 port13
540	P8_14	I/O		Port group 8 port14
541	P8_15	I/O		Port group 8 port15
542	P9_0	I/O	P9	Port group 9 port0
543	P9_1	I/O		Port group 9 port1
544	P9_2	I/O		Port group 9 port2
545	P9_3	I/O		Port group 9 port3
546	P9_4	I/O		Port group 9 port4
547	P9_5	I/O		Port group 9 port5
548	P9_6	I/O		Port group 9 port6
549	P9_7	I/O		Port group 9 port7
550	P9_8	I/O		Port group 9 port8

Table 2.4 Pin Function Name Definition (14/14)

Line	Function name	I/O	Category	Explanation
551	EnVCC	power	IO_Power	IO supply voltage n = 0, 1
552	EnVSS	power		IO ground n = 0, 1
553	VCC	power	Internal Regulator	Regulator supply voltage
554	VDD	power	Core_Power	Core supply voltage
555	VSS	power	Core_Ground	Core ground
556	DVCC	power	Trace_IF_Power	Aurora I/F supply voltage (Analog)
557	DVDD	power		Aurora I/F supply voltage (Digital)
558	DVSS	power		Aurora I/F ground
559	AnVCC	power	ADC	ADC supply voltage n = 0, 1
560	AnVSS	power		ADC ground n = 0, 1
561	AnVREFH	power		ADC reference voltage plus n = 0, 1
562	EMUVCC	power	EMU	Aurora control IO supply voltage
563	EMUVDD	power		Aurora control core supply voltage
564	EMUVSS	power		Aurora control ground
565	SYSVCC	power	System	System control supply voltage
566	OSCVSS	power	OSC	OSC ground
567	ERAMVDD	power	ERAM Control	ERAM core supply voltage
568	ERAMnVCC	power		ERAM IO supply voltage n = 0, 1
569	ERAMnVSS	power		ERAM ground n = 0, 1

Section 3 Electrical Specifications

3.1 Overview

The specifications in this section are for devices operating under the following conditions. Where a special condition is required for a given specification, the condition will be indicated. Furthermore, the specifications in this section are not guaranteed unless the conditions listed below are met.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are shown in the table below.

Conditions:

- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Voltage	VDD		–0.3		1.8	V
	VCC		–0.3		6.5	V
	SYSVCC		–0.3		6.5	V
	E0VCC		–0.3		6.5	V
	E1VCC		–0.3		6.5	V
	A0VCC		–0.3		6.5	V
	A1VCC		–0.3		6.5	V
	DVCC	Emulation Device Only	–0.3		4.5	V*1
	DVDD		–0.3		1.8	V*1
	EMUVCC		–0.3		4.5	V*1
	EMUVDD		–0.3		1.8	V*1
	ERAM0VCC		–0.3		4.5	V*1
	ERAM1VCC		–0.3		4.5	V*1
	ERAMVDD		–0.3		1.8	V*1
Input Voltage	VI	E0VCC pin*4	–0.3		E0VCC+0.3	V*2
		E1VCC pin*5	–0.3		E1VCC+0.3	V*2
		RESETZ X1 pins	–0.3		SYSVCC+0.3	V*2
		ERAMRES2Z pin	–0.3		ERAM1VCC+0.3	V*1,*2
		AURORES1Z AURORES2Z pins	–0.3		EMUVCC+0.3	V*1,*2
		CICREFN CICREFP pins	–0.3		DVDD+0.3	V*1,*2
		AUDR I/F, EVTIZ pins	–0.3		E1VCC+0.3	V*1,*2
		ERAMRESPDZ pin	–0.3		E1VCC+0.3	V*1,*2
		AURORESPDZ, MSYNZ pins	–0.3		E0VCC+0.3	V*1,*2
Analogue reference voltage	A0VREFH		–0.3		A0VCC +0.3	V*2
	A1VREFH		–0.3		A1VCC +0.3	V*2

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analogue input voltage	VIAN	A0VCC pins	–0.3		A0VCC +0.3	V*2
		A1VCC pins	–0.3		A1VCC +0.3	V*2
Output low current *3	I_{OL1p}	per pin			10	mA
	I_{OLall}	Sum of all output low currents of all EnVCC/AnVCC pins			200	mA
Output high current *3	I_{OH1p}	per pin			–10	mA
	I_{OHall}	Sum of all output high currents of all EnVCC/AnVCC pins			–200	mA
JunctionTemperature	Tj	BGA Package	–40		150	°C
		QFP Package	–40		160	
Storage Temperature	Tstg	BGA Package	–55		150	°C
		QFP Package	–55		160	

Note 1. Emulation Device only

Note 2. Input voltage of CICREFN and CICREFP must not exceed 1.8V, and Input voltage of other pins must not exceed 6.5V (4.5V in case of P1H-CE device).

Note 3. Given specification includes injected currents. For injected current refer to **Section 3.4.6**.

Note 4. P0, P3_11, P5, P6_2-15, P9, JP0*6, FLMD0, CVMOUTZ

Note 5. P1, P2, P3_0-10, P3_12-14, P4, P6_0-1, P7, P8, ERROROUTZ

Note 6. For P1H-CE device the JP0 is connected to E1VCC

CAUTION

- **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
- **Input voltage, analog reference voltage and analog input voltage must not exceed 6.5 V**
- **Even in case when input voltage does not meet the specified characteristics, it is accepted if the injected current characteristics specified in Section 3.4.6 are met.**
- **The device's function is not guaranteed outside of the condition Section 3.3 General Characteristics.**

3.3 General Characteristics

3.3.1 Supply Voltage Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.1 Supply Voltage Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Core supply voltage (DPS)	VDD	DPS = dual power supply (VDD from external)	1.20	1.25	1.35	V*4
Regulator supply voltage	VCC		V_{POC}*3		3.6	V
System control supply voltage	SYSVCC	*1, *2	V_{POC}*3		3.6	V
IO supply voltage	EnVCC		V_{POC}*3		3.6	V
ADC supply voltage	AnVCC		V_{POC}*3		3.6	V
ADC reference voltage supply	AnVREFH		V_{POC}*3		3.6	V
Aurora I/F supply voltage (Analog)	DVCC	Emulation devices only	V_{POC}*3		3.6	V
Aurora I/F supply voltage (Digital)	DVDD		1.175	1.25	1.325	V
ERAM IO supply voltage	ERAM1VCC		V_{POC}*3		3.6	V
ERAM core supply voltage	ERAMVDD		1.20	1.25	1.35	V
Aurora control IO supply voltage	EMUVCC		V_{POC}*3		3.6	V
Aurora control core supply voltage	EMUVDD		1.175	1.25	1.325	V
VDD slew rate @power-up	VDDsru				500	V/ms
VCC slew rate @power-up	VCCsru				500	V/ms
SYSVCC slew rate @power-up	SYSVCCsru				500	V/ms
EnVCC slew rate @power-up	EnVCCsru				500	V/ms
AnVCC slew rate @power-up	AnVCCsru				500	V/ms
AnVREFH slew rate @power-up	AnVRFHsru				500	V/ms

Note 1. The device will operate as normal above the transistor threshold voltage level. Above this threshold level the device will operate or it is controlled by RESET/POC — depending on CVM.

Note 2. SYSVCC is monitored by POC, see chapter POC Characteristics.

Note 3. Specification value "V_{POC}" means: supply voltage higher than POC threshold value V_{POC} or higher or equal to 3.0V. For V_{POC} specification please refer to **Section 3.7.1, POC Characteristics**.

Note 4. During RESET condition an enlarged VDD up to 1.55V is accepted for a maximum time of 150s over lifetime.

3.3.2 Main Oscillator Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.2 Main Oscillator Characteristics

Item	Symbol	Comment	Condition	MIN.	TYP.	MAX.	Unit
Frequency	f_{MOSC} *1*2	Crystal		16 –1%		24 + 1%	MHz
Stabilization time	t_{MOST}			3*5			ms
Internal Capacitor size selectable by CAP_SEL setting (OPBT setting)*4	Ccapsel	CAP_SEL [2:0]	=000b		0		pF
			=001b		1		pF
			=010b		3		pF
			=011b		4		pF
			=100b		5		pF
			=101b (default)		6		pF
			=110b		8		pF
			=111b		9		pF
Internal damping register size selectable by RDSEL setting (OPBT setting)	Rrdsel	RDSEL [2:0]	=000b		846		Ω
			=100b		632		Ω
			=x10b		265		Ω
			=xx1b		18		Ω

Note 1. To reach internal usable clocks only following 3 fMOSC frequencies are supported: 16MHz, 20MHz and 24MHz. Tolerance of external quartz crystal is assumed as +/–1%.

Note 2. The StartUp is supported without external components under following conditions:
- Default values for drivability and capacitance are defined as follows
  - — Maximum drivability (AMPSEL = 00b)
  - — Default damping resistor configuration (RDSEL = 100b)
  - — Default internal capacitance of 6pF (CAPSEL = 011b)
- Specification covers a maximum external stray capacitance of up to 6pF to each pin X1 and X2.
- After StartUp drivability and capacitance will be configured by OPBT
- A possible exceeding of the recommended maximum drive level for a crystal for all start-up phases has to be agreed with the crystal manufacturers separately.

Note 3. Depends on characteristics of selected crystal

Note 4. The CAP_SEL capacity values refer to the selectable internal device capacitances. The effective capacitance will be 1-4pF higher due to parasitic capacitances.

Note 5. Depends on characteristics of selected crystal. External reset must not be released, before oscillation becomes stable.

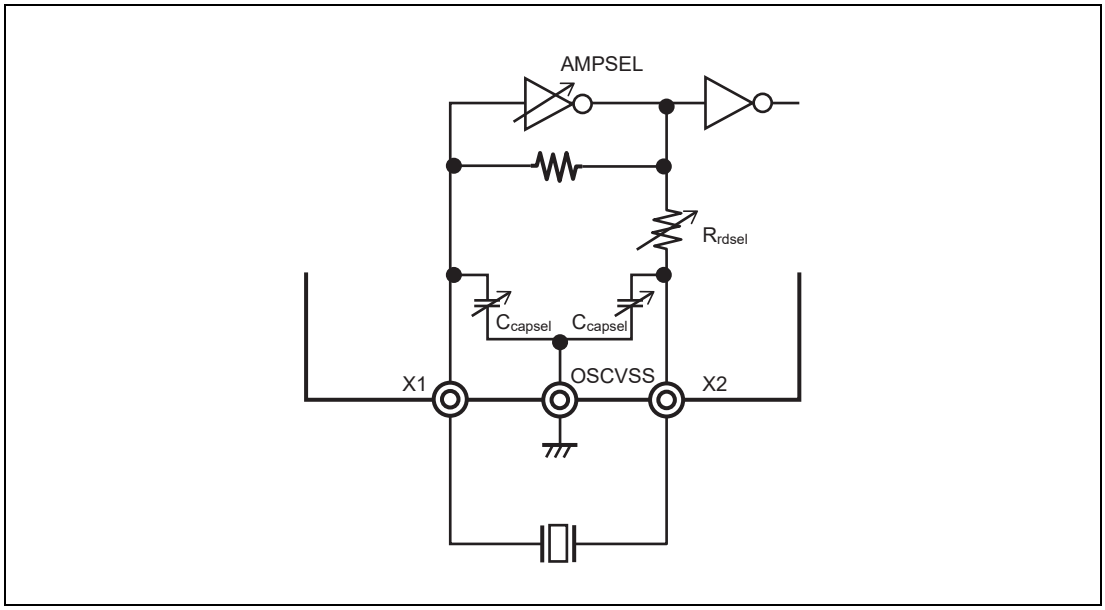


Figure 3.1 Oscillator Circuit Diagram and Connection Example of Crystal Resonator

NOTE

Figure 3.1 shows how to connect a crystal oscillator. For crystal oscillator that are tested and recommended by Renesas (inquire separately) any external components such as a load capacitor and a dumping resistor are not necessarily required for oscillation in general. However, proper operation should be verified under actual conditions prior to use including internal setting of AMPSEL, Ccapsel and Rrdsel.

3.3.3 PLL0 Characteristics

CAUTIONS

1. **PLL0 uses output of main (crystal) oscillator as input clock.**
2. **Below specification is based on the condition of an ideal clock input.**

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.3 PLL0 Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL output period jitter	t_{PJ}		–200		+200	ps
PLL output long term jitter	t_{LTJ}	term = 1 µs	–500		+500	ps

Note 1. Input clock: main oscillator. Condition: Ideal clock input.

3.3.4 Internal Oscillator Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.4 Internal Oscillator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Frequency	f_{RH1}	accuracy after trimming: +/–10%	14.4	16.0	17.6	MHz

3.3.5 Operational Condition

Conditions:

- Temperature range: Tjmin to Tjmax.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.5 Operational Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU operating clock frequency*1	f_{CPUCLK}				240	MHz
Junction temperature*2	T_j	For devices P1M-C (LQFP)	–40		160*4	°C
		For devices P1M-C (BGA-292)	–40		150*4	°C
		For devices P1M-C (BGA-156)	–40		150*4	°C
		For devices P1H-C (4MB)	–40		150*4	°C
		For devices P1H-C (8MB)	–40		150*4	°C
		For devices P1H-CE	–40		150*4	°C
Absolute DC output current per power supply pin	I_{O1s}	*3			70	mA
Ext. pull-down resistor for FLMD0	RPDMD0	*5	95			kΩ
		*6	0		750	Ω

Note 1. Please refer also to RH850/P1x-C Group User's Manual: Hardware **Section 3, CPU System** and RH850/P1x-C Group User's Manual: Hardware **Section 12, Clock Controller**.

Note 2. Details of thermal characteristics are described in **Section 3.8, Thermal Characteristics**.

Note 3. 1. Absolute value of the sum of DC output high and low currents of one EnVCC/AnVCC pin.
2. Regarding AC output currents, simultaneous switching of [max.] 8 output pins is allowed under the condition that the average current over lifetime does not exceed the limit given above for Item.

Note 4. In case of hotspots local Tj might exceeded. The function of the device is still ensured by test margin and library spec.

Note 5. An ext. pull-down resistor connected to FLMD0 pin is recommended in case flash programming will be used.

Note 6. A low resistance connection of FLMD0 pin to EnVSS prohibits any flash programming.

NOTES

1. If not otherwise stated, defines the valid condition for the specification values within this document.
2. The maximum frequency of a peripheral function is depending on the setting of the according clock domain in which the peripheral function resides. Please refer to RH850/P1x-C Group User's Manual: Hardware **Section 12, Clock Controller**.

3.3.6 IO Capacitances

Conditions:

- Temperature range: Tjmin to Tjmax.

Table 3.6 I/O Capacitances*1*2

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I*3	f = 1 MHz 0 V for non measurement pins			10	pF
Input/output capacitance	C_{IO}*4				10	pF
Output capacitance	C_O*5				10	pF
Input capacitance X1	C_{X1}	Main OSC. EXCLK mode, CAP_SEL = 010			10	pF

Note 1. Please note that for pins of the main oscillator the capacitance value given above are exceeded
Note 2. For analog input pins (ADCnIm) please refer to the **Section 3.7.3, A/D Converter Characteristics**
Note 3. C_I: capacitance of between the input pin and ground
Note 4. C_{IO}: capacitance of between the input/output pin and ground
Note 5. C_O: capacitance of between the output pin and ground

3.4 DC Characteristics

3.4.1 Input Leakage Current

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.7 Input Leakage Current

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1} *1	Digital I/O pins, VI = 0 to EnVCC			1.0	µA
Input leakage current, low	I_{LIL1} *1	Digital I/O pins, VI = 0 to EnVCC			–1.0	µA
Input leakage current, high	I_{LIH2}	RESETZ, VI = 0 to SYSVCC			1.0	µA
Input leakage current, low	I_{LIL2}	RESETZ, VI = 0 to SYSVCC			–1.0	µA
Input leakage current, high	I_{LIH3} *2	Analog input pins (ADCnlm), VIAN = 0 to AnVCC			0.15	µA
					1.0	µA
Input leakage current, low	I_{LIL3} *2	Analog input pins (ADCnlm), VIAN = 0 to AnVCC			–0.15	µA
					–1.0	µA
Input leakage current, high	I_{LIH4} *3	AUDR I/F, VIAU = 0 to EnVCC			5.0	µA
Input leakage current, low	I_{LIL4} *3	AUDR I/F, VIAU = 0 to EnVCC			–25.0	µA
Input leakage current, high	I_{LIH5} *1	ERAMRES2Z, VI = 0 to ERAM1VCC			1.0	µA
Input leakage current, low	I_{LIL5} *1	ERAMRES2Z, VI = 0 to ERAM1VCC			–1.0	µA
Input leakage current, high	I_{LIH6} *1	AURORESnZ, VI = 0 to EMUVCC			1.0	µA
Input leakage current, low	I_{LIL6} *1	AURORESnZ, VI = 0 to EMUVCC			–1.0	µA

Note 1. Pull-up/pull-down current sources/sinks are switched off.

Note 2. Leakage current under the condition that ADC conversion of the according analog input pin is switched off. When switched on, 1.0µA for high and -1.0µA for low. Both do not include charging current of the conversion sample circuits. Charging current can be judged with the equivalent input circuit and sampling time specified in **Section 3.7.3, A/D Converter Characteristics**.

Note 3. Emulation devices only

NOTE

For Aurora I/F there is no leakage current specification, because it is based on AC coupling only.

3.4.2 Digital IO Pins Input and Output Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.8 Digital IO Pins: Input and Output Characteristics (1/4)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH11}	CMOS, EnVCC = 3.0 to 3.6 V (Emulation devices only)	0.65 × EnVCC		EnVCC + 0.3	V
	V_{IH12}	SHMT1, EnVCC = 3.0 to 3.6 V	0.65 × EnVCC		EnVCC + 0.3	V
	V_{IH13}	SHMT2, EnVCC = 3.0 to 3.6 V	0.75 × EnVCC		EnVCC + 0.3	V
	V_{IH14}	SHMT4, EnVCC = 3.0 to 3.6 V	0.80 × EnVCC		EnVCC + 0.3	V
Low level input voltage	V_{IL11}	CMOS, EnVCC = 3.0 to 3.6 V (Emulation devices only)	–0.3		0.35 × EnVCC	V
	V_{IL12}	SHMT1, EnVCC = 3.0 to 3.6 V	–0.3		0.35 × EnVCC	V
	V_{IL13}	SHMT2, EnVCC = 3.0 to 3.6 V	–0.3		0.25 × EnVCC	V
	V_{IL14}	SHMT4, EnVCC = 3.0 to 3.6 V	–0.3		0.50 × EnVCC	V
Input hysteresis for Schmitt	V_{H11}	SHMT1, EnVCC = 3.0 to 3.6 V	0.3			V
	V_{H12}	SHMT2, EnVCC = 3.0 to 3.6 V	0.2 × EnVCC			V
	V_{H13}	SHMT4, EnVCC = 3.0 to 3.6 V	0.1			V
Input pull-up current source *2	I_{PU11}	EnVCC = 3.0 to 3.6 V, VI = EVSS*7	–150		–30	µA
		EnVCC = 3.3V, VI = EVSS*7, T_J = –40°C		–100		µA
		EnVCC = 3.3V, VI = EVSS*7, T_J = 25°C		–80		µA
		EnVCC = 3.3V, VI = EVSS*7, T_J = 150°C		–60		µA
Input pull-down current source*3	I_{PD11}	EnVCC = 3.0 to 3.6 V, VI = EnVCC*7	30		150	µA
		EnVCC = 3.3V, VI = EnVCC*7, T_J = –40°C		100		µA
		EnVCC = 3.3V, VI = EnVCC*7, T_J = 25°C		80		µA
		EnVCC = 3.3V, VI = EnVCC*7, T_J = 150°C		60		µA
Output resistance of GPIO buffer*6*8	R_{O11}	Drive strength 1, EnVCC = 3.0 to 3.6 V Forcing 0.4 V to 4 pins simultaneously or Forcing EnVCC – 0.4 V to 4 pins simultaneously	15	50	110	Ω
	R_{O12}	Drive strength 2, EnVCC = 3.0 to 3.6 V Forcing 0.4 V to 8pins simultaneously or Forcing EnVCC – 0.4 V to 8 pins simultaneously	30	100	220	Ω
	R_{O13}	Drive strength 3, EnVCC = 3.0 to 3.6 V Forcing 0.4 V to 16 pins simultaneously or Forcing EnVCC – 0.4 V to 16 pins simultaneously	60	200	440	Ω
	R_{O14}	Drive strength 4, EnVCC = 3.0 to 3.6 V Forcing 0.4 V to 16 pins simultaneously or Forcing EnVCC – 0.4 V to 16 pins simultaneously	120	400	880	Ω

Table 3.8 Digital IO Pins: Input and Output Characteristics (2/4)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output resistance of HSIO buffer*5*8	R_{O21}		Drive strength 1, E1VCC = 3.0 to 3.6 V Forcing 0.4 V to 4 pins simultaneously or Forcing E1VCC – 0.4 V to 4 pins simultaneously	6	20	44	Ω
	R_{O22}		Drive strength 2, E1VCC = 3.0 to 3.6 V Forcing 0.4 V to 4 pins simultaneously or Forcing E1VCC – 0.4 V to 4 pins simultaneously	15	50	110	Ω
	R_{O23}		Drive strength 3, E1VCC = 3.0 to 3.6 V Forcing 0.4 V to 16 pins simultaneously or Forcing E1VCC – 0.4 V to 16 pins simultaneously	60	200	440	Ω
	R_{O24}		Drive strength 4, E1VCC = 3.0 to 3.6 V Forcing 0.4 V to 16 pins simultaneously or Forcing E1VCC – 0.4 V to 16 pins simultaneously	120	400	880	Ω
High level output voltage of GPIO buffer	V_{OH11a}	@ Drive strength 1	I_{OH11} ≥ –4.0 mA per pin (4 output pins)*4	EnVCC – 0.8		EnVCC	V
			I_{OH11} ≥ –8.0 mA per pin (1 output pin)*4	EnVCC – 0.8		EnVCC	V
	V_{OH11b}		I_{OH11} ≥ –8.0 mA per pin (2 output pins)*4	EnVCC – 1.14		EnVCC	V
	V_{OH11c}		I_{OH11} ≥ –4.0 mA per pin (Ethernet pins)*4	E1VCC – 0.6		E1VCC	V
	V_{OH12}	@ Drive strength 2	I_{OH12} ≥ –2.0 mA per pin *4	EnVCC – 0.8		EnVCC	V
	V_{OH13}	@ Drive strength 3	I_{OH13} ≥ –1.0 mA per pin *4	EnVCC – 0.8		EnVCC	V
	V_{OH14}	@ Drive strength 4	I_{OH14} ≥ –0.5mA per pin *4	EnVCC – 0.8		EnVCC	V
High level output voltage of HSIO buffer	V_{OH21a}	@ Drive strength 1	I_{OH21} ≥ –8.0 mA per pin (1 output pin)*4	E1VCC – 0.8		E1VCC	V
	V_{OH21b}		I_{OH21} ≥ –8.0 mA per pin (2 output pins)*4	E1VCC – 1.14		E1VCC	V
	V_{OH21c}		I_{OH21} ≥ –4.0 mA per pin (Ethernet pins)*4	E1VCC – 0.6		E1VCC	V
	V_{OH22a}	@ Drive strength 2	I_{OH22} ≥ –4.0 mA per pin (4 output pins)*4	E1VCC – 0.8		E1VCC	V
			I_{OH22} ≥ –8.0 mA per pin (1 output pin)*4				
	V_{OH22b}		I_{OH22} ≥ –8.0 mA per pin (2 output pins)*4	E1VCC – 1.14		E1VCC	V
	V_{OH22c}		I_{OH22} ≥ –4.0 mA per pin (Ethernet pins)*4	E1VCC – 0.6		E1VCC	V
	V_{OH23}	@ Drive strength 3	I_{OH23} ≥ –1.0 mA per pin*4	E1VCC – 0.8		E1VCC	V
	V_{OH24}	@ Drive strength 4	I_{OH24} ≥ –0.5mA per pin*4	E1VCC – 0.8		E1VCC	V
Low level output voltage for GPIO buffer	V_{OL11a}	@ Drive strength 1	I_{OL11} ≤ 4.0 mA per pin (4 output pins)*4	0		0.7	V
			I_{OL11} ≤ 8.0 mA per pin (1 output pin)*4				
	V_{OL11b}		I_{OL11} ≤ 8.0 mA per pin (2 output pins)*4	0		1.14	V
	V_{OL11c}		I_{OL11} ≤ 4.0 mA per pin (Ethernet pins)*4	0		0.4	V
	V_{OL12}	@ Drive strength 2	I_{OL12} ≤ 2.0 mA per pin*4	0		0.7	V
	V_{OL13}	@ Drive strength 3	I_{OL13} ≤ 1.0 mA per pin*4	0		0.7	V
	V_{OL14}	@ Drive strength 4	I_{OL14} ≤ 0.5mA per pin*4	0		0.7	V

Table 3.8 Digital IO Pins: Input and Output Characteristics (3/4)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Low level output voltage for HSIO buffer	V_{OL21a}	@ Drive strength 1	I_{OL21} ≤ 8.0 mA per pin (1 output pins)*4	0		0.7	V
	V_{OL21b}		I_{OL21} ≤ 8.0 mA per pin (2 output pins)*4	0		1.14	V
	V_{OL21c}		I_{OL21} ≤ 4.0 mA per pin (Ethernet pins)*4	0		0.4	V
	V_{OL22a}	@ Drive strength 2	I_{OL22} ≤ 4.0 mA per pin (4 output pins)*4	0		0.7	V
			I_{OL22} ≤ 8.0 mA per pin (1 output pin)*4				
	V_{OL22b}		I_{OL22} ≤ 8.0 mA per pin (2 output pins)*4	0		1.14	V
	V_{OL22c}		I_{OL22} ≤ 4.0 mA per pin (Ethernet pins)*4	0		0.4	V
	V_{OL23}	@ Drive strength 3	I_{OL23} ≤ 1.0 mA per pin*4	0		0.7	V
	V_{OL24}	@ Drive strength 4	I_{OL24} ≤ 0.5mA per pin*4	0		0.7	V
Output rise and fall times of GPIO buffer	t_{OR111}/ t_{OF111}	Drive strength 1 (R_{O11})	Cload = 15 pF, 20% to 80%	0.5		3.6	ns
	t_{OR112}/ t_{OF112}		Cload = 20 pF, 20% to 80%	0.7		5.0	ns
	t_{OR113}/ t_{OF113}		Cload = 30 pF, 20% to 80%	1.0		7.0	ns
	t_{OR114}/ t_{OF114}		Cload = 100 pF, 20% to 80%	3.4		21.0	ns
	t_{OR121}/ t_{OF121}	Drive strength 2 (R_{O12})	Cload = 15 pF, 20% to 80%	1.2		7.0	ns
	t_{OR122}/ t_{OF122}		Cload = 20 pF, 20% to 80%	1.6		9.0	ns
	t_{OR123}/ t_{OF123}		Cload = 30 pF, 20% to 80%	2.3		13.5	ns
	t_{OR131}/ t_{OF131}	Drive strength 3 (R_{O13})	Cload = 20 pF, 20% to 80%	3.1		18.0	ns
	t_{OR132}/ t_{OF132}		Cload = 30 pF, 20% to 80%	4.6		26.0	ns
	t_{OR141}/ t_{OF141}	Drive strength 4 (R_{O14})	Cload = 20 pF, 20% to 80%	6.3		35.5	ns
	t_{OR142}/ t_{OF142}		Cload = 30 pF, 20% to 80%	9.3		55.0	ns

Table 3.8 Digital IO Pins: Input and Output Characteristics (4/4)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output rise and fall times of HSIO buffer	t_{OR211}/ t_{OF211}	Drive strength 1 (R_{O21})	Cload = 15 pF, 20% to 80%			2.0	ns
	t_{OR221}/ t_{OF221}	Drive strength 2 (R_{O22})	Cload = 15 pF, 20% to 80%	0.5		3.6	ns
	t_{OR222}/ t_{OF222}		Cload = 20 pF, 20% to 80%	0.7		5.0	ns
	t_{OR223}/ t_{OF223}		Cload = 30 pF, 20% to 80%	1.0		7.0	ns
	t_{OR224}/ t_{OF224}		Cload = 100 pF, 20% to 80%	3.4		21.0	ns
	t_{OR231}/ t_{OF231}	Drive strength 3 (R_{O23})	Cload = 20 pF, 20% to 80%	3.1		18.0	ns
	t_{OR232}/ t_{OF232}		Cload = 30 pF, 20% to 80%	4.6		26.0	ns
	t_{OR241}/ t_{OF241}	Drive strength 4 (R_{O24})	Cload = 20 pF, 20% to 80%	6.3		35.5	ns
	t_{OR242}/ t_{OF242}		Cload = 30 pF, 20% to 80%	9.3		55.0	ns

Note 1. Specification of parameters for IO supply voltage range EnVCC = VPOC to 3.0V is not guaranteed, but no malfunction of digital IO pins will occur.

Note 2. Pn_m, JP0_0-3, JP0_5, MSYNZ, EVTIZ
Regarding to treatment for FLMD0, please refer to **Section 3.3.5, Operational Condition** for the specification of an ext. pull-down resistor required to be connected to the FLMD0 pin, see **Table 3.5, Operational Condition**.

Note 3. Pn_m, JP0_0-5, RESETZ, ERAMRESPDZ, ERAMRES2Z, AURORES2Z, AURORES1Z, AURORESPDZ
Regarding to treatment for FLMD0, please refer to **Section 3.3.5, Operational Condition** for the specification of an ext. pull-down resistor required to be connected to the FLMD0 pin, see **Table 3.5, Operational Condition**.

Note 4. The number of pin indicates simultaneous ON. In addition, total current per 1 power supply pin of I_{OL}/I_{OH} is max. ±32mA (right side or left side to 1 power supply pin is max. +16/–16mA).

Note 5. P3_9, P3_10, P3_14, P8_9, P8_10, and P8_11

Note 6. JPn_m and Pn_m excluding P3_9, P3_10, P3_14, P8_9, P8_10, and P8_11

Note 7. VI is input voltage at related input pin.

Note 8. The resistance can increase above max data in case VOH11 to VOH24 or VOL11a to VOL24 exceed the condition.

3.4.3 Analog Input Pins (ADCnIm) Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.9 Analog Input Pins (ADCnIm) Characteristics*3

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Internal pull-up resistance*1	R_{PU21}	Analog input pins (ADCnIm), VIAN = AnVSS		10	20	40	kΩ
		AnVCC = 3.0V*2	VIAN = AnVSS			40	kΩ
			VIAN = AnVCC/2			25	
			VIAN = AnVCC			16	
		AnVCC = 3.6V*2	VIAN = AnVSS	10			kΩ
			VIAN = AnVCC/2	6.8			
			VIAN = AnVCC	3.6			
Internal pull-down resistance*1	R_{PD21}	Analog input pins (ADCnIm), VIAN = AnVCC		10	20	40	kΩ
		AnVCC = 3.0V*2	VIAN = AnVSS			10	kΩ
			VIAN = AnVCC/2			21	
			VIAN = AnVCC			40	
		AnVCC = 3.6V*2	VIAN = AnVSS	2			kΩ
			VIAN = AnVCC/2	6			
			VIAN = AnVCC	10			

Note 1. Pull-up/down resistors are only used for diagnostic test.
PU and PD resistor data includes TDE switch resistance.
For TDE switch resistance data see **Table 3.55, ADC Characteristics**.
Note 2. A linear extrapolation between the 3 specified points is allowed.
Note 3. Specification is valid for ADCnIm pins.

3.4.4 Main Oscillator Input Pin (X1) Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.10 Main Oscillator Input Pin (X1) Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage high level	V_{IH21}	SYSVCC = V_{POC} to 3.6V	0.7 × SYSVCC		SYSVCC	V
Input voltage low level	V_{IL21}		0		0.30 × SYSVCC	V

Note 1. Only valid for EXCLK mode, (selected by flash option byte).

3.4.5 Aurora Interface Clock Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.11 Aurora Interface Clock Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential input voltage external AC coupled	V_{CLK} *1		200		1600	mV
Recommended external AC coupling capacitor	TRF		75	100	200	nF
Differential input resistance	ZID		70	100	130	Ω

Note 1. Peak to peak differential input voltage.

3.4.6 Injected Current Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.12 Injected Current Operating Conditions*2

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Injection current per digital input	I_{INJ_DIN}	V_{IN} > EnVCC, VIN < EnVSS	–2.0		3.0	mA
Injection current per analog input	I_{INJ_AIN}	V_{IAN} > AnVCC, VIAN < AnVSS	–2.0		3.0	mA
Injection current ERAMRES2Z	I_{INJ_DINER}	V_{IN} > ERAM1VCC, V_{IN} < ERAM1VSS	–2.0		3.0	mA
Injection current AURORESnZ	I_{INJ_DINAU}	V_I > EMUVCC, V_I < EMUVSS	–2.0		3.0	mA
Total injection current of the device	I_{INJ_TOT}	*1	—		50.0	mA

Note 1. To be considered not only at supply pin but at every point of the supply part of an IO pin.
Sum of all injected currents into all pins of the device.

Note 2. The injected current operating condition for a pin will not degrade the specified performance and functionality of other ports pins which are not affected by injected current.

3.5 Supply Current Characteristics

3.5.1 General Definition

Total current consumption is defined as follows:

$I_{TOTn} = I_{VCC} + I_{VDD} (+ I_{VCC\_ED} + I_{VDD\_ED}) + I_{EnVCC} = I_{INT} + I_{EnVCC}$

with

- I_{TOTn}: total current consumption of the device.
- I_{VCC}: Current consumption of high-voltage (HV) domain (e.g. POC, RVG, OSC, CVM, ADC, PLL, temperature sensor, flash charge pump and regulator, ect.)
- I_{VDD}: Current consumption of core domain (depending on CPU frequency)
- I_{VCC_ED}: Current consumption of IO buffer of emulation domain
- I_{VDD_ED}: Current consumption of emulation core domain
- I_{INT}: Current consumption of IVCC and IVDD and IVCC_ED and IVDD_ED.
- I_{EnVCC}: Current consumption of IO buffer

CAUTION

The parameter I_{EnVCC} depends on customer's application and thus need to be defined by customer in order to determine the total power dissipation of a device.

3.5.2 Power Supply Currents (P1M-C)

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.13 Supply Current Consumption: Device P1M-C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Current consumption of HV domain	I_{VCC31}	VCC = SYSVCC = 3.6V			28	mA
Current consumption of core*1	I_{VDD32}	fCPUCLK = 240 MHz, VDD = 1.35V, TJ =150 °C			282	mA
	I_{VDD33}	fCPUCLK = 240 MHz, VDD =1.35V,TJ =160 °C			305	mA

Note 1. Include all cores and peripherals

Note 2. Delta current is based on the max use case as reflected in IVCC31.

3.5.3 Power Supply Currents (P1H-C (4MB))

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.14 Supply Current Consumption: Device P1H-C (4MB)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Current consumption of HV domain	I_{VCC41}	VCC = SYSVCC = 3.6V			26	mA
Current consumption of core*1	I_{VDD42}	f_{CPUCLK} = 240 MHz, VDD = 1.35V, T_{JMAX}			536	mA

Note 1. Include all cores and peripherals

Note 2. Delta current is based on the max use case as reflected in IVCC41.

3.5.4 Power Supply Currents (P1H-C (8MB))

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.15 Supply Current Consumption: Device P1H-C (8MB)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Current consumption of HV domain	I_{VCC51}	VCC = SYSVCC = 3.6V			30	mA
Current consumption of core*1	I_{VDD52}	f_{CPUCLK} = 240 MHz, VDD =1.35V,T_{JMAX}			546	mA

Note 1. Include all cores and peripherals.

Note 2. Delta current is based on the max use case as reflected in IVCC51.

3.5.5 Power Supply Currents (P1H-CE)

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.16 Supply Current Consumption: Device P1H-CE

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Current consumption of HV domain	I_{VCC71}	VCC = SYSVCC = 3.4V, MP domain			30	mA
	I_{VCC_ED71}	VCC = SYSVCC = 3.4V, ED domain			35	mA
Current consumption of core (MP domain)*1	I_{VDD72}	Dual core f_{CPUCLK} = 240 MHz, VDD = 1.32V, T_{JMAX}			868	mA
	I_{VDD73}	Single core f_{CPUCLK} = 240 MHz, VDD =1.32V,T_{JMAX}			750	mA
	I_{VDD74}	Single core fCPUCLK = 160 MHz, VDD =1.32V,T_{JMAX}			690	mA
Current consumption of core (ED domain)	$I_{VDD\_ED71,eram}$	f_{CPUCLK} = 240 MHz, VDD = 1.32V, ERAM domain			138	mA
	$I_{VDD\_ED71,aur}$	f_{CPUCLK} = 240 MHz, VDD = 1.32V, Aurora domain			87	mA
Total internal current consumption	I_{INT71}	f_{CPUCLK} = 240 MHz, VDD = 1.32V, VCC = SYSVCC = 3.4 V, T_{JMAX}			1158	mA

Note 1. Include all cores and peripherals

Note 2. Delta current is based on the max use case as reflected in IVCC71.

3.6 AC Characteristics

3.6.1 AC Test Conditions

3.6.1.1 General Conditions

Below conditions are valid for all subsequent timing specifications if not noted otherwise:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- IO supply voltage range: EnVCC = 3.0 to 3.6 V
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

If there is no specification in particular, the specified spec is the following conditions.

- Output buffer is selected 100 Ω
- Capacitive load (Cload) connected to output pins is 30pF

NOTE

Even though AC characteristics correspond to the nominal frequency, a main oscillator tolerance of up to 1000ppm is considered with regard to timing characteristics for communication modules.

3.6.1.2 Input Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

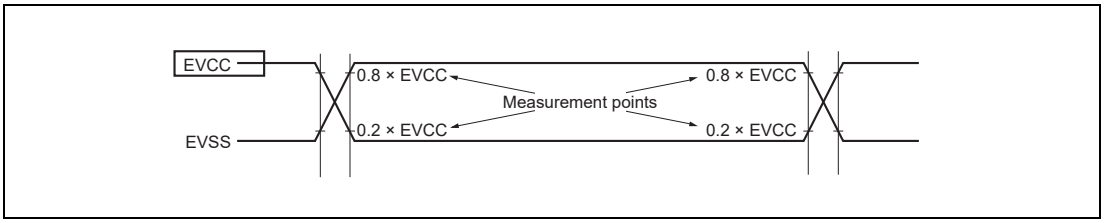


Figure 3.2 AC Input Measurement Points Definition

3.6.1.3 Output Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

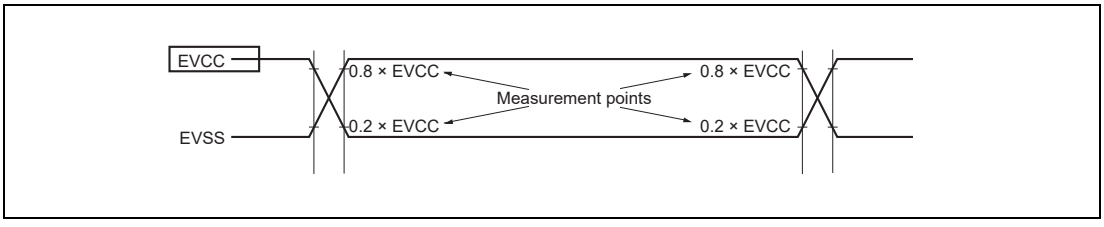


Figure 3.3 AC Output Measurement Points Definition

3.6.1.4 Load conditions

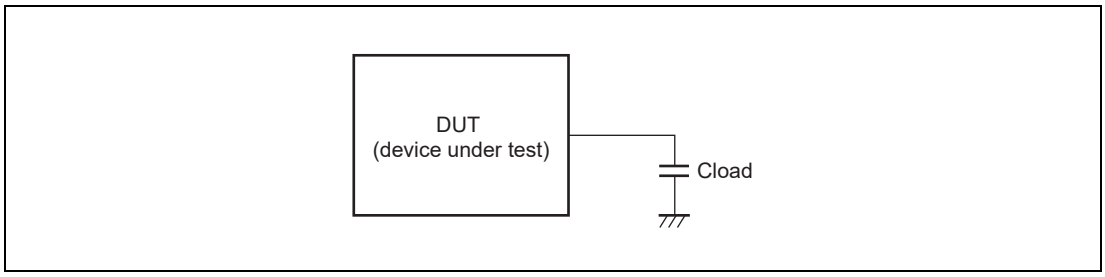


Figure 3.4 AC Load Conditions Definition

CAUTION

If not otherwise stated in conditions preceding to below AC timing specifications the following capacitive load condition is valid : Cload = 30 pF.

- **For GPIO pins with/ output drive strength 1 to 4: see the load conditions given for parameters “Output rise and fall times of GPIO buffer” in 3.4.2 Digital IO Pins Input and Output Characteristics.**
- **For HSIO pins with output drive strength 1 to 4: see the load conditions given for parameters “Output rise and fall times of HSIO buffer” in 3.4.2 Digital IO Pins Input and Output Characteristics.**

3.6.2 Power Up/Down Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**
- VCC = SYSVCC = IOVCC, with IOVCC = EnVCC, AnVCC

Table 3.17 Power-Up/Down Timing: Using RESETZ Pin*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Delay time VCC ↑ & SYSVCC ↑ & IOVCC ↑ to RESETZ ↑	$t_{DVCCPUR}$	Power-up	t_{MOST} *2			ms
Delay time VDD ↑ to RESETZ ↑	$t_{DVDDPUR}$	Power-up Only in case of DPS	0			ms
FLMD0/1 setup time time (vs RESETZ ↑)	t_{SMDR}		1			ms
FLMD1 hold time time (vs RESETZ ↑)	t_{HMDR}		1 *3			ms
MODE0/1 setup time time (vs RESETZ ↑)	t_{SMODR}		1			ms
MODE0/1 hold time time (vs RESETZ ↑)	t_{HMODR}		1			ms
Delay time RESETZ ↓ to VCC ↓ & SYSVCC↓ & IOVCC ↓ *2*4	$t_{DRVCCPD}$	Power-down*5	10.5			µs
Delay time RESETZ↓ to VDD↓*4	$t_{DRVDDPD}$	Power-down*5	10.5			µs

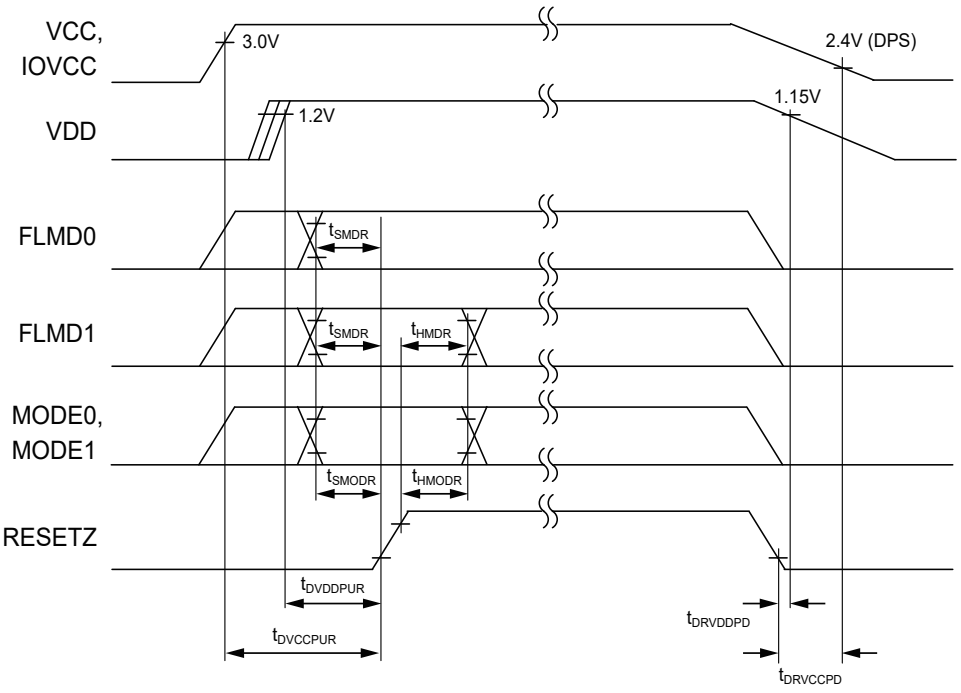
Note 1. In case power-up, power-down, RESETZ should be low. RESETZ must be asserted until CVMOUTZ is asserted and main osc. is stabilized.

Note 2. For t_{MOST} refer to **Section 3.3.2, Main Oscillator Characteristics**.

Note 3. Switching of FLMD0 after RESETZ ↑ is prohibited.

Note 4. The device can withstand up to 1000 uncontrolled power down cycles without impact on lifetime. Uncontrolled means not according to power down timing requirements.

Note 5. On reset assertion the IDD and ICC will drop significantly. Consequently the dynamic behavior to VCC and VDD has to be taken in account for the delay time.



Note: VCC = SYSVCC = IOVCC, with IOVCC = EnVCC, AnVCC.

Figure 3.5 Power-Up/Down Timing: Using RESETZ Pin

3.6.2.1 Power Up sequencing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.18 Power Up sequencing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Runtime from RESETZ ↑ to start of instruction fetch*1		P1H-CE (CLK_CPU = 240MHz), P1H-C (8MB), P1H-C (4MB) and P1M-C			22	ms
		P1H-CE (CLK_CPU = 120MHz and CLK_CPU = 160MHz)			23	ms

Note 1. Including HW BIST (see RH850/P1x-C Group User's Manual: Hardware **Section 8.4.5, HW BIST**), RAM initialization (see RH850/P1x-C Group User's Manual: Hardware **Section 8.4.6, RAM initialization**), Read Configuration Data from FLASH (see RH850/P1x-C Group User's Manual: Hardware **Section 8.4.4**, **Read Configuration Data from FLASH**) and PLL lock-up time (see **Section 3.3.3, PLL0 Characteristics**)

3.6.3 RESETZ Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.19 RESETZ Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RESETZ input low level width*1	t_{WRSL}	*2	2400			ns
RESETZ pulse rejection width*2	t_{WRRJ}	*3	400		2400	ns

Note 1. The RESETZ input incorporates an analog noise filter.

Note 2. To activate the RESETZ, the low pulse width at the RESETZ input must be greater than the specified value.

Note 3. Input pulses shorter than the given min. value will be filtered out (resulting in no Reset). Input pulses between min. and max. value result in an undefined Reset condition (i.e. pulses might be filtered out or not).

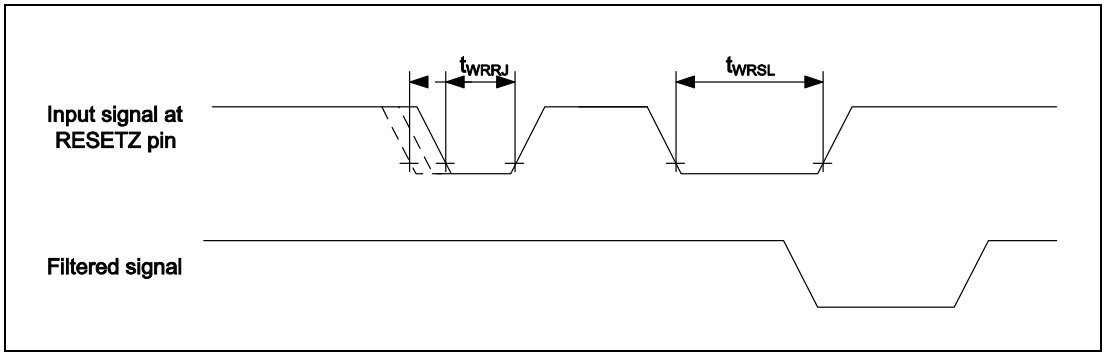


Figure 3.6 RESETZ Timing

3.6.4 Interrupt Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.20 Interrupt Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	*2	600			ns
NMI input low level width	t_{WNIL}	*2	600			ns
NMI pulse rejection width	t_{WNIRJ}	*3	100		600	ns
INTPn input high level width	t_{WITH}	*2	600			ns
INTPn input low level width	t_{WITL}	*2	600			ns
INTPn pulse rejection width	t_{WIRJ}	*3	100		600	ns

Note 1. Each NMI and INTPn input incorporates an analog noise filter.

Note 2. Pulses must be longer than the [min.] spec value in order to pass the filter.

Note 3. Input pulses shorter than the given min. value will be filtered out (resulting in no interrupt detected). Input pulses between min. and max. value result in an undefined interrupt signal condition (i.e. pulses might be filtered out or not).

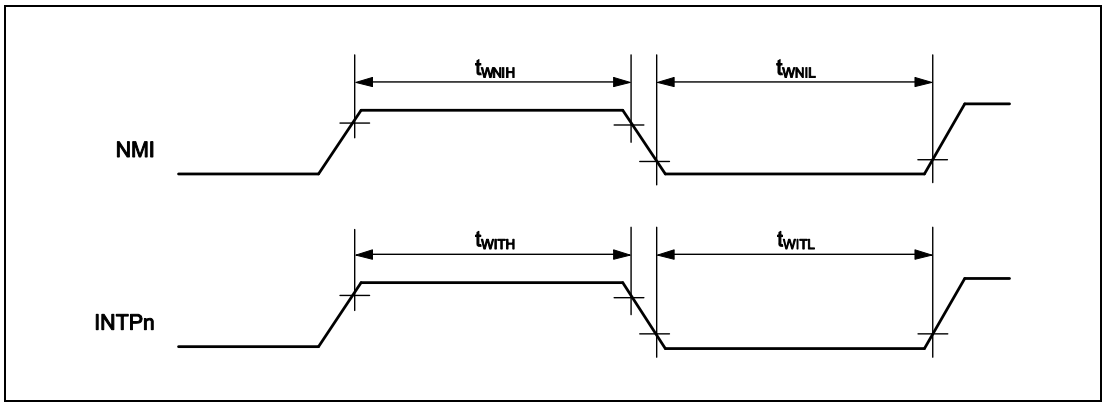


Figure 3.7 Interrupt Timing

3.6.5 Mode Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.21 Mode Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0/1 input high level width	t_{WFDH}	*2	600			ns
FLMD0/1 input low level width	t_{WFDL}	*2	600			ns
FLMD0/1 pulse rejection width	t_{WFDRJ}	*3	100		600	ns

Note 1. Each FLMD0/1 input incorporates an analog noise filter.

Note 2. Pulses must be longer than the [min.] spec value in order to pass the filter.

Note 3. Input pulses between min. and max. value result in an undefined mode signal condition (i.e. pulses might be filtered out or not).This characteristic is not tested in production.

NOTE

Switching of FLMD0 after RESETZ ↑ is prohibited.

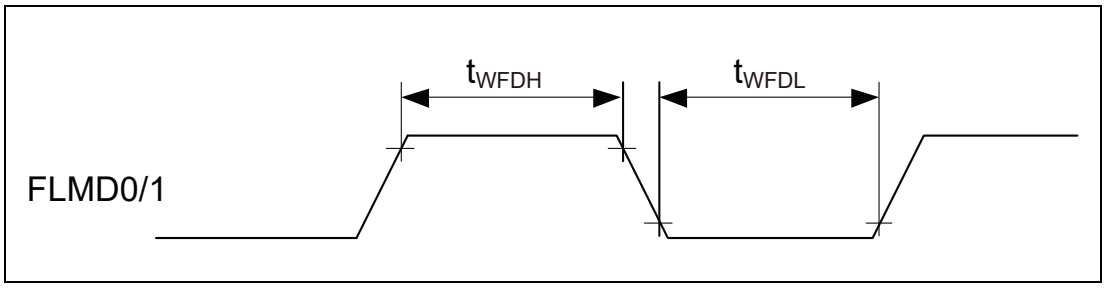


Figure 3.8 FLMD0/1 Timing

3.6.6 ADCnTRG Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.22 ADCnTRG Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCnTRG input high-level width	t_{WADH}	*2	$t_{DDNF, max}$ *3			ns
ADCnTRG input low-level width	t_{WADL}	*2	$t_{DDNF, max}$ *3			ns
ADCnTRG pulse rejection width	t_{WADRJ}	*4	$t_{DDNFmin}$ *3		$t_{DDNFmax}$ *3	ns

Note 1. The ADC trigger (ADCnTRG) input incorporates a digital noise filter (DNF).

Note 2. Pulses must be longer than the [min.] spec value in order to pass the digital filter.

Note 3. The minimum and maximum delay time of a DNF (t_{DDNF}) is calculate as follows:

$$t_{DDNF,min} = (S-1) \times \frac{1}{fs}$$

$$t_{DDNF,max} = S \times \frac{1}{fs}$$

with s: number of sampling times (S = 2.5); fs: sampling clock; f_{DNFCK}: DNF macro clock.
Please note the fs is calculated as follows:

$$fs = \frac{f_{DNFCK}}{PRS}$$; with PRS: prescaler (PRS = 1, 2, 4, 8, ..., 128)

Note 4. Input pulse shorter than the given min. value will be filtered out (resulting in no ADCnTRG). Input pulses between min. and max. value result in an undefined ADCnTRG signal condition (i.e. pulses might be filtered out or not).
This characteristic is not tested in production.

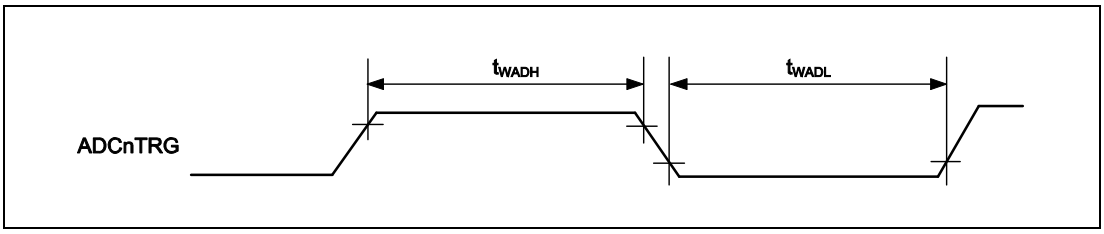


Figure 3.9 ADCnTRG Timing

3.6.7 Clock Output Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.23 Clock Output Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock output period time	t_{CLKOUT}		50			ns
Clock output high level width	t_{WCOH}		t_{CLKOUT} / 2 –15			ns
Clock output low level width	t_{WCOL}		t_{CLKOUT} / 2 –15			ns

Note 1. There is a function to output the internal clock via EXTCLKnO pin.
Note 2. For base clock refer to related RH850/P1x-C Group User's Manual: Hardware **Section 12, Clock Controller.**

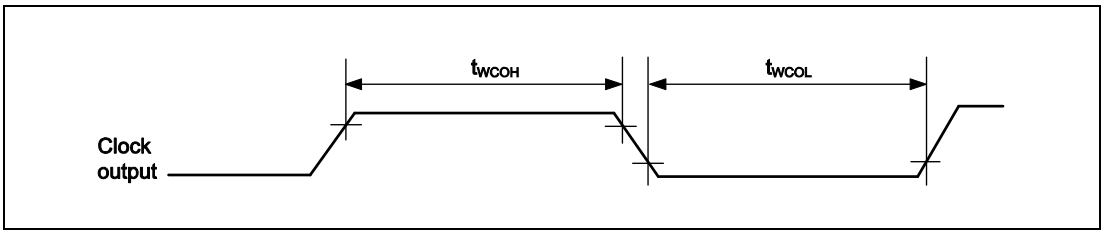


Figure 3.10 Clock Output Timing

3.6.8 High-Speed USRT Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.24 HS-USRT timing (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HSURTnCSIO to HSURTnSCKIO delay time	t_{DCSSCI}	input mode (RX)	t_{WHSCI}			ns
HSURTnSDIOm setup time	t_{SSDI}	input mode (RX)	7			ns
HSURTnSDIOm hold time	t_{SSDH}	input mode (RX)	7			ns
HSURTnSCKIO high level width	t_{WHSCI}	input mode (RX)	0.5 × t_{KCYS} – 4			ns
HSURTnSCKIO low level width	t_{WLSCI}	input mode (RX)	0.5 × t_{KCYS} – 4			ns
HSURTnSCKIO cycle time	t_{KCYS}	input mode (RX)	25			ns
HSURTnSCKIO to HSURTnCSIO delay time	t_{DSCICS}	input mode (RX)	10			ns
HSURTnCSIO high level width	t_{WHCS}	input mode (RX)	t_{KCYS}			ns
HSURTnSDIR to HSURTnCSIO delay time	t_{DSDCSI}	input mode (RX)	0			ns
HSURTnCSIO to HSURTnSDIR delay time	t_{DCSSDI}	input mode (RX)	0			ns
HSURTnCSIO to HSURTnSCKIO delay time	t_{DCSSCO}	output mode (TX)	0.5 × t_{KCYM}			ns
HSURTnSCKIO to SDO delay time	t_{DSCSDO}	output mode (TX)	0		25	ns
HSURTnSDIOm hold time	t_{HSDO}	output mode (TX)	25			ns

Table 3.24 HS-USRT timing (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HSURTnSCKIO to HSURTnCSIO inactive time	t_{ISCCSO}	output mode (TX)	0.5 × t_{KCYM}			ns
HSURTnSCKIO high level width	t_{WHSCO}	output mode (TX)	0.5 × t_{KCYM} – 15			ns
HSURTnSCKIO low level width	t_{WLSCO}	output mode (TX)	0.5 × t_{KCYM} – 15			ns
HSURTnSCKIO cycle time	t_{KCYM}	output mode (TX)	100			ns
Interframe delay	t_{KIFM}	output mode (TX)	2 × t_{KCYM}			ns
Input mode (RX)	RHSUrx				160	Mbit/s
Output mode (TX)	RUSHtx				40	Mbit/s

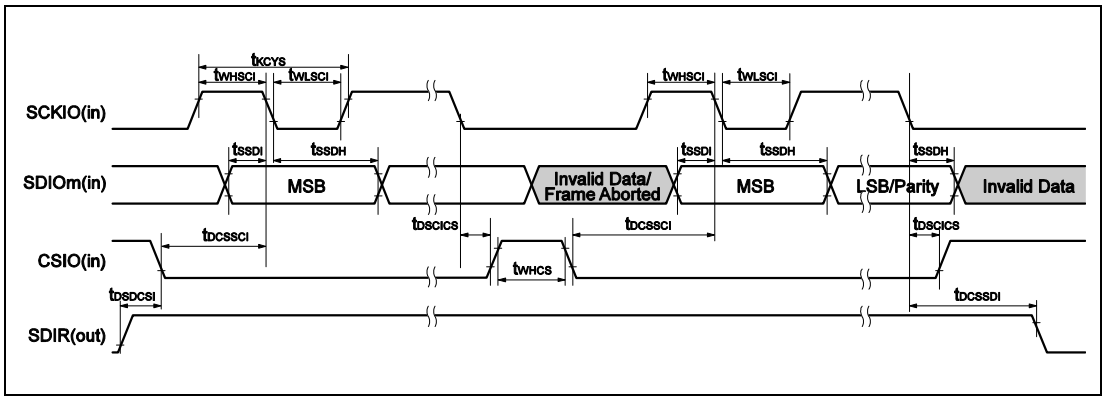


Figure 3.11 HS-USRT Receive Timing – General definition, Aborted Frame

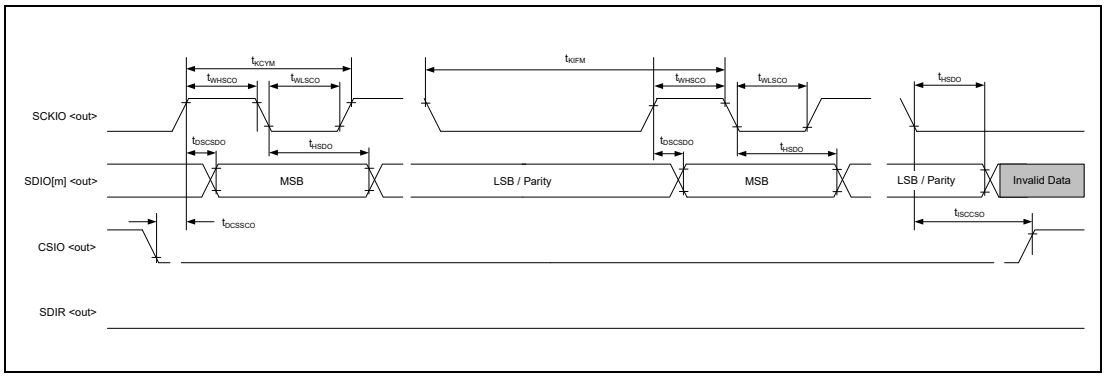


Figure 3.12 HS-USRT Transmit Timing – General Definition, two Subsequent Frames

3.6.9 CSIH Timing

3.6.9.1 CSIH Communication Speed Overview

Table 3.25 CSIH Communication Speed Overview

CSIHn/pin name \ Device		P1M-C (QFP)	P1M-C (BGA-292)	P1M-C (BGA-156)	P1H-C (4MB, BGA-292)	P1H-C (4MB, BGA-156)	P1H-C (8MB)	Port
CSIH0	SC0	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P5_6
	SO0	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P5_5
	SI0	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P5_7
	SC1	20MHz	20MHz	—	20MHz	—	20MHz	P2_12
	SO1	20MHz	20MHz	—	20MHz	—	20MHz	P2_13
	SI1	20MHz	20MHz	—	20MHz	—	20MHz	P2_11
	SC2	10MHz	10MHz	—	10MHz	—	10MHz	P0_8
	SO2	10MHz	10MHz	—	10MHz	—	10MHz	P0_9
	SI2	10MHz	10MHz	—	10MHz	—	10MHz	P0_7
CSIH1	SC0	20MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P4_3
	SO0	20MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P4_2
	SI0	20MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P4_4
	SC1	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P2_2
	SO1	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P1_2
	SI1	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P1_1
	SC2	10MHz	10MHz	—	10MHz	—	10MHz	P0_8
	SO2	10MHz	10MHz	—	10MHz	—	10MHz	P0_7
	SI2	10MHz	10MHz	—	10MHz	—	10MHz	P0_9
CSIH2	SC0	20MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P2_0
	SO0	20MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P2_1
	SI0	20MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P2_3
	SC1	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P5_7
	SO1	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P5_6
	SI1	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P5_10
	SC2	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P4_11
	SO2	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P4_10
	SI2	10MHz	10MHz	10MHz	10MHz	10MHz	10MHz	P4_12
CSIH3	SC0	10MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P1_2
	SO0	10MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P1_4
	SI0	10MHz	20MHz	20MHz	20MHz	20MHz	20MHz	P1_3
	SC1	—	10MHz	—	10MHz	—	10MHz	P6_10
	SO1	—	10MHz	—	10MHz	—	10MHz	P6_13
	SI1	—	10MHz	—	10MHz	—	10MHz	P6_12
	SC2	—	—	—	10MHz	—	10MHz	P8_3
	SO2	—	—	—	10MHz	—	10MHz	P8_0
	SI2	—	—	—	10MHz	—	10MHz	P8_1

Note: Description for CSIH communication is based on CSIH-pin group. A CSIH-pin group is defined by naming having same suffix n=> e.g. CSIH1SCn/CSIH1SOn/CSIH1SIn).

3.6.9.2 Master mode (10 MHz Communication Speed)

Conditions:

- See **Section 3.6.1.1, General Conditions**
- If not other mentioned the following conditions are different from the general ones given above:
  - Capacitive load (Cload) connected to output pins: CSIHnSC = 100pF, CSIHnSO = 100pF, CSIHnCSS = 100pF.
    It is necessary to select 50 Ω output buffer.
  - Capacitive load (Cload) connected to output pins: Up to 30pF.
    Output buffer can be selected 50/100/200 Ω.
  - EnVCC = 3.0 to 3.6V
- Usable pin for 10 MHz mode is random for all CSIH-pin group within one CSIHn (same suffix n). For CSIH-pin group see **Table 3.25, CSIH Communication Speed Overview**.
- Below terminals have no "100 Ω" output buffer.
  P3_9 (CSIH1CSS4), P3_10 (CSIH1CSS5)
  So using pin Group3 of CSIH1, please select "50 Ω" or "200 Ω" output buffer about all pin Group3 of CSIH1. About Group3 of CSIH1, see "**Section 2, Pin Functions**".

Table 3.26 CSIH Timing (Master Mode, 10 MHz Communication Speed) (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSIH Operation clock cycle time	t_{KCYn}		6.25			ns
CSIHnSC cycle time	t_{KCYMn}		100			ns
CSIHnSC high level width	t_{KWHMn}	Cload = 20pF@50Ω output buffer select	0.5 × t_{KCYMn} – 7			ns
		Cload = 30pF@50Ω output buffer select	0.5 × t_{KCYMn} – 9			ns
		Cload = 100pF@50Ω output buffer select	0.5 × t_{KCYMn} – 23			ns
		Cload = 15pF@100Ω output buffer select	0.5 × t_{KCYMn} – 9			ns
		Cload = 30pF@100Ω output buffer select	0.5 × t_{KCYMn} – 15.5			ns
		Cload = 20pF@200Ω output buffer select	0.5 × t_{KCYMn} – 20			ns
		Cload = 30pF@200Ω output buffer select	0.5 × t_{KCYMn} – 28			ns

Table 3.26 CSIH Timing (Master Mode, 10 MHz Communication Speed) (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSIHnSC low level width	t_{KWLMn}	Cload = 20pF@50Ω output buffer select	0.5 × t_{KCYMn} – 7			ns
		Cload = 30pF@50Ω output buffer select	0.5 × t_{KCYMn} – 9			ns
		Cload = 100pF@50Ω output buffer select	0.5 × t_{KCYMn} – 23			ns
		Cload = 15pF@100Ω output buffer select	0.5 × t_{KCYMn} – 9			ns
		Cload = 30pF@100Ω output buffer select	0.5 × t_{KCYMn} – 15.5			ns
		Cload = 20pF@200Ω output buffer select	0.5 × t_{KCYMn} – 20			ns
		Cload = 30pF@200Ω output buffer select	0.5 × t_{KCYMn} – 28			ns
CSIHnSI setup time (vs. CSIHnSC)*1	t_{SSIMn}	*4	28			ns
CSIHnSI hold time (vs. CSIHnSC)*1	t_{HSIMn}	*4	0			ns
CSIHnSO output delay	t_{DSOMn}*5				7	ns
CSIHnCSS[7:0] inactive width	t_{WSCSBn}		CSIDLE × t_{KCYMn} – 28 *1			ns
CSIHnCSS[7:0] setup time (vs. CSIHnSC)	$t_{SSCSBn0}$	CSIHnCTL1.CSIHnDAP = 0	CSSETUP × t_{KCYMn} – 10 *2			ns
	$t_{SSCSBn1}$	CSIHnCTL1.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMn} – 10*2			ns
CSIHnCSS[7:0] hold time (vs. CSIHnSC)	$t_{HSCSBn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMn} – 5*3			ns
	$t_{HSCSBn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMn} – 5*3			ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYI}		2 × t_{KCYn} + 54			ns
CSIHnRYI high level width	t_{WRYI}		t_{KCYn} + 5			ns

Note 1. CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]

Note 2. CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]

Note 3. CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]

Note 4. Please set SLRS = 1 if this specification can not be achieved by setting SLRS = 0 (See **Figure 3.13** and **Figure 3.14**). SLRS: Setting value of CSIHnCTL1.CSIHnSLRS

Note 5. tDSOMn timing is only valid for CSIHnSC and CSIHnSO have same output rise and fall times. If not identical the timing changes according the differences of Output rise and fall times. For tOR/tOF refer to “Output rise and fall times of GPIO buffer” in **Section 3.4.2, Digital IO Pins Input and Output Characteristics**.

3.6.9.3 Master mode (20 MHz Communication Speed)

Conditions:

- See **Section 3.6.1.1, General Conditions**
- If not other mentioned the following conditions are different from the general ones given above:
  - Capacitive load (Cload) connected to output pins: CSIHnSC = 15pF, CSIHnSO = 15pF, CSIHnCSS = 15pF.
    It is necessary to select 50 Ω output buffer.
  - EnVCC = 3.0 to 3.6V
- Usable pin for 20 MHz mode belong to same CSIH-pin group. For 20 MHz CSIH-pin group refer to **Table 3.25, CSIH Communication Speed Overview**.

Table 3.27 CSIH Timing (Master Mode, SLRS = 1, 20 MHz Communication Speed)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSIH Operation clock cycle time	t_{KCYn}		6.25			ns
CSIHnSC cycle time	t_{KCYMn}		50			ns
CSIHnSC high level width	t_{KWHMn}		$0.5 \times t_{KCYMn} - 6$			ns
CSIHnSC low level width	t_{KWLMn}		$0.5 \times t_{KCYMn} - 6$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMn}	SLRS = 1*4	20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMn}	SLRS = 1*4	0			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMn}				7	ns
CSIHnCSS[7:0] inactive width	t_{WSCSBn}		CSIDLE × t_{KCYMn} – 23*1			ns
CSIHnCSS[7:0] setup time (vs. CSIHnSC)	$t_{SSCSBn0}$	CSIHnCTL1.CSIHnDAP = 0	CSSETUP × t_{KCYMn} – 10*2			ns
	$t_{SSCSBn1}$	CSIHnCTL1.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMn} – 10*2			ns
CSIHnCSS[7:0] hold time (vs. CSIHnSC)	$t_{HSCSBn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMn} – 5*3			ns
	$t_{HSCSBn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMn} – 5*3			ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYI}		$2 \times t_{KCYn} + 48$			ns
CSIHnRYI high level width	t_{WRYI}		$t_{KCYn} + 5$			ns

Note 1. CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
Note 2. CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
Note 3. CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
Note 4. SLRS: Setting value of CSIHnCTL1.CSIHnSLRS

3.6.9.4 Slave mode (10 MHz Communication Speed)

Conditions:

- See **Section 3.6.1.1, General Conditions**
- If not other mentioned the following conditions are different from the general ones given above:
  - Capacitive load (Cload) connected to output pins: Up to 100pF
    It is necessary to select 50 Ω output buffer.
  - Capacitive load (Cload) connected to output pins: Up to 30pF.
    Output buffer can be selected 50/100/200 Ω.
  - EnVCC = 3.0 to 3.6V
- Usable pin for 10 MHz mode is random for all CSIH-pin group within one CSIHn (same suffix n).
  For CSIH-pin group see **Table 3.25, CSIH Communication Speed Overview**.

Table 3.28 CSIH Timing (Slave Mode, 10 MHz Communication Speed)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSIH Operation clock cycle time	t_{KCYn}		6.25			ns
CSIHnSC cycle time	t_{KCYSn}		100			ns
CSIHnSC high level width	t_{KWHSn}		0.5 × t_{KCYSn} – 28			ns
CSIHnSC low level width	t_{KWLSn}		0.5 × t_{KCYSn} – 28			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISn}		10			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISn}		t_{KCYn} + 5			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSn}				54	ns
CSIHnRYO output delay	t_{SRYOn}	t_{KCYSn} / t_{KCYn} is 8 and over			54	ns
		t_{KCYSn} / t_{KCYn} is less than 8			54 + tKCYSn	ns
CSIHnSSIZ setup time (vs. CSIHnSC)	t_{SSSIn}		0.5 × t_{KCYSn} – 10			ns
CSIHnSSIZ hold time (vs. CSIHnSC)	t_{HSSIn}		t_{KCYn} + 5			ns

3.6.9.5 Slave mode (20 MHz Communication Speed)

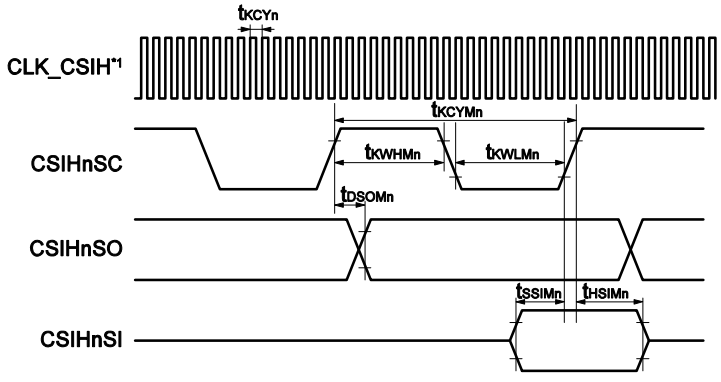
Conditions:

- See **Section 3.6.1.1, General Conditions**
- If not other mentioned the following conditions are different from the general ones given above:
  - Capacitive load (Cload) connected to output pins: Up to 15pF
    It is necessary to select 50 Ω output buffer.
  - EnVCC = 3.0 to 3.6V
- Usable pin for 20 MHz mode belong to same CSIH-pin group. For 20 MHz CSIH-pin group refer to **Table 3.25, CSIH Communication Speed Overview**.

Table 3.29 CSIH Timing (Slave Mode, 20 MHz Communication Speed)

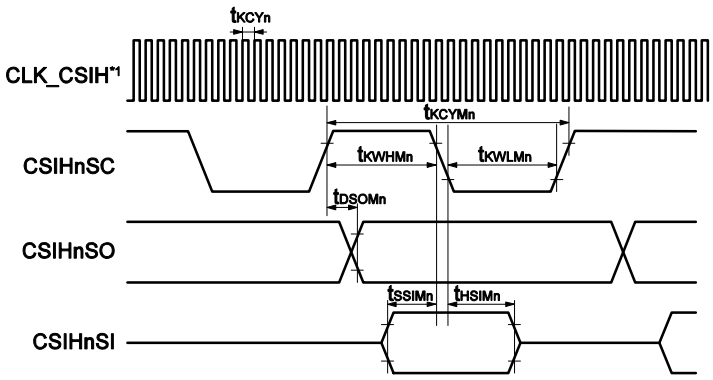
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSIH Operation clock cycle time	t_{KCYn}		6.25			ns
CSIHnSC cycle time	t_{KCYSn}		50			ns
CSIHnSC high level width	t_{KWHSn}		0.5 × t_{KCYSn} – 6			ns
CSIHnSC low level width	t_{KWLSn}		0.5 × t_{KCYSn} – 6			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISn}		10			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISn}		t_{KCYn} + 5			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOSn}				24	ns
CSIHnRYO output delay	t_{SRYOn}				24	ns
CSIHnSSIZ setup time (vs. CSIHnSC)	t_{SSSIn}		0.5 × t_{KCYSn} – 10			ns
CSIHnSSIZ hold time (vs. CSIHnSC)	t_{HSSIn}		t_{KCYn} + 5			ns

(1) CSIH Waveform (Master Mode)



Note 1. CLK_CSIH is internal clock.

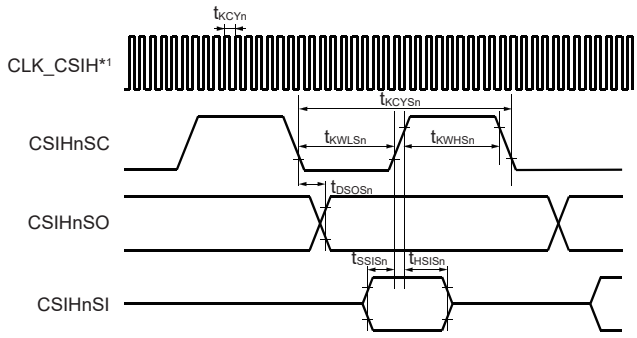
Figure 3.13 CSIH Master Mode Timing – SLRS = 1



Note 1. CLK_CSIH is internal clock.

Note: CSIHnCKR = 0, CSIHnCKP0 = 0, CSIHnDAP0 = 1 or CSIHnCKR = 0, CSIHnCKP0 = 1, CSIHnDAP0 = 0 or CSIHnCKR = 1, CSIHnCKP0 = 0, CSIHnDAP0 = 0

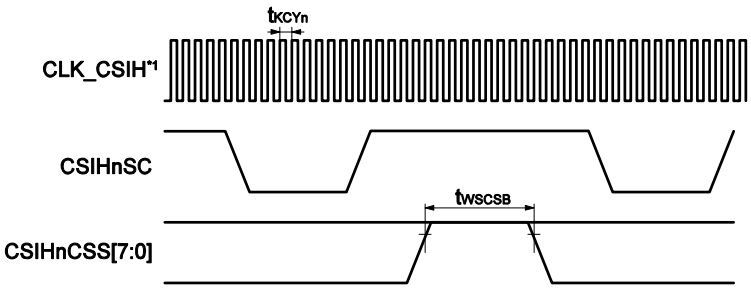
Figure 3.14 CSIH Master Mode Timing – SLRS = 0



Note 1. CLK_CSIH is internal clock.

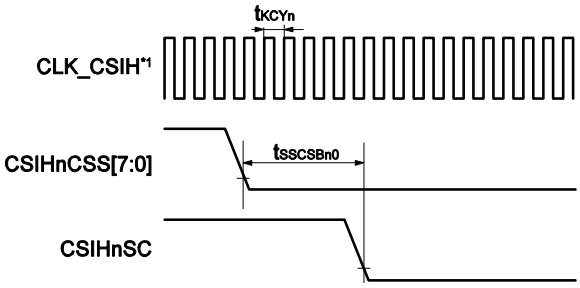
Note: CSIHnCKR = 0, CSIHnCKP0 = 0, CSIHnDAP0 = 0 or CSIHnCKR = 0, CSIHnCKP0 = 1, CSIHnDAP0 = 1 or CSIHnCKR = 1, CSIHnCKP0 = 0, CSIHnDAP0 = 1

Figure 3.15 CSIH Master Mode Timing – SLRS = 0



Note 1. CLK_CSIH is internal clock.

Figure 3.16 CSIH Master Mode Timing – CSS[7:0] inactive width



Note 1. CLK_CSIH is internal clock.

Figure 3.17 CSIH Master Mode Timing – CSS[7:0] setup (CSIHnDAP = 0)

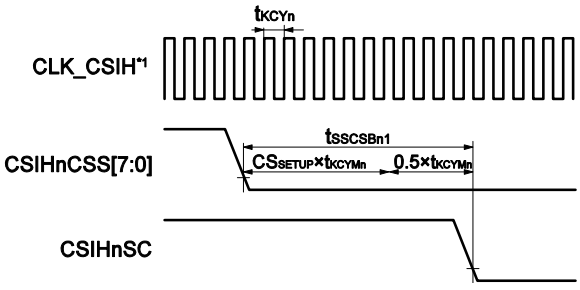
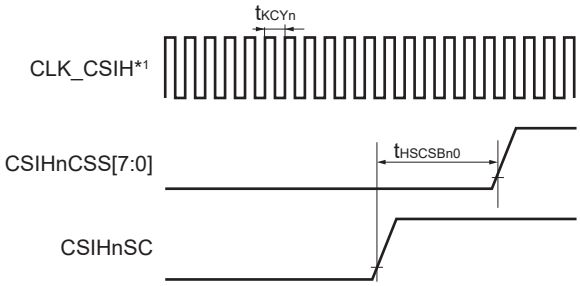
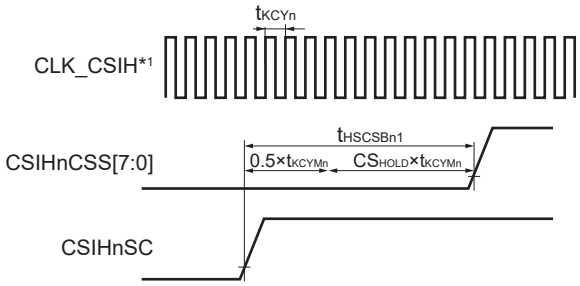


Figure 3.18 CSIH Master Mode Timing – CSS[7:0] setup (CSIHnDAP0 = 1)



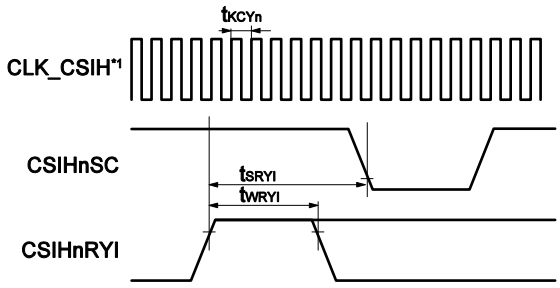
Note 1. CLK_CSIH is internal clock.

Figure 3.19 CSIH Master Mode Timing – CSS[7:0] hold (CSIHnSIT = 0)



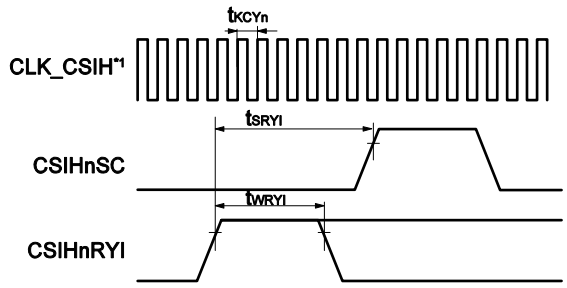
Note 1. CLK_CSIH is internal clock.

Figure 3.20 CSIH Master Mode Timing – CSS[7:0] hold (CSIHnSIT = 1)



Note 1. CLK_CSIH is internal clock.

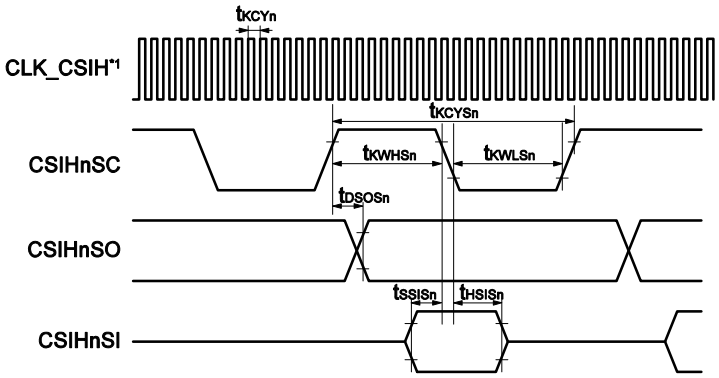
Figure 3.21 CSIH Master Mode Timing – CSS[7:0] RYI (CSIHnCKP0 = 0)



Note 1. CLK_CSIH is internal clock.

Figure 3.22 CSIH Master Mode Timing – CSS[7:0] RYI (CSIHnCKP0 = 1)

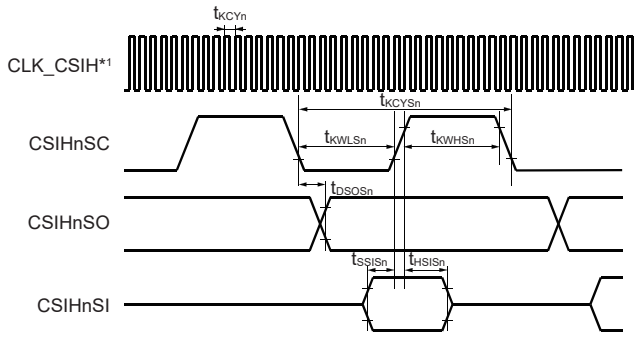
(2) CSIH Waveform (Slave Mode)



Note 1. CLK_CSIH is internal clock.

Note: CSIHnCKR = 0, CSIHnCKP0 = 0, CSIHnDAP0 = 1 or CSIHnCKR = 0, CSIHnCKP0 = 1, CSIHnDAP0 = 0 or CSIHnCKR = 1, CSIHnCKP0 = 0, CSIHnDAP0 = 0

Figure 3.23 CSIH Slave Mode Timing – General Definition



Note 1. CLK_CSIH is internal clock.

Note: CSIHnCKR = 0, CSIHnCKP0 = 0, CSIHnDAP0 = 0 or CSIHnCKR = 0, CSIHnCKP0 = 1, CSIHnDAP0 = 1 or CSIHnCKR = 1, CSIHnCKP0 = 0, CSIHnDAP0 = 1

Figure 3.24 CSIH Slave Mode Timing – General Definition

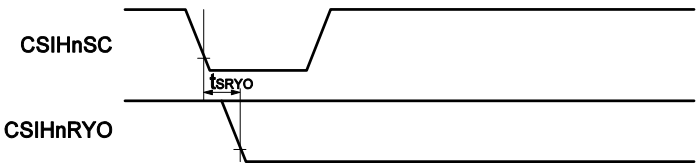


Figure 3.25 CSIH Slave Mode Timing – RYO (CSIHnCKP0 = 0, CSIHDAP0 = 0)

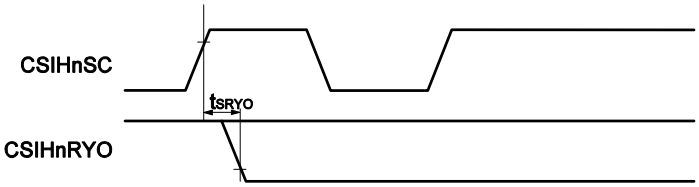


Figure 3.26 CSIH Slave Mode Timing – RYO (CSIHnCKP = 0, CSIHDAP0 = 1)

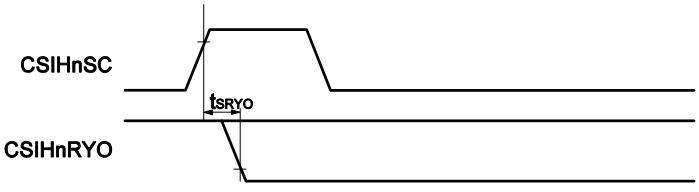


Figure 3.27 CSIH Slave Mode Timing – RYO (CSIHnCKP0 = 1, CSIHDAP0 = 0)

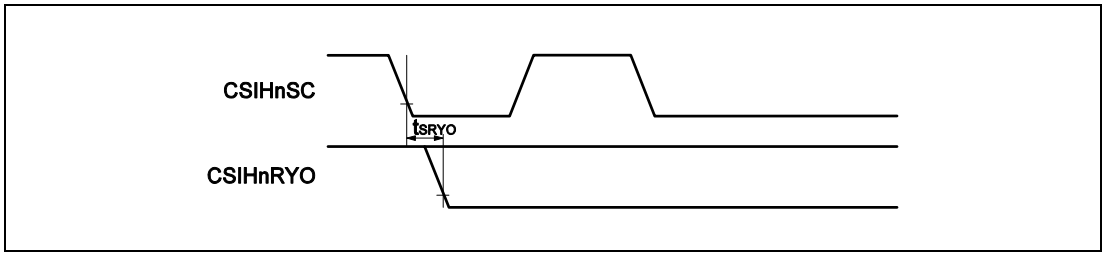
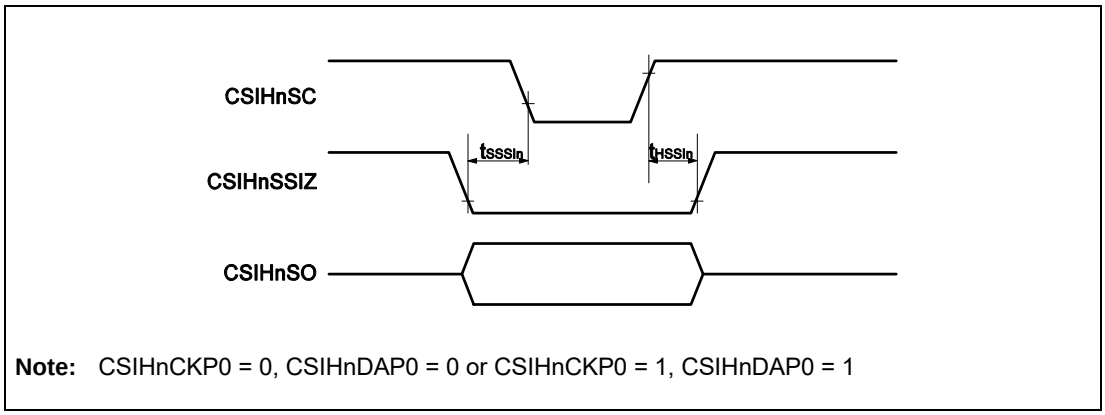
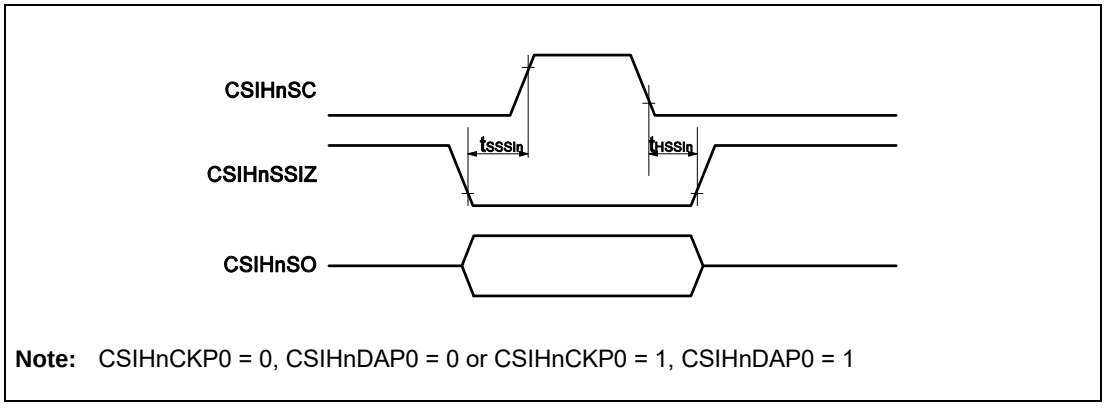


Figure 3.28 CSIH Slave Mode Timing – RYO (CSIHnCKP0 = 1, CSIHDAP0 = 1)



Note: CSIHnCKP0 = 0, CSIHnDAP0 = 0 or CSIHnCKP0 = 1, CSIHnDAP0 = 1

Figure 3.29 CSIH Slave Mode Timing – SSI



Note: CSIHnCKP0 = 0, CSIHnDAP0 = 0 or CSIHnCKP0 = 1, CSIHnDAP0 = 1

Figure 3.30 CSIH Slave Mode Timing – SSI

3.6.10 FlexRay Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**
- The following conditions are different from the general ones given above:
  - Capacitive load (Cload) connected to output pins: Up to 25pF
    It is necessary to select 50 Ω output buffer.
  - EnVCC = 3.0 to 3.6V.

Table 3.30 FlexRay Timing*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	RFLX	FLXnRXDA, FLXnRXDB, 10Mbps			10	Mbps

Note 1. Base of this specification is “FlexRay Electrical Physical Layer Specification V3.0.1, Oct-2010”

NOTE

“n” means unit number of Flexray. n = 0 or 1

3.6.11 RLIN3 Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.31 RLIN3 Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate	RRLlin	LIN mode			20	kbps
	RLurt	UART mode			6.6	Mbps

3.6.12 Ethernet Timing

3.6.12.1 MII Characteristics

Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: Up to 15pF
  It is necessary to select 50 Ω output buffer.

Table 3.32 Ethernet Timing – 100 Mbit/s MII Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHmTXCLK width	t_{MTC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETHmTXCLK high width	t_{MTCH}	*1	14	20	26	ns
ETHmTXCLK low width	t_{MTCL}	*1	14	20	26	ns
ETHmTXD [3:0] delay time	t_{MTXD}		0		25	ns
ETHmTXEN delay time	t_{MTXE}		0		25	ns
ETHmRXCLK width	t_{MRC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETHmRXCLK high width	t_{MRCH}	*1	14	20	26	ns
ETHmRXCLK low width	t_{MRCL}	*1	14	20	26	ns
ETHmRXD [3:0] setup time	t_{MRXDS}		10			ns
ETHmRXD [3:0] hold time	t_{MRXDH}		10			ns
ETHmRXDV, ETHmRXER setup time	t_{MRDES}		10			ns
ETHmRXDV, ETHmRXER hold time	t_{MRDEH}		10			ns

Note 1. The duty cycle of ETHmTXCLK and ETHmRXCLK shall be between 35 to 60% inclusive. (IEEE802.3)

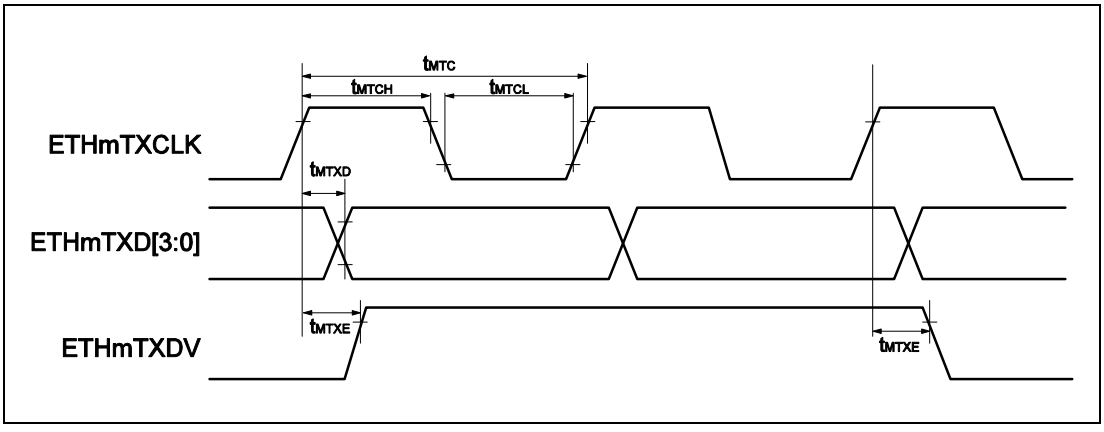


Figure 3.31 Ether net Timing – MII Transmitter

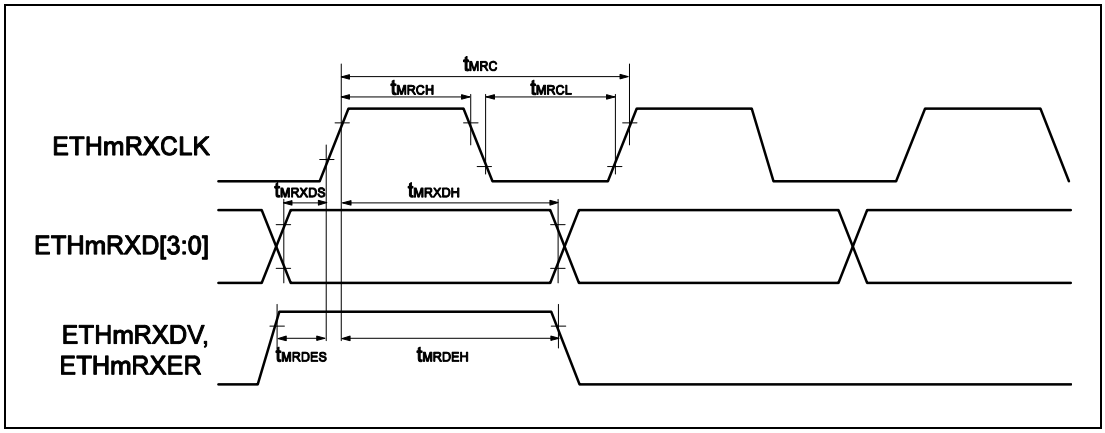


Figure 3.32 Ethernet Timing – MII Receiver

3.6.12.2 RMII Characteristics

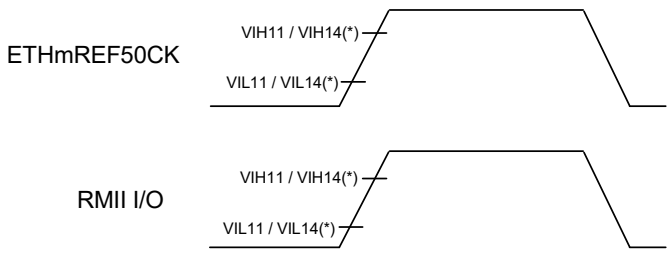
Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: Up to 15pF
  It is necessary to select 20 Ω output buffer.

Table 3.33 Ethernet Timing – RMII Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHmREF50CK width	t_{RMC}		20 – 50 ppm	20	20 + 50 ppm	ns
ETHmREF50CK high width	t_{RMCH}	*1	7		13	ns
ETHmREF50CK low width	t_{RMCL}	*1	7		13	ns
ETHmRXD [1:0], ETHmCRS and ETHmRXER setup time	t_{RMS}		4			ns
ETHmRXD [1:0], ETHmCRS and ETHmRXER hold time	t_{RMH}		2			ns
ETHmTXD [1:0], ETHmTXEN output delay time	t_{RMD}	Cload < 15 pF	2		16	ns

Note 1. The duty cycle of ETHmREF50CK shall be between 35% to 65% inclusive. (RMII™ specification)



Note 1. VIH and VIL specification depend on PISn/JPIS0 register setting. Refer to **Section 2 Pin Functions**

Figure 3.33 Ethernet Timing – RMII AC Measurements (Valid I/O Levels)

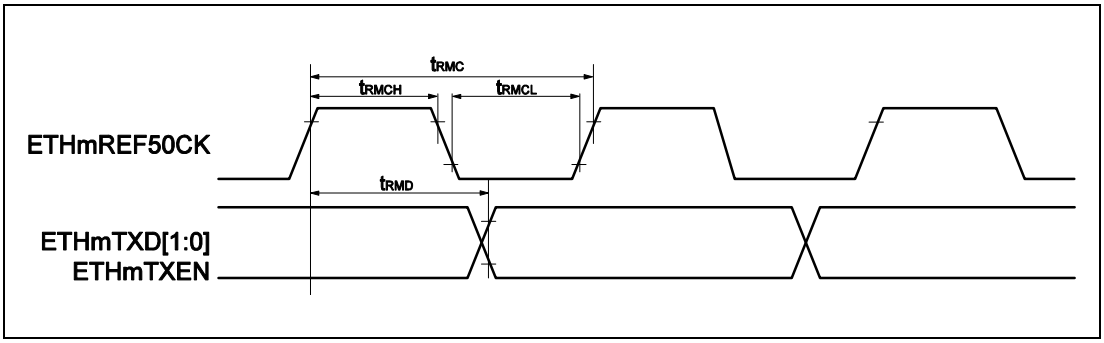


Figure 3.34 Ethernet Timing – RMII Transmitter

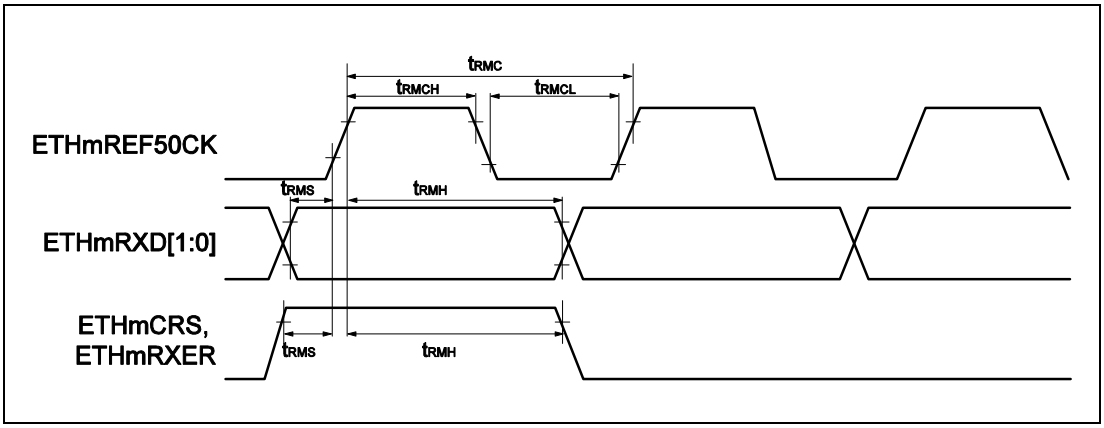


Figure 3.35 Ethernet Timing – RMII Receiver

3.6.13 GTM Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**
- Below terminals have no “100 Ω” output buffer.
  P3_9 (GTMAT1O0), P3_10 (GTMAT0O1), P3_14 (GTMAT0O1),
  P8_9 (GTMAT2O0), P8_10 (GTMAT20N), P8_11 (GTMAT2O1)
  So please select “50 Ω” or “200 Ω” output buffer about these terminals.

Table 3.34 GTM Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
GTM input high-level width	t_{WGTH}		$2 \times T_{samp}$ *1			ns
GTM input low-level width	t_{WGTL}		$2 \times T_{samp}$ *1			ns
GTM output cycle time	t_{CYGT}		$4 \times T_{samp}$ *1			ns

Note 1. $T_{samp} = 1 / f_{CLK\_HSB}$

3.6.14 MCAN Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**
- Below terminals have no “100 Ω” output buffer.
  P8_10 (MTTCAN0SOC), P8_11 (MTTCAN0TMP)
  So please select “50 Ω” or “200 Ω” output buffer about these terminals.

Table 3.35 MCAN Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate*1	RMCN1	CAN-FD arbitration and CAN 2.0B			1	Mbps
	RMCN2*2	CAN-FD data phase			8	Mbps
Internal delay time (input plus output)	tDMCIN	tDIN + tDOUT (Cload = 15pF, with 50 Ω output buffer)			30	ns

Note 1. Protocol layer clock needs to be configured appropriately.
Note 2. It is necessary to select 50 Ω output buffer.

3.6.15 External Memory Controller (MEMC0) Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**
- The following conditions are different from the general ones given above:
  - Please use internal pull-up for external memory interface data signal MEMC0D[7:0]I /MEMC0D[7:0]O
  - Below terminals have no “100 Ω” output buffer.
    P8_9 (MEMC0D1O), P8_10 (MEMC0D2O), P8_11 (MEMC0D3O)
    So please select “50 Ω” output buffer about these terminals.

3.6.15.1 MEMC0 — Read Access Timing (50 Ω output buffer / 30pF).

Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: Up to 30pF
  It is necessary to select 50 Ω output buffer.

Table 3.36 MEMC0 – Read Access Timing (50 Ω output buffer / 30pF)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T	Max. 20 MHz	50			ns
MEMC0D[7:0] data input setup time (from _MEMC0RDZ↓)	t_{SRDID}				T(*1) – 29	ns
MEMC0RDZ low level width	t_{WRDL}		T(*1) – 19			ns
MEMC0A[8:0] address, MEMC0CS[3:0]Z →MEMC0RDZ↓ delay time	t_{DARD}		T – 19			ns
MEMC0RDZ↑→from MEMC0A[8:0] address, MEMC0CS[3:0]Z delay time	t_{DRDA}		–15			ns
MEMC0D[7:0] data input hold time (from MEMC0RDZ↑)	t_{HRDID}		0			ns
MEMC0RDZ↑→MEMC0D[7:0] data output delay time	t_{DRDOD}		T(*2) – 9			ns

Note 1. Adjustment by WD is possible. W_D: wait cycle determined by DWC0 register.
Note 2. Adjustment by IWR is possible. I_{WR}: number of idle state after read cycle.

3.6.15.2 MEMC0 — Read Access Timing (100 Ω output buffer / 30pF).

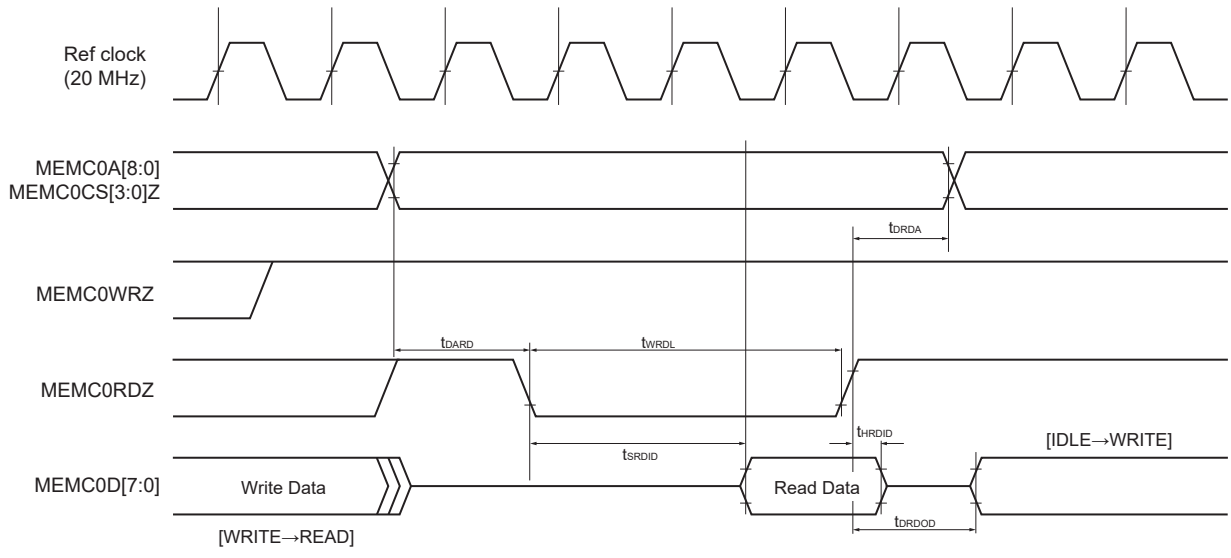
Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: Up to 30pF
  Output buffer can be selected 50/100 Ω output buffer.

Table 3.37 MEMEC0 – Read Access Timing (100 Ω output buffer / 30pF)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T	Max. 20 MHz	50			ns
MEMC0D[7:0] data input setup time (from _MEMC0RDZ↓)	t_{SRDID}				T(*1) – 38	ns
MEMC0RDZ low level width	t_{WRDL}		T(*1) – 19			ns
MEMC0A[8:0] address, MEMC0CS[3:0]Z →MEMC0RDZ↓ delay time	t_{DARD}		T – 25.5			ns
MEMC0RDZ↑→from MEMC0A[8:0] address, MEMC0CS[3:0]Z delay time	t_{DRDA}		–15			ns
MEMC0D[7:0] data input hold time (from MEMC0RDZ↑)	t_{HRDID}		0			ns
MEMC0RDZ↑→MEMC0D[7:0] data output delay time	t_{DRDOD}		T(*2) – 9			ns

Note 1. Adjustment by WD is possible. W_D: wait cycle determined by DWC0 register.
Note 2. Adjustment by IWR is possible. I_{WR}: number of idle state after read cycle.



Note: The dashed lines indicates high impedance.

Figure 3.36 MEMC0 – READ Access Timing

3.6.15.3 MEMC0 — Write Access Timing (50 Ω output buffer / 30pF)

Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: Up to 30pF
  It is necessary to select 50 Ω output buffer.

Table 35.38 MEMC0 – Write Access Timing (50 Ω output buffer / 30pF)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T	Max. 20 MHz	50			ns
MEMC0A[8:0] address, MEMC0CS[3:0]Z delay time (from _MEMC0WRZ↓)	t_{DAWR}		T – 19			ns
MEMC0WRZ↑→MEMC0A[8:0] address, MEMC0CS[3:0]Z delay time	t_{DWRA}		T(*2) – 25			ns
MEMC0WRZ low level width	t_{WWRL}		T(*1) – 19			ns
MEMC0D[7:0] data output setup time (from MEMC0WRZ↑)	t_{SODWR1}	WRITE2	2T(*1) – 19			ns
MEMC0D[7:0] data output setup time (from MEMC0WRZ↑)	t_{SODWR2}	WRITE1	2T(*1) – 19			ns
MEMC0D[7:0] data output hold time (from MEMC0WRZ↑)	t_{HWROD1}	WRITE2	T(*2) – 9			ns
MEMC0D[7:0] data output hold time (from MEMC0WRZ↑)	t_{HWROD2}	WRITE1	T(*2) – 9			ns

Note 1. Adjustment by WD is possible. W_D: Wait cycle determined by DWC0 register.
Note 2. Adjustment by WDH is possible. W_{DH}: wait cycle determined by DHC register.

3.6.15.4 MEMC0 — Write Access Timing (100 Ω output buffer / 30pF)

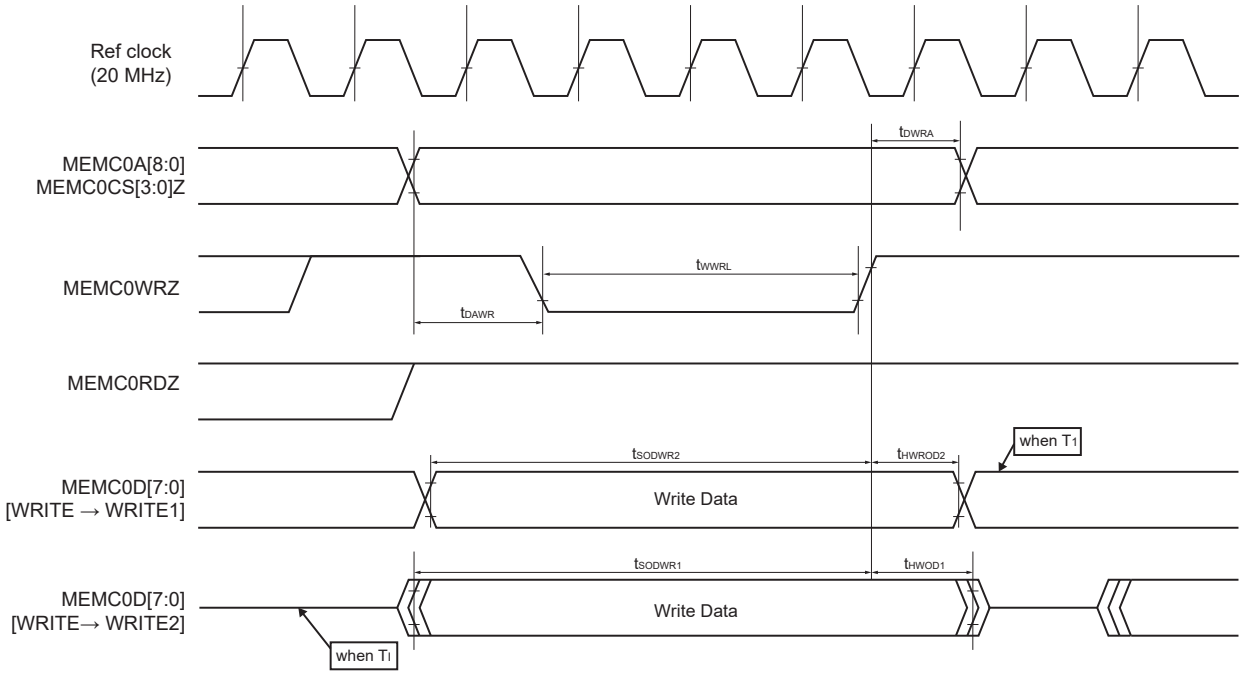
Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: Up to 30pF
  Output buffer can be selected 50/100 Ω output buffer.

Table 3.39 MEMC0 – Write Access Timing (100 Ω output buffer / 30pF)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bus operational period	T	Max. 20 MHz	50			ns
MEMC0A[8:0] address, MEMC0CS[3:0]Z delay time (from _MEMC0WRZ↓)	t_{DAWR}		T – 25.5			ns
MEMC0WRZ↑→MEMC0A[8:0] address, MEMC0CS[3:0]Z delay time	t_{DWRA}		T(*2) – 25			ns
MEMC0WRZ low level width	t_{WWRL}		T(*1) – 19			ns
MEMC0D[7:0] data output setup time (from MEMC0WRZ↑)	t_{SODWR1}	WRITE2	2T(*1) – 25.5			ns
MEMC0D[7:0] data output setup time (from MEMC0WRZ↑)	t_{SODWR2}	WRITE1	2T(*1) – 25.5			ns
MEMC0D[7:0] data output hold time (from MEMC0WRZ↑)	t_{HWROD1}	WRITE2	T(*2) – 9			ns
MEMC0D[7:0] data output hold time (from MEMC0WRZ↑)	t_{HWROD2}	WRITE1	T(*2) – 9			ns

Note 1. Adjustment by WD is possible. W_D: Wait cycle determined by DWC0 register.
Note 2. Adjustment by WDH is possible. W_{DH}: wait cycle determined by DHC register.



Note 1. In case of WRITE → WRITE operation
If TI cycle is not inserted, MEMC0 operates as [WRITE → WRITE1]
If TI cycle is inserted, MEMC0 operates as [WRITE → WRITE2]

Note 2. The dashed lines indicates high impedance.

Figure 3.37 MEMC0 – Write Access Timing

3.6.16 Emergency Shut-Off (ESO) Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.40 ESO Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Delay time ESOnZ ↓ to GTMATnOx HiZ	t_{DESO}				50	ns

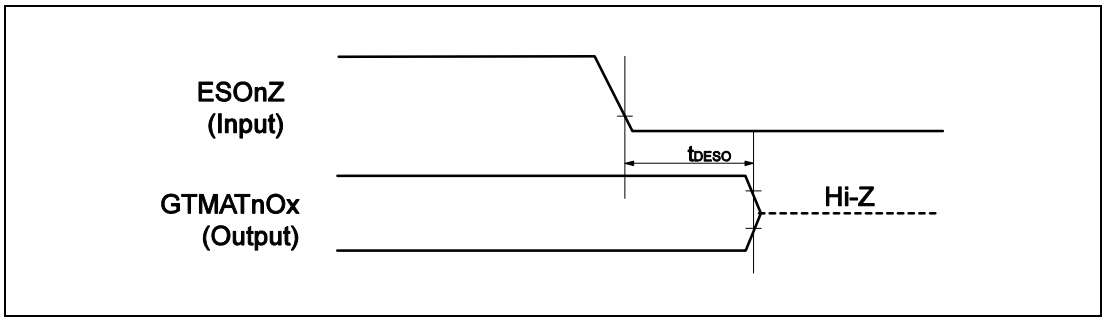


Figure 3.38 ESO Timing

3.6.17 TRSTZ Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

Table 3.41 TRSTZ Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TRSTZ input low level width	t_{WTRL}		600			ns
TRSTZ release timing delay	t_{DTRT2R}		30			ms

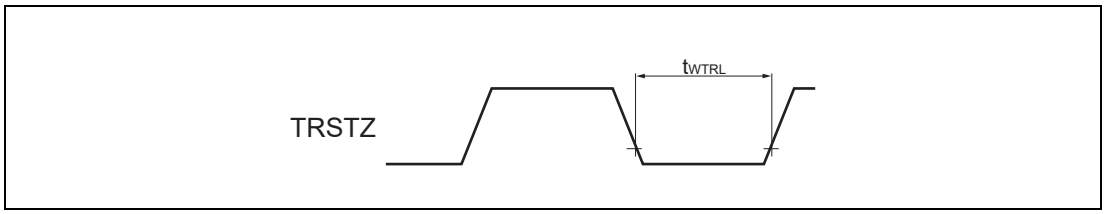


Figure 3.39 TRSTZ low level timing

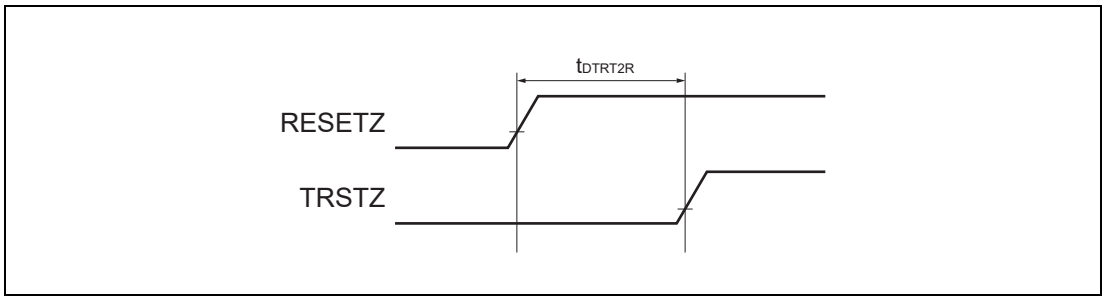


Figure 3.40 TRSTZ release timing

3.6.18 Nexus Interface Timing

Conditions:

- See **Section 3.6.1.1, General Conditions** except output buffer. Output buffer is selected 50Ω.

Table 3.42 Nexus Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK Cycle width	t_{DCKW}		50		666	ns
TCK high level width	t_{CKWH}		21			ns
TCK low level width	t_{CKWL}		21			ns
TDI setup time (vs. TCK ↑)	t_{SDI}		40			ns
TDI hold time (vs. TCK ↑)	t_{HDI}		3			ns
TMS setup time (vs. TCK ↑)	t_{SMS}		40			ns
TNS hold time (vs. TCK ↑)	t_{HMS}		3			ns
TDO delay time (vs. TCK ↓)	t_{DDO}		0		20	ns
RDYZ delay time (vs. TCK ↓)	t_{RDYZ}		0		20	ns

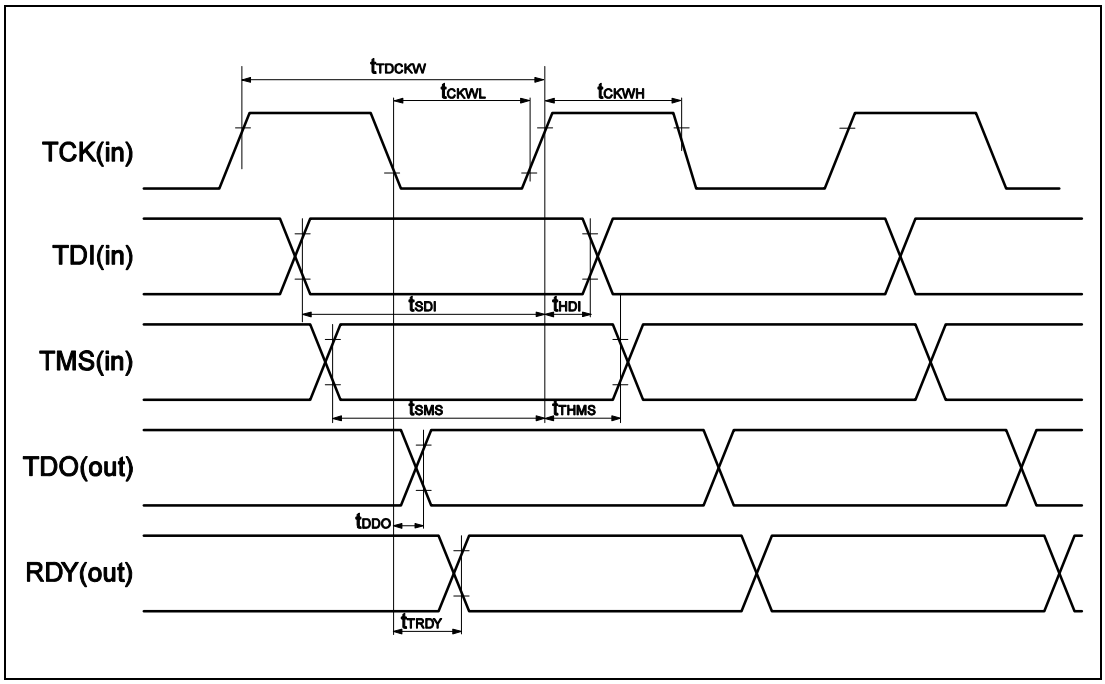


Figure 3.41 NEXUS Interface Timing

3.6.19 LPD (4pin) Interface Timing

Conditions:

- See **Section 3.6.1.1, General Conditions** except output buffer. Output buffer is selected 50Ω.

Table 3.43 LPD (4pin) Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time / LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max. 12MHz)		666	ns
LPDCLK high level width / LPDCLK low level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT high level width / LPDCLKOUT low level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (vs. LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (vs. LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (vs. LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns

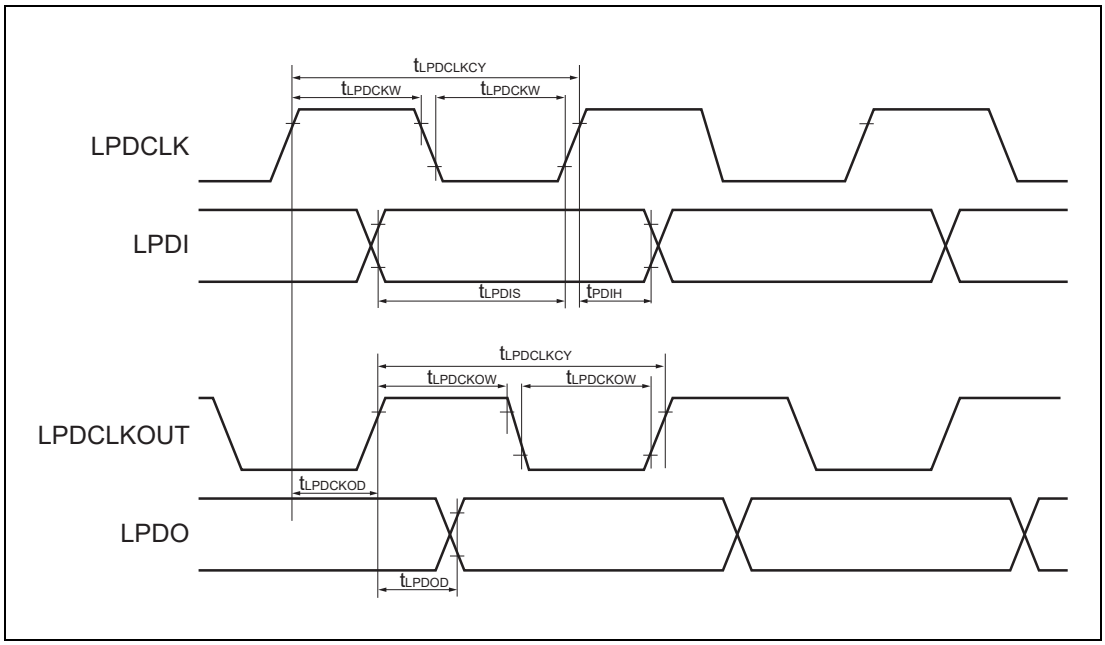


Figure 3.42 LPD (4pin) Interface Timing

3.6.20 AUDR Interface Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**
- Capacitive load (Cload) connected to output pins: 10pF

Table 3.44 AUDR Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
AUDCK cycle time	$t_{AUCKcyc}$		20			ns
AUDCK high level width	t_{AUCKH}		0.4			$t_{AUCKcyc}$
AUDCK low level width	t_{AUCKL}		0.4			$t_{AUCKcyc}$
AUDRSTZ setup time	t_{AURSTS}		12			ns
AUDRSTZ pulse width	t_{AURSTW}		5			$t_{AUCKcyc}$
AUDSYNCZ setup time	t_{AUSYS}		10			ns
AUDSYNCZ hold time	t_{AUSYH}		5			ns
AUDATA input setup time	t_{AUDTS}		8			ns
AUDATA input hold time	t_{AUDTH}		5			ns
AUDATA output delay	t_{AUDTD}				$t_{AUCKcyc}$ – 3.4	ns

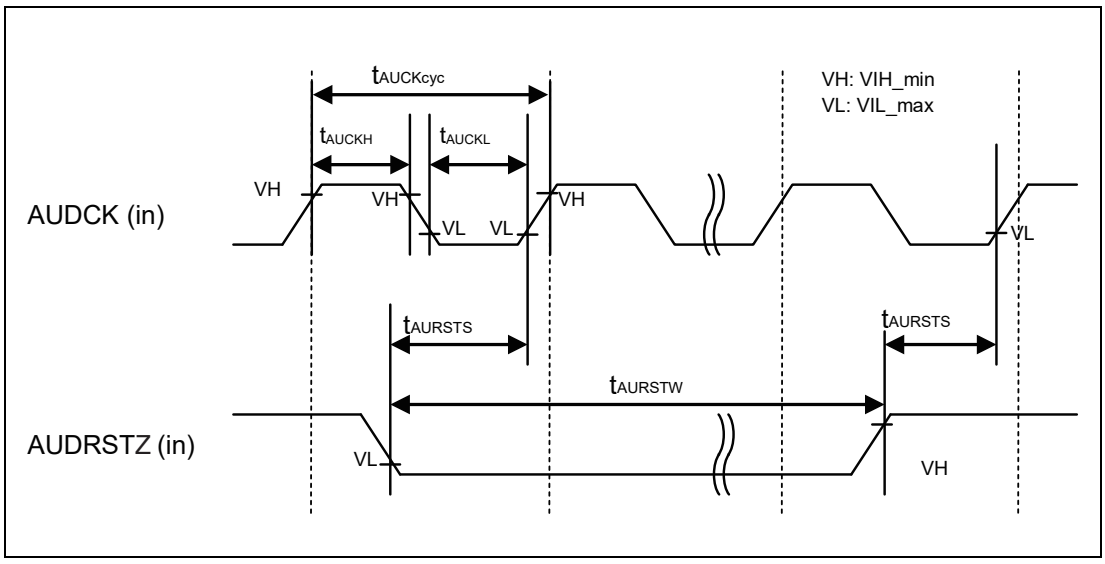


Figure 3.43 AUDRSTZ Timing

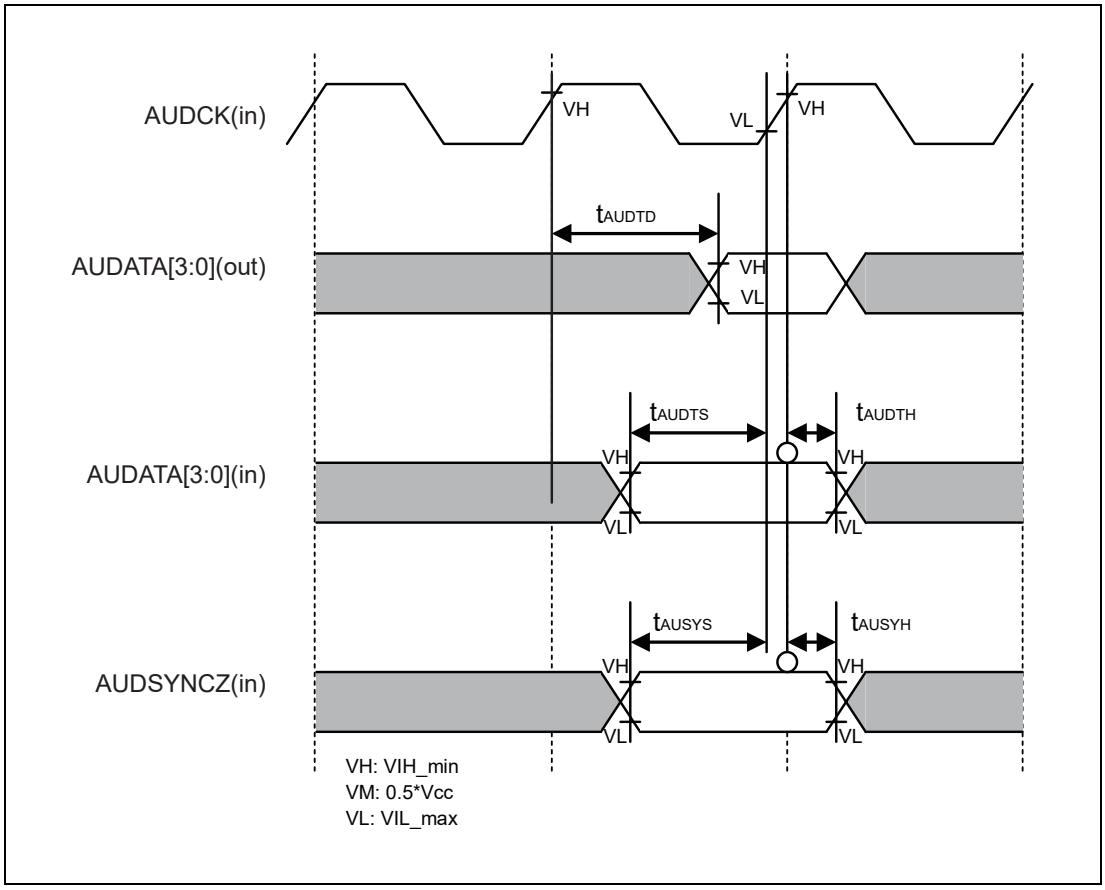


Figure 3.44 AUDR AC Timing

3.6.21 Aurora Interface Timing

Conditions:

- See **Section 3.6.1.1, General Conditions**

3.6.21.1 Aurora Interface — 1.25 Gbps baud rate

Table 3.45 Aurora Interface Operating Condition – 1.25Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential Voltage	VDIFF	*1	800		1600	mV
Rise / Fall Time	TRF	*2	60			ps
Deterministic jitter	JD				0.17	UI
Total jitter	JT				0.35	UI
Output skew	SO	*3			25	ps
Multiple output skew	SMO	*4			1000	ps
Unit interval	UI	± 100 ppm	800		800	ps
Differential output resistance	ZOD		70		130	Ω

Note 1. Peak to peak differential.
Note 2. At driver output.
Note 3. Skew at transmitter output between the differential pair.
Note 4. Skew at transmitter output between lanes of a multi-lane channel.

3.6.21.2 Aurora Interface — 2.5 Gbps baud rate

Table 3.46 Aurora Interface Operating Condition – 2.5Gbps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential Voltage	VDIFF	*1	800		1600	mV
Rise / Fall Time	TRF	*2	40			ps
Deterministic jitter	JD				0.17	UI
Total jitter	JT				0.35	UI
Output skew	SO	*3			20	ps
Multiple output skew	SMO	*4			1000	ps
Unit interval	UI	± 100 ppm	400		400	ps
Differential output resistance	ZOD		70		130	Ω

Note 1. Peak to peak differential.
Note 2. At driver output.
Note 3. Skew at transmitter output between the differential pair.
Note 4. Skew at transmitter output between lanes of a multi-lane channel.

3.6.21.3 Aurora Interface – 3.125 Gbps baud rate

Table 3.47 Aurora Interface Operating Condition – 3.125Gps baud rate

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential Voltage	VDIFF	*1	800		1600	mV
Rise / Fall Time	TRF	*2	30			ps
Deterministic jitter	JD				0.17	UI
Total jitter	JT				0.35	UI
Output skew	SO	*3			15	ps
Multiple output skew	SMO	*4			1000	ps
Unit interval	UI	± 100 ppm	320		320	ps
Differential output resistance	ZOD		70		130	Ω

Note 1. Peak to peak differential.
Note 2. At driver output.
Note 3. Skew at transmitter output between the differential pair.
Note 4. Skew at transmitter output between lanes of a multi-lane channel.

3.6.21.4 Aurora Interface – Transmitter clock Timing

Table 3.48 Aurora Interface Transmitter clock timing

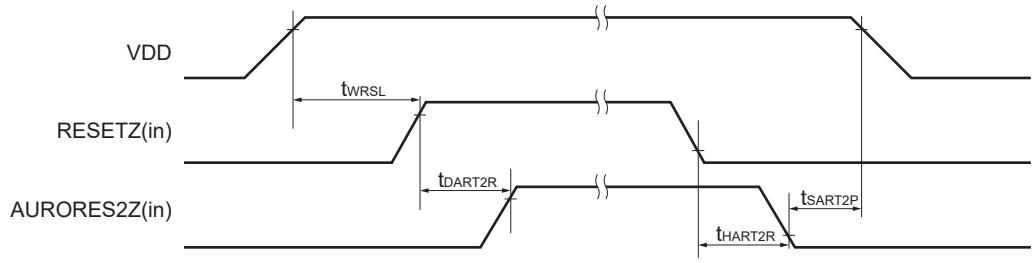
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference clock frequency	CLKP	1.25 Gbps baud rate			62.5	MHz
		2.5 Gbps baud rate			125	MHz
		3.125 Gbps baud rate			156.25	MHz
Reference clock rise time					400	ps
Reference clock fall time					400	ps
Reference clock duty cycle			45		55	%
Reference clock total jitter		*1			40	ps
Stability			50			ppm

Note 1. Peak to peak.

3.6.22 Debug Resource (Aurora, ERAM) Specific Reset Timing

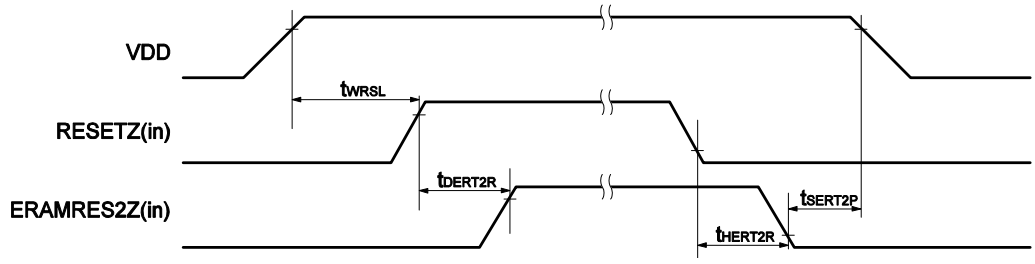
Table 3.49 Debug Resource (Aurora, ERAM) Specific Reset Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
AURORES2Z release timing delay	t_{DART2R}		0		400	ns
AURORES2Z inactive hold time	t_{HART2R}		2.4			µs
AURORES2Z setup time	t_{SART2P}		0			ns
ERAMRES2Z release timing delay	t_{DERT2R}		0		400	ns
ERAMRES2Z inactive hold time	t_{HERT2R}		2.4			µs
ERAMRES2Z assert setup time	t_{SERT2P}		0			ns
AURORES1Z release timing delay	$t_{DART2AVD}$		2.4			µs
AUROREST1Z inactive hold time	$t_{SART2AVD}$		2.4			µs
ERAMRESPDZ release timing delay	$t_{DERT2EVD}$		2.4			µs
ERAMRESPDZ inactive hold time	$t_{SERT2EVD}$		2.4			µs



Note: About the parameter t_{WRSL}, please refer to “RESETZ low pulse width” in **Section 3.6.3**

Figure 3.45 AURORES2Z AC Timing



Note: About the parameter t_{WRSL}, please refer to “RESETZ low pulse width” in **Section 3.6.3**

Figure 3.46 ERAMRES2Z AC Timing

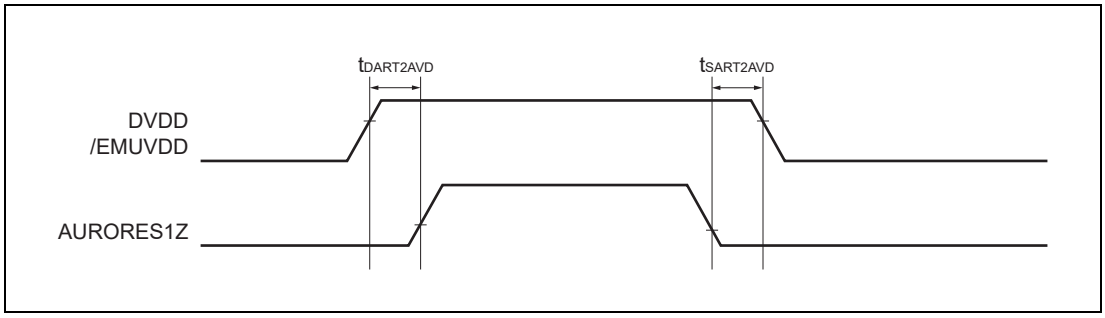


Figure 3.47 AURORES1Z AC Timing

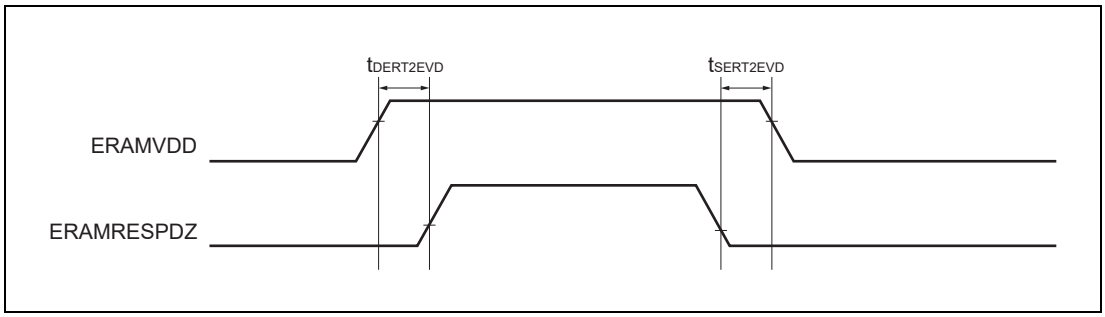


Figure 3.48 ERAMRESPDZ AC Timing

3.6.23 Debug Event Interface Timing

Table 3.50 Debug Event Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
EVTIZ input high level width	t_{WEVIH}		t_{CPUCLK} *2			ns
EVTIZ input low level width	t_{WEVIL}		t_{CPUCLK} *2			ns
EVTOZ output high level width	t_{WEVOH}	*1	16 × $t_{CPUCLK6}$ – 10	60		ns
EVTOZ output low level width	t_{WEVOL}	*1	16 × $t_{CPUCLK6}$ – 10	60		ns
MSYNZ input high level width	t_{WMSNH}		40			ns
MSYNZ input low level width	t_{WMSNL}		40			ns

Note 1. Base clock frequency is CPU operating clock frequency (f_{CPUCLK}). Typical value corresponds to the case f_{CPUCLK} = 240 MHz.

Note 2. t_{CPUCLK} indicates a period of the lowest CPU clock in the device.

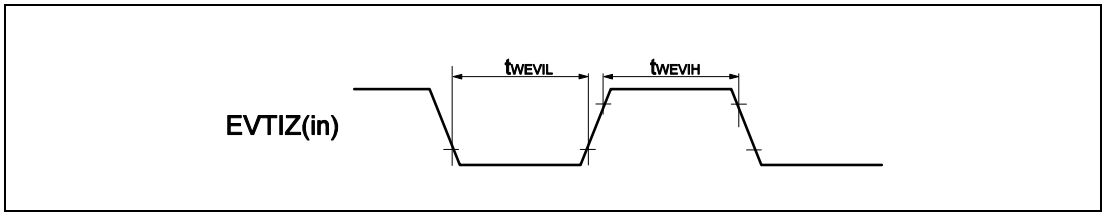


Figure 3.49 EVITZ AC Timing

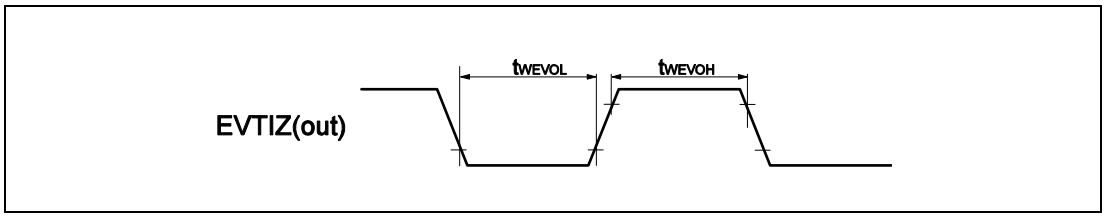


Figure 3.50 EVOTZ AC Timing

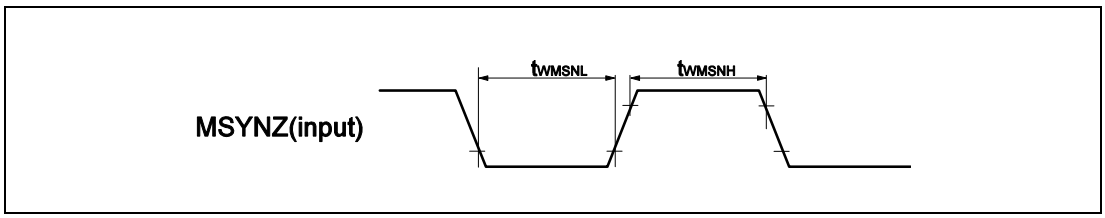


Figure 3.51 MSYNZ AC Timing

3.6.24 Flash Programming Characteristics

Conditions:

- See **Section 3.6.1.1, General Conditions** except output buffer. Output buffer is selected 50Ω.

Table 3.51 Flash FLSCI programming characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLSCI3 transfer rate		1-wired UART mode (f_{CLK_LSB} = 40MHz)			1	Mbps
		2-wired UART mode (f_{CLK_LSB} = 40MHz)			2	Mbps
FLSCI3SCKI cycle time	t_{KCYSF}	3-wired Clock Sync mode (f_{CLK_LSB} = 40MHz)	200*1			ns
FLSCI3SCKI high level width	t_{KWHSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SCKI low level width	t_{KWLSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3RXD setup time (vs. FLSCI3SCKI)	t_{SSISF}	3-wired Clock Sync mode	2 × t_{Pcyc}*2			ns
FLSCI3RXD hold time (vs. FLSCI3SCKI)	t_{HSISF}	3-wired Clock Sync mode	2 × t_{Pcyc}*2			ns
FLSCI3TXD output delay (vs. FLSCI3SCKI)	t_{DSOSF}	3-wired Clock Sync mode	2 × t_{Pcyc}*2		3 × t_{Pcyc}*2 + 36	ns

Note 1. Input the external clock data is more than 6 clocks of CLK_LSB.
Note 2. t_{Pcyc} is a period of CLK_LSB

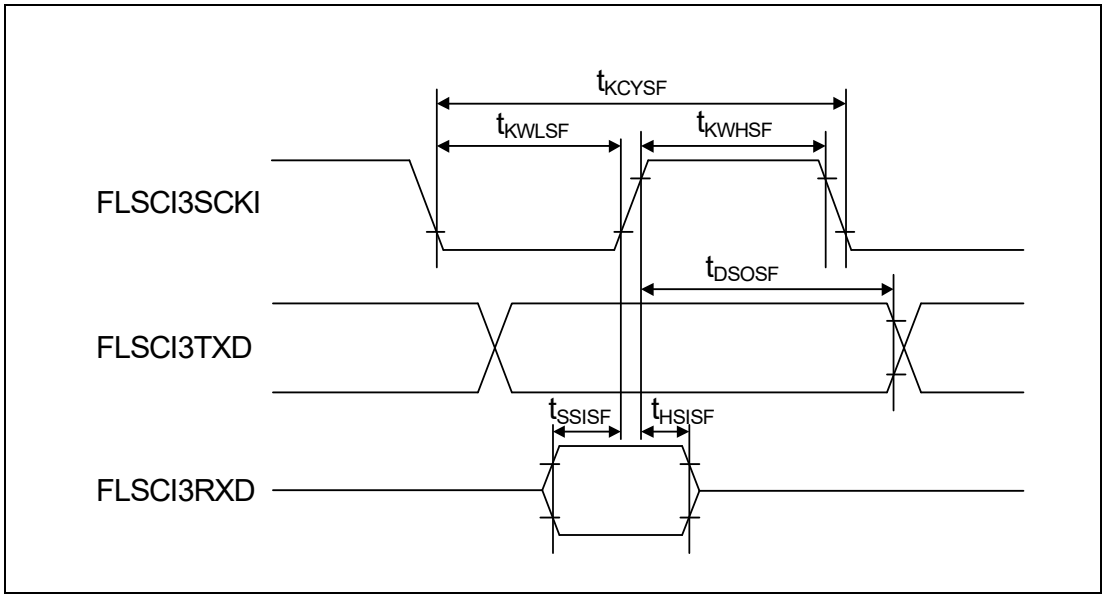


Figure 3.52 FLSCI Timing

Table 3.52 Serial Programmer Setup Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Delay time VCC ↑ & SYSVCC ↑ & IOVCC ↑ to RESETZ ↑	t_{DPOR}		t_{MOST} *1			ms
FLMD0, 1 setup time (vs RESETZ ↑)	t_{SMDR} *3		1			ms
FLMD0, 1 hold time (vs RESETZ ↑)	t_{HMDR} *3		1			ms
FLMD0 pulse input start time	t_{RP}		900			µs
FLMD0 pulse input end time	t_{RPE}				11.5	ms
FLMD0 high level width	t_{PWH}		t_{WFDH} *2			ns
FLMD0 low level width	t_{PWL}		t_{WFDL} *2			ns
FLMD0 rise time	t_R				1	µs
FLMD0 fall time	t_F				1	µs

Note 1. For t_{MOST} refer to **Section 3.3.2, Main Oscillator Characteristics**.

Note 2. For t_{PWH}/t_{PWL} refer to **Section 3.6.5, Mode Timing**

Note 3. Refer to **Section 3.6.2, Power Up/Down Timing**

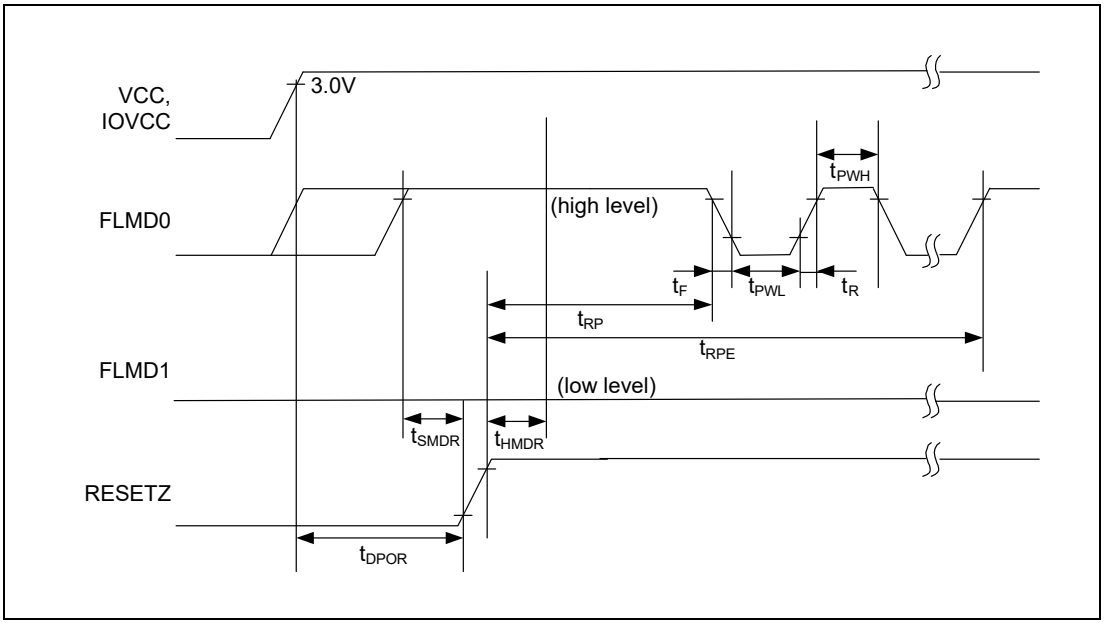


Figure 3.53 Serial Programmer Setup Timing

3.7 Analog Functions Characteristics

3.7.1 POC Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.53 POC Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection threshold voltage	V_{POC}	Rise	2.70	2.85	3.00	V
		Fall	2.70	2.80	2.90	V
POC delay time	t_{DPOC}				2	ms
POC minimum pulse width	t_{WPOC}		0.2			ms

Note 1. POC monitors SYSVCC supply voltage.

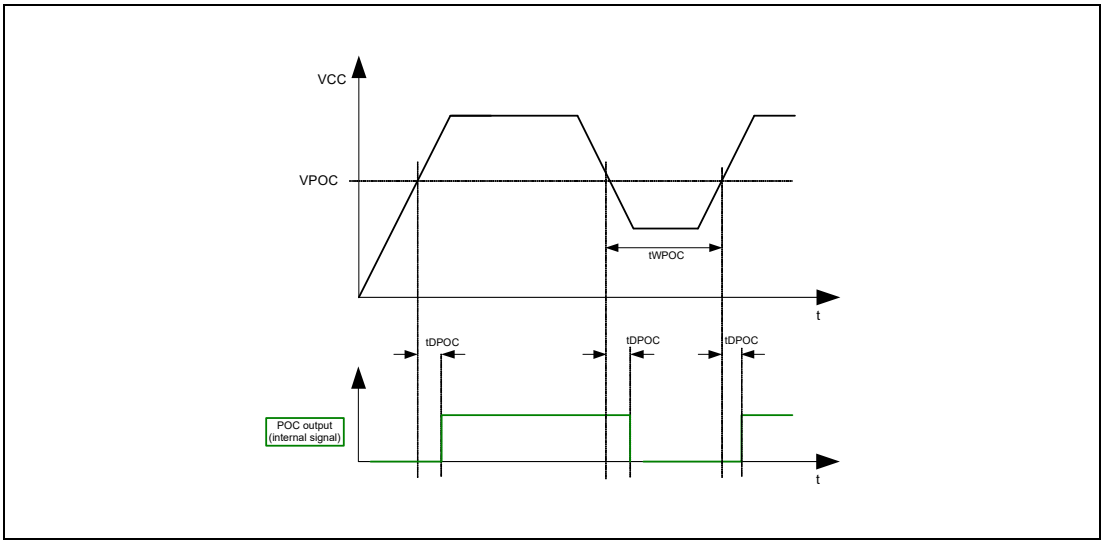


Figure 3.54 POC Characteristics

3.7.2 Core Voltage Monitor (CVM) Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.54 CVM Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CVM high detection level	V_{CVMH}		1.35	1.39	1.43	V
CVM low detection level	V_{CVML}		1.10	1.15	1.20	V
CVM delay time	t_{DCVM}		0.2		10	µs
CVM filter time	t_{FCVM}		2	4	6	µs

3.7.3 A/D Converter Characteristics

Conditions:

- Temperature range: Tjmin to Tjmax.
- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

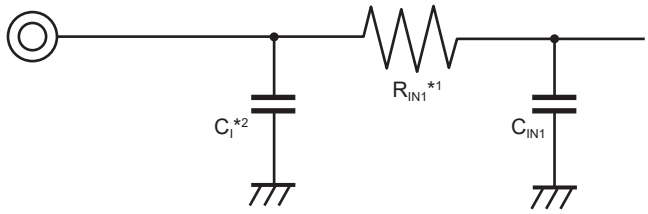
Table 3.55 ADC Characteristics

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Resolution					12		Bit
Analog supply voltages	AnVCC			3.0		3.6	V
		No guarantee of accuracy required, guarantee of operation is mandatory.		V_{POC}		3.0	V
Reference voltages	AnVREFH			3.0		AnVCC	V
		No guarantee of accuracy required, guarantee of operation is mandatory.		V_{POC}		3.0	V
Analog input voltage	V_{IAN}			AnVSS		AnVREFH	V
Operation frequency	f_{ADCLK}			8		40	MHz
A0VCC current	I_{A0VCC}					4	mA
A1VCC current	I_{A1VCC}					4	mA
A0VREFH current	$I_{A0VREFH}$					0.5	mA
A1VREFH current	$I_{A1VREFH}$					0.5	mA
Power up time w/o T&H	t_{PU}					1.0	µs
Conversion time (standard)	t_{CONV1}	t_{CONV} includes t_{SAMP}		1.0			µs
Sample time	t_{SAMP}			t_{CONV1} × (18/40)			ns
Total overall error	TOE	Include quantization error		–6.0		+6.0	LSB
Integral non-linearity error	INL			–3.0		+3.0	LSB
Differential non-linearity error	DNL	No missing code		–1.0		+2.0	LSB
Offset error	OSE			–5.5		+5.5	LSB
Full-scale error	FSE			–5.5		+5.5	LSB
Self-diagnosis accuracy	TOEdiag	A/D Conversion Circuit Diagnosis on single ADC*2	Include quantization error	–8.0		+8.0	LSB
		Pin Level Diagnosis from I/O*1		–40.0		+40.0	LSB
Equivalent input resistance w/o T&H	RIN1*3	PIN – RRanp: 96.7% PIN – 12 bit SAR – ADC: 3.3%				3.1	kΩ
Equivalent input sampling capacitance w/o T&H	CIN1					5.8	pF
TDE switch resistance	RTDE*3	ADCFnTDCR.TDE = 0		100		600	Ω

Note 1. The accuracy of the conversion result for the applied diagnostic voltage could be out of specification in case injected current is injected to the pin of this channel

Note 2. For details to operate “A/D Conversion Circuit Diagnostic Function” refer to CAUTION on RH850/P1x-C Group User's Manual: Hardware **A/D Section 27.4.7.2,Conversion Circuit Diagnostic Function**

Note 3. RIN1 includes RTDE. For detail of TDE switch, see RH850/P1x-C Group User's Manual: Hardware **Figure 27.11, diagnosis circuits**.



Note 1. RIN1 includes RTDE. For detail of TDE switch, see RH850/P1x-C Group User's Manual: Hardware Figure 27.11, diagnosis circuits.

Note 2. For CI data, see **Section 3.3.6, IO Capacitances**.

Figure 3.55 Equivalent Circuit

3.7.4 Temperature Sensor Characteristics

Conditions:

- Supply voltage range: Refer to **Section 3.3.1, Supply Voltage Characteristics**.
- System control supply voltage range: SYSVCC = 3.0V to 3.6V.
- EnVSS = AnVSS = OSCVSS = VSS.
- Reference ground potential: VSS = 0 V.

Table 3.56 Temperature Sensor (TS) Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature range	TTS1	*2	Tjmin		Tjmax*1	°C
Temperature accuracy*3	ACCTS1		–3		+3	°C
Temperature update period	t_{TSUP}				10	ms
Stand-by return time	t_{TSSB1}				200	µs
Operation frequency	f_{OTSCLK}*4		36		40	MHz

Note 1. Value of Tjmax is device dependent, see par. **Table 3.5 Operational Condition**.

Note 2. The operation of Temperature Sensor itself and ICUMC reaction for thermal attack between Tjmax and Tj=165degC is guaranteed, but by design only and will not be tested.

Note 3. For an absolute temperature within the given accuracy an offset has to be considered. The offset is given by trimming data in the register OTS0COEFFRA to OTS0COEFFRC.

Note 4. For f_{OTSCLK}, refer to RH850/P1x-C Group User's Manual: Hardware **Section 11.1.3, Clock Supply**.

3.7.5 Flash Characteristics

(1) Code Flash

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.57 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLK_LSB}		2		40	MHz
Operation voltage	VDD		1.20		1.35	V
	VCC		3.0		3.6	V
Number of rewrites*1	CWRT	Data retention of 20 years*2	1000			times
Programming temperature (Tj)	TPRG		Tjmin*3		Tjmax*3	°C

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. This is the case when the average Ta is 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. Refer to **Table 3.5 Operational Condition**

Table 3.58 Programming Characteristics

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Programming time*1		f_{CLK_LSB} ≥ 20 MHz CWRT < 100 times	256 B		2	6	ms
		f_{CLK_LSB} ≥ 20 MHz CWRT ≥ 100 times	256 B		2.4	7.2	ms
		f_{CLK_LSB} ≥ 20 MHz	8 KB		16	96	ms
		f_{CLK_LSB} ≥ 20 MHz	32 KB		64	384	ms
		f_{CLK_LSB} ≥ 20 MHz CWRT < 10 times Tj = 10 – 80 °C	512 KB		0.8	3.6	s
		f_{CLK_LSB} ≥ 20 MHz CWRT ≥ 100 times	512 KB		1.03	6.15	s
Erasure time		f_{CLK_LSB} ≥ 20 MHz	8 KB		47	235	ms
		f_{CLK_LSB} ≥ 20 MHz	32 KB		169	576	ms
		f_{CLK_LSB} ≥ 20 MHz CWRT < 10 times Tj = 10 – 80 °C	512 KB		2.3	4.5	s
		f_{CLK_LSB} ≥ 20 MHz CWRT ≥ 100 times	512 KB		2.71	8.4	s

Note 1. Timings are based on availability of write buffer according to programmed block size of either 256 B, 8 KB or 32 KB.

Table 3.59 Program/Erase suspend latency Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Program Suspend Latency*1		f_{CLK_LSB} ≥ 20 MHz			120	µs
Erase Suspend Latency*1*2		Suspension-Priority (1st suspension for a pulse application) f_{CLK_LSB} ≥ 20 MHz			120	µs
		Suspension-Priority (2nd suspension for a pulse application) f_{CLK_LSB} ≥ 20 MHz			1.7	ms
		Erasure-Priority f_{CLK_LSB} ≥ 20 MHz			1.7	ms
Program Resume Latency*1		f_{CLK_LSB} ≥ 20 MHz			50	µs
Erase Resume Latency*1		Suspension-Priority (after 1st suspension) f_{CLK_LSB} ≥ 20 MHz			1.7	ms
		Suspension-Priority (after 2nd suspension) f_{CLK_LSB} ≥ 20 MHz			80	µs
		Erasure-Priority f_{CLK_LSB} ≥ 20 MHz			80	µs

Note 1. The target value is the hardware suspend time. A possible software overhead is not considered.

Note 2. FACI command (Code Flash Erase) with erase counter update cannot be suspended until erase counter update has finished.

(2) Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception

Table 3.60 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLK_LSB}		2		40	MHz
Operation voltage	VDD		1.20		1.35	V
	VCC		3.0		3.6	V
Number of rewrites[*1]	CWRT	Data retention 20 years[*2]	125 k			times
		Data retention 3 years[*2]	250 k			times
Programming temperature (Tj)	TPRG		Tjmin[*3]		Tjmax[*3]	°C

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 168 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. This is the case when the average Ta is 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Note 3. Refer to **Table 3.5 Operational Condition**.

Table 3.61 Programming Characteristics

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Programming time		f_{CLK_LSB} ≥ 20 MHz	4 B		0.16	1.7	ms
Erasure time		f_{CLK_LSB} ≥ 20 MHz CWRT < 10 times Tj = 10 – 80 °C	8 KB		216	640	ms
		f_{CLK_LSB} ≥ 20 MHz	64 B		1.7	10	ms
Blank check time		f_{CLK_LSB} ≥ 20 MHz	4 B			30	µs

Table 3.62 Program/Erase suspend latency Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Program Suspend Latency*1		f_{CLK_LSB} ≥ 20 MHz			120	µs
Erase Suspend Latency*1		Suspension-Priority (1st suspension for a pulse application) f_{CLK_LSB} ≥ 20 MHz			120	µs
		Suspension-Priority (2nd suspension for a pulse application) f_{CLK_LSB} ≥ 20 MHz			300	µs
		Erasure-Priority f_{CLK_LSB} ≥ 20 MHz			300	µs
Program Resume Latency*1		f_{CLK_LSB} ≥ 20 MHz			50	µs
Erase Resume Latency*1		Suspension-Priority (after 1st suspension) f_{CLK_LSB} ≥ 20 MHz			300	µs
		Suspension-Priority (after 2nd suspension) f_{CLK_LSB} ≥ 20 MHz			70	µs
		Erasure-Priority f_{CLK_LSB} ≥ 20 MHz			70	µs

Note 1. The target value is the hardware suspend time. A possible software overhead is not considered.

3.8 Thermal Characteristics

The chip junction temperature TJ, max must never be exceeded. Please refer to the device and package dependent specification of TJ, max below.

It is the responsibility of the user to make sure the maximum junction temperature is not exceeded.

The actual TJ depends on the power dissipation and the thermal characteristics of the application. Please refer to chapter **Section 3.5, Supply Current Characteristics**, how to calculate the power dissipation. Power dissipation can be influenced by choosing several parameters. The thermal characteristic of the application environment need to be considered throughout the design process. The following sub-chapters describe metrics to consider this.

3.8.1 Junction-to-Board Resistance (Ψjb)

The simplest method to determine the actual chip temperature is to use the single resistance metric of Ψjb.

The following equation may be used:

$$T_j = T_b + (P_{TOTn} \times Y_{jb})$$

with:

- T_J: chip junction temperature in [°C]
- T_b: board temperature (according to JEDEC standard JESD51-2A) in [°C]
- P_{tot}: total power consumption (refer to **Section 3.5, Supply Current Characteristics**) in [W]
- Ψjb: thermal resistance between junction and board in [°C/W]

This simple metric considers the test board properties in a natural convection environment. The thermal resistance is derived from a defined test fixture (JEDEC) or simulation of such test fixture using a 3D simulation with a detailed model.

Table 3.63 Thermal Characteristics - Junction to Board Resistance (Ψjb)

Device	Symbol*1	Package	Condition*2*3	MAX Value	Unit
P1M-C	Ψjb32	BGA292	JEDEC, JESD51-9, TJ, max = 150°C	13.2*5	°C/W
	Ψjb34	BGA156	JEDEC, JESD51-9, TJ, max = 150°C	13.3	°C/W
	Ψjb33	LQFP144	JEDEC, JESD51-7, TJ, max = 160°C	26.7*4	°C/W
P1H-C (4MB)	Ψjb41	BGA292	JEDEC, JESD51-9, TJ, max = 150 °C	10.0*5	°C/W
	Ψjb42	BGA156	JEDEC, JESD51-9, TJ, max = 150 °C	10.2	°C/W
P1H-C (8MB)	Ψjb51	BGA292	JEDEC, JESD51-9, TJ, max = 150 °C	8.2*5	°C/W
P1H-CE	Ψjb71	BGA404	JEDEC, JESD51-9, TJ, max = 150 °C	5.1*5	°C/W

Note 1. In case of LQFP, Ψjb is a thermal resistance between junction and board surface at tip of LQFP pin. In case of BGA, Ψjb is a thermal resistance between junction and board surface beneath center of package

Note 2. Thermal resistance is based on a solder saturation (solder wetting) >= 50 %.

Note 3. Total power of Digital IO Pins and Analog Input Pins is calculated by assuming 60mW for P1M-C and P1H-C.
Note 4. Rth Tolerance: +2degC/W, L/F: standard L/F
Note 5. Data includes max Rth Tolerance

Section 4 Package

4.1 Package Line Up

RH850/P1x-C Product	P1M-C 144	P1M-C 156, P1H-C 156	P1M-C 292, P1H-C 292	P1H-CE
Renesas code	PLQP0144LB-A	PLBG0156JB-A	PRBG0292GC-A	PRBG0404GA-A
JEITA code	P-LFQFP144-16x16-0.40	P-FBGA156-10x10-0.65	P-FBGA292-17x17-0.80	P-FBGA404-19x19-0.80
Name	LQFP	FBGA	FBGA	FBGA
Terminal count	144	156	292	404
Terminal pitch (mm)	0.4	0.65	0.8	0.8
Dimensions (mm)	16x16	10x10	17x17	19x19
Mass (g)[TYP]	0.9	0.37	0.95	1.1
Mounting height (mm)[MAX]	1.7	1.7	1.9	1.9
Terminal material - Base	Cu alloy	Sn-Ag-Cu	Sn-Ag-Cu	Sn-Ag-Cu
Environment	Lead free	Lead free	Lead free	Lead free

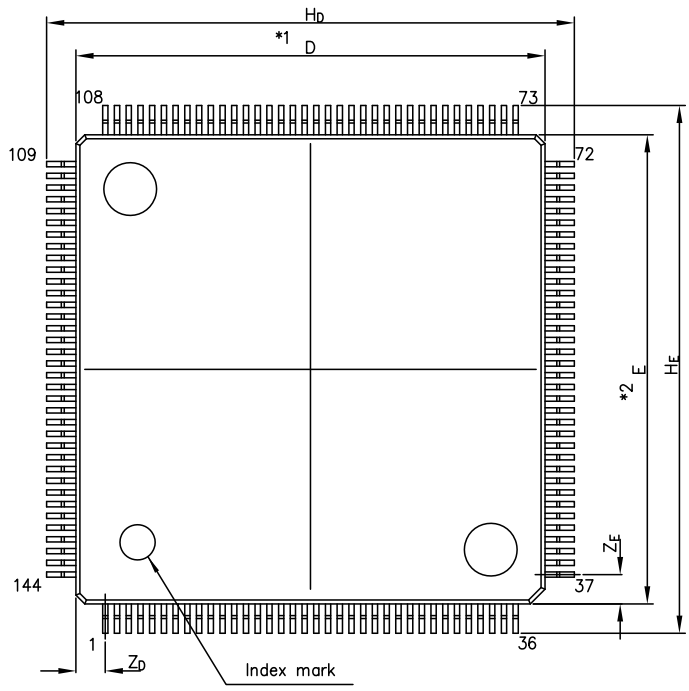
4.2 Package Outline

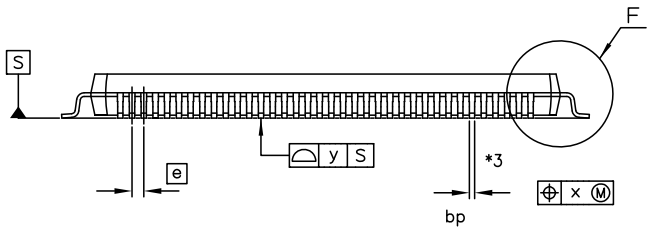
4.2.1 LQFP Package Drawing

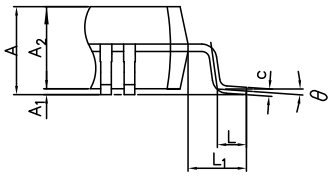
- **Figure 4.1** shows LQFP outline.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-16x16-0.40	PLQP0144LB-A	——	0.9g

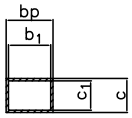
Unit: mm







Detail F



Terminal cross section

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

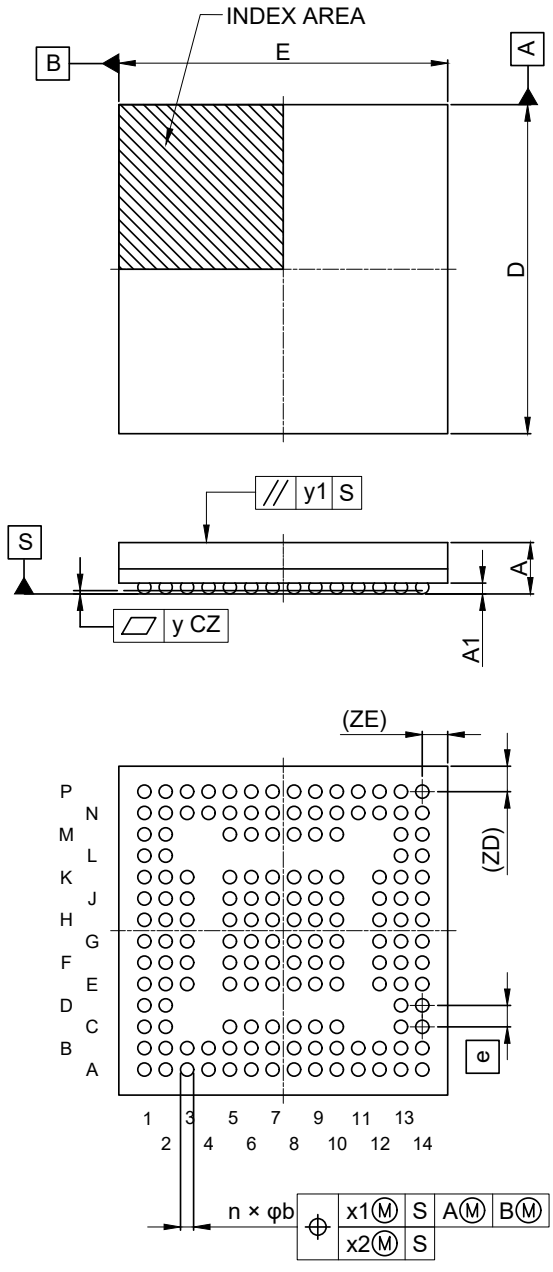
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.9	16.0	16.1
E	15.9	16.0	16.1
A2	——	1.4	——
HD	17.8	18.0	18.2
HE	17.8	18.0	18.2
A	——	——	1.7
A1	0.05	0.10	0.15
bp	0.13	0.18	0.23
b1	——	0.16	——
c	0.09	0.145	0.20
c1	——	0.125	——
θ	0°	——	8°
e	——	0.4	——
x	——	——	0.07
y	——	——	0.08
ZD	——	1.0	——
ZE	——	1.0	——
L	0.35	0.5	0.65
L1	——	1.0	——

Figure 4.1 LQFP outline

4.2.2 FBGA (156pin) Package Drawing

- **Figure 4.3** shows FBGA (156pin) outline.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA156-10x10-0.65	PLBG0156JB-A	0.37



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	9.92	10.00	10.08
E	9.92	10.00	10.08
A	—	—	1.70
A1	0.21	0.26	0.31
e	—	0.65	—
b	0.40	0.45	0.50
x1	—	—	0.15
x2	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
n	—	156	—
ZD	—	0.775	—
ZE	—	0.775	—

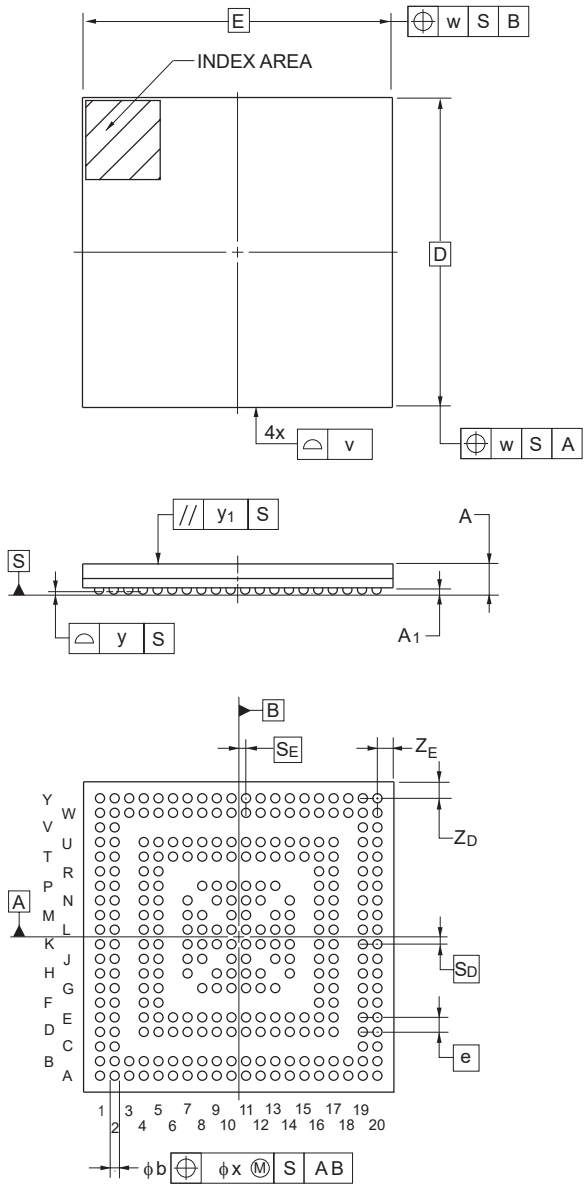
Figure 4.3 FBGA (156pin) outline

4.2.3 FBGA (292pin) Package Drawing

- **Figure 4.4** shows FBGA (292pin) outline.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-FBGA292-17x17-0.80	PRBG0292GC-A	T292F1-80-GNP	—

Unit: mm



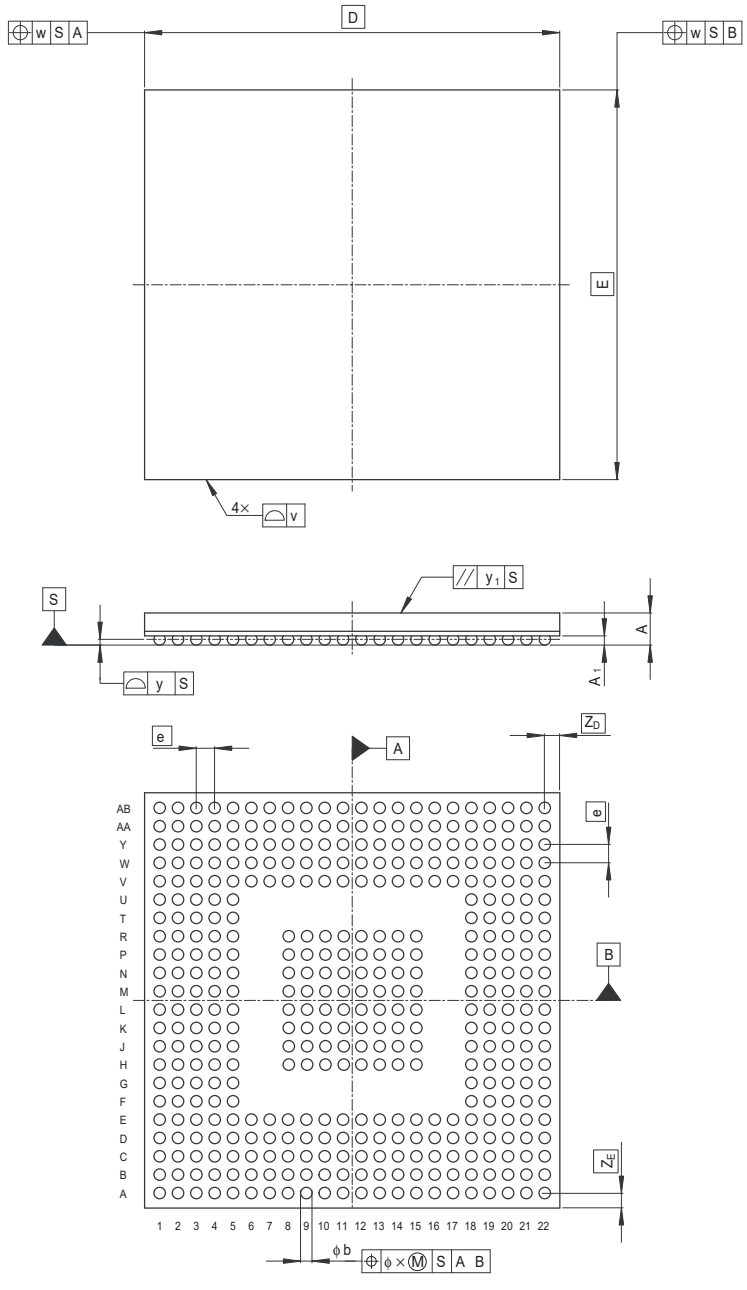
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	—	17.00	—
E	—	17.00	—
A	—	—	1.90
A_1	0.30	0.35	0.40
e	—	0.80	—
b	0.50	0.55	0.60
x	—	—	0.12
y	—	—	0.10
y_1	—	—	0.20
Z_D	—	0.90	—
Z_E	—	0.90	—
v	—	—	0.15
w	—	—	0.20
S_D	—	0.40	—
S_E	—	0.40	—

Figure 4.4 FBGA (292pin) outline

4.2.4 FBGA (404pin) Package Drawing

- **Figure 4.5** shows FBGA (404pin) outline.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-FBGA404-19x19-0.80	PRBG0404GA-A	—	1.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	19	—
E	—	19	—
v	—	—	0.15
w	—	—	0.2
A	—	—	1.9
A_1	0.35	0.4	0.45
e	—	0.8	—
b	0.45	0.5	0.55
x	—	—	0.08
y	—	—	0.1
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	1.1	—
Z_E	—	1.1	—

Figure 4.5 FBGA (404pin) outline

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2025.12.19	-	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

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