RH850/U2C

Renesas microcontroller

Section 1 Overview

The RH850/U2C8-EVA, U2C8, U2C4 and U2C2 are products of the single-chip microcontroller RH850 series from Renesas Electronics.

This section gives an overview of the RH850/U2C8-EVA, U2C8, U2C4 and U2C2.

1.1 Outline

This RH850/U2C is a 32-bit single-chip microcontroller with multiple CPUs, Code Flash, Data Flash, RAM modules, DMA controllers, A/D converters, timer units and many communication interfaces that are used in the automotive applications. RH850/U2Cx conforms to the Automotive Safety Integrity Level (ASIL) that is highly demanded in the recent automotive field (ASIL D level).

RH850/U2C main features are as follows:

(1) **RH850 multi-core CPU**

This microcontroller contains multi RH850G4KH cores support RISC-type instruction sets and have significantly improved the instruction execution speed with basic instructions (one clock cycle per instruction) and the optimized 5-stage pipeline configurations. Furthermore, this product also supports multiplication instructions using a 32-bit hardware multiplier, saturated product-sum operation instructions, and bit manipulation instructions as instructions best suited for various fields.

Two-byte basic instructions and high-level language instructions improve object code efficiency for the C compiler and reduce the program size. Furthermore, this product is suited for advanced real-time control applications by offering a high-speed response time including the processing time of the onchip interrupt controller.

(2) **On-Chip Code Flash and Data Flash**

This microcontroller has high-speed Code Flash from which CPU can fetch the instructions and the constant data. Code Flash with a capacity of up to 8 MB can be reprogrammed when the chip is implemented in the application system.

This chip also has Data Flash capable of EEPROM emulation with a capacity of up to 384 KB and 64 KB exclusively for ICUMHB.

(3) **Rich peripheral functionality**

This microcontroller supports common communication interfaces such as SPI as well as automotive-oriented communication interfaces such as Ethernet, Ethernet 10base-T1S, FlexRay, CAN-FD, CANXL, LIN, SENT and PSI5. As internal peripheral modules, this microcontroller incorporates A/D Converter, System Timer, Generic Timer Module, and a dedicated Peripheral Interconnection module which connects the functionalities of these peripherals.

(4) **Functional Safety support**

This microcontroller includes several dedicated functionalities such as Dual-Core Lockstep configuration for CPU, the memory protection with ECC/EDC on data and the address feedback mechanism, the bus protection with ECC/EDC on data and address, the peripheral module protection, and clock monitors to support the functional safety standard (ISO26262) required in the automotive applications.

(5) **Security support**

This microcontroller supports various security features. The Intelligent Cryptographic Unit - Master (ICUMHB) has a dedicated secure CPU (RH850 G3K) and some secure peripherals such as AES engines, a public key cryptography coprocessor, an engine that supports a HASH function based on SHA and Random Number Generator (RNG). This microcontroller also realizes the HW-level domain separation between non-secure and secure domains. The internal resources such as Code and Data Flash can be assigned to either a non-secure or secure domain, and the secure domain is protected against non-secure accesses by the HW mechanism. This microcontroller also has the protection scheme for debug and test functionality.

1.2 Features

Item	Features
Pin and Port Functions	• Most of the digital pins have selectable functionalities and a general purpose I/O port • Selectable drivability for output pins • Selectable pull-up/pull-down/none for input pins • Selectable Inversion/non-inversion for output pins • General-purpose I/O ports can be accessed per-pin basis by multiple CPUs without mutual exclusion • General-purpose I/O ports can operate in the following three different modes: – Port mode • The pin operates as a general-purpose I/O port. • The selection between input or output is selected by S/W via control bits. – S/W I/O control alternative mode • The pin is operated by an alternative function in S/W I/O control alternative mode • The selection between input or output is selected by S/W via control bits. – Direct I/O control alternative mode The pin is operated by an alternative function in direct I/O control alternative mode In contrast to S/W I/O control alternative mode, input/output is directly controlled by the alternative function in this mode.
CPU Subsystem	• G4KH1.1 CPU – High-performance 32-bit architecture for embedded control – 32-bit internal data bus – Thirty-two 32-bit general purpose registers – RISC-type instruction set • Long/short type load/store instructions • Three-operand instructions • Instruction sets based on the C language – CPU operating modes: User mode / Supervisor mode – Address space: 4-GB linear address space for data and instructions • Floating Point Unit (FPU) – Each CPU has its own FPU. Supports single precision (32 bits) and double precision (64 bits). – Supports IEEE754-compliant data types and exceptions. – Rounding modes: Nearest, 0 direction, +∞ direction and -∞ direction – Handling of non-normalized numbers: Truncation to zero / IEEE754-compliant exception • Interrupt Handling – 16-level interrupt priority that can be specified for each channel – Two methods of interrupt handler address calculation: • Direct vector method • Table reference method – PUSHSP and POPSP instructions for high-speed context switch – Support for high-speed context save on interrupts by using the register bank feature – Support for restoration from the register bank using a dedicated instruction (RESBANK)

Item	Features
	• Protection Mechanisms – Memory Protection Unit (MPU) protects memory regions against illegal accesses by software. (24 areas settable) – PE Guard (PEG) protects Local RAM and internal peripheral registers against illegal accesses by external bus masters. – Cluster RAM Guard (CRG) protects Cluster RAM regions against illegal accesses by all bus masters. • Instruction Cache – Each CPU has its own instruction cache for the Code Flash. – 2-way cache – Cache line size is 16 bytes. • Local RAM – Each CPU has its own Local RAM. • Cluster RAM – Each CPU can access Cluster RAM. • Inter-processor Communication and Mutual Exclusion Mechanisms – Inter-processor interrupt registers (IPIR) – Barrier-Synchronization (BARR) – Time Protection Timer (TPTM) – Three types of atomic instructions • CAXI (Compare and Exchange for Interlock) • SET1, CLR1 and NOT1 for atomic one-bit set and clear • LDL (Load Linked) and STC (Store Conditional)
Operating Modes	This MCU has multiple operating modes, which can be selected by the pins and option byte settings. • Normal Operating Mode : After release from the reset state, an instruction fetch is carried out from the user area. • User Boot Mode : After release from the reset state, an instruction fetch is carried out from the user boot area. • Serial Programming Mode: After release from the reset state, the MCU boots up from the on-chip boot program and starts connection in the specified protocol for flash programming.
Interrupt Functions	1 non-maskable interrupt (NMI pin) 1 FE level interrupt Maskable interrupts, See the RH850/U2C Group User's Manual: Hardware Section 6.2.1, Outline. Simultaneous distribution of interrupt sources to multiple cores (each CPU) • Applicable sources: non-maskable interrupt (NMI pin), FE level interrupt, 32 high-speed maskable interrupts External interrupt input function (IRQ pins) Software interrupt function (SINT) Inter-processor interrupt function (IPIR) 16-level priority specifiable for maskable interrupts For RH850G4KH exceptions, see the RH850/U2C Group User's Manual: Hardware Section 3.2.2.3, Exceptions and Interrupts.

Item	Features
Direct Memory Access	• Two types of DMA controller: DTS and sDMAC • DTS – Transfer information is stored in the dedicated SRAM (DTSRAM) – Up to 128 channels – Selectable transfer size: 1, 2, 4, 8, 16 bytes – 64-bit (8byte) × 2-burst transfer when 16byte transfer size – Dual-address transfer mode – Address reloading function – Chain transfer function – Three transfer modes settable • Single transfer • Block transfer 1 (specified by the number of transfers) • Block transfer 2 (specified by address count) – Transfer target • On-chip memory • On-chip peripheral modules (excluding DTS and sDMAC) – Transfer requests can be set by interrupt sources and the software. • sDMAC – Transfer information is stored in the sDMAC control registers and can be loaded from the dedicated descriptor memory. – Up to 32 channels can be active at the same time. – Address space: 4 GB – Source and destination addresses are 32-bit wide – Selectable transfer size: 1, 2, 4, 8, 16, 32, 64 bytes – Supports scatter/gather and descriptor function. – Parallel reads and writes (fly-by) – Address mode: Dual address mode – Transfer request: Two request modes are available. Requests are triggered by on-chip modules and auto request. – Bus mode: Each channel can be set either normal speed mode or slow speed mode. – Arbitration mode can be set either fixed priority arbitration mode or round-robin arbitration mode between transfer channels. – Interrupt request: CPU interrupts from sDMAC are triggered by the following three factors. • Termination of the descriptor step • Termination of a data transfer • Occurrence of an address error
Reset Controller	7 reset functions • Power On Reset • System Reset 1 • System Reset 2 • Application Reset • DeepSTOP Reset • Module Reset • JTAG Reset External Reset output pin: $\overline{\text{RESETOUT}}$ Automatic RAM initialization after reset
Power Supply	• This product can be operated with the power management IC with three output voltages (5.0 V, 3.3 V, VDD) and with two output voltages (5.0 V/3.3 V, VDD). VDD can also be supplied by internal regulator (eVR), not by the power management IC directory. See **Section 1.5, Differences in the Specifications of RH850/U2C** for detail.
Clock Controller	• Main Oscillator (Main OSC) with an oscillation frequency of 8/16/20/24 MHz • SubOSC with an oscillation frequency 32.768KHz • High and low speed internal oscillators • PLL to generate high speed internal clocks by multiplying Main OSC input • Software-configurable external clock outputs

Item	Features
Standby Controller	• RUN mode – RUN mode is a normal operating mode where the CPU is operation and all of other modules can operate. The CPU can enter “HALT” state by executing the “HALT” instruction to stop its operation in this mode. • STOP mode: – STOP mode is a chip-level stand-by mode in which the clock supply to a certain clock domain can be stopped. • DeepSTOP mode – DeepSTOP mode is a chip-level stand-by mode in which further reduction of power consumption is possible than STOP mode. In addition to the clock supply stop, the power supply to the isolated area is switch off. • Cyclic RUN mode – Cyclic RUN mode is a low-power operation mode in which limited modules can operate at low speed. • HALT mode: – When the HALT instruction is executed, CPU transits to HALT mode and stops instruction execution. – Each CPU can be controlled individually. – CPU returns from this state by the occurrence of a reset, interrupt, or exception. • Module standby: – This function stops the clock for peripheral modules to reduce the power consumption in accordance with register settings.
Low-Power Sampler	Support checking the digital input ports and analog input ports to monitor the external input without consuming CPU resources.
Serial Flash Memory Interface	• Connection to one serial flash memory device is possible. • Selectable data bus sizes are 1 bit, 2 bits, or 4 bits. • 4-Gbyte address space • A built-in read cache enables efficient data reception (64-bit line × 16 entries). • Arbitrary bit rate settable by the on-chip baud rate generator
Multimedia Card Interface	• Compliant with JEDEC STANDARD JESD84-A441 (neither DDR mode nor 1.8-V operation is supported). • Supports 1-/4-/8-bit MMC bus widths. • Supports the backward-compatible mode. • High-speed mode is supported. • Supports the single data rate. • MMC Clock frequency = MMCA module clock frequency/2k (k = 1 to 10). • Supports block transfer. • Supports boot operation. • Supports high priority interrupts (HPI). • Supports background operation. • Interrupt requests: normal operation and error/timeout. • DMA transfer requests: buffer write and buffer read.
MSPI	• Chip select: Up to 8 for each channel • Master mode and slave mode selectable • Clock polarity, clock / data phase: Phase of clock and data selectable chip select output signals with phase of clock and data settable. • Transmission rate: Up to 20Mbps
RLIN3	• Protocol: LIN Specification Package Revision 1.3, 2.0, 2.1, 2.2, and SAEJ2602 • Three operating modes – LIN master mode – LIN slave mode – UART mode (half-duplex, full-duplex) • Arbitary bit rate settable by the on-chip baud rate generator • LIN self-test mode with internal data loopback

Item	Features
RI3C	• I3C mode – Operation Mode: • Master (Main Master/Secondary Master) mode and Slave mode selectable – Data handler: Master and Slave FIFO buffer transfer – Communication Protocol • SDR (I3C Single Data Rate) Mode • Legacy I2C Message Transfer rate up to 400 kbps – In-Band Interrupt • Slave Interrupt Request • Master Ship Request (Secondary Master only) – Address Format: 7-bit Address – Address Detection: Slave and Broadcast Address – Clock Stalling: Clock Stalling capability – Timing Control: Synchronous and Asynchronous Timing Control • I2C mode – Operation Mode: Master mode and Slave mode selectable – Data Handler: Single buffer transfer – Communication Protocol • I2C Bus format • Standard-mode (Sm) : 0 to 100 kbit/s • Fast-mode (Fm) : 0 to 400 kbit/s – Address Format :7-bit address or 10-bit address – Address Detection • Slave address (Static Address) (Max 3 Address) • General call address • Device ID • 10-bit slave addressing – Clock Stretching capability – Noise-Filter: Digital Noise-Filter
RS-CANFD	• Classical CAN mode – Conforming to CAN-FD ISO-11898-1 (2015) – Transfer speed: Up to 1 Mbps – Reception filtering • CAN-FD mode – Conforming to CAN-FD ISO 11898-1 (2015) – Transfer speed: Up to 8 Mbps – Reception filtering
CANXL	• Conform with ISO11898-1:2015 and CiA610-1. • Transmission and reception message filtering. • 1 priority queue, 8 TX FIFO queues, 8 RX FIFO queues. • Classical CAN mode: – Data frame: up to 8 bytes. – Communication speed: up to 1 Mbps. • CAN FD mode: – Data frame: up to 64 bytes. – Communication speed: up to 1 Mbps for nominal bit rate, up to 8 Mbps for data bit rate. • CAN XL mode: – Data frame: up to 2048 bytes. – Communication speed: up to 1 Mbps for nominal bit rate, up to 20 Mbps for data bit rate.

Item	Features
FlexRay	• Conforming to Protocol Specification 2.1 • Buffer size: 8 KB (up to 128 message buffers) • Message filter: ID filter, channel filter, cycle counter filter • Bit rate: Up to 10 Mbps
RSENT	• Conforming to the SENT (single edge nibble transmission) protocol specified in the SAE J2716_201604 standard and the SPC (short PWM code) extension to the SENT specification • Unidirectional or bidirectional transfer through a single pin • Bidirectional transfer through two pins • Data transmission protected with CRC
PSI5	• Conformance with PSI5 protocol specification V2.0 • Bit rates: Low speed(125 kbps), High speed(189 kbps), PAS compatibility mode(250 kbps) • Communication mode selectable
PSI5S	• Supports the UART-based communication for PSI5 transceiver. • Conforming to PSI5 protocol specification V2.2 • Generates a PSI5 message from the UART transfer data. • The bit rate of the UART can be set by the built-in baud rate generator.
CXPI	• Baud rate: 9.6 kbps/10.4 kbps/19.2 kbps/20.0 kbps • Master or Slave Mode • Event trigger method / Polling method • Output and sample the PWM waveform by PWM encoding/decoding function
Ethernet Controller	Integrated Ethernet Communication Controller (Ethernet MAC)- according to standard IEEE 802.3 - 2008. • The controller supports these operation modes - 10/100/1000 Mbps • Full-duplex operation • PHY Interface: MII, RMII, SGMII • Supports Receive filtering (L2~L4 including VLAN(up to 10)) • Supports Jumbo Frame(up to 16KB) • Supports IEEE 802.1AS-rev • Supports IEEE 802.1Qci Ingress Policing • Supports IEEE 802.1Qav - 2009 Credit-based shaper • Supports IEEE 802.1Qbv Time Aware Shaper • Supports IEEE 802.3br Interspersed Express Traffic • Supports IEEE 802.1Qbu Frame Preemption • Automatic Tx/Rx CRC computed by Ethernet Controller • Interrupt-free data transfer between system memory and network • Integrated DMA for data transfers from/to system memory • Integrated FIFO in Ethernet controller • Test modes - Internal loopback - External loopback • Magic PacketTM*1 detection • Generation of gPTP and AVTP timers *1 Magic Packet is a trademark of Advanced Micro Devices, inc
ETNF	• Flow control conforming with the IEEE 802.3x standard • Conform to OATC14 10base-T1S Transceiver Interfaces • Conform to OATC14 10base-T1S PLCA Management Registers • Conforming with the following standards stipulated for IEEE 802.1BA. • Transfer speed 10Mbps or 100Mbps • Support RMII (Full-duplex mode) or T1S mode • PHY interface: RMII (Reduced Media Independent Interface) • Open Alliance 10base-T1S Transceiver Interface • Built-in DMA transfer function • Timestamp support

Item	Features
TAUD	• 16 channels • 16-bit counter and 16-bit data register per channel • Independent channel operation • Synchronous channel operation (master and slave operation) • Generation of different types of output signal • Real-time output • Counter which can be triggered by external signal • Interrupt generation • The TAUD can operate independently or synchronously (combine with other channels)
TAUJ	• Independent channel operation function (operated using a single channel) • Synchronous channel operation function (operated using a master channel and multiple slave channels) The TAUJ can operate independently or synchronously (combine with other channels)
PWM-Diag	One PWBA block for generating clock signals • Generates a count clock signal for PWGC. Up to 96 PWGC blocks generate PWM signals. • Outputs PWM waveforms and A/D conversion triggers to PWSD. One PWSD block for generating triggers for A/D conversion • Transmits the required setting information to the A/D converter and outputs the A/D conversion start trigger.
SSIF	• Communication mode – Master/slave – Transmission/reception/transmission and reception • Communication format – I^2S format – Monaural format – TDM format • Interrupt – Communication error/idle mode error – Receive data full interrupt – Transmit data empty interrupt • Transmit FIFO/receive FIFO: 4 bytes × 32 stages
Watchdog Timer	• Can generate a signal to the ECM when a counter overflows (timer expires). • Can generate an interrupt at 75% of the counter overflow value. • An interrupt request can be generated at any function of the counter value. • A window open period can be set to any function of the counter value.
Secure WDT	• Can generate an error signal for the Interrupt Controller in response to an error. • Confirmation of matching with a specified Program Counter (PC) value of the CPU0.
OS Timer	• A 32-bit timer assuming use by an OS • Interval timer mode or free-running timer mode selectable • Synchronous start between units available
Long-Term System Counter (LTSC)	• Free-run up counting • Atomic read/write access to all registers • Anytime read access to counter registers • Application reset (SW reset) can be masked. When masked, counter keeps running on reset occurrence and counter register will not be initialized.

Item	Features
Motor Control Timer (TSG3)	The TSG3n is an 18-bit timer counter with various motor control functions. • Count clock resolution: Minimum 12.5 ns (count clock = 80 MHz) • Operating mode corresponding to various motor control methods • Compare registers with reload buffer • 10-bit dead time counter • A/D conversion trigger signal generation • Interrupt skipping – Skipping rate: 1/1 to 1/32 • Forced output stop function • Compare value setting – Reload (simultaneous rewrite) or anytime rewrite can be selected. • Various reload mode • HT-PWM mode with 0-100% duty cycles output • 120-DC control • Three-phase encoder function (Hall sensor signals can be input). • Active level of the output pins TSG3nO1 to TSG3nO6 can be set individually. • Fail-safe function (Warning interrupt or error interrupt can be generated). • Timer output control by input terminal.
Generic Timer Module (GTM)	GTM is a modular timer unit and consists of the following submodules : • Advanced Routing Unit (ARU) • Clock Management Unit (CMU) • Cluster Configuration Module (CCM) • Time Base Unit (TBU) • Timer Input Module (TIM) • ARU-connected Timer Output Module (ATOM) • Timer Input Output Module (TIO) • Dead Time Module (DTM) • Multi-Channel Sequencer (MCS) • Interrupt Concentrator Module (ICM) • Output Compare Unit (CMP) • Monitoring Unit (MON)
Real-Time Clock (RTCA)	• Counters for years, months, day of the month, day of the week, hours, minutes, seconds, and a subcounter. • One Hz pulse output function • Fixed interval interrupt function • Alarm interrupt function
Encoder Timer A (ENCA)	The Encoder Timer A (ENCA) has the following functions: • Generation of the counter control signal from the encoder input signal, and counter operation in synchronization with peripheral high-speed clock. • Capture function for capturing the counter value with an external trigger signal • Compare function for compare match judgment with the counter value • Two capture compare registers that can be set separately for capture operation and for compare operation • Interrupt mask function for masking the interrupt request signal output as a result of compare match judgment during compare operation • Function for loading the value of the capture compare register to the counter upon underflow occurrence • Encoder input signal can be applied to the timer counter clearing condition • Edge or level for clearing the encoder input signal of the timer counter clearing condition can be selected • Detection of counter overflow and underflow and output of error flags and error interrupts • Five interrupts: two capture compare interrupts, one counter clear interrupt, one overflow interrupt, and one underflow interrupt.

Item	Features
Timer Option (TAPA)	Timer Option (TAPA) is for use with Timer Array Unit D (TAUD), Motor Control Timer (TSG3) and SAR Analog to Digital Converter(SAR-ADC). • Asynchronous Hi-Z control to each TAUD and TSG3 output is enabled by TAPA input signals. • A peak and valley interrupt based on interrupt signals fromTAUD can be output. • Two conversion-trigger signals for SAR-ADC based on interrupt signals from TAUD can be output.
Peripheral Interconnect	The peripheral interconnection handles synchronous operations using multiple timers. • Peripheral timer control • ADC trigger selection
Analog to Digital Converter (ADCK)	• A/D conversion method: Successive approximation • Configuration of analog input pins • Resolution: 12/10-bit • Conversion speed: 1.0 µs • Scan groups for five systems for each converter • Two scan modes (multicycle scan mode and continuous scan mode) • Up to 64 virtual channels each ADCK • Addition mode A/D conversion functions incorporated • Can enter data directly to the Generic Timer Module. • Safety functions • Supporting an upper / lower-limit-excess-notice-function for the ADC Voltage Monitor Secondary Error Generator in each virtual channel • Track & Hold (T&H) input channels Several channel inputs can select T&H circuit for synchronize conversion.
Functional Safety	• Development compliant with ISO26262 functional safety standard • Major safety mechanisms – Flash memory ECC error detection function – RAM ECC error detection function – Peripheral module RAM ECC error detection function (e.g. FlexRay, CAN, GTM) – Clock monitor – Error Control Module (ECM) – Duplexing of modules (e.g. CPUs) – Automatic Power-on BIST execution after reset – Standby Resume BIST (SR-BIST) execution selection after wake-up from DeepSTOP mode.
Error Control Module (ECM)	The ECM collects error signals coming from different error sources and monitoring circuits. When an error is detected, ECM: • Generates FE or EI interrupt. • Generates internal reset. • Changes port state to Hi-Z. • Outputs errors via a dedicated pin. And the error flags which are captured in the ECM can be only cleared by Power On Reset or DeepSTOP Reset.
Data CRC Function (KCRC)	• Supports major CRC polynomials – 64-bit CRC64ECMA: 42F0E1EB A9EA3693$_H$ – 32-bit Ethernet CRC: 04C11DB7$_H$ – 32-bit CRC32C: 1EDC6F41$_H$ – 32-bit CRC32P4: F4ACFB13$_H$ – 16-bit CCITT: 1021$_H$ – 8-bit SAE J1850: 1D$_H$ – 8-bit 0x2F: 2F$_H$

Item	Features
Power Supply Voltage Monitor	• The power supply voltage monitor is used for monitoring power domain E0VCC, VCC, ISOVDD and AWOVDD. • The power supply voltage monitor has H-side (HDET) and L-side (LDET) voltage detectors, which detect if the monitored voltage is higher or lower than the specified voltage. • If the power supply voltage monitor detects an error, it gives the error notification to external devices outside of the MCU via ERROROUT_M pin (VMONOUT is merged to ERROROUT_M). • The Primary detection function is performed by Voltage Monitor. The Secondary detection function is performed by the ADCK.
Clock Monitor	• Up to 9 clock monitors depending on the device configuration. • Detects clock disturbances that results in lower or higher frequency than target frequency, and sends an error notification to the ECM. Supports the self-diagnosis function.
Temperature Sensor	• Out of range detection of temperature. • Operating modes – Single measurement mode – Continuous measurement mode • Interrupt requests – Temperature Measurement End Interrupt (INTOTSOTI) – Temperature rise/fall Interrupt (INTOTSOTULI) – Abnormal temperature error signal (OTABE) – Temperature Sensor Error (INTOTSOTE) • Support self-diagnosis function
Debugging and Calibration	• Debug interface – Nexus JTAG interface – Low Pin Debug Interface (4-pin) – External event triggers (input and output) – RHSIF Debug interface – Aurora Trace Interface
Flash Memory	• Code Flash – Program unit: 512 bytes, Erase unit: 16 KB for the first 8 blocks and 64 KB for remaining blocks in each Bank – Per-block OTP (One Time Programmable) support • Data Flash – Program unit: 4, 8, 16, 32, 64, 128 bytes, Erase unit:4-Kbyte • ECC support for error detection and correction • Programming method – Serial programming: Programming of flash memory by Dedicated Flash Memory programmer – Self-programming: Programming of flash memory by a user program • BGO (Back Ground Operation) support – Code Flash read is possible during Data Flash programming/erasure. – Code Flash read from other banks is possible during programming/erasure of a bank of Code Flash. – Data Flash read from other Data Areas is possible during programming/erasure of a Data Area of Data Flash. – Data Flash read is possible during Code Flash programming/erasure. • Multi FPSYS Operation support • Suspend/Resume function supported • Hardware Property Area is separated from Code Flash and Data Area to store the system configuration parameters. • OTA (Over-the-Air) update support

Item	Features
Basic Security	• This product includes the following security functions: – Hardware-level domain separation – Flash protection – Mode entry protection – Debugger authentication – Serial programing authentication – Device degradation
ICUM	• The ICUMHB is an on-chip Hardware Security Module (HSM). • The ICUMHB supports user-defined security services to the overall system based on cryptographic primitives.
ACEU	• The ACEU supports encryption and decryption based on AES algorithm.
RAM Modules	• Local RAM for each CPU – Any bus masters can access the Local RAM of CPUs. • Cluster RAM – Any bus masters can access the Cluster RAM. • Local RAM, Cluster RAM, Retention RAM and peripheral module RAMs are protected by SEC-DED ECC on data for functional safety. – Local RAM and Cluster RAM also include address feedback.
Boundary Scan	• Compliant with IEEE 1149.1 • JTAG interface (TDI, TDO, TMS, TCK and $\overline{\text{TRST}}$) • TAP controller • Supports the following instructions – BYPASS – EXTEST – SAMPLE/PRELOAD – CLAMP – HIGHZ – IDCODE

1.3 Application Fields

Automotive field (including body control, chassis & safety, engine control system and transmission control system)

1.4 Ordering Information

Table 1.1 Product Name List

Product Name*1	Package	On-Chip ROM	Operating Temperature (Tj)	External Oscillator	Maximum Operating Frequency	Core Power Supply
R7F702Z32AFDBF-C (RH850/U2C8-EVA)	Plastic FBGA404 0.8-mm ball pitch 19 mm × 19 mm	8 MB	max. 160°C	8/16/20/24 MHz	320 MHz	DPS
R7F702600AFABB-C (RH850/U2C8)	Plastic FBGA292 0.8-mm ball pitch 17 mm × 17 mm	8 MB	max. 160°C	8/16/20/24 MHz	320 MHz	DPS
R7F702606AFABB-C (RH850/U2C4)	Plastic FBGA292 0.8-mm ball pitch 17 mm × 17 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	DPS
R7F702606AFAFM-C R7F702606AFAFB-C (RH850/U2C4)	Plastic HLQFP144 0.4-mm pin pitch 16 mm × 16 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	DPS
R7F702606AFAFQ-C*2 R7F702606AFAFD-C (RH850/U2C4)	Plastic HLQFP100 0.4-mm pin pitch 12 mm × 12 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	DPS
R7F702616AFABB-C (RH850/U2C4)	Plastic FBGA292 0.8-mm ball pitch 17 mm × 17 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR (V_{VCC}=4.5V to 5.5V)
R7F702613AFABB-C (RH850/U2C4)	Plastic FBGA292 0.8-mm ball pitch 17 mm × 17 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR (V_{VCC}=V_{POC} to 3.6V)
R7F702616AFAFM-C R7F702616AFAFB-C (RH850/U2C4)	Plastic HLQFP144 0.4-mm pin pitch 16 mm × 16 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR (V_{VCC}=4.5V to 5.5V)
R7F702614AFAFM-C R7F702614AFAFB-C (RH850/U2C4)	Plastic HLQFP144 0.4-mm pin pitch 16 mm × 16 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR (V_{VCC}=V_{POC} to 3.6V)
R7F702616AFAFQ-C*2 R7F702616AFAFD-C (RH850/U2C4)	Plastic HLQFP100 0.4-mm pin pitch 12 mm × 12 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR (V_{VCC}=4.5V to 5.5V)
R7F702613AFAFQ-C*2 R7F702613AFAFD-C (RH850/U2C4)	Plastic HLQFP100 0.4-mm pin pitch 12 mm × 12 mm	4 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR (V_{VCC}=V_{POC} to 3.6V)
R7F702615AFAFM-C R7F702615AFAFB-C (RH850/U2C2)	Plastic HLQFP144 0.4-mm pin pitch 16 mm × 16 mm	2 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR
R7F702608AFAFQ-C*2 R7F702608AFAFD-C (RH850/U2C2)	Plastic HLQFP100 0.4-mm pin pitch 12 mm × 12 mm	2 MB	max. 160°C	8/16/20/24 MHz	320 MHz	eVR

Note 1. The character before "-" in Product Name depends on the assembly site.

Note 2. Reserved product number. For more details, please contact local sales.

1.5 Differences in the Specifications of RH850/U2C

The table below lists the differences in the specifications of RH850/U2C.

Table 1.2 Device Overview Table (1/3)

Feature			RH850/ U2C8- EVA 404 pins	RH850/ U2C8 292 pins	RH850/ U2C4 292 pins	RH850/ U2C4 144 pins	RH850/ U2C4 100 pins	RH850/ U2C2 144 pins	RH850/ U2C2 100 pins
Core	Main Core/Lockstep		2/2	2/2	2/2	2/2	2/2	1/1	1/1
	FPU		2	2	2	2	2	1	1
	MPU Region		24	24	24	24	24	24	24
	Frequency		320 MHz	320 MHz	320 MHz	320 MHz	320 MHz	320 MHz	320 MHz
Flash	Code Flash		8 Mbyte	8 Mbyte	4 Mbyte	4 Mbyte	4 Mbyte	2 Mbyte	2 Mbyte
	Data Flash (EEPROM emulation)		384 Kbyte	384 Kbyte	256 Kbyte	256 Kbyte	256 Kbyte	128 Kbyte	128 Kbyte
	Data Flash (HSM)		64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte
SRAM	Total (CRAM + LRAM)		1504 Kbyte	1504 Kbyte	704 Kbyte	704 Kbyte	704 Kbyte	288 Kbyte	288 Kbyte
	Local Data (LRAM)		128 Kbyte/ core	128 Kbyte/ core	128 Kbyte/ core	128 Kbyte/ core	128 Kbyte/ core	128 Kbyte/ core	128 Kbyte/ core
	Cluster (CRAM)		1248 Kbyte	1248 Kbyte	448 Kbyte	448 Kbyte	448 Kbyte	160 Kbyte	160 Kbyte
	Retention RAM (RRAM)		32 Kbyte	32 Kbyte	32 Kbyte	32 Kbyte	32 Kbyte	32 Kbyte	32 Kbyte
	Instruction Cache		8 Kbyte/ core (2way)	8 Kbyte/ core (2way)	8 Kbyte/ core (2way)	8 Kbyte/ core (2way)	8 Kbyte/ core (2way)	8 Kbyte/ core (2way)	8 Kbyte/ core (2way)
	Data Cache (Flash only)		4lines/ core (256bit/ line)	4lines/ core (256bit/ line)	4lines/ core (256bit/ line)	4lines/ core (256bit/ line)	4lines/ core (256bit/ line)	4lines/ core (256bit/ line)	4lines/ core (256bit/ line)
	Trace RAM		32 Kbyte	-	-	-	-	-	-
DMA	Channels (sDMAC/DTS)		32/128	32/128	32/128	32/128	32/128	32/128	32/128
SAR ADC	Units		3	3	2	2	2	2	2
	ADCK1/2/A (High accuracy inputs)		20/8/20	20/8/20	20/0/20	16/0/12	15/0/4	16/0/12	15/0/4
	ADCK1/2/A (Low accuracy inputs)		14/12/14	14/12/14	14/0/14	8/0/14	6/0/10	8/0/14	6/0/10
	Total inputs		88	88	68	50	35	50	35
	Virtual channels per module		64	64	64	64	64	64	64
Timer	GTM	Units	1	1	1	1	1	1	1
	PWM-Diag	Units	96	96	96	64	48	64	48
	TAPA	Units	4	4	4	4	4	4	4
	TAUD	Units	3	3	3	3	3	3	3
	TAUJ	Units	4	4	4	4	4	4	4
	TSG3	Units	2	2	2	2	2	2	2
	ENCA	Units	1	1	1	1	1	1	1
	RTCA	Units	1	1	1	1	1	1	1
	Window Watchdog Timer (WDTB)	Units	3	3	3	3	3	2	2
	Secure Watchdog Timer (SWDT)	Units	1	1	1	1	1	1	1

Table 1.2 Device Overview Table (2/3)

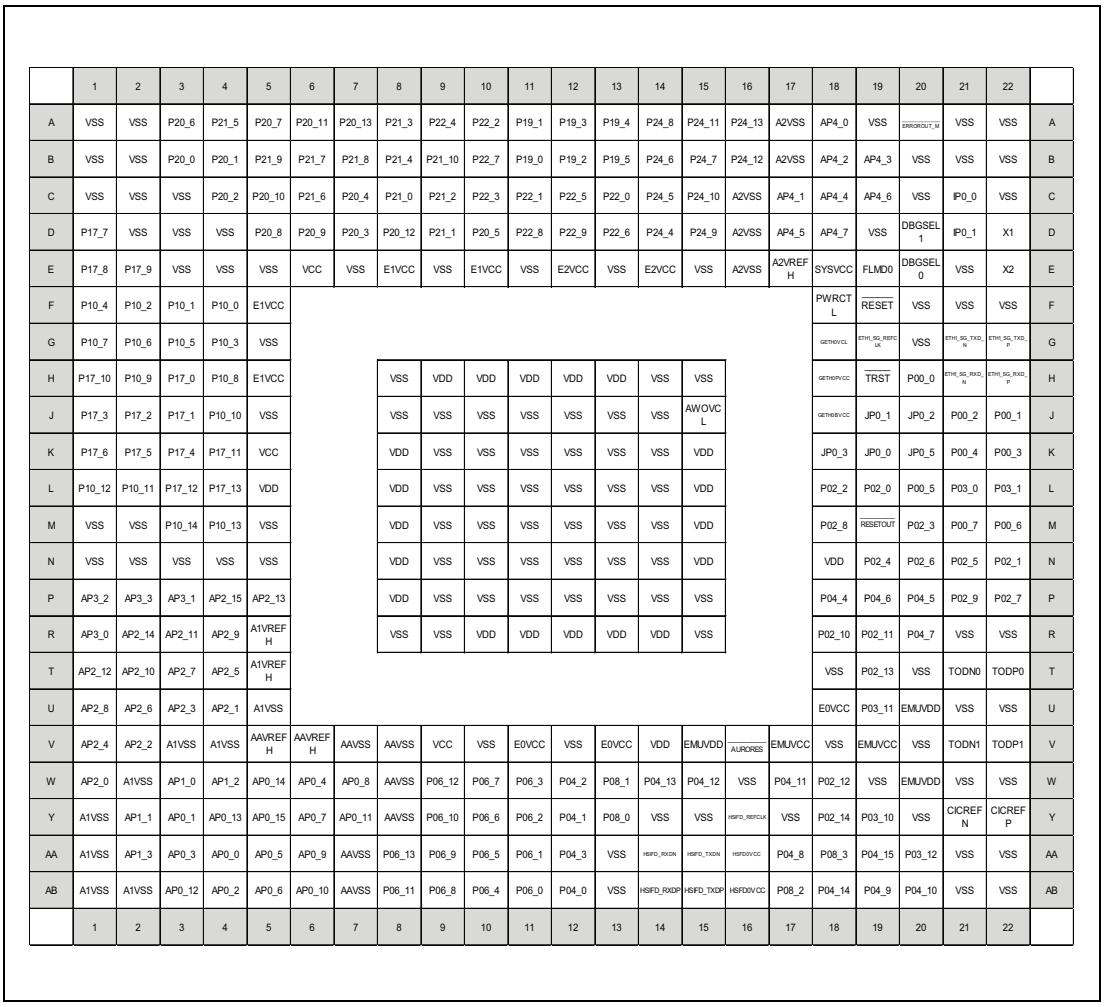
Feature			RH850/ U2C8-EVA 404 pins	RH850/ U2C8 292 pins	RH850/ U2C4 292 pins	RH850/ U2C4 144 pins	RH850/ U2C4 100 pins	RH850/ U2C2 144 pins	RH850/ U2C2 100 pins
	OS Timer (OSTM)	Units	2	2	2	2	2	1	1
	Time Protection Timer (TPTM)	Timer sets	2	2	2	2	2	1	1
	Long-Term System Counter (LTSC)	Units	1	1	1	1	1	1	1
Security	ICUMHB		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Secure RAM		128 Kbyte	128 Kbyte	128 Kbyte	128 Kbyte	128 Kbyte	128 Kbyte	128 Kbyte
	Secure Data Flash		64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte	64 Kbyte
	Code Flash Protection		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ACEU	Units	1	1	1	1	1	1	1
Interfaces	FlexRay	Units [Channels]	1 [2ch]	1 [2ch]	1 [2ch]	1 [2ch]	1 [2ch]	-	-
	CANXL	Units	2	2	2	2	2	1	1
	RS-CANFD	Units [Channels]	2 [14ch]	2 [14ch]	1 [6ch]	1 [6ch]	1 [4ch]	1 [6ch]	1 [4ch]
	MSPI	Units	10	10	8	8	8	8	6
	RLIN3	Units	20	20	16	16	14	12	8
	RI3C	Units	4	4	3	3	3	3	3
	RSENT	Units	8	8	8	8	8	8	8
	PSI5	Units	2	2	2	2	2	2	2
	PSI5S	Units	1	1	-	-	-	-	-
	Ethernet TSN (ETND)	Channel (100Mb/1Gb)	1/1	1/1	1/0	1/0	1/0	-	-
		ETND0 (MII/RMII/ SGMII)	1/1/0	1/1/0	1/1/0	1/1/0	0/1/0	-	-
		ETND1 (MII/RMII/ SGMII)	0/0/1	0/0/1	-	-	-	-	-
	Ethernet 10base-T1S (ETNF)	ETNF0 (T1S/RMII)	1/1	1/1	1/1	1/1	1/0	-	-
	CXPI	Units	4	4	4	2	2	2	2
	SSIF	Units	2	2	2	2	2	2	2
Safety	ASIL level		-	D	D	D	D	D	D
	CRC	Units	8	8	8	8	8	8	8
	ECM		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Clock monitor		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Error injection for self-diagnosis of several safety mechanisms		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	LBIST		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	MBIST		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Bus ECC		Yes	Yes	Yes	Yes	Yes	Yes	Yes
System Control	Voltage monitor		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Temperature Sensor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 1.2 Device Overview Table (3/3)

Feature			RH850/ U2C8- EVA 404 pins	RH850/ U2C8 292 pins	RH850/ U2C4 292 pins	RH850/ U2C4 144 pins	RH850/ U2C4 100 pins	RH850/ U2C2 144 pins	RH850/ U2C2 100 pins
Power Management	LPS		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	STBC		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	STOP mode		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	DeepSTOP mode		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Cyclic RUN mode		Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Memory Interfaces	MMCA	Units	1	1	1	1	1	-	-
	SFMA	Units	1	1	1	1	1	1	1
Debug	Nexus-JTAG		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Trace I/F (Aurora)		Yes	-	-	-	-	-	-
	Lopw Pin Debug I/F (4-pin)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
	RHSIF Debug I/F		Yes	-	-	-	-	-	-
	Boundary Scan		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Power Supply	Core Power Supply		DPS	DPS	DPS/ eVR *1	DPS/ eVR *1	DPS/ eVR *1	eVR	eVR
I/O port			198	181	190	117	77	117	77
Package	BGA404 0.8mm pitch		Yes	-	-	-	-	-	-
	BGA292 0.8mm pitch		-	Yes	Yes	-	-	-	-
	HLQFP144 0.4mm pitch		-	-	-	Yes	-	Yes	-
	HLQFP100 0.4mm pitch		-	-	-	-	Yes	-	Yes

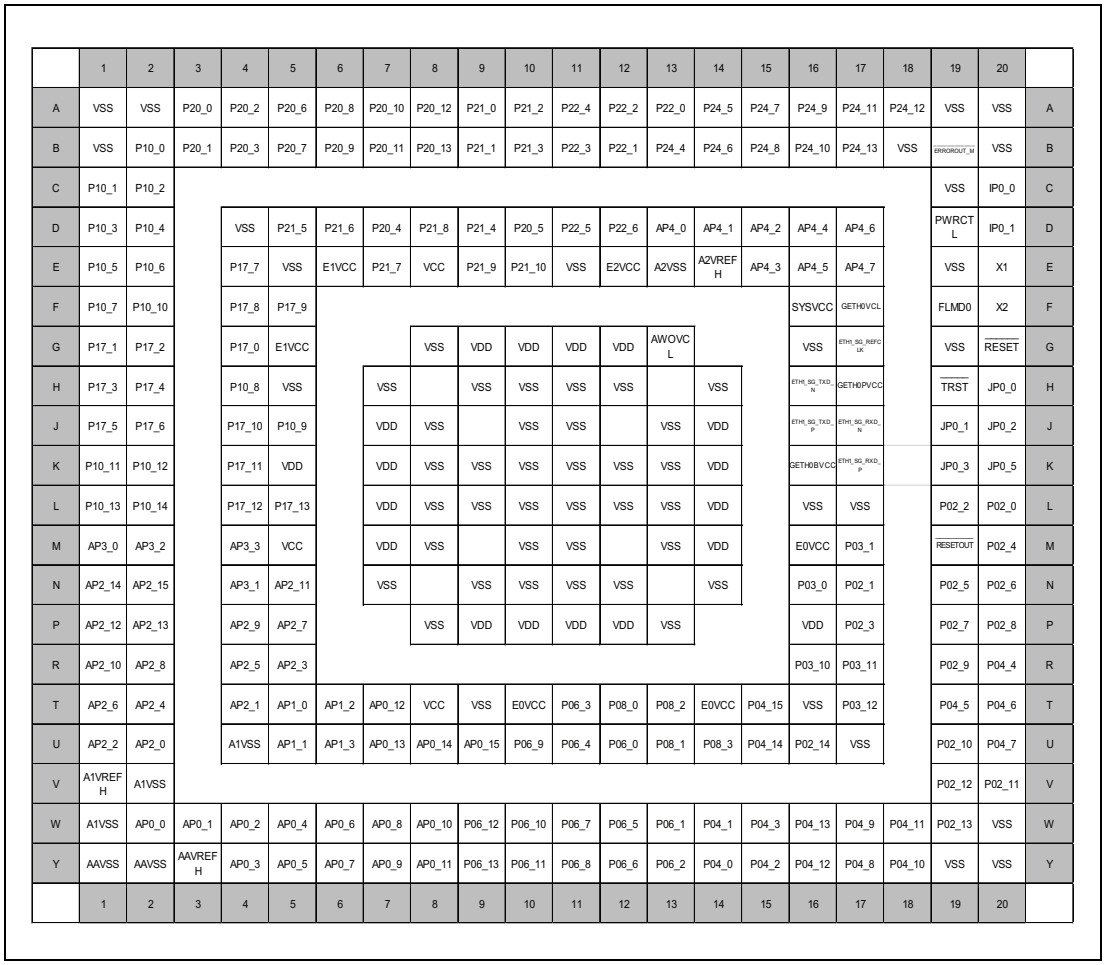
Note 1. Supported Core Power Supply is dependent on package. See **Section 1.4, Ordering Information**.

1.6 Pin Connection Diagram (Top View)



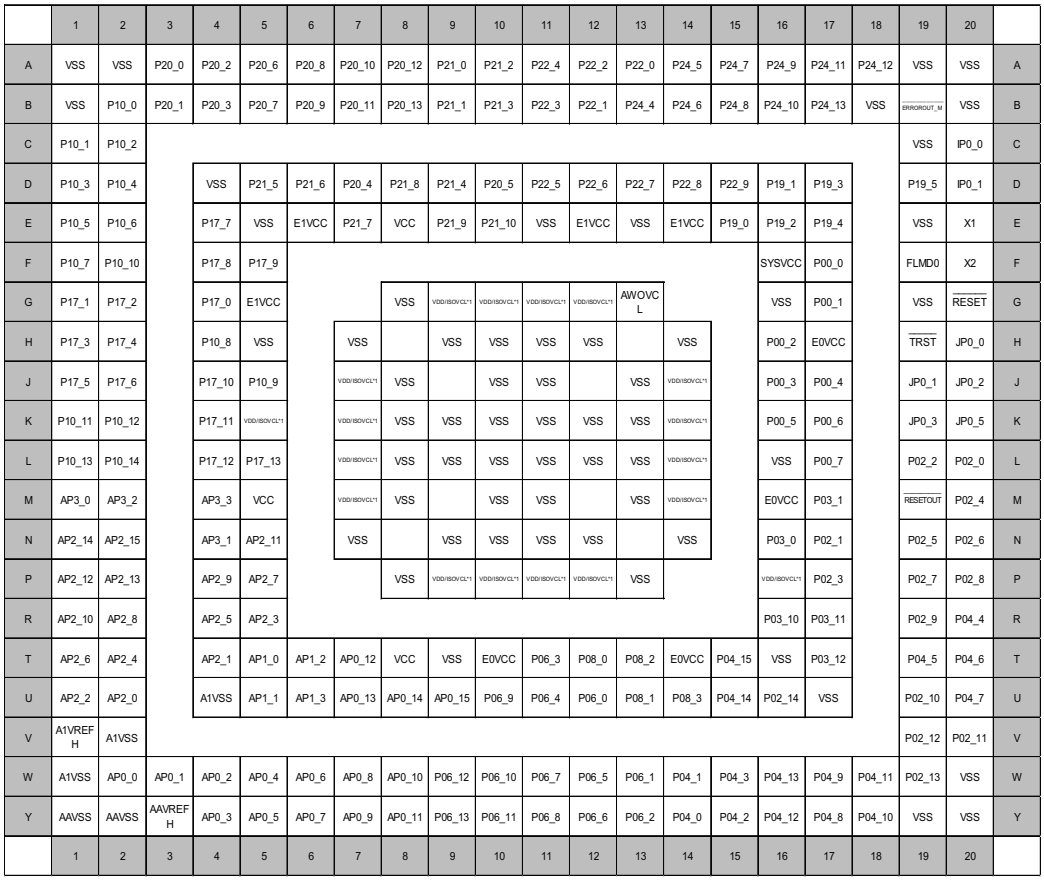
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	VSS	VSS	P20_6	P21_5	P20_7	P20_11	P20_13	P21_3	P22_4	P22_2	P19_1	P19_3	P19_4	P24_8	P24_11	P24_13	A2VSS	AP4_0	VSS	ERROROUT_M	VSS	VSS	A
B	VSS	VSS	P20_0	P20_1	P21_9	P21_7	P21_8	P21_4	P21_10	P22_7	P19_0	P19_2	P19_5	P24_6	P24_7	P24_12	A2VSS	AP4_2	AP4_3	VSS	VSS	VSS	B
C	VSS	VSS	VSS	P20_2	P20_10	P21_6	P20_4	P21_0	P21_2	P22_3	P22_1	P22_5	P22_0	P24_5	P24_10	A2VSS	AP4_1	AP4_4	AP4_6	VSS	IP0_0	VSS	C
D	P17_7	VSS	VSS	VSS	P20_8	P20_9	P20_3	P20_12	P21_1	P20_5	P22_8	P22_9	P22_6	P24_4	P24_9	A2VSS	AP4_5	AP4_7	VSS	DBGSEL1	IP0_1	X1	D
E	P17_8	P17_9	VSS	VSS	VSS	VCC	VSS	E1VCC	VSS	E1VCC	VSS	E2VCC	VSS	E2VCC	VSS	A2VSS	A2VREFH	SYSVCC	FLMD0	DBGSEL0	VSS	X2	E
F	P10_4	P10_2	P10_1	P10_0	E1VCC													PWRCTL	RESET	VSS	VSS	VSS	F
G	P10_7	P10_6	P10_5	P10_3	VSS													GETH0VCL	ETHI_SG_REFCLK	VSS	ETHI_SG_TXD_N	ETHI_SG_TXD_P	G
H	P17_10	P10_9	P17_0	P10_8	E1VCC			VSS	VDD	VDD	VDD	VDD	VDD	VSS	VSS			GETH0PVCC	TRST	P00_0	ETHI_SG_RXD_N	ETHI_SG_RXD_P	H
J	P17_3	P17_2	P17_1	P10_10	VSS			VSS	VSS	VSS	VSS	VSS	VSS	VSS	AWOVCL			GETH0SVCC	JP0_1	JP0_2	P00_2	P00_1	J
K	P17_6	P17_5	P17_4	P17_11	VCC			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD			JP0_3	JP0_0	JP0_5	P00_4	P00_3	K
L	P10_12	P10_11	P17_12	P17_13	VDD			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD			P02_2	P02_0	P00_5	P03_0	P03_1	L
M	VSS	VSS	P10_14	P10_13	VSS			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD			P02_8	RESETOUT	P02_3	P00_7	P00_6	M
N	VSS	VSS	VSS	VSS	VSS			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD			VDD	P02_4	P02_6	P02_5	P02_1	N
P	AP3_2	AP3_3	AP3_1	AP2_15	AP2_13			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS			P04_4	P04_6	P04_5	P02_9	P02_7	P
R	AP3_0	AP2_14	AP2_11	AP2_9	A1VREFH			VSS	VSS	VDD	VDD	VDD	VDD	VDD	VSS			P02_10	P02_11	P04_7	VSS	VSS	R
T	AP2_12	AP2_10	AP2_7	AP2_5	A1VREFH													VSS	P02_13	VSS	TODN0	TODP0	T
U	AP2_8	AP2_6	AP2_3	AP2_1	A1VSS													E0VCC	P03_11	EMUVDD	VSS	VSS	U
V	AP2_4	AP2_2	A1VSS	A1VSS	AAVREFH	AAVREFH	AAVSS	AAVSS	VCC	VSS	E0VCC	VSS	E0VCC	VDD	EMUVDD	AURORES	EMUVCC	VSS	EMUVCC	VSS	TODN1	TODP1	V
W	AP2_0	A1VSS	AP1_0	AP1_2	AP0_14	AP0_4	AP0_8	AAVSS	P06_12	P06_7	P06_3	P04_2	P08_1	P04_13	P04_12	VSS	P04_11	P02_12	VSS	EMUVDD	VSS	VSS	W
Y	A1VSS	AP1_1	AP0_1	AP0_13	AP0_15	AP0_7	AP0_11	AAVSS	P06_10	P06_6	P06_2	P04_1	P08_0	VSS	VSS	HSIFD_REFCLK	VSS	P02_14	P03_10	VSS	CICREFN	CICREFP	Y
AA	A1VSS	AP1_3	AP0_3	AP0_0	AP0_5	AP0_9	AAVSS	P06_13	P06_9	P06_5	P06_1	P04_3	VSS	HSIFD_RXDN	HSIFD_TXDN	HSFD0VCC	P04_8	P08_3	P04_15	P03_12	VSS	VSS	AA
AB	A1VSS	A1VSS	AP0_12	AP0_2	AP0_6	AP0_10	AAVSS	P06_11	P06_8	P06_4	P06_0	P04_0	VSS	HSIFD_RXDP	HSIFD_TXDP	HSFD0VCC	P08_2	P04_14	P04_9	P04_10	VSS	VSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 1.1 Pin Connection Diagram RH850/U2C8-EVA (BGA404)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	P20_0	P20_2	P20_6	P20_8	P20_10	P20_12	P21_0	P21_2	P22_4	P22_2	P22_0	P24_5	P24_7	P24_9	P24_11	P24_12	VSS	VSS	A
B	VSS	P10_0	P20_1	P20_3	P20_7	P20_9	P20_11	P20_13	P21_1	P21_3	P22_3	P22_1	P24_4	P24_6	P24_8	P24_10	P24_13	VSS	ERRORCUT_M	VSS	B
C	P10_1	P10_2																	VSS	IP0_0	C
D	P10_3	P10_4		VSS	P21_5	P21_6	P20_4	P21_8	P21_4	P20_5	P22_5	P22_6	AP4_0	AP4_1	AP4_2	AP4_4	AP4_6		PWRCTL	IP0_1	D
E	P10_5	P10_6		P17_7	VSS	E1VCC	P21_7	VCC	P21_9	P21_10	VSS	E2VCC	A2VSS	A2VREFH	AP4_3	AP4_5	AP4_7		VSS	X1	E
F	P10_7	P10_10		P17_8	P17_9											SYSVCC	GETH0VCL		FLMD0	X2	F
G	P17_1	P17_2		P17_0	E1VCC			VSS	VDD	VDD	VDD	VDD	AWOVCL			VSS	ETH1_SG_REFCLK		VSS	RESET	G
H	P17_3	P17_4		P10_8	VSS		VSS		VSS	VSS	VSS	VSS		VSS		ETH1_SG_TXD_N	GETH0PVCC		TRST	JP0_0	H
J	P17_5	P17_6		P17_10	P10_9		VDD	VSS		VSS	VSS		VSS	VDD		ETH1_SG_TXD_P	ETH1_SG_RXD_N		JP0_1	JP0_2	J
K	P10_11	P10_12		P17_11	VDD		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		GETH0BVCC	ETH1_SG_RXD_P		JP0_3	JP0_5	K
L	P10_13	P10_14		P17_12	P17_13		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	VSS		P02_2	P02_0	L
M	AP3_0	AP3_2		AP3_3	VCC		VDD	VSS		VSS	VSS		VSS	VDD		E0VCC	P03_1		RESETOUT	P02_4	M
N	AP2_14	AP2_15		AP3_1	AP2_11		VSS		VSS	VSS	VSS	VSS		VSS		P03_0	P02_1		P02_5	P02_6	N
P	AP2_12	AP2_13		AP2_9	AP2_7			VSS	VDD	VDD	VDD	VDD	VSS			VDD	P02_3		P02_7	P02_8	P
R	AP2_10	AP2_8		AP2_5	AP2_3											P03_10	P03_11		P02_9	P04_4	R
T	AP2_6	AP2_4		AP2_1	AP1_0	AP1_2	AP0_12	VCC	VSS	E0VCC	P06_3	P08_0	P08_2	E0VCC	P04_15	VSS	P03_12		P04_5	P04_6	T
U	AP2_2	AP2_0		A1VSS	AP1_1	AP1_3	AP0_13	AP0_14	AP0_15	P06_9	P06_4	P06_0	P08_1	P08_3	P04_14	P02_14	VSS		P02_10	P04_7	U
V	A1VREFH	A1VSS																	P02_12	P02_11	V
W	A1VSS	AP0_0	AP0_1	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P06_12	P06_10	P06_7	P06_5	P06_1	P04_1	P04_3	P04_13	P04_9	P04_11	P02_13	VSS	W
Y	AAVSS	AAVSS	AAVREFH	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P06_13	P06_11	P06_8	P06_6	P06_2	P04_0	P04_2	P04_12	P04_8	P04_10	VSS	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

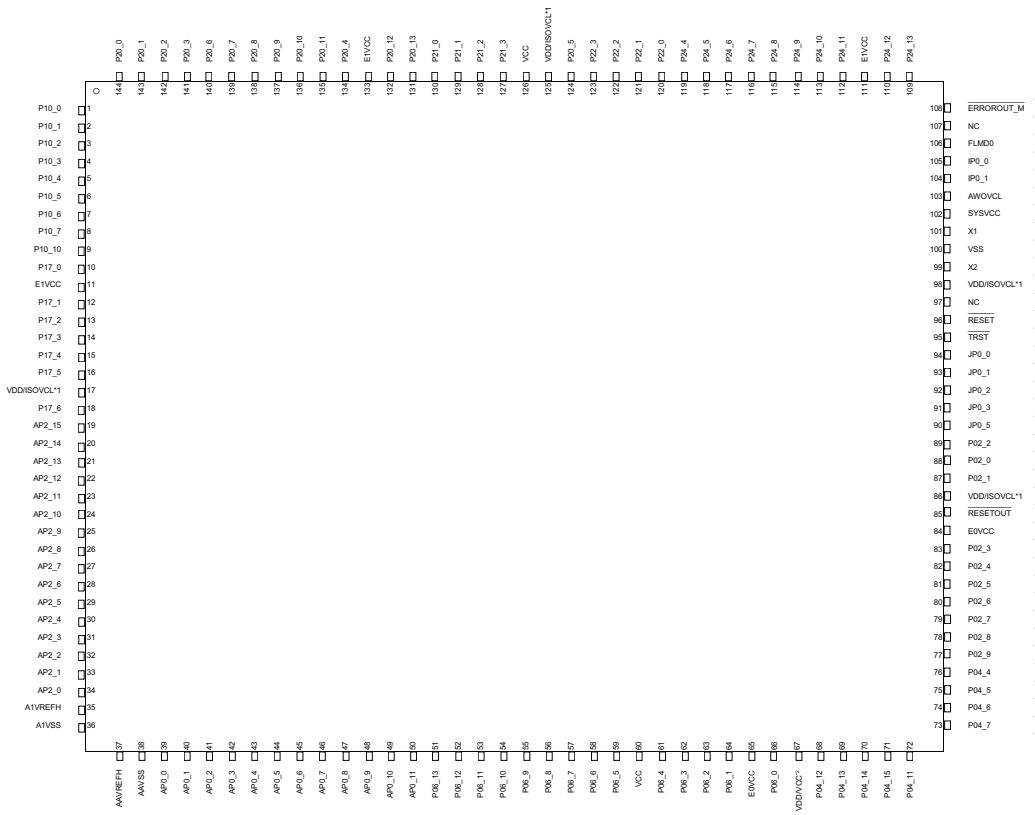
Figure 1.2 Pin Connection Diagram RH850/U2C8 (BGA292)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	VSS	P20_0	P20_2	P20_6	P20_8	P20_10	P20_12	P21_0	P21_2	P22_4	P22_2	P22_0	P24_5	P24_7	P24_9	P24_11	P24_12	VSS	VSS	A
B	VSS	P10_0	P20_1	P20_3	P20_7	P20_9	P20_11	P20_13	P21_1	P21_3	P22_3	P22_1	P24_4	P24_6	P24_8	P24_10	P24_13	VSS	$\overline{\text{ERROROUT\_M}}$	VSS	B
C	P10_1	P10_2																	VSS	IP0_0	C
D	P10_3	P10_4		VSS	P21_5	P21_6	P20_4	P21_8	P21_4	P20_5	P22_5	P22_6	P22_7	P22_8	P22_9	P19_1	P19_3		P19_5	IP0_1	D
E	P10_5	P10_6		P17_7	VSS	E1VCC	P21_7	VCC	P21_9	P21_10	VSS	E1VCC	VSS	E1VCC	P19_0	P19_2	P19_4		VSS	X1	E
F	P10_7	P10_10		P17_8	P17_9											SYSVCC	P00_0		FLMD0	X2	F
G	P17_1	P17_2		P17_0	E1VCC			VSS	VDD/ISOVCL*1	VDD/ISOVCL*1	VDD/ISOVCL*1	VDD/ISOVCL*1	AWOVCL			VSS	P00_1		VSS	$\overline{\text{RESET}}$	G
H	P17_3	P17_4		P10_8	VSS		VSS		VSS	VSS	VSS	VSS		VSS		P00_2	E0VCC		$\overline{\text{TRST}}$	JP0_0	H
J	P17_5	P17_6		P17_10	P10_9		VDD/ISOVCL*1	VSS		VSS	VSS		VSS	VDD/ISOVCL*1		P00_3	P00_4		JP0_1	JP0_2	J
K	P10_11	P10_12		P17_11	VDD/ISOVCL*1		VDD/ISOVCL*1	VSS	VSS	VSS	VSS	VSS	VSS	VDD/ISOVCL*1		P00_5	P00_6		JP0_3	JP0_5	K
L	P10_13	P10_14		P17_12	P17_13		VDD/ISOVCL*1	VSS	VSS	VSS	VSS	VSS	VSS	VDD/ISOVCL*1		VSS	P00_7		P02_2	P02_0	L
M	AP3_0	AP3_2		AP3_3	VCC		VDD/ISOVCL*1	VSS		VSS	VSS		VSS	VDD/ISOVCL*1		E0VCC	P03_1		$\overline{\text{RESETOUT}}$	P02_4	M
N	AP2_14	AP2_15		AP3_1	AP2_11		VSS		VSS	VSS	VSS	VSS		VSS		P03_0	P02_1		P02_5	P02_6	N
P	AP2_12	AP2_13		AP2_9	AP2_7			VSS	VDD/ISOVCL*1	VDD/ISOVCL*1	VDD/ISOVCL*1	VDD/ISOVCL*1	VSS			VDD/ISOVCL*1	P02_3		P02_7	P02_8	P
R	AP2_10	AP2_8		AP2_5	AP2_3											P03_10	P03_11		P02_9	P04_4	R
T	AP2_6	AP2_4		AP2_1	AP1_0	AP1_2	AP0_12	VCC	VSS	E0VCC	P06_3	P08_0	P08_2	E0VCC	P04_15	VSS	P03_12		P04_5	P04_6	T
U	AP2_2	AP2_0		A1VSS	AP1_1	AP1_3	AP0_13	AP0_14	AP0_15	P06_9	P06_4	P06_0	P08_1	P08_3	P04_14	P02_14	VSS		P02_10	P04_7	U
V	A1VREFH	A1VSS																	P02_12	P02_11	V
W	A1VSS	AP0_0	AP0_1	AP0_2	AP0_4	AP0_6	AP0_8	AP0_10	P06_12	P06_10	P06_7	P06_5	P06_1	P04_1	P04_3	P04_13	P04_9	P04_11	P02_13	VSS	W
Y	AAVSS	AAVSS	AAVREFH	AP0_3	AP0_5	AP0_7	AP0_9	AP0_11	P06_13	P06_11	P06_8	P06_6	P06_2	P04_0	P04_2	P04_12	P04_8	P04_10	VSS	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Note 1. VDD on U2C4 DPS package. ISOVCL on U2C4 eVR package.

Figure 1.3 Pin Connection Diagram RH850/U2C4 (BGA292)

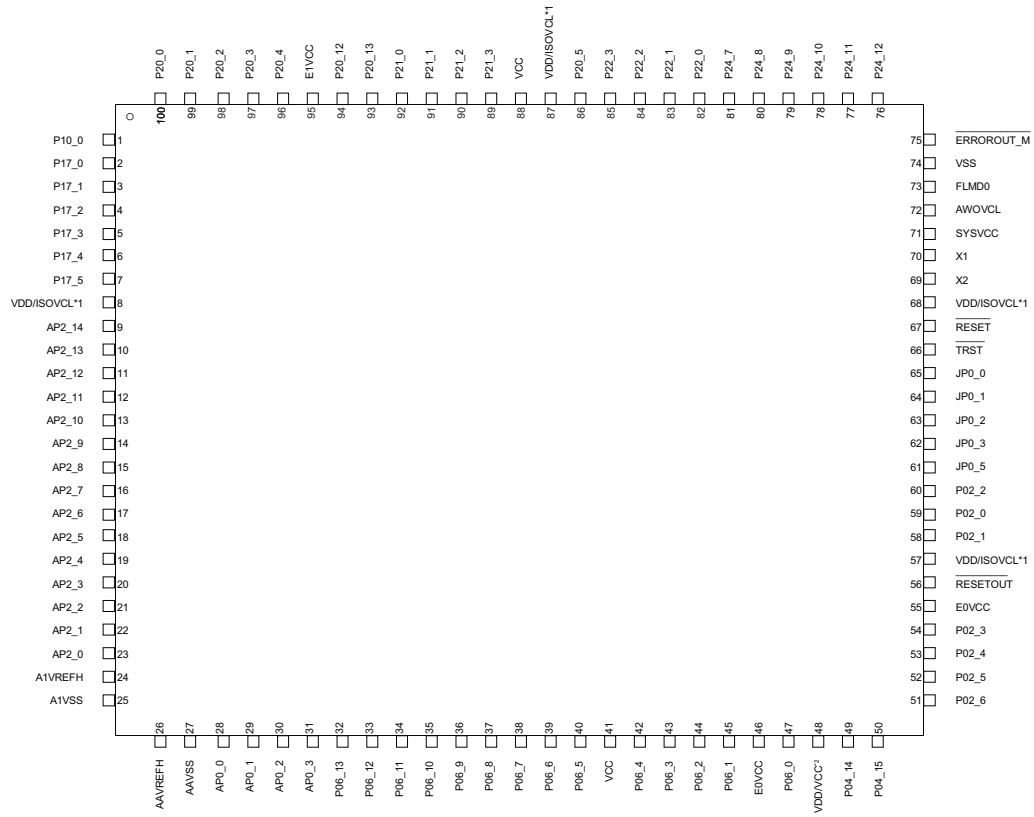


Note 1. VDD on U2C4 DPS package. ISOVCL on U2C4 eVR package and U2C2.

Note 2. VDD on U2C4 DPS package. VCC on U2C4 eVR package and U2C2.

Note: The Exposed Pad shall be connected to VSS.

Figure 1.4 Pin Connection Diagram RH850/U2C4, U2C2 (HLQFP144)



Note 1. VDD on U2C4 DPS package. ISOVCL on U2C4 eVR package and U2C2.

Note 2. VDD on U2C4 DPS package. VCC on U2C4 eVR package and U2C2.

Note: The Exposed Pad shall be connected to VSS.

Figure 1.5 Pin Connection Diagram RH850/U2C4, U2C2 (HLQFP100)

Table 1.3 Differences in the specifications of BGA292

Pin No.	RH850/U2C8	RH850/U2C4
D13	AP4_0	P22_7
D14	AP4_1	P22_8
D15	AP4_2	P22_9
D16	AP4_4	P19_1
D17	AP4_6	P19_3
D19	PWRCTL	P19_5
E12	E2VCC	E1VCC
E13	A2VSS	VSS
E14	A2VREFH	E1VCC
E15	AP4_3	P19_0
E16	AP4_5	P19_2
E17	AP4_7	P19_4
F17	GETH0VCL	P00_0
G17	ETH1_SG_REFCLK	P00_1
H16	ETH1_SG_TXD_N	P00_2
H17	GETH0PVCC	E0VCC
J16	ETH1_SG_TXD_P	P00_3
J17	ETH1_SG_RXD_N	P00_4
K16	GETH0BVCC	P00_5
K17	ETH1_SG_RXD_P	P00_6
L17	VSS	P00_7
*1	VDD	VDD/ISOVCL *1

Note 1. RH850/U2C4 eVR package mount ISOVCL on pin no.G9, G10, G11, G12, J7, J14, K5, K7, K14, L7, L14, M7, M14, P9, P10, P11, P12, P16.
RH850/U2C4 DPS package mount VDD as same as U2C8.

1.7 Functional Block Configuration

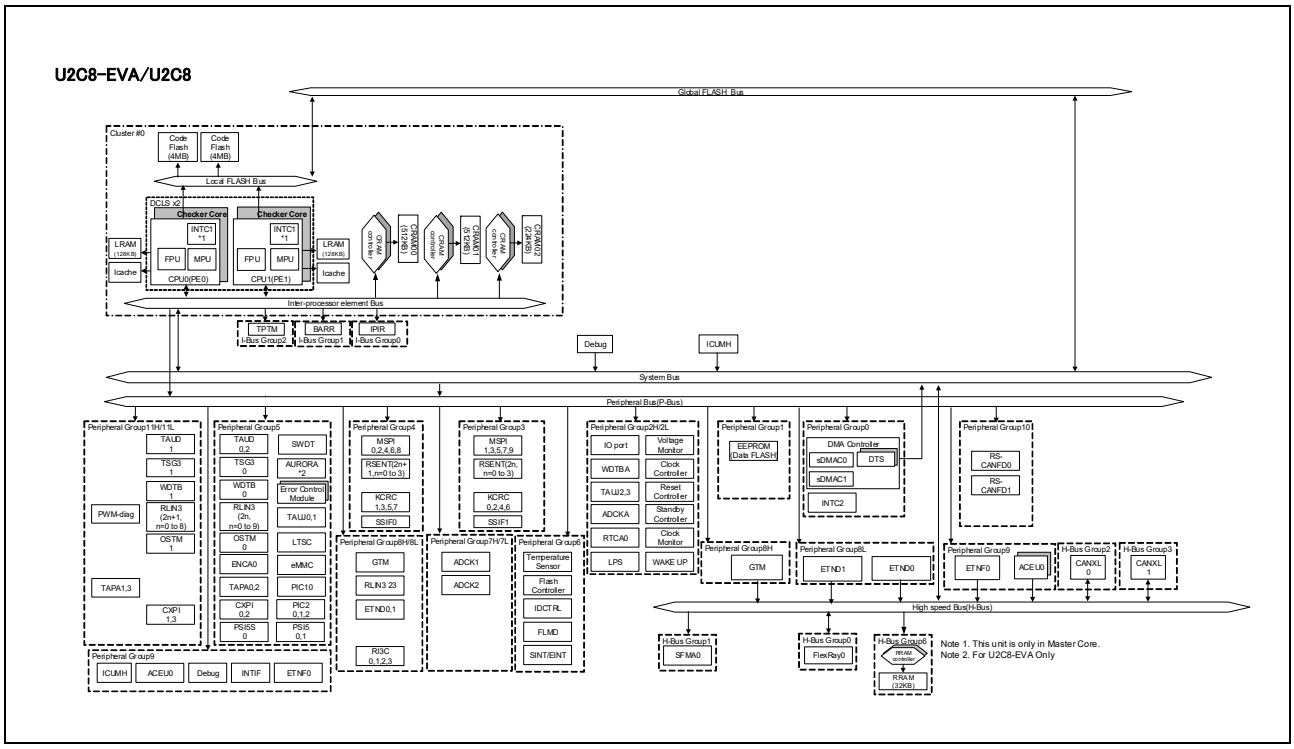


Figure 1.6 Internal Block Diagram (U2C8-EVA/U2C8)

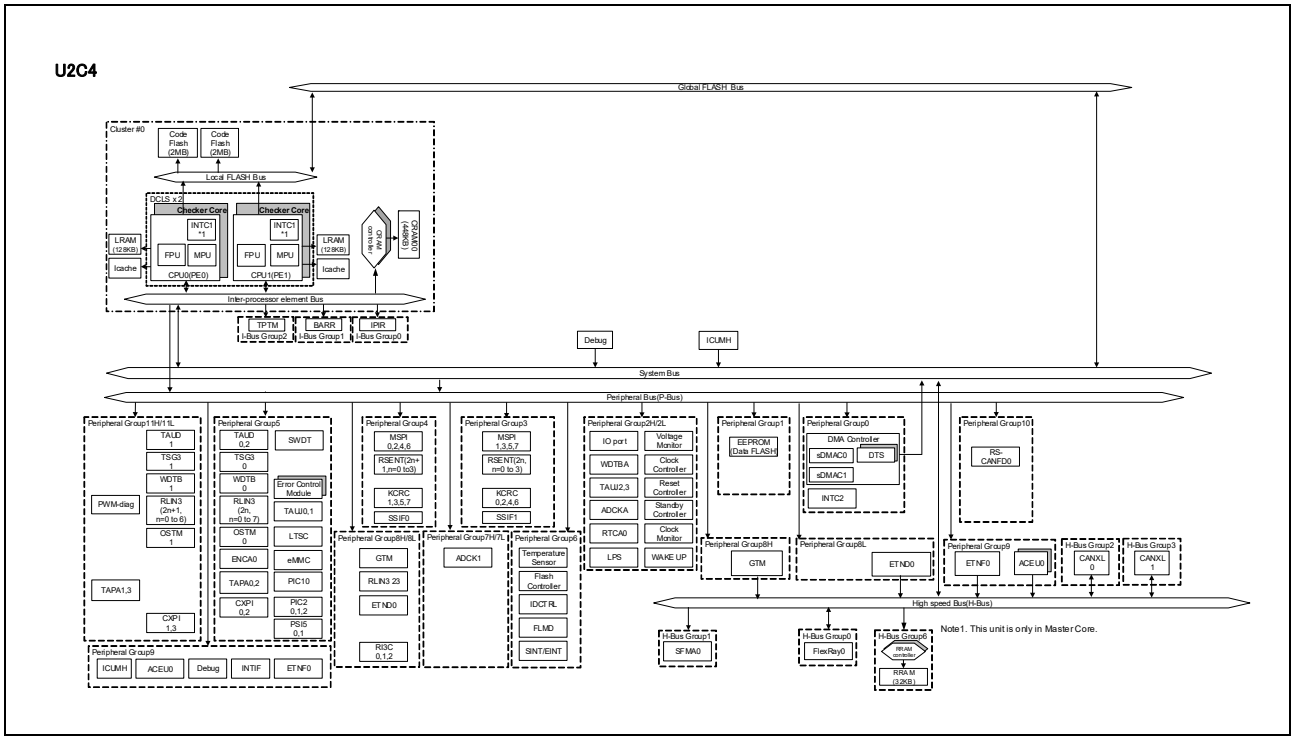


Figure 1.7 Internal Block Diagram (U2C4)

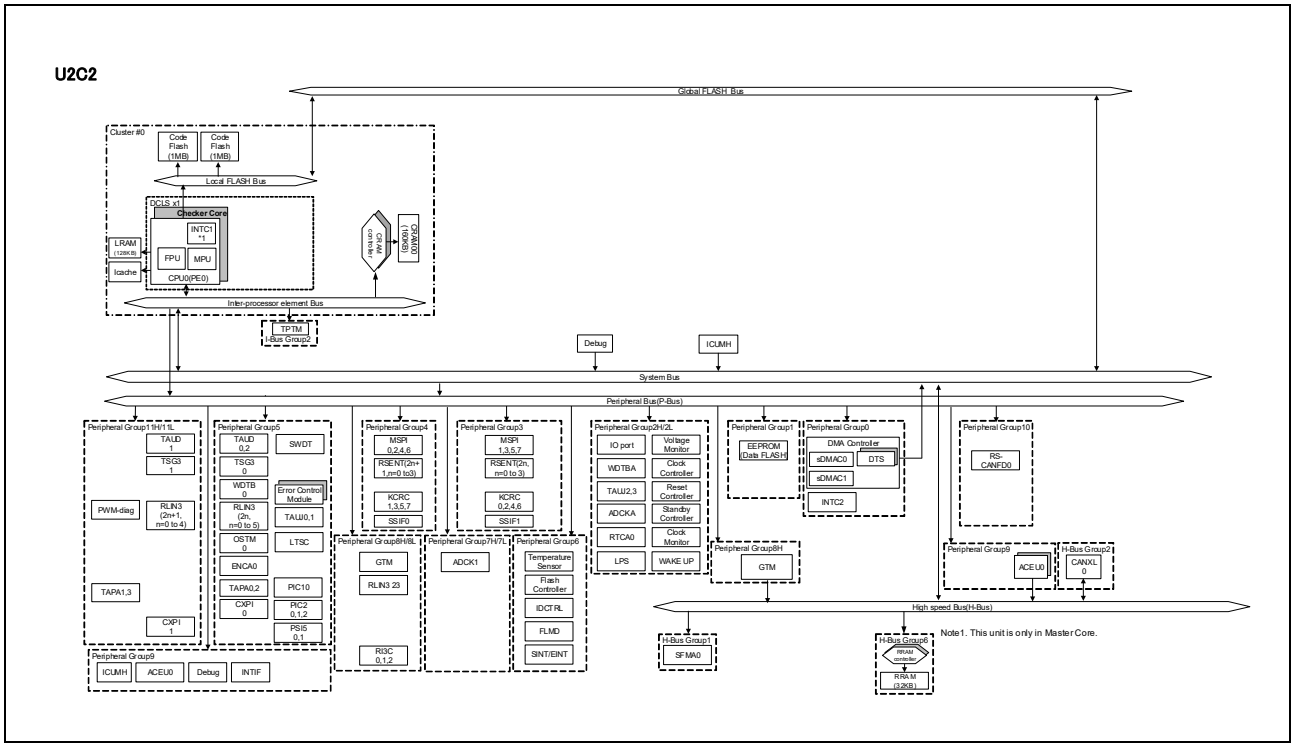


Figure 1.8 Internal Block Diagram (U2C2)

Section 2 Pin Functions

This section describes the pin connections and respective pin functions.

2.1 Pin List

2.1.1 Pin List and Function assignment

For detail information, refer to Appendix “E02_01_List_of_Pin_Assignment.xlsx”.

2.1.2 Pin Function name

For detail information, refer to Appendix “E02_03_List_of_Pin_Function.xlsx".

Section 3 Electrical Characteristics

The specifications in this section are for devices operating under the conditions shown in **Section 3.2.1.1, Supply Voltage Characteristics**. Where a special condition is required for a given specification, the condition will be indicated. Furthermore, the specifications in this section are not guaranteed unless the conditions listed below are met.

Refer to **Table 1.1, Product Name List** for the relation of product number and core power supply.

3.1 Absolute Maximum Ratings

Conditions:

- VSS = AnVSS
- Reference ground potential: VSS = 0 V.

Table 3.1 Absolute Maximum Ratings (1/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power Voltage	$V_{AMRSYSVCC}$	SYSVCC	–0.5		6.5*8	V
	V_{AMRVCC}	VCC	–0.5		6.5*8	V
	V_{AMRVDD}	VDD	–0.5		1.42*9	V
	$V_{AMRE0VCC}$	E0VCC	–0.5		6.5*8	V
	$V_{AMRE1VCC}$	E1VCC	–0.5		6.5*8	V
	$V_{AMRE2VCC}$	E2VCC	–0.5		6.5*8	V
	$V_{AMRAAVREFH}$	AAVREFH	–0.5		6.5*8	V
	$V_{AMRA1VREFH}$	A1VREFH	–0.5		6.5*8	V
	$V_{AMRA2VREFH}$	A2VREFH	–0.5		6.5*8	V
	$V_{AMREMUVCC}$	EMUVCC	–0.5		4.6*10	V
	$V_{AMREMUVDD}$	EMUVDD	–0.5		1.42*9	V
	$V_{AMRGETH0BVCC}$	GETH0BVCC	–0.5		4.6*10	V
	$V_{AMRGETH0PVCC}$	GETH0PVCC	–0.5		6.5*8	V
	$V_{AMRHSFD0VCC}$	HSFD0VCC	–0.5		6.5*8	V
Input Voltage	V_{AMRI}	E0VCC pin*1	–0.5		E0VCC + 0.5*7	V
		E1VCC pin*2	–0.5		E1VCC + 0.5*7	V
		E2VCC pin*3	–0.5		E2VCC + 0.5*7	V
		$\overline{\text{RESET}}$, FLMD0, X1, X2 PWRCTL, IP0_0, IP0_1 pin	–0.5		SYSVCC + 0.5*7	V
		CICREFN, CICREFP	–0.5		EMUVDD + 0.5*7	V
		$\overline{\text{AURORES}}$	–0.5		EMUVCC + 0.5*7	V
		RHSIF (debug)	–0.5		HSFD0VCC + 0.5	V
		SGMII I/F*4	–0.5		GETH0BVCC + 0.5*7	V
		ETH1_SG_REFCLK	–0.5		GETH0PVCC + 0.5*7	V
Analogue input voltage	$V_{AMRAVREF}$	AAVREFH pin	–0.5		AAVREFH + 0.5	V
		A1VREFH pin	–0.5		A1VREFH + 0.5	V
		A2VREFH pin	–0.5		A2VREFH + 0.5	V
VSS differential voltage	$V_{VSSDIFF}$		–0.1		0.1	V

Table 3.1 Absolute Maximum Ratings (2/2)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Injection current per digital input	I_{INJ_DIN}	*11	–25		25	mA
Injection current per analog input	I_{INJ_AIN}	*11	–25		25	mA
Total Injection current of the device	$\|I_{INJ\_TOT}\|$	*11			120	mA
Output low current*5	I_{OL1p}	per pin			10	mA
	I_{OLall}	Sum of all output low currents of all EnVCC/AnVREFH pins			200	mA
Output high current*5	I_{OH1p}	per pin			–10	mA
	I_{OHall}	Sum of all output high currents of all EnVCC/AnVREFH pins			–200	mA
Junction temperature	T_j		–40		160	°C
Storage temperature*6	T_{stg}		–55		160	°C

Note 1. JP0, P00, P02, P03, P04, P06, P08, $\overline{\text{TRST}}$, $\overline{\text{RESETOUT}}$

Note 2. P10, P17, P20, P21
P19 [U2C4 only]
P22, P24 [U2C4/U2C2 only]

Note 3. P19 [U2C8-EVA only]
P22, P24 [U2C8-EVA/U2C8 only]

Note 4. ETH1_SG_TXD_N, ETH1_SG_TXD_P, ETH1_SG_RXD_N, ETH1_SG_RXD_P

Note 5. Given specification includes injected currents.

Note 6. After mounting

Note 7. See **Table 3.2, Supply Voltage Characteristics**

Note 8. Voltage overshoot 5.8 V to 6.5 V is permissible, cumulative time is less than 2 h. Voltage overshoot 5.5 V to 5.8 V is permissible, cumulative time is less than 100 h.

Note 9. Voltage overshoot 1.205 V to 1.42 V is permissible, cumulative time is less than 2 h. Voltage overshoot 1.155 V to 1.205 V is permissible, cumulative time is less than 100 h.

Note 10. Voltage overshoot 3.9 V to 4.6 V is permissible, cumulative time is less than 2 h. Voltage overshoot 3.6 V to 3.9 V is permissible, cumulative time is less than 100 h.

Note 11. Input voltage must be kept within -0.8 V ≤ Vin ≤ 6.5 V. Power supply voltage must be kept within rated values. Injection current must be kept within rated values on all states include ramp-up/down, and power-on/off. Injection current effects power dissipation in the package for thermal characteristics.

CAUTION

- **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
- **Input voltage, analog reference voltage and analog input voltage must not exceed 6.5 V.**
- **Even in case when input voltage does not meet the specified characteristics, it is accepted if the injected current characteristics specified in Section 3.2.7 are met.**

3.2 General & DC Characteristics

3.2.1 Operational Condition

3.2.1.1 Supply Voltage Characteristics

Conditions:

- Temperature range: Tj (min) to Tj (max)
- VSS = AnVSS
- Reference ground potential: VSS = 0 V

Table 3.2 Supply Voltage Characteristics*5

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System control supply voltage*4	V_{SYSVCC}	For U2C4 eVR	V_{POC}		3.6	V
			4.5		5.5	
		Other than above	V_{POC}		5.5	V
Regulator supply voltage	V_{VCC}	For U2C4 eVR	V_{POC}		3.6	V
			4.5		5.5	
		Other than above	V_{POC}		5.5	V
Core supply voltage	V_{VDD}		1.025	1.09	1.155	V
IO supply voltage	V_{E0VCC}		V_{POC}		5.5	V
	V_{E1VCC}					
	V_{E2VCC}					
ADC supply voltage	$V_{AAVREFH}$		3.0		5.5	V
	$V_{A1VREFH}$					
	$V_{A2VREFH}$					
RHSIF (debug) supply voltage*6	$V_{HSFD0VCC}$		3.0		3.6	V
			4.5		5.5	V
Aurora I/F supply voltage (Analog) Aurora control IO supply voltage	V_{EMUVCC}		3		3.6	V
Aurora I/F supply voltage (Digital) Aurora control core supply voltage	V_{EMUVDD} (V_{DVDD})	Aurora used	1.04	1.09	1.14	V
		Aurora unused	1.025	1.09	1.155	V
SGMII supply voltage*3	$V_{GETH0PVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused	3		5.5	V
	$V_{GETH0BVCC}$	SGMII used	3.14	3.3	3.46	V
		SGMII unused		*2		V

Note 1. SYSVCC is monitored by POC, see **Section 3.2.13, Voltage Detector (POC) Characteristics**.
Note 2. Input 3.0V to 3.6V voltage or connect to VSS with 1 kΩ or more pull-down resistance.
Note 3. Maximum allowable noise for SGMII power is 50mV peak to peak.
Note 4. Maximum allowable noise for SYSVCC is 100mV peak to peak.
When MainOSC is used as the clock source of SGMII or when ETNF is working, allowable noise for SYSVCC will be 50mV peak to peak.
Note 5. Use this device with the following conditions.
AAVREFH ≥ VCC
AAVREFH ≥ E0VCC = HSFD0VCC
GETH0PVCC = GETH0BVCC, when SGMII use.
Note 6. Maximum allowable noise for HSFD0VCC is 100mV peak to peak.

CAUTION

During operations, supply the specified voltages to all power lines. When stopping operation, turn off all of the power supplies.

3.2.1.2 Main Oscillator Characteristics

Conditions:

- Supply voltage range: Refer to **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.3 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC} *1*2	Crystal/Ceramic		8 – 1%		24 + 1%	MHz
		Crystal*5		20 – 100 ppm		20 + 100 ppm	MHz
MainOSC oscillation operating point	V_{MOSCOP}	Crystal/Ceramic			0.89		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$	Crystal/Ceramic		0.54			V
MainOSC oscillation stabilization time	t_{MSTB}	Crystal/Ceramic				5	ms
MainOSC oscillation amplifier reaction time	$t_{MOSCAMP}$	Crystal/Ceramic				200	µs
Internal Capacitor size selectable by CAP_SEL setting (OPBT setting)	C_{capsel}	CAP_SEL [3:0]	= 0000_B	*4	0 (3.7), 0 (4.9)*3	*4	pF
			= 0001_B	*4	1 (4.6), 1 (5.9)*3	*4	pF
			= 0010_B	*4	2 (5.6), 2 (6.9)*3	*4	pF
			= 0011_B	*4	3 (6.6), 3 (7.9)*3	*4	pF
			= 0100_B	*4	4 (7.3), 4 (8.6)*3	*4	pF
			= 0101_B	*4	5 (8.3), 5 (9.5)*3	*4	pF
			= 0110_B	*4	6 (9.3), 6 (10.5)*3	*4	pF
			= 0111_B	*4	7 (10.2), 7 (11.4)*3	*4	pF
			= 1000_B	*4	8 (11.3), 8 (12.3)*3	*4	pF
			= 1001_B	*4	9 (12.1), 9 (13.3)*3	*4	pF
			= 1010_B	*4	10 (13), 10 (14.2)*3	*4	pF
Internal damping resistor size selectable by RDSEL setting (OPBT setting)*2	R_{rdsel}	MOSC_RD_SEL_A [2:0] MOSC_RD_SEL_B [2:0]	= 000_B	217	334	568	Ω
			= 001_B	341	525	998	Ω
			= 010_B	513	790	1383	Ω
			= 011_B	680	1047	1728	Ω
			= 100_B	857	1319	2045	Ω
			= 101_B	1595	2454	3313	Ω
			= 110_B	1595	2454	3313	Ω
			= 111_B	1595	2454	3313	Ω

Table 3.3 Main Oscillator Characteristics (2/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Trans conductance size (g_m) and Output conductance size (g_{ds}) selectable by MOSC_SHTSTBY_A, MOSC_AMPSEL_A, MOSC_SHTSTBY_B and, MOSC_AMPSEL_B setting (OPBT10 setting)*2	g_m, g_{ds}	{MOSC_SHTSTBY_A, MOSC_AMPSEL_A [2:0]} or {MOSC_SHTSTBY_B, MOSC_AMPSEL_B [2:0]} SYSVCC = 3.0 V to 3.6 V	= 0000_B	0.49, 0.02	0.77, 0.04	1.09, 0.08	mS
			= 0001_B	0.79, 0.03	1.22, 0.05	1.74, 0.1	mS
			= 0010_B	1.66, 0.07	2.55, 0.1	3.78, 0.17	mS
			= 0011_B	2.52, 0.09	3.97, 0.14	6.33, 0.23	mS
			= 0100_B	3.73, 0.13	6, 0.19	9.14, 0.31	mS
			= 0101_B	4.98, 0.17	8.02, 0.24	12.13, 0.38	mS
			= 0110_B	6.54, 0.21	10.46, 0.31	15.71, 0.47	mS
			= 0111_B	7.58, 0.25	12.08, 0.35	17.96, 0.55	mS
			= 1000_B	1.42, 0.08	2.6, 0.13	3.57, 0.24	mS
			= 1001_B	2.15, 0.1	3.48, 0.15	4.85, 0.26	mS
			= 1010_B	3.47, 0.14	5.59, 0.2	8.04, 0.32	mS
			= 1011_B	4.54, 0.18	7.37, 0.25	10.76, 0.38	mS
			= 1100_B	5.85, 0.22	9.5, 0.3	13.97, 0.46	mS
			= 1101_B	7.08, 0.25	11.48, 0.36	16.92, 0.52	mS
			= 1110_B	8.54, 0.29	13.81, 0.41	20.35, 0.6	mS
			= 1111_B	9.17, 0.32	14.87, 0.45	21.82, 0.66	mS
Trans conductance size (g_m) and Output conductance size (g_{ds}) selectable by MOSC_SHTSTBY_A, MOSC_AMPSEL_A, MOSC_SHTSTBY_B and MOSC_AMPSEL_B setting (OPBT10 setting)*2	g_m, g_{ds}	{MOSC_SHTSTBY_A, MOSC_AMPSEL_A [2:0]} or {MOSC_SHTSTBY_B, MOSC_AMPSEL_B [2:0]} SYSVCC = 4.5 V to 5.5 V	= 0000_B	0.5, 0.02	0.78, 0.04	1.13, 0.08	mS
			= 0001_B	0.79, 0.03	1.24, 0.05	1.8, 0.11	mS
			= 0010_B	1.65, 0.06	2.57, 0.09	3.85, 0.17	mS
			= 0011_B	2.54, 0.09	4, 0.14	6.12, 0.23	mS
			= 0100_B	3.79, 0.12	6.03, 0.19	9.22, 0.31	mS
			= 0101_B	5.07, 0.16	8.07, 0.24	12.24, 0.38	mS
			= 0110_B	6.67, 0.2	10.55, 0.3	15.84, 0.46	mS
			= 0111_B	7.75, 0.24	12.22, 0.34	18.12, 0.54	mS
			= 1000_B	1.68, 0.08	2.66, 0.12	3.65, 0.2	mS
			= 1001_B	2.22, 0.1	3.55, 0.14	4.94, 0.23	mS
			= 1010_B	3.53, 0.14	5.67, 0.2	8.15, 0.31	mS
			= 1011_B	4.64, 0.17	7.46, 0.24	10.86, 0.37	mS
			= 1100_B	6, 0.21	9.62, 0.29	14.11, 0.44	mS
			= 1101_B	7.28, 0.24	11.64, 0.34	17.1, 0.51	mS
			= 1110_B	8.81, 0.28	14.02, 0.4	20.61, 0.59	mS
			= 1111_B	9.49, 0.31	15.15, 0.44	22.12, 0.65	mS
X1 clock Input frequency	f_{EX}*1	EXCLK mode		7.9		24.0	MHz
X1 clock Input cycle time	t_{EXCYC}	EXCLK mode		41.7		126.6	ns
X1 High level Input voltage	V_{IH}			0.8 × SYSVCC		SYSVCC + 0.3	V
X1 Low level Input voltage	V_{IL}			–0.3		0.2 × SYSVCC	V
X1 Input leakage current	I_{LIH}	VI = SYSVCC				0.5	µA
	I_{LIL}	VI = 0 V				–0.5	µA
X1 clock Input low level pulse width	t_{EXL}	EXCLK mode	f_{EX} = 8 MHz	58			ns
			f_{EX} = 16 MHz	26			ns
			f_{EX} = 20 MHz	20			ns
			f_{EX} = 24 MHz	16			ns

Table 3.3 Main Oscillator Characteristics (3/3)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
X1 clock Input high level pulse width	t_{EXH}	EXCLK mode	f_{EX} = 8 MHz	58			ns
			f_{EX} = 16 MHz	26			ns
			f_{EX} = 20 MHz	20			ns
			f_{EX} = 24 MHz	16			ns
X1 clock rise time	t_{EXR}	EXCLK mode	f_{EX} = 8 MHz			4	ns
			f_{EX} = 16 MHz			4	ns
			f_{EX} = 20 MHz			4	ns
			f_{EX} = 24 MHz			3	ns
X1 clock fall time	t_{EXF}	EXCLK mode	f_{EX} = 8 MHz			4	ns
			f_{EX} = 16 MHz			4	ns
			f_{EX} = 20 MHz			4	ns
			f_{EX} = 24 MHz			3	ns
X1 clock Input total jitter (Dj + 14 × rms Random jitter)	t_{CITJ}	The clock source of SGMII used @ 20MHz				73*6	ps peak to peak
X1 Input capacitance	C_{X1}	Main OSC. EXCLK mode, MOSC_CAP_SEL = 0010				10	pF

Note 1. To reach internal usable clocks only following 4 frequencies are supported: 8MHz, 16MHz, 20MHz and 24MHz. Tolerance of external quartz crystal is assumed as +/–1%.
When ETNF is used, Ethernet grade crystal will need to be used to be compliant with the standard frequency tolerance.

Note 2. The StartUp is supported without external components under following conditions:
• See the RH850/U2C Group User's Manual: Hardware Section 53.12.15, OPBT10 — Option Byte 10 for default values of drivability, damping resistance and internal capacitance.
• Specification covers a maximum external stray capacitance of up to 6pF to each pin X1 and X2.
• After StartUp drivability and capacitance will be configured by OPBT10
• A possible exceeding of the recommended maximum drive level for a crystal for all start-up phases has to be agreed with the crystal manufacturers separately.

Note 3. Ccapsel_x1 (Ccapsel_x1 including parasitic capacitance to ground at the X1 side), Ccapsel_x2 (Ccapsel_x2 including parasitic capacitance to ground at the X2 side).

Note 4. The capacitor tolerance is ±15%.

Note 5. The clock source of SGMII used. Ethernet grade crystal is mandatory. Example: CX3225GA(KYOCERA)

Note 6. 12 kHz to 20 MHz rms jitter = 3 ps.

CAUTION

Oscillation stabilization times differ according to matching with the resonator. Secure an oscillation stabilization time determined through evaluation of matching.

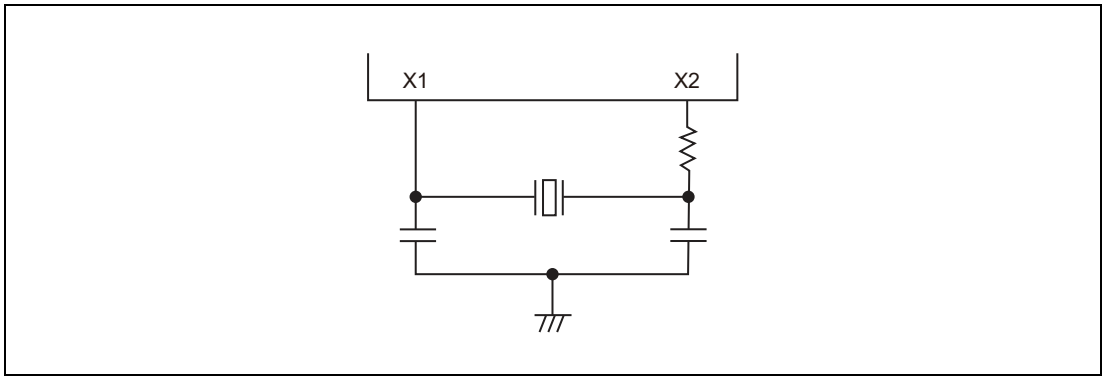


Figure 3.1 Oscillator Circuit Diagram (Crystal with External Components)

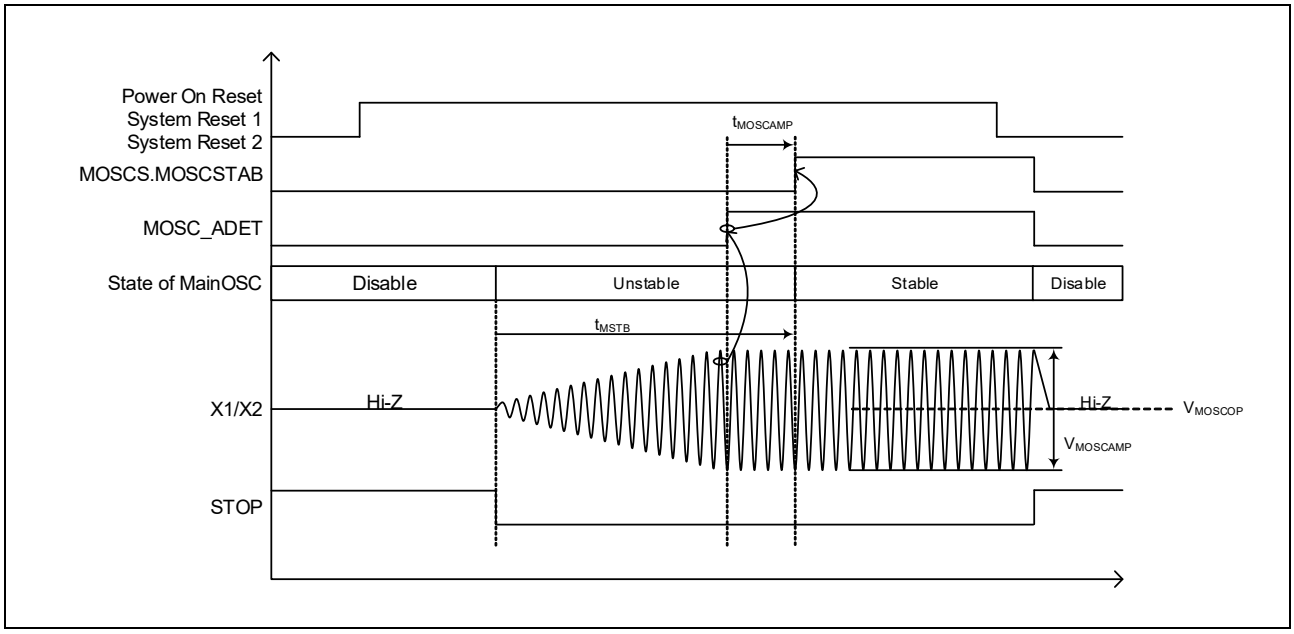


Figure 3.2 Main OSC Stabilization

3.2.1.3 Sub Oscillator Characteristics

Table 3.4 Sub Oscillator Characteristics

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
SubOSC frequency	f_{SOSC}	Crystal		30	32.768	38	kHz
SubOSC current consumption	I_{SOSC}	After	Standard Mode		1.4*2	6*2	µA
			High drive mode		2*2	8*2	µA
SubOSC DC operating point	$V_{SOSCDCOP}$				0.64*2		V
SubOSC oscillation stabilization time	t_{SSTB}				*1		s

Note 1. Oscillator stabilization time is time until being set (“1”) in SOSCS.SOSCSTAB bit after SOSCE.SOSCENTRG bit is written “1”, and depends on the setting value of SOSCST register. Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

Note 2. This is reference value.

CAUTION

The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

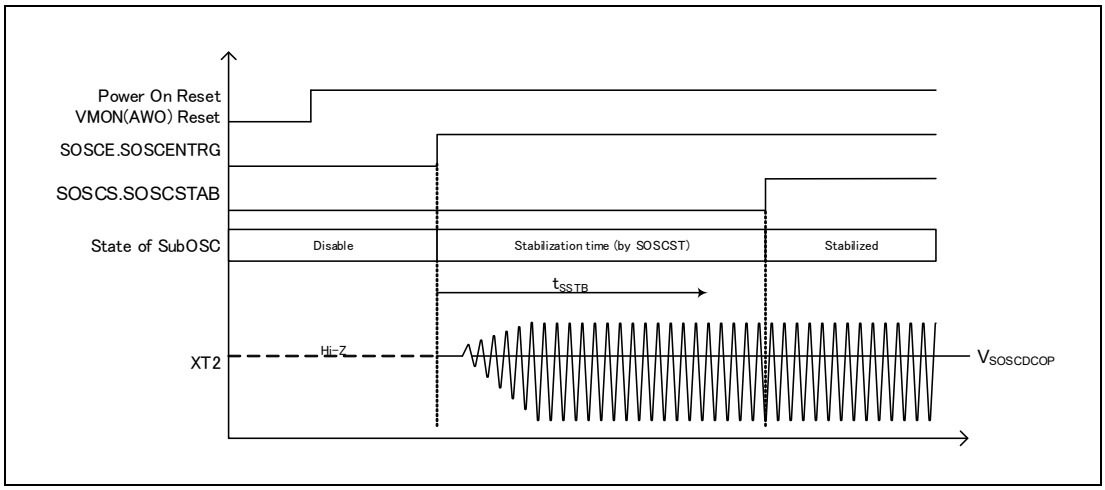


Figure 3.3 Sub OSC Stabilization

3.2.1.4 Internal Oscillator Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.5 Internal Oscillator Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		29.491	32.768	36.045	kHz
HS IntOSC frequency	f_{RH}		192	200	208	MHz
HS IntOSC frequency	f_{RH}	After user trimming @ trimming temp[*1]	198	200	202	MHz

Note 1. Trimming temperature is Tj.

3.2.1.5 PLL Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.6 PLL Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL output long term jitter*1	t_{PLLLTJ}	Term = 1 µs	–500		500	ps
		Term = 20 µs	–1		1	ns
PLL lock time*2	t_{PLLLCT}		201		222	µs

Note 1. This characteristic is not tested in production.
Note 2. Lock time is time until being set “1” in PLLS.PLLCLKSTAB bit after PLLE.PLLENTRG bit is written “1”.

Table 3.7 SSCG PLL Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Modulation frequency	f_{mod}		20		60	kHz
Frequency dithering range*1	f_{dit}	SELMPERCENT = 000	0.9	0.95	0.995	%
		SELMPERCENT = 001	1.64	2.0	2.36	%
		SELMPERCENT = 010	2.46	3.0	3.54	%
		SELMPERCENT = 011	3.28	4.0	4.72	%
		SELMPERCENT = 100	4.10	5.0	5.90	%
PLL lock time	t_{PLLLCT}		201		222	µs

Note 1. Dithered frequency mode is only supported in down spread mode.

Table 3.8 RHSIF PLL Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL lock time	$t_{RHPLLLCT}$				50	µs

3.2.1.6 Regulator Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.9 Regulator Characteristics

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output voltage	V_{AWOVCL}	AWOVCL pin		1.025	1.09	1.155	V
	V_{ISOVCL}	ISOVCL pin		1.025	1.09	1.155	V
	$V_{GETH0VCL}$	GETH0VCL pin		1.025	1.09	1.155	V
Capacitance*7	C_{AWOVCL}	AWOVCL pin		0.14	0.2	0.286	µF
	C_{ISOVCL}*1	ISOVCL pin V_{VCC} = V_{POC} to 3.6V [For U2C4 QFP Only]		0.329 × 4pcs	0.47 × 4pcs	0.611 × 4pcs	µF/pcs
		ISOVCL pin V_{VCC} = V_{POC} to 3.6V [For U2C4 BGA Only]		0.329 × 5pcs	0.47 × 5pcs	0.611 × 5pcs	µF/pcs
		ISOVCL pin V_{VCC} = 4.5 to 5.5V [For U2C4 QFP Only]		0.329 × 4pcs	0.47 × 4pcs	0.611 × 4pcs	µF/pcs
		ISOVCL pin V_{VCC} = 4.5 to 5.5V [For U2C4 BGA Only]		0.154 × 5pcs	0.22 × 5pcs	0.286 × 5pcs	µF/pcs
		ISOVCL pin [For U2C2 Only]		0.329 × 4pcs	0.47 × 4pcs	0.611 × 4pcs	µF/pcs
	$C_{GETH0VCL}$	GETH0VCL pin		0.154	0.22	0.286	µF
Equivalent series resistance for capacitance*1	R_{VRAWO}	for C_{AWOVCL}				40*2	mΩ
	R_{VRISO}	for C_{ISOVCL}				40*2	mΩ
	$R_{VRGETH0}$	for $C_{GETH0VCL}$				40*2	mΩ
Resistance	R_{ISOVCL}	ISOVCL pin Vcc = 4.5 to 5.5V [For U2C4 QFP Only]		2.09 × 4pcs	2.2 × 4pcs	2.31 × 4pcs	Ω/pcs
		ISOVCL pin Vcc = 4.5 to 5.5V [For U2C4 BGA Only]		2.09 × 5pcs	2.2 × 5pcs	2.31 × 5pcs	Ω/pcs
Inrush current during power-on	$I_{RUSYSVCC}$	SYSVCC*4				350*3	mA
	I_{RUVCC}	VCC*5 V_{VCC} = V_{POC} to 3.6V				150	mA/20µs
		VCC*5 V_{VCC} = V_{POC} to 5.5V				230	mA/20µs
		VCC*6 V_{VCC} = V_{POC} to 3.6V				150	mA/20µs
		VCC*6 V_{VCC} = 4.5 to 5.5V				230	mA/20µs
	$I_{RUGETH0PVCC}$	GETH0PVCC				100*2	mA
Operating current variation*8*9	ΔI	I_{ISOVDD_R} [For U2C4 eVR and U2C2 Only]	CyclicRUN mode			30	mA/20µs
			Other than above			50	mA/20µs

Note 1. External capacitor have to meet this specification at the simplified model which is not included frequency dependence.

Note 2. This is reference value.

Note 3. The time of current flow is less than 2.5 µs.
Note 4. For U2C8 only.
Note 5. For U2C2 only.
Note 6. For U2C4 eVR only.
Note 7. Minimum and maximum value of capacitance include initial tolerance and deratings of temperature, voltage and aging. And low ESR ceramic capacitor (e.g., X7R, X8R) must be used. C_{ISOVCL} is specified total capacitance to the ISOVCL pins for the device, it has to be distributed evenly to all ISOVCL pins.
Note 8. Operating current variation filtered by simple moving average of 10us window can be ignored.
Note 9. ISOVDD supply current of eVR is the part of VCC supply current.

3.2.2 Input Voltage Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.10 Input Voltage Characteristics (Input Voltage IOVCC = 3.0 to 5.5V)

Item	Symbol	Condition*1	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	SHMT1, IOVCC = 3.0 to 5.5 V	0.65 × IOVCC		IOVCC + 0.3	V
	V_{IH2}	SHMT2, IOVCC = 3.0 to 5.5 V	0.75 × IOVCC		IOVCC + 0.3	V
	V_{IH3}	SHMT4, IOVCC = 3.0 to 5.5 V	0.80 × IOVCC		IOVCC + 0.3	V
	V_{IH4}	TTL, IOVCC = 3.0 to 5.5 V	2.2		IOVCC + 0.3	V
Low level input voltage	V_{IL1}	SHMT1, IOVCC = 3.0 to 5.5 V	–0.3		0.35 × IOVCC	V
	V_{IL2}	SHMT2, IOVCC = 3.0 to 5.5 V	–0.3		0.25 × IOVCC	V
	V_{IL3}	SHMT4, IOVCC = 3.0 to 5.5 V	–0.3		0.50 × IOVCC	V
	V_{IL4}	TTL, IOVCC = 3.0 to 5.5 V	–0.3		0.8	V
Input hysteresis for Schmitt*3	V_{HS1}	SHMT1, IOVCC = 4.5 to 5.5 V	0.4			V
		SHMT1, IOVCC = 3.0 to 4.5 V	0.3			V
	V_{HS2}	SHMT2, IOVCC = 3.0 to 5.5 V	0.2 × IOVCC			V
	V_{HS3}	SHMT4, IOVCC = 3.0 to 5.5 V	0.1			V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. For X1 pin, see **Section 3.2.1.2, Main Oscillator Characteristics**.

Note 3. The configured drive strength of the output terminals in a power group might affect the hysteresis characteristics of the input terminals in the same power group. See Appendix file "*E02_01_List_of_Pin_Assignment.xlsx*" for the assignment of the power group.

Table 3.11 Input Voltage Characteristics (Input Voltage IOVCC = VPOC to 3.0V)

Item	Symbol	Condition*1	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	SHMT1, IOVCC = VPOC to 3.0 V	0.7 × IOVCC		IOVCC + 0.3	V
	V_{IH2}	SHMT2, IOVCC = VPOC to 3.0 V	0.77 × IOVCC		IOVCC + 0.3	V
	V_{IH3}	SHMT4, IOVCC = VPOC to 3.0 V	0.81 × IOVCC		IOVCC + 0.3	V
	V_{IH4}	TTL, IOVCC = VPOC to 3.0 V	2.2		IOVCC + 0.3	V
Low level input voltage	V_{IL1}	SHMT1, IOVCC = VPOC to 3.0 V	–0.3		0.35 × IOVCC	V
	V_{IL2}	SHMT2, IOVCC = VPOC to 3.0 V	–0.3		0.25 × IOVCC	V
	V_{IL3}	SHMT4, IOVCC = VPOC to 3.0 V	–0.3		0.50 × IOVCC	V
	V_{IL4}	TTL, IOVCC = VPOC to 3.0 V	–0.3		0.8	V
Input hysteresis for Schmitt	V_{HS1}	SHMT1, IOVCC = VPOC to 3.0 V	0.25			V
	V_{HS2}	SHMT2, IOVCC = VPOC to 3.0 V	0.2 × IOVCC			V
	V_{HS3}	SHMT4, IOVCC = VPOC to 3.0 V	0.03			V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "E02_01_List_of_Pin_Assignment.xlsx" for the power supply of each pin.

Note 2. For X1 pin, see **Section 3.2.1.2, Main Oscillator Characteristics**.

3.2.3 Input Leakage Current

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.12 Input Leakage Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LIH1}	Vin = 0 to EnVCC • Pn_m (Except P20_0, P20_1, P20_12, P20_13)	Tj ≤ 105°C			0.5	µA
			105°C < Tj ≤ 150°C			1.0	µA
			150°C < Tj			2.0	µA
	I_{LIH2}	Vin = 0 to EnVCC • P20_0, P20_1, P20_12, P20_13	Tj ≤ 105°C			0.5	µA
			105°C < Tj			2.0	µA
	I_{LIH3}	Vin = 0 to AnVREFH • APn_m	Tj ≤ 150°C			0.5	µA
			150°C < Tj			1.0	µA
	I_{LIL1}	Vin = 0 to EnVCC • Pn_m (Except P20_0, P20_1, P20_12, P20_13)	Tj ≤ 105°C			–0.5	µA
			105°C < Tj ≤ 150°C			–1.0	µA
			150°C < Tj			–2.0	µA
	I_{LIL2}	Vin = 0 to EnVCC • P20_0, P20_1, P20_12, P20_13	Tj ≤ 105°C			–0.5	µA
			105°C < Tj			–2.0	µA
	I_{LIL3}	Vin = 0 to AnVREFH • APn_m	Tj ≤ 150°C			–0.5	µA
			150°C < Tj			–1.0	µA

3.2.4 Pull-up/Pull-down Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.13 Pull-up/Pull-down Characteristics (IOVCC = 3.0 to 5.5V)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input pull-up current source	I_{PU1}		IOVCC*1 = 3.0 to 5.5V, Vin = 0V	30		350	µA
Input pull-down current source	I_{PD1}	Other than the below	IOVCC*1 = 3.0 to 5.5V, Vin = IOVCC*1	30		350	µA
	I_{PD2}	$\overline{\text{RESET}}$, $\overline{\text{AURORES}}$	IOVCC*1 = 3.0 to 5.5V, Vin = IOVCC*1			110	µA

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Table 3.14 Pull-up/Pull-down Characteristics (IOVCC = VPOC to 3.0V)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input pull-up current source	I_{PU1}		IOVCC*1 = VPOC to 3.0V, Vin = 0V	18		350	µA
Input pull-down current source	I_{PD1}	Other than the below	IOVCC*1 = VPOC to 3.0V, Vin = IOVCC*1	18		350	µA
	I_{PD2}	$\overline{\text{RESET}}$, $\overline{\text{AURORES}}$	IOVCC*1 = VPOC to 3.0V, Vin = IOVCC*1			110	µA

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "E02_01_List_of_Pin_Assignment.xlsx" for the power supply of each pin.

3.2.5 Output Voltage Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.15 Output Voltage Characteristics (IOVCC = 3.0 to 5.5V)

Item	Symbol	Condition*1		MIN.*1	TYP.	MAX.	Unit
Output resistance	R_{O11}	Drive strength = 1	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	6		40	Ω
	R_{O12}	Drive strength = 2	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	11		72	Ω
	R_{O13}	Drive strength = 3	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	18		100	Ω
	R_{O14}	Drive strength = 4	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	32		200	Ω
	R_{O15}	Drive strength = 5	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	61		400	Ω
High level output voltage	V_{OH1}	Drive strength = 1 IOVCC = 3.0 to 5.5 V	I_{OH} = –4 mA / pin (4 output pins)*2	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (4 output pins)*2	IOVCC–0.5			V
	V_{OH2}	Drive strength = 2 IOVCC = 3.0 to 3.6 V	I_{OH} = –4 mA / pin (8 output pins)*2	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (8 output pins)*2	IOVCC–0.5			V
		Drive strength = 2 IOVCC = 3.6 to 5.5 V	I_{OH} = –4 mA / pin (2 output pins)*2	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (2 output pins)*2	IOVCC–0.5			V
	V_{OH3}	Drive strength = 3 IOVCC = 3.0 to 5.5 V	I_{OH} = –4 mA / pin (8 output pins)*2	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (8 output pins)*2	IOVCC–0.5			V
	V_{OH4}	Drive strength = 4 IOVCC = 3.0 to 5.5 V	I_{OH} = –2 mA / pin (16 output pins)*2	IOVCC–0.7			V
			I_{OH} = –1 mA / pin (16 output pins)*2	IOVCC–0.5			V
	V_{OH5}	Drive strength = 5 IOVCC = 3.0 to 5.5 V	I_{OH} = –1 mA / pin (16 output pins)*2	IOVCC–0.7			V
			I_{OH} = –500 µA / pin (16 output pins)*2	IOVCC–0.5			V
Low level output voltage	V_{OL1}	Drive strength = 1 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (4 output pins)*2			0.8	V
			I_{OL} = 2 mA / pin (4 output pins)*2			0.5	V
	V_{OL2}	Drive strength = 2 IOVCC = 3.0 to 3.6 V	I_{OL} = 4 mA / pin (8 output pins)*2			0.8	V
			I_{OL} = 2 mA / pin (8 output pins)*2			0.5	V
		Drive strength = 2 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (2 output pins)*2			0.8	V
			I_{OL} = 2 mA / pin (2 output pins)*2			0.5	V
	V_{OL3}	Drive strength = 3 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (8 output pins)*2			0.7	V
			I_{OL} = 2 mA / pin (8 output pins)*2			0.5	V
	V_{OL4}	Drive strength = 4 IOVCC = 3.0 to 5.5 V	I_{OL} = 2 mA / pin (16 output pins)*2			0.7	V
			I_{OL} = 1 mA / pin (16 output pins)*2			0.5	V
	V_{OL5}	Drive strength = 5 IOVCC = 3.0 to 5.5 V	I_{OL} = 1 mA / pin (16 output pins)*2			0.7	V
			I_{OL} = 500 µA / pin (16 output pins)*2			0.5	V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix "*E02_01_List_of_Pin_Assignment.xlsx*" for the power supply of each pin.

Note 2. The number of pin indicates simultaneous ON in one power. The influence of the noise emission should be considered when switching the output level.

Table 3.16 Output Voltage Characteristics (IOVCC = VPOC to 3.0V)

Item	Symbol	Condition[*1]		MIN.[*1]	TYP.	MAX.	Unit
Output resistance	R_{O11}	Drive strength = 1	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	6		50	Ω
	R_{O12}	Drive strength = 2	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	11		90	Ω
	R_{O13}	Drive strength = 3	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	18		150	Ω
	R_{O14}	Drive strength = 4	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	32		300	Ω
	R_{O15}	Drive strength = 5	IOVCC – V_{OH} = 0.4 V, V_{OL} = 0.4 V	61		580	Ω
High level output voltage	V_{OH1}	Drive strength = 1 IOVCC = 3.0 to 5.5 V	I_{OH} = –4 mA / pin (4 output pins)[*2]	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (4 output pins)[*2]	IOVCC–0.5			V
	V_{OH2}	Drive strength = 2 IOVCC = 3.0 to 3.6 V	I_{OH} = –4 mA / pin (8 output pins)[*2]	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (8 output pins)[*2]	IOVCC–0.5			V
		Drive strength = 2 IOVCC = 3.6 to 5.5 V	I_{OH} = –4 mA / pin (2 output pins)[*2]	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (2 output pins)[*2]	IOVCC–0.5			V
	V_{OH3}	Drive strength = 3 IOVCC = 3.0 to 5.5 V	I_{OH} = –4 mA / pin (8 output pins)[*2]	IOVCC–0.8			V
			I_{OH} = –2 mA / pin (8 output pins)[*2]	IOVCC–0.5			V
	V_{OH4}	Drive strength = 4 IOVCC = 3.0 to 5.5 V	I_{OH} = –2 mA / pin (16 output pins)[*2]	IOVCC–0.73			V
			I_{OH} = –1 mA / pin (16 output pins)[*2]	IOVCC–0.5			V
	V_{OH5}	Drive strength = 5 IOVCC = 3.0 to 5.5 V	I_{OH} = –1 mA / pin (16 output pins)[*2]	IOVCC–0.73			V
			I_{OH} = –500 µA / pin (16 output pins)[*2]	IOVCC–0.5			V
Low level output voltage	V_{OL1}	Drive strength = 1 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (4 output pins)[*2]			0.8	V
			I_{OL} = 2 mA / pin (4 output pins)[*2]			0.5	V
	V_{OL2}	Drive strength = 2 IOVCC = 3.0 to 3.6 V	I_{OL} = 4 mA / pin (8 output pins)[*2]			0.8	V
			I_{OL} = 2 mA / pin (8 output pins)[*2]			0.5	V
		Drive strength = 2 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (2 output pins)[*2]			0.8	V
			I_{OL} = 2 mA / pin (2 output pins)[*2]			0.5	V
	V_{OL3}	Drive strength = 3 IOVCC = 3.0 to 5.5 V	I_{OL} = 4 mA / pin (8 output pins)[*2]			0.7	V
			I_{OL} = 2 mA / pin (8 output pins)[*2]			0.5	V
	V_{OL4}	Drive strength = 4 IOVCC = 3.0 to 5.5 V	I_{OL} = 2 mA / pin (16 output pins)[*2]			0.7	V
			I_{OL} = 1 mA / pin (16 output pins)[*2]			0.5	V
	V_{OL5}	Drive strength = 5 IOVCC = 3.0 to 5.5 V	I_{OL} = 1 mA / pin (16 output pins)[*2]			0.7	V
			I_{OL} = 500 µA / pin (16 output pins)[*2]			0.5	V

Note 1. "IOVCC" means power supply voltage for I/O ports. See the appendix “E02_01_List_of_Pin_Assignment.xlsx” for the power supply of each pin.

Note 2. The number of pin indicates simultaneous ON in one power. The influence of the noise emission should be considered when switching the output level.

3.2.6 Output Current

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.17 Output Current Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level output current	$\|I_{OH}\|$	per pin			8	mA
	$\Sigma\|I_{OH}\|$ EnVCC	Each EnVCC			60	mA
	$\Sigma\|I_{OH}\|$ AnVREFH	Each AnVREFH			16	mA
Low level output current	$\|I_{OL}\|$	per pin			8	mA
	$\Sigma \|I_{OL}\|$ EnVCC	Each EnVCC			60	mA
	$\Sigma \|I_{OL}\|$ AnVREFH	Each AnVREFH			16	mA

3.2.7 Injection Current Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.18 Injection Current Operating Conditions

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DC injection current (per pin)	I_{INJ_DIN}	Digital pin *1	–2		3	mA
	I_{INJ_AIN}	Analogue pin	–3		3	mA
DC injection current (each power supply)	I_{INJ_E0VCC}	E0VCC			50	mA
	I_{INJ_E1VCC}	E1VCC			50	mA
	I_{INJ_E2VCC}	E2VCC			30	mA
	$I_{INJ\_AAVREFH}$	AAVREFH			20	mA
	$I_{INJ\_A1VREFH}$	A1VREFH			20	mA
	$I_{INJ\_A2VREFH}$	A2VREFH			20	mA
DC injection current (total)	I_{INJ_TOTAL}				80	mA

Note 1. Injection current to the logic pin multiplied with LVDS function is prohibited when LVDS function is used. When LVDS function is not used, Injection current to the logic pin multiplied with LVDS function causes at maximum additional 1 µA leakage current at the P/N combinational pin. For example, injection current to HSIFD_TXDP causes at maximum additional 1 µA leakage current at HSIFD_TXDN.

NOTE

- Input voltage must be kept within –0.8V ≤ Vin ≤ 6.0V, if injection current is kept within rated value.
- Power supply voltage must be kept within operating conditions.
- Injection current effects power dissipation in the package for thermal characteristics.

3.2.8 LVDS Characteristics

3.2.8.1 LVDS Driver Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.19 LVDS Driver Characteristics (based on IEEE 1596.3-1996 Reduced)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output low-level voltage	V_{LVDSOL}		1000			mV
Output high-level voltage	V_{LVDSOH}				1400	mV
Output differential voltage	V_{LVDSOD}		150		250	mV
Offset voltage	V_{LVDSOS}		1.125		1.275	V
Output impedance	R_{LVDSOI}		40		300	Ω

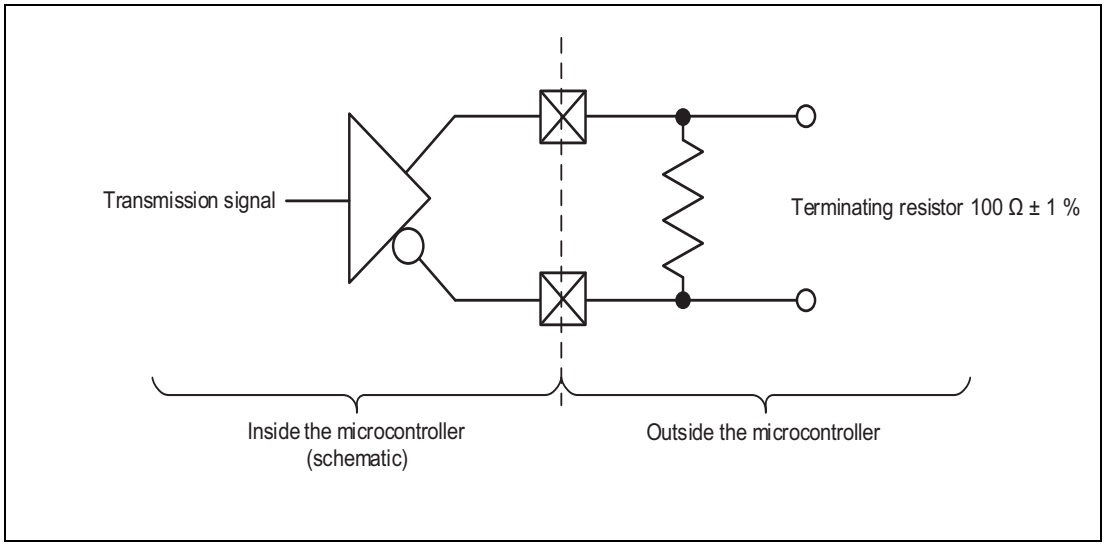


Figure 3.4 LVDS Driver Measurement Conditions

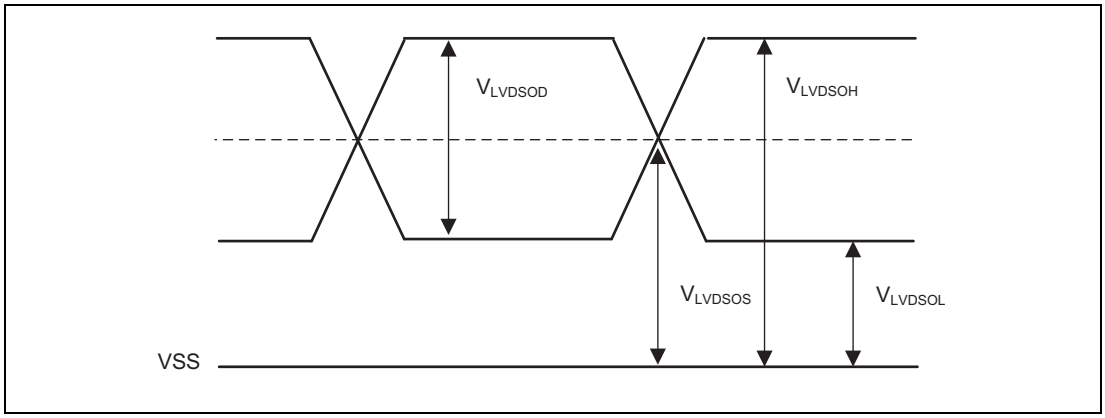


Figure 3.5 Meaning of LVDS Driver Symbols

Table 3.20 DC Characteristics (LVDS Driver (ANSI/TIA/EIA-644 standard) Characteristics)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output differential voltage	V_{OD}		250	—	450	mV
Offset voltage	V_{OS}		1125	—	1375	mV

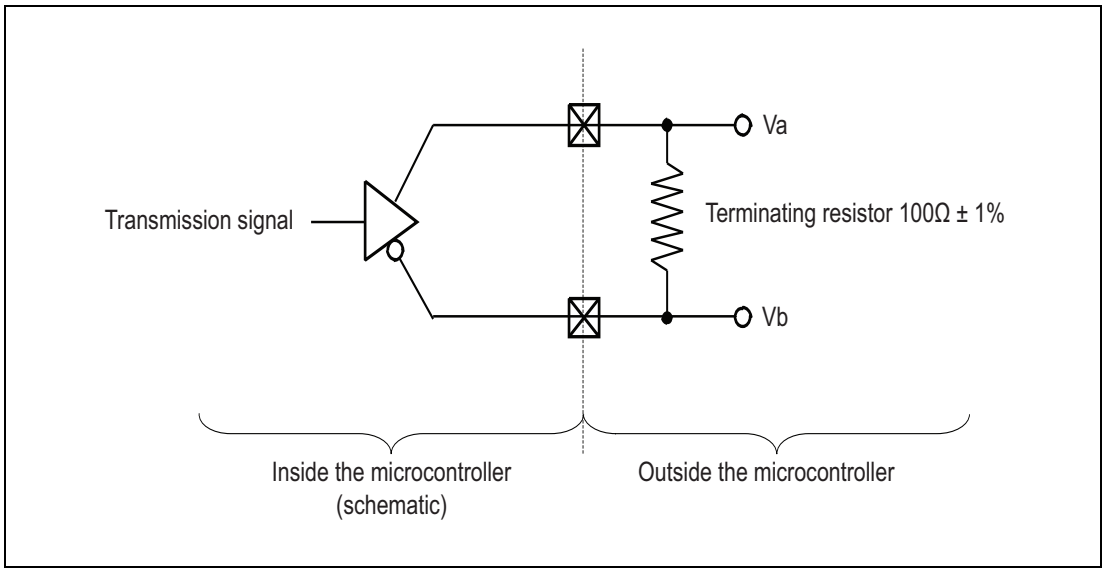


Figure 3.6 LVDS Driver Va / Vb Measurement Conditions

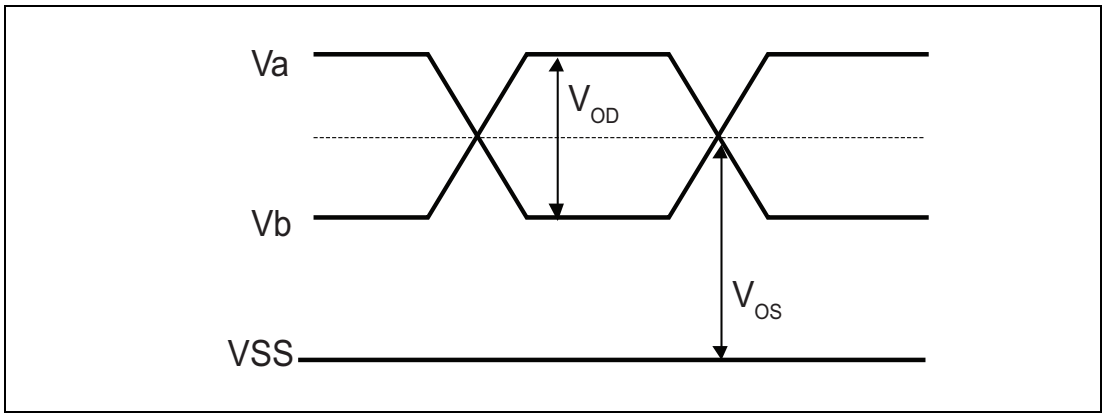


Figure 3.7 Definition of LVDS Driver Symbols

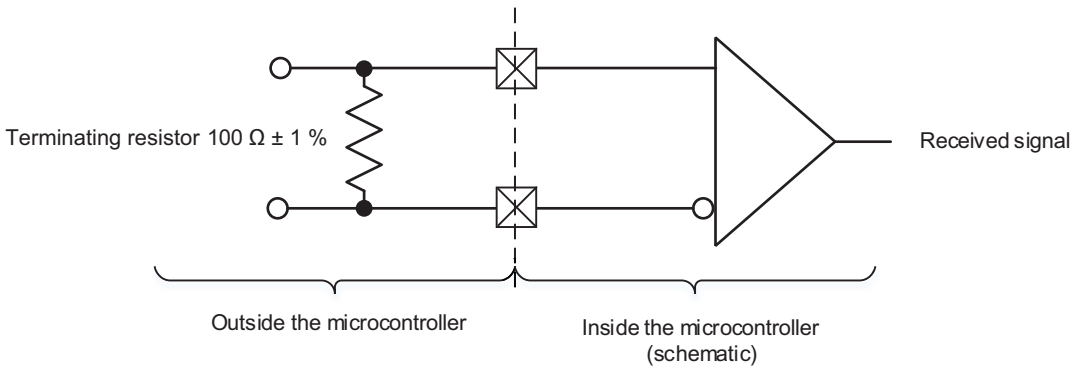
3.2.8.2 LVDS Receiver Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.21 LVDS Receiver Characteristics (based on ANSI/TIA/EIA-644)

Parameter	Symbol	Condition	MIN.	TYP.	MAX	Unit
Differential Input threshold voltage	$V_{LVDSIDTH}$		–100		100	mV
Input voltage range	V_{LVDI}		0.5		2.0	V



Note: Be sure to connect a terminating resistor of the LVDS receiver nearest the microcontroller, because it isn't built in the microcontroller.

Figure 3.8 LVDS Receiver Measurement Conditions

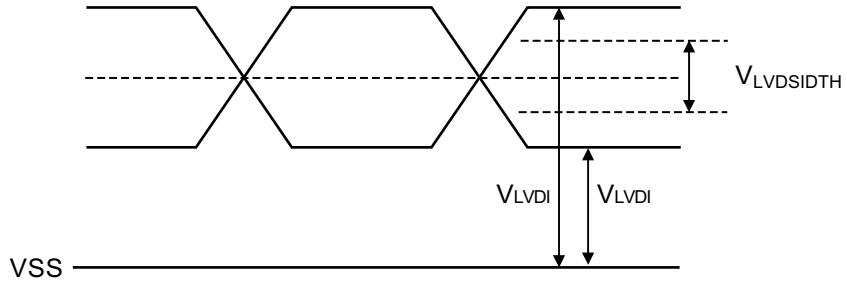


Figure 3.9 Meaning of LVDS Receiver Symbols

3.2.9 SGMII Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.22 SGMII REFCK Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.0		GETH0BVCC + 0.3	V
Low level input voltage	V_{IL}		–0.3		0.8	V

Table 3.23 SGMII Tx Buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V_{OH}				1525	mV
Output voltage low	V_{OL}		875			mV
Output Differential Voltage	$\|V_{OD}\|$		150		400	mV
Output Offset Voltage	V_{OS}		1075		1325	mV
Change in V_{OD} between “0” and “1”	$\Delta\|V_{OD}\|$				25	mV
Change in V_{OS} between “0” and “1”	ΔV_{OS}				25	mV
Output current on Short to GND	I_{sa}, I_{sb}				40	mA
Output current when a, b are shorted	I_{sab}				12	mA

Note 1. For a detailed description of the symbols, please refer to the IEEE1596.3-1996 standard.
Note 2. All parameters measured at Rload = 100 Ω ±1 % load

Table 3.24 SGMII Rx Buffer Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Voltage range a or b	V_I		675		1725	mV
Input differential threshold	V_{idth}		–50		50	mV
Receiver differential input impedance	R_{in}		80		120	Ω

Note 1. For a detailed description of the symbols please refer to the IEEE1596.3-1996 standard.

3.2.10 Aurora Interface Clock Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.25 Aurora Interface Clock Characteristics (CICREFP, CICREFN)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential input voltage	$V_{DIFFCIC}$ *1		200		1600	mV
External AC coupling capacitor	C_{ACC}		75	100	200	nF
Differential input resistance	$Z_{DIFFCIC}$		70	100	130	Ω

Note 1. Peak to peak differential input voltage.

Table 3.26 Aurora Interface Characteristics (TODP0-1/TODN0-1)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential output voltage	$V_{DIFFTOD}$ *1		800		1600	mV
Differential output resistance	$Z_{DIFFTOD}$		70		130	Ω

Note 1. Peak to peak differential input voltage.

3.2.11 IO Capacitances

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.27 IO Capacitances *1, *2, *3

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V for non measurement pins			10	pF
Input/output capacitance	C_{IO}				10	pF
Output capacitance	C_O				10	pF

Note 1. This capacity is the capacity value per BGA_Ball 1 terminal.
Note 2. X1 and X2 are excluded. About X1 and X2 configuration, see the RH850/U2C Group User's Manual: Hardware Section 13, Clock Controller.
Note 3. For analog input pins (ADCKnIm and ADCKnImS), refer to **Section 3.4, A/D Converter Characteristics**.

3.2.12 Supply Current Characteristics

3.2.12.1 General Definition

Power consumption except for the current of I/O buffer (I_{EnVCC}) is specified below.
The parameter I_{EnVCC} depends on customer's application and thus need to be defined by customer in order to determine the total power dissipation of a device

3.2.12.2 Power Supply Currents

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.28 Current consumption for RH850/U2C8[*2]

Item	Symbol	Power supply		CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
RUN mode current	I_{VCC_R}[*12]	SYSVCC and VCC[*3] SYSVCC=VCC=5.5V		320 MHz		32	50	mA
				240 MHz		32	50	mA
				160 MHz		32	50	mA
			BIST			32	50	mA
	I_{VDD_R}	ISOVDD		320 MHz		252	600	mA
				240 MHz		206	540	mA
				160 MHz		180	510	mA
			BIST			240	580	mA
STOP mode current[*5]	I_{VCC_S}[*12]	SYSVCC and VCC SYSVCC=VCC=5.5V	Tj = 25°C			2.5	3.1	mA
			Tj = 160°C				10	mA
	I_{VDD_S}	ISOVDD	Tj = 25°C			5.8	14.8	mA
			Tj = 160°C				334	mA
DeepSTOP mode current[*6]	I_{VCC_DS}[*11*12]	SYSVCC and VCC SYSVCC=VCC=5.5V	Tj = 25°C			82[*8]	164[*9]	uA
			Tj = 160°C				2.8[*10]	mA
	I_{VDD_DS}[*4]	ISOVDD	Tj = 25°C			6	14.1	mA
			Tj = 160°C				334	mA
Cyclic RUN mode current[*7]	I_{VCC_CR}[*11*12]	SYSVCC and VCC SYSVCC=VCC=5.5V	Tj = 25°C	10 MHz		1.9	2.4	mA
			Tj = 160°C	10 MHz			5.8	mA
		SYSVCC and VCC SYSVCC=VCC=5.5V	Tj = 25°C	100 MHz		3.2	4.4	mA
			Tj = 160°C	100 MHz			11	mA
	I_{VDD_CR}	ISOVDD	Tj = 25°C	10 MHz		9.2	20.4	mA
			Tj = 160°C	10 MHz			313	mA
			Tj = 25°C	100 MHz		35	44	mA
			Tj = 160°C	100 MHz			370	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- EnVCC = AnVREFH = 5.0 V
- GETH0PVCC = GETH0BVCC = 3.3 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of I/O buffer.

Note 3. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.

Note 4. Indicated leak current will be applied if the power continues supplying to ISOVDD during DeepSTOP mode.

Note 5. Only LS IntOSC is operated.

Note 6. Only LS IntOSC is operated. Size of Retention RAM is 16KB.

Note 7. Only LS IntOSC, HS IntOSC and CPU(PE0) are operated.

Note 8. It will increase 6 µA if size of Retention Ram is 32KB.

Note 9. It will increase 6 µA if size of Retention Ram is 32KB.

Note 10. It will increase 0.1 mA if size of Retention Ram is 32KB.

Note 11. Power supply mode of AWOVDC is Low Power Mode (AWOPSM.AWOPSM = 1).
Note 12. This value is the sum of the SYSVCC current and the VCC current.

Table 3.29 Current consumption for RH850/U2C8-EVA (ISOVDD and specific power supply)*1

Item	Symbol	Power supply	CPU frequency	MIN.	TYP.*1	MAX.	Unit
RUN mode current	I_{VDD_R}	ISOVDD	320 MHz			670	mA
EMUVCC	I_{EMUVCC}					15.2	mA
EMUVDD	I_{EMUVDD}					205	mA
HSFD0VCC	$I_{HSFD0VCC}$				24	40	mA

Note 1. Reference value

Table 3.30 Current consumption for RH850/U2C4[*2] (1/2)

Item	Symbol	Power supply		CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
RUN mode current	I_{VCC_R}[*13]	SYSVCC and VCC[*3] SYSVCC=VCC=5.5V eVR		320 MHz		297	509	mA
				240 MHz		247	456	mA
				160 MHz		210	438	mA
			BIST			237	489	mA
		SYSVCC and VCC[*3] SYSVCC=VCC=3.6V eVR		320 MHz		297	509	mA
				240 MHz		247	456	mA
				160 MHz		210	438	mA
			BIST			237	489	mA
		SYSVCC and VCC[*3] SYSVCC=VCC=5.5V DPS		320 MHz		32	44	mA
				240 MHz		32	44	mA
				160 MHz		32	44	mA
			BIST			32	44	mA
	I_{VDD_R}	ISOVDD DPS		320 MHz		238	420	mA
				240 MHz		188	383	mA
				160 MHz		151	360	mA
			BIST			163	400	mA
STOP mode current[*5]	I_{VCC_S}[*13]	SYSVCC and VCC SYSVCC=VCC=5.5V eVR	Tj = 25°C			20	27	mA
			Tj = 160°C				282	mA
		SYSVCC and VCC SYSVCC=VCC=3.6V eVR	Tj = 25°C			20	27	mA
			Tj = 160°C				282	mA
		SYSVCC and VCC SYSVCC=VCC=5.5V DPS	Tj = 25°C			2.5	3.1	mA
			Tj = 160°C				10	mA
	I_{VDD_S}	ISOVDD DPS	Tj = 25°C			3.9	8.4	mA
			Tj = 160°C				240	mA

Table 3.30 Current consumption for RH850/U2C4[*2] (2/2)

Item	Symbol	Power supply		CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
DeepSTOP mode current[*4, *6]	I_{VCC_DS}[*11*13]	SYSVCC and VCC SYSVCC=VCC=5.5V eVR	Tj = 25°C			82*[8]	142*[9]	µA
			Tj = 160°C				2.5*[10]	mA
		SYSVCC and VCC SYSVCC=VCC=3.6V eVR	Tj = 25°C			82*[8]	142*[9]	µA
			Tj = 160°C				2.5*[10]	mA
		SYSVCC and VCC SYSVCC=VCC=5.5V DPS	Tj = 25°C			82*[8]	142*[9]	µA
			Tj = 160°C				2.5*[10]	mA
	I_{VDD_DS}	ISOVDD DPS	Tj = 25°C			3.7	8.1	mA
			Tj = 160°C				240	mA
Cyclic RUN mode current[*7]	I_{VCC_CR}[*11*13]	SYSVCC and VCC[*12] SYSVCC=VCC=5.5V eVR	Tj = 25°C	10 MHz		13.5	25.4	mA
			Tj = 160°C	10 MHz			270	mA
		SYSVCC and VCC[*12] SYSVCC=VCC=3.6V eVR	Tj = 25°C	10 MHz		13.5	25.4	mA
			Tj = 160°C	10 MHz			270	mA
		SYSVCC and VCC SYSVCC=VCC=5.5V DPS	Tj = 25°C	10 MHz		1.9	2.3	mA
			Tj = 160°C	10 MHz			5.8	mA
		SYSVCC and VCC[*12] SYSVCC=VCC=5.5V eVR	Tj = 25°C	100 MHz		36	43	mA
			Tj = 160°C	100 MHz			297	mA
		SYSVCC and VCC[*12] SYSVCC=VCC=3.6V eVR	Tj = 25°C	100 MHz		36	43	mA
			Tj = 160°C	100 MHz			297	mA
		SYSVCC and VCC SYSVCC=VCC=5.5V DPS	Tj = 25°C	100 MHz		2.4	3.4	mA
			Tj = 160°C	100 MHz			6.6	mA
	I_{VDD_CR}	ISOVDD DPS	Tj = 25°C	10 MHz		6.1	12.7	mA
			Tj = 160°C	10 MHz			244	mA
			Tj = 25°C	100 MHz		27	32	mA
			Tj = 160°C	100 MHz			269	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- EnVCC = AnVREFH = 5.0 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of I/O buffer.
Note 3. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.
Note 4. This value shows the case that power supply for ISOVDD is stopped at outside.
Note 5. Only LS IntOSC is operated.
Note 6. Only LS IntOSC is operated. Size of Retention RAM is 16KB.
Note 7. Only LS IntOSC, HS IntOSC and CPU(PE0) are operated.
Note 8. It will increase 6 µA if size of Retention RAM is 32KB.
Note 9. It will increase 6 µA if size of Retention RAM is 32KB.
Note 10. It will increase 0.1 mA if size of Retention RAM is 32KB.
Note 11. Power supply mode of AWOVDC is Low Power Mode (AWOPSM.AWOPSM = 1).
Note 12. Skip Field BIST2 (BSEQ2CTL.HWBISTEXE = 0).
Note 13. This value is the sum of the SYSVCC current and the VCC current.

Table 3.31 Current consumption for RH850/U2C2[*2]

Item	Symbol	Power supply		CPU frequency	MIN.	TYP.[*1]	MAX.	Unit
RUN mode current	I_{VCC_R}[*13]	SYSVCC and VCC[*3] SYSVCC=VCC=5.5V		320 MHz		201	379	mA
				240 MHz		171	331	mA
				160 MHz		159	317	mA
			BIST			201	346	
STOP mode current[*5]	I_{VCC_S}[*13]	SYSVCC and VCC SYSVCC=VCC=5.5V	Tj = 25°C			17	24	mA
			Tj = 160°C				173	mA
DeepSTOP mode current[*4, *6]	I_{VCC_DS}[*11*13]	SYSVCC and VCC SYSVCC=VCC=5.5V	Tj = 25°C			82[*8]	142[*9]	µA
			Tj = 160°C				2.1[*10]	mA
Cyclic RUN mode current[*7]	I_{VCC_CR}[*11*13]	SYSVCC and VCC[*12] SYSVCC=VCC=5.5V	Tj = 25°C	10 MHz		12	21.5	mA
			Tj = 160°C	10 MHz			140	mA
		SYSVCC and VCC[*12] SYSVCC=VCC=5.5V	Tj = 25°C	100 MHz		31	38	mA
			Tj = 160°C	100 MHz			163	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
- Tj = 25°C
- EnVCC = AnVREFH = 5.0 V
- ISOVDD = 1.09 V

Note 2. The above value does not include the current of I/O buffer.

Note 3. Additional current (max.60 mA for Code Flash per unit, max.35 mA for Data Flash per unit) will be applied when data writing/erasing to Code or Data Flash is processing.

Note 4. This value shows the case that power supply for ISOVDD is stopped at outside.

Note 5. Only LS IntOSC is operated.

Note 6. Only LS IntOSC is operated. Size of Retention RAM is 16KB.

Note 7. Only LS IntOSC, HS IntOSC and CPU(PE0) are operated.

Note 8. It will increase 6 µA if size of Retention RAM is 32KB.

Note 9. It will increase 6 µA if size of Retention RAM is 32KB.

Note 10. It will increase 0.1 mA if size of Retention RAM is 32KB.

Note 11. Power supply mode of AWOVDC is Low Power Mode (AWOPSM.AWOPSM = 1).

Note 12. Skip Field BIST2 (BSEQ2CTL.HWBISTEXE = 0).

Note 13. This value is the sum of the SYSVCC current and the VCC current.

3.2.12.3 Power Supply Currents for specific features

See **Section 3.2.1, Operational Condition**

Table 3.32 Current consumption for RH850/U2C8

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Gigabit Ethernet	I_{GBETH}	Current of GETH0BVCC, GETH0PVCC				95	mA
ADCJ1	$I_{ADC1REF}$	Current of A1VREFH 4ch T&H function is used				8.6	mA
ADCJ2	$I_{ADC2REF}$	Current of A2VREFH				3.6	mA
ADCJA	$I_{ADCAREF}$	Current of AAVREFH 4ch T&H function is used				7.9	mA

Table 3.33 Current consumption for RH850/U2C4

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
ADCJ1	$I_{ADC1REF}$	Current of A1VREFH 4ch T&H function is used				8.6	mA
ADCJA	$I_{ADCAREF}$	Current of AAVREFH 4ch T&H function is used				7.9	mA

Table 3.34 Current consumption for RH850/U2C2

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
ADCJ1	$I_{ADC1REF}$	Current of A1VREFH 4ch T&H function is used				8.6	mA
ADCJA	$I_{ADCAREF}$	Current of AAVREFH 4ch T&H function is used				7.9	mA

3.2.13 Voltage Detector (POC) Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.35 Voltage Detector (POC) Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage (SYSVCC)	V_{POC}		2.75		3.0	V
Response time	t_{DPOC1}	Rise			1.2	ms
	t_{DPOC2}	Fall			10	µs
SYSVCC minimum pulse width	t_{WPOC}		0.2			ms
SYSVCC voltage ramp	t_{SYSVS}		0.002		550	ms/V

Note 1. POC monitors SYSVCC supply voltage.

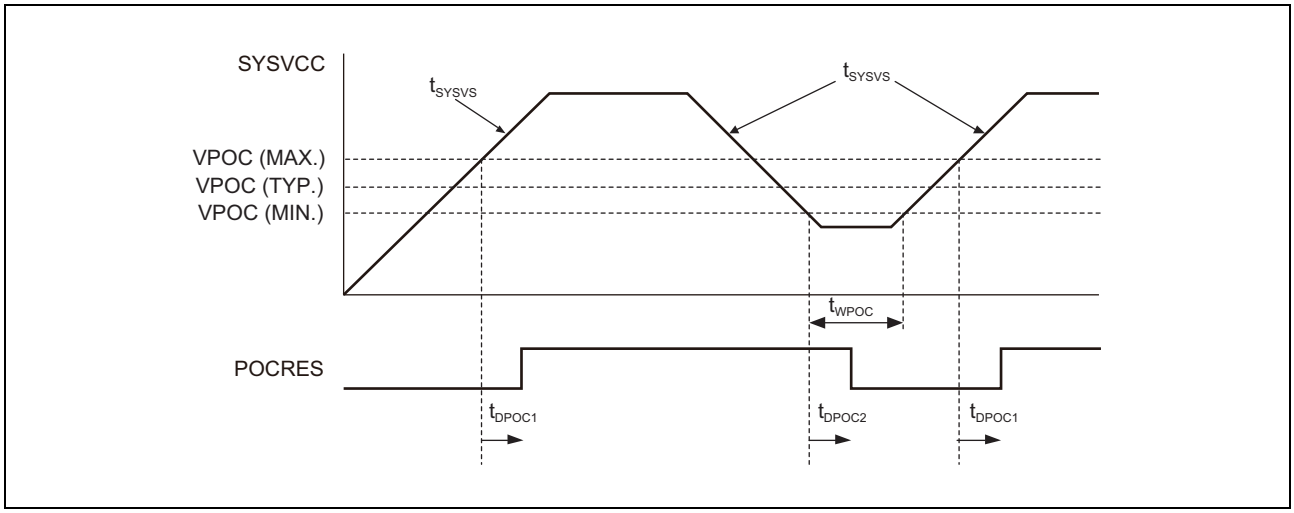


Figure 3.10 POC Characteristics

3.2.14 VMON Characteristics

Conditions:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.

Table 3.36 VMON Characteristics*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VDD primary high detection level	V_{VDDMAH}	AWOVDD	1.155	1.17	1.205	V
	V_{VDDMIH}	ISOVDD	1.155	1.17	1.205	V
VDD primary low detection level	V_{VDDMAL}	AWOVDD	0.975	1.01	1.025	V
	V_{VDDMIL}	ISOVDD Enable assist by Delay Monitor (DMON)	0.985	1.01	1.025	V
VCC primary high detection level	V_{VCCMH}		5.5	5.64	5.8	V
VCC primary low detection level	V_{VCCML}		2.8	2.9	3	V
E0VCC primary high detection level	V_{EVCCMH}		5.5	5.64	5.8	V
E0VCC primary low detection level	V_{EVCCML}		2.8	2.9	3	V
$\overline{\text{VMONOUT}}$ delay time	t_{DVMON}				10+Filter time*1	µs
VMON minimum pulse width	t_{WVMON}		0.2			ms
Voltage ramp	t_{VS}		0.002		550	ms/V

Note 1. See the RH850/U2C Group User's Manual: Hardware Section 11.3.6, Registers for details specification of filter time.

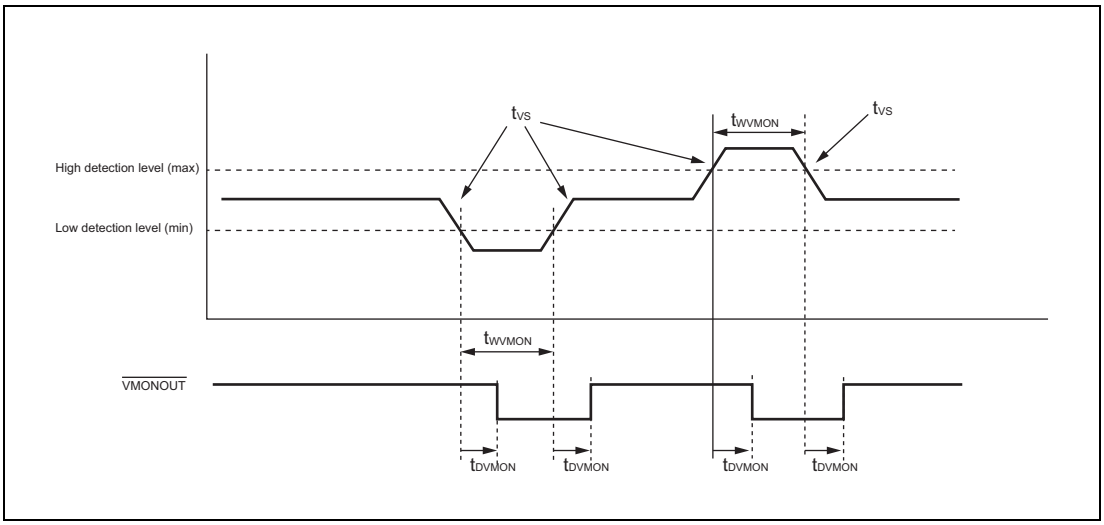


Figure 3.11 VMON Characteristics

3.3 AC Characteristics

3.3.1 AC Characteristic Measurement Condition

3.3.1.1 General Conditions

Below conditions are valid for all subsequent timing specifications if not noted otherwise:

- See **Section 3.2.1.1, Supply Voltage Characteristics**.
  V_{SYSVCC}, V_{VCC}, V_{EnVCC}: MIN. 3.0V
- Drive strength = 3
- CL = 30 pF
- All bits of PINVn/JPINV0 are set as 0.
- All bits of PODCn/JPODC0 are set as 0 except for specification on RI3C timing.

NOTE

Even though AC characteristics correspond to the nominal frequency, a main oscillator tolerance of up to 1000 ppm is considered with regard to timing characteristics for communication modules.

The AC characteristics are specified on the assumption that each pin is used at the same EnVCC voltage.

3.3.1.2 Input Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

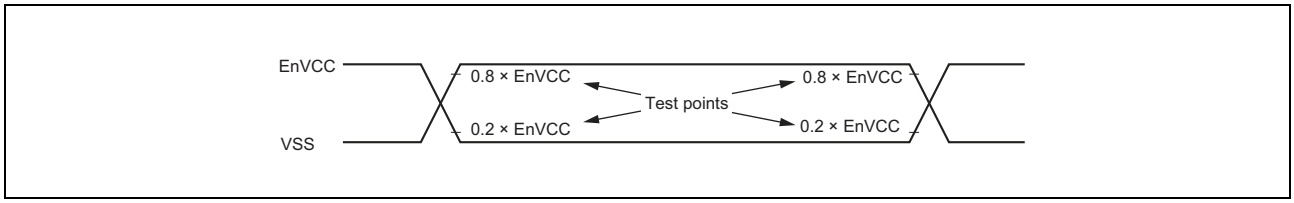


Figure 3.12 AC Input Measurement Points

3.3.1.3 Output Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:

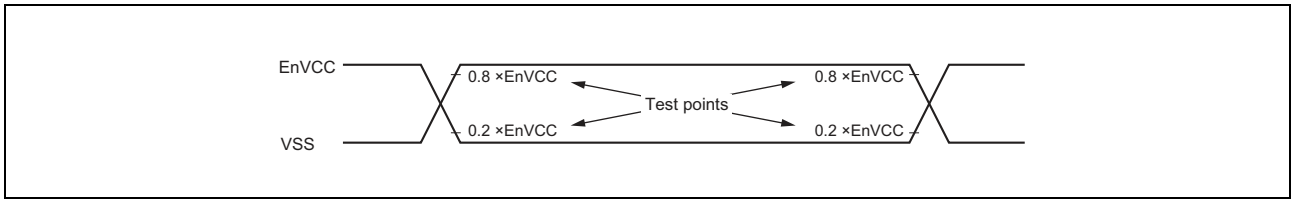


Figure 3.13 AC Output Measurement Points

3.3.1.4 Load conditions

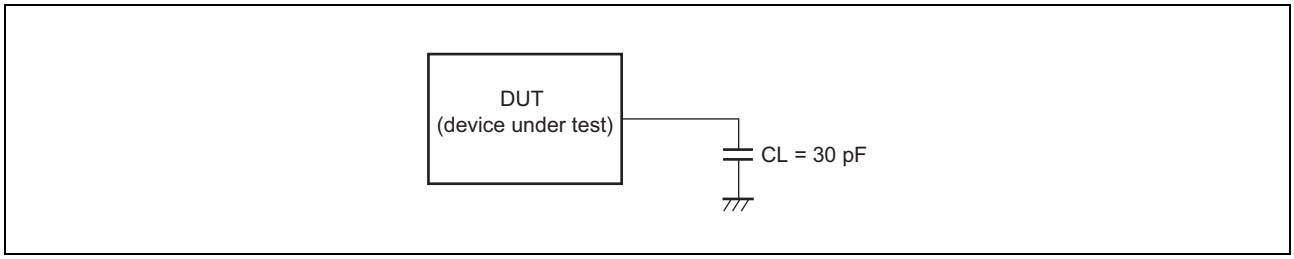


Figure 3.14 AC Load Conditions

3.3.2 Power On/Off Timing

Conditions:

• See **Section 3.3.1, AC Characteristic Measurement Condition**.

3.3.2.1 Power On/Off Timing for external supply [For U2C4/U2C8/U2C8-EVA Only]

Table 3.37 Power On/Off Timing for external power supply

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reset hold time at power-on	t_{RESH1}	Power-up*1	0.2			ms
Power hold time at reset assertion*5	t_{PWH}	Power-down*2 (ETND1 (SGMII) used)	64			µs
		Power-down*2 (ETND1 (SGMII) not used)	10.5			µs
Operation mode low level hold time at power-on	t_{MDL1}		0.1			ms
Operating mode setup time at power-on	t_{MDS1}		0.1			ms
Operating mode setup time at reset assert	t_{MDS2}		1			ms
Operating mode hold time at reset negate	t_{MDH1}		1			ms
Operating mode hold time at power-off	t_{MDH2}		0			µs
Delay time at power-on-1	t_{PDLY1}	Time since SYSVCC/VCC were power-up	0			ms
Delay time at power-on-2	t_{PDLY2}	Time since supply except VDD were power-up	0			ms
Delay time at power-on-3	t_{PDLY3}	Time since SYSVCC/VCC were power-up			10	ms
PWRCTL (Dedicated terminal) negate time	t_{PWRCTL}	Time since POC released			90	µs
VDD power up time	t_{VDD}	Time since PWRCTL were negated	0			ms
POC release delay time	t_{POC}	Time since SYSVCC/VCC were power-up			1.5	ms
Delay time at power-off	t_{PDLY4}	Time since SYSVCC/VCC were power-off	0		25	ms
$\overline{\text{TRST}}$ setup time at reset*2	t_{TRMDS}		2			µs
$\overline{\text{TRST}}$ hold time at reset negate*4	t_{TRMDH}		30			ms
$\overline{\text{TRST}}$ hold time at power-on	t_{TRSTH1}		0.19			ms
$\overline{\text{TRST}}$ low level hold time at reset negate	t_{TRMDL}		30			ms
Oscillator stabilization time	t_{OSC}				6.1	ms
PLL lock in time	t_{PLLL}	*3			1	ms

Note 1. t_{RESH1} is the reset time required for the supply of internal clock signals to become stable after all power supplies are turned on.

Note 2. t_{PWH} is the time from assertion of the reset signal until any of the power voltages have dropped below the lower-limit voltages.

Note 3. t_{PLLL} is the time required for PLL to lock in after MOSC oscillation has become stable.

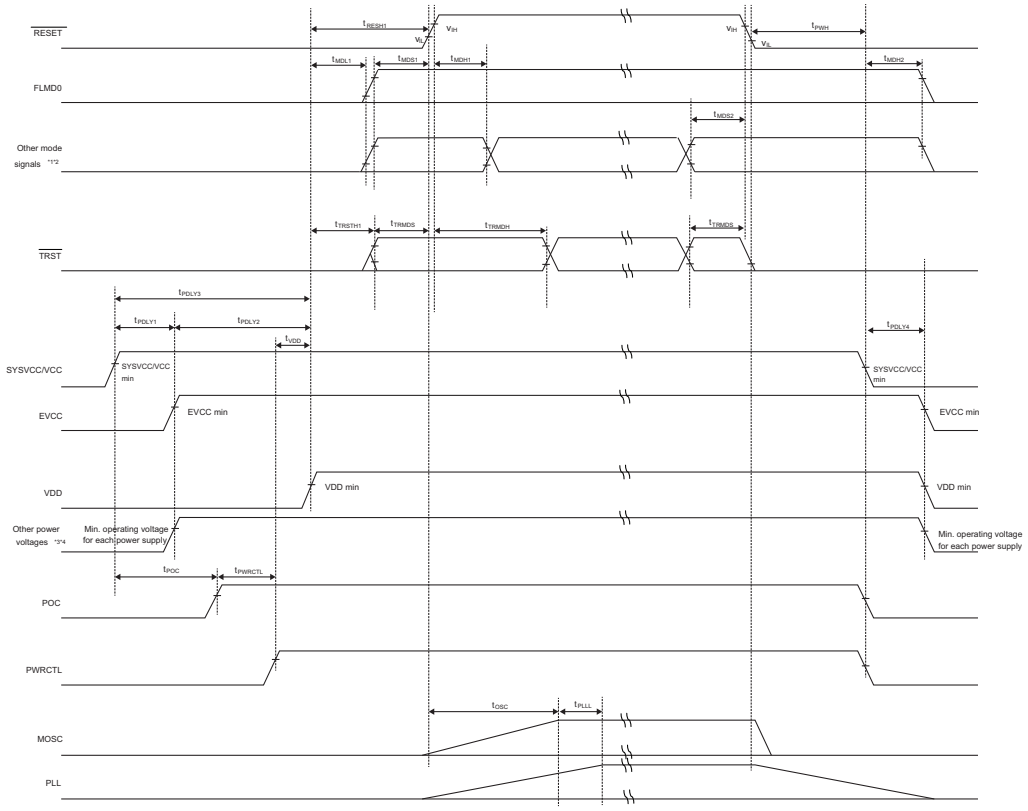
Note 4. Access by the Nexus, LPD and BSCAN during t_{TRMDH} duration is prohibited (both of High and low condition of $\overline{\text{TRST}}$).

Note 5. The device can withstand up to 1000 uncontrolled power down cycles without impact on lifetime. Uncontrolled means not according to power down timing requirements.

CAUTION

- **The states of I/O pins are not reset during the noise cancellation interval of the reset signal following its assertion while power is being turned off. During that**

time, do not allow any input of mid-range potential to the pin or contention of output data.



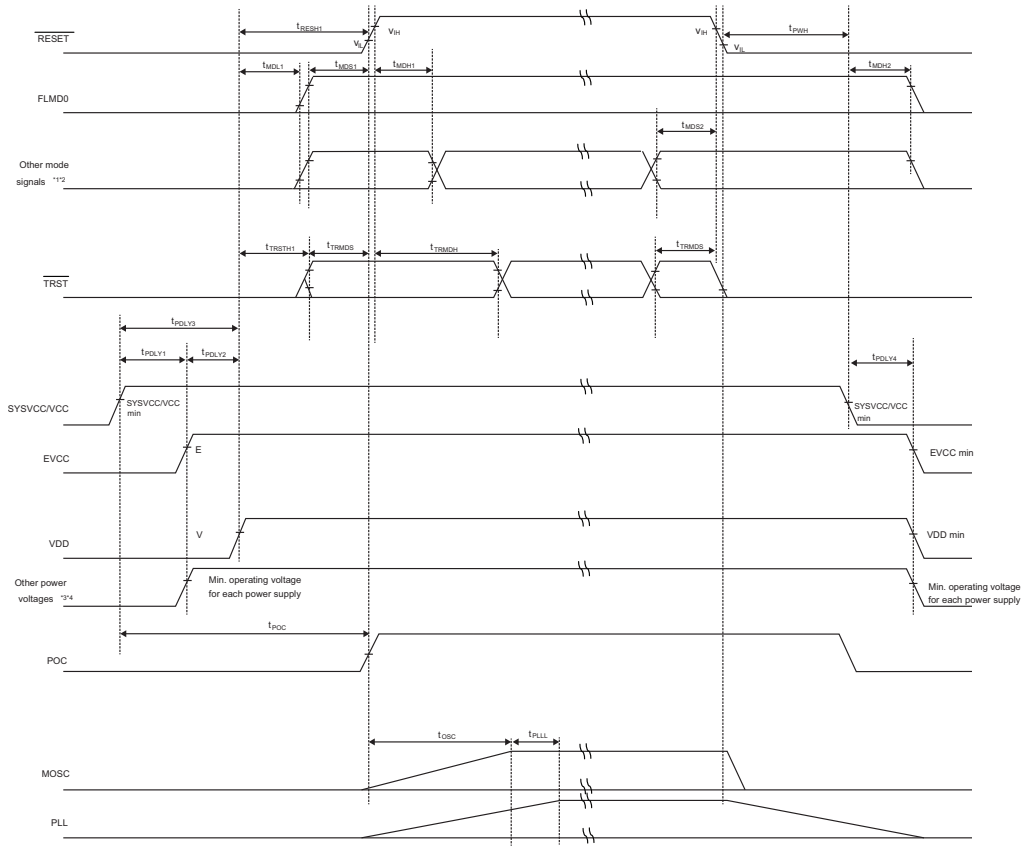
Note 1. FLMD1

Note 2. Should keep as same as mode pins level when $\overline{\text{RESET}}$ are negated and asserted, in order not to change operation mode at $\overline{\text{RESET}}$ assert.

Note 3. EMUVCC, EMUVDD are not included in the other power voltages

Note 4. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1kΩ or more pull-down resistance

Figure 3.15 Power On/Off Timings for external supply with PWRCTL (Dedicated terminal)



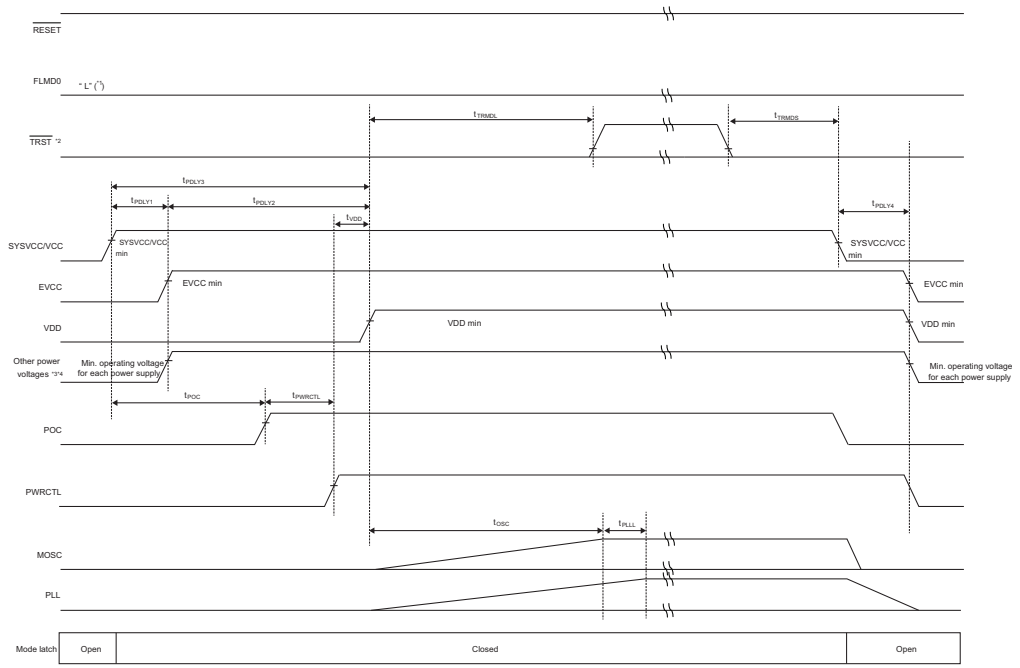
Note 1. FLMD1

Note 2. Should keep as same as mode pins level when $\overline{\text{RESET}}$ are negated and asserted, in order not to change operation mode at $\overline{\text{RESET}}$ assert.

Note 3. EMUVCC, EMUVDD are not included in the other power voltages

Note 4. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1kΩ or more pull-down resistance

Figure 3.16 Power On/Off Timings for external supply without PWRCTL



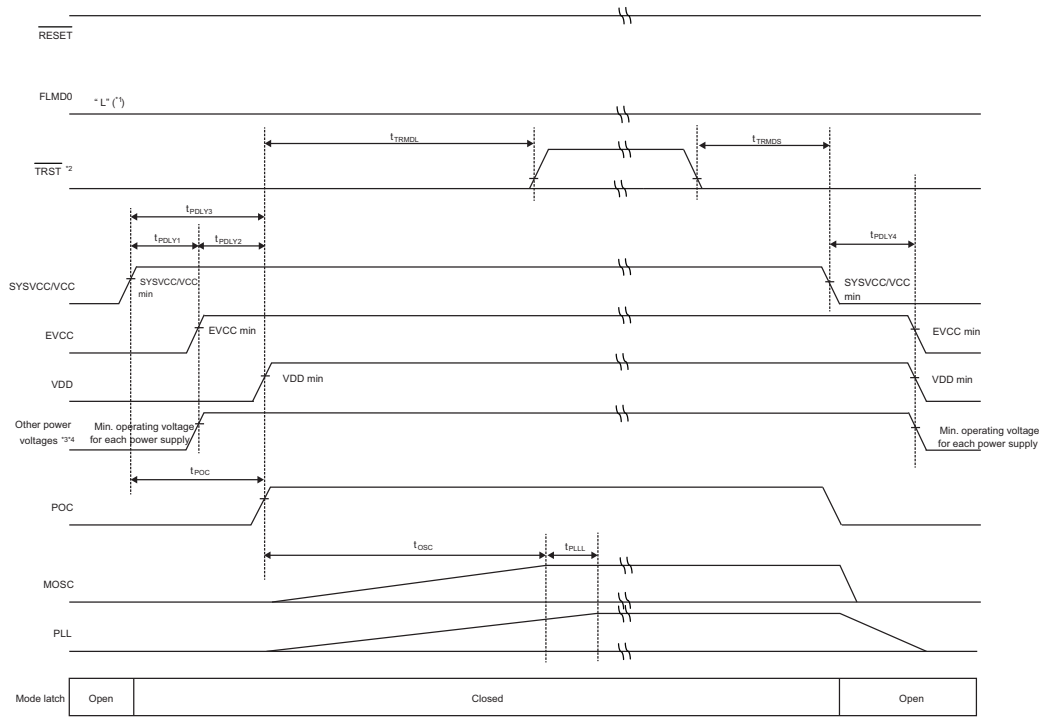
Note 1. FLMD0 should be fixed to L in case of external reset pull-up.

Note 2. $\overline{\text{TRST}}$ should be fixed to L at mode entry in case of external reset pull-up, then CPU will autonomously run.

Note 3. EMUVCC, EMUVDD are not included in the other power voltages

Note 4. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1kΩ or more pull-down resistance

Figure 3.17 Power On/Off Timings for external supply with PWRCTL(Dedicated terminal) and with reset pull-up



Note 1. FLMD0 should be fixed to L in case of external reset pull-up.

Note 2. $\overline{\text{TRST}}$ should be fixed to L at mode entry in case of external reset pull-up, then CPU will autonomously run.

Note 3. EMUVCC, EMUVDD are not included in the other power voltages

Note 4. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1kΩ or more pull-down resistance

Figure 3.18 Power On/Off Timings for external supply without PWRCTL and with reset pull-up

3.3.2.2 Power On/Off Timing for internal power supply [For U2C2/U2C4 Only]

Table 3.38 Power On/Off Timing for internal power supply

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reset hold time at power-on	t_{RESH1}	Power-up*1	0.2			ms
Power hold time at reset assertion	t_{PWH}	Power-down*2	2			µs
Operation mode low level hold time at power-on	t_{MDL1}		0.1			ms
Operating mode setup time at power-on	t_{MDS1}		0.1			ms
Operating mode setup time at reset assert	t_{MDS2}		1			ms
Operating mode hold time at reset negate	t_{MDH1}		1			ms
Operating mode hold time at power-off	t_{MDH2}		0			µs
Delay time at power-on-1	t_{PDLY1}	Time since SYSVCC/VCC were power-up	0			ms
Delay time at power-on-3	t_{PDLY3}	Time since SYSVCC/VCC were power-up			10	ms
Delay time at power-on-3 for terminal reset pull up case	t_{PDLY3P}	Time since SYSVCC/VCC were power-up			0.51	ms
VDD power up time	t_{VDD2}	Time since POC released			1.1	ms
POC release delay time	t_{POC}	Time since SYSVCC/VCC were power-up			1.5	ms
Delay time at power-off	t_{PDLY4}	Time since SYSVCC/VCC were power-off	0		25	ms
$\overline{TRST}$ setup time at reset	t_{TRMDS}		2			µs
$\overline{TRST}$ hold time at reset negate*4	t_{TRMDH}		30			ms
$\overline{TRST}$ hold time at power-on	t_{TRSTH1}		0.19			ms
$\overline{TRST}$ low level hold time at reset negate*2	t_{TRMDL}		30			ms
Oscillator stabilization time	t_{OSC}				6.1	ms
PLL lock in time	t_{PLLL}	*3			1	ms

Note 1. t_{RESH1} is the reset time required for the supply of internal clock signals to become stable after all power supplies are turned on.

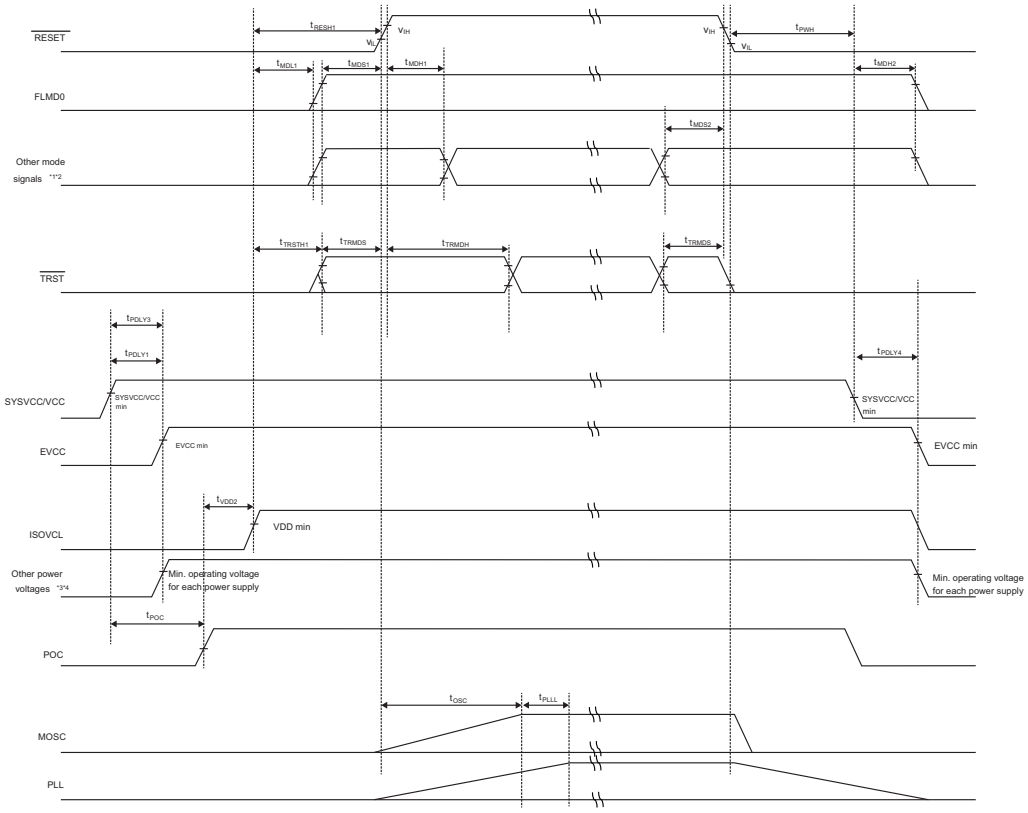
Note 2. t_{PWH} is the time from assertion of the reset signal until any of the power voltages have dropped below the lower-limit voltages.

Note 3. t_{PLLL} is the time required for PLL to lock in after MOSC oscillation has become stable.

Note 4. Access by the Nexus, LPD and BSCAN during t_{TRMDH} duration is prohibited (both of High and low condition of $\overline{TRST}$).

CAUTION

- **The states of I/O pins are not reset during the noise cancellation interval of the reset signal following its assertion while power is being turned off. During that time, do not allow any input of mid-range potential to the pin or contention of output data.**



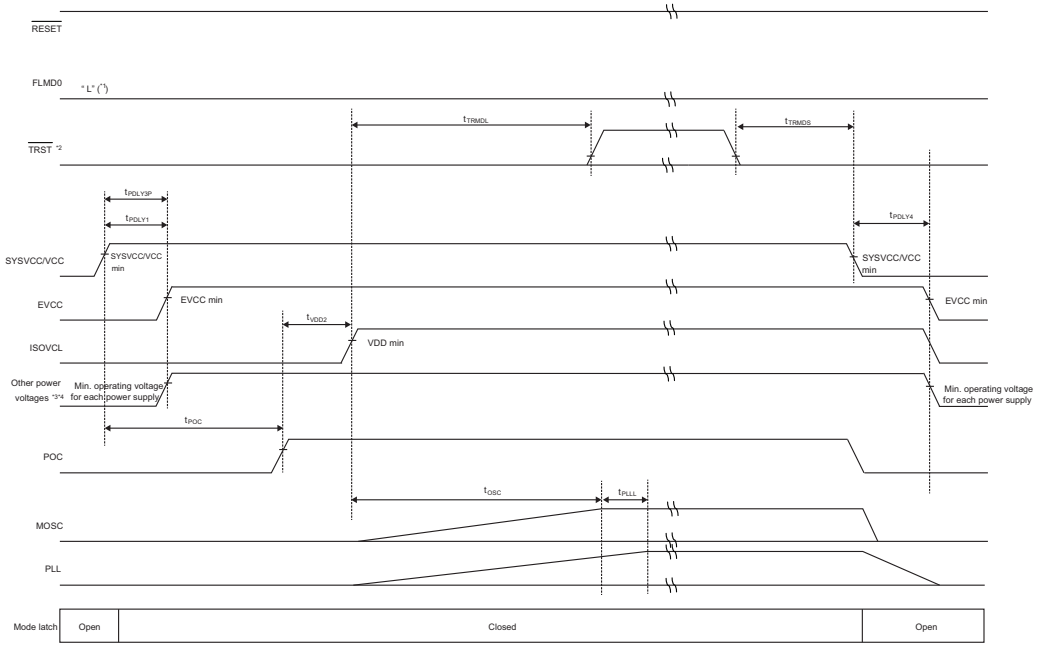
Note 1. FLMD1

Note 2. Should keep as same as mode pins level when $\overline{\text{RESET}}$ are negated and asserted, in order not to change operation mode at $\overline{\text{RESET}}$ assert.

Note 3. EMUVCC, EMUVDD are not included in the other power voltages

Note 4. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1kΩ or more pull-down resistance

Figure 3.19 Power On/Off Timings for internal power supply without PWRCTL



Note 1. FLMD0 should be fixed to L in case of external reset pull-up.

Note 2. $\overline{\text{TRST}}$ should be fixed to L at mode entry in case of external reset pull-up, then CPU will autonomously run.

Note 3. EMUVCC, EMUVDD are not included in the other power voltages

Note 4. In case SGMII is not used, GETH0BVCC power supply pin allowed to be connect VSS with 1kΩ or more pull-down resistance

Figure 3.20 Power On/Off Timings for internal power supply without PWRCTL and with reset pull-up

Power On/Off Timings for internal power supply with PWRCTL is under confirming.

It is not considered in U2C8 development and will be considered in U2C4 development.

3.3.3 CPU Reset Release Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**

Table 3.39 In Case the $\overline{\text{RESET}}$ Pin is Not Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SYSVCC ↑ to CPU reset release*1	t_{DPCRR}				3.94*2 + 0.58*3 + t_{BIST}*3	ms

Note 1. This is reference value.

Note 2. Add (t_{PDLY3} - 2.6 ms) if t_{PDLY3} is longer than 2.6 ms. The value includes the RAM initialization time. See the RH850/U2C Group User's Manual: Hardware Section 9.5.6, RAM Initialization.

Note 3. In case FBIST0 is not skipped.
t_{BIST} means BIST run time. Refer to Table 45.528, BIST scenario selection at the next System Reset 2 on the RH850/U2C Group User's Manual: Hardware Section 45.6.2.27, BSEQ0SEL — BIST Scenario Select Register for details. Note that the given BIST run time is the typical value and the tolerance of the corresponding clock needs to be taken into account for the maximum value.

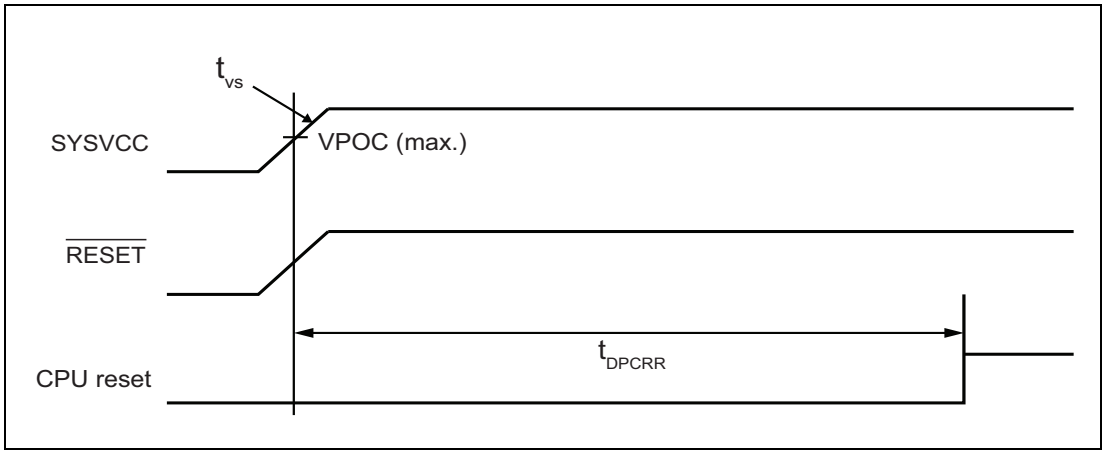


Figure 3.21 CPU Reset Release Timing (In Case the $\overline{\text{RESET}}$ Pin is Not Used)

Table 3.40 In Case the $\overline{\text{RESET}}$ Pin is Used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				1.14*2 + 0.58*3 + t_{BIST}*3	ms

Note 1. This is reference value.

Note 2. In case the time (t_{DRSL}) until releasing the RESET pin is longer than 2.8 ms. If t_{DRSL} is shorter than 2.8 ms, add (2.8 ms - t_{DRSL}). The value includes the RAM initialization time. See the RH850/U2C Group User's Manual: Hardware Section 9.5.6, RAM Initialization.

Note 3. In case FBIST0 is not skipped.
t_{BIST} means BIST run time. Refer to Table 45.528, BIST scenario selection at the next System Reset 2 on the RH850/U2C Group User's Manual: Hardware Section 45.6.2.27, BSEQ0SEL — BIST Scenario Select Register for details. Note that the given BIST run time is the typical value and the tolerance of the corresponding clock needs to be taken into account for the maximum value.

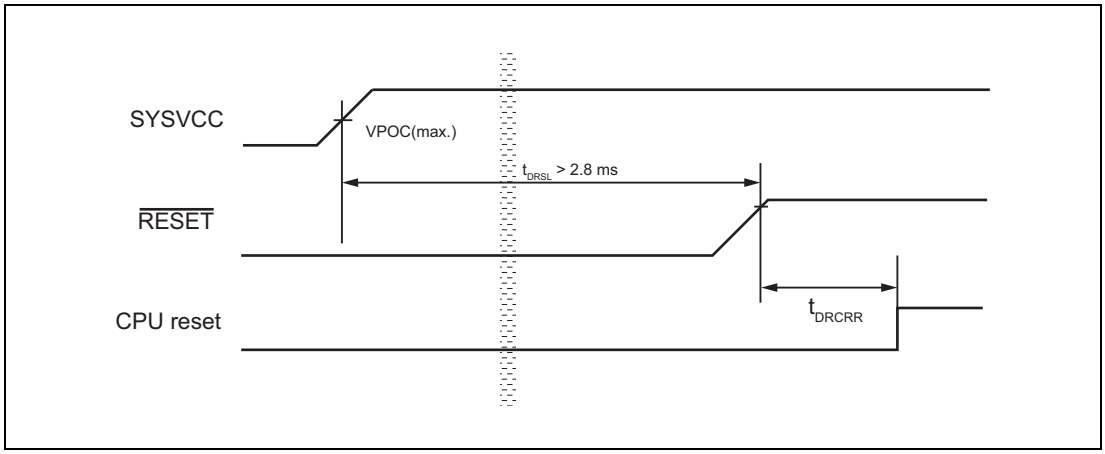


Figure 3.22 CPU Reset Release Timing (In Case the $\overline{\text{RESET}}$ Pin is Used)

3.3.4 Standby Transition/Return Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**

Table 3.41 DeepSTOP Transition/Return Timing In case of VDD External Supply

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Wake-up trigger to PWRCTL delay time	$t_{DPWRCTL}$				100	µs
VDD hold time	t_{HDD}		0			µs
VDD power-on start time	t_{PDD}		0			µs

3.3.5 Clock Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.42 Clock Output Timing*1*2

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock output period time	t_{CLKOUT}		41.6			ns
Clock output high level width	t_{WCOH}	*3	t_{CLKOUT} / 2 – 10			ns
		*4	t_{CLKOUT} × ((N-1) / 2) + t_{CLKOUT} × 0.3 – 10			ns
Clock output low level width	t_{WCOL}	*3	t_{CLKOUT} / 2 – 10			ns
		*4	t_{CLKOUT} × ((N-1) / 2) + t_{CLKOUT} × 0.3 – 10			ns

Note 1. There is a function to output the internal clock via EXTCLKnO pin.

Note 2. For base clock, refer to related the RH850/U2C Group User's Manual: Hardware Section 13, Clock Controller.

Note 3. Source Clock Setting = CLK_MOSC (24MHz, 20MHz), CLK_HSIOSC / 20, CLK_HSB, CLKC_HSB or N (Clock Divider) is even (N = 2, 4, 6,…) case.

Note 4. Source Clock Setting = CLK_MOSC (16MHz, 8MHz), CLK_LSIOSC, CLK_SOSC and N (Clock Divider) is odd (N = 1, 3, 5,…) case.

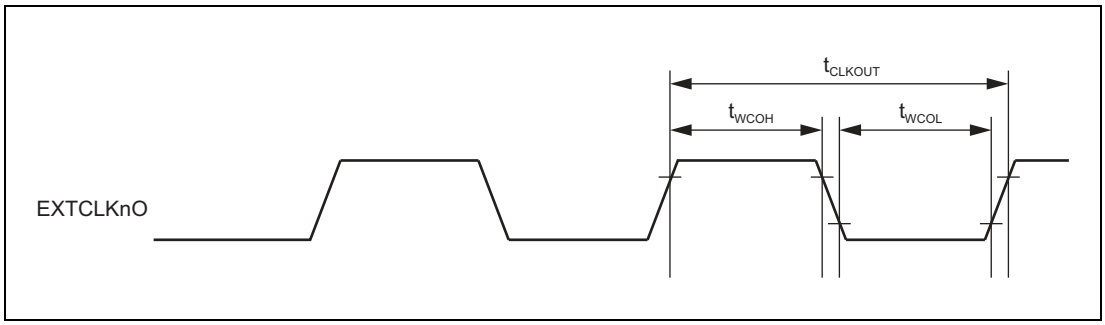


Figure 3.23 Clock Output Timing

3.3.6 Output Slew Rate

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.43 Output Slew Rate

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output rise and fall time	t_{KRP11} / t_{KFP11}	Drive strength = 1 20% to 80%	CL = 100 pF			6.7	ns
	t_{KRP12} / t_{KFP12}	Drive strength = 2 20% to 80%	CL = 30 pF			4.0	ns
			CL = 50 pF			6.7	ns
			CL = 100 pF			13.4	ns
	t_{KRP13} / t_{KFP13}	Drive strength = 3 20% to 80%	CL = 30 pF			6.7	ns
			CL = 50 pF			11.1	ns
			CL = 100 pF			21.0	ns
	t_{KRP14} / t_{KFP14}	Drive strength = 4 20% to 80%	CL = 30 pF			13.5	ns
			CL = 50 pF			22.5	ns
			CL = 100 pF			45.0	ns
	t_{KRP15} / t_{KFP15}	Drive strength = 5 20% to 80%	CL = 30 pF			27.0	ns
			CL = 50 pF			45.0	ns
			CL = 100 pF			90.0	ns

3.3.7 Control Signal Timing

3.3.7.1 $\overline{\text{RESET}}$ Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.44 $\overline{\text{RESET}}$ Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}*1		2000			µs
$\overline{\text{RESET}}$ pulse rejection width*2	t_{WRRJ}		200		1200	ns

Note 1. t_{WRSL} is the minimum required time to complete the external reset state generated by an external reset signal. When an external reset signal is input that is shorter than this time, the external reset state will continue even after the external reset signal release. This microcontroller is completely reset after completion of the external and internal reset state. An external reset request is accepted with an external reset signal input width of more than the maximum time of t_{WRRJ}. When the external reset signal pulse width is less than the minimum value of the reset pulse rejection width, the reset request is not accepted. When the external reset signal is input during DeepSTOP mode, the external reset state will continue during the wait time set by PWRGD_CNT even when the external reset signal is released.

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

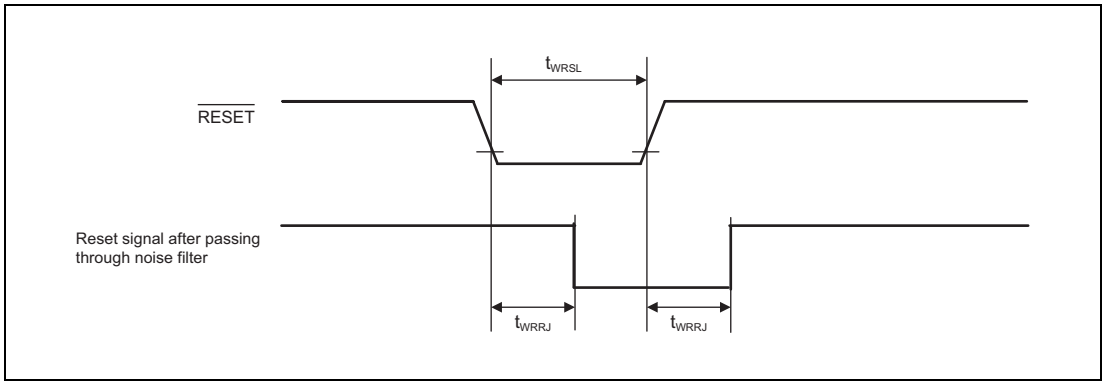


Figure 3.24 $\overline{\text{RESET}}$ Timing

3.3.7.2 Interrupt, Wake-up and Error Input Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.45 Interrupt Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	*3	600			ns
		*4	150			µs
NMI input low level width	t_{WNIL}	*3	600			ns
		*4	150			µs
NMI pulse rejection width*2	t_{WNIRJ}		100		600	ns
IRQn input high level width	t_{WITH}	*3	600			ns
		*4	150			µs
IRQn input low level width	t_{WITL}	*3	600			ns
		*4	150			µs
INTPn pulse rejection width*2	t_{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t_{WRLINH}		S × 1/fs*1			ns
RLIN3nRX wake-up input low level width	t_{WRLINL}		S × 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	$t_{WRLINRJ}$		(S – 1) × 1/fs*1		S × 1/fs*1	ns
CANnRX wake-up input high level width	t_{WCANH}		S × 1/fs*1			ns
CANnRX wake-up input low level width	t_{WCANL}		S × 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t_{WCANRJ}		(S – 1) × 1/fs*1		S × 1/fs*1	ns
FLXnRXDA wake-up input high level width	t_{WFLXH}		S × 1/fs*1			ns
FLXnRXDA wake-up input low level width	t_{WFLXL}		S × 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t_{WFLXRJ}		(S – 1) × 1/fs*1		S × 1/fs*1	ns
$\overline{\text{ERRORINn}}$ wake-up input high level width	t_{WERRH}		S × 1/fs*1			ns
$\overline{\text{ERRORINn}}$ wake-up input low level width	t_{WERRL}		S × 1/fs*1			ns
$\overline{\text{ERRORINn}}$ wake-up pulse rejection width*2	t_{WERRRJ}		(S – 1) × 1/fs*1		S × 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOSC/20)

Note 4. Level Detection (CLKA_LPS is operated by CLK_LSIOSC)

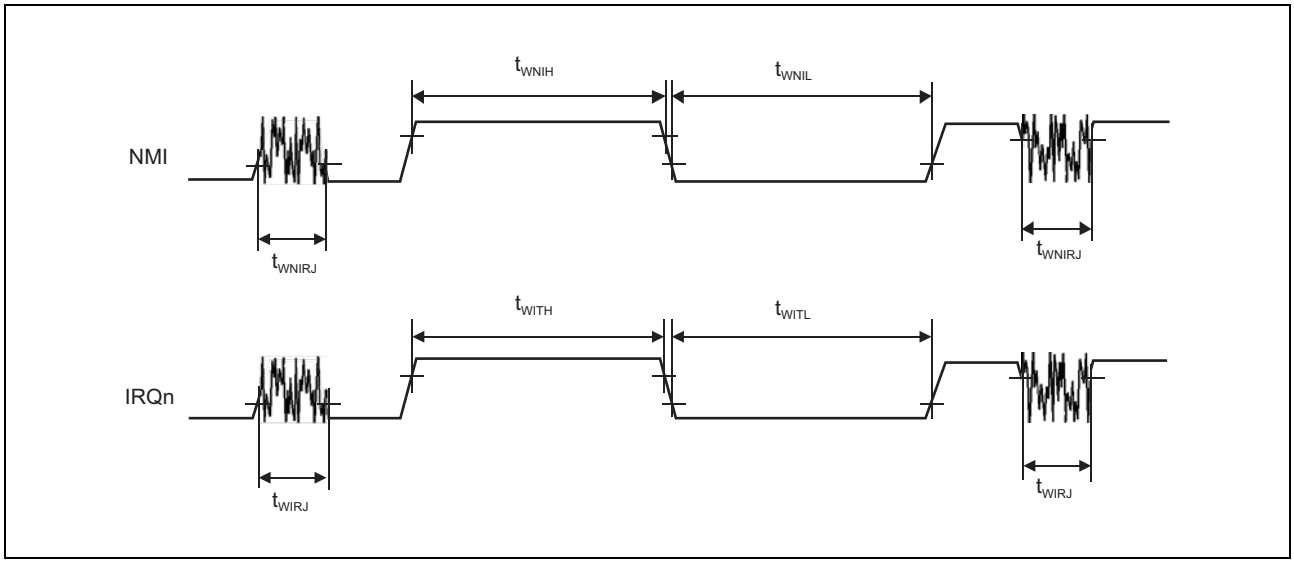


Figure 3.25 Interrupt, wake-up and error input timing

3.3.7.3 Mode Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.46 Mode Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0, FLMD1 input high level width	t_{WMDH}		600			ns
FLMD0, FLMD1 input low level width	t_{WMDL}		600			ns
FLMD0, FLMD1 pulse rejection width*1	t_{WMDRJ}		100		600	ns

Note 1. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

NOTE

Switching of FLMD0 after rising edge of $\overline{\text{RESET}}$ is prohibited except for serial programming mode.

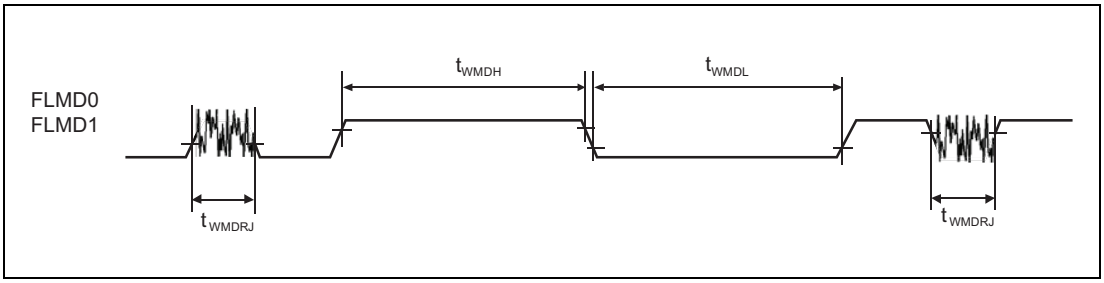


Figure 3.26 Mode Timing

3.3.7.4 ADTRG Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.47 ADCKnTRGm Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCKnTRGm input high level width	t_{WADH}		S × 1/fs*1			ns
ADCKnTRGm input low level width	t_{WADL}		S × 1/fs*1			ns
ADCKnTRGm pulse rejection width*2	t_{WADRJ}		(S – 1) × 1/fs*1		S × 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB, CLKA_ADC
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

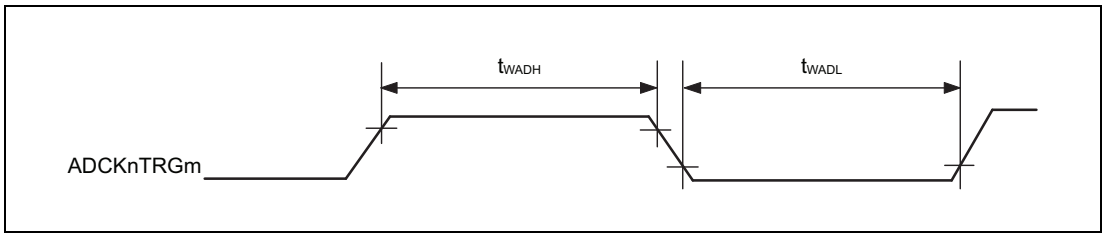


Figure 3.27 ADCKnTRGm Timing

3.3.7.5 Communication Signal Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.48 Control Signal

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	$t_{WSENTIH}$	Analog filter	600			ns
		Digital filter	S × 1/fs*1			ns
SENTnRX input low level width	$t_{WSENTIL}$	Analog filter	600			ns
		Digital filter	S × 1/fs*1			ns
SENTnRX pulse rejection width*2	$t_{WSENTIRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) × 1/fs*1		S × 1/fs*1	ns
PSI5nRX input high level width	$t_{WPSI5IH}$	Analog filter	600			ns
		Digital filter	S × 1/fs*1			ns
PSI5nRX input low level width	$t_{WPSI5IL}$	Analog filter	600			ns
		Digital filter	S × 1/fs*1			ns
PSI5nRX pulse rejection width*2	$t_{WPSI5IRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) × 1/fs*1		S × 1/fs*1	ns
SSIFn related terminals input high level width*3			S × 1/fs*1			ns
SSIFn related terminals input low level width*3			S × 1/fs*1			ns
SSIFn related terminals pulse rejection width*2*3			(S – 1) × 1/fs*1		S × 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKC_HSB (for SENTnRX and PSI5nRX)
frequency of CLK_LSB (for RHSBnEMRG)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. The following shows the SSIF related terminals.
SSIFnSCK, SSIFnWS, SSIFnRXD, SSIFACK

3.3.8 Low Power Sampler (DPIN input) Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4 (SELDP2-0)

Table 3.49 Low Power Sampler Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time	t_{DSDDI}				150	ns

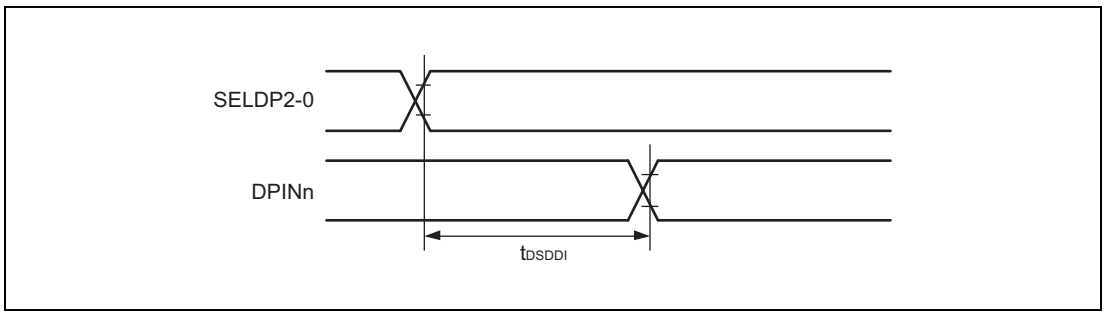


Figure 3.28 Low Power Sampler Timing

3.3.9 SFMA Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.50 SFMA Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SFMA0CLK clock cycle	$t_{SFMAcyc}$		25			ns
SFMA0CLK high pulse width	t_{SFMAWH}		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
SFMA0CLK low pulse width	t_{SFMAWL}		0.4 × $t_{SFMA0cyc}$		0.6 × $t_{SFMA0cyc}$	ns
Data input setup time	$t_{SFMADIS}$		9.0			ns
Data input hold time	$t_{SFMADIH}$		0.0			ns
SFMA0SSL setup time	t_{SFMASS}		1 × $t_{SFMA0cyc}$ – 12.5		8 × $t_{SFMA0cyc}$	ns
SFMA0SSL hold time	t_{SFMASH}		1.5 × $t_{SFMA0cyc}$		8.5 × $t_{SFMA0cyc}$ + 12.5	ns
Continuous transfer delay time	$t_{SFMACTD}$		1 × $t_{SFMA0cyc}$		8 × $t_{SFMA0cyc}$	ns
Data output delay time	$t_{SFMADOD}$				6.6	ns
Data output hold time	$t_{SFMADOH}$		–4.6			ns
Data output buffer on time	$t_{SFMADBON}$				6.6	ns
Data output buffer off time	$t_{SFMADBOFF}$		–7.0		3.0	ns

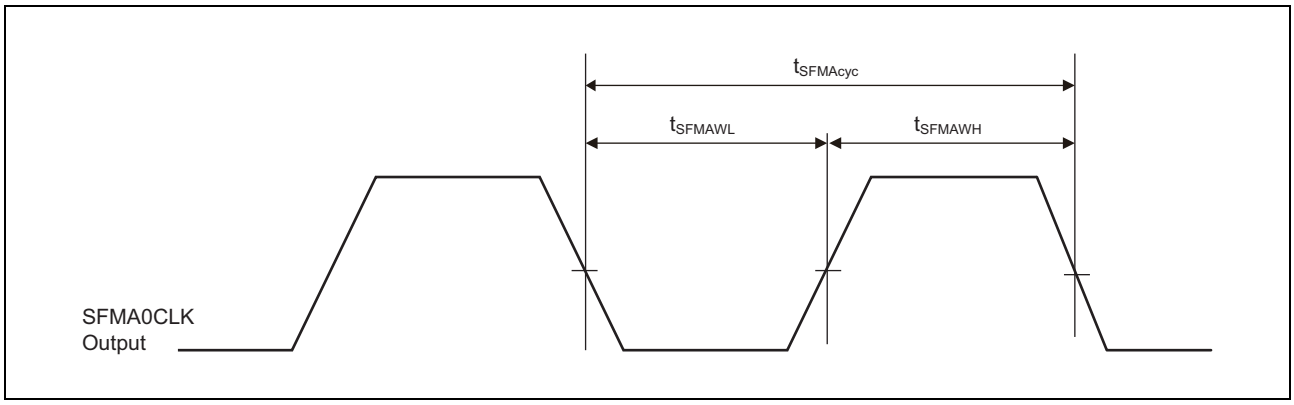


Figure 3.29 SFMA Clock Output Timing

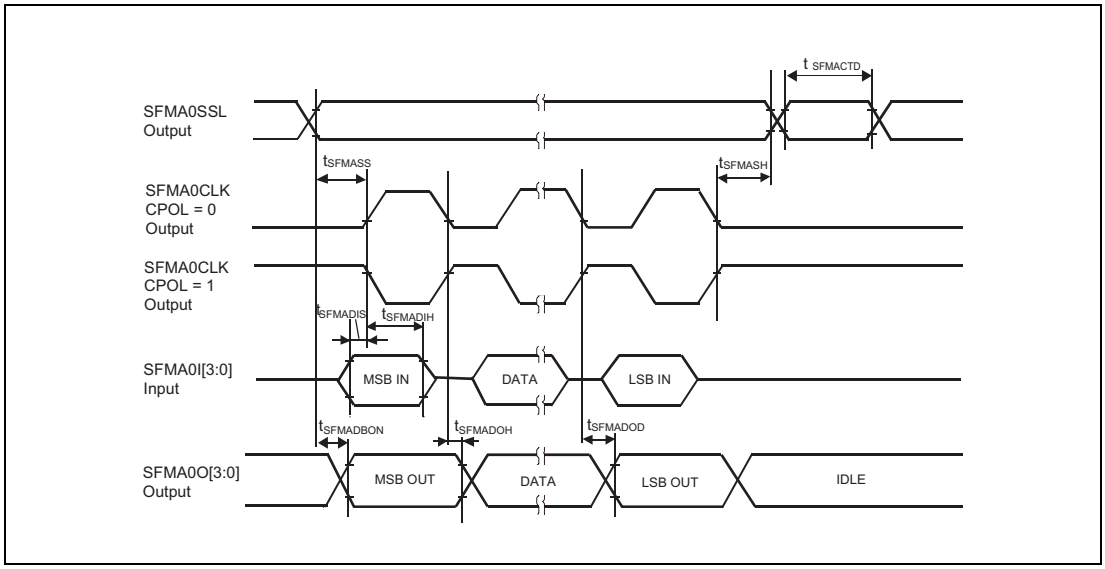


Figure 3.30 SFMA Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)

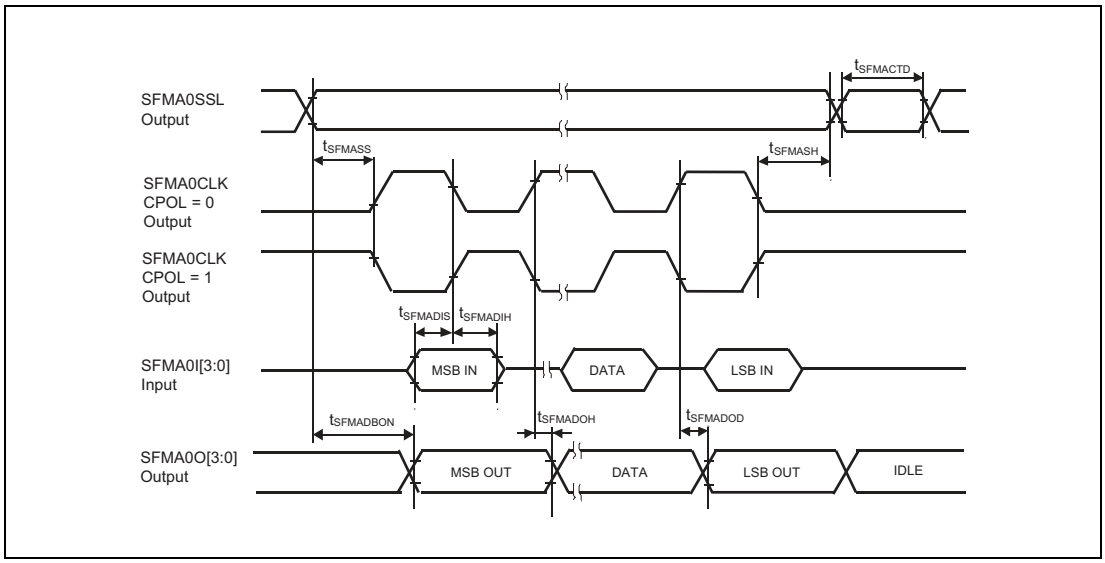


Figure 3.31 SFMA Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)

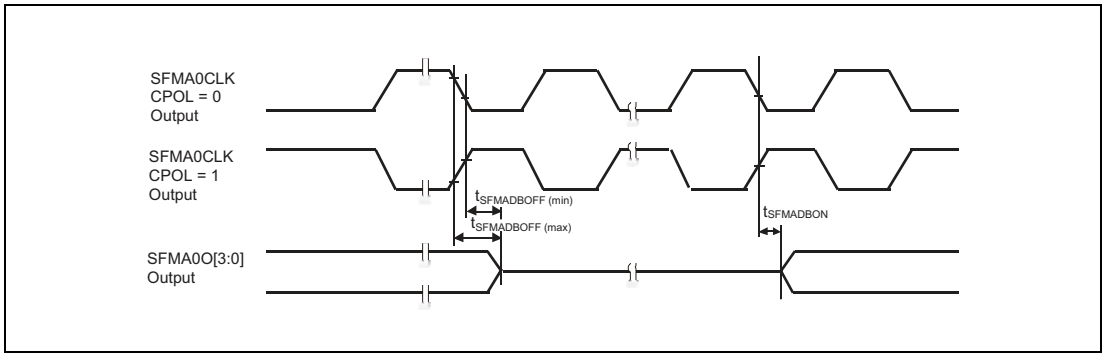


Figure 3.32 SFMA Timing Switching the Buffers on and off (CPHAT = 0, CPHAR = 0)

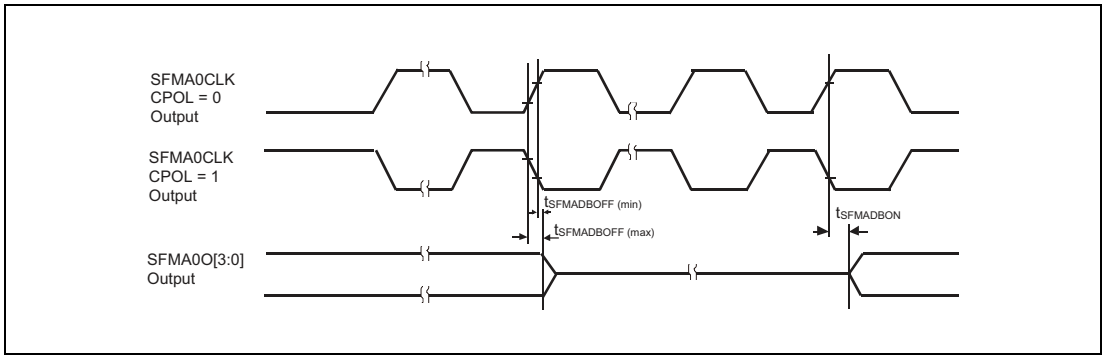


Figure 3.33 SFMA Timing for Switching the Buffers on and off (CPHAT = 1, CPHAR = 1)

3.3.10 MMCA Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.51 MMCA Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MMCA0CLK clock cycle	$t_{MMCA0CYC}$		25			ns
MMCA0CLK high time	$t_{MMCA0WH}$		6.5			ns
MMCA0CLK low time	$t_{MMCA0WL}$		6.5			ns
MMCA0CMD output data delay time	$t_{MMCA0CMDD}$		– 6.5		6.5	ns
Data output delay time	$t_{MMCA0DADD}$		– 6.5		6.5	ns
MMCA0CMD input data setup time	$t_{MMCA0CMS}$		7.5			ns
MMCA0CMD input data hold time	$t_{MMCA0CMH}$		2.5			ns
Data input setup time	$t_{MMCA0DAS}$		7.5			ns
Data input hold time	$t_{MMCA0DAH}$		2.5			ns

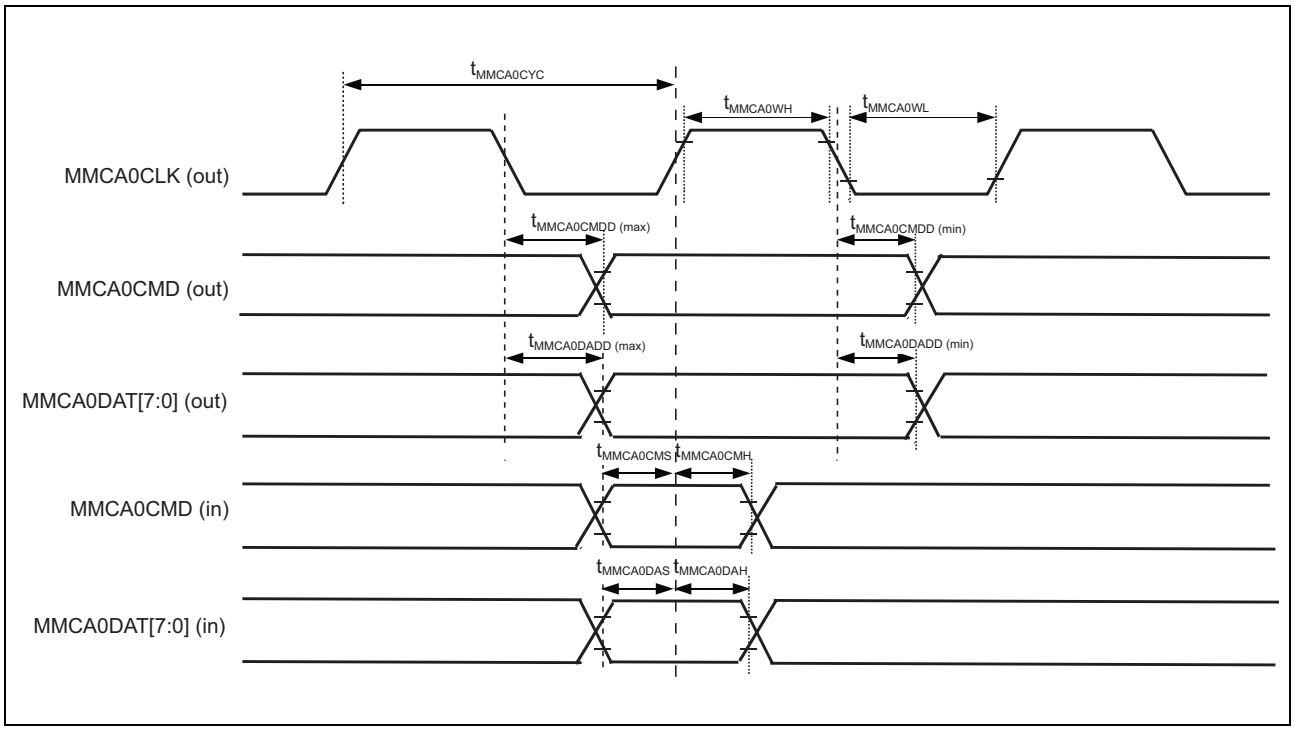


Figure 3.34 MMCA Timing

3.3.11 MSPI Timing

3.3.11.1 MSPI Communication Speed Overview

Table 3.52 MSPI Communication Speed Overview (1/3)

MSPIn pin name		Port	Max. Frequency
MSPI0	SC	P20_0	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SO	P20_1	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SI	P20_2	20 MHz
	SC	P06_6	10 MHz
	SO	P06_7	10 MHz
	SI	P06_5	10 MHz
	SC	P08_3	10 MHz
	SO	P02_14	10 MHz
	SI	P04_14	10 MHz
MSPI1	SC	P20_12	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SO	P20_13	20 MHz (The selection of "Drive strength = 1" (Very High) is available at equal or less than 10 MHz.)
	SI	P21_0	20 MHz
	SC	P02_3	10 MHz
	SO	P02_5	10 MHz
	SI	P02_4	10 MHz
	SC	P10_4	10 MHz
			20MHz (U2C4, U2C2)
	SO	P10_3	10 MHz
			20MHz (U2C4, U2C2)
	SI	P10_5	10 MHz
			20MHz (U2C4, U2C2)
MSPI2	SC	P17_4	20 MHz
	SO	P17_3	20 MHz
	SI	P17_5	20 MHz
	SC	P24_13	10 MHz
	SO	P24_12	10 MHz
	SI	P24_11	10 MHz
	SC	P06_2	10 MHz
	SO	P06_3	10 MHz
	SI	P06_1	10 MHz

Table 3.52 MSPI Communication Speed Overview (2/3)

MSPIn pin name		Port	Max. Frequency
MSPI3	SC	P22_1	20 MHz
	SO	P22_2	20 MHz
	SI	P22_0	20 MHz
	SC	P06_2	10 MHz
	SO	P06_4	10 MHz
	SI	P06_3	10 MHz
MSPI4	SC	P17_3	20 MHz
	SO	P17_5	20 MHz
	SI	P17_4	20 MHz
	SC	P20_6	10 MHz
	SO	P20_3	10 MHz
	SI	P20_7	10 MHz
	SC	P02_2	10 MHz
	SO	P02_1	10 MHz
	SI	P02_0	10 MHz
MSPI5	SC	P21_2	20 MHz
	SO	P21_3	20 MHz
	SI	P21_1	20 MHz
	SC	P02_7	10 MHz
	SO	P02_6	10 MHz
	SI	P02_8	10 MHz
	SC	P06_12	10 MHz
	SO	P06_11	10 MHz
	SI	P06_10	10 MHz
MSPI6	SC	P24_8	20 MHz
	SO	P24_10	20 MHz
	SI	P24_7	20 MHz
	SC	P10_2	10 MHz
	SO	P10_1	10 MHz
	SI	P10_0	10 MHz
	SC	P02_7	10 MHz
	SO	P02_8	10 MHz
	SI	P02_6	10 MHz
MSPI7	SC	P24_9	20 MHz
	SO	P24_11	20 MHz
	SI	P24_10	20 MHz
	SC	P04_5	10 MHz
	SO	P04_4	10 MHz
	SI	P04_6	10 MHz

Table 3.52 MSPI Communication Speed Overview (3/3)

MSPIn pin name		Port	Max. Frequency
MSPI8	SC	P20_9	20 MHz
	SO	P20_10	20 MHz
	SI	P20_11	20 MHz
	SC	P03_11	10 MHz
	SO	P03_1	10 MHz
	SI	P03_10	10 MHz
MSPI9	SC	P21_7	20 MHz
	SO	P21_9	20 MHz
	SI	P21_8	20 MHz
	SC	P02_13	10 MHz
	SO	P02_11	10 MHz
	SI	P02_12	10 MHz

3.3.11.2 MSPI Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.53 MSPI Timing (Master mode : Communication Speed 10MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*5	T_{SCKCYC}		100			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 30 pF Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 9			ns
		CL = 50 pF Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 12			ns
		CL = 100 pF Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 23			ns
		CL = 30 pF Drive strength = 4 (Low)	0.5 × T_{SCKCYC} – 15.5			ns
		CL = 50 pF Drive strength = 2 (High)	0.5 × T_{SCKCYC} – 10			ns
		CL = 100 pF Drive strength = 1*4 (Very High)	0.5 × T_{SCKCYC} – 10			ns
Chip select signal setup time*2*6	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] × $T_{MSPInCLK}$ - 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] × $T_{MSPInCLK}$ - 5			ns
Receive data setup time (MSPInSAMP =0)	T_{MSISU1}		20			ns
Receive data setup time (MSPInSAMP =1)	T_{MSISU2}		20			ns
Receive data hold time (MSPInSAMP =0)	T_{MSIHO}		0			ns
Receive data hold time (MSPInSAMP =1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}		—		7	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC} / 2) – 5			ns

Note 1. This parameter is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].
Note 2. This parameter is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.
Note 3. This parameter is programmable, the value can be set by MSPInHOLDm.
Note 4. The selection of "Drive strength = 1" is available on P20_0 and P20_12 only.
Note 5. Use by “PCLK/2 ≧ MSPInSCK”.
Note 6. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.54 MSPI Timing (Master mode : Communication Speed 20MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle*1*4	T_{SCKCYC}		50			ns
MSPInSCK Low/High width*1	T_{SCKWID}	CL = 15pF@50Ω Drive strength = 3 (Medium)	0.5 × T_{SCKCYC} – 6			ns
Chip select signal setup time*2*5	T_{MCSSU}	$T_{MSPInCLK}$ = 12.5 ns	MSPInSEUPm [11:0] × $T_{MSPInCLK}$ – 15			ns
Chip select signal hold time*3	T_{MCSHO}	$T_{MSPInCLK}$ = 12.5 ns	MSPInHOLDm [11:0] × $T_{MSPInCLK}$ – 5			ns
Receive data setup time (MSPInSAMP = 1)	T_{MSISU2}		20			ns
Receive data hold time (MSPInSAMP = 1)	T_{MSIHO}		0			ns
Transmit data delay time	T_{MSODL}		—		7	ns
Transmit data hold time	T_{MSOHL}		(T_{SCKCYC} / 2) – 5			ns

Note 1. This parameter is programmable, the value can be set by MSPInPRCSm[1:0] and MSPInCDIVm[4:0].

Note 2. This parameter is programmable, the value can be set by MSPInSEUPm[11:0] and it must be set to 002_H or above.

Note 3. This parameter is programmable, the value can be set by MSPInHOLDm.

Note 4. Use by “PCLK/2 ≧ MSPInSCK”.

Note 5. When using the MSPI at master mode with the setting MSPInCFGm1.MSPInCPHAm = 0, set the period from CS active to the first edge of SCK to 1/2 or more of the communication rate by MSPInSEUPm.

Table 3.55 MSPI Timing (Slave mode : Communication Speed 10MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		100			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 23$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}		—		54	ns
Transmit data delay time 2 (MSPInCSIE = 1)	T_{SSODL2}		—		40	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC} / 2) - 5$			ns
Transmit data release time (MSPInCSIE = 1)	T_{SSOREL}		—		40	ns

Table 3.56 MSPI Timing (Slave mode : Communication Speed 20MHz)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MSPI operation clock cycle	$T_{MSPInCLK}$		12.5			ns
MSPInSCK cycle	T_{SCKCYC}		50			ns
MSPInSCK Low/High width	T_{SCKWID}		$0.5 \times T_{SCKCYC} - 6$			ns
Chip select signal setup time (MSPInCSIE = 1)	T_{SCSSU}		15			ns
Chip select signal hold time (MSPInCSIE = 1)	T_{SCSHO}		10			ns
Receive data setup time	T_{SSISU}		6			ns
Receive data hold time	T_{SSIHO}		5			ns
Transmit data delay time 1	T_{SSODL1}		—		24	ns
Transmit data delay time 2 (MSPInCSIE = 1)	T_{SSODL2}		—		40	ns
Transmit data hold time	T_{SSOHL}		$(T_{SCKCYC} / 2) - 5$			ns
Transmit data release time (MSPInCSIE = 1)	T_{SSOREL}		—		40	ns

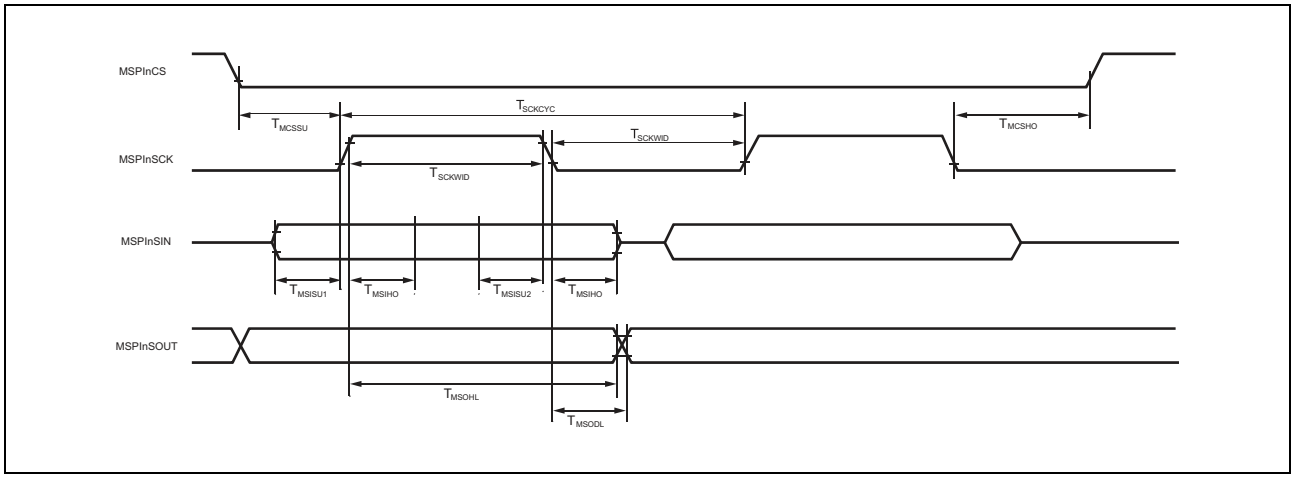


Figure 3.35 MSPIn Timing (Master Mode, MSPInCPHAm = 0)

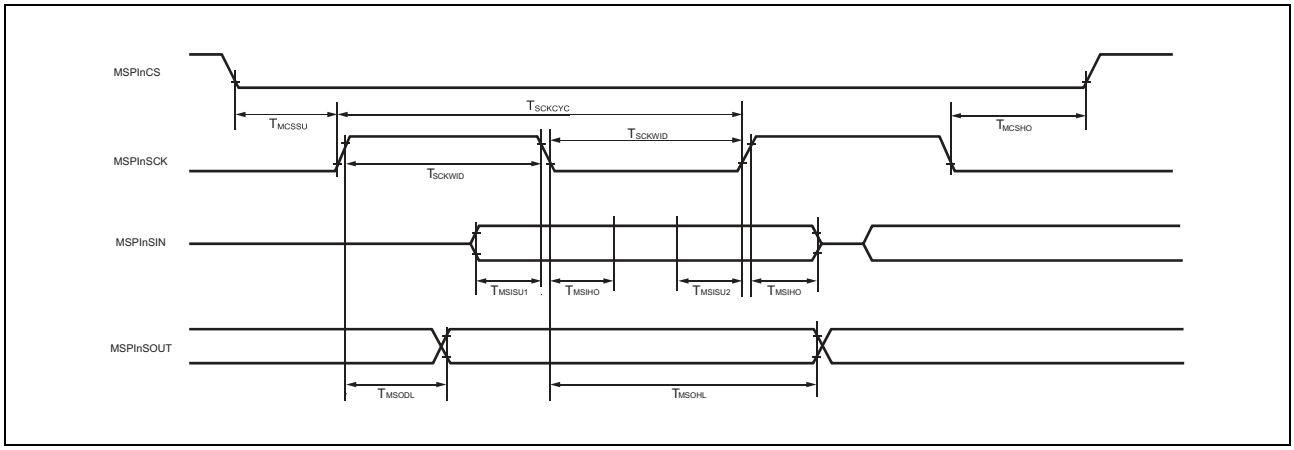


Figure 3.36 MSPIn Timing (Master Mode, MSPInCPHAm = 1)

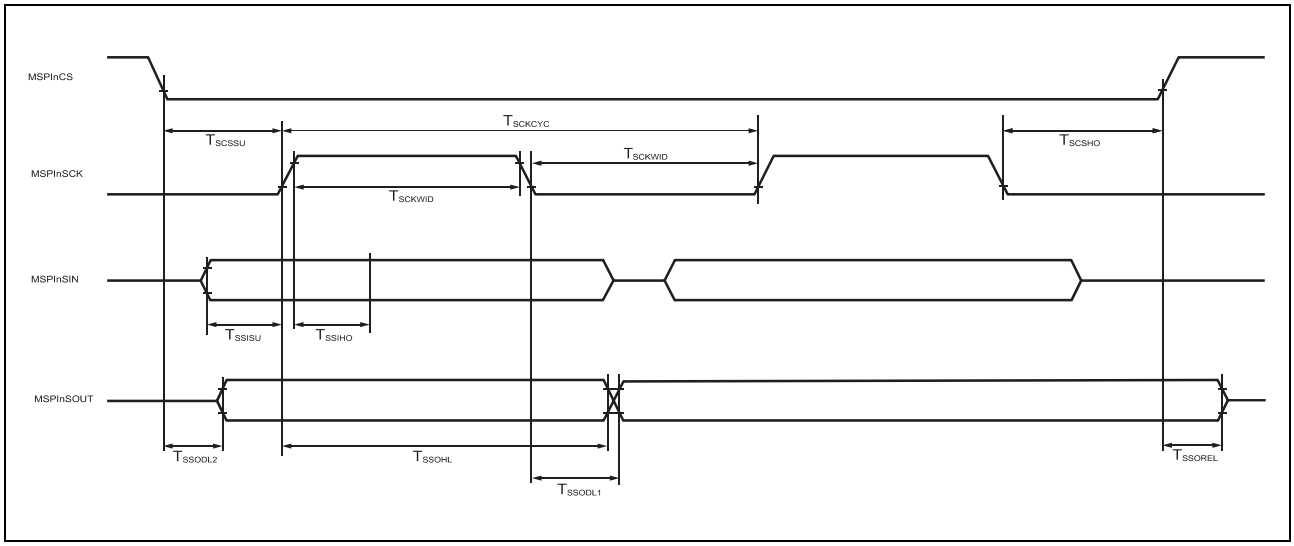


Figure 3.37 MSPIn Timing (Slave Mode, MSPInCPHA0 = 0)

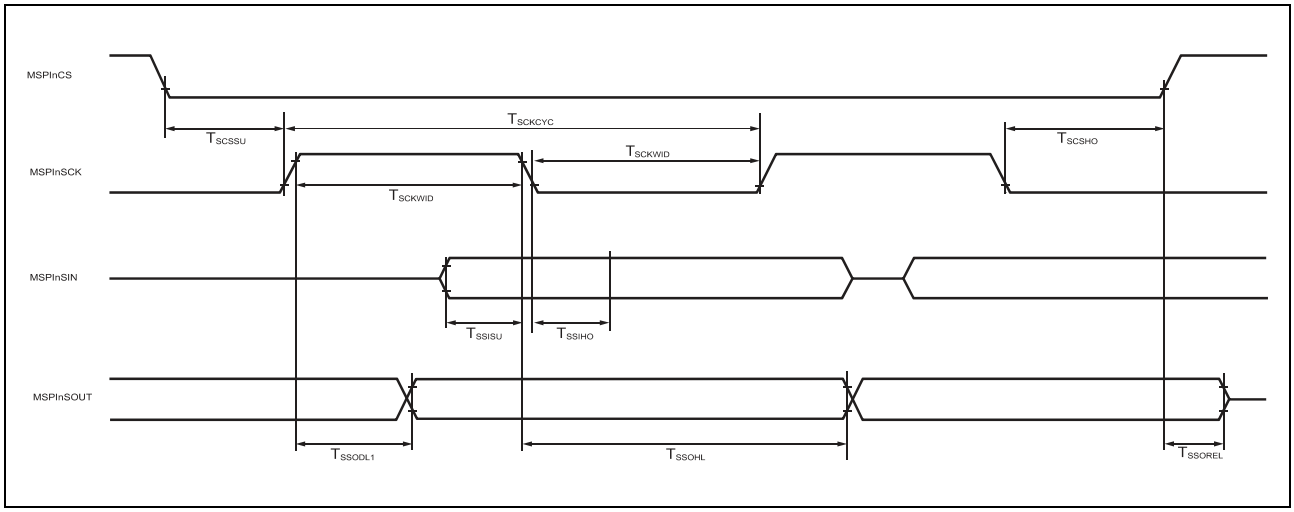


Figure 3.38 MSPIn Timing (Slave Mode, MSPInCPHA0 = 1)

3.3.12 RLIN3 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.57 RLIN3 Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate	r_{RLin}	LIN mode			20	kbps
	r_{RLine}	LIN extended baud rate*1			115.2	kbps
	r_{RLurt}	UART mode (LIN communication clock is 100MHz)			25	Mbps
		UART mode (LIN communication clock is 80MHz)			20	Mbps

Note 1. The LIN extended baud rate is not part of the LIN standard specification.

3.3.13 RI3C Timing

Table 3.58 RI3C Pin group specification

RI3Cn pin name	Group	Mode	Port (RI3CnSCL)	Port (RI3CnSDA)
RI3C0	Group1	I3C/I2C	P21_2	P21_3
	Group2	I2C	P24_6	P24_5
	Group3	I2C	P03_1	P03_0
RI3C1	Group1	I3C/I2C	P17_5	P17_4
	Group2	I2C	P06_8	P06_9
RI3C2	Group1	I3C/I2C	P24_11	P24_12
	Group2	I2C	P10_13	P10_12
RI3C3	Group1	I3C/I2C	P22_1	P22_0
	Group2	I2C	P21_7	P21_6

3.3.13.1 I2C Mode

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.59 I2C Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RI3CnSCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RI3CnSCL clock low level width	t_{LOW}		4.7			µs
RI3CnSCL clock high level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		I^2C mode	0*2		*3	µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs

Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RI3CnSDA signal (at VIH min. of RI3CnSCL signal). In order to occupy the undefined area at the falling edge of RI3CnSCL.

Note 3. If the system does not extend the RI3CnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Table 3.60 I2C Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RI3CnSCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RI3CnSCL clock low level width	t_{LOW}		1.3			µs
RI3CnSCL clock high level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	I^2C mode	0*2		*5	µs
Data setup time	t_{SU}: DAT		100*3			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		*4	ns

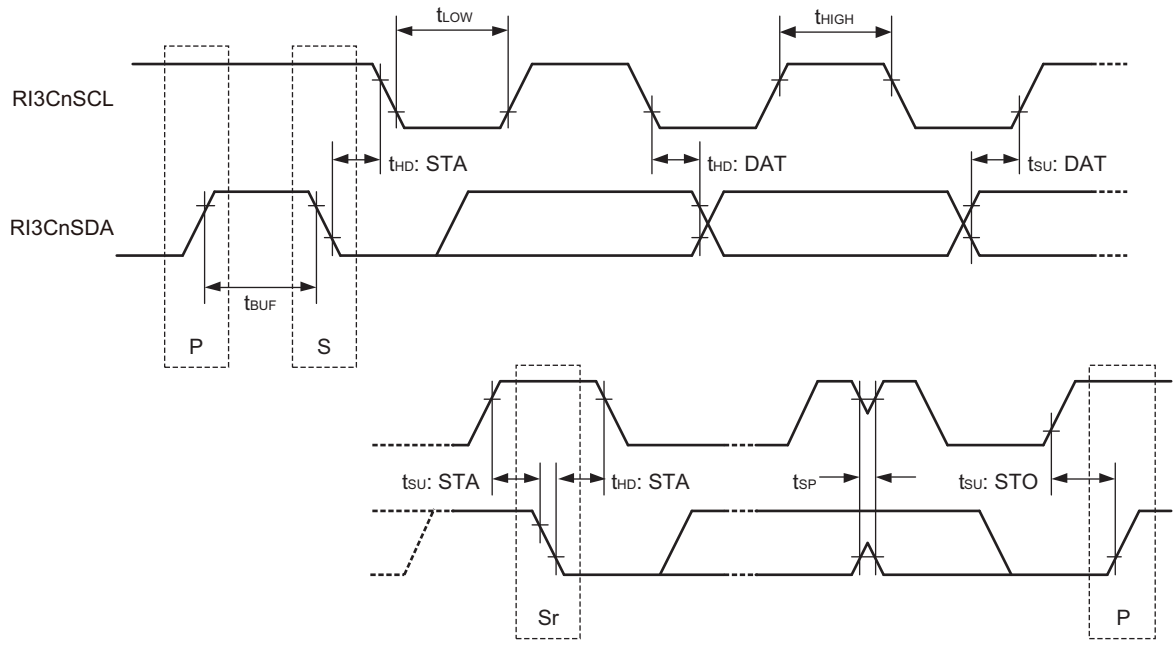
Note 1. At the start condition, the first clock pulse is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RI3CnSDA signal (at VIH min. of RI3CnSCL signal). In order to occupy the undefined area at the falling edge of RI3CnSCL.

Note 3. The fast mode I^2C bus can be used in normal mode I^2C bus system. In this case, set the fast mode I^2C bus so that it meets the following conditions.
- If the system does not extend the RI3CnSCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RI3CnSCL signal's low state hold time:
Transmit the following data bit to the RI3CnSDA line prior to releasing the RI3CnSCL line (1250 ns: Normal mode I^2C bus specification).

Note 4. The filtered width is specified by the frequency of I2CΦ and the value of RI3CnMR3.NF[1:0].

Note 5. If the system does not extend the RI3CnSCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.



Note
P: Stop condition S: Start condition Sr: Restart condition

Figure 3.39 I2C Timing

3.3.13.2 I3C Mode

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- CL = 50 pF
- Buffer type = SHMT1

Table 3.61 I3C Timing (Open Drain Timing)

Parameter	Symbol	Timing Diagram	MIN.	TYP.	MAX.	Unit
RI3CnSCL Clock Low Period	t_{LOW_OD} *1*2	**Figure 3.43**	200			ns
	$t_{DIG\_OD\_L}$	**Figure 3.43**	t_{LOW_ODmin} + $t_{fDA\_OD\_min}$			ns
RI3CnSCL Clock High Period	t_{HIGH} *3*4	**Figure 3.41**			41	ns
	t_{DIG_H}	**Figure 3.41**			t_{HIGH} + t_{CF}	ns
RI3CnSDA Signal Fall Time	t_{fDA_OD}	**Figure 3.43**	t_{CF}		12	ns
RI3CnSDA Data Setup Time Open Drain Mode	t_{SU_OD} *1	**Figure 3.42** **Figure 3.43**	3			ns
Clock After START (S) Condition	t_{CAS} *5*6	**Figure 3.43**	38.4		For ENAS0: 1 µ	seconds
					For ENAS1: 100 µ	
					For ENAS2: 2 milli	
					For ENAS3: 50 milli	
Clock Before STOP (P) Condition	t_{CBP}	**Figure 3.44**	t_{CASmin} / 2			seconds
Current Master to Secondary Master Overlap time during handoff	$t_{MMOverlap}$	**Figure 3.49**	$t_{DIG\_OD\_Lmin}$			ns
Bus Available Condition	t_{AVAL} *7	-	1			µs
Bus Idle Condition	t_{IDLE}	-	1			ms
Time Internal Where New Master Not Driving RI3CnSDA Low	t_{MMLock}	**Figure 3.49**	$t_{AVALmin}$			µs

Note 1. This is approximately equal to t_{LOWmin} + t_{DS_ODmin} + t_{rDA_ODtyp} + t_{SU_ODmin}

Note 2. The Master may use a shorter Low period if it knows that this is safe, i.e., that RI3CnSDA is already above VIH

Note 3. Based on t_{SPIKE}, rise and fall times, and interconnect

Note 4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I2C Devices, and/or in consideration of the interconnect (e.g., a short Bus).

Note 5. On a Legacy Bus where I2C Devices need to see Start

Note 6. Slaves that do not support the optional ENTASx CCCs shall use the t_{CAS} Max value shown for ENTAS3

Note 7. On a Mixed Bus with Fm Legacy I2C Devices, t_{AVAL} is 300ns shorter than the Fm Bus Free Condition time (t_{BUF})

Table 3.62 I3C Timing (Push-pull Timing)

Parameter		Symbol	Timing Diagram	MIN.	TYP.	MAX.	Unit
RI3CnSCL Clock Frequency		f_{SCL} *1		0.01	12.5	12.9	MHz
RI3CnSCL Clock Low Period		t_{LOW}	**Figure 3.40**	24			ns
		t_{DIG_L} *2*4	**Figure 3.41**	32			ns
RI3CnSCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	**Figure 3.41**	24			ns
		$t_{DIG\_H\_MIXED}$ *2*3	**Figure 3.41**	32		45	ns
RI3CnSCL Clock High Period		t_{HIGH}	**Figure 3.40**	24			ns
		t_{DIG_H} *2	**Figure 3.41** **Figure 3.40**	32			ns
Clock in to Data Out for Slave		t_{SCO}	**Figure 3.46**			12	ns
RI3CnSCL Clock Rise Time		t_{CR}	**Figure 3.40**			150*1 /f_{SCV} (capped at 60)	ns
RI3CnSCL Clock Fall Time		t_{CF}	**Figure 3.40**			150*1 /f_{SCV} (capped at 60)	ns
RI3CnSDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP} *4	**Figure 3.45**	t_{CR} + 3 and t_{CF} + 3			
	Slave	t_{HD_PP}	**Figure 3.47**	0			
RI3CnSDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	**Figure 3.45** **Figure 3.46**	3		N/A	ns
Clock After Repeated START (Sr)		t_{CASr}	**Figure 3.48**	t_{CASmin}		N/A	ns
Clock Before Repeated START (Sr)		t_{CBSr}	**Figure 3.48**	t_{CASmin} / 2		N/A	ns
Capacitive Load per Bus Line (RI3CnSDA/RI3CnSCL)		C_b				50	pF

Note 1. $F_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$

Note 2. t_{DIG_L} and t_{DIG_H} are the clock Low and High periods as seen at the receiver end of the I3C Bus using V_{IL} and V_{IH} (see **Figure 3.40**)

Note 3. When communicating with an I3C Device on a mixed Bus, the $t_{DIG\_H\_MIXED}$ period must be constrained in order to make sure that I2C Devices do not interpret I3C signaling as valid I2C signaling.

Note 4. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., t_{CF} + 3 for falling edge clocks, and t_{CR} + 3 for rising edge clocks.

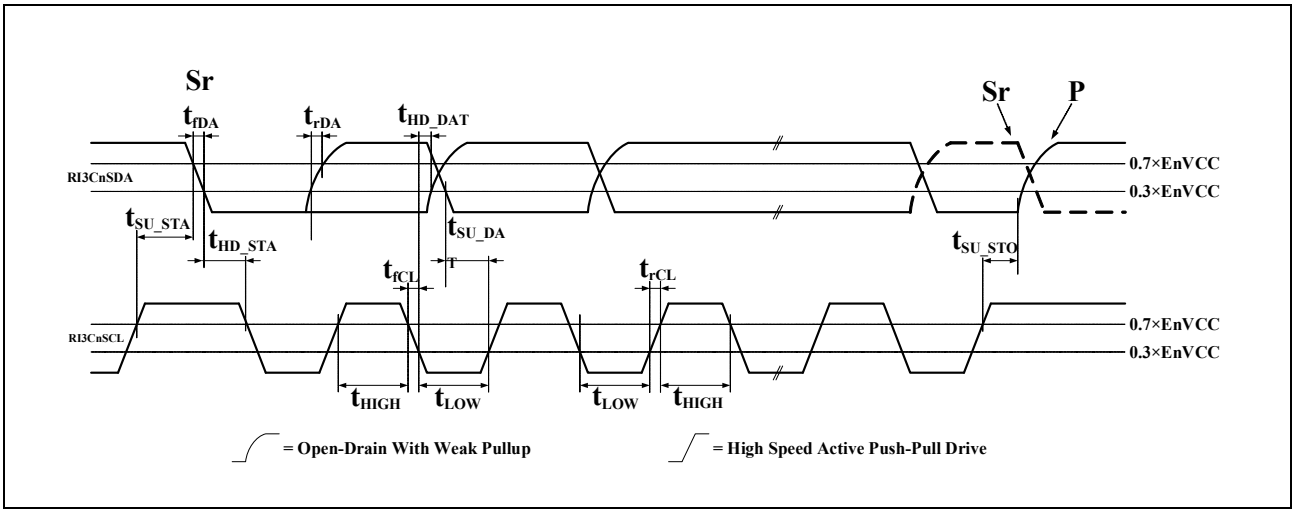


Figure 3.40 I^2C Mode (I3C Legacy Mode) Timing

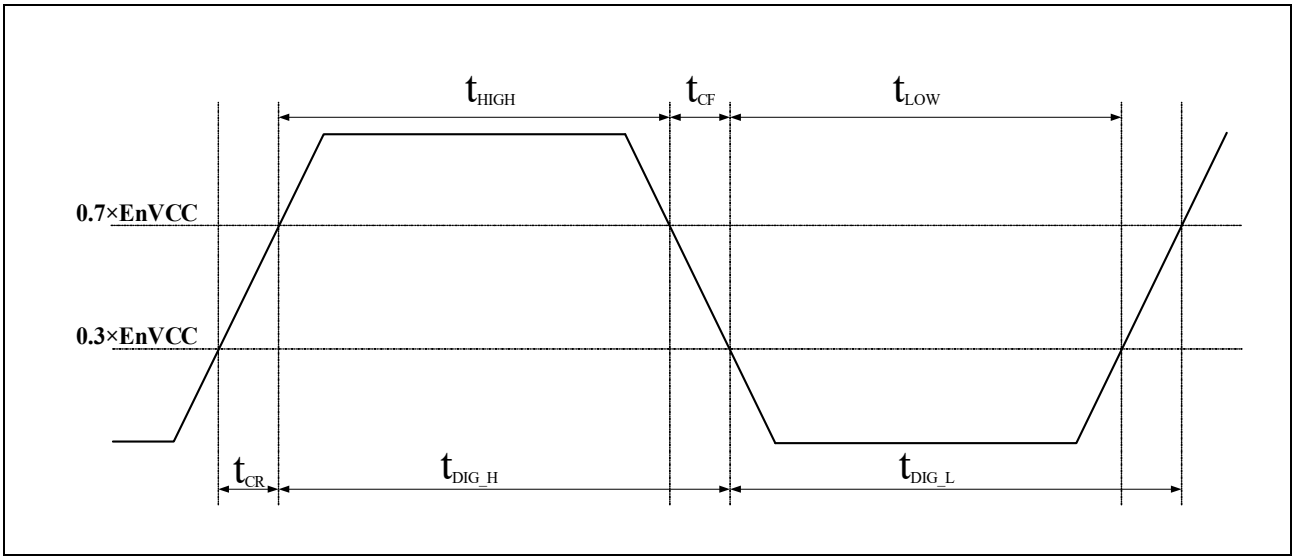


Figure 3.41 t_{DIG_H} and t_{DIG_L}

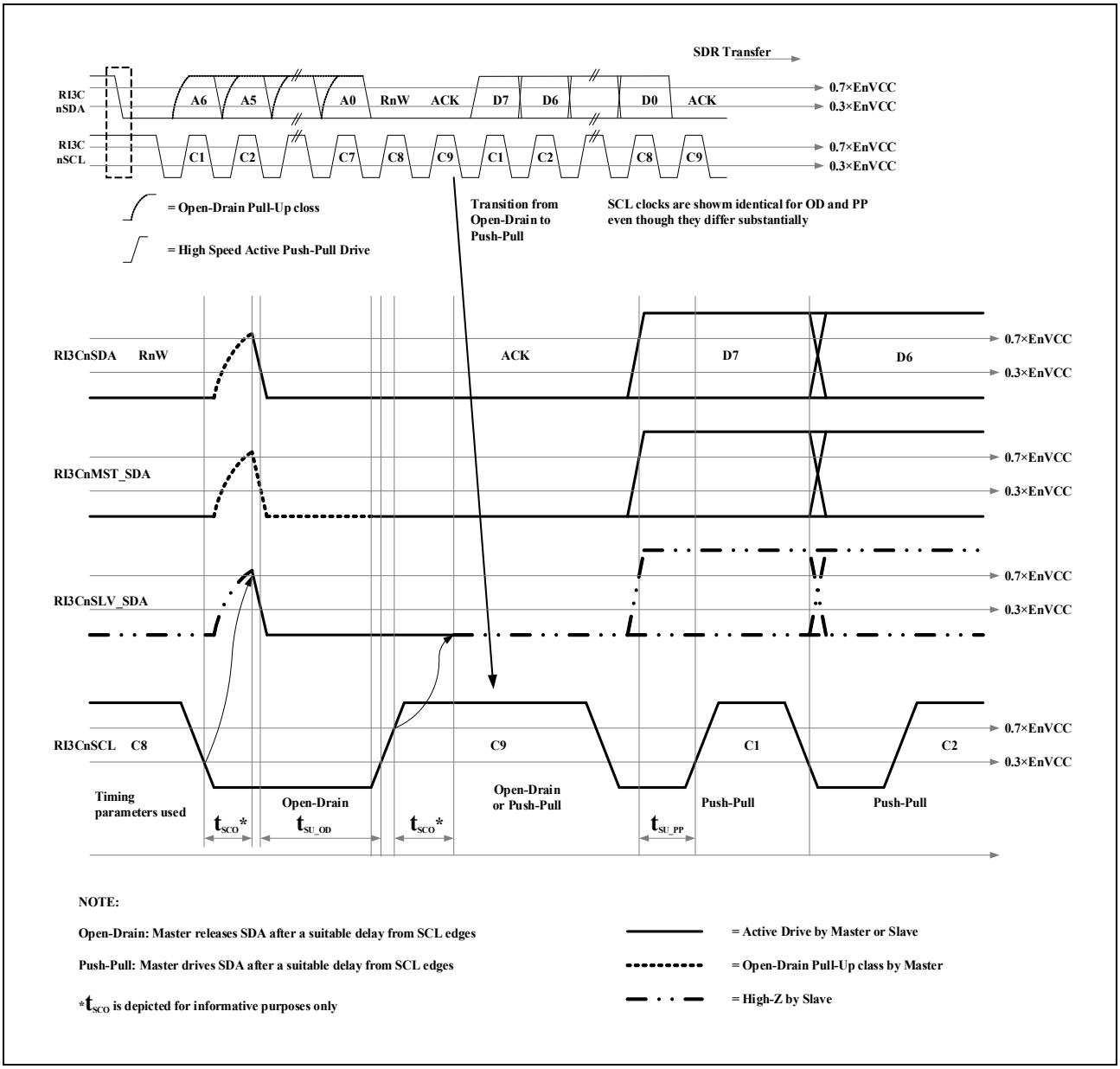


Figure 3.42 I3C Data Transfer – ACK by Slave

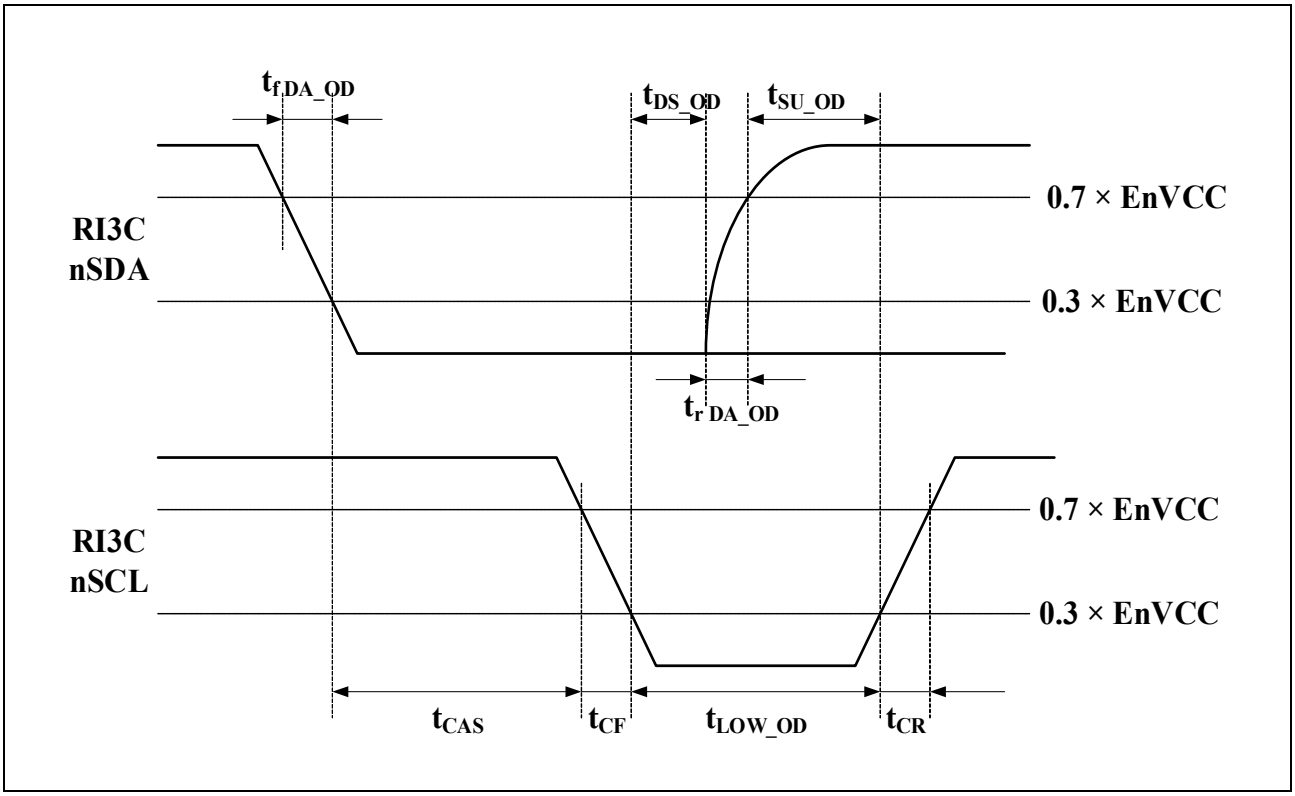


Figure 3.43 I3C START condition Timing

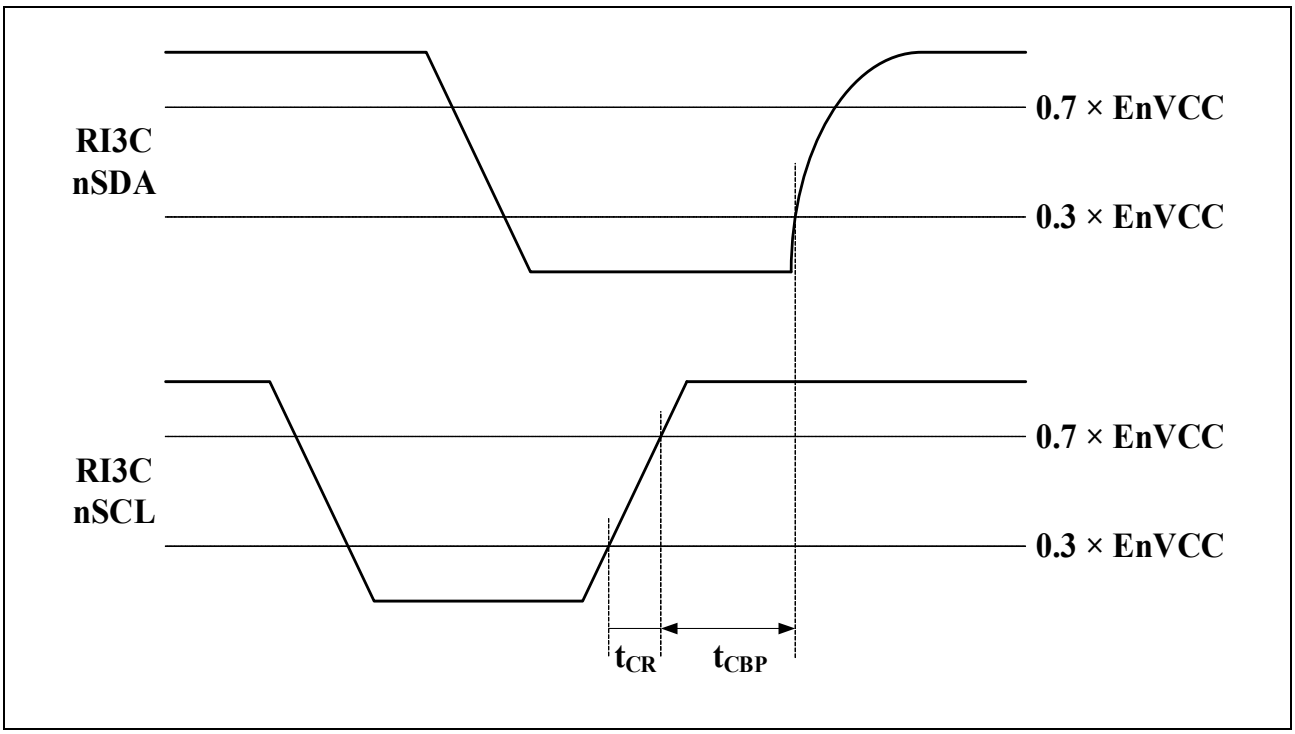


Figure 3.44 I3C STOP condition Timing

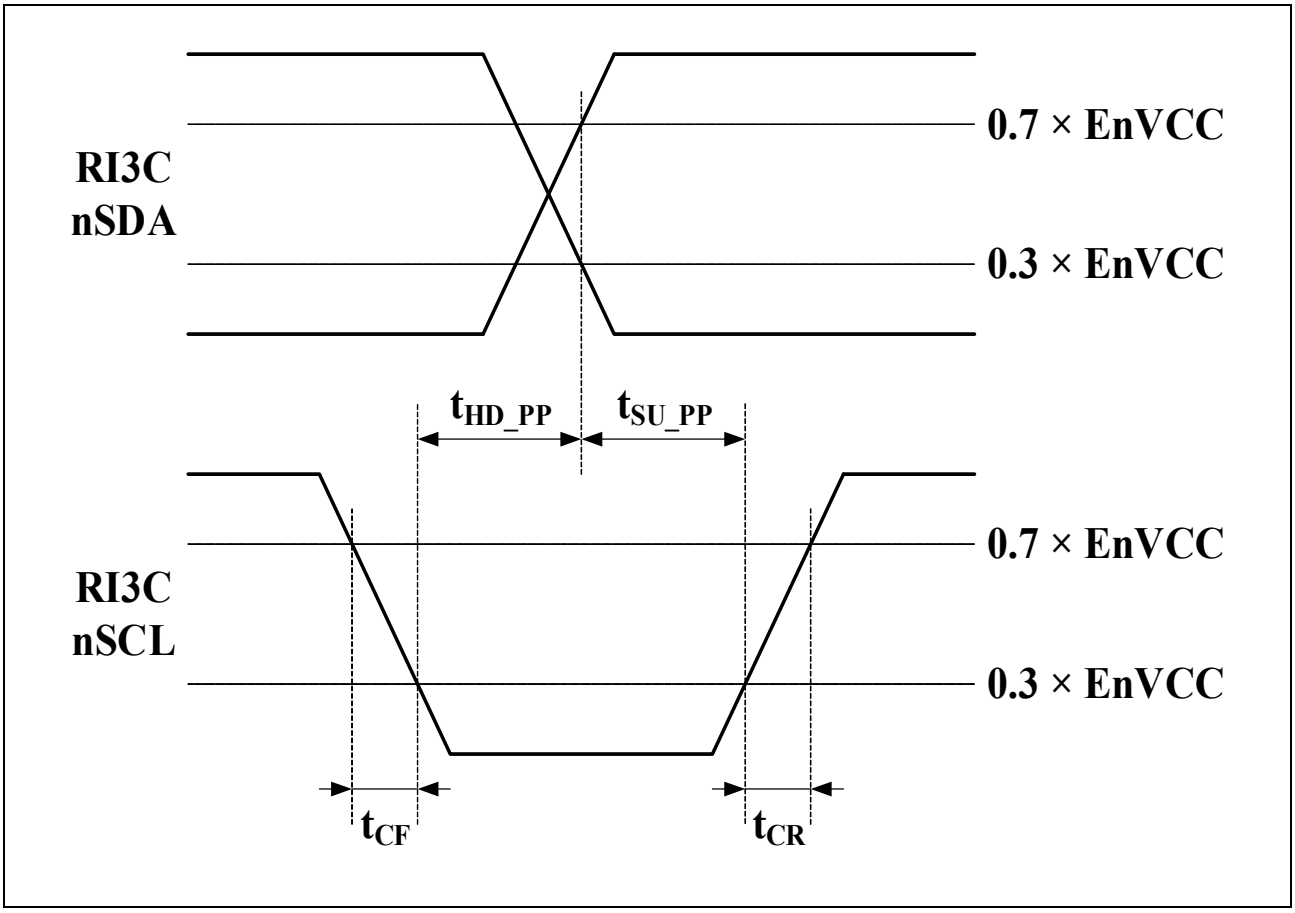


Figure 3.45 I3C Master Out Timing

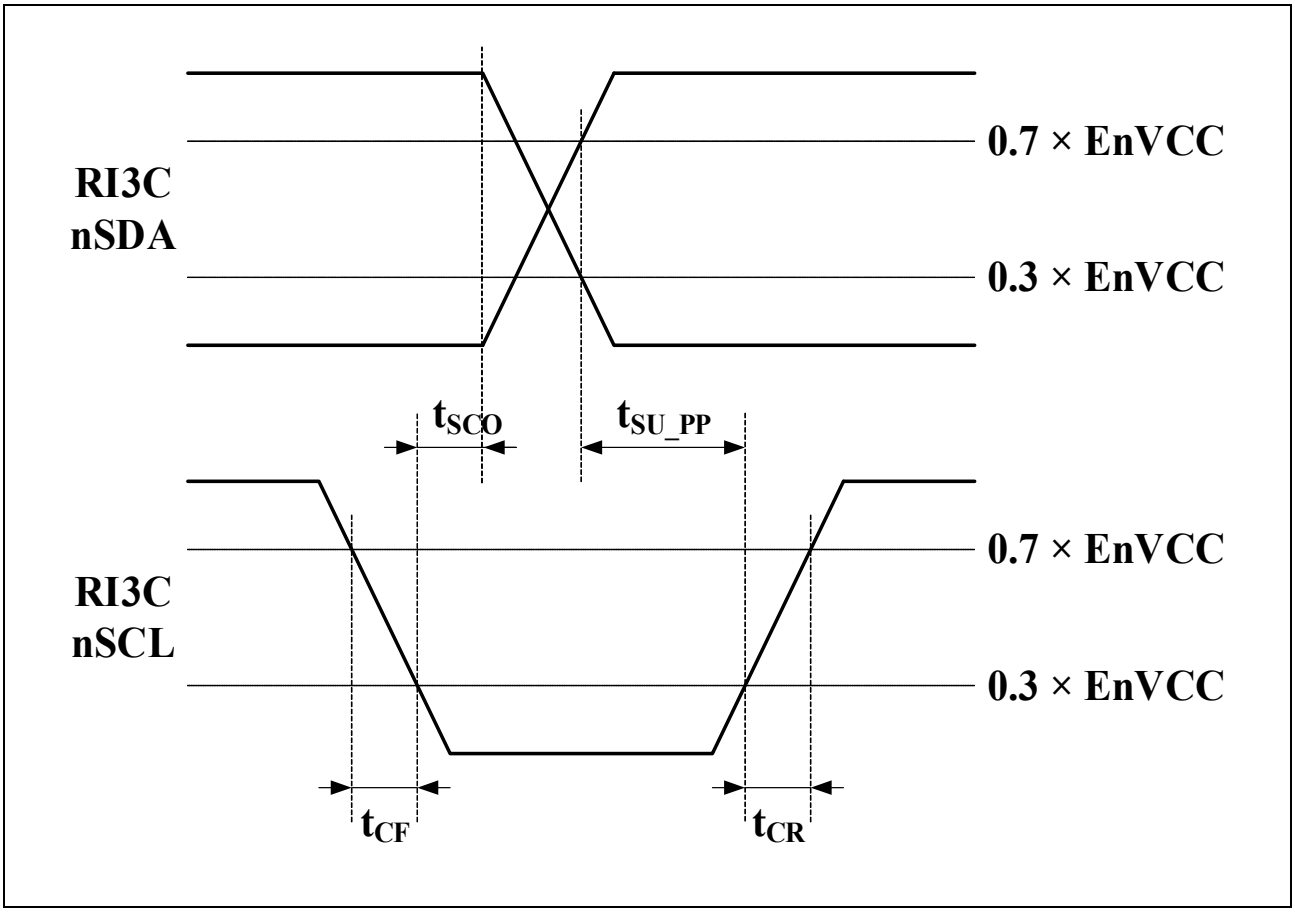


Figure 3.46 I3C Slave Out Timing

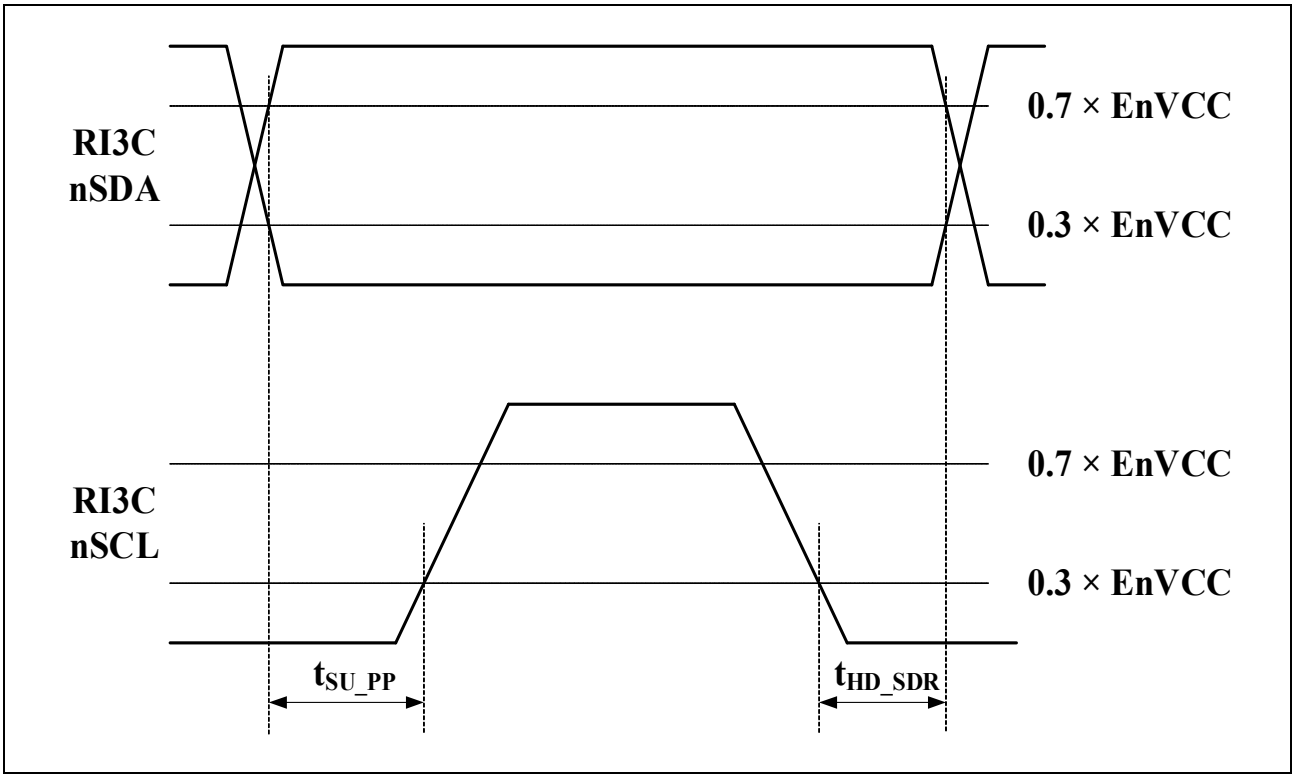


Figure 3.47 Master SDR Timing

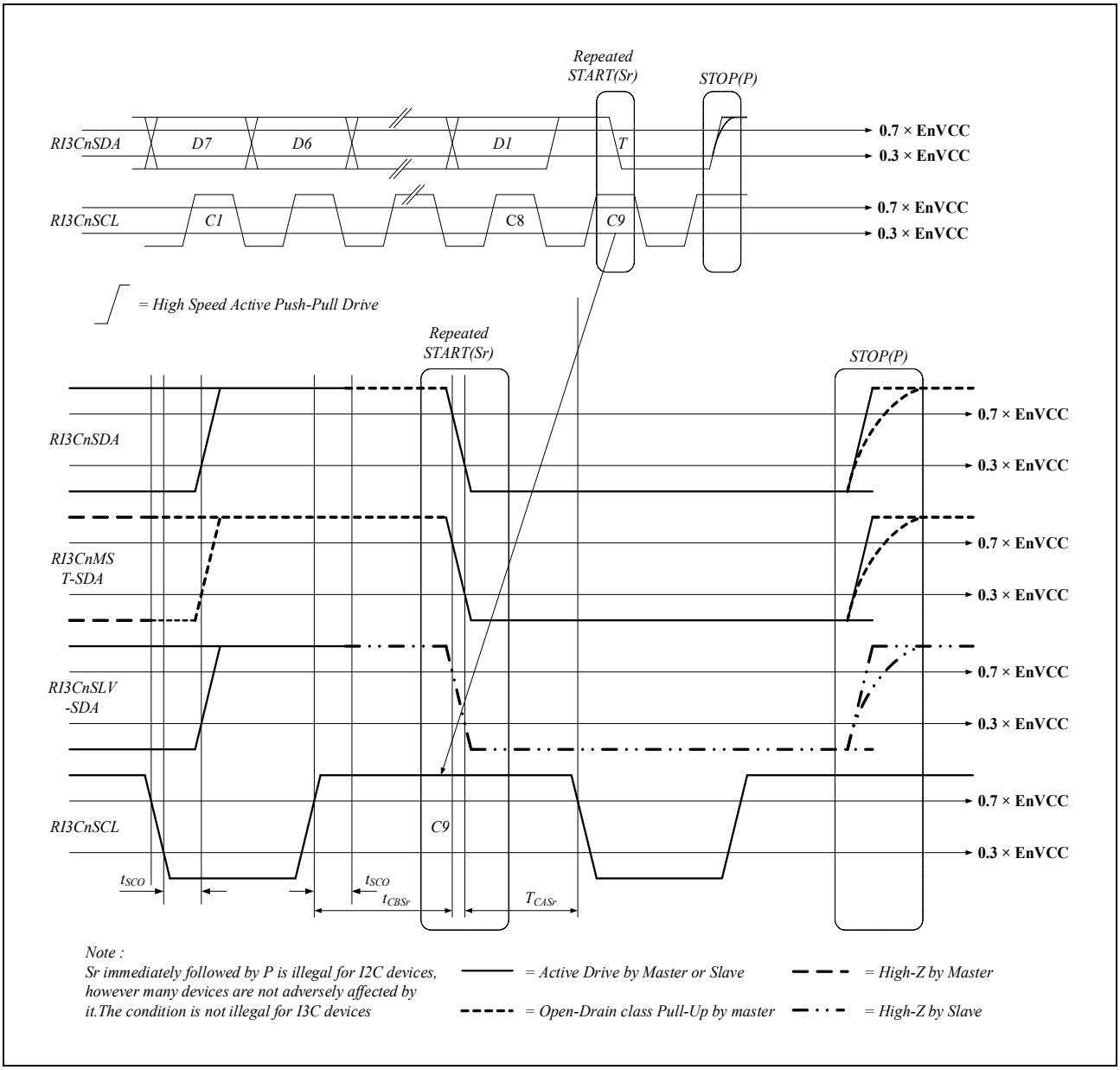


Figure 3.48 T-Bit When Master Ends Read with Repeated START and STOP

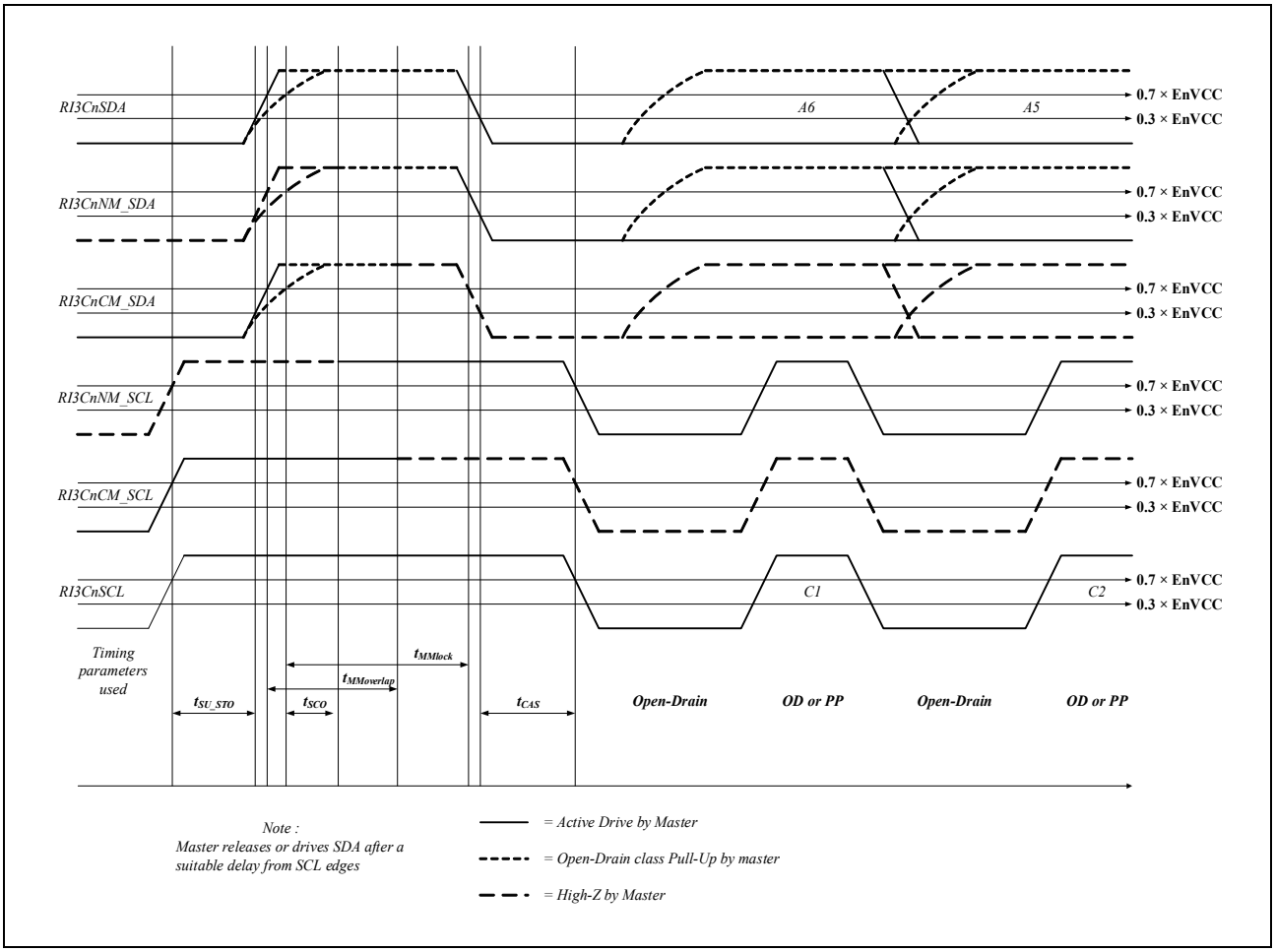


Figure 3.49 Master to Master Bus Handoff

3.3.14 RS-CANFD Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.63 RS-CANFD Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	r_{CN1}	Classical CAN mode			1	Mbps
	r_{CN2}	CAN FD mode (nominal bit rate)			1	Mbps
	r_{CN3}	CAN FD mode (data bit rate)			8	Mbps
Internal delay time	t_{DCIN}	$t_{INPUT} + t_{OUTPUT}$			50	ns

Note 1. For the configuration of the transfer speed, see the RH850/U2C Group User's Manual: Hardware Section 22.5.1.3, Baud Rate.

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file "*Limited_conditions_for_AC_specification.xlsx*".

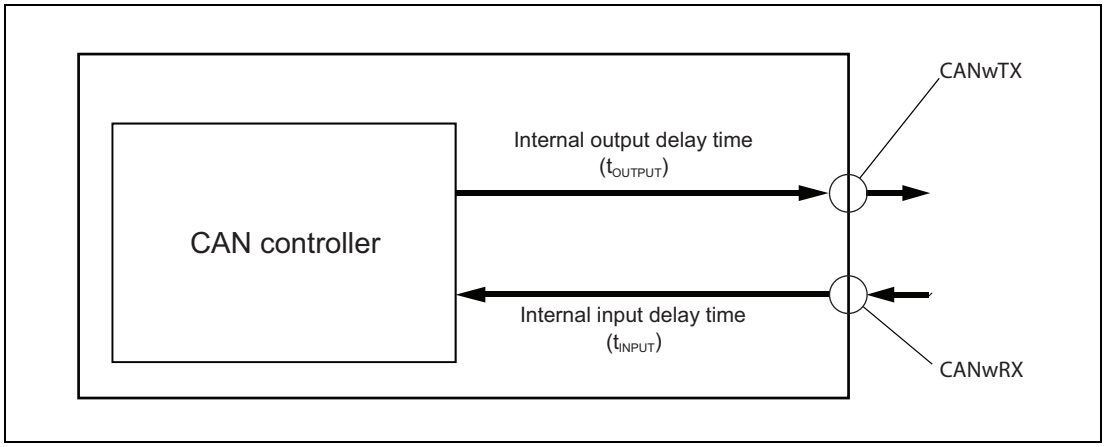


Figure 3.50 RS-CANFD Timing

3.3.15 CANXL Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.64 CANXL Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	r_{CN1}	Classical CAN mode			1	Mbps
	r_{CN2}	CAN FD mode (nominal bit rate)			1	Mbps
	r_{CN3}	CAN FD mode (data bit rate)			8	Mbps
	r_{CN4}	CANXL mode			20	Mbps
Internal delay time	t_{DCIN0}	$t_{INPUT} + t_{OUTPUT}$			40	ns
	t_{DCIN1}	$t_{INPUT} + t_{OUTPUT}$			50	ns

Note 1. The definition of the internal delay time is different for each pin. For details, see **Table 3.65**

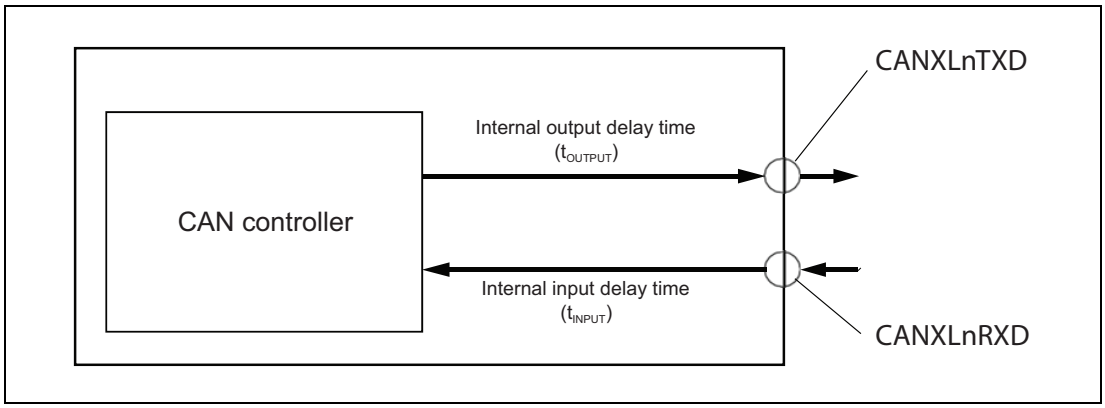


Figure 3.51 CANXL Timing

Table 3.65 CANXL internal delay

Unit	Group	Port (CANXLnRXD)	Port (CANXLnTXD)	Delay definition
CANXL0	Group1	P17_2	P17_3	t_{DCIN0}
	Group2	P10_0	P10_1	t_{DCIN1}
	Group3	P06_1	P06_0	t_{DCIN1}
	Group4	P20_3	P20_4	t_{DCIN1}
CANXL1	Group1	P24_8	P24_7	t_{DCIN0}
	Group2	P10_2	P10_3	t_{DCIN1}

Table 3.66 PWM mode pulse timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PWM pulse high width	t_{PWMH}	*1	(PWMS + 1) × 6.25 - 5	(PWMS + 1) × 6.25	(PWMS + 1) × 6.25 + 5	ns
PWM pulse low width	t_{PWML}	*1	(PWMS + 1) × 6.25 - 5	(PWMS + 1) × 6.25	(PWMS + 1) × 6.25 + 5	ns

Note 1. PWMS is the value of PWME_CFG.PWMS[5:0]. PWMS must be set to 1 or greater. Values smaller than 2 cycles cannot be set to the pulse width.

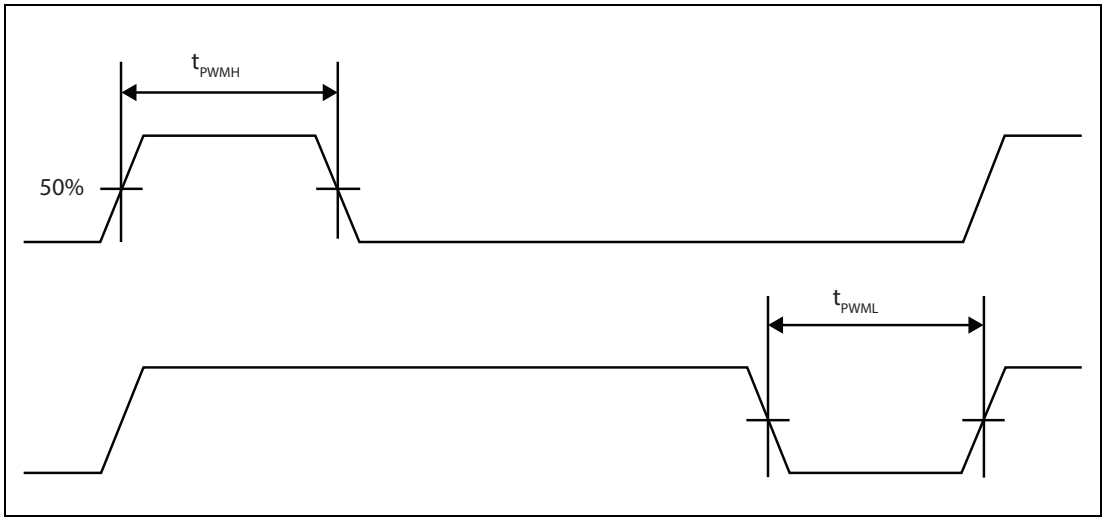


Figure 3.52 PWM mode pulse timing

3.3.16 FlexRay Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 2 (High)
- Buffer type = SHMT1

Table 3.67 FlexRay Timing*1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	rFLXA				10	Mbps

Note 1. Base of this specification is “FlexRay Electrical Physical Layer Specification V3.0.1, Oct-2010”

3.3.17 RSENT Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4 (Low)
- Buffer type = SHMT1

Table 3.68 RSENT Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Tick Time			1		90	µs

3.3.18 Renesas High-speed Serial I/F Timing (For debug) [U2C8-EVA only]

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIFD_REFCLK: Buffer type = TTL

Table 3.69 External Reference Clock Input/Output Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
External Reference Clock Input frequency	f_{REFCKI}		20		20	MHz
External Reference Clock Input duty cycle	DCREFCKI		35		65	%

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- HSIFD_TXDP, HSIFD_TXDN: CL = 5.0 pF

Table 3.70 RHSIF Transmit Data Timing (Debug)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmit data cycle	f_{TX}	Fast mode			320	M Baud

Table 3.71 RHSIF Receipt Data Timing (Debug)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Receipt data cycle	f_{RX}	Fast mode			320	M Baud

3.3.19 CXPI Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4
- Buffer type = SHMT1

Table 3.72 CXPI Timing (CXPI-PWM Mode, Master node)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CXPI transfer rate	r_{CXPI}				20	kbps
CXPI cycle time	Tbit		50			µs
Required loop back delay time (from CXP1nTX to CXP1nRX)	t_{pwm_loop}				0.05 × Tbit	µs

Table 3.73 CXPI Timing (CXPI-PWM Mode, Slave node)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CXPI transfer rate	r_{CXPI}				20	kbps
CXPI cycle time	Tbit		50			µs
CXP1nTX output delay time (from CXP1nRX)	$t_{tx\_0\_pd}$		4 × t_{PCLK} *1		511 × t_{PCLK} + 4 × t_{PCLK} + 0.1 *1,*2	µs
Required loop back delay time (from CXP1nTX to CXP1nRX)	t_{pwm_loop}				0.05 × Tbit	µs

Note 1. t_{PCLK} is period of CLK_HSB

Note 2. "511 × t_{PCLK}" means maximum surge noise filter time. For details, see the RH850/U2C Group User's Manual: Hardware Section 30.4.1.6, CXP1nFIL — CXPI Input Filter Setting Register

Table 3.74 CXPI Timing (CXPI-NRZ Mode, Master or Slave node)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CXPI transfer rate	r_{CXPI}				20	kbps
CXPI cycle time	Tbit		50			µs
Required loop back delay time (from CXP1nTX to CXP1nRX)	t_{nrz_loop}		1 × Tbit		4 × Tbit	µs

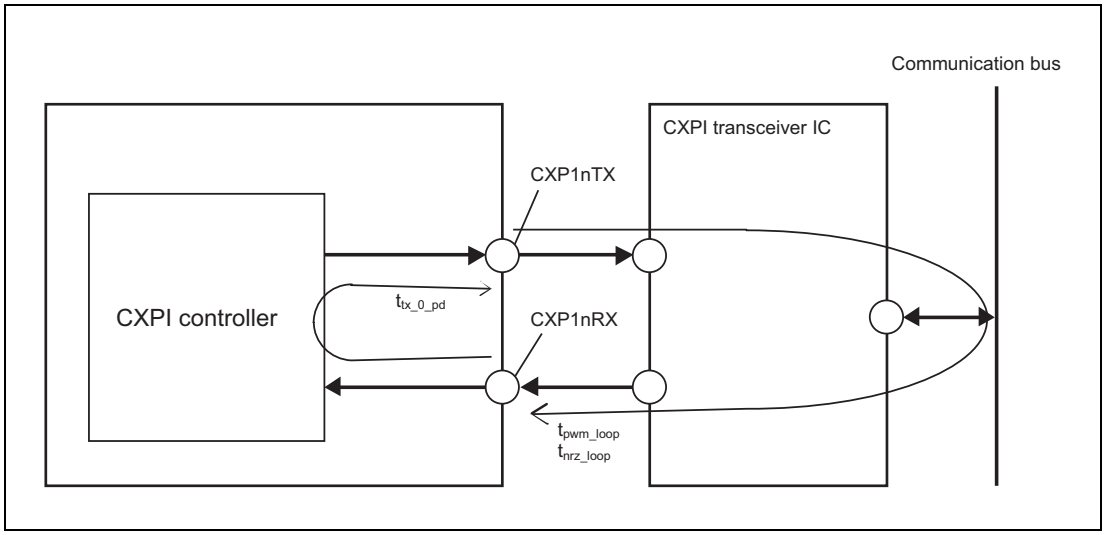


Figure 3.53 CXPI Block Diagram and Timing Path

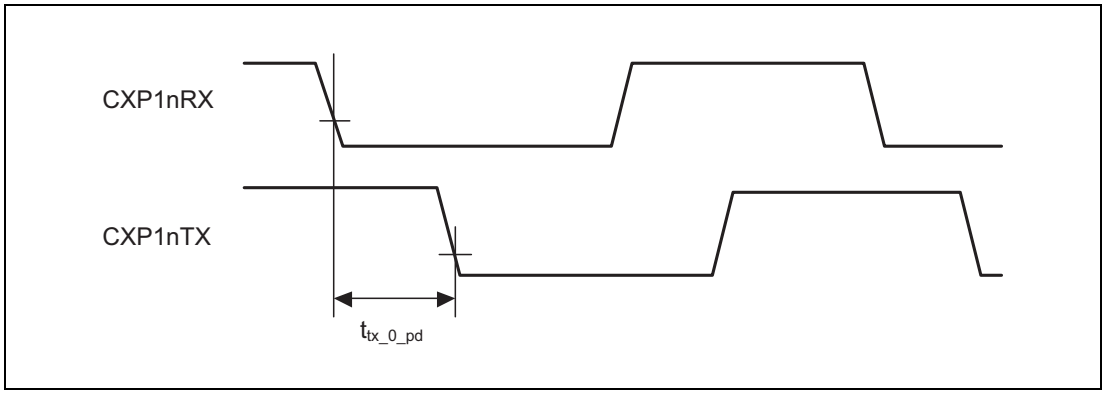


Figure 3.54 $t_{tx\_0\_pd}$ Waveform in CXPI PWM Mode

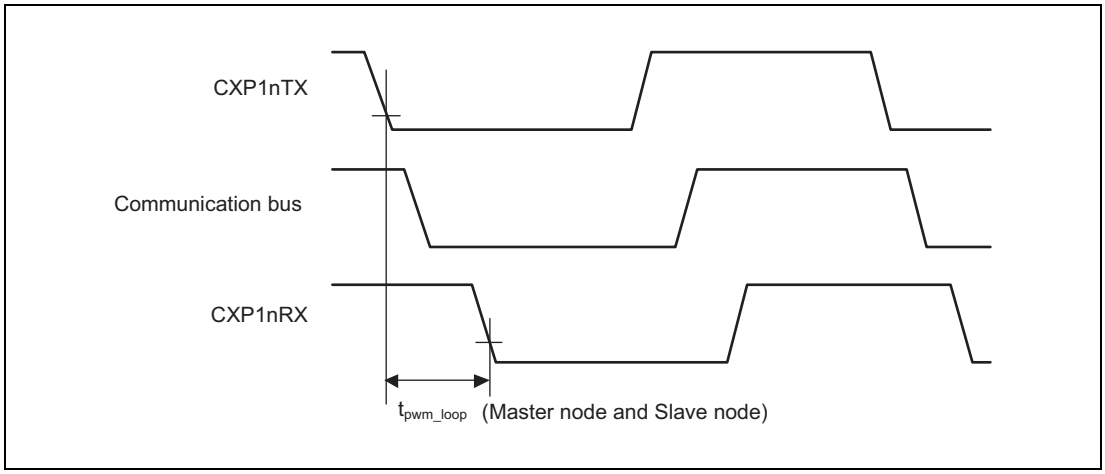


Figure 3.55 t_{pwm_loop} Waveform in CXPI PWM Mode

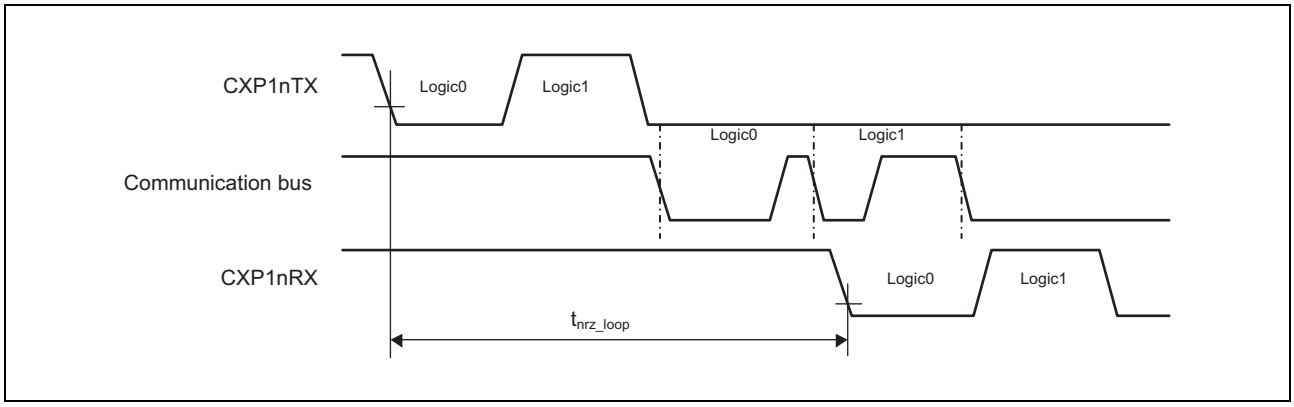


Figure 3.56 t_{nrz_loop} Waveform in CXPI NRZ Mode

3.3.20 Ethernet Timing

3.3.20.1 MII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Buffer type = TTL

Table 3.75 Ethernet Timing – 10 Mbit/s MII Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	t_{MTC}		400 – 100 ppm	400	400 + 100 ppm	ns
ETHn_MII_TX_CLK high width	t_{MTCH}	*1	140	200	260	ns
ETHn_MII_TX_CLK low width	t_{MTCL}	*1	140	200	260	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		0		25	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		0		25	ns
ETHn_MII_RX_CLK width	t_{MRC}		400 – 100 ppm	400	400 + 100 ppm	ns
ETHn_MII_RX_CLK high width	t_{MRCH}	*1	140	200	260	ns
ETHn_MII_RX_CLK low width	t_{MRCL}	*1	140	200	260	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		10			ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		10			ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Cload = 15 pF
- Drive strength = 2
- Buffer type = TTL

Table 3.76 Ethernet Timing – 100 Mbit/s MII Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	t_{MTC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETHn_MII_TX_CLK high width	t_{MTCH}	*1	14	20	26	ns
ETHn_MII_TX_CLK low width	t_{MTCL}	*1	14	20	26	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		0		25	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		0		25	ns
ETHn_MII_RX_CLK width	t_{MRC}		40 – 100 ppm	40	40 + 100 ppm	ns
ETHn_MII_RX_CLK high width	t_{MRCH}	*1	14	20	26	ns
ETHn_MII_RX_CLK low width	t_{MRCL}	*1	14	20	26	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		10			ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		10			ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65%inclusive (IEEE802.3).

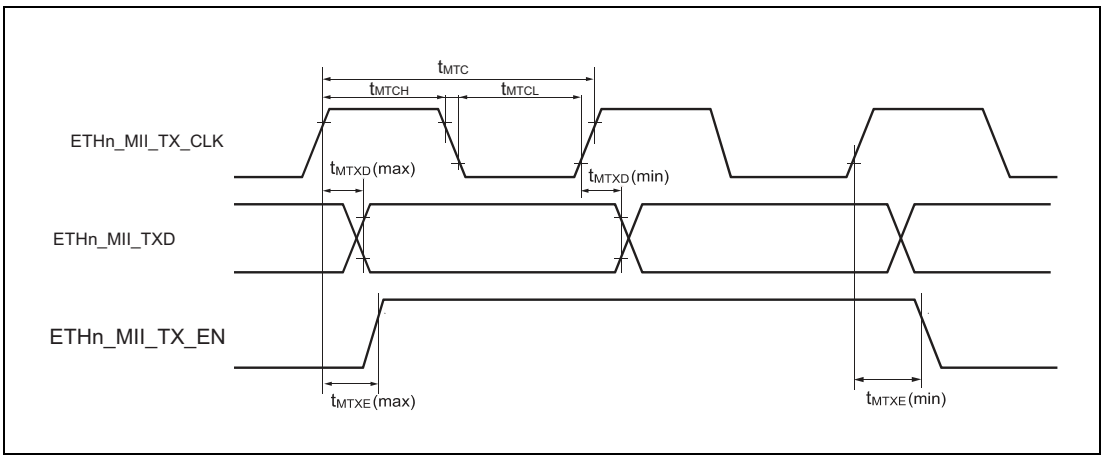


Figure 3.57 Ethernet Timing – MII Transmitter

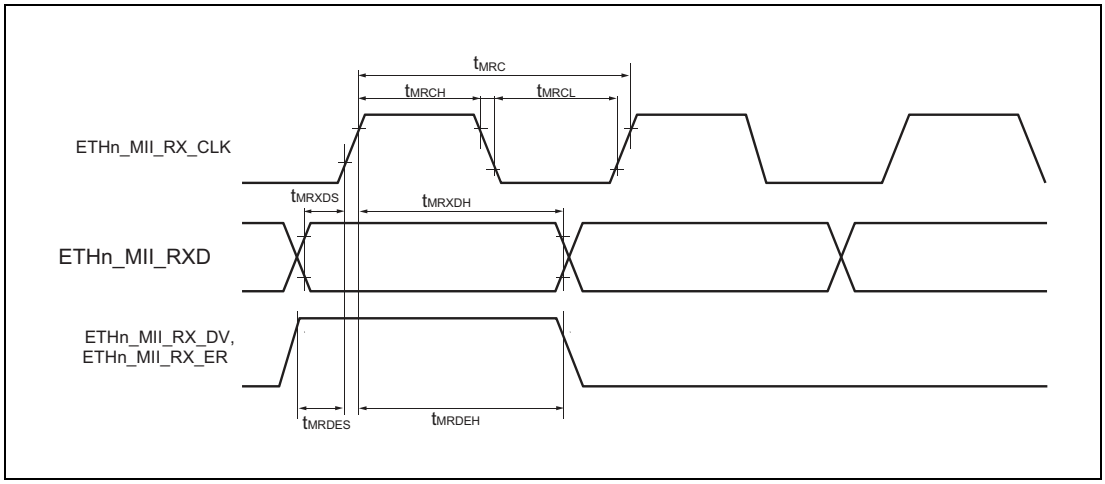


Figure 3.58 Ether net Timing – MII Receiver

3.3.20.2 Reverse-PHY MII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Drive strength = 2 (High)
- Buffer type = TTL

Table 3.77 10 Mbit/s MII (Reverse MII MAC mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	t_{MTC}		400 - 1%		400 + 1%	ns
ETHn_MII_TX_CLK high level width	t_{MTCH}	*1	140		260	ns
ETHn_MII_TX_CLK low level width	t_{MTCL}	*1	140		260	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		0		20	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		0		20	ns
ETHn_MII_RX_CLK width	t_{MRC}		400 - 1%		400 + 1%	ns
ETHn_MII_RX_CLK high level width	t_{MRCH}	*1	140		260	ns
ETHn_MII_RX_CLK low level width	t_{MRCL}	*1	140		260	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		10			ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		10			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		10			ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Table 3.78 10 Mbit/s MII (Reverse MII PHY mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) width	t_{MTC}		400 - 1%		400 + 1%	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) high level width	t_{MTCH}	*1, *2	140		260	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) low level width	t_{MTCL}	*1, *2	140		260	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		10		28	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		10		28	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) width	t_{MRC}		400 - 1%		400 + 1%	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) high level width	t_{MRCH}	*1, *2	140		260	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) low level width	t_{MRCL}	*1, *2	140		260	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		18			ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		0			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		18			ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		0			ns

Note 1. The duty cycle of ETHn_MII_TX_CLK and ETHn_MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Note 2. When Reverse MII PHY mode, ETHn_MII_TX_CLK and ETHn_MII_RX_CLK all are ETHn_RevMII_CLK pin

Table 3.79 100 Mbit/s MII (Reverse MII MAC mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK width	t_{MTC}		40 - 1%		40 + 1%	ns
ETHn_MII_TX_CLK high level width	t_{MTCH}	*1	14		26	ns
ETHn_MII_TX_CLK low level width	t_{MTCL}	*1	14		26	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		0		20	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		0		20	ns
ETHn_MII_RX_CLK width	t_{MRC}		40 - 1%		40 + 1%	ns
ETHn_MII_RX_CLK high level width	t_{MRCH}	*1	14		26	ns
ETHn_MII_RX_CLK low level width	t_{MRCL}	*1	14		26	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		10		-	ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		10		-	ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		10		-	ns
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		10		-	ns

Note 1. The duty cycle of MII_TX_CLK and MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Table 3.80 100 Mbit/s MII (Reverse MII PHY mode)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) width	t_{MTC}		40 - 1%		40 + 1%	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) high level width	t_{MTCH}	*1, *2	14		26	ns
ETHn_MII_TX_CLK(ETHn_RevMII_CLK) low level width	t_{MTCL}	*1, *2	14		26	ns
ETHn_MII_TXD [3:0] delay time	t_{MTXD}		10		28	ns
ETHn_MII_TX_EN delay time	t_{MTXE}		10		28	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) width	t_{MRC}		40 - 1%		40 + 1%	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) high level width	t_{MRCH}	*1, *2	14		26	ns
ETHn_MII_RX_CLK(ETHn_RevMII_CLK) low level width	t_{MRCL}	*1, *2	14		26	ns
ETHn_MII_RXD [3:0] setup time	t_{MRXDS}		18		-	ns
ETHn_MII_RXD [3:0] hold time	t_{MRXDH}		0		-	
ETHn_MII_RX_DV, ETHn_MII_RX_ER setup time	t_{MRDES}		18		-	
ETHn_MII_RX_DV, ETHn_MII_RX_ER hold time	t_{MRDEH}		0		-	

Note 1. The duty cycle of ETHn_MII_TX_CLK and ETHn_MII_RX_CLK shall be between 35 to 65% inclusive (IEEE802.3).

Note 2. When Reverse MII PHY mode, ETHn_MII_TX_CLK and ETHn_MII_RX_CLK all are ETHn_RevMII_CLK pin

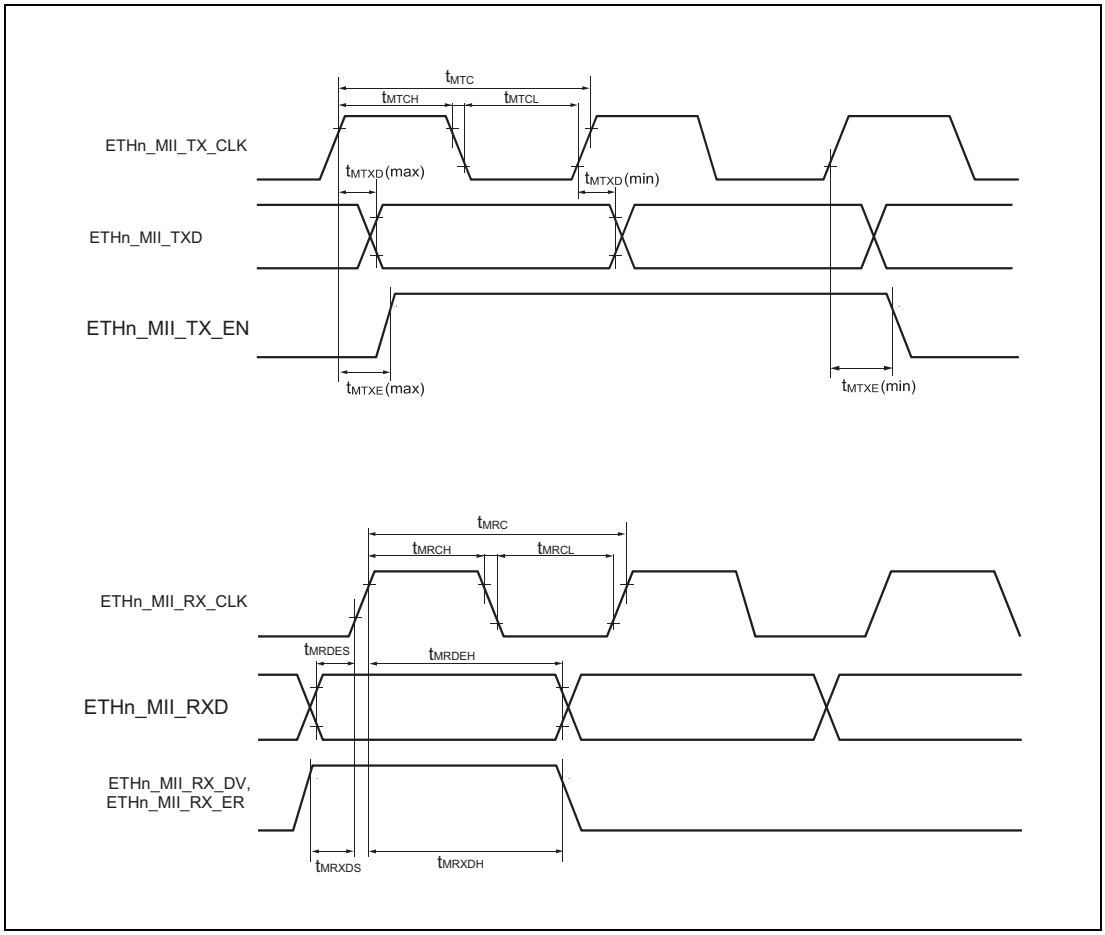


Figure 3.59 Ethernet Timing – Reverse-PHY MII

3.3.20.3 RMII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Drive strength = 2 (High)
- Buffer type = TTL

Table 3.81 Ethernet Timing – RMII Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ETNCnREF50CK width	t_{RMC}		20 – 50 ppm	20	20 + 50 ppm	ns
ETNCnREF50CK high width	t_{RMCH}	*1, *2	7		13	ns
ETNCnREF50CK low width	t_{RMCL}	*1, *2	7		13	ns
ETHn_RMII_RXD [1:0], ETHn_RMII_RX_DV and ETHn_RMII_RX_ER setup time	t_{RMS}		4			ns
ETHn_RMII_RXD [1:0], ETHn_RMII_RX_DV and ETHn_RMII_RX_ER hold time	t_{RMH}		2			ns
ETHn_RMII_TXD [1:0], ETHn_RMII_TX_EN output delay time	t_{RMD}		2		16	ns

Note 1. The duty cycle of ETNC0REF50CK shall be between 35 to 65% inclusive (RMIITM specification).
Note 2. ETNCnREF50CK is same with ETHn_MII_TX_CLK pin in RMII mode

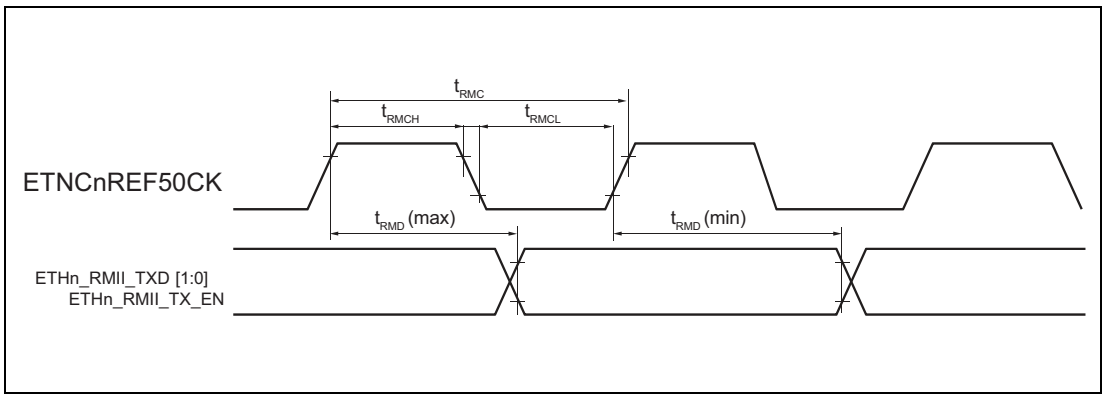


Figure 3.60 Ethernet Timing – RMII Transmitter

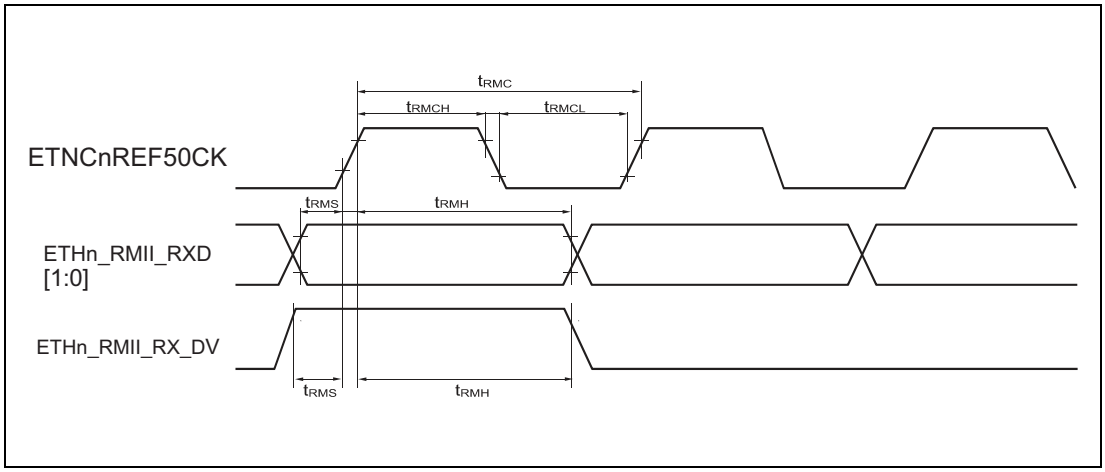


Figure 3.61 Ethernet Timing – RMII Receiver

3.3.20.4 SGMII Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition***2.

Table 3.82 Ethernet Timing – SGMII REFCK Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock input frequency	t_{CIF}	MainOSC frequency Crystal (for SGMII) = 20MHz	50 – 100 ppm		50 + 100 ppm	ns
Clock input duty cycle	t_{CIDC}		45		55	%
Clock input rising/falling time (20%-80%)	t_{CIRFT}	MainOSC frequency Crystal (for SGMII) = 20MHz			3	ns
Clock Input Total jitter (Dj+ 14* rms Random jitter)	t_{CITJ}				73*1	ps peak to peak

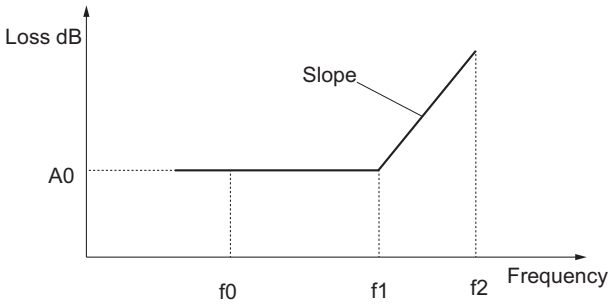
Note 1. 12 kHz to 20 MHz rms jittrer = 3ps.

Note 2. No CL defenition in this chapter.

Table 3.83 Ethernet Timing – SGMII Tx buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Signaling speed	t_{SS}		1.25 – 100 ppm		1.25 + 100 ppm	GBd
Total output jitter (Dj+14*rms random jitter)	t_{TOJ}				300	ps peak to peak
VOD rise/fall time (20% - 80%)	t_{VRFT}		60		250	ps
Differential output return loss (min)	DORL				*1	dB

Note 1. See the **Figure 3.62, Differential output return loss** for the detail of differential output return loss.



Parameter value		Unit
A0	-8	dB
f0	50	MHz
f1	0.625	GHz
f2	1.25	GHz
Slope	10	dB/dec

Figure 3.62 Differential output return loss

Table 3.84 Ethernet Timing – SGMII Rx buffer Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Signaling speed	t_{SS}		1.25 – 100 ppm		1.25 + 100 ppm	GBd
Total input jitter tolerance (Dj+14*rms random jitter)	t_{TIJT}				400	ps peak to peak

Table 3.85 Ethernet Timing – Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SGMII power stabilization time	t_{SPST}				1.2	ms

3.3.20.5 Management Interface

Timing of management interface (ETHn_MDC and ETHn_MDIO) depends on software. It is necessary to adjust wait time according to AC specification of PHY.

3.3.21 Ethernet 10BASE-T1S Timing

3.3.21.1 T1S Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- CL = 15 pF
- Buffer type = TTL

Table 3.86 T1S Timing – Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TX low pulse duration	t_{TXPL}			20		ns
TX high pulse duration	t_{TXPH}			20		ns
ED low width	t_{EDL}	*1	15			ns
		*2	8			ns
RX low width	t_{RXL}		6			ns
RX high width	t_{RXH}		6			ns

Note 1. ETNFnT1SCTL0.PMA_CFG = 1
Note 2. ETNFnT1SCTL0.PMA_CFG = 0

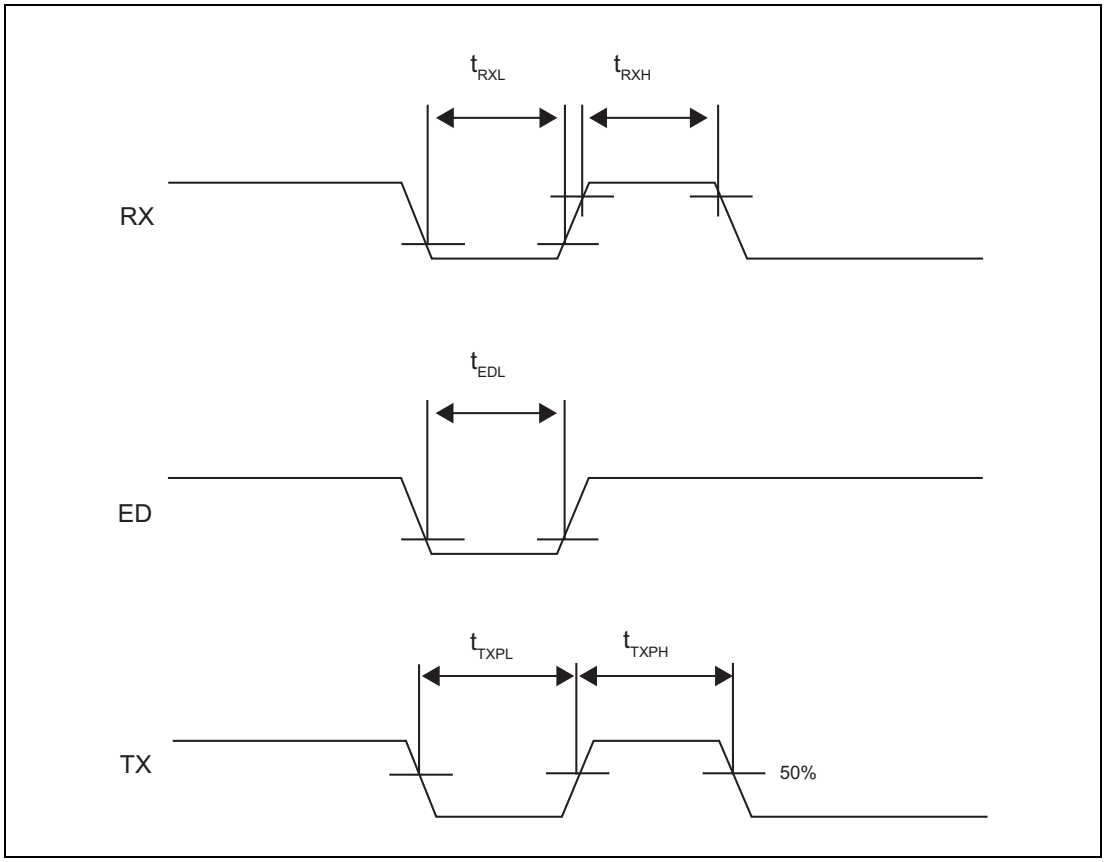


Figure 3.63 T1S Timing

3.3.21.2 RMII timing

Refer to **Section 3.3.20.3, RMII Characteristics**

Note: Refer to the following correspondence table for signal names.

Table 3.87 RMII correspondence signal name

ETNF RMII signal name	ETND RMII signal name
ETNFn_RMII_REFCLK	ETNDnREF50CK
ETNFn_RMII_TXD	ETHn_RMII_TXD
ETNFn_RMII_TXEN	ETHn_RMII_TX_EN
ETNFn_RMII_RXD	ETHn_RMII_RXD
ETNFn_RMII_CRSDV	ETHn_RMII_RX_DV

3.3.22 PSI5 Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive strength = 4 (Low)
- Buffer type = SHMT1

Table 3.88 PSI5 Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Bit time		125 kbps (Low speed)	7.6	8.0	8.4	µs
		189 kbps (High speed)	5.0	5.3	5.6	µs
		250 kbps (PAS compatibility)	3.8	4.0	4.2	µs
Gap time		125 kbps (Low speed)	8.4			µs
		189 kbps (High speed)	5.6			µs
		250 kbps (PAS compatibility)	2.0			µs

3.3.23 PSI5S Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.89 PSI5S Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PSI5S transfer rate	r_{PSI5S1}	PSI5S mode			5.33	Mbps
	r_{PSI5S2}	UART mode			5.33	Mbps
Output clock cycle	$t_{PSIScyc}$	PSI5S mode	37.5			ns
Output clock pulse width	$t_{PSISCKW}$	PSI5S mode	0.3 × $t_{PSIScyc}$		0.5 × $t_{PSIScyc}$	ns

NOTE

This AC characteristics is limited to specific pin groups. For details, please refer to Appendix file *"Limited_conditions_for_AC_specification.xlsx"*.

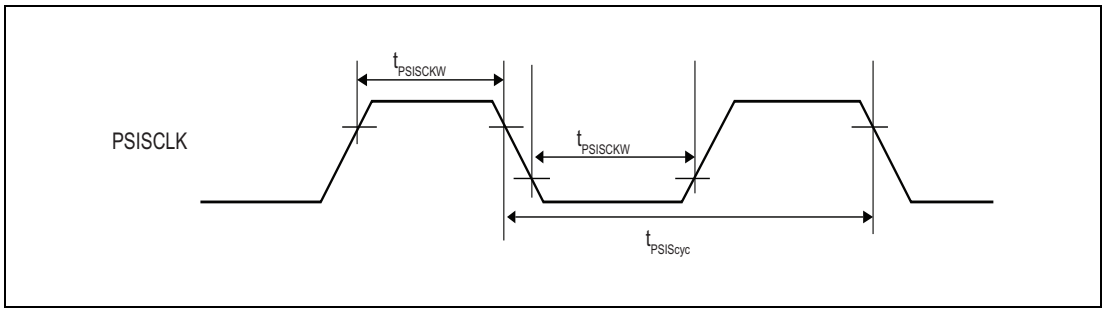


Figure 3.64 PSI5S Clock Output Timing

3.3.24 SSIF Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = SHMT1

Table 3.90 Audio Clock Input Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
AUDIO_CLK period	t_{ACKI}	DNF used	100		1000	ns
		DNF not used	20		1000	ns
AUDIO_CLK high width	t_{ACKH}	DNF used	0.45 × t_{ACKI}		0.55 × t_{ACKI}	ns
		DNF not used*1	0.45 × t_{ACKI}		0.55 × t_{ACKI}	ns
		DNF not used*2	0.50 × t_{ACKI} - 3			ns
AUDIO_CLK low width	t_{ACKL}	DNF used	0.45 × t_{ACKI}		0.55 × t_{ACKI}	ns
		DNF not used*1	0.45 × t_{ACKI}		0.55 × t_{ACKI}	ns
		DNF not used*2	0.50 × t_{ACKI} - 3			ns

Note 1. When AUDIO_CLK period (t_{ACKI}) is more than 80 ns
Note 2. When AUDIO_CLK period (t_{ACKI}) is up to 80 ns

Table 3.91 I2S Master Mode Interface Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SSIBCK output cycle time	t_{MO}	DNF used	200		64000	ns
		DNF not used	80		64000	ns
SSIBCK output high width	t_{MHC}		0.35 × t_{MO}		0.65 × t_{MO}	ns
SSIBCK output low width	t_{MLC}		0.35 × t_{MO}		0.65 × t_{MO}	ns
SSITxD, SSILRCK/SSIFS output delay time	t_{DTR}				30	ns
SSITxD, SSILRCK/SSIFS output hold time	t_{HTR}		0			ns
SSIRxD input setup time	t_{SR}	DNF used	25 + t_{DNFDD}			ns
		DNF not used	25			ns
SSIRxD input hold time	t_{HR}	DNF used	25 + t_{DNFDD}			ns
		DNF not used	25			ns

Table 3.92 I2S Slave Mode Interface Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SSIBCK input cycle time	t_{SO}	DNF used	200		64000	ns
		DNF not used	80		64000	ns
SSIBCK input high width	t_{SHC}		0.35 × t_{SO}		0.65 × t_{SO}	ns
SSIBCK input low width	t_{SLC}		0.35 × t_{SO}		0.65 × t_{SO}	ns
SSITxD output delay time	t_{DTR}	DNF used			30 + t_{DNFDD}	ns
		DNF not used			30	ns
SSITxD output hold time	t_{HTR}	DNF used	0			ns
		DNF not used	0			ns
SSIRxD input setup time SSILRCK/SSIFS input setup time	t_{SR}	DNF used	25 + t_{DNFDD}			ns
		DNF not used	25			ns
SSIRxD input hold time SSILRCK/SSIF input hold time	t_{HR}	DNF used	25 + t_{DNFDD}			ns
		DNF not used	25			ns
SSILRCK/SSIFS to TxD delay time	t_{DTC}	DNF used			40 + t_{DNFDD}	ns
		DNF not used			40	ns

$t_{DNFDD} = (S + 2) \times 1/fs + 5 \times 1/f_{SSIF}$

S: Number of sampling times (only 2 can be set)

fs: The value given by following formula

$fs = f_{DNFCK} / PRS$

f_{DNFCK}: frequency of CLKC_HSB

PRS: 1,2,4,8, …,128 (only 1 can be set)

f_{SSIF}: frequency of CLK_HSB_SSIF

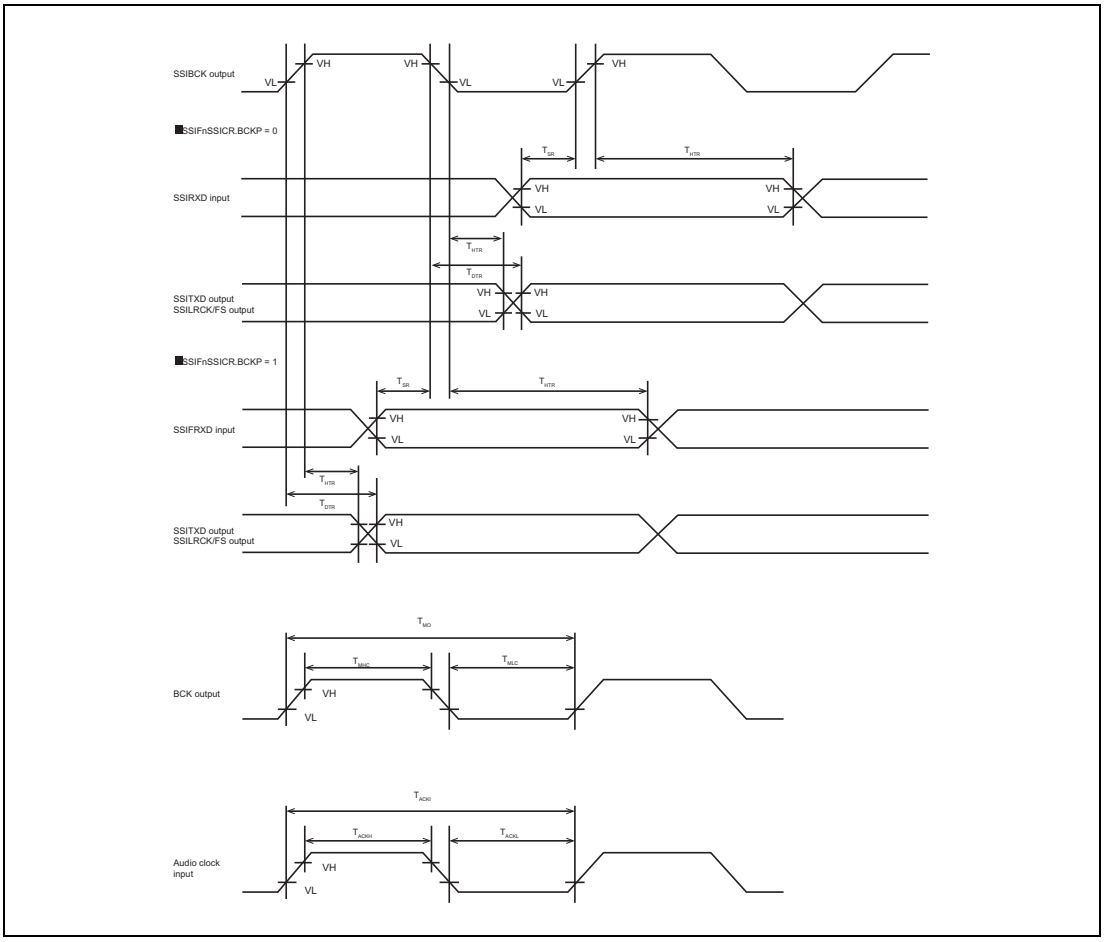


Figure 3.65 I2S Master Mode Interface timing

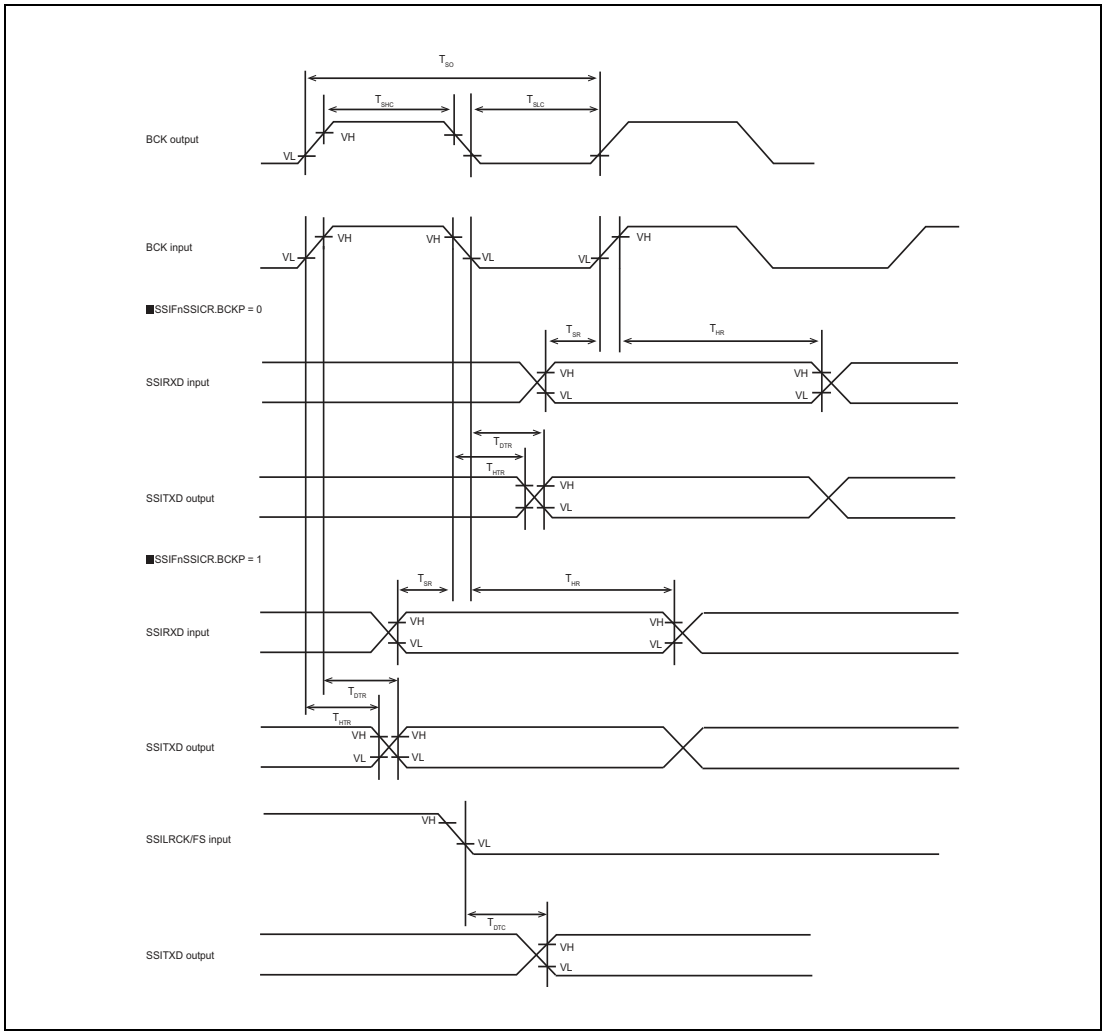


Figure 3.66 I2S Slave Mode Interface timing

3.3.25 Timer Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.93 Timer Input Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t_{WTDIH}		S × 1/fs[*1]			ns
TAUDnIm input low level width	t_{WTDIL}		S × 1/fs[*1]			ns
TAUDnIm pulse rejection width[*2]	t_{WTDRJ}		(S – 1) × 1/fs[*1]		S × 1/fs[*1]	ns
TAUJnIm input high level width	t_{WTJIH}	Analog noise filter	600[*3]			ns
		Digital noise filter	S × 1/fs[*1]			ns
TAUJnIm input low level width	t_{WTJIL}	Analog noise filter	600[*3]			ns
		Digital noise filter	S × 1/fs[*1]			ns
TAUJnIm pulse rejection width[*2]	t_{WTJRJ}	Analog noise filter	100		600[*3]	ns
		Digital noise filter	(S – 1) × 1/fs[*1]		S × 1/fs[*1]	ns
TAPAnESO input high level width[*4]	t_{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	S × 1/fs[*1]			ns
TAPAnESO input low level width[*4]	t_{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	S × 1/fs[*1]			ns
TAPAnESO pulse rejection width[*2, *4]	t_{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	(S – 1) × 1/fs[*1]		S × 1/fs[*1]	ns
ENCAnTINm input high level width	t_{WENIH}		S × 1/fs[*1]			ns
ENCAnTINm input low level width	t_{WENIL}		S × 1/fs[*1]			ns
ENCAnTINm pulse rejection width[*2]	t_{WENRJ}		(S – 1) × 1/fs[*1]		S × 1/fs[*1]	ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI high level width	t_{WTGIH}		S × 1/fs[*1]			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI low level width	t_{WTGIL}		S × 1/fs[*1]			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI pulse rejection width[*2]	t_{WTGRJ}		(S – 1) × 1/fs[*1]		S × 1/fs[*1]	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLKC_HSB (others)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not.
This characteristic is not tested in production.

Note 3. When CLK_LSOSC is selected by CKS_ATAUJC register, at least one clock period of CLK_LSOSC (4.6 µs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 µs width may be rejected.

Note 4. By-pass of filter is possible. For detail, see the RH850/U2C Group User's Manual: Hardware Section 2.7.2.11, ANF/DNF Type F1.

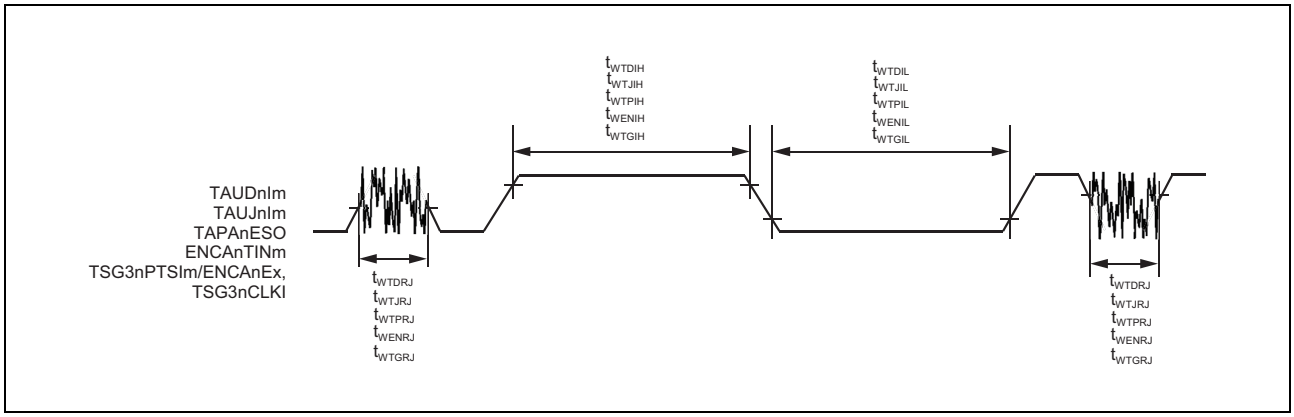


Figure 3.67 Timer Input Timing

3.3.26 GTM Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.94 GTM Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
GTM input high level width	t_{WGTIH}		4 × Tsamp*1			ns
GTM input low level width	t_{WGTIL}		4 × Tsamp*1			ns
GTM output cycle time	t_{CYGTO}		25			ns
GTMECLKn output cycle	$t_{CYGTECLK}$		25			ns
GTMECLKn output high level width	t_{WGTOH}	Z / N*2*3: Integer value	$t_{CYGTECLK}$ / 2 – 4			ns
		Z / N*2*3: Indivisible value	$t_{CYGTECLK}$ / 2 × (2Z / N – 1) / (2Z / N) – 4			ns
GTMECLKn output low level width	t_{WGTOL}	Z / N*2*3: Integer value	$t_{CYGTECLK}$ / 2 – 4			ns
		Z / N*2*3: Indivisible value	$t_{CYGTECLK}$ / 2 × (2Z / N – 1) / (2Z / N) – 4			ns

Note 1. Tsamp = $1/f_{CLK\_GTM}$

Note 2. "Z" is the value of "Numerator for external clock divider" by CMU_ECLK_[z]_NUM register.

Note 3. "N" is the value of "Denominator for external clock divider" by CMU_ECLK_[z]_DEN register.

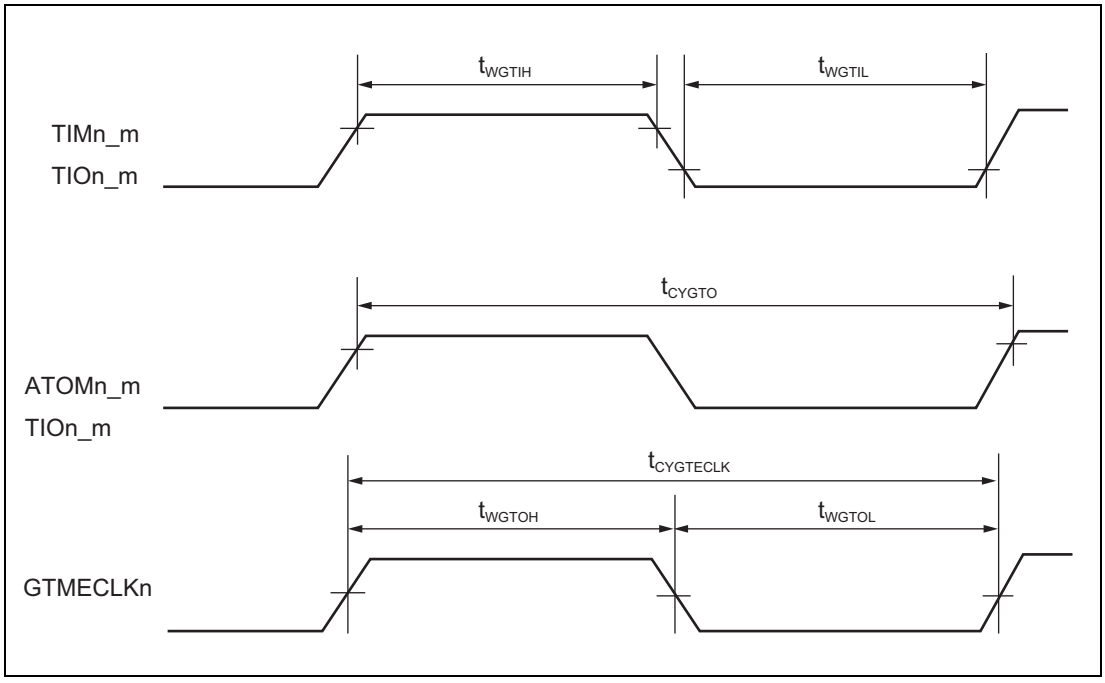


Figure 3.68 GTM Timing

3.3.27 Emergency shut-Off (ESO) Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.95 ESO Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ATOMn_m(N) Hi-z delay time	t_{DESO}				50	ns

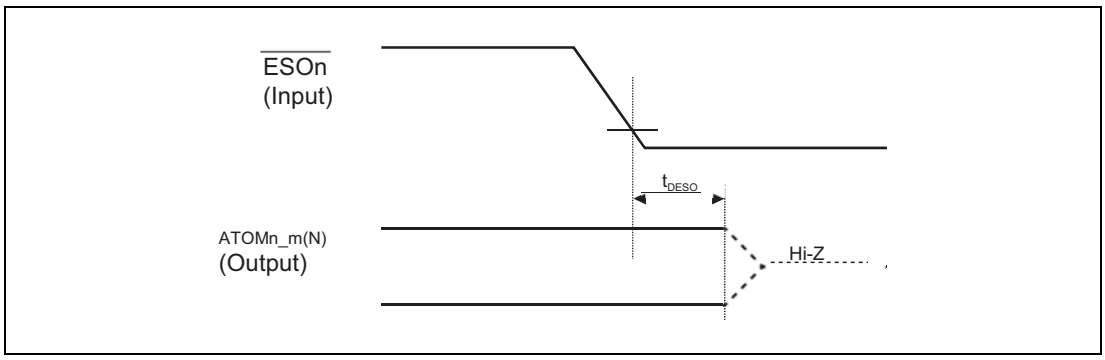


Figure 3.69 ESO Timing

3.3.28 Debug Reset Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.96 Debug Reset Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{TRST}}$ input low level width	t_{WTRL}		600			ns
$\overline{\text{TRST}}$ pulse rejection*1	t_{WTRRJ}		100		600	ns
Aurora reset hold time at emulation power-on	$t_{AURORESH}$		2.4	-	-	µs
Aurora reset noise cancel width	$t_{ARESNCW}$		0.2	-	1.2	µs
$\overline{\text{AURORES}}$ input low level width	t_{WARSL}		600			ns
$\overline{\text{AURORES}}$ pulse rejection width*1	t_{WARRJ}		100		600	ns

Note 1. Input pulses shorter than the given min. value will be filtered out (resulting in no interrupt detected). Input pulses between min. and max. value result in an undefined interrupt request signal condition (i.e. pulses might be filtered out or not).

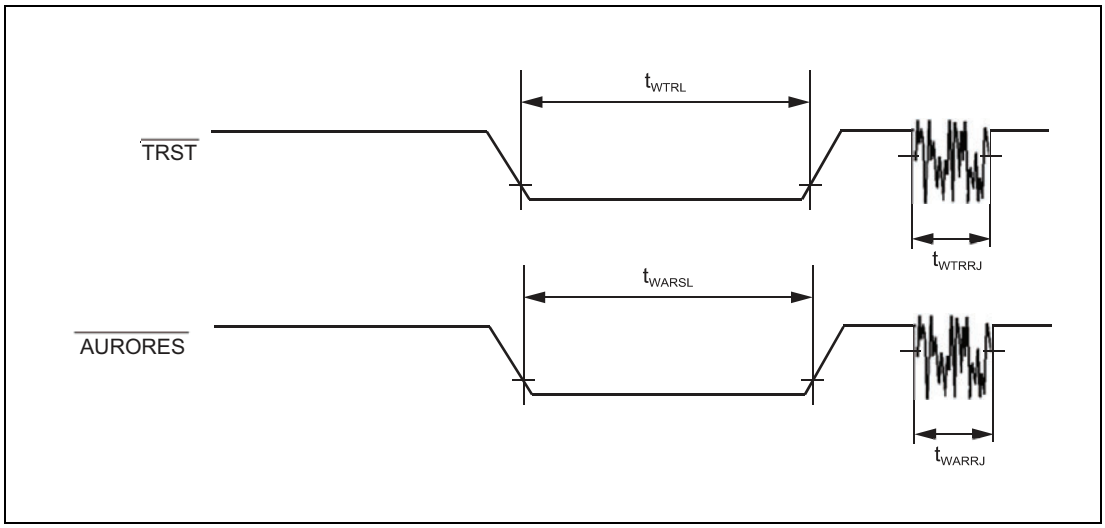


Figure 3.70 Debug Reset Timing

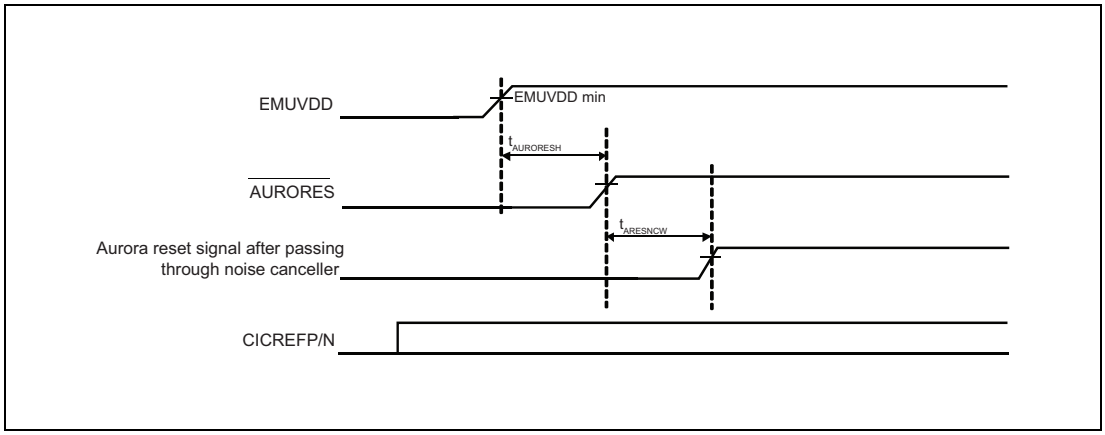


Figure 3.71 Aurora Reset Timing

3.3.29 Nexus Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive Strength = 2 (fast)
- Buffer type = TTL

Table 3.97 Nexus Interface Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK Cycle width	t_{TCKW}		25			ns
TCK high level width	t_{TCKWH}		10			ns
TCK low level width	t_{TCKWL}		10			ns
TMS/TDI setup time	t_{TISU}		6			ns
TMS/TDI hold time	t_{TIH}		6			ns
TDO output delay time	t_{TDOD}				14	ns
$\overline{RDY}$ delay time	t_{RDYD}				14	ns
TCK/$\overline{TRST}$/TMS/TDI input rising time	t_{TIR}				4	ns
TCK/$\overline{TRST}$/TMS/TDI input falling time	t_{TIF}				4	ns

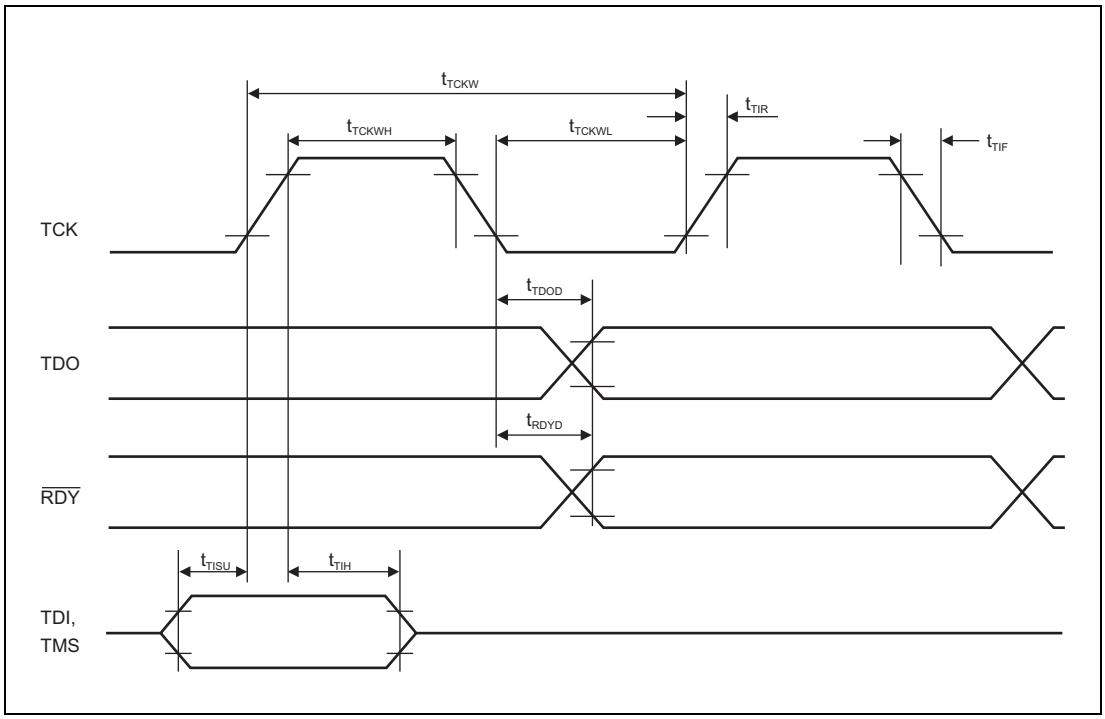


Figure 3.72 Nexus Interface Timing

3.3.30 LPD (4pin) Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Buffer type = TTL

Table 3.98 LPD (4pin) Interface Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLKI cycle time	$t_{LPDCKCYC}$		25			ns
LPDCLKI high/low level width	t_{LPDCKW}		4.5			ns
LPDCLKI input rising/falling time	$t_{LPDCKRF}$				8	ns
LPDI setup time	t_{LPDSU}		3			ns
LPDI hold time	t_{LPDH}		3			ns
LPDCLKO cycle time	$t_{LPDCKOCYC}$		25			ns
LPDCLKO high/low level width	$t_{LPDCKOW}$		t_{LPDCKW} - 2			ns
LPDCLKI to LPDCLKO delay time	$t_{LPDCKOD}$				44	ns
LPDO output delay	t_{LPDOD}		0		18	ns

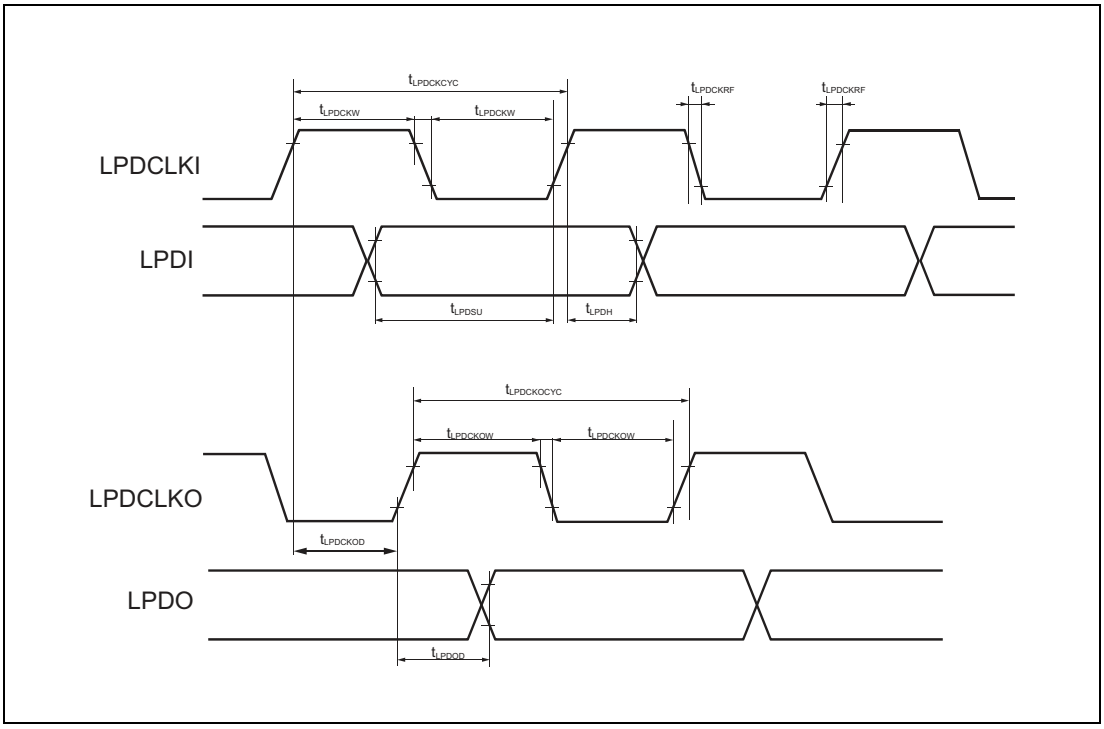


Figure 3.73 LPD (4pin) Interface Timing

3.3.31 BSCAN Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Drive Strength = 2 (fast)
- Buffer type = TTL

Table 3.99 BSCAN Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TCK (JP0_2) cycle width	t_{DCKW}		100			ns
TDI (JP0_0) setup time	t_{SDI}		12			ns
TDI (JP0_0) hold time	t_{HDI}		3			ns
TMS (JP0_3) setup time	t_{SMS}		12			ns
TMS (JP0_3) hold time	t_{HMS}		3			ns
TDO (JP0_1) delay time	t_{DDO}		0		30	ns

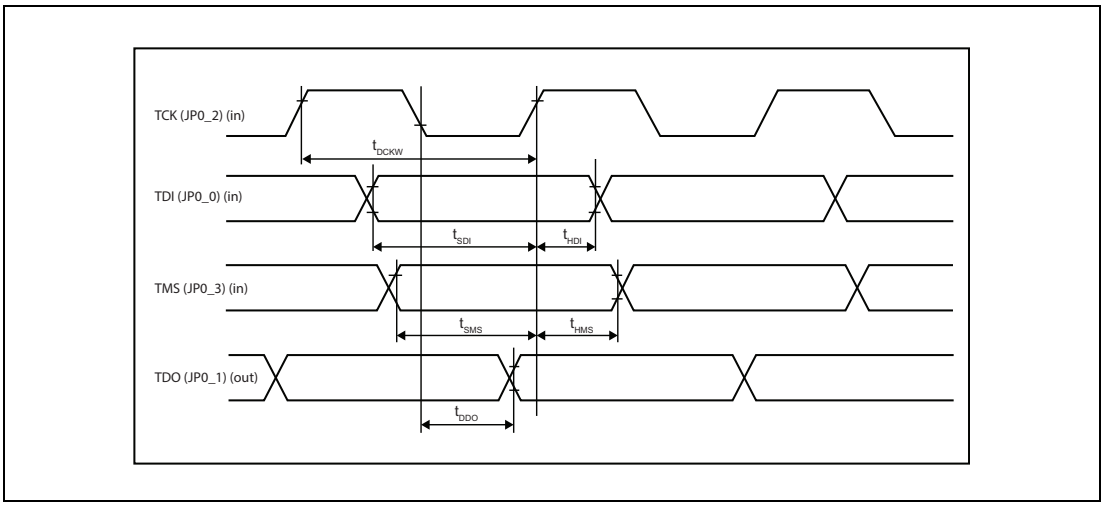


Figure 3.74 BSCAN Timing

3.3.32 Aurora Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

3.3.32.1 Aurora Interface — 1.25 Gbps baud rate

Table 3.100 Aurora Interface Operating Condition – 1.25Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	60			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			25	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	800		800	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.32.2 Aurora Interface — 2.5 Gbps baud rate

Table 3.101 Aurora Interface Operating Condition – 2.5Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise/Fall Time	t_{AITRF}	*1	40			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			20	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	400		400	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.32.3 Aurora Interface — 3.125 Gbps baud rate

Table 3.102 Aurora Interface Operating Condition – 3.125Gbps baud rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Rise / Fall Time	t_{AITRF}	*1	30			ps
Deterministic jitter	t_{AIDJ}				0.17	UI
Total jitter	t_{AITJ}				0.35	UI
Output skew	t_{AIOS}	*2			15	ps
Multiple output skew	t_{AIMOS}	*3			1000	ps
Unit interval	t_{AIUI}	± 100 ppm	320		320	ps

Note 1. At driver output.
Note 2. Skew at transmitter output between the differential pair.
Note 3. Skew at transmitter output between lanes of a multi-lane channel.

3.3.32.4 Aurora Interface — Transmitter clock Timing

Table 3.103 Aurora Interface Transmitter clock timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference clock frequency	f_{AICLK}	1.25 Gbps baud rate		62.5		MHz
		2.5 Gbps baud rate		125		MHz
		3.125 Gbps baud rate		156.25		MHz
Reference clock rise time	t_{AICTR}			200	400	ps
Reference clock fall time	t_{AICTF}			200	400	ps
Reference clock duty cycle			45		55	%
Reference clock total jitter	t_{AICTJ}	*1			40*2	ps
Stability	$t_{AICSTAB}$				50	ppm

Note 1. Peak to peak.

Note 2. Phase noise of CICREF[P/N] should be below the line of **Figure 3.75, Phase noise of CICREF[P/N]**.

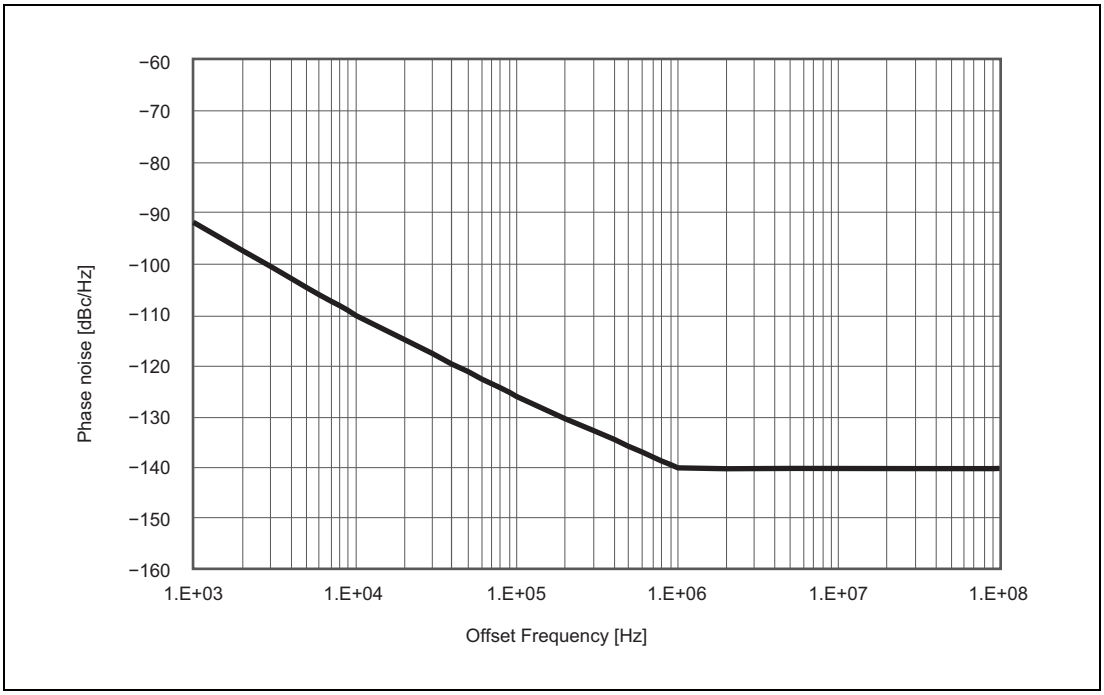


Figure 3.75 Phase noise of CICREF[P/N]

3.3.33 Debug Event Interface Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.104 Debug Event Interface Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{EVTI}}$ input high level width	t_{WEVIH}	*1	2 ×t_{MCKW} *3			ns
		*2	2 ×t_{TCKW}			ns
$\overline{\text{EVTI}}$ input low level width	t_{WEVIL}	*1	2 ×t_{MCKW} *3			ns
		*2	2 ×t_{TCKW}			ns
$\overline{\text{EVTO}}$ output high level width	t_{WEVOH}		t_{MCKW} *3			ns
$\overline{\text{EVTO}}$ output low level width	t_{WEVOL}		t_{MCKW} *3			ns
$\overline{\text{MSYN}}$ input high level width	t_{WMSNH}		2 ×t_{MCKW} *3			ns
$\overline{\text{MSYN}}$ input low level width	t_{WMSNL}		2 ×t_{MCKW} *3			ns

Note 1. When used as event trigger.

Note 2. When used as break input.

Note 3. t_{MCKW} is the cycle of the clock (MCKO) obtained by dividing the CPU clock (CLK_CPU) and the value must be divided by 16 (default). For details, refer to the *RH850/U2C Group User's Manual: Emulation*.

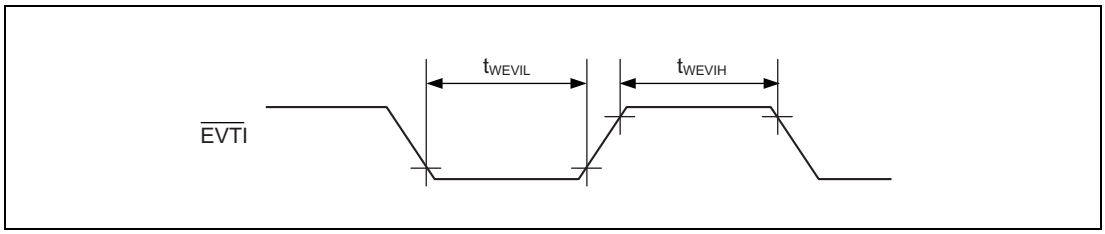


Figure 3.76 $\overline{\text{EVTI}}$ Timing

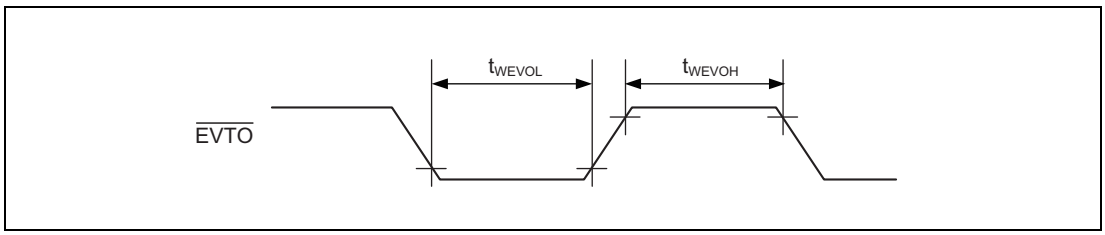


Figure 3.77 $\overline{\text{EVTO}}$ Timing

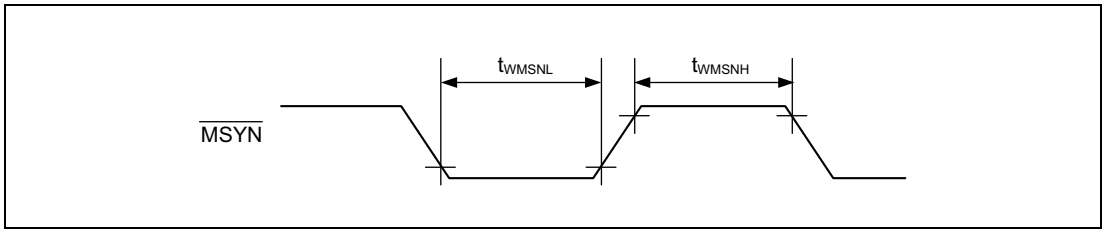


Figure 3.78 $\overline{\text{MSYN}}$ Timing

3.3.34 Debug Interface Mode Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.105 Debug Interface Mode Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TCK (JP0_2) input timing before $\overline{\text{TRST}}$	$t_{DBGIFSWCK}$		$10\times t_{LPDCKCYC}$ $10\times t_{TCKW}$			ns
TDI (JP0_0) setup time	$t_{DBGIFSWS}$		$10\times t_{LPDCKCYC}$ $10\times t_{TCKW}$			ns
TDI (JP0_0) hold time	$t_{DBGIFSWH}$		2			µs

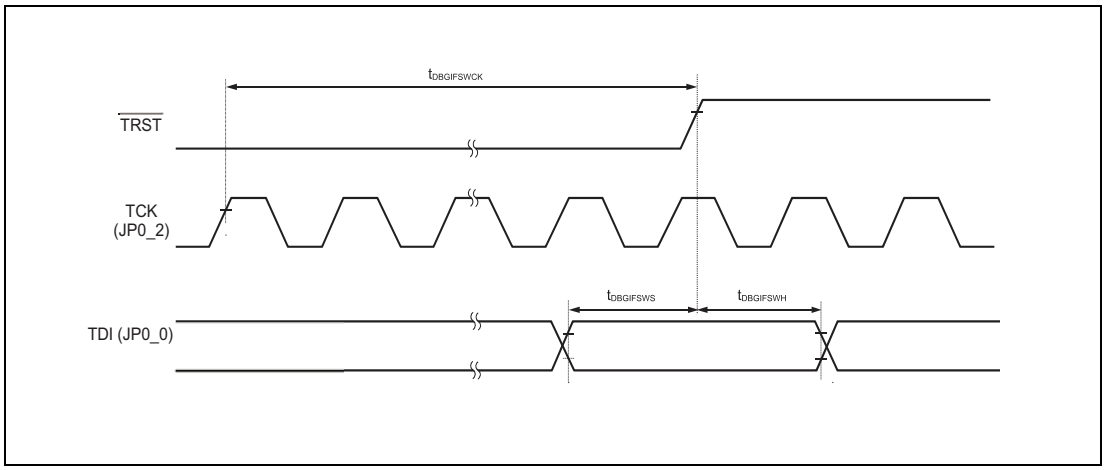


Figure 3.79 Debug Interface Mode Timing

3.3.35 Debug Wake-up Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.106 Debug wake-up timing

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
INTDCUTDI setup time	t_{IDCUS}		1			ms
INTDCUTDI hold time	t_{IDCUH}		3			ms

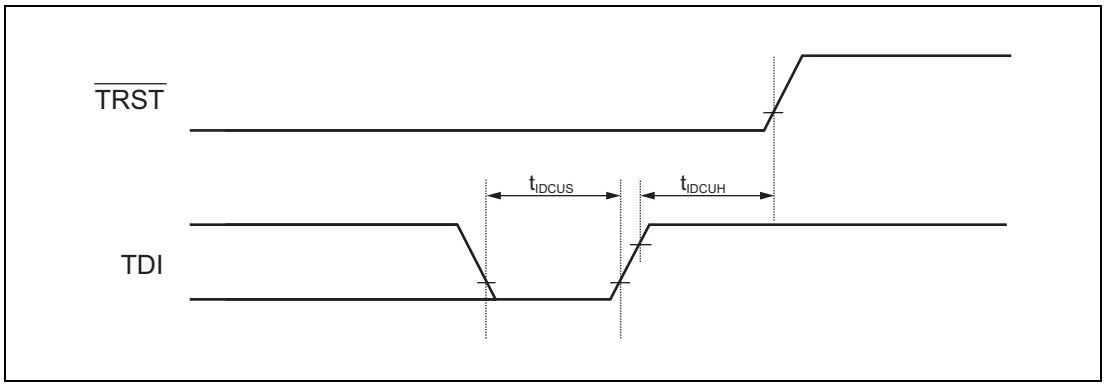


Figure 3.80 Debug wake-up timing

3.3.36 Flash Programming

3.3.36.1 Flash Programming Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.107 Flash Programming transfer rate

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Flash Programming transfer rate	r_{FP}	2-wired UART mode			2.5	Mbps
FPCK cycle time	t_{KCYSF}	3-wired Clock Sync mode	100*1			ns
FPCK high level width	t_{KWHSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 10			ns
FPCK low level width	t_{KWLSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 10			ns
FPDR setup time	t_{SSISF}	3-wired Clock Sync mode	2 × t_{FPcyc}*2			ns
FPDR hold time	t_{HSISF}	3-wired Clock Sync mode	2 × t_{FPcyc}*2			ns
FPDT output delay	t_{DSOSF}	3-wired Clock Sync mode	2 × t_{FPcyc}*2		3 × t_{FPcyc}*2 + 32	ns
FPDT hold time	t_{HSOSF}	3-wired clock sync mode	2 × t_{FPcyc}*2			ns

Note 1. Input the external clock data is more than or equal to 8 clocks of CLK_HSB.
Note 2. t_{FPcyc} is a period of CLK_HSB.

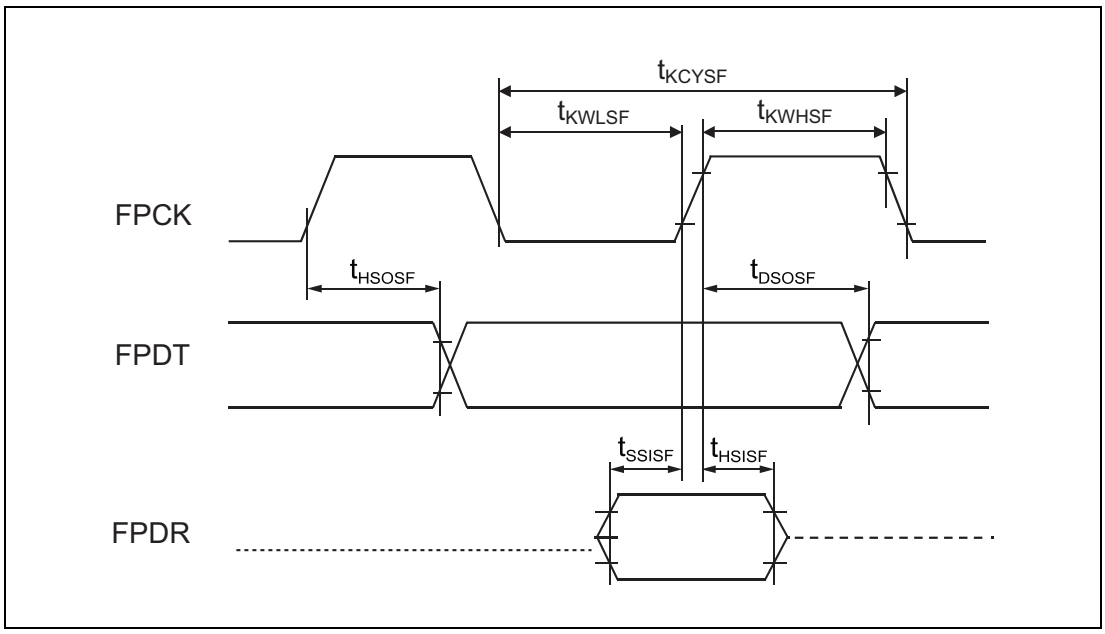


Figure 3.81 Flash Programming transfer rate

3.3.36.2 Serial Programming Setup Timing

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.108 Serial Programming Setup Timing

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{MD0IS}		2			ms
FLMD0 pulse input end time	t_{MD0IE}				100	ms
FLMD0 low/high level width	t_{MD0PWL} / t_{MD0PWH}		4			µs
FLMD0 rise time	t_{MD0R}				20	ns
FLMD0 fall time	t_{MD0F}				20	ns

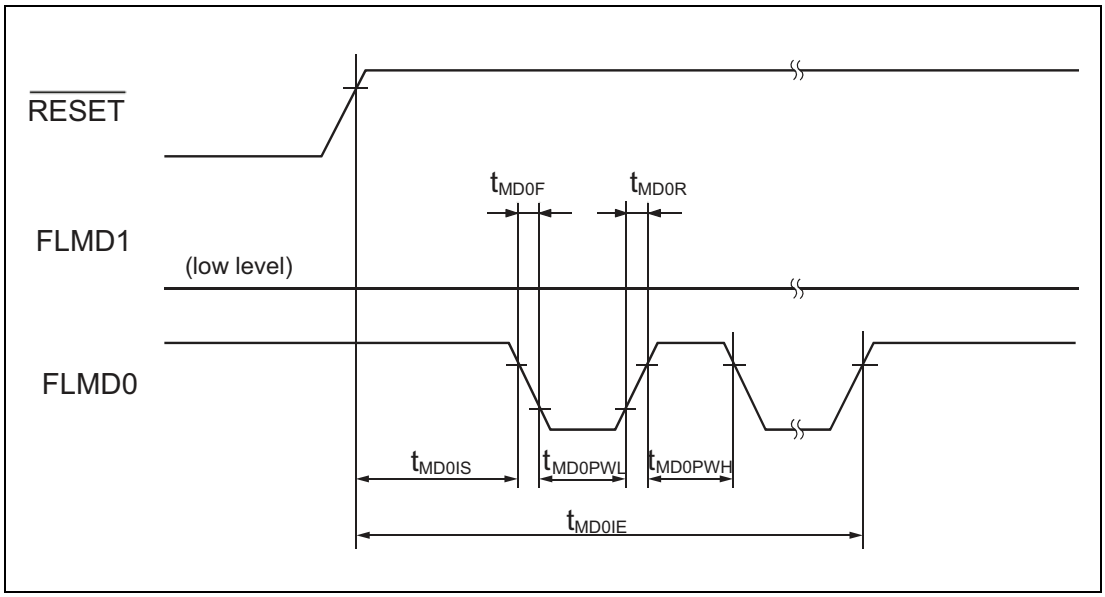


Figure 3.82 Flash Programming transfer rate

NOTE

For FLMD0 pulses, see the RH850/U2C Group User's Manual: Hardware Section 53.7.3, Selection of Flash Programming Interface.

3.4 A/D Converter Characteristics

3.4.1 SAR A/D Converter Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.109 ADC Characteristics (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RESn		10		12	bit
Analog supply voltages	AnVREFH		3.0		5.5	V
Analog input voltage	V_{IAN}	ADCKnIm (T&H not used)	AnVSS		AnVREFH	V
		ADCKnIm (T&H used)	0.2		AnVREFH – 0.2	V
		ADCKAImS (AAVREFH≧E0VCC)	AAVSS		E0VCC	V
		ADCK1ImS (A1VREFH≧E1VCC)	A1VSS		E1VCC	V
		ADCK2ImS (A2VREFH≧E2VCC)	A2VSS		E2VCC	V
Operation frequency	f_{ADCLK}	AWO	10*6		40	MHz
Operation frequency	f_{ADCLK}	ISO		40*1		MHz
Conversion time	t_{CONV}	t_{SPL} + t_{SAR}*2	1.0			µs
Sample time	t_{SPL}*2		0.45			µs
T&H sampling time	t_{THSMP}	In self-diagnosis	0.45			µs
		First conversion (including after self-diagnosis)	10			µs
		Other than above	0.45			µs
T&H hold time	t_{THHOLD}				10	µs
Slope of analog input voltage	t_{VSIAN}	T&H used	-5		5	kV/s
Total error*3	TOE	ADCKnIm (T&H not used)	–4.0		4.0	LSB
		ADCKnIm (Either T&H group A or group B used)	–6.0		6.0	LSB
		ADCKnIm (Both T&H group A and group B used)	–8.0		8.0	LSB
		ADCKnImS	–8.0		8.0	LSB
Integral non-liniarity error*4	ILE	ADCKnIm (T&H not used)	–2.0		2.0	LSB
		ADCKnIm (T&H used)	–3.0		3.0	LSB
		ADCKnImS	–6.0		6.0	LSB
Differential non-liniarity error*4	DLE	ADCKnIm (T&H not used)	–1.0		2.0	LSB
		ADCKnIm (T&H used)	–1.0		2.0	LSB
		ADCKnImS	–1.0		4.0	LSB
Offset error*4 (Zero scale error)	OSE	ADCKnIm (T&H not used)	–3.5		3.5	LSB
		ADCKnIm (T&H used)	–5.5		5.5	LSB
		ADCKnImS	–7.5		7.5	LSB

Table 3.109 ADC Characteristics (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Full-scale error*4	FSE	ADCKnIm (T&H not used)		–3.5		3.5	LSB
		ADCKnIm (T&H used)		–5.5		5.5	LSB
		ADCKnImS		–7.5		7.5	LSB
Pin self diagnosis				–40.0		40.0	LSB
AD core self-diagnosis Function				–8.0		8.0	LSB
Secondary power supply voltage monitor absolute error*5		for E0VCC, VCC		–16.0		16.0	LSB
		for AWOVDD, ISOVDD		–10.0		10.0	LSB
Pull-up resistor for wiring break detection	RPU	ADCKnIm pins	VIAN = AnVSS	10		34	kΩ
			VIAN = AnVREFH/2	5		22	kΩ
			VIAN = AnVREFH	3		16	kΩ
		ADCKnImS pins	VIAN = AnVSS	10		34	kΩ
			VIAN = EnVCC/2	5		22	kΩ
			VIAN = EnVCC	3		16	kΩ
Pull-down resistor for wiring break detection	RPD	ADCKnIm pins	VIAN = AnVSS	1.5		10	kΩ
			VIAN = AnVREFH/2	5		19	kΩ
			VIAN = AnVREFH	10		34	kΩ
		ADCKnImS pins	VIAN = AnVSS	1.5		10	kΩ
			VIAN = EnVCC/2	5		19	kΩ
			VIAN = EnVCC	10		34	kΩ

Note 1. It is decided logically, so it has typical value only.

Note 2. For details of tSPL and tSAR, see the RH850/U2C Group User's Manual: Hardware Section 44.4.26, Analog Input Sampling and Scan Group Processing Time of Section 44, Analog to Digital Converter (ADCK).

Note 3. Sampling error is not included.

Note 4. Quantization error (± 0.5 LSB) is not included.

Note 5. Error of only voltage monitor.

Note 6. 10MHz is typical value of CLK_HSIOSC/20.

CAUTION

An analog input pin can also be used as a digital general-purpose input or output pin.

Changes in a digital input or output at the analog input pin during an AD conversion may reduce the precision of conversion.

The coupling noise from the changes in digital inputs or outputs of pins near the analog input pin during an AD conversion may also reduce the precision of conversion.

The power supply noise from the changes in digital outputs of pins of the same power supply as the analog input or the ADC that are performing AD conversion may also reduce the precision of conversion.

3.4.2 Sampling Errors in the External Circuit of the A/D Converter

Sampling error is error to which “Errors (Sampling error 1) which depend on input leakage current of analog pin” and “Errors (Sampling error 2) which depend on conversion cycles with charge sharing” were added.

$$Sampling\ error\ =\ Sampling\ error\ 1\ +\ Sampling\ error\ 2$$

The external circuit of the A/D pin indicates below about the factor (sampling error 1 and sampling error 2) which becomes sampling error.

(a) Errors (Sampling error 1) which depend on input leakage current of analog pin

The error depends on the input leakage current (ILeak) of analog pin and external resistance (Re), and occurs.

The error which depends on the input leakage current is given by the formula of the following.

$$Sampling\ error\ 1\ (LSB)\ =\ Re \times ILeak \times \frac{4096}{V_{avrefh}}$$

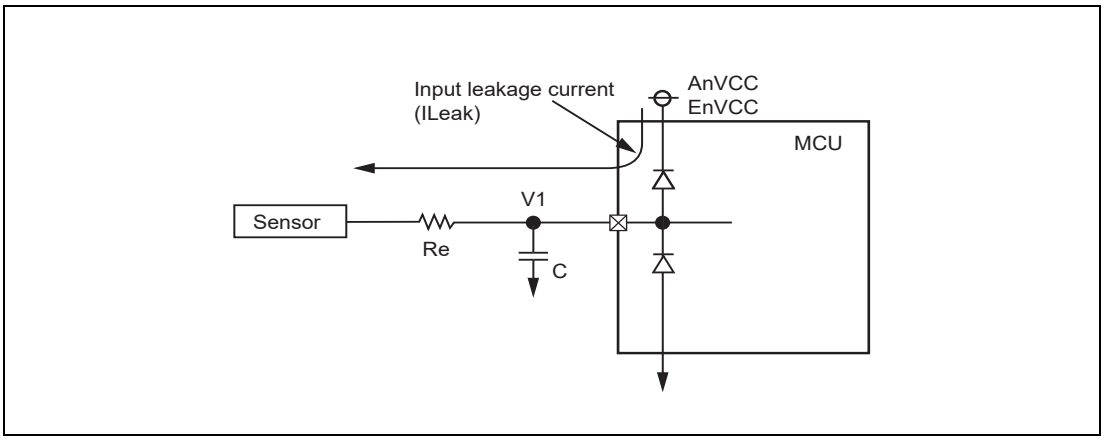


Figure 3.83 Errors (Sampling error 1) which Depend on Input Leakage Current of Analog Pin

(b) Errors (Sampling error 2) which depend on conversion cycles with charge sharing

A formula for errors in sampled values due to the external circuit of the A/D converter is given below. These errors will depend on the input circuit and conversion cycle. The formula given below for the errors is simplified for the calculation of sampling error based on internal stray capacitance, amplifier offset, resistance of the signal source, and conversion cycle. This formula can also be used to calculate the effects of the signal source resistance and conversion cycle on these errors.

The formula gives the error of analog input 2 as shown in the figure below when A/D conversion is performed in the order of analog input 1 then 2.

$$Sampling\ error\ 2\ (LSB) = \left[\left(\frac{|V2 - V1| \times CIN1}{Ce + CIN1} + \frac{|V_{vfaerr}| \times CIN2}{Ce + CIN2}\right) \times \frac{1}{1 - e^{(-T1)/(Re \times Ce)}} + \left(\frac{1}{T1} \times C1 \times V3 \times Re\right)\right] \times \frac{4096}{V_{avrefh}}$$

Table 3.110 Definition of the symbols for the Sampling Error Formula [For U2C8 Only]

Parameter	Symbol	Condition	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	ADCKAIm	2.0	pF
		ADCKAImS	6.7	pF
		ADCK1Im	2.0	pF
		ADCK1ImS	7.3	pF
		ADCK2Im	2.0	pF
		ADCK2ImS	6.7	pF
Common capacitance of the final stage of the amplifier and T&H control circuit	CIN2	ADCKAIm, ADCKAImS	9.2	pF
		ADCK1Im, ADCK1ImS	8.9	pF
		ADCK2Im, ADCK2ImS	8.0	pF

Table 3.111 Definition of the symbols for the Sampling Error Formula [For U2C4/U2C2 Only]

Parameter	Symbol	Condition	Reference	Unit
Common capacitance of the final stage of channel multiplexer	CIN1	ADCKAIm	2.0	pF
		ADCKAImS	6.7	pF
		ADCK1Im	2.0	pF
		ADCK1ImS	7.3	pF
Common capacitance of the final stage of the amplifier and T&H control circuit	CIN2	ADCKAIm, ADCKAImS	9.2	pF
		ADCK1Im, ADCK1ImS	8.9	pF

Table 3.112 Definition of the symbols for the Sampling Error Formula [Common]

Parameter	Symbol	Condition	Reference	Unit
External capacitor on analog input pin	Ce		Depends on customer's environment	µF
Signal source impedance	Re			kΩ
Conversions cycle of analog Input pin	T1			ms
AnVREFH voltage	Vavrefh			V
Potential difference between V1 and V2	V2-V1			V
Offset voltage of the amplifier	Vvfaerr		50	mV
Parasitic capacitance in the channel multiplexer	C1	ADCKnIm	2	pF
		ADCKnImS	4	pF
|AnVCC voltage / 2.5 - measured pin voltage (V2)|	V3		Depends on customer's environment	V

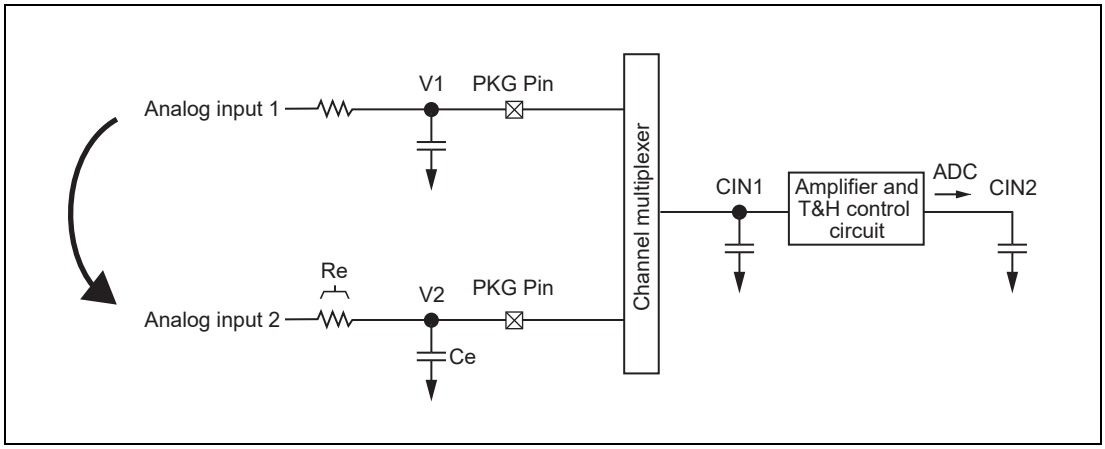


Figure 3.84 Schematic for Sampling Error 2 Formula

Values for conversion error calculated by using this formula do not include error (absolute error, etc.) specified in the A/D converter characteristics.

This formula is a desktop formula and is theoretical. When the signal source has an extremely high resistance or when the conversion cycle is too short, calculated and measured values may differ. Actual error depends on the external capacitor, external resistor, capacitance and resistance of board wiring, so please evaluate and verify the error on the user board is no greater than the value produced by this formula (Condition of this formula is “Re < 1.5 MΩ and T1 ≥ 10 μs”, or “1.5 MΩ ≤ Re ≤ 2 MΩ and T1 ≥ 512 μs”).

3.5 Code Flash Characteristics

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.113 Code Flash Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLKFC} *1		8		40	MHz
Number of rewrites*2	CWRT	Data retention of 20 years*3	1000			times

Note 1. f_{CLKFC} is the frequency of CLK_LSB.

Note 2. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n”, the device can be erased “n” times for each block. For example, when a block of 64 KB is erased after 512 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 3. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Only the processing time of the hardware. The overhead required by the software is not included.

Table 3.114 Code Flash Programming Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming time		512 B	CWRT < 100 times		0.31	1.6		0.25	1.4		0.24	1.3	ms
			CWRT ≥ 100 times		0.39	1.9		0.3	1.7		0.29	1.6	ms
		8 KB	CWRT < 100 times		5.0	12.5		4.0	10.6		3.8	9.8	ms
			CWRT ≥ 100 times		6.0	15.0		4.8	12.7		4.6	11.8	ms
		64 KB	CWRT < 100 times		40	100		32	84.8		30.4	78.4	ms
			CWRT ≥ 100 times		48	120		38.4	101.6		36.8	94.4	ms
		1 MB	CWRT < 100 times		0.64	1.60		0.5	1.36		0.47	1.25	s
			CWRT ≥ 100 times		0.77	1.92		0.6	1.63		0.57	1.50	s
Erasure time*1		16 KB	CWRT < 100 times		26	108		24	98		24	96	ms
			CWRT ≥ 100 times		32	130		29	118		29	116	ms
		64 KB	CWRT < 100 times		88	374		81	340		78	330	ms
			CWRT ≥ 100 times		106	449		98	408		94	396	ms
		1 MB	CWRT < 100 times		1.4	6.0		1.3	5.4		1.25	5.3	s
			CWRT ≥ 100 times		1.7	7.2		1.6	6.5		1.5	6.4	s

Note 1. When erase counter function is used, add the erase counter update time. For detail, see **Table 3.118, Erase Counter update time Characteristics**.

Table 3.115 Code Flash Programming/Erasure suspend latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Suspend Latency	t_{SPD}					150			120			120	µs
Erasure Suspend Latency	t_{SED}					150			120			120	µs

Table 3.116 Code Flash Programming/Erasure resume latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Resume Latency	t_{RPT}					80			50			50	µs
Erasure Resume Latency	t_{RECT}					110			80			80	µs

Table 3.117 Code Flash Forced Stop command latency

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Forced Stop command Latency	t_{FD}					28			20			20	µs

Table 3.118 Erase Counter update time Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFC} < 20 MHz			20MHz ≤ f_{CLKFC} < 40 MHz			f_{CLKFC} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Erase Counter update time					16.06	190.5		14.67	180.54		14.44	178.02	ms

3.6 Data Flash Characteristics

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 3.119 Data Flash Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CLKFD} *1		8		40	MHz
Number of rewrites*2	DWRT	Data retention 20 years*3	125k			Times
		Data retention 3 years*3	250k			Times

Note 1. f_{CLKFD} is the frequency of CLK_LSB.

Note 2. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n”, the device can be erased “n” times for each block. For example, when a block of 4096 bytes is erased after 4 bytes of writing have been performed for different addresses 1024 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 3. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.
- Only the processing time of the hardware. The overhead required by the software is not included.

Table 3.120 Data Flash Programming Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming time		4 B			0.12	0.82		0.09	0.70		0.08	0.66	ms
		8 B			0.13	0.88		0.09	0.73		0.08	0.67	ms
		16 B			0.14	0.97		0.09	0.76		0.08	0.70	ms
		32 B			0.14	0.97		0.09	0.76		0.08	0.70	ms
		64 B			0.14	0.97		0.10	0.76		0.09	0.70	ms
		128 B			0.17	1.20		0.13	0.95		0.11	0.89	ms
		2 KB			2.72	9.64		2.08	7.56		1.76	6.92	ms
		128 KB			0.174	0.62		0.13	0.48		0.11	0.44	s
Property Programming time		32 B			0.41	2.64		0.29	2.18		0.25	2.03	ms
Switch Programming time		32 B			0.26	1.79		0.18	1.46		0.16	1.36	ms
TAG Update time					0.30	1.70		0.21	1.43		0.18	1.34	ms
Erasure time		2 KB *1			11.1	105		9.9	95		9.6	92	ms
		4 KB			19.2	179		17	160		16.4	155	ms
		128 KB			0.62	5.73		0.55	5.12		0.53	4.96	s
Blank check command time		4 B				5.5			2.3			1.3	µs
		4 KB				1.8			0.8			0.5	ms
Property Erase time		2 KB			11.1	105		9.9	9.5		9.6	92	ms
Switch Erase time		2 KB			11.4	106.7		10.1	96.4		9.8	93.4	ms
TAG Erase time		2 KB			11.4	106.7		10.1	96.4		9.8	93.4	ms

Note 1. Extended Data Area Only

Table 3.121 Data Flash Programming/Erasure suspend latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Suspend Latency*1	t_{SPD}					150			120			120	µs
Erase Suspend Latency*1	t_{SED}					150			120			120	µs

Note 1. Data Area and Extended Data Area Only

Table 3.122 Data Flash Programming/Erasure resume latency Characteristics

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD} < 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Programming Resume Latency*1	t_{RPDTS}		After programming or erasing to programming suspending data flash			100			70			70	µs
	t_{RPT}		Other than those above			80			50			50	µs
Erasure Resume Latency*1	t_{REDT}					100			70			70	µs

Note 1. Data Area and Extended Data Area Only

Table 3.123 Forced Stop command latency

Parameter	Symbol	Block size	Condition	8MHz ≤ f_{CLKFD}< 20 MHz			20MHz ≤ f_{CLKFD} < 40 MHz			f_{CLKFD} = 40 MHz			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Forced Stop command Latency	t_{FD}					28			20			20	µs

3.7 Temperature Sensor Characteristics

Conditions:

- See **Section 3.3.1, AC Characteristic Measurement Condition**.

Table 3.124 Temperature Sensor Characteristics*1*2*3

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature accuracy	A_{CCTS1}	- 40°C ≤ Tj ≤ + 140 °C	–4		4	°C
	A_{CCTS2}	Tj > 140 °C	–2		2	°C
Temperature update period	t_{TSUP}		10			ms
Operation stabilization waiting time	t_{TSSB}				200	µs

Note 1. The temperature borders need to be set keeping the temperature range (Tj(min) to Tj(max)) including the temperature sensor accuracy.

Note 2. It does not include accuracy of measuring equipment.

Note 3. Temperature sensor cannot detect local heat generation inside the chip.

3.8 Thermal Characteristics

3.8.1 Thermal Characteristics Parameter

Table 3.125 Thermal Characteristics*1

Parameter	Estimated value							Unit	Remark
	U2C8-EVA	U2C8	U2C4			U2C2			
	BGA404	BGA292	BGA292	QFP144	QFP100	QFP144	QFP100		
θja	14.5	16.5	19.3	13.7	14.1	14.5	15.2	°C/W	BGA: JESD51-9 compliant (4 layers) QFP: JESD51-7 compliant (4 layers)
θjb	8.6	10.3	13.3	6	6.0	6.7	7.0	°C/W	
θjc	6.9	8.15	10	13.4	14.9	15.0	16.6	°C/W	
θjcbot	6.2	7.4	10.4	1.5	2.3	1.9	3	°C/W	
Ψjb	8.4	10	13	5.8	5.8	6.5	6.9	°C/W	
Ψjmb*2	5.6	6.7	9.5	1.2	1.9	1.6	2.6	°C/W	
Ψjt	0.2	0.2	0.3	0.3	0.3	0.4	0.4	°C/W	
4Lθja	17.0	19.5	22.2	16.2	16.4	17.0	17.5	°C/W	L board (4 layers)
4Lθjb	9.9	11.9	14.9	7.8	7.5	8.6	8.6	°C/W	
4LΨjb	9.5	11.4	14.4	7.8	7.4	8.5	8.5	°C/W	
4LΨjmb*2	5.5	6.5	9.2	1.1	1.8	1.5	2.5	°C/W	
4LΨjt	0.2	0.3	0.4	0.4	0.4	0.4	0.5	°C/W	
4LTb_inc	7.6	8.1	8	8.6	9.1	8.6	9.2	°C/W	

Note 1. The thermal characterization parameters depends on the usage environment.

Note 2. Ψjmb shows thermal characterization parameter from junction to board surface (center of the PKG on layer-1; Tmb).

Ψjmb = (Tj-Tmb)/Pd (Pd: power consumption of the chip)

3.8.2 Assumed Board

Table 3.126 JESD51-9 Compliant Board (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board Size	101.5	114.5	11621.75
Remaining copper rate		Conductor thickness	
50 – 95 – 95 – 50%		70 – 35 – 35 – 70 µm	

Table 3.127 JESD51-7 Compliant Board (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board	76.2	114.3	8709.66
Remaining copper rates		Thickness of conductors	
50–95–95–50%		70–35–35–70 µm	

Table 3.128 L board (4 layers)

	Board Size (mm)		
	X	Y	Area (mm^2)
Board Size	90	160	14400
Remaining copper rate		Conductor thickness	
30 – 80 – 80 – 30%		35 – 35 – 35 – 35 µm	

Section 4 Package

4.1 Package Outline

Table 4.1 RH850/U2Cx Package list

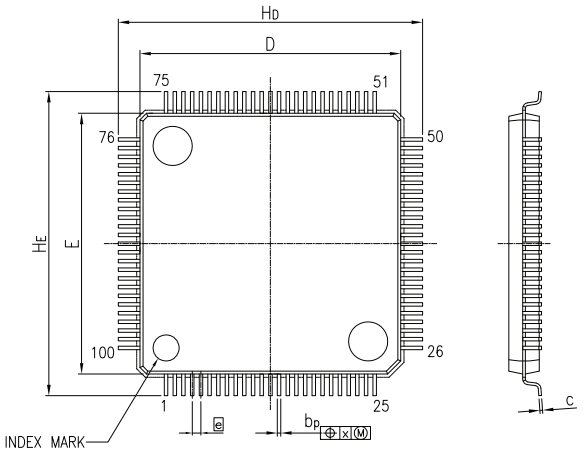
Package	RH850/U2C8-EVA	RH850/U2C8	RH850/U2C4	RH850/U2C2
Plastic HLQFP100 0.4-mm ball pitch 12 mm × 12 mm			√	√
Plastic HLQFP144 0.4-mm ball pitch 16 mm × 16 mm			√	√
Plastic FBGA292 0.8-mm ball pitch 17 mm × 17 mm		√	√	
Plastic FBGA404 0.8-mm ball pitch 19 mm × 19 mm	√			

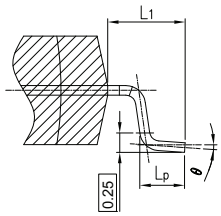
4.1.1 HLQFP100 Package (0.4 mm ball pitch) Drawing

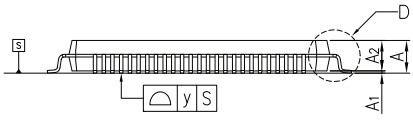
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HLFQFP100-12x12-0.40	PLQP0100LB-A	0.50

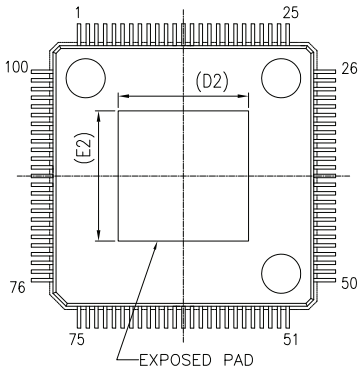
UNIT:MM

NOTE)
1. DIMENSION "D"&"E" DO NOT INCLUDE MOLD FLASH.
2. LEAD WIDTH "bp" DOES NOT INCLUDE TRIM OFFSET.





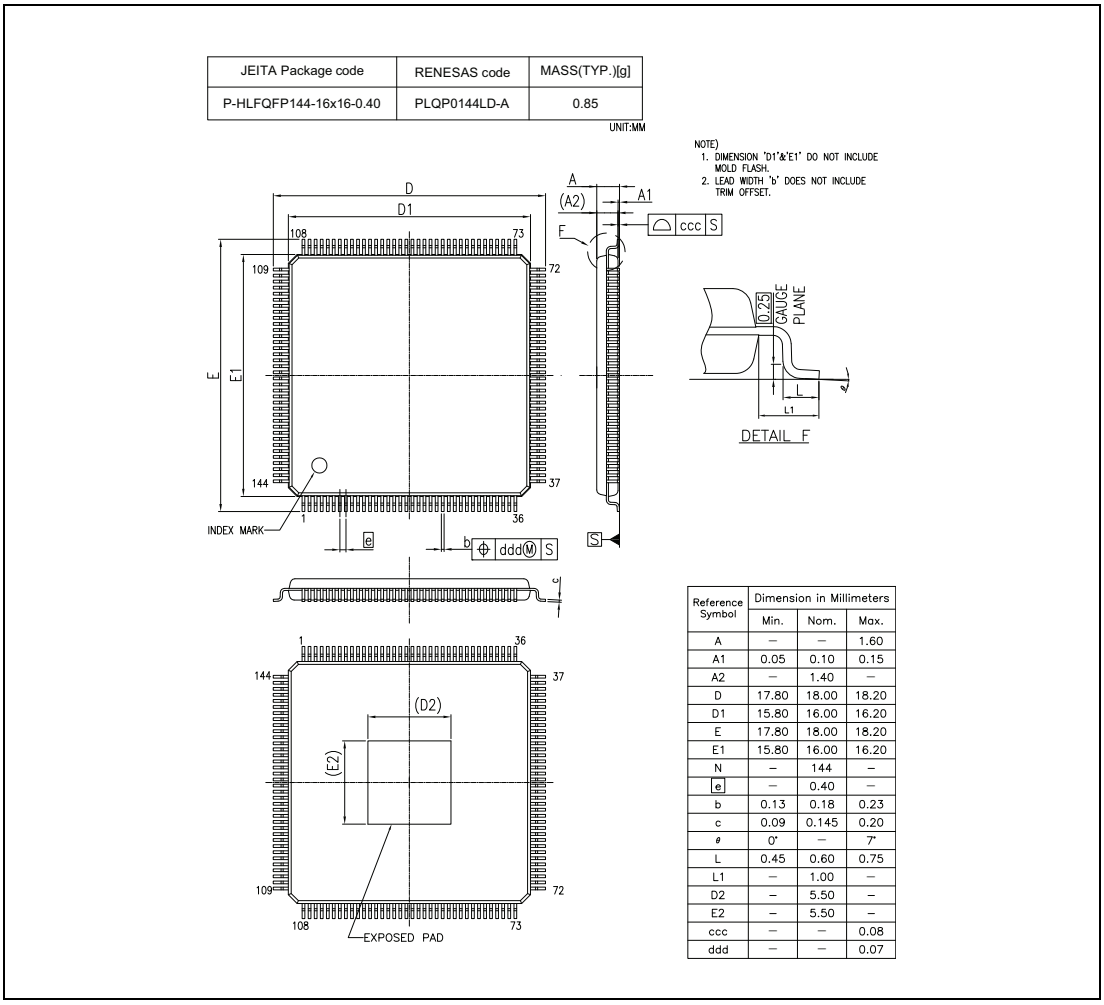




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.70
A_1	0.05	0.10	0.15
A_2	–	1.40	–
H_D	13.80	14.00	14.20
D	11.90	12.00	12.10
H_E	13.80	14.00	14.20
E	11.90	12.00	12.10
N	–	100	–
e	–	0.40	–
b_p	0.13	0.18	0.23
c	0.09	0.145	0.20
θ	0°	–	8°
L_p	0.45	0.60	0.75
L_1	–	1.00	–
D2	–	6.00	–
E2	–	6.00	–
y	–	–	0.08
x	–	–	0.07

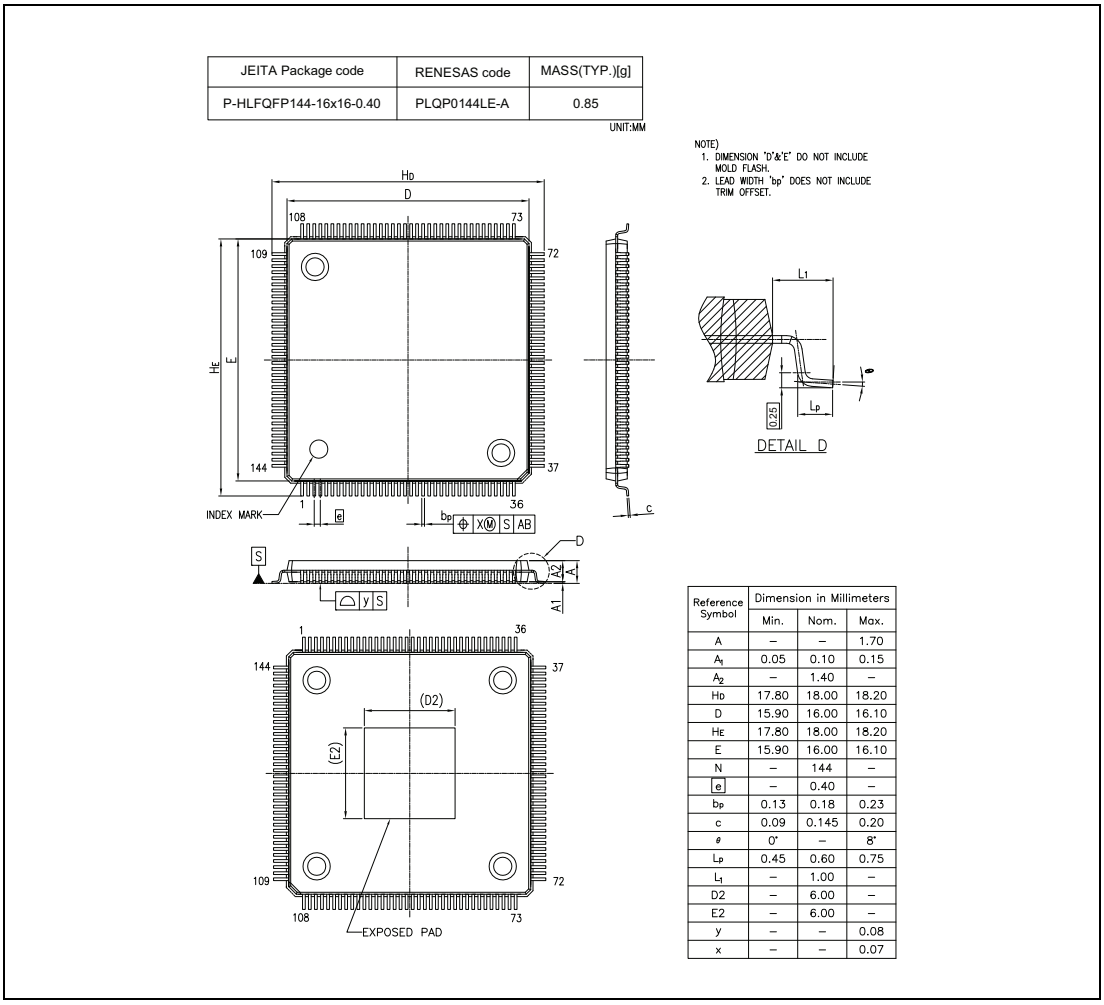
Figure 4.1 HLQFP100 (0.4 mm ball pitch) outline for R7F7026*FD-C

4.1.2 HLQFP144 Package (0.4 mm ball pitch) Drawing



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	0.10	0.15
A2	–	1.40	–
D	17.80	18.00	18.20
D1	15.80	16.00	16.20
E	17.80	18.00	18.20
E1	15.80	16.00	16.20
N	–	144	–
e	–	0.40	–
b	0.13	0.18	0.23
c	0.09	0.145	0.20
θ	0°	–	7°
L	0.45	0.60	0.75
L1	–	1.00	–
D2	–	5.50	–
E2	–	5.50	–
ccc	–	–	0.08
ddd	–	–	0.07

Figure 4.2 HLQFP144 (0.4 mm ball pitch) outline for R7F7026*FM-C

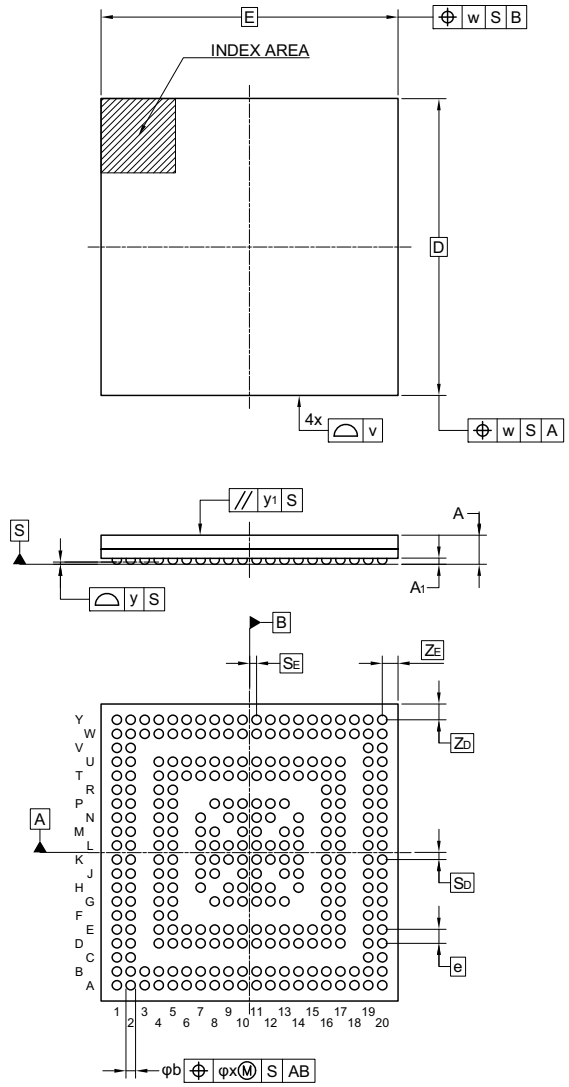


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	–	–	1.70
A_1	0.05	0.10	0.15
A_2	–	1.40	–
H_D	17.80	18.00	18.20
D	15.90	16.00	16.10
H_E	17.80	18.00	18.20
E	15.90	16.00	16.10
N	–	144	–
e	–	0.40	–
b_p	0.13	0.18	0.23
c	0.09	0.145	0.20
θ	0°	–	8°
L_p	0.45	0.60	0.75
L_1	–	1.00	–
D2	–	6.00	–
E2	–	6.00	–
y	–	–	0.08
x	–	–	0.07

Figure 4.3 HLQFP144 (0.4 mm ball pitch) outline for R7F7026*FB-C

4.1.3 FBGA292 Package Drawing

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA292-17x17-0.80	PRBG0292GC-A	T292F1-80-GNP	0.9



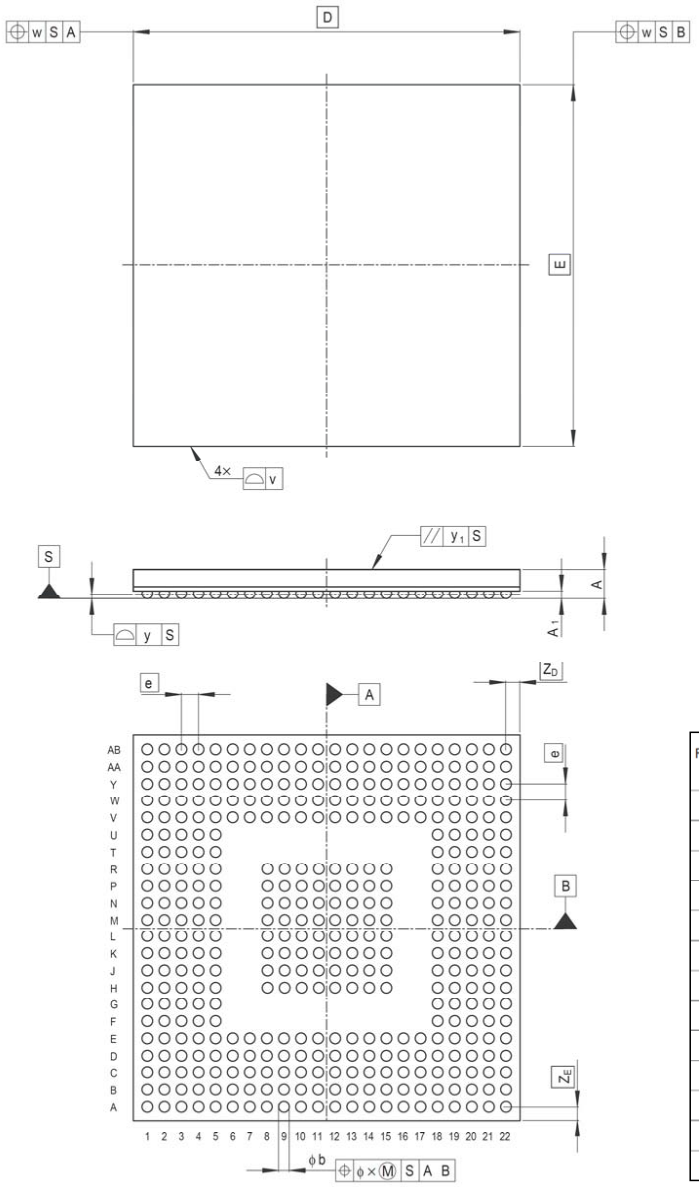
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	–	17.00	–
E	–	17.00	–
A	–	–	1.90
A_1	0.30	0.35	0.40
e	–	0.80	–
b	0.50	0.55	0.60
x	–	–	0.12
y	–	–	0.10
y_1	–	–	0.20
Z_D	–	0.90	–
Z_E	–	0.90	–
v	–	–	0.15
w	–	–	0.20
S_D	–	0.40	–
S_E	–	0.40	–

Note: • INDEX AREA is on the corner near a ball A1 (Top view side).

Figure 4.4 FBGA (292pin) outline

4.1.4 FBGA404 Package Drawing

JEITA Package Code	RENESAS Code	Previous Code	MASS(TYP.)[g]
P-FBGA404-19x19-0.80	PRBG0404GA-A	-	1.1



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	19	—
E	—	19	—
v	—	—	0.15
w	—	—	0.2
A	—	—	1.9
A_1	0.35	0.4	0.45
e	—	0.8	—
b	0.45	0.5	0.55
x	—	—	0.08
y	—	—	0.1
y_1	—	—	0.2
Z_D	—	1.1	—
Z_E	—	1.1	—

Note: • INDEX AREA is on the corner near a ball A1 (Top view side).

Figure 4.5 FBGA (404pin) outline

Revision History

Rev	Date	Description	
		Section	Summary
1.00	Jan. 31, 2026	—	Initial release The descriptions of 3.3.7.2, 3.3.7.4, 3.3.3.5, and 3.3.25 have been updated from those in the RH850/U2C Group User's Manual: Hardware Rev.1.00.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to power supply or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
5. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
6. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
7. Power ON/OFF sequence
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/