RJE0627JNS

–60V, –7A, P Channel Thermal FET
Power Switching

R07DS1533EJ0100
Rev.1.00
Dec 01, 2023

Description

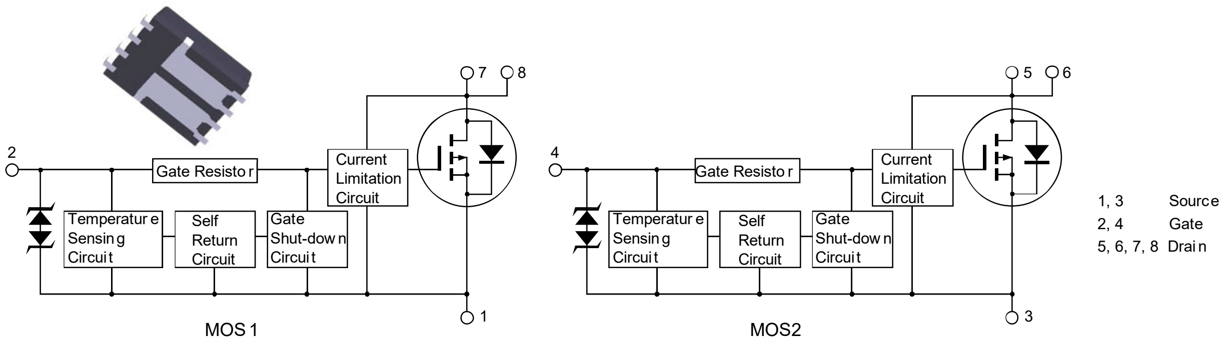
This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (3 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Hysteresis type shut down operation.
- High density mounting
- Built-in the current limitation circuit.
- Power supply voltage applies 12 V and 24 V.
- AEC-Q101Rev-E compliant.

Outline

RENESAS Package code: PLSN0008DA-A
(Package name: 8-pin HSON dual)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	–16	V
Gate to source voltage	V_{GSS}	2.5	V
Drain current	I_D Note4	–7	A
Body-drain diode reverse drain current	I_{DR}	–7	A
Avalanche current	I_{AP} Note 3	–7	A
Avalanche energy	E_{AR} Note 3	14.7	mJ
Channel dissipation	Pch Note 1	30	W
Channel dissipation	Pch Note 2	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes:
1. Tch = 25°C, 1 Drive operation.
2. 1 Drive operation : When using the glass epoxy board (FR4 40 × 40 × 1.6 mm)
3. Tch = 25°C, Rg ≥ 50 Ω
4. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	–3	—	—	V	
	V_{IL}	—	—	–1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	–100	μA	Vi = –8 V, V_{DS} = 0
	I_{IH2}	—	—	–50	μA	Vi = –3.5 V, V_{DS} = 0
	I_{IL}	—	—	–1	μA	Vi = –1.2 V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH(sd)1}$	—	–0.8	—	mA	Vi = –8 V, V_{DS} = 0
	$I_{IH(sd)2}$	—	–0.35	—	mA	Vi = –3.5 V, V_{DS} = 0
Shut down temperature	Tsd	—	175	—	°C	Channel temperature
Return temperature	Thr	—	145	—	°C	Channel temperature
Gate operation voltage	Vop	–3	—	–12	V	
Drain current (Current limitation value)	$I_{D\ limt}$	–7	—	—	A	Vi = –12 V, V_{DS} = –10 V $^{\text{Note 5}}$

Notes: 5. Pulse test

Electrical Characteristics

(Ta = 25°C)

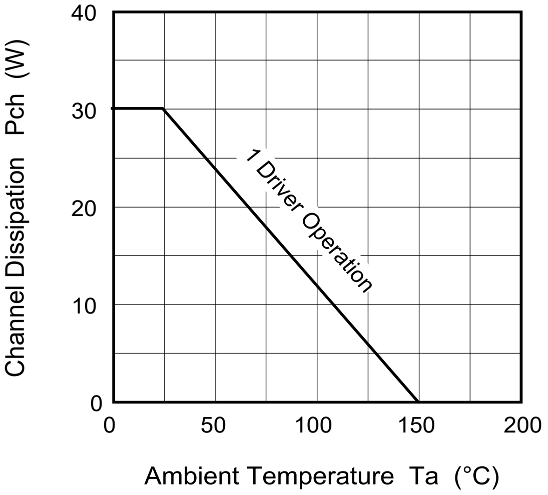
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_D	—	—	—	mA	V_{GS} = –1.2 V, V_{DS} = –10 V $^{\text{Note 6}}$
	I_D	–0.8	—	—	A	V_{GS} = –3 V, V_{DS} = –10 V $^{\text{Note6}}$
	I_D	–7	—	—	A	V_{GS} = –12 V, V_{DS} = –10 $^{\text{Note 6}}$
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	–16	—	—	V	I_G = –800 μA, V_{DS} = 0
	$V_{(BR)GSS}$	2.5	—	—	V	I_G = 100 μA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	–100	μA	V_{GS} = –8 V, V_{DS} = 0
	I_{GSS}	—	—	–50	μA	V_{GS} = –3.5 V, V_{DS} = 0
	I_{GSS}	—	—	–1	μA	V_{GS} = –1.2 V, V_{DS} = 0
	I_{GSS}	—	—	100	μA	V_{GS} = 2.4 V, V_{DS} = 0
Input current (shut down)	$I_{GS(OP)}$	—	–0.8	—	mA	V_{GS} = –8 V, V_{DS} = 0
	$I_{GS(OP)}$	—	–0.35	—	mA	V_{GS} = –3.5 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–10	μA	V_{DS} = –60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.9	—	–2.1	V	V_{DS} = –10 V, I_D = –1 mA
Forward transfer admittance	$\lvert y_{fs} \rvert$	1.5	4.3	—	S	I_D = –3.5 A, V_{GS} = –10 V $^{\text{Note 6}}$
Static drain to source on state resistance	$R_{DS(on)}$	—	358	800	mΩ	I_D = –0.4 A, V_{GS} = –3V $^{\text{Note 6}}$
	$R_{DS(on)}$	—	312	400	mΩ	I_D = –3.5 A, V_{GS} = –4 V $^{\text{Note 6}}$
	$R_{DS(on)}$	—	232	260	mΩ	I_D = –3.5 A, V_{GS} = –10 V $^{\text{Note 6}}$
Output capacitance	Coss	—	247	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	1.2	—	μs	V_{GS} = –10 V, I_D= –3.5 A, R_L = 8.57 Ω
Rise time	t_r	—	5.2	—	μs	
Turn-off delay time	$t_{d(off)}$	—	1.2	—	μs	
Fall time	t_f	—	2.3	—	μs	
Body-drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –7 A, V_{GS} = 0
Body-drain diode reverse recovery time	t_{rr}	—	83	—	ns	I_F = –7 A, V_{GS} = 0 di_F/dt = 50 A/μs
Over load shut down operation time $^{\text{Note 7}}$	t_{os1}	—	2.6	—	ms	V_{GS} = –5 V, V_{DD} = –16 V
Over load shut down operation time $^{\text{Note 7}}$	t_{os2}	—	1.1	—	ms	V_{GS} = –5 V, V_{DD} = –24 V

Notes: 6. Pulse test

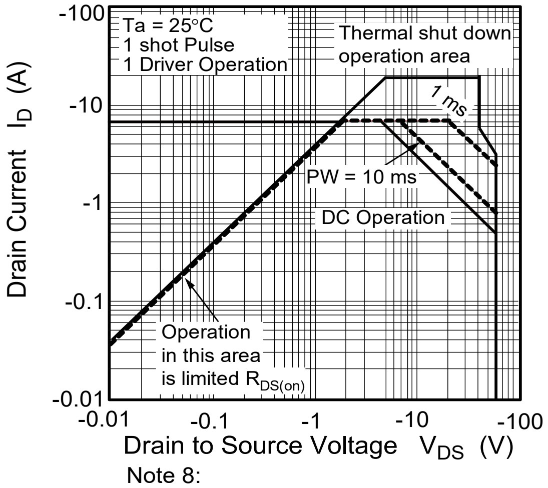
7. Including the junction temperature rise of the over loaded condition.

Main Characteristics

Power vs. Temperature Derating

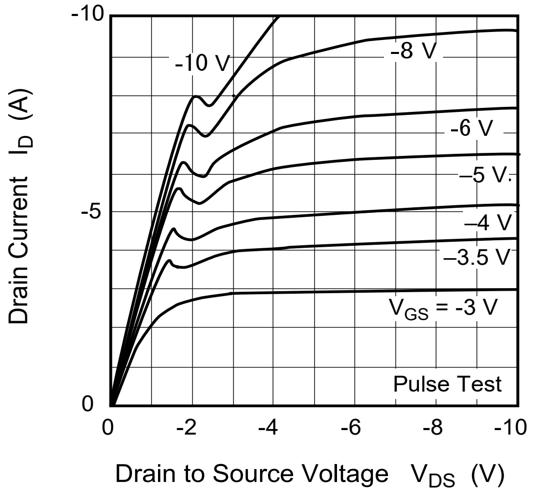


Maximum Safe Operation Area

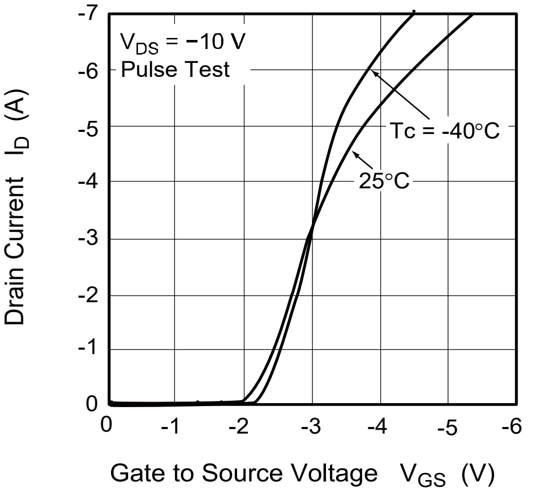


Note 8:
When using the glass epoxy board.
(FR4 40 x 40 x 1.6 mm)

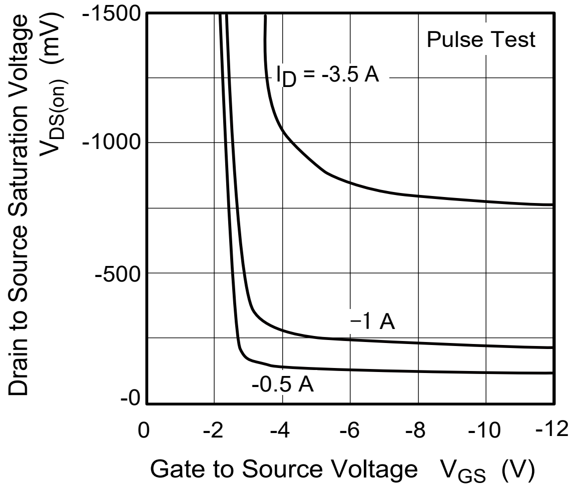
Typical Output Characteristics



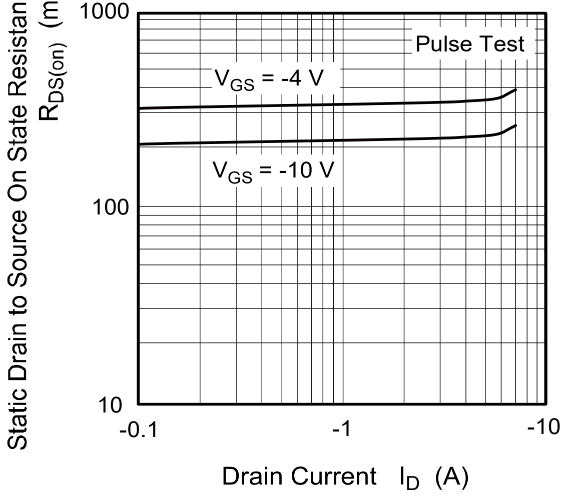
Typical Transfer Characteristics

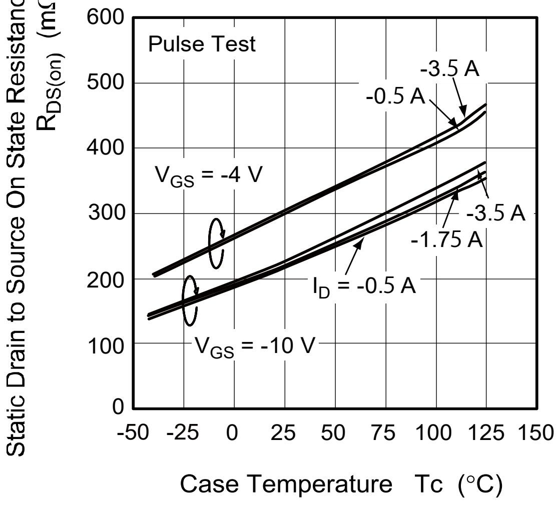


Drain to Source Saturation Voltage vs.
Gate to Source Voltage

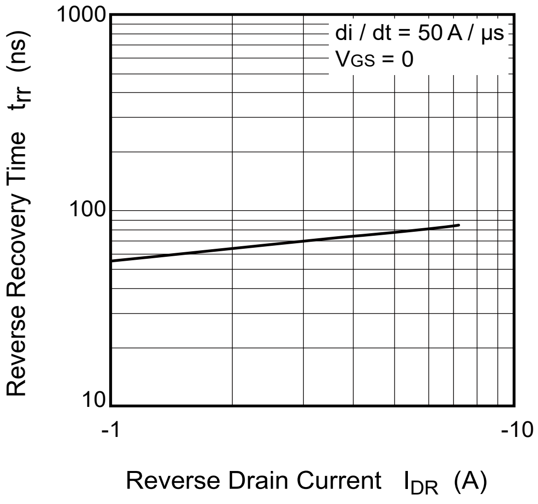


Static Drain to Source On State Resistance
vs. Drain Current

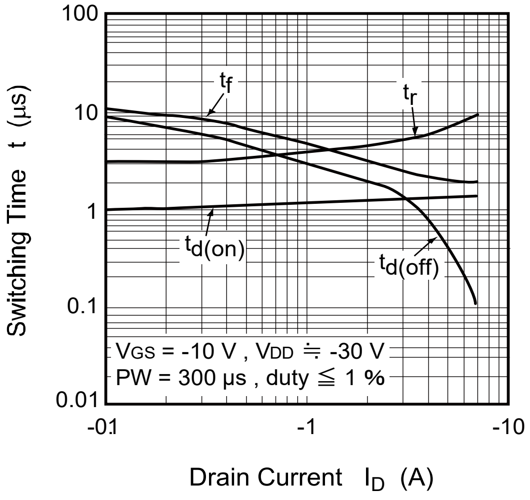




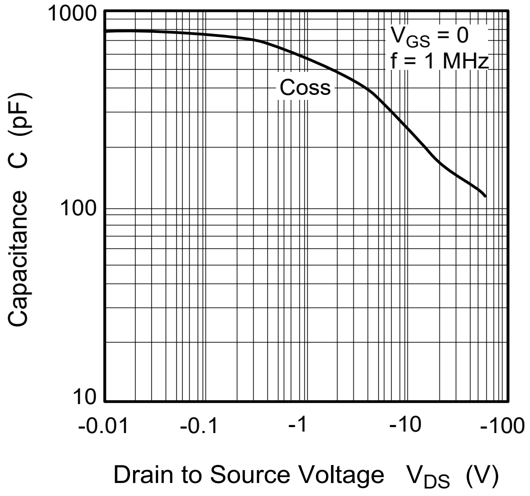
Static Drain to Source On State Resistance vs. Temperature



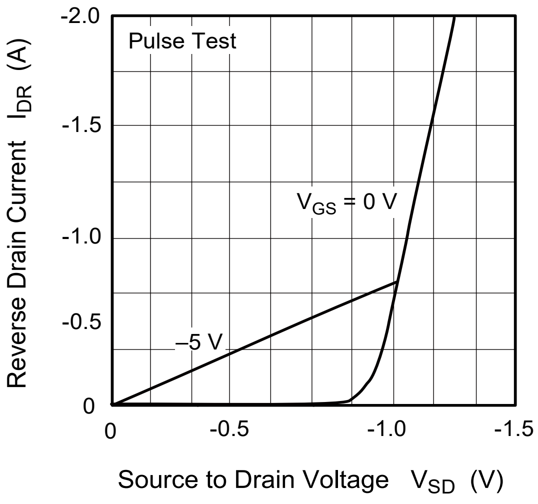
Body-Drain Diode Reverse Recovery Time



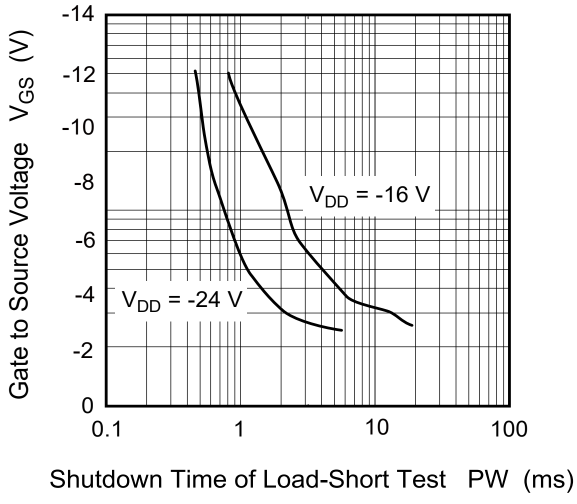
Switching Characteristics



Typical Capacitance vs. Drain to Source Voltage

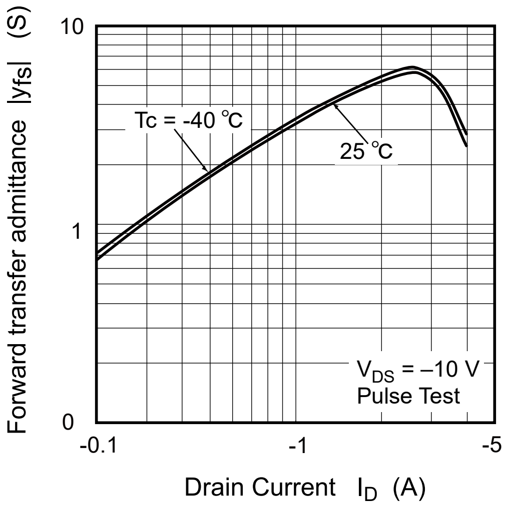


Reverse Drain Current vs. Source to Drain Voltage

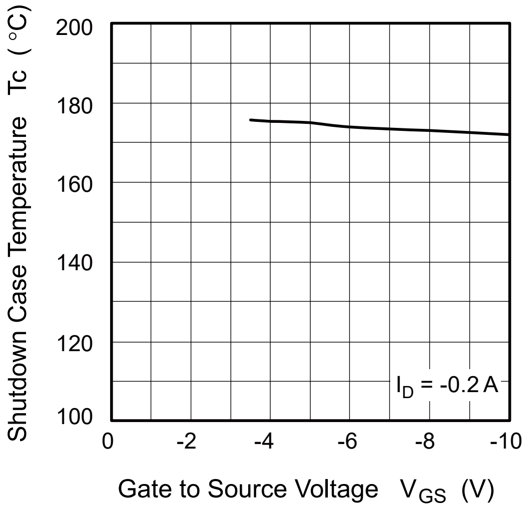


Gate to Source Voltage vs. Shutdown Time of Load-Short Test

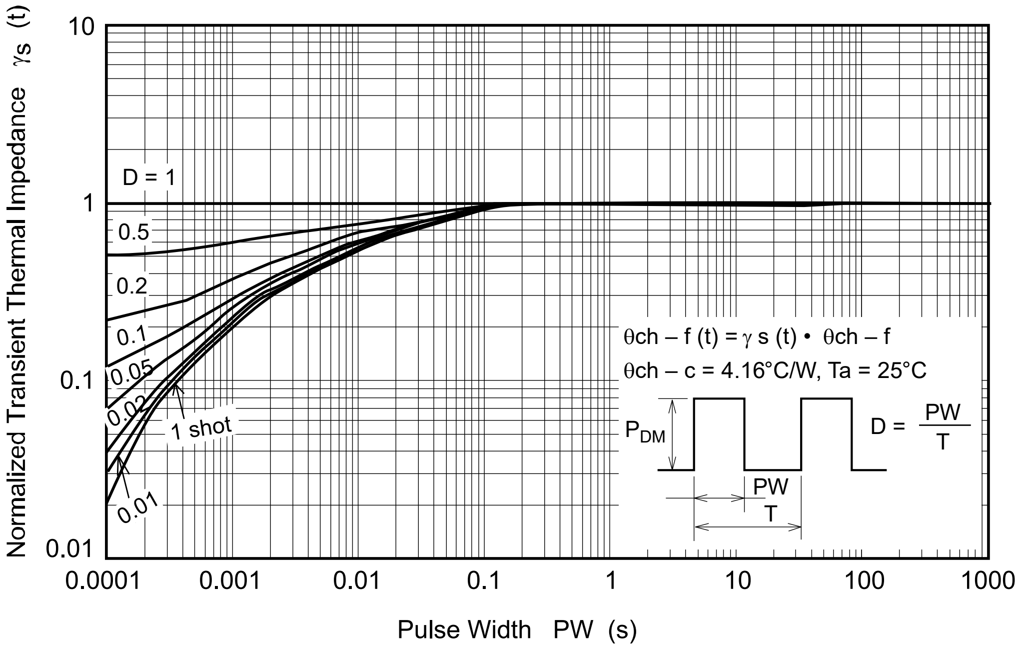
Forward transfer admittance vs. Drain Current



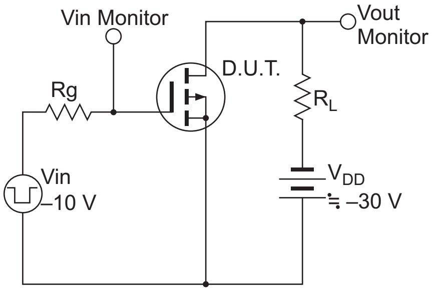
Shutdown Case Temperature vs. Gate to Source Voltage



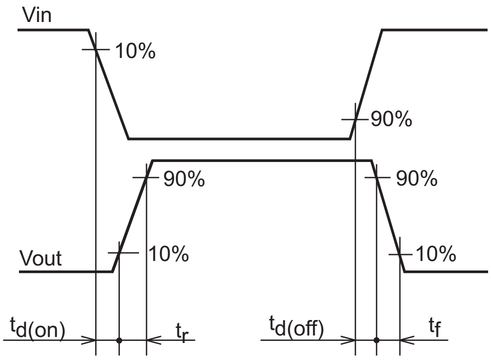
Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)



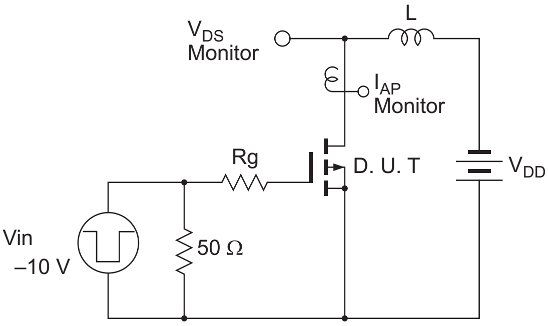
Switching Time Test Circuit



Waveform

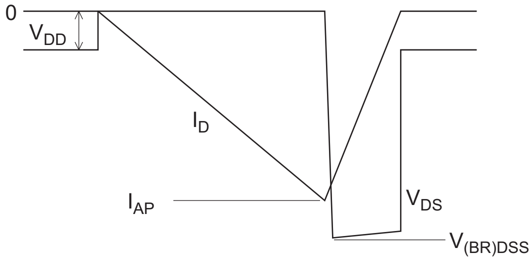


Avalanche Test Circuit



Avalanche Waveform

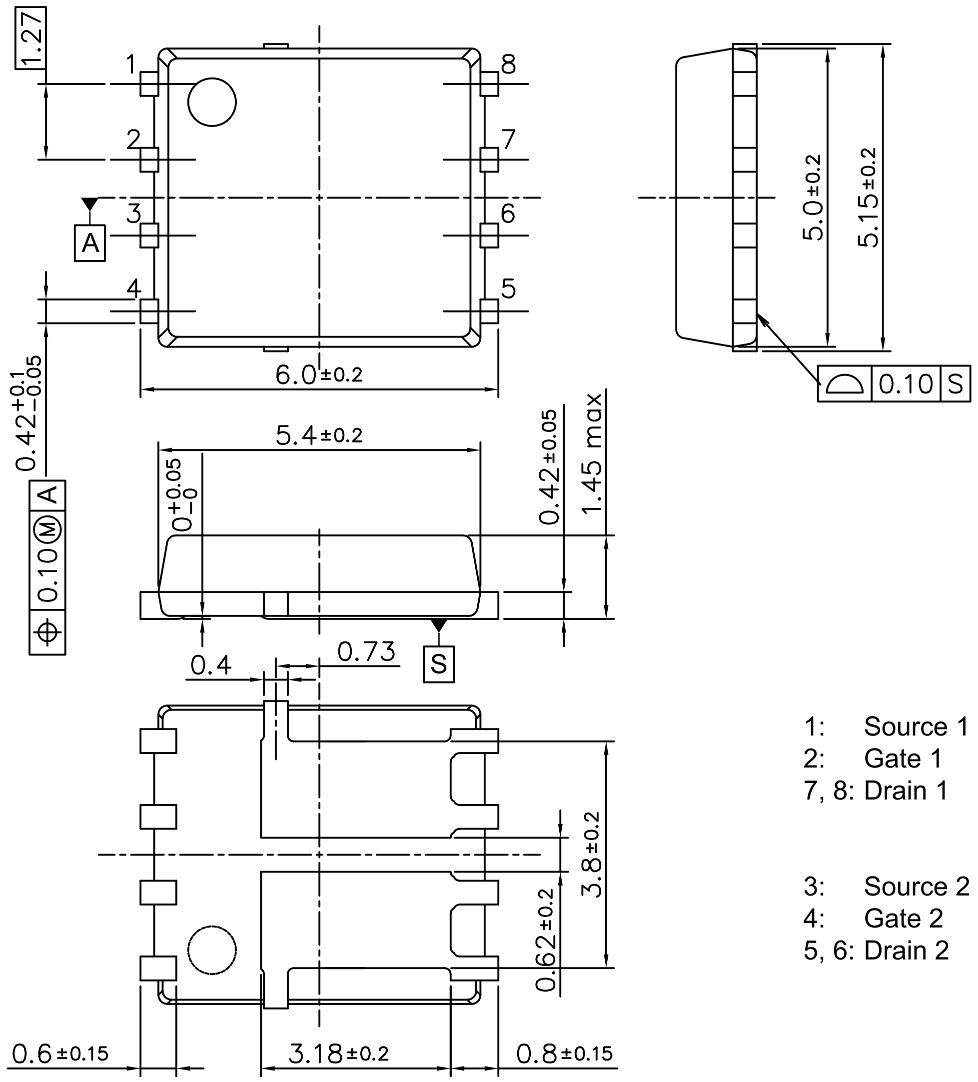
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}{}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Package Dimensions

8-pin HSON Dual (Mass: 0.12 g TYP.)

Renesas package code: PLSN0008DA-A



1: Source 1
2: Gate 1
7, 8: Drain 1

3: Source 2
4: Gate 2
5, 6: Drain 2

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJE0627JNS-00-Q7	2500 pcs/reel	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".