RJP65S04DWA / RJP65S04DWS

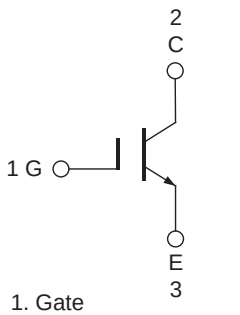
650V - 50A - IGBT
Application: Inverter

R07DS0821EJ0400
Rev.4.00
Nov. 06, 2015

Features

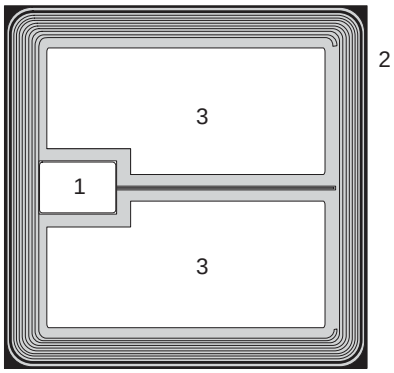
- Low collector to emitter saturation voltage
  $V_{CE(sat)}$ = 1.5 V typ. (at I_C = 50 A, V_{GE} = 15 V, Ta = 25°C)
- High speed Switching
- Short circuit withstands time (10 μs min.)

Outline

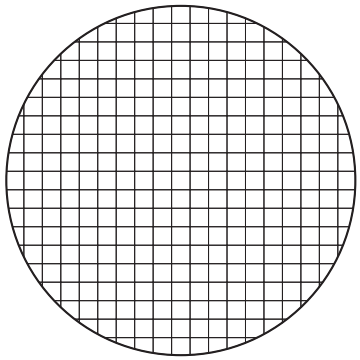


1. Gate
2. Collector (The back)
3. Emitter

Die: RJP65S04DWT-80



Wafer: RJP65S04DWA-80



Absolute Maximum Ratings

(Tc = 25°C unless otherwise noted)

Item		Symbol	Ratings	Unit
Collector to emitter voltage		V_{CES}	650	V
Gate to emitter voltage		V_{GES}	±30	V
Collector current	Tc = 25°C	I_C	100	A
	Tc = 100°C	I_C	50	A
Junction temperature		Tj	175 Note1	°C

Notes: 1. Please use this device in the thermal conditions where the junction temperature does not exceed 175°C.
IGBT Application Note is disclosed about reliability test and application condition up to Tj = 175°C.

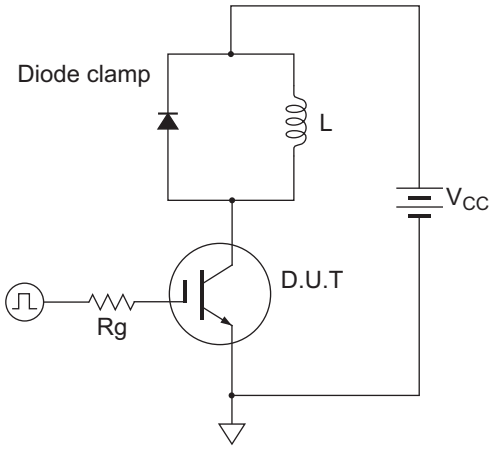
Electrical Characteristics (Datas below are measured values on a package configuration.)

(Tc = 25°C unless otherwise noted)

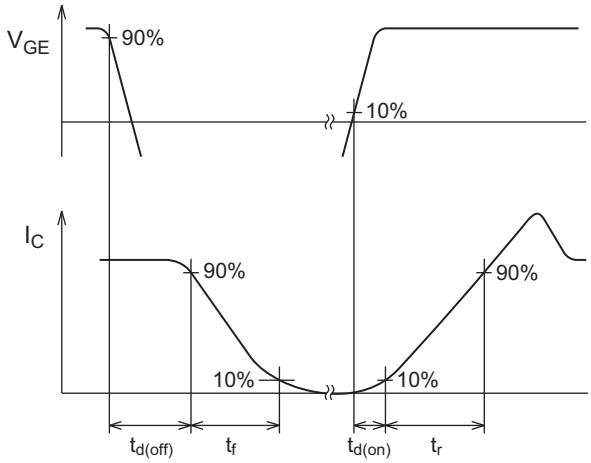
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage collector current	I_{CES}	—	—	1	μA	V_{CE} = 650 V, V_{GE} = 0
Gate to emitter leak current	I_{GES}	—	—	±1	μA	V_{GE} = ±30 V, V_{CE} = 0
Gate to emitter cutoff voltage	$V_{GE(off)}$	5.0	—	6.8	V	V_{CE} = 10 V, I_C = 1.0mA
Collector to emitter saturation voltage	$V_{CE(sat)}$	—	1.50	1.80	V	I_C = 50 A, V_{GE} = 15 V Note2
Input capacitance	Cies	—	4500	—	pF	V_{CE} = 25 V V_{GE} = 0 f = 1 MHz
Output capacitance	Coes	—	200	—	pF	
Reveres transfer capacitance	Cres	—	150	—	pF	
Total gate charge	Qg	—	225	—	nC	V_{GE} = 15 V V_{CE} = 300 V I_C = 50 A
Gate to emitter charge	Qge	—	40	—	nC	
Gate to collector charge	Qgc	—	120	—	nC	
Switching time Note3	$t_{d(on)}$	—	25	—	ns	V_{CC} = 300 V I_C = 50 A V_{GE} =±15 V Rg = 10 Ω, Tc = 150 °C Inductive load
	t_r	—	35	—	ns	
	$t_{d(off)}$	—	215	—	ns	
	t_f	—	100	—	ns	
Short circuit withstand time Note4	t_{sc}	10	—	—	μs	V_{CC} ≤ 360 V , V_{GE} = 15 V Tc = 150 °C

Notes: 2. Pulse test.
3. Switching time test circuit and waveform are shown below.
4. Verified by design.

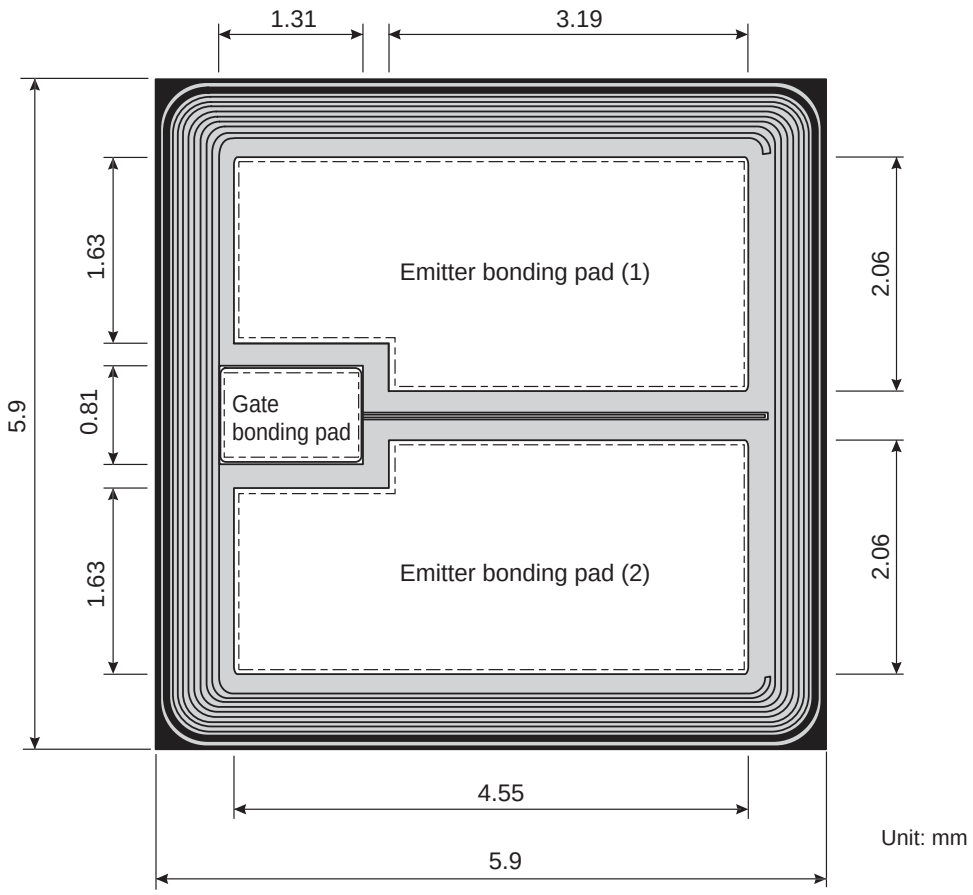
Switching Time Test Circuit



Waveform



Die Dimension



Note 1.

Illustration	Definition
Part of white	Al pattern
Part of dotted line	Bonding area
Part of gray	Final passivation

Note 2. The back of the chip is processed with Au evaporation.

Note 3. Recognition, target and any other patterns which are not related to Diode operation, may be changed without notice.

Ordering Information

Orderable Part Number	Shipment form
RJP65S04DWA-80#W0	Unsawn wafer
RJP65S04DWS-80#W0	Sawn wafer

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