RL78/D1A

RENESAS MCU

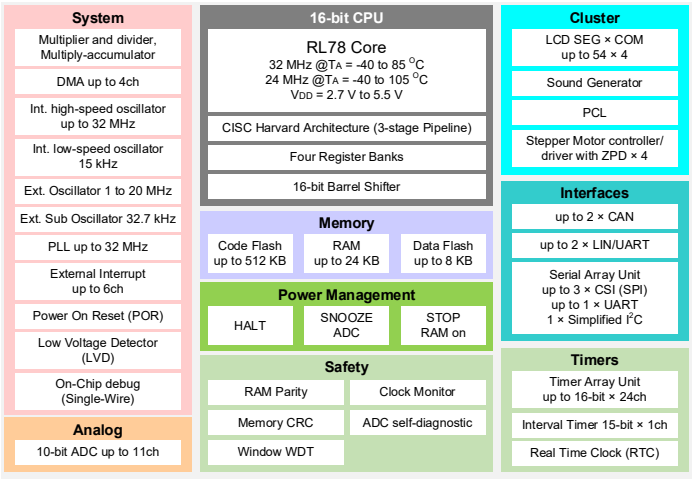
R01DS0463EJ0110
Rev. 1.10
Dec 27. 2024

RL78/D1A microcontrollers have a built-in sound generator which can set a volume level and tone frequency of 100 Hz to 6 kHz and has an automatic volume decrement function, up to four channels of stepper motor controller/driver which can set an 8-bit precision (pseudo 9-bit precision using a 1-bit addition function) pulse width (PWM output), and an LCD controller/driver which supports up to 216 segments. The 128-pin version has a built-in LCD bus interface and two channels of CAN, and expanded flash memory/RAM up to a maximum of 512 KB/24 KB, making these microcontrollers ideal for low-end instrument cluster.

1. OUTLINE

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.03125 μs: @ 32 MHz operation with high-speed on-chip oscillator clock) to ultra low-speed (30.5 μs: @ 32.768 kHz operation with subsystem clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM: 24 to 512 KB
- RAM: 2 to 24 KB
- Data flash memory: 8 KB
- On-chip high-speed on-chip oscillator clocks
  Select from 32 MHz (TYP.), 24 MHz (TYP.), 16 MHz (TYP.), 8 MHz (TYP.), and 4 MHz (TYP.)
- On-chip single-power-supply flash memory (with prohibition of block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated low-speed on-chip oscillator clock)
- On-chip multiplier and divider/multiply-accumulator
  16 bits × 16 bits = 32 bits (Unsigned or signed)
  32 bits ÷ 32 bits = 32 bits (Unsigned)
  16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 38 to 112
  CMOS I/O port: 35 to 107 (LED direct drive port: 9 to 16, N-ch OD selectable port: 4 to 6)
  CMOS input port: 5
  CMOS output port: 0 to 1
- Timer
  - 16-bit timer: 24 channels
  - Watchdog timer: 1 channel
  - Real-time clock: 1 channel
  - Interval timer: 1 channel
- Serial interface
  - CSI
  - UART (LIN-bus supported)
  - Simplified I^2C communication
  - aFCAN controller
- Stepper motor controller/driver with zero point detection (ZPD): 1, 2, 4-channels
- LCD controller/driver (seg × com): 27 × 4, 39 × 4, 48 × 4, 53 × 4 and 54 × 4
- LCD Bus I/F
- RESET output
- STOP status output
- Sound generator
- 8/10-bit resolution A/D converter (V_{DD} = EV_{DD} =2.7 to 5.5 V): 3+2 to 9+2 channels
- Standby function: HALT, STOP, SNOOZE mode
- Power supply voltage: V_{DD} = 2.7 to 5.5 V
- Operating ambient temperature:
  J grade products T_A = –40 to +85°C,
  L grade products T_A = –40 to +105°C



RL78/D1A Block Diagram (Outline)

Remark The functions mounted depend on the product.
See **1.7 Outline of Functions**.

Table 1-1. ROM, RAM capacities

Flash ROM	Data flash	RAM	48-pin		64-pin		80-pin	
512 KB	8 KB	24 KB	–	–	–	–	–	–
384 KB		20 KB	–	–	–	–	–	–
256 KB		16 KB	–	–	–	–	–	R5F10DMJxFB
128 KB		8 KB	–	–	–	–	–	R5F10DMGxFB
96 KB		6 KB	–	–	–	–	–	R5F10DMFxFB
64 KB		4 KB	–	R5F10DGExFB	–	R5F10DLExFB	R5F10CMExFB	R5F10DMExFB
48 KB		3 KB	R5F10CGDxFB	R5F10DGDxFB	R5F10CLDxFB	R5F10DLDxFB	R5F10CMDxFB	R5F10DMDxFB
32 KB		2 KB	R5F10CGCxFB	R5F10DGCxFB	–	–	–	–
24 KB		2 KB	R5F10CGBxFB	–	–	–	–	–
CAN (ch)			0	1	0	1	0	1
Stepper Motor (ch)			1		2		4	
LCD (seg × com)			27 × 4		39 × 4		48 × 4	

Flash ROM	Data flash	RAM	100-pin		128-pin
512 KB	8 KB	24 KB	–	R5F10DPLxFB	R5F10DSLxFB
384 KB		20 KB	–	R5F10DPKxFB	R5F10DSKxFB
256 KB		16 KB	R5F10TPJxFB	R5F10DPJxFB	R5F10DSJxFB
128 KB		8 KB	R5F10DPGxFB	–	–
96 KB		6 KB	R5F10DPFxFB	–	–
64 KB		4 KB	R5F10DPExFB	–	–
48 KB		3 KB	–	–	–
32 KB		2 KB	–	–	–
24 KB		2 KB	–	–	–
CAN (ch)			1	2	2
Stepper Motor (ch)			4		4
LCD (seg × com)			53 × 4		54 × 4

1.2 Applications

Automotive electrical appliances (instrument cluster)

1.3 Ordering Information

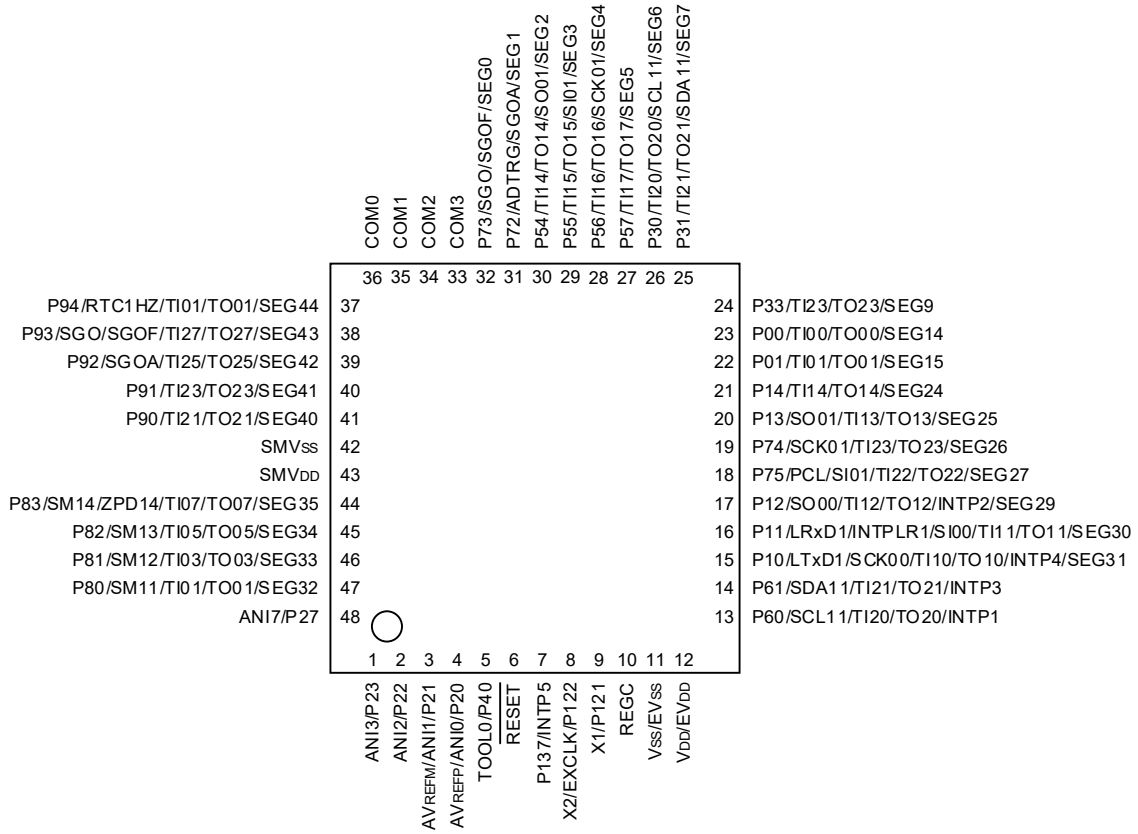
[List of Part Number]

Pin count	Package	Part Number	
		Operating ambient temperature J grade (TA = -40 to +85 °C)	Operating ambient temperature L grade (TA = -40 to +105 °C)
48-pin	48-pin plastic LQFP (fine pitch) (7 × 7)	R5F10CGBCJFB R5F10CGCCJFB R5F10CGDCJFB R5F10DGCCJFB R5F10DGDCJFB R5F10DGECJFB	R5F10CGBCLFB R5F10CGCCLFB R5F10CGDCLFB R5F10DGCCLFB R5F10DGDCLFB R5F10DGECLFB
64-pin	64-pin plastic LQFP (fine pitch) (10 × 10)	R5F10CLDCJFB R5F10DLDCJFB R5F10DLECJFB	R5F10CLDCLFB R5F10DLDCLFB R5F10DLECLFB
80-pin	80-pin plastic LQFP (fine pitch) (12 × 12)	R5F10CMDCJFB R5F10CMECJFB R5F10DMDCJFB R5F10DMECJFB R5F10DMFCJFB R5F10DMGCJFB R5F10DMJCJFB	R5F10CMDCLFB R5F10CMECLFB R5F10DMDCLFB R5F10DMECLFB R5F10DMFCLFB R5F10DMGCLFB R5F10DMJCLFB
100-pin	100-pin plastic LQFP (fine pitch) (14 × 14)	R5F10DPECJFB R5F10DPFCJFB R5F10DPGCJFB R5F10TPJCJFB R5F10DPJCJFB R5F10DPKJFB R5F10DPLJFB	R5F10DPECLFB R5F10DPFCLFB R5F10DPGCLFB R5F10TPJCLFB R5F10DPJCLFB R5F10DPKLFB R5F10DPLLFB
128-pin	128-pin plastic LQFP (fine pitch) (14 × 20)	R5F10DSLJFB R5F10DSKJFB R5F10DSJJFB	R5F10DSLLFB R5F10DSKLFB R5F10DSJLFB

1.4 Pin Configuration (Top View)

1.4.1 48-pin products (R5F10CGBxFB, R5F10CGCxFB, R5F10CGDxFB: with no CAN)

48-pin plastic LQFP (fine pitch) (7 × 7)

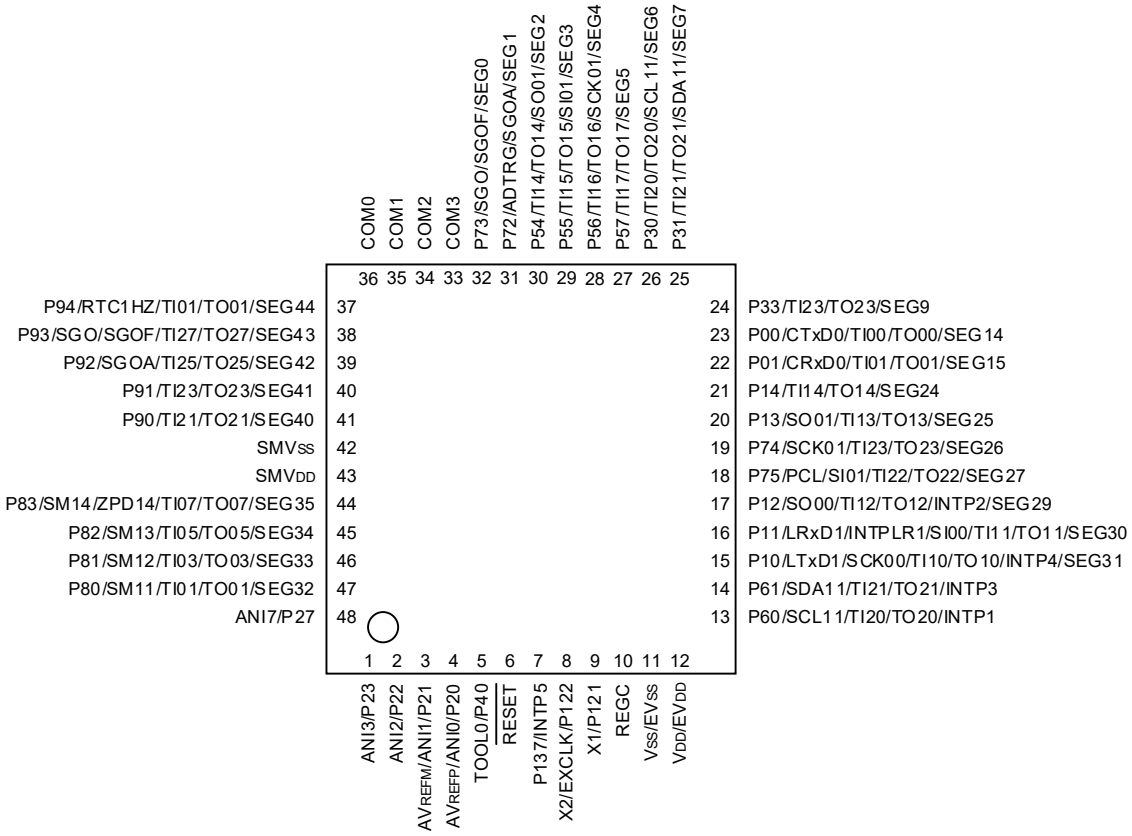


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.2 48-pin products (R5F10DGCxFB, R5F10DGDxFB, R5F10DGExFB: with CAN)

48-pin plastic LQFP (fine pitch) (7 × 7)

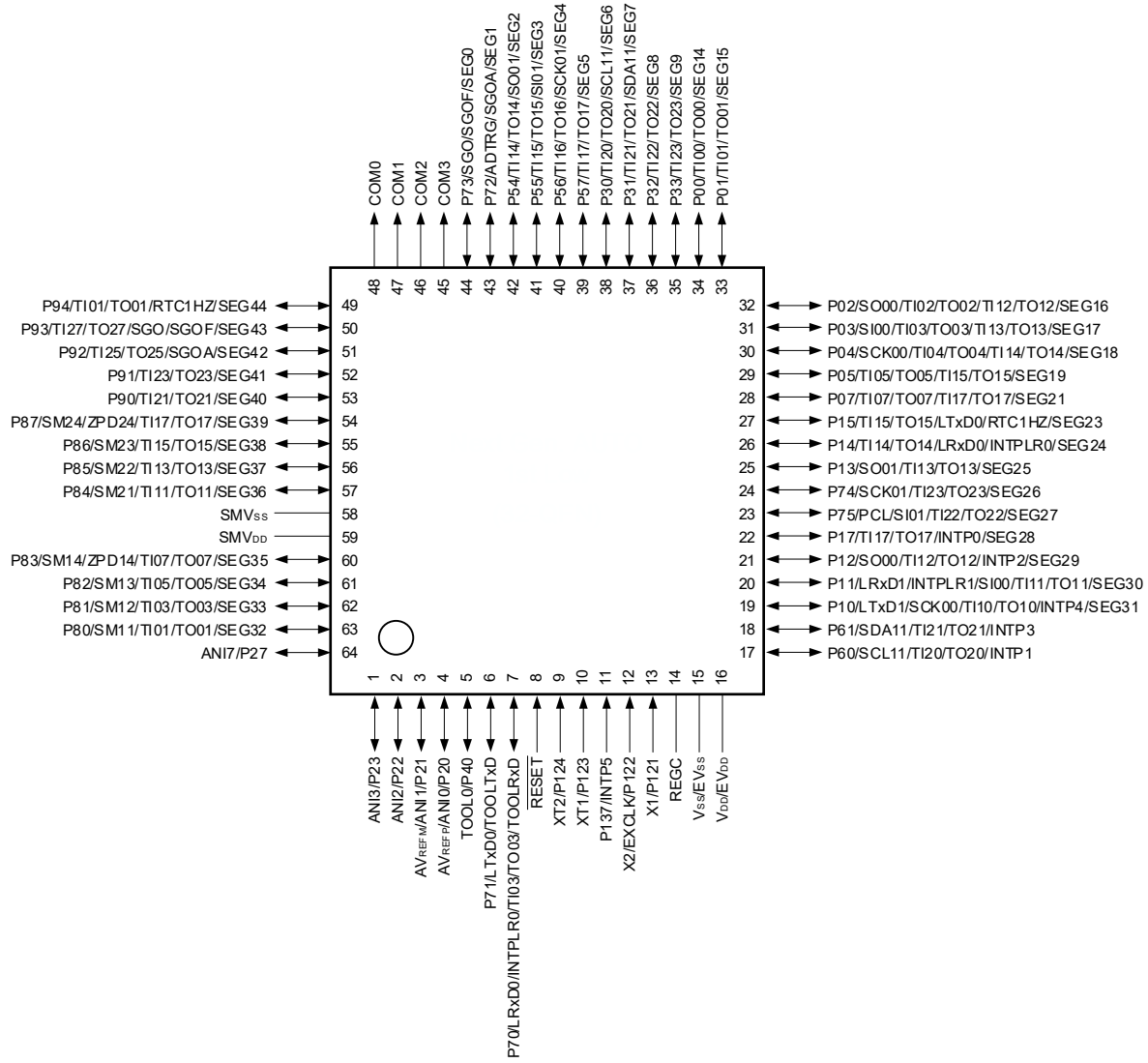


Caution Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.3 64-pin products (R5F10CLDxFB: with no CAN)

64-pin plastic LQFP (fine pitch) (10 × 10)

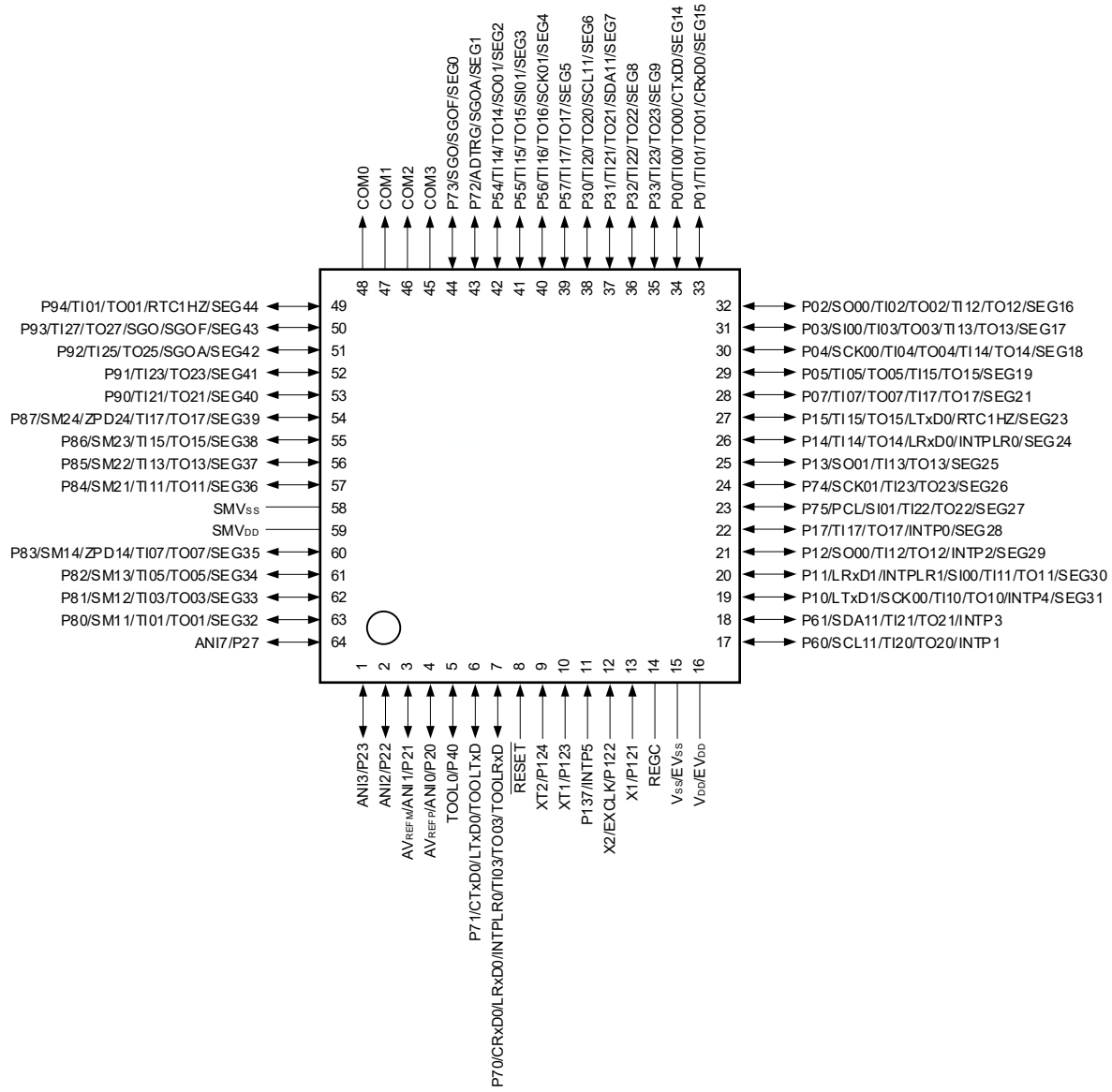


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.4 64-pin products (R5F10DLDxFB, R5F10DLExFB: with CAN)

64-pin plastic LQFP (fine pitch) (10 × 10)

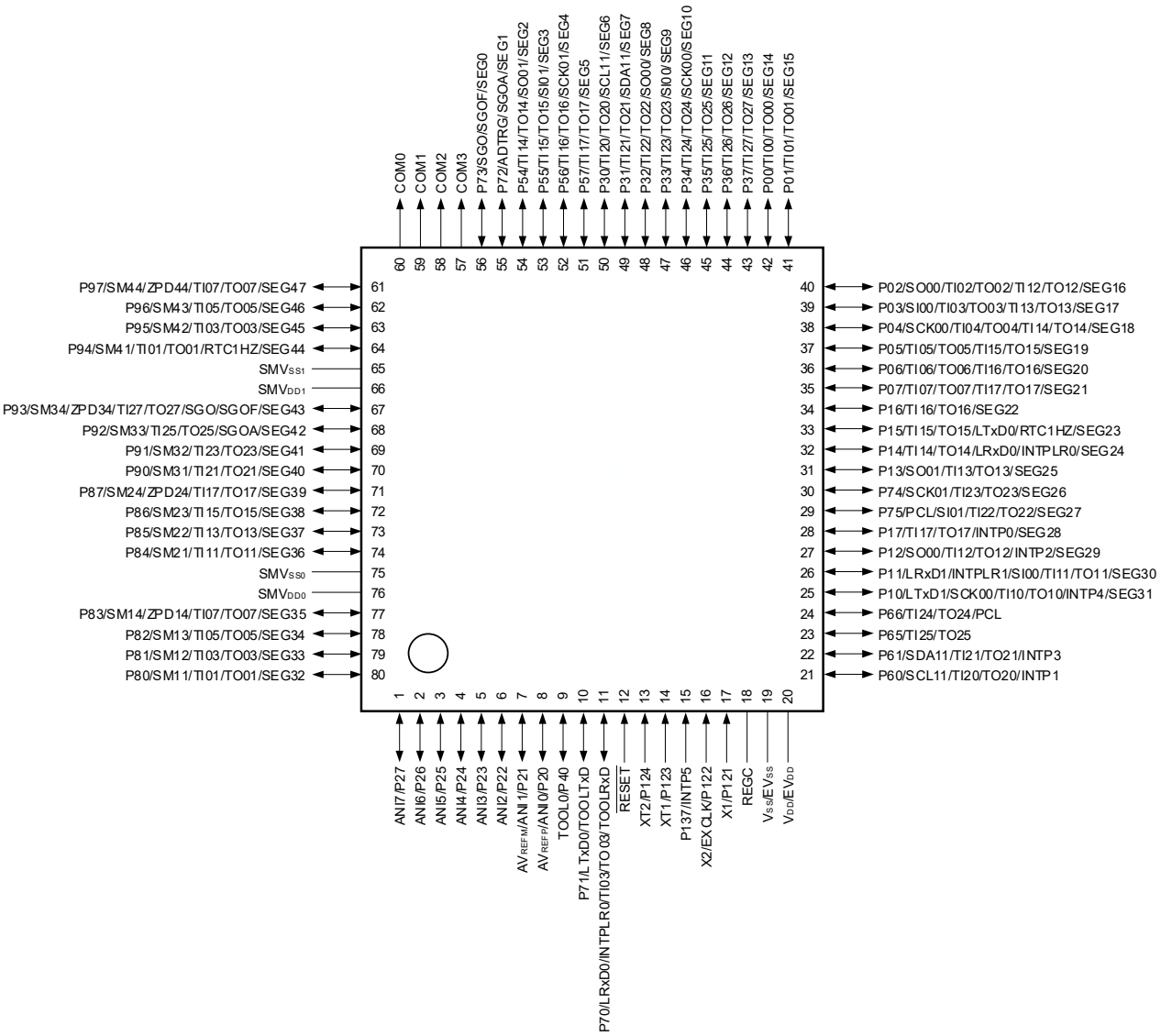


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.5 80-pin products (R5F10CMDxFB, R5F10CMExFB: with no CAN)

80-pin plastic LQFP (fine pitch) (12 × 12)

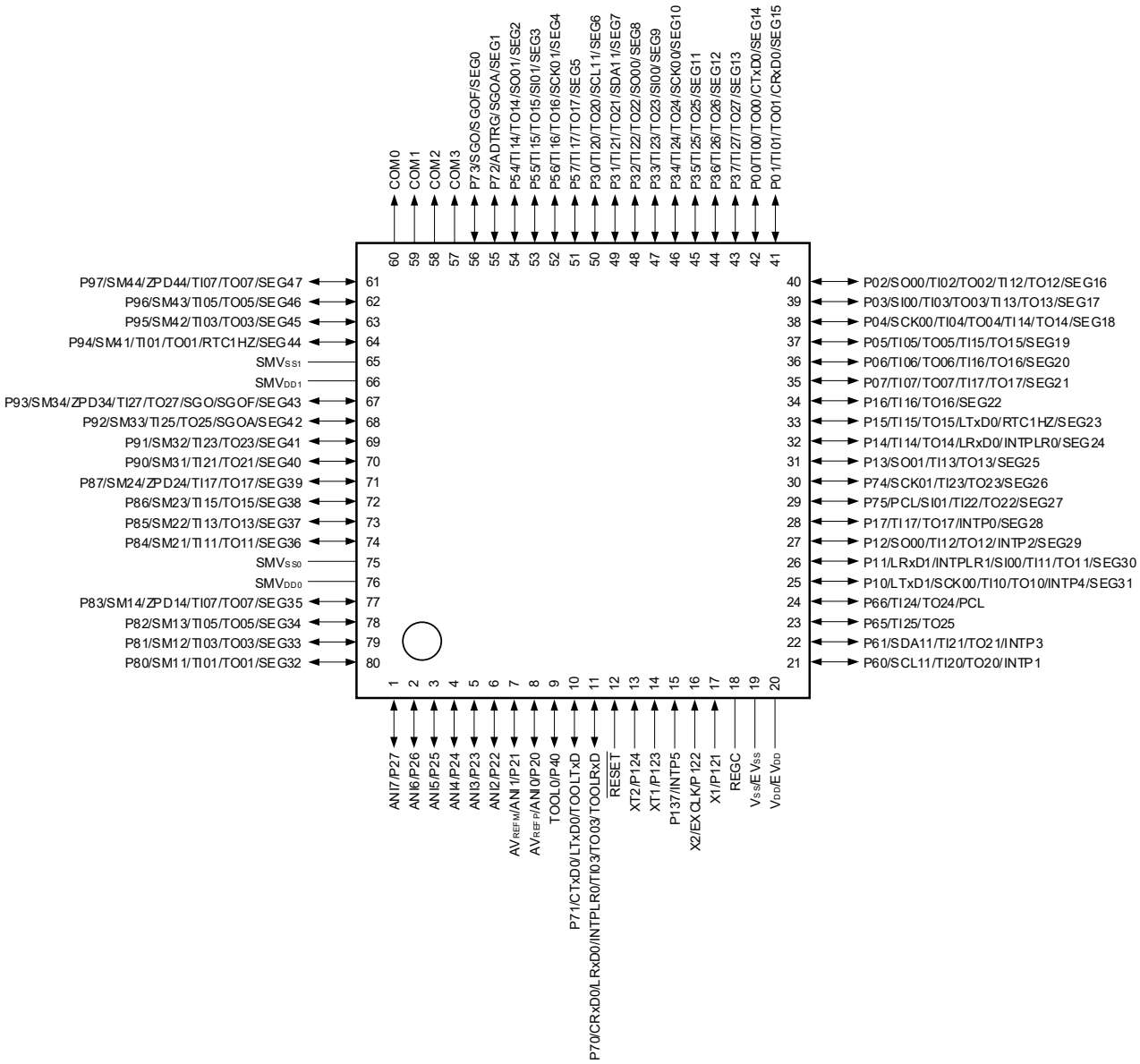


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.6 80-pin products (R5F10DMDxFB, R5F10DMExFB, R5F10DMFxFB, R5F10DMGxFB, R5F10DMJxFB: with CAN)

80-pin plastic LQFP (fine pitch) (12 × 12)

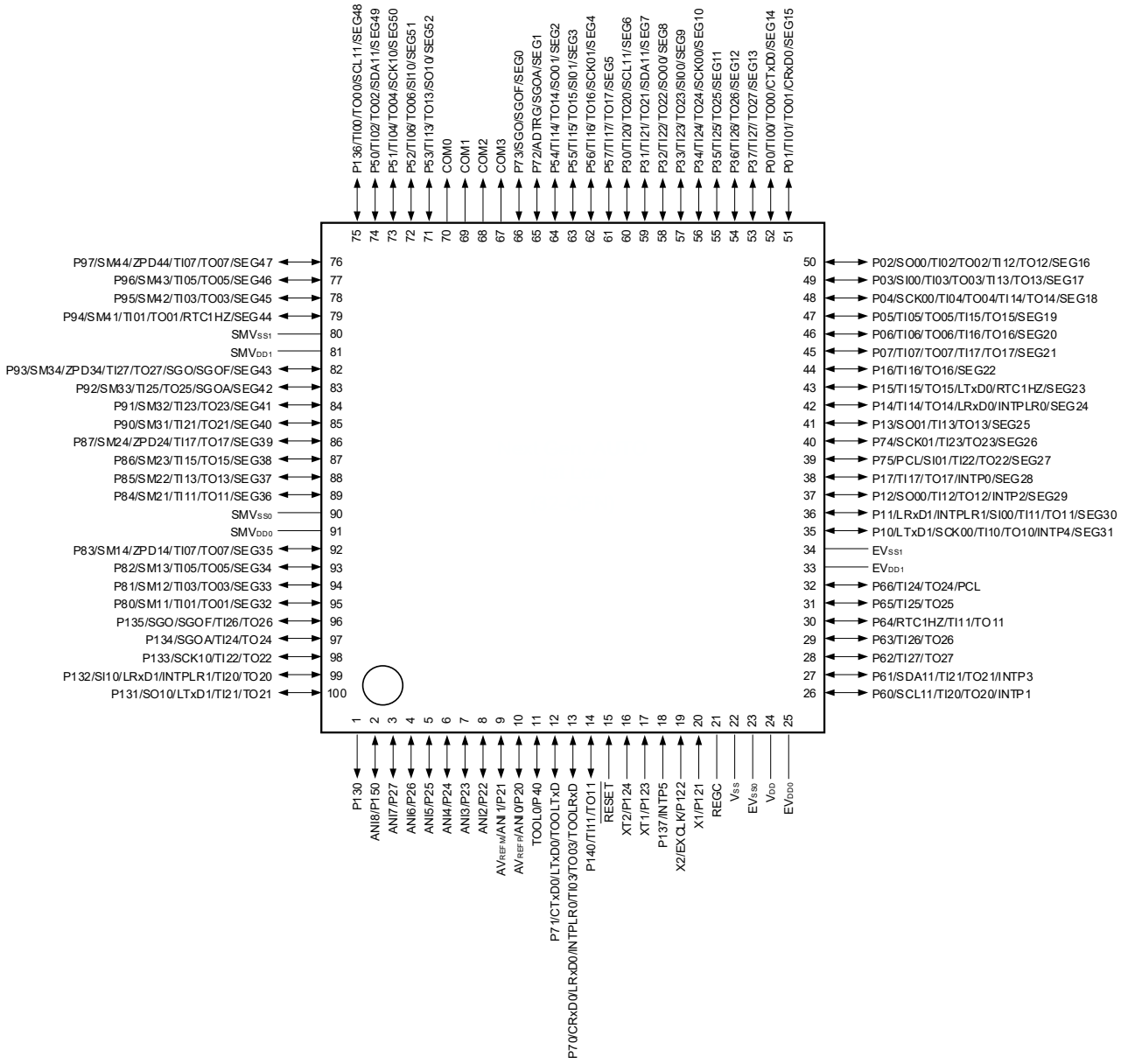


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.7 100-pin products (R5F10DPExFB, R5F10DPFxFB, R5F10DPGxFB, R5F10TPJxFB: with 1 ch of CAN)

100-pin plastic LQFP (fine pitch) (14 × 14)

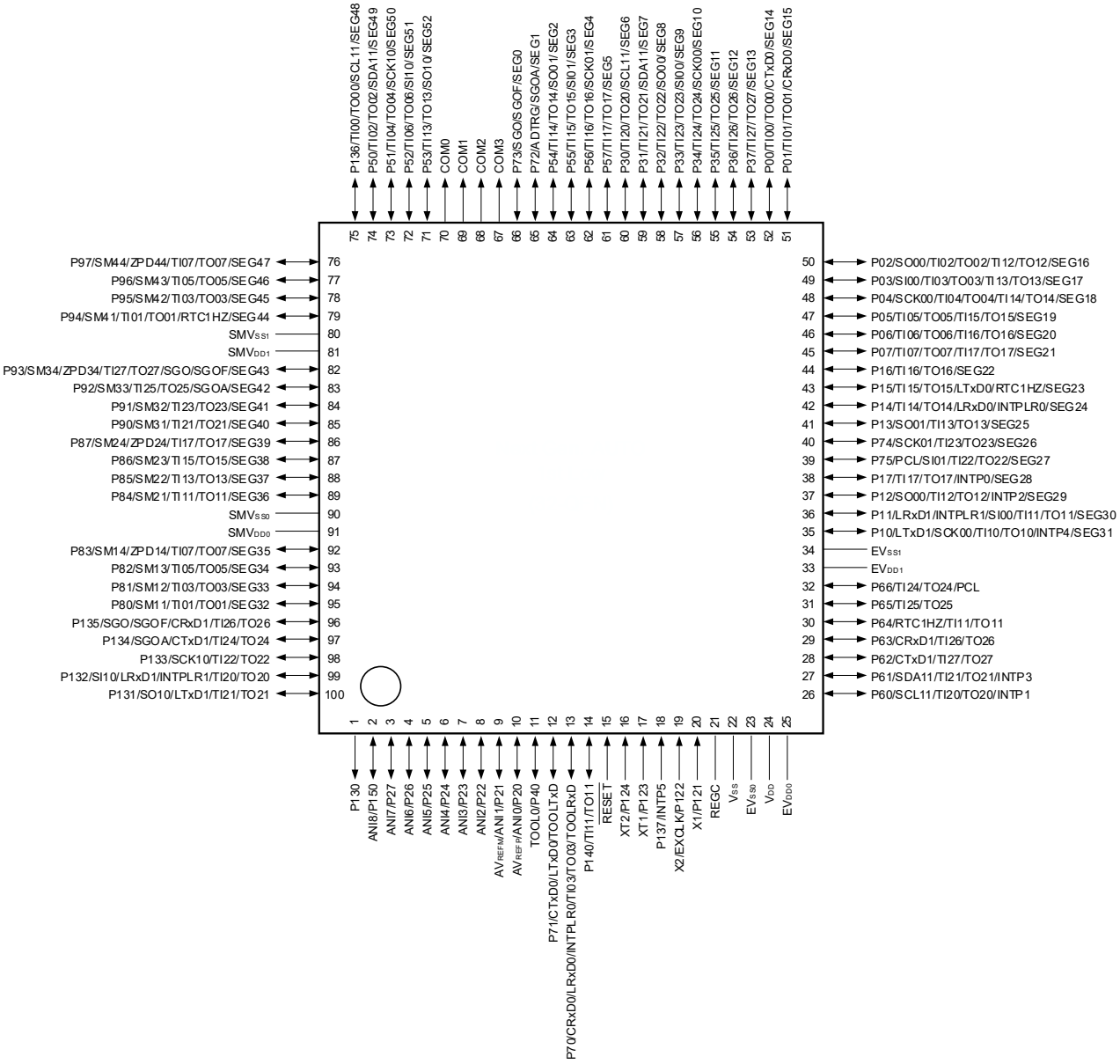


Caution Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.8 100-pin products (R5F10DPJxFB, R5F10DPKxFB, R5F10DPLxFB: with 2 ch of CAN)

100-pin plastic LQFP (fine pitch) (14 × 14)

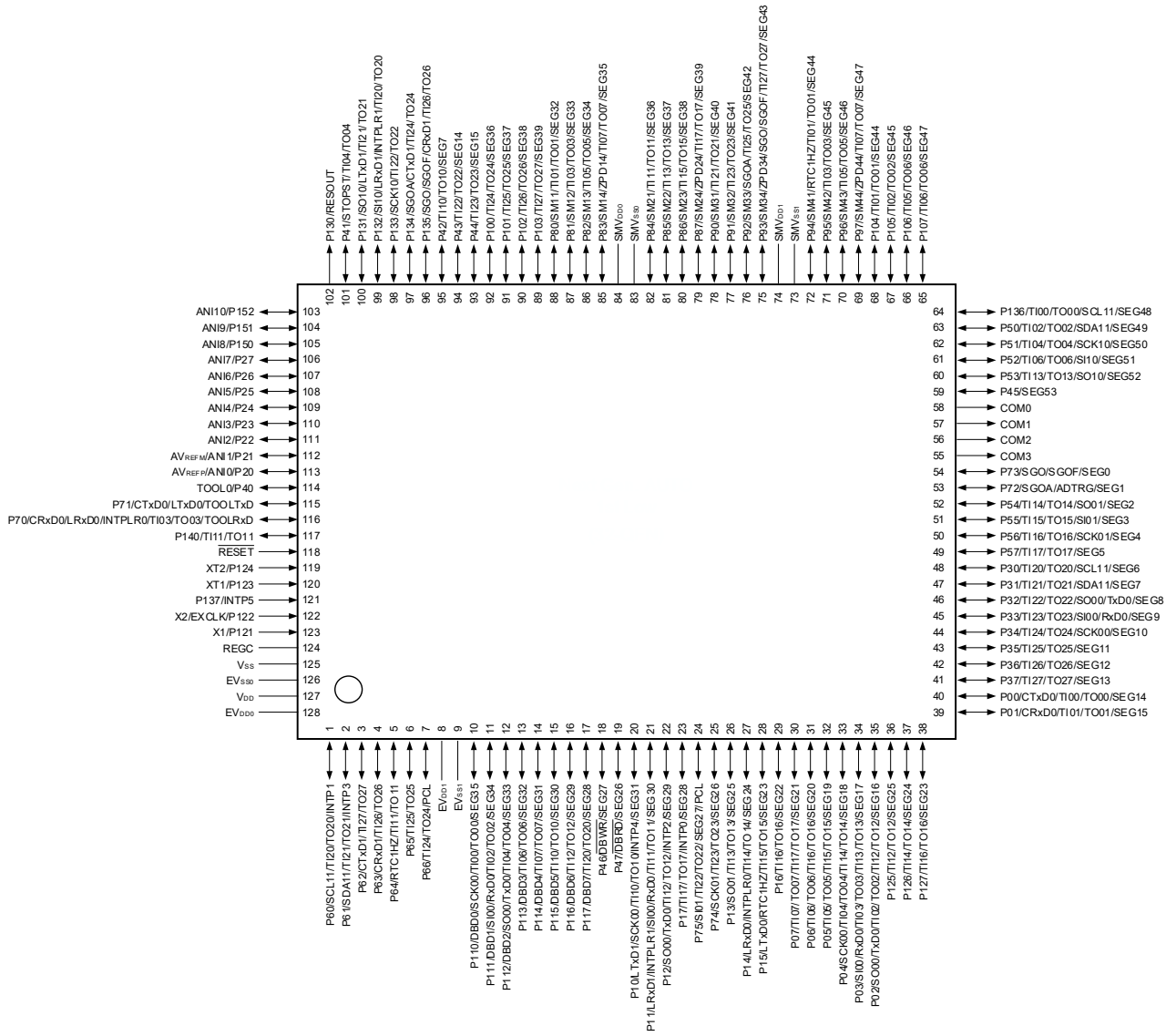


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

Remark For pin identification, see 1.5 Pin Identification.

1.4.9 128-pin products (R5F10DSLxxFB, R5F10DSKxxFB, R5F10DSJxxFB)

128-pin plastic LFQFP (fine pitch) (14 × 20)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF)

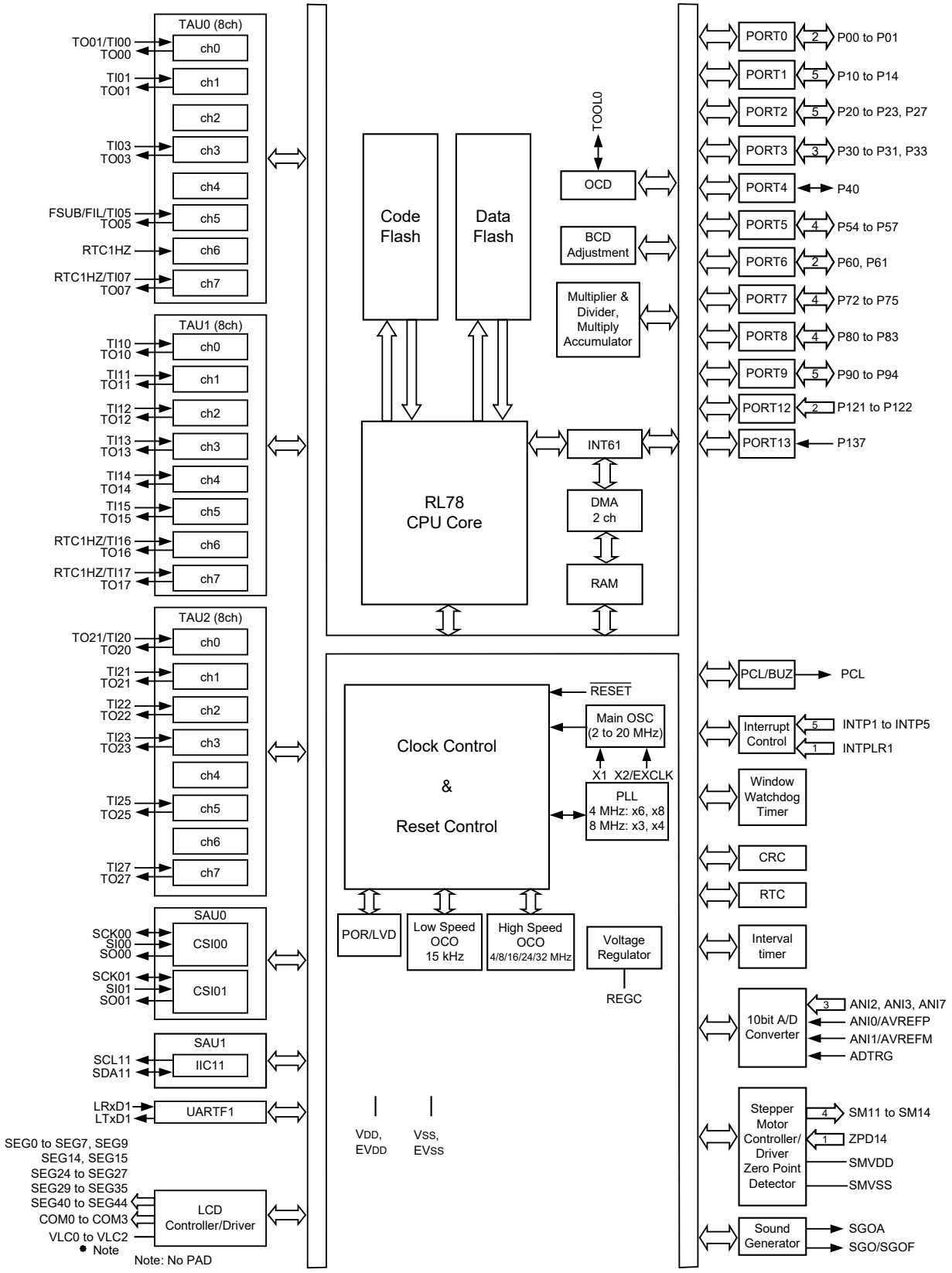
Remark For pin identification, see 1.5 Pin Identification.

1.5 Pin Identification

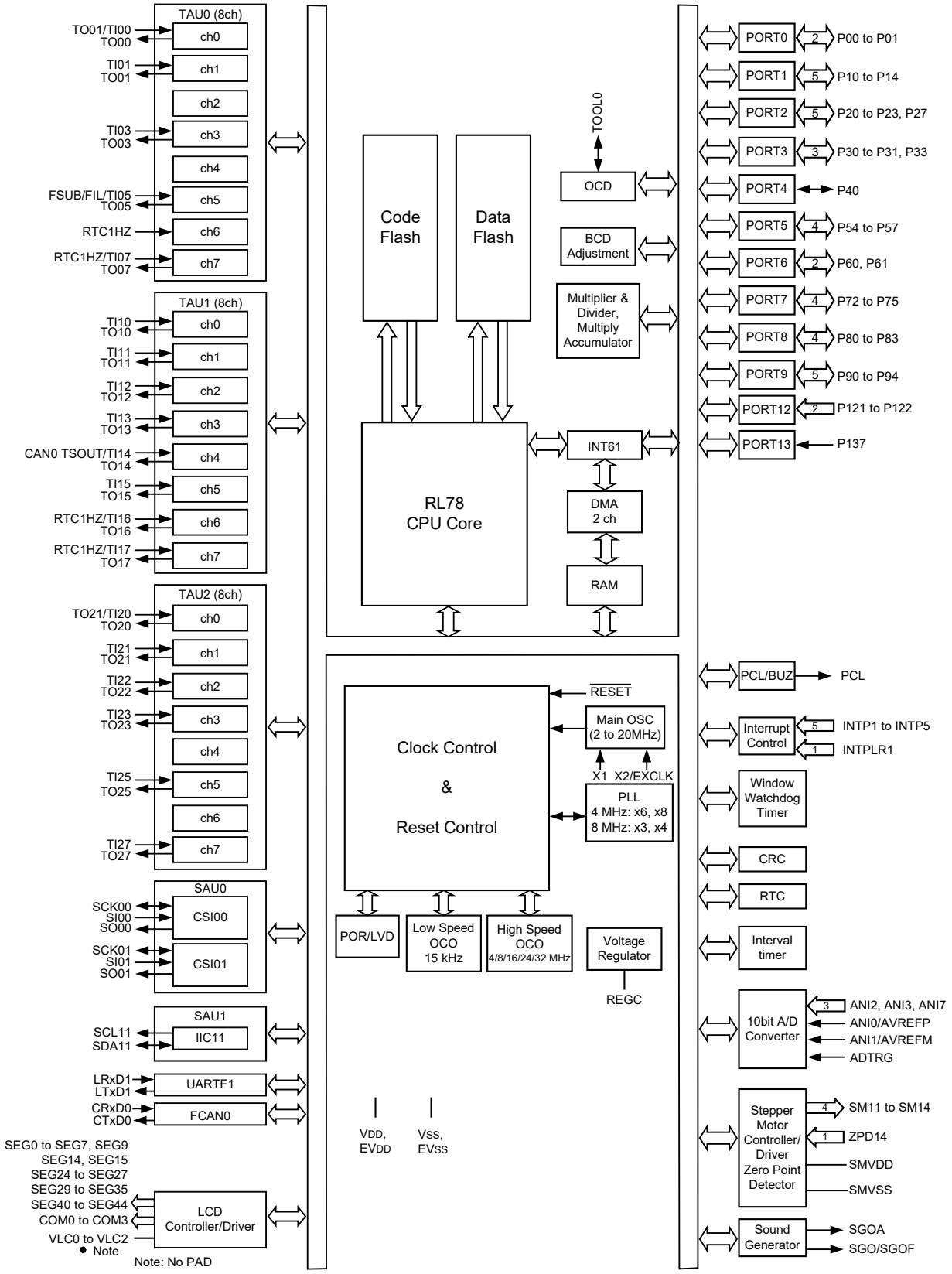
ANI0 to ANI10: Analog input
ADTRG: A/D conversion start trigger external input
AV_{REFM}: A/D converter reference potential (− side) input
AV_{REFP}: A/D converter reference potential (+ side) input
COM0 to COM3: Common output
CRxD0, CRxD1: Receive data for CAN
CTxD0, CTxD1: Transmit data for CAN
DBD0 to DBD7: LCD Bus I/F data lines
$\overline{DBWR}$: LCD Bus I/F write strobe
$\overline{DBRD}$: LCD Bus I/F read strobe
EV_{DD}, EV_{DD0}, EV_{DD1}: Power supply for port
EV_{SS}, EV_{SS0}, EV_{SS1}: Ground for port
EXCLK: External clock input (main system clock)
INTP0 to INTP5: External interrupt input
INTPLR0, INTPLR1: External interrupt input for LIN
LRxD0, LRxD1: Serial data input to LIN
LTxD0, LTxD1: Serial data output from LIN
P00 to P07: Port 0
P10 to P17: Port 1
P20 to P27: Port 2
P30 to P37: Port 3
P40: Port 4
P50 to P57: Port 5
P60 to P66: Port 6
P70 to P75: Port 7
P80 to P87: Port 8
P90 to P97: Port 9
P121 to P124: Port 12
P130 to P137: Port 13
P140: Port 14
P150 to P152: Port 15
PCL: Programmable clock output
REGC: Regulator capacitance
$\overline{RESET}$: Reset
RESOUT: Reset output signal
RTC1HZ: Real-time clock correction clock (1 Hz) output
RxD0: Receive data for UART
SCK00, SCK01, SCK10: Serial clock input/output
SCL11: Serial clock input/output
SDA11: Serial data input/output
SEG0 to SEG53: Segment output
SGO: Sound generator output
SGOA: Sound generator amplitude PWM output
SGOF: Sound generator frequency output
SI00, SI01, SI10: Serial data input
SM11 to SM14, SM21 to SM24, SM31 to SM34, SM41 to SM44: Stepper motor outputs
SMV_{DD}, SMV_{DD0}, SMV_{DD1}: Stepper motor controller/driver supply voltage
SMV_{SS}, SMV_{SS0}, SMV_{SS1}: Stepper motor controller/driver ground
SO00, SO01, SO10: Serial data output
STOPST: STOP status output
TI00 to TI07, TI10 to TI17, TI20 to TI27: Timer input
TO00 to TO07, TO10 to TO17, TO20 to TO27: Timer output
TOOL0: Data input/output for tool
TOOLRxD, TOOLTxD: Data input/output for external device
TxD0: Transmit data for UART
V_{DD}: Power supply
V_{SS}: Ground
X1, X2: Crystal oscillator (Main system clock)
XT1, XT2: Crystal oscillator (Sub system clock)
ZPD14, ZPD24, ZPD34, ZPD44: Zero point detection input

1.6 Block Diagram

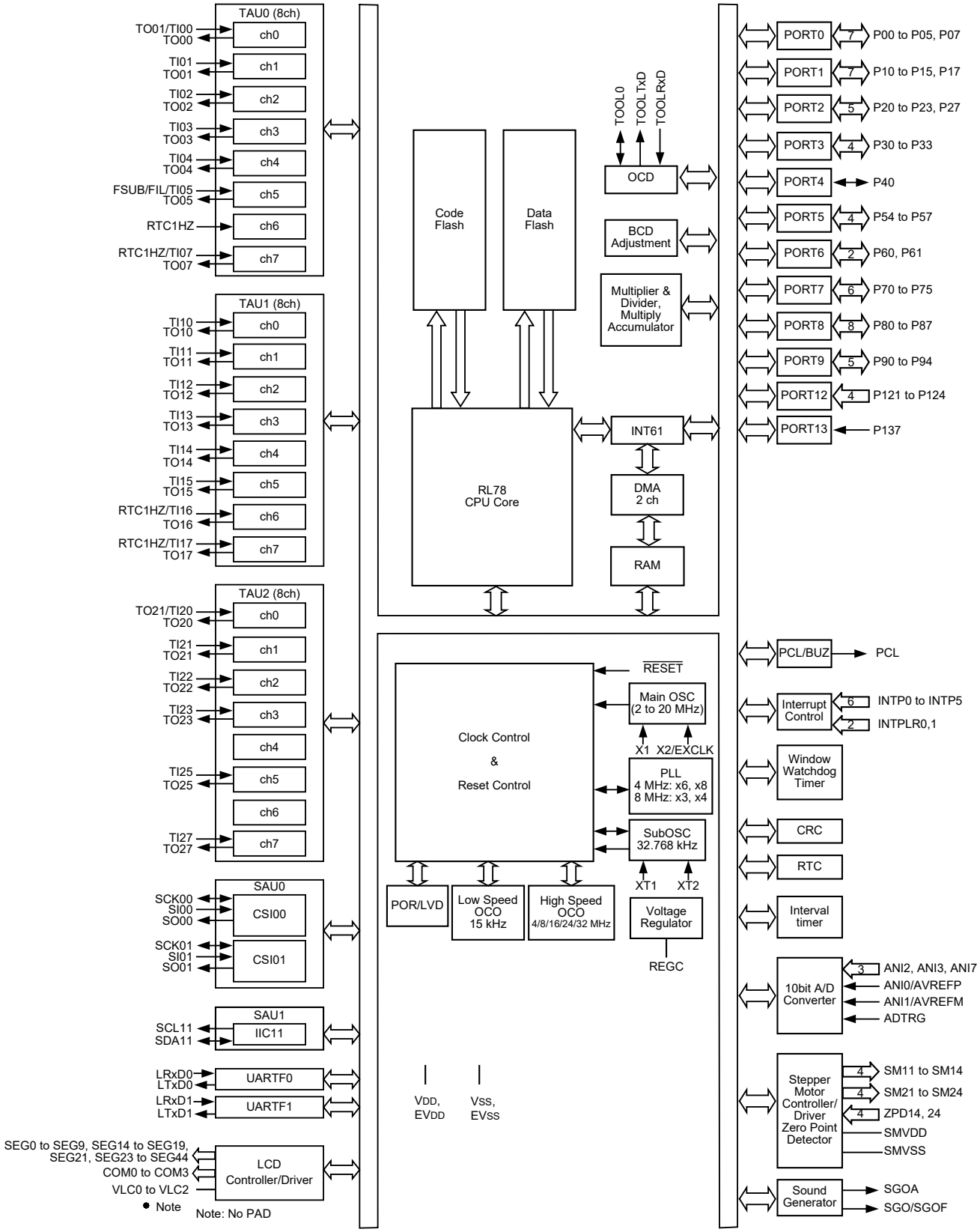
1.6.1 48-pin products (R5F10CGBxFB, R5F10CGCxFB, R5F10CGDxFB: with no CAN)



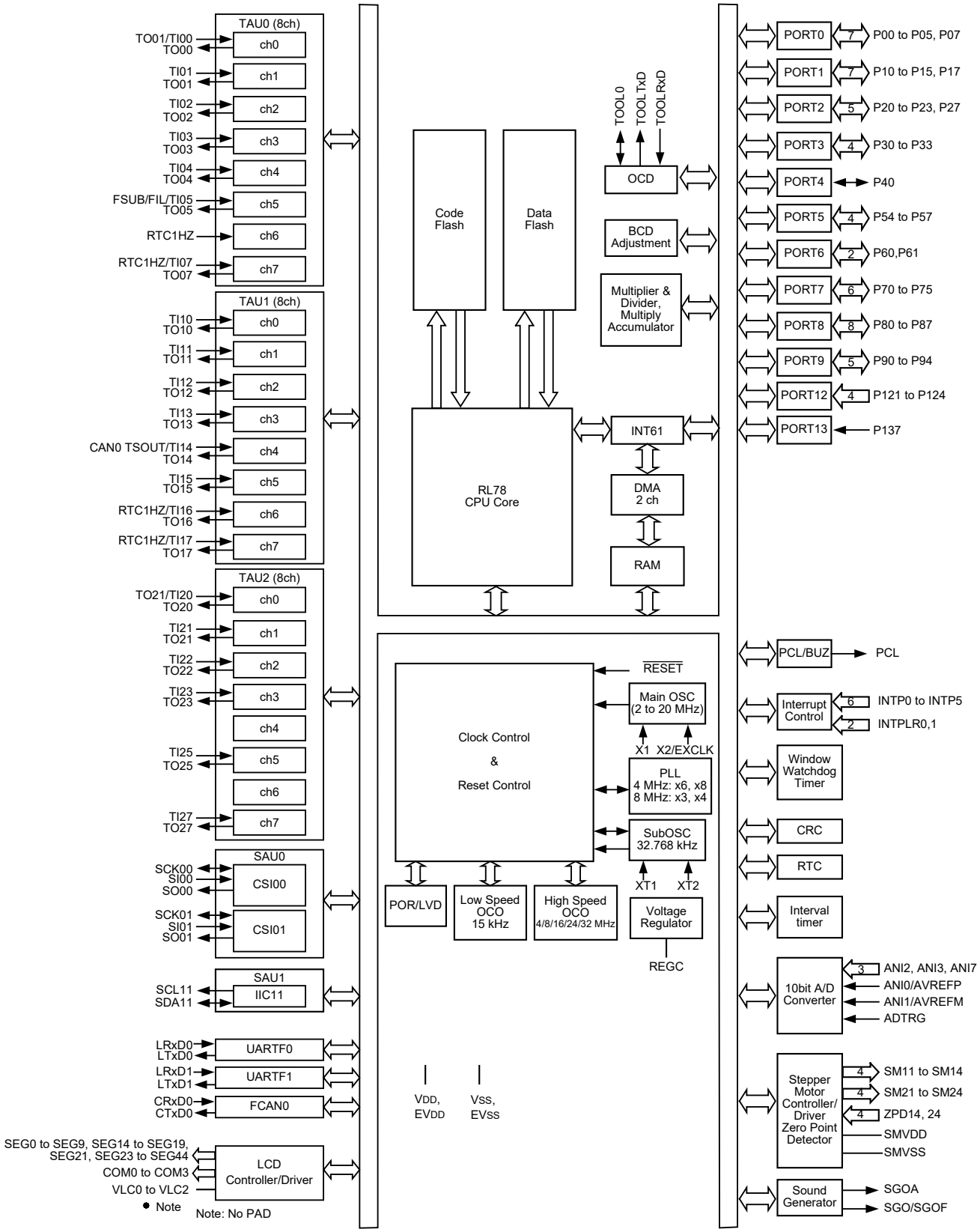
1.6.2 48-pin products (R5F10DGCxFB, R5F10DGDxFB, R5F10DGExFB: with CAN)



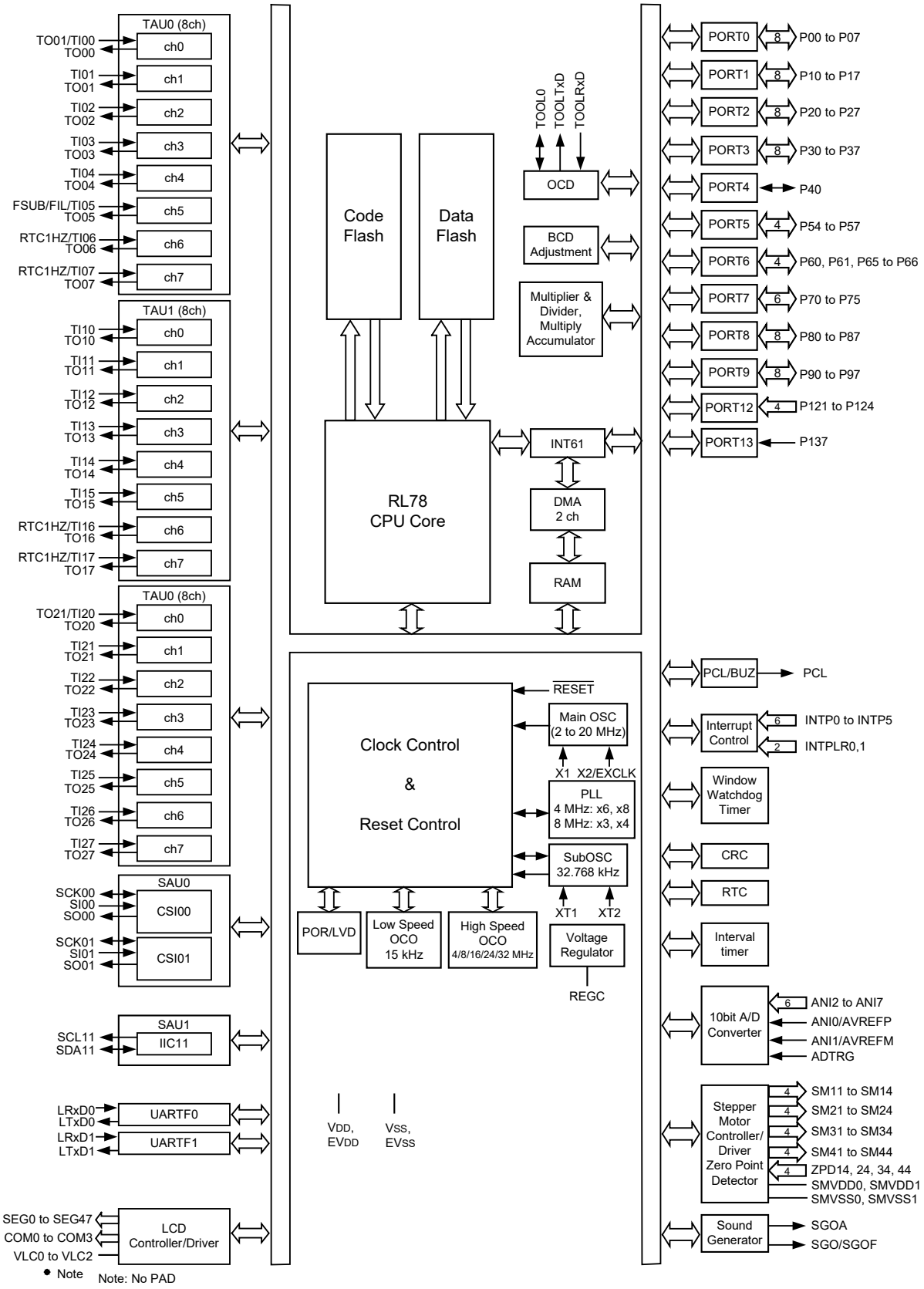
1.6.3 64-pin products (R5F10CLDxFB: with no CAN)



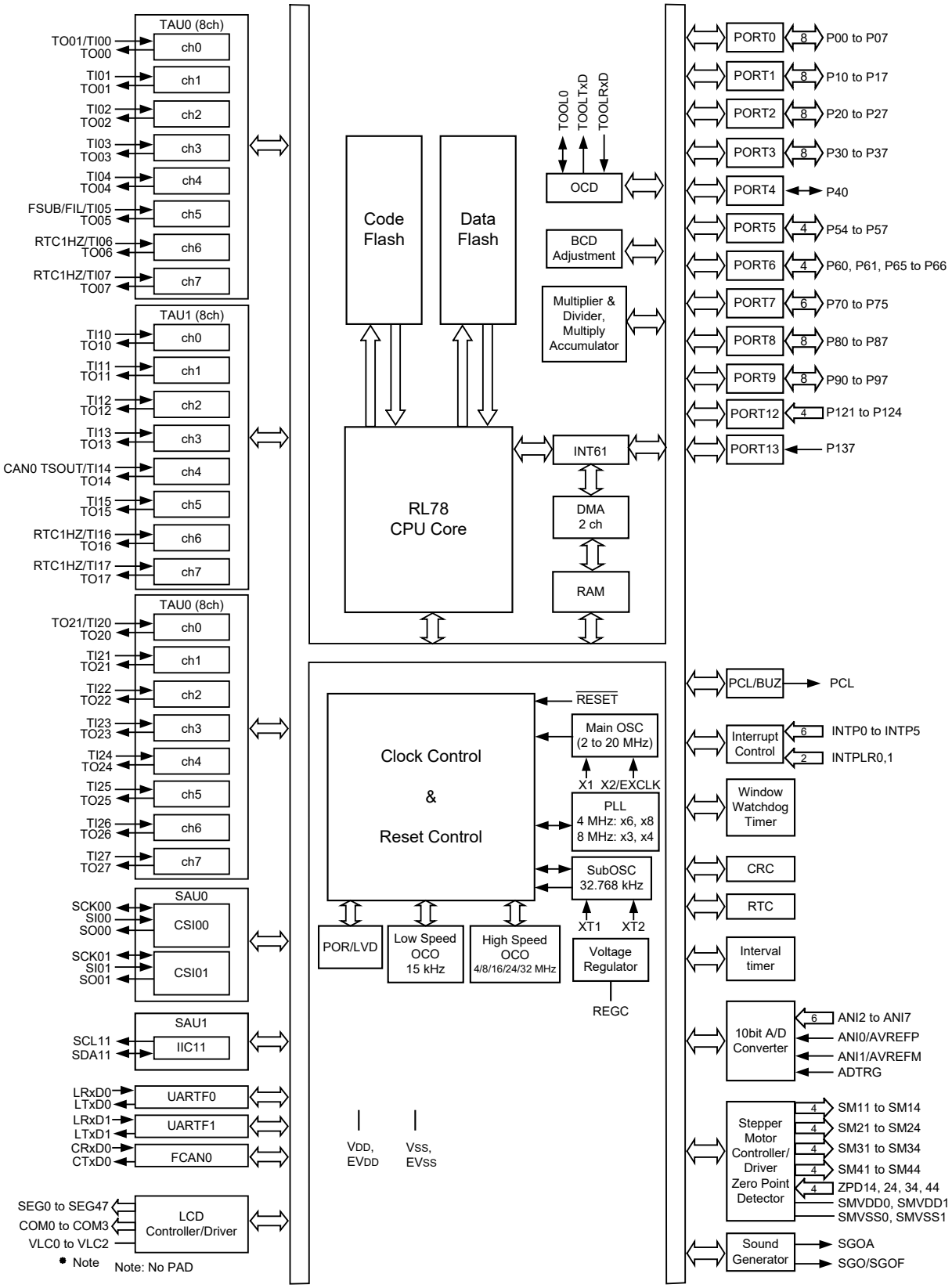
1.6.4 64-pin products (R5F10DLDxFB, R5F10DLExFB: with CAN)



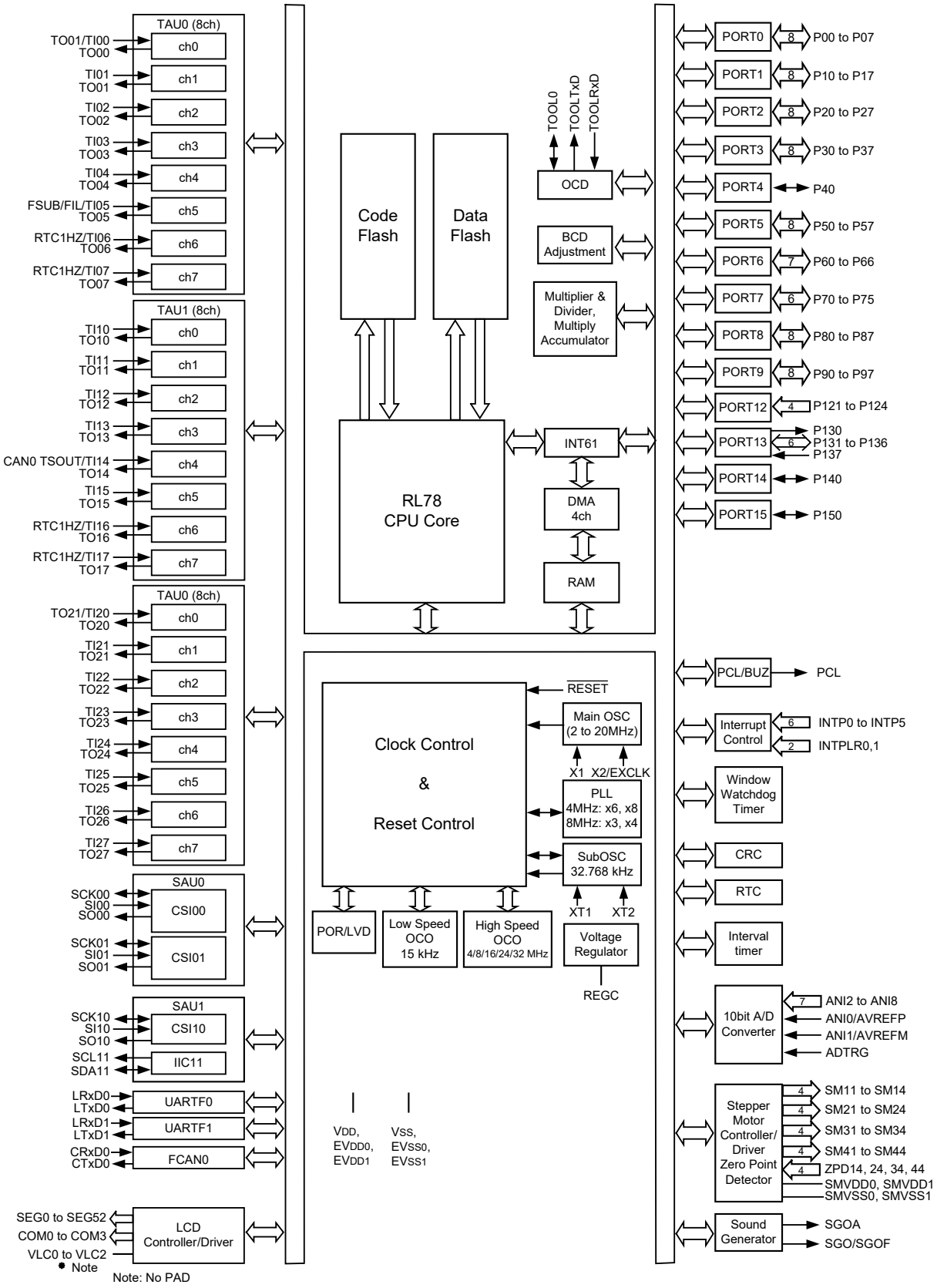
1.6.5 80-pin products (R5F10CMDxFB, R5F10CMExFB: with no CAN)



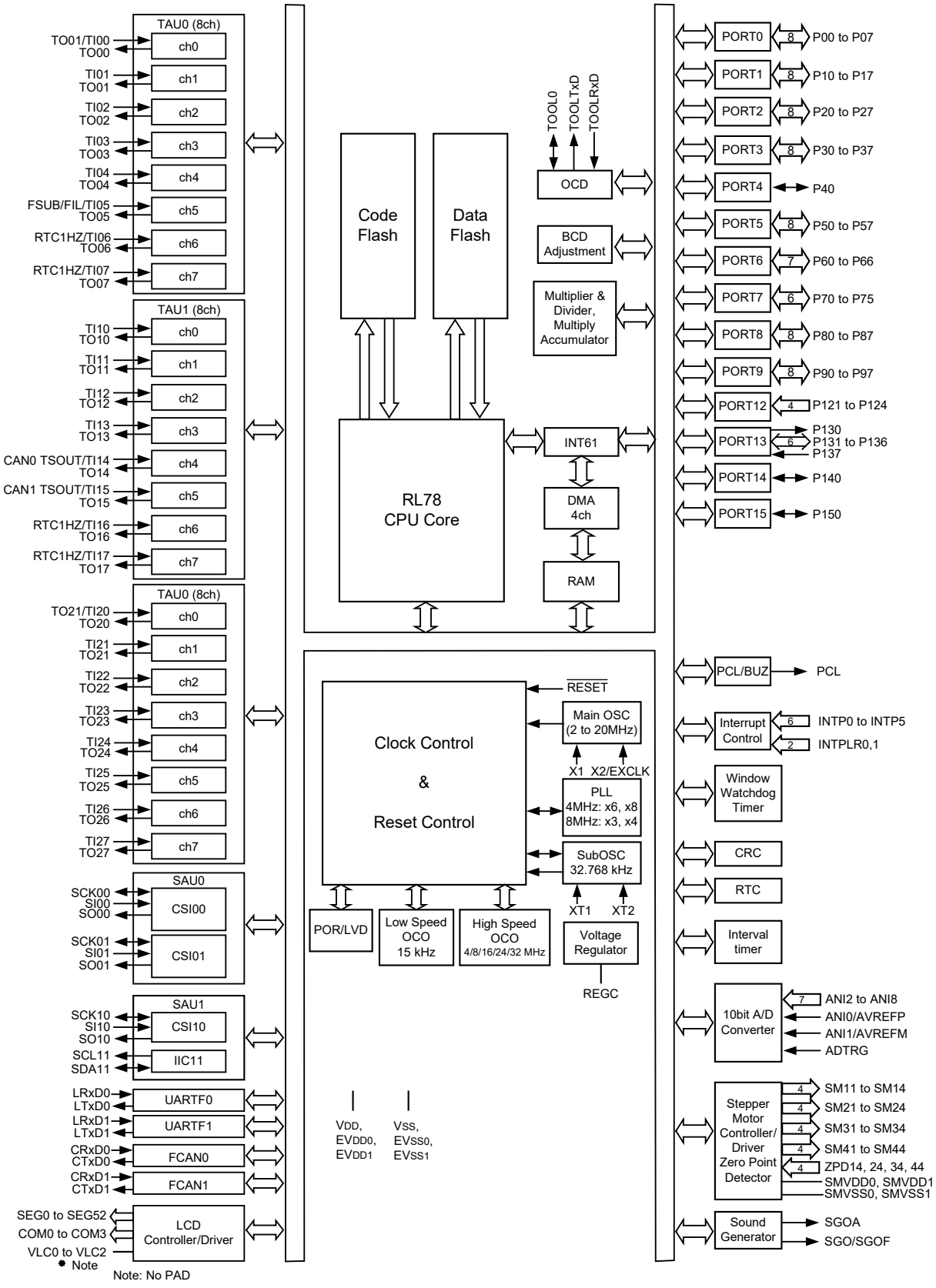
1.6.6 80-pin products (R5F10DMDxFB, R5F10DMExFB, R5F10DMFxFB, R5F10DMGxFB, R5F10DMJxFB: with CAN)



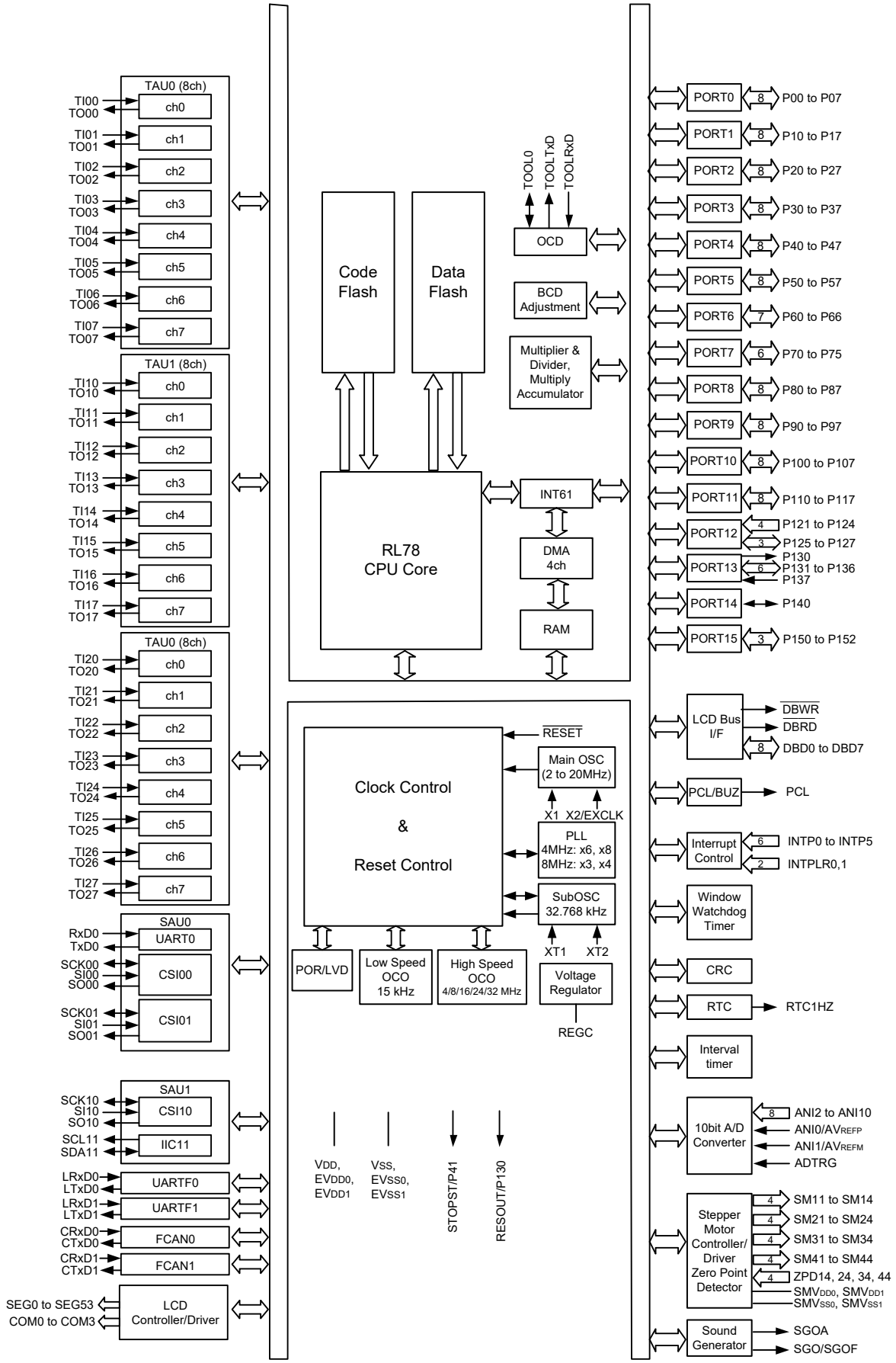
1.6.7 100-pin products (R5F10DPExFB, R5F10DPFxFB, R5F10DPGxFB, R5F10TPJxFB: with 1 ch of CAN)



1.6.8 100-pin products (R5F10DPJxFB, R5F10DPKxFB, R5F10DPLxFB: with 2 ch of CAN)



1.6.9 128-pin products (R5F10DSJxFB, R5F10DSKxFB, R5F10DSLxFB)



1.7 Outline of Functions

(1/4)

Item			48-pin						64-pin			80-pin						
	ROM	RAM	R5F10CGBxFB	R5F10CGCxFB	R5F10CGDxFB	R5F10DGCxFB	R5F10DGDxFB	R5F10DGExFB	R5F10CLDxFB	R5F10DLDxFB	R5F10DLExFB	R5F10CMDxFB	R5F10CMExFB	R5F10DMDxFB	R5F10DMExFB	R5F10DMFxFB	R5F10DMGxFB	R5F10DMJxFB
ROM/ RAM capacities	512 KB	24 KB																
	384 KB	20 KB																
	256 KB	16 KB																√
	128 KB	8 KB															√	
	96 KB	6 KB														√		
	64 KB	4 KB						√			√		√		√			
	48 KB	3 KB			√		√		√	√		√		√				
	32 KB	2 KB		√		√												
	24 KB	2 KB	√															
Data flash memory			8 KB															
Memory space			1 MB															
General-purpose register			8 bits × 32 registers (8 bits × 8 registers × 4 banks)															
Main System clock	High-speed system clock		1 to 20 MHz (VDD = 2.7 V to 5.5 V)															
	High-speed on-chip oscillation clock		4/8/16/24/32 MHz (T_A = -40 to 85°C) 4/8/16/24 MHz (T_A = -40 to 105°C)															
PLL			4 MHz × 16/2 = 32 MHz, 8 MHz × 16/4 = 32 MHz (T_A= -40 to 85°C) 4 MHz × 12/2 = 24 MHz, 8 MHz × 12/4 = 24 MHz (T_A= -40 to 105°C)															
Subsystem clock			32.768kHz															
Low-speed on-chip oscillation clock			15 kHz															
Minimum instruction execution time			0.03125 μs (Main system clock 32 MHz T_A = -40 to +85°C) 0.04167 μs (Main system clock 24 MHz T_A = -40 to 105°C) 30.5 μs (Subsystem clock 32.768 kHz operation)															
Instruction set			• 8-bit operation,16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.															
I/O port	Total number of port		38						54			68						
	CMOS I/O port		35						49			63						
		N-ch open-drain Selectable port	4															
		LED direct drive port	9						13			16						
	CMOS input port		3						5									
	CMOS output port		0															
Timer	16-bit timer		8 ch × 3 units															
	Real-time clock (RTC)		1 ch															
	Interval timer		1 ch															
	Watchdog timer (WDT)		1 ch															
	Timer output		19						21			24						
	RTC output		1															
Clock output/buzzer output			1															
10-bit resolution A/D converter			3+2									6+2						

(2/4)

Item		48-pin						64-pin			80-pin						
		R5F10CGBxFB	R5F10CGCxFB	R5F10CGDxFB	R5F10DGCxFB	R5F10DGDxFB	R5F10DGExFB	R5F10CLDxFB	R5F10DLDxFB	R5F10DLExFB	R5F10CMDxFB	R5F10CMExFB	R5F10DMDxFB	R5F10DMExFB	R5F10DMFxFB	R5F10DMGxFB	R5F10DMJxFB
Serial interface	CSI	2 ch															
	UART	–															
	Simplified IIC	1 ch															
	LIN-UART	1 ch						2 ch									
	aFCAN	0 ch			1 ch			0 ch		1 ch		0 ch			1 ch		
Multiplier and divider/multiply accumulator		• 16-bits × 16 bits = 32 bits (Unsigned or signed) • 32-bits ÷ 32 bits = 32 bits (Unsigned) • 16-bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)															
DMA controller		2 ch															
Vectored interrupt sources	Internal	39			43			42		46		42			46		
	External	6						8									
	Software	1															
	Debugger	1															
LCD controller driver	Bias	Static, 1/3 bias, 1/3 or 1/4 duty															
	SEG × COM	27 × 4						39 × 4			48 × 4						
Sound generator		1 channel															
Stepper motor controller/driver (with ZPD)		1 ch						2 ch			4 ch						
Safety function	FLASH memory CRC calculation	Provided															
	RAM parity bit error detection	Provided															
	Illegal-memory access detection	Provided															
	Frequency detection	Provided															
	Clock monitor	Provided															
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution • Internal reset by RAM parity error • Internal reset by illegal-memory access • Internal reset by clock monitor															
Power on reset (POR)		Power on reset: 1.51 V ± 0.06 V Power down reset: 1.50 V ± 0.06 V															
Voltage detector		Rising edge detection voltage = 2.81 to 4.06 V (6 step) Falling edge detection voltage = 2.75 to 3.98 V (6 step)															
On-chip debug function		Provided															
Power supply voltage		V_{DD} = 2.7 to 5.5 V															
Operating ambient temperature		J grade products:T_A = -40 to +85 °C, L grade products: T_A = -40 to +105 °C															

(3/4)

Item			100-pin							128-pin		
	ROM	RAM	R5F10DPExFB	R5F10DPFxFB	R5F10DPGxFB	R5F10TPJxFB	R5F10DPJxFB	R5F10DPKxFB	R5F10DPLxFB	R5F10DSJxFB	R5F10DSKxFB	R5F10DSLxFB
ROM/ RAM capacities	512 KB	24 KB							√			√
	384 KB	20 KB						√			√	
	256 KB	16 KB				√	√			√		
	128 KB	8 KB			√							
	96 KB	6 KB		√								
	64 KB	4 KB	√									
	48 KB	3 KB										
	32 KB	2 KB										
	24 KB	2 KB										
Data flash memory			8 KB									
Memory space			1 MB									
General-purpose register			8 bits × 32 registers (8 bits × 8 registers × 4 banks)									
Main System clock	High-speed system clock		1 to 20 MHz (VDD = 2.7 V to 5.5 V)									
	High-speed on-chip oscillation clock		4/8/16/24/32 MHz (T_A = -40 to 85°C) 4/8/16/24 MHz (T_A = -40 to 105°C)									
PLL			4 MHz × 16/2 = 32 MHz, 8 MHz × 16/4 = 32 MHz (T_A= -40 to 85°C) 4 MHz × 12/2 = 24 MHz, 8 MHz × 12/4 = 24 MHz (T_A= -40 to 105°C)									
Subsystem clock			32.768kHz									
Low-speed on-chip oscillation clock			15 kHz									
Minimum instruction execution time			0.03125 μs (Main system clock 32 MHz T_A = -40 to +85°C) 0.04167 μs (Main system clock 24 MHz T_A = -40 to 105°C) 30.5 μs (Subsystem clock 32.768 kHz operation)									
Instruction set			• 8-bit operation,16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.									
I/O port	Total number of port		84							112		
	CMOS I/O port		78							107		
		N-ch open-drain Selectable port	6									
		LED direct drive port	16									
	CMOS input port		5									
	CMOS output port		1									
Timer	16-bit timer		8 ch × 3 units									
	Real-time clock (RTC)		1 ch									
	Interval timer		1 ch									
	Watchdog timer (WDT)		1 ch									
	Timer output		24									
	RTC output		1									
Clock output/buzzer output			1									
10-bit resolution A/D converter			7+2							9+2		
Reset output			Can be output from P130									
STOP status output			Can be output from P41									

(4/4)

Item		100-pin							128-pin		
		R5F10DPExFB	R5F10DPFxFB	R5F10DPGxFB	R5F10TPJxFB	R5F10DPJxFB	R5F10DPKxFB	R5F10DPLxFB	R5F10DSJxFB	R5F10DSKxFB	R5F10DSLxFB
Serial interface	CSI	3 ch									
	UART	–							1 ch		
	Simplified IIC	1 ch									
	LIN-UART	2 ch									
	aFCAN	1 ch				2 ch					
Multiplier and divider/multiply accumulator		• 16-bits × 16 bits = 32 bits (Unsigned or signed) • 32-bits ÷ 32 bits = 32 bits (Unsigned) • 16-bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		4 ch									
Vectored interrupt sources	Internal	53									
	External	8									
	Software	1									
	Debugger	1									
LCD controller driver	Bias	Static, 1/3 bias, 1/3 or 1/4 duty									
	SEG × COM	53 × 4							54 × 4		
LCD Bus I/F		–							Provided (8 bit, RD, WR)		
Sound generator		1 channel									
Stepper motor controller/driver (with ZPD)		4 ch									
Safety function	FLASH memory CRC calculation	Provided									
	RAM parity bit error detection	Provided									
	Illegal-memory access detection	Provided									
	Frequency detection	Provided									
	Clock monitor	Provided									
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution • Internal reset by RAM parity error • Internal reset by illegal-memory access • Internal reset by clock monitor									
Power on reset (POR)		Power on reset: 1.51 V ± 0.06 V Power down reset: 1.50 V ± 0.06 V									
Voltage detector		Rising edge detection voltage = 2.81 to 4.06 V (6 step) Falling edge detection voltage = 2.75 to 3.98 V (6 step)									
On-chip debug function		Provided									
Power supply voltage		V_{DD} = 2.7 to 5.5 V									
Operating ambient temperature		J grade products:T_A = -40 to +85 °C, L grade products: T_A = -40 to +105 °C									

2. PIN FUNCTIONS

2.1 Pin Function List

Pin I/O buffer power supplies depend on the product. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

(1) 48-pin products

Power Supply	Corresponding Pins
V_{DD}/EV_{DD}	Port pins other than P80 to P83 and P90 to P94
SMV_{DD}	P80 to P83, P90 to P94

(2) 64-pin products

Power Supply	Corresponding Pins
V_{DD}/EV_{DD}	Port pins other than P80 to P87and P90 to P94
SMV_{DD}	P80 to P87, P90 to P94

(3) 80-pin products

Power Supply	Corresponding Pins
V_{DD}/EV_{DD}	Port pins other than P80 to P87 and P90 to P97
SMV_{DD0}, SMV_{DD1}	P80 to P87, P90 to P97

(4) 100-pin products

Power Supply	Corresponding Pins
V_{DD}	P20 to P27, P150, P137, P121 to P124, $\overline{\text{RESET}}$
EV_{DD0}, EV_{DD1}	P00 to P07, P10 to P17, P30 to P37, P40, P50 to P57, P60 to P66, P70 to P75, P130 to P136, P140
SMV_{DD0}, SMV_{DD1}	P80 to P87, P90 to P97

(5) 128-pin products

Power Supply	Corresponding Pins
V_{DD}	P20 to P27, P150 to P152, P137, P121 to P124, $\overline{\text{RESET}}$
EV_{DD0}, EV_{DD1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P66, P70 to P75, P100 to P107, P110 to P117, P125 to P127, P130 to P136, and P140
SMV_{DD0}, SMV_{DD1}	P80 to P87, P90 to P97

The setting of I/O, buffer and pull-up resistor in each port is also valid for alternate functions.

2.1.1 48-pin products

Table 2-2. Port Pins for R5F10CGBxFB, R5F10CGCxFB, R5F10CGDxFB, R5F10DGCxFB, R5F10DGDxFB, R5F10DGExFB (1/2)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input of P01 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI00/TO00/CTxD0/SEG14[Note1]
P01					TI01/TO01/CRxD0/SEG15[Note1]
P10	I/O	Port 1. 5-bit I/O port. Input of P10 and P11 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	LTxD1/SCK00/TI10/TO10/INTP4/SEG31
P11					LRxD1/INTPLR1/SI00/TI11/TO11/SEG30
P12					SO00/TI12/TO12/INTP2/SEG29
P13					SO01/TI13/TO13/SEG25
P14					TI14/TO14/SEG24
P20	I/O	Port 2. 5-bit I/O port. Can be set to analog input [Note2] Input/output can be specified in 1-bit units.	HZ	Analog Input	AVREFP/ANI0
P21					AVREFM/ANI1
P22					ANI2
P23					ANI3
P27					ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 can be set to schmitt 1 input buffer. Output of P30 and P31 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI20/TO20/SCL11/SEG6
P31					TI21/TO21/SDA11/SEG7
P33					TI23/TO23/SEG9
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: HZ Int.: PU	Input	TOOL0
P54	I/O	Port 5. 4-bit I/O port. Input of P55 to P57 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI14/TO14/SO01/SEG2
P55					TI15/TO15/SI01/SEG3
P56					TI16/TO16/SCK01/SEG4
P57					TI17/TO17/SEG5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset, PD: Pull down, PU: Pull up, HZ: High impedance

Notes 1. CTxD0 and CRxD0 are not provided for R5F10CGDxFB, R5F10CGCxFB and R5F10CGBxFB with no CAN channel.

2. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

Table 2-2. Port Pins for
R5F10CGBxFB, R5F10CGCxFB, R5F10CGDxFB, R5F10DGCxFB, R5F10DGDxFB, R5F10DGExFB (2/2)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P60	I/O	Port 6. 2-bit I/O port. Input of P61 can be set to schmitt 1 input buffer. Output of P60 and P61 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	SCL11/TI20/TO20/INTP1
P61					SDA11/TI21/TO21/INTP3
P72	I/O	Port 7. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	ADTRG/SGOA/SEG1
P73					SGO/SGOF/SEG0
P74					SCK01/TI23/TO23/SEG26
P75					PCL/SI01/TI22/TO22/SEG27
P80	I/O	Port 8. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM11/TI01/TO01/SEG32
P81					SM12/TI03/TO03/SEG33
P82					SM13/TI05/TO05/SEG34
P83					SM14/ZPD14/TI07/TO07/SEG35
P90	I/O	Port 9. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI21/TO21/SEG40
P91					TI23/TO23/SEG41
P92					TI25/TO25/SGOA/SEG42
P93					TI27/TO27/SGO/SGOF/SEG43
P94					TI01/TO01/RTC1HZ/SEG44
P121	I	Port 12. 2-bit Input port.	HZ	Input	X1
P122					X2/EXCLK
P137	I	Port 13. 1-bit Input port.	HZ	Input	INTP5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, HZ: High impedance

2.1.2 64-pin products

Table 2-3. Port Pins for R5F10CLDxFB, R5F10DLDxFB, R5F10DLExFB (1/2)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P00	I/O	Port 0. 7-bit I/O port. Input of P01 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI00/TO00/CTxD0/SEG14 Note1
P01					TI01/TO01/CRxD0/SEG15 Note1
P02					SO00/TI02/TO02/TI12/TO12/SEG16
P03					SI00/TI03/TO03/TI13/TO13/SEG17
P04					SCK00/TI04/TO04/TI14/TO14/SEG18
P05					TI05/TO05/TI15/TO15/SEG19
P07					TI07/TO07/TI17/TO17/SEG21
P10	I/O	Port 1. 7-bit I/O port. Input of P10, P11, and P17 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	LTxD1/SCK00/TI10/TO10/INTP4/SEG31
P11					LRxD1/INTPLR1/SI00/TI11/TO11/SEG30
P12					SO00/TI12/TO12/INTP2/SEG29
P13					SO01/TI13/TO13/SEG25
P14					TI14/TO14/LRxD0/INTPLR0/SEG24
P15					TI15/TO15/LTxD0/RTC1HZ/SEG23
P17					TI17/TO17/INTP0/SEG28
P20	I/O	Port 2. 5-bit I/O port. Can be set to analog input Note2 Input/output can be specified in 1-bit units.	HZ	Analog Input	AVREFP/ANI0
P21					AVREFM/ANI1
P22					ANI2
P23					ANI3
P27					ANI7
P30	I/O	Port 3. 4-bit I/O port. Input of P31 can be set to schmitt 1 input buffer. Output of P30 and P31 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI20/TO20/SCL11/SEG6
P31					TI21/TO21/SDA11/SEG7
P32					TI22/TO22/SEG8
P33					TI23/TO23/SEG9
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: HZ Int.: PU	Input	TOOL0
P54	I/O	Port 5. 4-bit I/O port. Input of P55 to P57 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI14/TO14/SO01/SEG2
P55					TI15/TO15/SI01/SEG3
P56					TI16/TO16/SCK01/SEG4
P57					TI17/TO17/SEG5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset, PD: Pull down, PU: Pull up, HZ: High impedance

Notes 1. CTxD0 and CRxD0 are not provided for R5F10CLDxFB with no CAN channel.

2. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

Table 2-3. Port Pins for R5F10CLDxFB, R5F10DLDxFB, R5F10DLExFB (2/2)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P60	I/O	Port 6. 2-bit I/O port. Input of P61 can be set to schmitt 1 input buffer. Output of P60 and P61 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	SCL11/TI20/TO20/INTP1
P61					SDA11/TI21/TO21/INTP3
P70	I/O	Port 7. 6-bit I/O port. Input of P70 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	CRxD0/LRxD0/INTPLR0/TI03/TO03/TOOLRXD[Note]
P71					CTxD0/LTxD0/TOOLTXD[Note]
P72			Ext.: PD Int.: HZ		ADTRG/SGOA/SEG1
P73					SGO/SGOF/SEG0
P74					SCK01/TI23/TO23/SEG26
P75					PCL/SI01/TI22/TO22/SEG27
P80	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM11/TI01/TO01/SEG32
P81					SM12/TI03/TO03/SEG33
P82					SM13/TI05/TO05/SEG34
P83					SM14/ZPD14/TI07/TO07/SEG35
P84					SM21/TI11/TO11/SEG36
P85					SM22/TI13/TO13/SEG37
P86					SM23/TI15/TO15/SEG38
P87					SM24/ZPD24/TI17/TO17/SEG39
P90	I/O	Port 9. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI21/TO21/SEG40
P91					TI23/TO23/SEG41
P92					TI25/TO25/SGOA/SEG42
P93					TI27/TO27/SGO/SGOF/SEG43
P94					TI01/TO01/RTC1HZ/SEG44
P121	I	Port 12. 4-bit Input port.	HZ	Input	X1
P122					X2/EXCLK
P123					XT1
P124					XT2
P137	I	Port 13. 1-bit Input port.	HZ	Input	INTP5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset, PD: Pull down, HZ: High impedance

Note CTxD0 and CRxD0 are not provided for R5F10CLDxFB with no CAN channel.

2.1.3 80-pin products

Table 2-4. Port Pins for R5F10CMDxFB, R5F10CMExFB, R5F10DMDxFB, R5F10DMExFB, R5F10DMFxFB, R5F10DMGxFB, R5F10DMJxFB (1/2)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P00	I/O	Port 0. 8-bit I/O port. Input of P01 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI00/TO00/CTxD0/SEG14 Note1
P01					TI01/TO01/CRxD0/SEG15 Note1
P02					SO00/TI02/TO02/TI12/TO12/SEG16
P03					SI00/TI03/TO03/TI13/TO13/SEG17
P04					SCK00/TI04/TO04/TI14/TO14/SEG18
P05					TI05/TO05/TI15/TO15/SEG19
P06					TI06/TO06/TI16/TO16/SEG20
P07					TI07/TO07/TI17/TO17/SEG21
P10	I/O	Port 1. 8-bit I/O port. Input of P10, P11, and P17 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	LTxD1/SCK00/TI10/TO10/INTP4/SEG31
P11					LRxD1/INTPLR1/SI00/TI11/TO11/SEG30
P12					SO00/TI12/TO12/INTP2/SEG29
P13					SO01/TI13/TO13/SEG25
P14					TI14/TO14/LRxD0/INTPLR0/SEG24
P15					TI15/TO15/LTxD0/RTC1HZ/SEG23
P16					TI16/TO16/SEG22
P17					TI17/TO17/INTP0/SEG28
P20	I/O	Port 2. 8-bit I/O port. Can be set to analog input Note2 Input/output can be specified in 1-bit units.	HZ	Analog Input	AVREFP/ANI0
P21					AVREFM/ANI1
P22 to P27					ANI2 to ANI7
P30	I/O	Port 3. 8-bit I/O port. Input of P31 can be set to schmitt 1 input buffer. Output of P30 and P31 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI20/TO20/SCL11/SEG6
P31					TI21/TO21/SDA11/SEG7
P32					TI22/TO22/SO00/SEG8
P33					TI23/TO23/SI00/SEG9
P34					TI24/TO24/SCK00/SEG10
P35					TI25/TO25/SEG11
P36					TI26/TO26/SEG12
P37					TI27/TO27/SEG13
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: HZ Int.: PU	Input	TOOL0
P54	I/O	Port 5. 4-bit I/O port. Input of P55 to P57 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI14/TO14/SO01/SEG2
P55					TI15/TO15/SI01/SEG3
P56					TI16/TO16/SCK01/SEG4
P57					TI17/TO17/SEG5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset, PD: Pull down, PU: Pull up, HZ: High impedance

Notes 1. CTxD0 and CRxD0 are not provided for R5F10CMExFB and R5F10CMDxFB with no CAN channel.

2. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

Table 2-4. Port Pins for R5F10CMDxFB, R5F10CMExFB, R5F10DMDxFB, R5F10DMExFB, R5F10DMFxFB, R5F10DMGxFB, R5F10DMJxFB (2/2)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P60	I/O	Port 6. 4-bit I/O port. Input of P61 can be set to schmitt 1 input buffer. Output of P60 and P61 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	SCL11/TI20/TO20/INTP1
P61					SDA11/TI21/TO21/INTP3
P65					TI25/TO25
P66					TI24/TO24/PCL
P70	I/O	Port 7. 6-bit I/O port. Input of P70 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	CRxD0/LRxD0/INTPLR0/TI03/TO03/TOOLRXD[Note]
P71					CTxD0/LTxD0/TOOLTXD[Note]
P72			Ext.: PD Int.: HZ		ADTRG/SGOA/SEG1
P73					SGO/SGOF/SEG0
P74					SCK01/TI23/TO23/SEG26
P75					PCL/SI01/TI22/TO22/SEG27
P80	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM11/TI01/TO01/SEG32
P81					SM12/TI03/TO03/SEG33
P82					SM13/TI05/TO05/SEG34
P83					SM14/ZPD14/TI07/TO07/SEG35
P84					SM21/TI11/TO11/SEG36
P85					SM22/TI13/TO13/SEG37
P86					SM23/TI15/TO15/SEG38
P87					SM24/ZPD24/TI17/TO17/SEG39
P90	I/O	Port 9. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM31/TI21/TO21/SEG40
P91					SM32/TI23/TO23/SEG41
P92					SM33/TI25/TO25/SGOA/SEG42
P93					SM34/ZPD34/TI27/TO27/SGO/SGOF/SEG43
P94					SM41/TI01/TO01/RTC1HZ/SEG44
P95					SM42/TI03/TO03/SEG45
P96					SM43/TI05/TO05/SEG46
P97					SM44/ZPD44/TI07/TO07/SEG47
P121	I	Port 12. 4-bit Input port.	HZ	Input	X1
P122					X2/EXCLK
P123					XT1
P124					XT2
P137	I	Port 13. 1-bit Input port.	HZ	Input	INTP5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset, PD: Pull down, HZ: High impedance

Note CTxD0 and CRxD0 are not provided for R5F10CMExFB and R5F10CMDxFB with no CAN channel.

2.1.4 100-pin products

Table 2-5. Port Pins for R5F10DPExFB, R5F10DPFxFB, R5F10DPGxFB, R5F10TPJxFB, R5F10DPJxFB (1/3)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P00	I/O	Port 0. 8-bit I/O port. Input of P01 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI00/TO00/CTxD0/SEG14
P01					TI01/TO01/CRxD0/SEG15
P02					SO00/TI02/TO02/TI12/TO12/SEG16
P03					SI00/TI03/TO03/TI13/TO13/SEG17
P04					SCK00/TI04/TO04/TI14/TO14/SEG18
P05					TI05/TO05/TI15/TO15/SEG19
P06					TI06/TO06/TI16/TO16/SEG20
P07					TI07/TO07/TI17/TO17/SEG21
P10	I/O	Port 1. 8-bit I/O port. Input of P10, P11, and P17 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	LTxD1/SCK00/TI10/TO10/INTP4/SEG31
P11					LRxD1/INTPLR1/SI00/TI11/TO11/SEG30
P12					SO00/TI12/TO12/INTP2/SEG29
P13					SO01/TI13/TO13/SEG25
P14					TI14/TO14/LRxD0/INTPLR0/SEG24
P15					TI15/TO15/LTxD0/RTC1HZ/SEG23
P16					TI16/TO16/SEG22
P17					TI17/TO17/INTP0/SEG28
P20	I/O	Port 2. 8-bit I/O port. Can be set to analog input [Note] Input/output can be specified in 1-bit units.	HZ	Analog Input	AV_{REFP}/ANI0
P21					AV_{REFM}/ANI1
P22 to P27					ANI2 to ANI7
P30	I/O	Port 3. 8-bit I/O port. Input of P31 can be set to schmitt 1 input buffer. Output of P30 and P31 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI20/TO20/SCL11/SEG6
P31					TI21/TO21/SDA11/SEG7
P32					TI22/TO22/SO00/SEG8
P33					TI23/TO23/SI00/SEG9
P34					TI24/TO24/SCK00/SEG10
P35					TI25/TO25/SEG11
P36					TI26/TO26/SEG12
P37					TI27/TO27/SEG13
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: HZ Int.: PU	Input	TOOL0
P50	I/O	Port 5. 8-bit I/O port. Input of P50 to P52 and P55 to P57 can be set to schmitt 1 input buffer. Output of P50 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI02/TO02/SDA11/SEG49
P51					TI04/TO04/SCK10/SEG50
P52					TI06/TO06/SI10/SEG51
P53					TI13/TO13/SO10/SEG52
P54					TI14/TO14/SO01/SEG2
P55					TI15/TO15/SI01/SEG3
P56					TI16/TO16/SCK01/SEG4
P57					TI17/TO17/SEG5

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, PU: Pull up, HZ: High impedance

Note Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

Table 2-5. Port Pins for R5F10DPExFB, R5F10DPFxFB, R5F10DPGxFB, R5F10TPJxFB, R5F10DPJxFB (2/3)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P60	I/O	Port 6. 4-bit I/O port. Input of P61, P63 can be set to schmitt 1 input buffer. Output of P60 and P61 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	SCL11/TI20/TO20/INTP1
P61					SDA11/TI21/TO21/INTP3
P62					CTxD1/TI27/TO27[Note]
P63					CRxD1/TI26/TO26[Note]
P64					RTC1HZ/TI11/TO11
P65					TI25/TO25
P66					TI24/TO24/PCL
P70	I/O	Port 7. 6-bit I/O port. Input of P70 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	CRxD0/LRxD0/INTPLR0/TI03/TO03/TOOLRXD
P71					CTxD0/LTxD0/TOOLTXD
P72			Ext.: PD Int.: HZ		ADTRG/SGOA/SEG1
P73					SGO/SGOF/SEG0
P74					SCK01/TI23/TO23/SEG26
P75					PCL/SI01/TI22/TO22/SEG27
P80	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM11/TI01/TO01/SEG32
P81					SM12/TI03/TO03/SEG33
P82					SM13/TI05/TO05/SEG34
P83					SM14/ZPD14/TI07/TO07/SEG35
P84					SM21/TI11/TO11/SEG36
P85					SM22/TI13/TO13/SEG37
P86					SM23/TI15/TO15/SEG38
P87					SM24/ZPD24/TI17/TO17/SEG39
P90	I/O	Port 9. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM31/TI21/TO21/SEG40
P91					SM32/TI23/TO23/SEG41
P92					SM33/TI25/TO25/SGOA/SEG42
P93					SM34/ZPD34/TI27/TO27/SGO/SGOF/SEG43
P94					SM41/TI01/TO01/RTC1HZ/SEG44
P95					SM42/TI03/TO03/SEG45
P96					SM43/TI05/TO05/SEG46
P97					SM44/ZPD44/TI07/TO07/SEG47
P121	I	Port 12. 4-bit Input port.	HZ	Input	X1
P122					X2/EXCLK
P123					XT1
P124					XT2

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset, PD: Pull down, HZ: High impedance

Note CTxD1 and CRxD1 are not provided for R5F10TPJxFB, R5F10DPGxFB, R5F10DPFxFB and R5F10DPExFB with a CAN channel.

Table 2-5. Port Pins for R5F10DPExFB, R5F10DPFxFB, R5F10DPGxFB, R5F10TPJxFB, R5F10DPJxFB (3/3)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P130	O	Port 13. 1-bit output port, 1-bit input port and 6-bit I/O port. Input of P135 can be set to schmitt 1 input buffer. Output of P136 can be set to N-ch open-drain output. Input/output of P131 to P136 can be specified in 1-bit units. Use of an on-chip pull-up resistor of P131 to P136 can be specified by a software setting	Output Low	Output	–
P131	I/O		HZ	Input	SO10/LTxD1/TI21/TO21
P132					SI10/LRxD1/INTPLR1/TI20/TO20
P133					SCK10/TI22/TO22
P134					SGOA/CTxD1/TI24/TO24[Note1]
P135					SGO/SGOF/CRxD1/TI26/TO26[Note1]
P136			Ext.: PD Int.: HZ		TI00/TO00/SCL11/SEG48
P137	I		HZ	Input	INTP5
P140	I/O	Port 14. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting	HZ	Input	TI11/TO11
P150	I/O	Port 14. 1-bit I/O port. Can be set to analog input[Note2] Input/output can be specified.	HZ	Analog Input	ANI8

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, HZ: High impedance

Notes 1. CTxD1 and CRxD1 are not provided for R5F10TPJxFB, R5F10DPGxFB, R5F10DPFxFB and R5F10DPExFB with a CAN channel.

2. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

2.1.5 128-pin products

Table 2-6. R5F10DSJxFB, R5F10DSKxFB, R5F10DSLxFB (1/4)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P00	I/O	Port 0. 8-bit I/O port. Input of P01 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	CTxD0/TI00/TO00/SEG14
P01					CRxD0/TI01/TO01/SEG15
P02					SO00/TxD0/TI02/TO02/TI12/TO12/SEG16
P03					SI00/RxD0/TI03/TO03/TI13/TO13/SEG17
P04					SCK00/TI04/TO04/TI14/TO14/SEG18
P05					TI05/TO05/TI15/TO15/SEG19
P06					TI06/TO06/TI16/TO16/SEG20
P07					TI07/TO07/TI17/TO17/SEG21
P10	I/O	Port 1. 8-bit I/O port. Input of P10, P11, and P17 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	LTxD1/SCK00/TI10/TO10/INTP4/SEG31
P11					LRxD1/INTPLR1/SI00/RxD0/TI11/TO11/SEG30
P12					SO00/TxD0/TI12/TO12/INTP2/SEG29
P13					SO01/TI13/TO13/SEG25
P14					LRxD0/INTPLR0/TI14/TO14/SEG24
P15					LTxD0/RTC1HZ/TI15/TO15/SEG23
P16					TI16/TO16/SEG22
P17					TI17/TO17/INTP0/SEG28
P20	I/O	Port 2. 8-bit I/O port. Can be set to analog input Note Input/output can be specified in 1-bit units.	HZ	Analog Input	AV_{REFP}/ANI0
P21					AV_{REFM}/ANI1
P22 to P27					ANI2 to ANI7
P30	I/O	Port 3. 8-bit I/O port. Input of P31 can be set to schmitt 1 input buffer. Output of P30 and P31 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI20/TO20/SCL11/SEG6
P31					TI21/TO21/SDA11/SEG7
P32					TI22/TO22/SO00/TxD0/SEG8
P33					TI23/TO23/SI00/RxD0/SEG9
P34					TI24/TO24/SCK00/SEG10
P35					TI25/TO25/SEG11
P36					TI26/TO26/SEG12
P37					TI27/TO27/SEG13
P40	I/O	Port 4. 8-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: HZ Int.: PU	Input	TOOL0
P41			HZ		STOPST/TI04/TO04
P42			Ext.: PD Int.: HZ		TI10/TO10/SEG7
P43					TI22/TO22/SEG14
P44					TI23/TO23/SEG15
P45					SEG53
P46					$\overline{\text{DBWR}}$/SEG27
P47					$\overline{\text{DBRD}}$/SEG26

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, PU: Pull up, HZ: High impedance

Note Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

Table 2-6. R5F10DSJxFB, R5F10DSKxFB, R5F10DSLxFB (2/4)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P50	I/O	Port 5. 8-bit I/O port. Input of P50 to P52 and P55 to P57 can be set to schmitt 1 input buffer. Output of P50 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI02/TO02/SDA11/SEG49
P51					TI04/TO04/SCK10/SEG50
P52					TI06/TO06/SI10/SEG51
P53					TI13/TO13/SO10/SEG52
P54					TI14/TO14/SO01/SEG2
P55					TI15/TO15/SI01/SEG3
P56					TI16/TO16/SCK01/SEG4
P57					TI17/TO17/SEG5
P60	I/O	Port 6. 7-bit I/O port. Input of P61, P63 can be set to schmitt 1 input buffer. Output of P60 and P61 can be set to N-ch open-drain output. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	SCL11/TI20/TO20/INTP1
P61					SDA11/TI21/TO21/INTP3
P62					CTxD1/TI27/TO27
P63					CRxD1/TI26/TO26
P64					RTC1HZ/TI11/TO11
P65					TI25/TO25
P66					TI24/TO24/PCL
P70	I/O	Port 7. 6-bit I/O port. Input of P70 can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	HZ	Input	CRxD0/LRxD0/INTPLR0/TI03/TO03/TOOLRxD
P71					CTxD0/LTxD0/TOOLTxD
P72			Ext.: PD Int.: HZ		SGOA/ADTRG/SEG1
P73					SGO/SGOF/SEG0
P74					SCK01/TI23/TO23/SEG26
P75					SI01/TI22/TO22/SEG27/PCL
P80	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM11/TI01/TO01/SEG32
P81					SM12/TI03/TO03/SEG33
P82					SM13/TI05/TO05/SEG34
P83					SM14/ZPD14/TI07/TO07/SEG35
P84					SM21/TI11/TO11/SEG36
P85					SM22/TI13/TO13/SEG37
P86					SM23/TI15/TO15/SEG38
P87					SM24/ZPD24/TI17/TO17/SEG39

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, HZ: High impedance

Table 2-6. R5F10DSJxFB, R5F10DSKxFB, R5F10DSLxFB (3/4)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P90	I/O	Port 9. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	SM31/TI21/TO21/SEG40
P91					SM32/TI23/TO23/SEG41
P92					SM33/SGOA/TI25/TO25/SEG42
P93					SM34/ZPD34/SGO/SGOF/TI27/TO27/SEG43
P94					SM41/RTC1HZ/TI01/TO01/SEG44
P95					SM42/TI03/TO03/SEG45
P96					SM43/TI05/TO05/SEG46
P97					SM44/ZPD44/TI07/TO07/SEG47
P100	I/O	Port 10. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	TI24/TO24/SEG36
P101					TI25/TO25/SEG37
P102					TI26/TO26/SEG38
P103					TI27/TO27/SEG39
P104					TI01/TO01/SEG44
P105					TI02/TO02/SEG45
P106					TI05/TO05/SEG46
P107					TI06/TO06/SEG47
P110	I/O	Port 10. 8-bit I/O port. Input can be set to schmitt 1 input buffer. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Ext.: PD Int.: HZ	Input	DBD0/SCK00/TI00/TO00/SEG35
P111					DBD1/SI00/RxD0/TI02/TO02/SEG34
P112					DBD2/SO00/TxD0/TI04/TO04/SEG33
P113					DBD3/TI06/TO06/SEG32
P114					DBD4/TI07/TO07/SEG31
P115					DBD5/TI10/TO10/SEG30
P116					DBD6/TI12/TO12/SEG29
P117					DBD7/TI20/TO20/SEG28
P121	I	Port 12. 4-bit Input port, 3-bit I/O port. Input/output of P125 to P127 can be specified in 1-bit units. Use of an on-chip pull-up resistor of P125 to P127 can be specified by a software setting.	HZ	Input	X1
P122					X2/EXCLK
P123					XT1
P124					XT2
P125	I/O		Ext.: PD Int.: HZ		TI12/TO12/SEG25
P126					TI14/TO14/SEG24
P127					TI16/TO16/SEG23

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, HZ: High impedance

Table 2-6. R5F10DSJxFB, R5F10DSKxFB, R5F10DSLxFB (4/4)

Pin Name	I/O	Function	During Reset	After Reset	Alternate Function
P130	O	Port 13. 1-bit output port, 1-bit input port and 6-bit I/O port. Input of P135 can be set to schmitt 1 input buffer. Output of P136 can be set to N-ch open-drain output. Input/output of P131 to P136 can be specified in 1-bit units. Use of an on-chip pull-up resistor of P131 to P136 can be specified by a software setting	Output Low	Output	RESOUT
P131	I/O		HZ	Input	SO10/LTxD1/TI21/TO21
P132					SI10/LRxD1/INTPLR1/TI20/TO20
P133					SCK10/TI22/TO22
P134					SGOA/CTxD1/TI24/TO24
P135					SGO/SGOF/CRxD1/TI26/TO26
P136			Ext.: PD Int.: HZ		TI00/TO00/SCL11/SEG48
P137	I		HZ	Input	INTP5
P140	I/O	Port 14. 1-bit I/O port. Input/output can be specified. Use of an on-chip pull-up resistor can be specified by a software setting	HZ	Input	TI11/TO11
P150	I/O	Port 15. 3-bit I/O port. Can be set to analog input Note Input/output can be specified.	HZ	Analog Input	ANI8
P151					ANI9
P152					ANI10

Remark Ext. (external reset): POR reset or pin reset, Int. (internal reset): WDT reset or LVD reset,
PD: Pull down, HZ: High impedance

Note Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

2.1.6 Pins for each product (pins other than port pins)

(1/6)

Function Name	I/O	Function	48-pin	64-pin	80-pin	100-pin	128-pin
			R5F10CGx/ R5F10DGx	R5F10CLx/ R5F10DLx	R5F10CMx/ R5F10DMx	R5F10TPx/ R5F10DPx	R5F10DSx
ADTRG	Input	A/D conversion start trigger external input	31	43	55	65	53
ANI0/AVREFP		A/D converter analog input	4	4	8	10	113
ANI1/AVREFM			3	3	7	9	112
ANI2			2	2	6	8	111
ANI3			1	1	5	7	110
ANI4			–	–	4	6	109
ANI5			–	–	3	5	108
ANI6			–	–	2	4	107
ANI7			48	64	1	3	106
ANI8			–	–	–	2	105
ANI9			–	–	–	–	104
ANI10			–	–	–	–	103
COM0	Output	LCD common output 0	36	48	60	70	58
COM1		LCD common output 1	35	47	59	69	57
COM2		LCD common output 2	34	46	58	68	56
COM3		LCD common output 3	33	45	57	67	55
SEG0	Output	LCD segment output 0	32	44	56	66	54
SEG1		LCD segment output 1	31	43	55	65	53
SEG2		LCD segment output 2	30	42	54	64	52
SEG3		LCD segment output 3	29	41	53	63	51
SEG4		LCD segment output 4	28	40	52	62	50
SEG5		LCD segment output 5	27	39	51	61	49
SEG6		LCD segment output 6	26	38	50	60	48
SEG7		LCD segment output 7	25	37	49	59	47, 95
SEG8		LCD segment output 8	–	36	48	58	46
SEG9		LCD segment output 9	24	35	47	57	45
SEG10		LCD segment output 10	–	–	46	56	44
SEG11		LCD segment output 11	–	–	45	55	43
SEG12		LCD segment output 12	–	–	44	54	42
SEG13		LCD segment output 13	–	–	43	53	41
SEG14		LCD segment output 14	23	34	42	52	40, 94
SEG15		LCD segment output 15	22	33	41	51	39, 93
SEG16		LCD segment output 16	–	32	40	50	35
SEG17		LCD segment output 17	–	31	39	49	34
SEG18		LCD segment output 18	–	30	38	48	33
SEG19		LCD segment output 19	–	29	37	47	32
SEG20		LCD segment output 20	–	–	36	46	31
SEG21		LCD segment output 21	–	28	35	45	30
SEG22		LCD segment output 22	–	–	34	44	29
SEG23		LCD segment output 23	–	27	33	43	28, 38
SEG24		LCD segment output 24	21	26	32	42	27, 37
SEG25		LCD segment output 25	20	25	31	41	26, 36
SEG26		LCD segment output 26	19	24	30	40	25, 19

(2/6)

Function Name	I/O	Function	48-pin	64-pin	80-pin	100-pin	128-pin
			R5F10CGx/ R5F10DGx	R5F10CLx/ R5F10DLx	R5F10CMx/ R5F10DMx	R5F10TPx/ R5F10DPx	R5F10DSx
SEG27	Output	LCD segment output 27	18	23	29	39	24, 18
SEG28		LCD segment output 28	–	22	28	38	23, 17
SEG29		LCD segment output 29	17	21	27	37	22, 16
SEG30		LCD segment output 30	16	20	26	36	21, 15
SEG31		LCD segment output 31	15	19	25	35	20, 14
SEG32		LCD segment output 32	47	63	80	95	88 ,13
SEG33		LCD segment output 33	46	62	79	94	87 ,12
SEG34		LCD segment output 34	45	61	78	93	86 ,11
SEG35		LCD segment output 35	44	60	77	92	85 ,10
SEG36		LCD segment output 36	–	57	74	89	82 ,92
SEG37		LCD segment output 37	–	56	73	88	81 ,91
SEG38		LCD segment output 38	–	55	72	87	80 ,90
SEG39		LCD segment output 39	–	54	71	86	79 ,89
SEG40		LCD segment output 40	41	53	70	85	78
SEG41		LCD segment output 41	40	52	69	84	77
SEG42		LCD segment output 42	39	51	68	83	76
SEG43		LCD segment output 43	38	50	67	82	75
SEG44		LCD segment output 44	37	49	64	79	72, 68
SEG45		LCD segment output 45	–	–	63	78	71, 67
SEG46		LCD segment output 46	–	–	62	77	70, 66
SEG47		LCD segment output 47	–	–	61	76	69, 65
SEG48		LCD segment output 48	–	–	–	75	64
SEG49		LCD segment output 49	–	–	–	74	63
SEG50		LCD segment output 50	–	–	–	73	62
SEG51		LCD segment output 51	–	–	–	72	61
SEG52		LCD segment output 52	–	–	–	71	60
SEG53		LCD segment output 53	–	–	–	–	59
TI00	Input	External count clock input/capture trigger to 16-bit timer 00 to 07	23	34	42	75,52	40, 64,10
TI01			22, 37, 47	63,49,33	80,64,41	95,79,51	39, 88, 72, 68
TI02			–	32	40	74,50	35, 63, 67, 11
TI03			46	62,7,31	79,63,11,39	94,78,49,13	34, 87, 71, 116
TI04			–	30	38	48,73	33, 62, 12, 101
TI05			45	61, 29	78,62,37	93,77,47	32, 86, 70, 66
TI06			–	–	36	46,72	31, 61, 65, 13
TI07			44	60,28	77,61,35	92,76,45	30, 85, 69, 14
TO00	Output	16-bit timer 00 to 07 output	23	34	42	75,52	40, 64, 10
TO01			22, 37, 47	63,49,33	80,64,41	95,79,51	39, 88, 72, 68
TO02			–	32	40	74,50	35, 63, 67, 11
TO03			46	62,7, 31	79,63,11,39	94,78,49,13	34, 87, 71, 116
TO04			–	30	38	48,73	33, 62, 12, 101
TO05			45	61,29	78,62,37	93,77,47	32, 86, 70, 66
TO06			–	–	36	46,72	31, 61, 65, 13
TO07			44	60,28	77,61,35	92,76,45	30, 85, 69, 14

(3/6)

Function Name	I/O	Function	48-pin R5F10CGx/ R5F10DGx	64-pin R5F10CLx/ R5F10DLx	80-pin R5F10CMx/ R5F10DMx	100-pin R5F10TPx/ R5F10DPx	128-pin R5F10DSx
TI10	Input	External count clock input/capture trigger to 16-bit timer 10 to 17	15	19	25	35	20, 15 , 95
TI11			16	57, 20	74, 26	89,14,30, 36	21, 82, 117, 5
TI12			17	32, 21	40, 27	50, 37	22, 36, 35, 16
TI13			20	56,25,31	73,31,39	88,71,41,49	34, 26, 60, 81
TI14			21, 30	30,26,42	38,32,54	48,42,64	27, 37, 52, 33
TI15			29	55,41,27,29	72,53,33,37	87,63,43,47	28, 32, 51, 80
TI16			28	40	36,34,52	46,44,62	29, 38, 50, 31
TI17			27	54,39,22,28	71,51,28,35	86,61,38,45	23, 30, 79, 49
TO10	Output	16-bit timer 10 to 17 output	15	19	25	35	20, 15, 95
TO11			16	57, 20	74,26	89,14,30,36	21, 82, 117, 5
TO12			17	32,21	40,27	50,37	22, 36, 35, 16
TO13			20	56,25,31	73,31,39	88,71,41,49	34, 26, 60, 81
TO14			21, 30	30,26,42	38,32,54	48,42,64	27, 37, 52, 33
TO15			29	55,41,27,29	72,53,33,37	87,63,43,47	28, 32, 51, 80
TO16			28	40	36,34,52	46,44,62	29, 38, 50, 31
TO17			27	54,39,22,28	71,51,28,35	86,61,38,45	23, 30, 79, 49
TI20	Input	External count clock input/capture trigger to 16-bit timer 20 to 27	13, 26	17,38	21,50	26,60,99	1, 48, 99, 17
TI21			14, 25, 41	53,37,18	70,49,22	100,85,59,27	2, 47, 100, 78
TI22			18	23,36	29,48	39,58,98	24, 46, 98, 94
TI23			19, 24, 40	52,35,24	69,47,30	84,57,40	25, 45, 77, 93
TI24			–	–	24,46	32,56,97	7, 44, 97, 92
TI25			39	51	68,45,23	83,55,31	6, 76, 43, 91
TI26			–	–	44	29,54,96	4, 42, 96, 90
TI27			38	50	67,43	82,53,28	75, 3, 41, 89
TO20	Output	16-bit timer 20 to 27 output	13, 26	17,38	21,50	26,60,99	1, 48, 99, 17
TO21			14, 25, 41	53,37,18	70,49,22	100,85,59,27	2, 47, 100, 78
TO22			18	23,36	29,48	39,58,98	24, 46, 98, 94
TO23			19, 24, 40	52,35,24	69,47,30	84,57,40	25, 45, 77, 93
TO24			–	–	24,46	32,56,97	7, 44, 97, 92
TO25			39	51	68,45,23	83,55,31	6, 76, 43, 91
TO26			–	–	44	29,54,96	4, 42, 96, 90
TO27			38	50	67,43	82,53,28	75, 3, 41, 89
SCK00	Input/ Output	Clock input/output for CSI00	15	19,30	46,25,38	56,35,48	20, 33, 44,10
SI00	Input	Serial data input to CSI00	16	20,31	47,26,39	57,36,49	21, 34, 45, 11
SO00	Output	Serial data output from CSI00	17	21,32	48,27,40	58,37,50	22, 35, 46, 12
SCK01	Input/ Output	Clock input/output for CSI01	19, 28	40,24	52,30	62,40	50, 25
SI01	Input	Serial data input to CSI01	18, 29	41,23	53,29	63,39	51, 24
SO01	Output	Serial data output from CSI01	20, 30	42,25	54,31	64,41	52, 26

(4/6)

Function Name	I/O	Function	48-pin	64-pin	80-pin	100-pin	128-pin
			R5F10CGx/ R5F10DGx	R5F10CLx/ R5F10DLx	R5F10CMx/ R5F10DMx	R5F10TPx/ R5F10DPx	R5F10DSx
RxD0	Input	Serial data input to UART0	–	–	–	–	21, 34, 45, 11
TxD0	Output	Serial data output from UART0	–	–	–	–	22, 35, 46, 12
SCK10	Input/ Output	Clock input/output for CSI10	–	–	–	98,73	98, 62
SI10	Input	Serial data input to CSI10	–	–	–	99,72	99, 61
SO10	Output	Serial data output from CSI10	–	–	–	100,71	100, 60
SCL11	Output	Clock output for simplified I^2C	13, 26	38,17	50,21	75,60,26	64, 48, 1
SDA11	Input/ Output	Serial data I/O for simplified I^2C	14, 25	37,18	49,22	74,59,27	63, 47, 2
LRxD0	Input	Serial data input to LIN-UART0	–	26,7	32,11	42,13	27, 116
INTPLR0	Input	External interrupt request input for which the valid edge for LIN-UART0	–	26,7	32,11	42,13	27, 116
LTxD0	Output	Serial data output from LIN-UART0	–	27,6	33,10	43,12	28, 115
LRxD1	Input	Serial data input to LIN-UART1	16	20	26	99,36	99, 21
INTPLR1	Input	External interrupt request input for which the valid edge for LIN-UART1	16	20	26	99,36	99, 21
LTxD1	Output	Serial data output from LIN-UART1	15	19	25	100,35	100, 20
CRxD0	Input	CAN receive data input 0	22Note1	33,7Note1	41,11Note1	51,13	39, 116
CTxD0	Output	CAN transmit data output 0	23Note1	34,6Note1	42,10Note1	52,12	40, 115
CRxD1	Input	CAN receive data input 1	–	–	–	96,29Note2	96, 4
CTxD1	Output	CAN transmit data output 1	–	–	–	97,28Note2	97, 3
RTC1Hz	Output	Realtime clock calibration output (1Hz)	37	49,27	64,33	79,30,43	72, 28, 5
SGOA	Output	SG output(Amplitude PWM)	31, 39	51,43	68,55	97,83,65	97, 76, 53
SGO/SGOF	Output	SG output (AND with PWM & Frequency) / SG output (Frequency)	32, 38	50,44	67, 56	96,82,66	96, 75, 54
SM11	Output	Stepper motor output 11	47	63	80	95	88
SM12	Output	Stepper motor output 12	46	62	79	94	87
SM13	Output	Stepper motor output 13	45	61	78	93	86
SM14	Output	Stepper motor output 14	44	60	77	92	85
ZPD14	Input	Zero point detection input 14	44	60	77	92	85

Notes 1. These pins are only for the following products:
- R5F10DGE, R5F10DGD, R5F10DGC (48 pin products)
- R5F10DLE, R5F10DLD (64 pin products)
- R5F10DMJ, R5F10DMG, R5F10DMF, R5F10DME, R5F10DMD (80 pin products)
- R5F10TPJ, R5F10DPG. R5F10DPF, R5F10DPE, R5F10DPL, R5F10DPK,R5F10DPJ (100-pin products)

2. These pins are only for R5F10DPL, R5F10DPK,R5F10DPJ.

(5/6)

Function Name	I/O	Function	48-pin	64-pin	80-pin	100-pin	128-pin
			R5F10CGx/ R5F10DGx	R5F10CLx/ R5F10DLx	R5F10CMx/ R5F10DMx	R5F10TPx/ R5F10DPx	R5F10DSx
SM21	Output	Stepper motor output 21	–	57	74	89	82
SM22	Output	Stepper motor output 22	–	56	73	88	81
SM23	Output	Stepper motor output 23	–	55	72	87	80
SM24	Output	Stepper motor output 24	–	54	71	86	79
ZPD24	Input	Zero point detection input 24	–	54	71	86	79
SM31	Output	Stepper motor output 31	–	–	70	85	78
SM32	Output	Stepper motor output 32	–	–	69	84	77
SM33	Output	Stepper motor output 33	–	–	68	83	76
SM34	Output	Stepper motor output 34	–	–	67	82	75
ZPD34	Input	Zero point detection input 34	–	–	67	82	75
SM41	Output	Stepper motor output 41	–	–	64	79	72
SM42	Output	Stepper motor output 42	–	–	63	78	71
SM43	Output	Stepper motor output 43	–	–	62	77	70
SM44	Output	Stepper motor output 44	–	–	61	76	69
ZPD44	Input	Zero point detection input 44	–	–	61	76	69
DBD0	Input/ Output	LCD Bus I/F data lines 0	–	–	–	–	10
DBD1	Input/ Output	LCD Bus I/F data lines 1	–	–	–	–	11
DBD2	Input/ Output	LCD Bus I/F data lines 2	–	–	–	–	12
DBD3	Input/ Output	LCD Bus I/F data lines 3	–	–	–	–	13
DBD4	Input/ Output	LCD Bus I/F data lines 4	–	–	–	–	14
DBD5	Input/ Output	LCD Bus I/F data lines 5	–	–	–	–	15
DBD6	Input/ Output	LCD Bus I/F data lines 6	–	–	–	–	16
DBD7	Input/ Output	LCD Bus I/F data lines 7	–	–	–	–	17
$\overline{\text{DBWR}}$	Output	LCD Bus I/F write strobe	–	–	–	–	18
$\overline{\text{DBRD}}$	Output	LCD Bus I/F read strobe	–	–	–	–	19
STOPST	Output	STOP status output	–	–	–	–	101
RESOUT	Output	Reset output signal	–	–	–	–	102
PCL	Output	Clock output	18	23	24,29	32,39	24, 7
INTP0	Input	Interrupt from peripheral 0	–	22	28	38	23
INTP1	Input	Interrupt from peripheral 1	13	17	21	26	1
INTP2	Input	Interrupt from peripheral 2	17	21	27	37	22
INTP3	Input	Interrupt from peripheral 3	14	18	22	27	2
INTP4	Input	Interrupt from peripheral 4	15	19	25	35	20
INTP5	Input	Interrupt from peripheral 5	7	11	15	18	121

(6/6)

Function Name	I/O	Function	48-pin	64-pin	80-pin	100-pin	128-pin
			R5F10CGx/ R5F10DGx	R5F10CLx/ R5F10DLx	R5F10CMx/ R5F10DMx	R5F10TPx/ R5F10DPx	R5F10DSx
EXCLK	Input	External clock input for main system clock	8	12	16	19	122
X1		Resonator connection for main system clock	9	13	17	20	123
X2			8	12	16	19	122
XT1		Resonator connection for sub clock	–	10	14	17	120
XT2			–	9	13	16	119
$\overline{\text{RESET}}$	Input	External system reset input	6	8	12	15	118
TOOLRxD	Input	UART reception pin for the external device connection used during flash memory programming	–	7	11	13	116
TOOLTxD	Output	UART transmission pin for the external device connection used during flash memory programming	–	6	10	12	115
TOOL0	Input/ output	Data I/O for flash memory programmer/debugger	5	5	9	11	114
REGC		Connecting regulator output stabilization capacitance for internal operation. Connect to VSS via a capacitor (0.47 to 1 μF).	10	14	18	21	124
V_{DD}		Power supply for P20 to P27, P150, P137, P121 to P124, $\overline{\text{RESET}}$	12	16	20	24	127
EV_{DD}, EV_{DD0}, EV_{DD1}		Power supply for P00 to P07, P10 to P17, P30 to P37, P50 to P57, P60 to P66, P70 to P75, P130 to P136 and P140	12	16	20	25, 33	8, 128
SMV_{DD}, SMV_{DD0}, SMV_{DD1}		Power supply for P80 to P87, P90 to P97	43	59	66, 76	81, 91	74, 84
V_{SS}		Ground potential for P20-P27, P150, P137, P121 to P124, $\overline{\text{RESET}}$	11	15	19	22	125
EV_{SS}, EV_{SS0}, EV_{SS1}		Ground potential for P00 to P07, P10 to P17, P30 to P37, P50 to P57, P60 to P66, P70 to P75, P130 to P136 and P140	11	15	19	23, 34	9, 126
SMV_{SS}, SMV_{SS0}, SMV_{SS1}		Ground potential for P80 to P87, P90 to P97	42	58	65, 75	80, 90	73, 83

3. ELECTRICAL SPECIFICATIONS (J GRADE PRODUCT)

Cautions 1. These specifications show target values, which may change after device evaluation.

2. The RL78/D1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Definition of Pin Groups

Definition of pin groups described in this chapter is shown in the following table.

Pin groups		Pin names				
		48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Pin group 1	Group 1R	P40	P40, P70, P71	P40, P70, P71	P40, P70, P71, P130 to P135, P140	P40 to P44, P70, P71, P100 to P103, P130 to P135, P140
	Group 1L	P00 to P01, P10 to P14, P30 to P33, P54 to P57, P60, P61, P72 to P75	P00 to P05, P07, P10 to P15, P17, P30 to P33, P54 to P57, P60, P61, P72 to P75	P00 to P07, P10 to P17, P30 to P37, P54 to P57,P60, P61, P65, P66, P72 to P75	P00 to P07, P10 to P17, P30 to P37, P50 to P57, P72 to P75, P136	P00 to P07, P10 to P17, P30 to P37, P45 to P47, P50 to P57, P72 to P75, P104 to P107, P110 to P117, P125 to P127 P136
	Group 1C	-	-	-	P60 to P66	P60 to P66
Pin group 2 (ANI pins)		P20 to P23, P27	P20 to P23, P27	P20 to P27	P20 to P27, P150	P20 to P27, P150 to P152
Pin group 3 (SMC pins)	Group 3A	P80 to P83	P80 to P83	P80 to P83	P80 to P83	P80 to P83
	Group 3B	-	P84 to P87	P84 to P87	P84 to P87	P84 to P87
	Group 3C	P90 to P94	P90 to P94	P90 to P93	P90 to P93	P90 to P93
	Group 3D	-	-	P94 to P97	P94 to P97	P94 to P97
	Group 3E	P90 to P94	P84 to P87, P90 to P94	-	-	-
Pin group 4 (System pins)		P121 to P122, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137

Definition of Product Groups

Definition of product groups described in this chapter is shown in the following table.

Product groups	Product names				
	48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Product Group A	R5F10CGBJFB R5F10CGCJFB R5F10CGDJFB R5F10DGCJFB R5F10DGDJFB R5F10DGEJFB	R5F10CLDJFB R5F10DLDJFB R5F10DLEJFB	R5F10CMDJFB R5F10CMEJFB R5F10DMDJFB R5F10DMEJFB R5F10DMFJFB R5F10DMGJFB R5F10DMJJFB	R5F10DPEJFB R5F10DPFJFB R5F10DPGJFB R5F10DPJJFB R5F10TPJJFB	-
Product Group B	-	-	-	R5F10DPKJFB R5F10DPLJFB	R5F10DSJJFB R5F10DSKJFB R5F10DSLJFB

3.1 Absolute Maximum Ratings

T_A = +25 °C

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	-0.5 to +6.5	V
	EV_{DD0} EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5 and -0.5 to V_{DD} + 0.3	V
	SMV_{DD0} SMV_{DD1}	$SMV_{DD0} = SMV_{DD1}$	-0.5 to +6.5 and -0.5 to V_{DD} + 0.3	V
	V_{SS}	V_{SS}	-0.5 to +0.3	V
	EV_{SS0} EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
	SMV_{SS0} SMV_{SS1}	$SMV_{SS0} = SMV_{SS1}$	-0.5 to +0.3	V
Supply voltage up/down ramp	V_{DDRAMP}		≤50	V/ms
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note1	V
Input voltage	V_{I1}	Pin group 1	-0.3 to +6.5 and -0.3 to EV_{DD0}(EV_{DD1}) + 0.3	V
	V_{I2}	Pin group 2	-0.3 to +6.5 and -0.3 to V_{DD} + 0.3	V
	V_{I3}	Pin group 3	-0.3 to +6.5 and -0.3 to SMV_{DD0}(SMV_{DD1}) + 0.3	V
	V_{I4}	Pin group 4	-0.3 to +6.5 and -0.3 to V_{DD} + 0.3	V

(Continue to next page)

T_A = +25 °C

Parameter	Symbols	Conditions			Ratings	Unit
Output voltage	V_{O1}	Pin group 1			-0.3 to EV_{DD0} (EV_{DD1}) + 0.3	V
	V_{O2}	Pin group 2			-0.3 to V_{DD} + 0.3	V
	V_{O3}	Pin group 3			-0.3 to SMV_{DD0} (SMV_{DD1}) + 0.3	V
	V_{COM}	COM0 to COM3			-0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin	Pin group 1		-20	mA
		Total	Pin group 1		-150	mA
				Pin group 1L	-60	mA
				Pin group 1R	-55	mA
				Pin group 1C	-40	mA
	I_{OH2}	Per pin	Pin group 2		-0.5	mA
		Total			-2.0	mA
	I_{OH3}	Per pin	Pin group 3		-58	mA
		Total	Pin group 3	48-pin, 64-pin	-270	mA
				80-pin, 100-pin, 128-pin	-480	mA
				Pin group 3A	-120	mA
				Pin group 3B	-120	mA
				Pin group 3C	-120	mA
				Pin group 3D	-120	mA
				Pin group 3E	-150	mA
	I_{OHCOM}	Per pin	COM0 to COM3		-0.5	mA
		Total	COM0 to COM3		-1.0	mA
Output current, low	I_{OL1}	Per pin	Pin group 1		20	mA
		Total	Pin group 1		150	mA
				Pin group 1L	60	mA
				Pin group 1R	50	mA
				Pin group 1C	40	mA
	I_{OL2}	Per pin	Pin group 2		1.0	mA
		Total			5.0	mA
	I_{OL3}	Per pin	Pin group 3		58	mA
		Total	Pin group 3	48-pin, 64-pin	270	mA
				80-pin, 100-pin, 128-pin	480	mA
				Pin group 3A	120	mA
				Pin group 3B	120	mA
				Pin group 3C	120	mA
				Pin group 3D	120	mA
				Pin group 3E	150	mA
	I_{OLCOM}	Per pin	COM0 to COM3		0.5	mA
		Total	COM0 to COM3		1.0	mA
Operating ambient temperature	T_A	for normal operation mode			-40 to +85	°C
		for code flash programming			-40 to +85	°C
		for data flash programming			-40 to +85	°C
Storage temperature	T_{stg}				-65 to +150	°C

Note Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

3.2 Power consumption characteristics

3.2.1 Product group A

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, run mode	I_{DD1} Note 1	High speed MAIN RUN Note 2, 3, 4	f_{CLK} = 32 MHz	f_{HOCO} = 32 MHz	5.2	22	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	4.2	18	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	3.8	16	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	2.1	11	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	1.6	9	mA
				f_X = 4 MHz			
		SUB RUN Note 2, 3, 5	f_{CLK} = f_{XT} = 32.768 kHz		6	300	μA

Notes 1. The common condition for I_{DD1}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The program is running in the code flash.

2. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

3. The maximum value is that when all peripheral devices are operating. But the A/D converter, RTC, LCD circuit and stepper motor circuit are stopped, and the data flash and the code flash are stated to read mode. The 16-bit wakeup timer operates with f_{LOCO}.

4. Either f_X or f_{HOCO} which is selected for f_{CLK} is operated. The other is stopped.

5. f_X and f_{HOCO} are stopped.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, halt mode	I_{DD2} Note 1	High speed MAIN HALT Note 3, 4, 5	f_{CLK} = 32 MHz 2.7 V≤V_{DD}	f_{HOCO} = 32 MHz	1.0	8.1	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	0.8	6.9	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	0.7	6.0	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	0.4	4.3	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	0.35	3.6	mA
				f_X = 4 MHz			
		SUB HALT Note 3, 4, 6	f_{CLK} = f_{XT} = 32.768 kHz	RTC is stopped	1.0	130	μA
				RTC is operated by f_{XT} = 32.768KHz	1.2		
Supply current, stop mode	I_{DD3} Note 2	STOP Note 3, 4	RTC and f_{XT} are stopped		0.4	60	μA
			RTC is operated by f_{XT} = 32.768KHz		0.8		

Notes 1. The common condition for I_{DD2}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The HALT instruction is executed by the program in the code flash.
- The specification shows the stable current during HALT mode.

2. The common condition for I_{DD3}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The STOP instruction is executed by the program in the code flash during MAIN RUN operation.
- The spec shows the stable current during STOP mode.

3. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

4. The maximum value is that when all peripheral devices are operating. But the A/D converter, LCD circuit, stepper motor circuit, the data flash and the code flash are stopped. The 16-bit wakeup timer operates with f_{LOCO}.

5. Either f_X or f_{HOCO} which is selected for f_{CLK} is operated. The other is stopped.

6. f_X and f_{HOCO} are stopped.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Typ.	Max.	Unit
WDT operating current Note 1	I_{WDT}			0.25	1.0	μA
ADC operating current Note 2	I_{ADC}	Normal mode	V_{DD} = 5.0 V	1.3	1.7	mA
		Low voltage mode	V_{DD} = 3.0 V	0.5	0.7	mA
LCD operating Current Note 3	I_{LCD}	f_{LCD} = f_{SUB}, LCD clock = 512 Hz	V_{DD} = 5.0 V	100	140	μA
			V_{DD} = 3.0 V	90	130	μA
ZPD operating current Note 4	I_{ZPD}	One ZPD operated	V_{DD} = 5.0 V	150	600	μA
			V_{DD} = 3.0 V	100	500	μA
		Four ZPDs operated	V_{DD} = 5.0 V	500	2000	μA
			V_{DD} = 3.0 V	400	1600	μA

Notes
1. Current flowing only to the watchdog timer. The maximum specification of I_{DD1}, I_{DD2} and I_{DD3} include I_{WDT}.
2. Current flowing only to the A/D converter.The current value of the RL78/D1A is the sum of I_{DD} and I_{ADC} when the A/D converter operates.
3. Current flowing only to the LCD controller/driver circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{LCD} when the LCD controller/driver circuit operates.
4. Current flowing only to the ZPD circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{ZPD} when the ZPD circuit operates.

3.2.2 Product group B

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, run mode	I_{DD1} Note 1	High speed MAIN RUN Note 2, 3, 4, 5	f_{CLK} = 32 MHz	f_{HOCO} = 32 MHz	5.7	24	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	4.7	20	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	4.3	17.5	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	2.4	12	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	1.8	9.5	mA
				f_X = 4 MHz			
		SUB RUN Note 2, 3, 6	f_{CLK} = f_{XT} = 32.768 kHz		7	360	μA

Notes 1. The common condition for I_{DD1}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The program is running in the code flash.

2. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

3. The maximum value is that when all peripheral devices are operating. But the A/D converter, RTC, LCD circuit and stepper motor circuit are stopped, and the data flash and the code flash are stated to read mode. The 16-bit wakeup timer operates with f_{LOCO}.

4. Either f_X or f_{HOCO} which is selected for f_{CLK} is operated. The other is stopped.

5. At 128-pin products, the value of I_{DD1} does not include the LCDB (P11x, P46-7) pin toggle current.
I_{DD1} condition of LCDB macro is f_{CLK}=32MHz, mod8 mode, data rate=8MHz, 4cycle, 16bit write/read.

6. f_X and f_{HOCO} are stopped.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, halt mode	I_{DD2} Note 1	High speed MAIN HALT Note 3, 4, 5	f_{CLK} = 32 MHz 2.7 V≤V_{DD}	f_{HOCO} = 32 MHz	1.0	8.9	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	0.8	7.5	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	0.7	6.5	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	0.4	4.5	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	0.35	3.8	mA
				f_X = 4 MHz			
		SUB HALT Note 3, 4, 6	f_{CLK} = f_{XT} = 32.768 kHz	RTC is stopped	1.0	140	μA
				RTC is operated by f_{XT} = 32.768KHz	1.2		
Supply current, stop mode	I_{DD3} Note 2	STOP Note 3, 4	RTC and f_{XT} are stopped		0.4	70	μA
			RTC is operated by f_{XT} = 32.768KHz		0.8		

Notes 1. The common condition for I_{DD2}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The HALT instruction is executed by the program in the code flash.
- The specification shows the stable current during HALT mode.

2. The common condition for I_{DD3}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The STOP instruction is executed by the program in the code flash during MAIN RUN operation.
- The spec shows the stable current during STOP mode.

3. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

4. The maximum value is that when all peripheral devices are operating. But the A/D converter, LCD circuit, stepper motor circuit, the data flash and the code flash are stopped. The 16-bit wakeup timer operates with f_{LOCO}.

5. Either f_X or f_{HOCO} which is selected for f_{CLK} is operated. The other is stopped.

6. f_X and f_{HOCO} are stopped.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Typ.	Max.	Unit
WDT operating current Note 1	I_{WDT}			0.25	1.0	μA
ADC operating current Note 2	I_{ADC}	Normal mode	V_{DD} = 5.0 V	1.3	1.7	mA
		Low voltage mode	V_{DD} = 3.0 V	0.5	0.7	mA
LCD operating Current Note 3	I_{LCD}	f_{LCD} = f_{SUB}, LCD clock = 512 Hz	V_{DD} = 5.0 V	100	140	μA
			V_{DD} = 3.0 V	90	130	μA
ZPD operating current Note 4	I_{ZPD}	One ZPD operated	V_{DD} = 5.0 V	150	600	μA
			V_{DD} = 3.0 V	100	500	μA
		Four ZPDs operated	V_{DD} = 5.0 V	500	2000	μA
			V_{DD} = 3.0 V	400	1600	μA

Notes
1. Current flowing only to the watchdog timer. The maximum specification of I_{DD1}, I_{DD2} and I_{DD3} include I_{WDT}.
2. Current flowing only to the A/D converter.The current value of the RL78/D1A is the sum of I_{DD} and I_{ADC} when the A/D converter operates.
3. Current flowing only to the LCD controller/driver circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{LCD} when the LCD controller/driver circuit operates.
4. Current flowing only to the ZPD circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{ZPD} when the ZPD circuit operates.

3.3 Oscillator characteristics

3.3.1 Main(X1) oscillator characteristics

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Main(X1) clock oscillation frequency	f_X	Ceramic resonator	1.0		20.0	MHz
		Crystal resonator	1.0		20.0	MHz

Remark Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3.3.2 High speed on chip oscillator characteristics

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
HOCO oscillation frequency	f_{HOCO}	4 MHz mode	3.92	4.00	4.08	MHz
		8 MHz mode	7.84	8.00	8.16	MHz
		16 MHz mode	15.68	16.00	16.32	MHz
		24 MHz mode	23.52	24.00	24.48	MHz
		32 MHz mode	31.36	32.00	32.64	MHz

Remark Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3.3.3 Low speed on chip oscillator characteristics

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
LOCO oscillation frequency	f_{LOCO}		12.75	15.0	17.25	kHz

3.3.4 Sub(XT1) oscillator characteristics

T_A = -40 to +85 °C, 2.7 V≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Sub(XT1) clock oscillation frequency	f_{XT}	Possible to oscillate	29.0	32.768	35.0	kHz

Remark Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3.4 DC characteristics

3.4.1 Pin group 1

T_A = -40 to +85 °C, 4.0 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V (1/2)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin				-5.0	mA
	I_{OH2}	Per pin, P73 or P135 (SG port)				-13.0	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note 2])	Group 1L			-40.0	mA
			Group 1R			-40.0	mA
			Group 1C (128-pin, 100-pin)			-30.0	mA
		for 128-pin, 100-pin				-110.0	mA
		for 80-pin, 64-pin, 48-pin				-60.0	mA
Output current, low	I_{OL1}	Per pin				8.5	mA
	I_{OL2}	Per pin, P73 or P135 (SG ports)				13.0	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note 3])	Group 1L			40.0	mA
			Group 1R			35.0	mA
			Group 1C (128-pin, 100-pin)			40.0	mA
		for 128-pin, 100-pin				115.0	mA
		for 80-pin, 64-pin, 48-pin				60.0	mA

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -30.0 mA

Total output current of pins = (-30.0 × 0.7)/(80 × 0.01) ≈ -26.2 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 40.0 mA

Total output current of pins = (40.0 × 0.7)/(80 × 0.01) = 35.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

T_A = -40 to +85 °C, 4.0 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V (2/2)

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Input voltage, high Note 2	V_{IH1}	Schmitt3 mode	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	Schmitt1 mode Note 3	0.65EV_{DD}		EV_{DD}	V
Input voltage, low Note 2	V_{IL1}	Schmitt3 mode	0		0.5EV_{DD}	V
	V_{IL2}	Schmitt1 mode Note 3	0		0.35EV_{DD}	V
Input hysteresis width Note 2, 4	V_{IHYS1}	Schmitt3 mode	0.1	0.19	0.29	V
	V_{IHYS2}	Schmitt1 mode Note 3	0.15	0.59	0.84	V
Output voltage, high Note 1	V_{OH1}	I_{OH} = -5.0 mA	EV_{DD}-1.0		EV_{DD}	V
		I_{OH} = -3.0 mA up to 6 pins	EV_{DD}-0.5		EV_{DD}	V
	V_{OH2}	I_{OH} = -13.0 mA, P73 or P135 (SG port)	EV_{DD}-0.7		EV_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 8.5 mA	0		0.7	V
		I_{OL} = 3.0 mA up to 6 pins	0		0.5	V
	V_{OL2}	I_{OL} = 13.0 mA, P73 or P135 (SG port)	0		0.7	V
Input leakage current, high	I_{LIH1}	V_I = EV_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = EV_{SS}			-1	μA
On chip pull-up resistance Note 5	R_U	V_I = EV_{SS}	10	20	100	kΩ
On chip pull-down resistance Note 6	R_D	V_I = EV_{DD}	100			kΩ

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. Except P130 because it is output only port.

3. P01, P10, P11, P17, P31, P40, P50 to P52, P55 to P57, P61, P63, P70, P110 to P117, P135 only.

4. This value is defined by evaluation result.

5. Except P130 and P137. Pull-up resistance is connected by software when pin is set to input mode.

6. LCD segment shared pins only. Pull-down resistance is connected during reset.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

T_A = -40 to +85 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ 4.0 V, EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, VSS = EV_{SS0} = EV_{SS} = 0 V (1/2)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin				-1.0	mA
	I_{OH2}	Per pin, P73 or P135 (SG port)				-7.5	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note 2])	Group 1L			-15.0	mA
			Group 1R			-30.0	mA
			Group 1C (128-pin, 100-pin)			-7.0	mA
		for 128-pin, 100-pin				-52.0	mA
		for 80-pin, 64-pin, 48-pin				-33.0	mA
Output current, low	I_{OL1}	Per pin				1.5	mA
	I_{OL2}	Per pin, P73 or P135 (SG ports)				7.0	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note 3])	Group 1L			18.0	mA
			Group 1R			30.0	mA
			Group 1C (128-pin, 100-pin)			10.0	mA
		for 128-pin, 100-pin				58.0	mA
		for 80-pin, 64-pin, 48-pin				35.0	mA

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -7.0 mA

Total output current of pins = (-7.0 × 0.7)/(80 × 0.01) ≈ -6.1 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

T_A = -40 to +85 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ 4.0 V, EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, VSS = EV_{SS0} = EV_{SS} = 0 V (2/2)

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Input voltage, high Note 2	V_{IH1}	Schmitt3 mode	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	Schmitt1 mode Note 3	0.7EV_{DD}		EV_{DD}	V
Input voltage, low Note 2	V_{IL1}	Schmitt3 mode	0		0.4EV_{DD}	V
	V_{IL2}	Schmitt1 mode Note 3	0		0.3EV_{DD}	V
Input hysterisis width Note 2, 4	V_{IHYS1}	Schmitt3 mode	0.05		0.21	V
	V_{IHYS2}	Schmitt1 mode Note 3	0.08		0.53	V
Output voltage, high Note 1	V_{OH1}	I_{OH} = -1.0 mA	EV_{DD}-0.5		EV_{DD}	V
	V_{OH2}	I_{OH} = -7.5 mA, P73 or P135 (SG port)	EV_{DD}-0.7		EV_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 1.5 mA	0		0.5	V
	V_{OL2}	I_{OL}= 7.0 mA, P73 or P135 (SG port)	0		0.7	V
Input leakage current, high	I_{LIH1}	V_I = EV_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = EV_{SS}			-1	μA
On chip pull-up resistance Note 5	R_U	V_I = EV_{SS}	10	20	100	kΩ
On chip pull-down resistance Note 6	R_D	V_I = EV_{DD}	100			kΩ

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. Except P130 because it is output only port.

3. P01, P10, P11, P17, P31, P40, P50 to P52, P55 to P57, P61, P63, P70, P110 to P117, P135 only.

4. This value is defined by evaluation result.

5. Except P130 and P137. Pull-up resistance is connected by software when pin is set to input mode.

6. LCD segment shared pins only. Pull-down resistance is connected during reset.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

3.4.2 Pin group 2 (ANI pins)

T_A = -40 to +85 °C, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin			-0.1	mA
	$I_{OHTOTAL}$	Total			-0.8	mA
Output current, low	I_{OL1}	Per pin			0.4	mA
	$I_{OLTOTAL}$	Total			3.2	mA
Input voltage, high	V_{IH1}		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}		0		0.5V_{DD}	V
Input hysteresis width Note	V_{IHYS1}		0.1	0.19	0.29	V
Output voltage, high	V_{OH1}	I_{OH} = -0.1 mA	V_{DD}-0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 0.4 mA	0		0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = V_{SS}			-1	μA

Note This specification is guaranteed by design. It is not tested when shipment.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 4.0 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin			-0.1	mA
	$I_{OHTOTAL}$	Total			-0.8	mA
Output current, low	I_{OL1}	Per pin			0.4	mA
	$I_{OLTOTAL}$	Total			3.2	mA
Input voltage, high	V_{IH1}		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}		0		0.4V_{DD}	V
Input hysteresis width Note	V_{IHYS1}		0.05		0.21	V
Output voltage, high	V_{OH1}	I_{OH} = -0.1 mA	V_{DD}-0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 0.4 mA	0		0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = V_{SS}			-1	μA

Note This specification is guaranteed by design. It is not tested when shipment.

3.4.3 Pin group 3 (SMC pins)

T_A = -40 to +85 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (1/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin		T_A = -40 °C			-52	mA
				T_A = +25 °C			-39	mA
				T_A = +85 °C			-32	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
			Group 3B	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
			Group 3C 128-pin, 100-pin 80-pin	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
			Group 3C 64-pin 48-pin	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
			Group 3D (128-pin, 100-pin, 80-pin)	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
			Group 3E (64-pin, 48-pin)	T_A = -40 °C			-148	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -118.0 mA

Total output current of pins = (-118.0 × 0.7)/(80 × 0.01) ≈ -103.2 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +85 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (2/3)

Parameter	Symbols	Conditions				Min.	Typ.	Max.	Unit
Output current, low	I_{OL1}	Per pin			T_A = -40 °C			52	mA
					T_A = +25 °C			39	mA
					T_A = +85 °C			32	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A		T_A = -40 °C			118	mA
					T_A = +25 °C			118	mA
					T_A = +85 °C			96	mA
			Group 3B		T_A = -40 °C			118	mA
					T_A = +25 °C			118	mA
					T_A = +85 °C			96	mA
			Group 3C	128-pin, 100-pin 80-pin	T_A = -40 °C			118	mA
					T_A = +25 °C			118	mA
					T_A = +85 °C			96	mA
				64-pin 48-pin	T_A = -40 °C			118	mA
					T_A = +25 °C			118	mA
					T_A = +85 °C			96	mA
			Group 3D (128-pin, 100-pin, 80-pin)		T_A = -40 °C			118	mA
					T_A = +25 °C			118	mA
					T_A = +85 °C			96	mA
			Group 3E (64-pin, 48-pin)		T_A = -40 °C			148	mA
					T_A = +25 °C			118	mA
					T_A = +85 °C			96	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 118.0 mA
Total output current of pins = (118.0 × 0.7)/(80 × 0.01) ≈ 103.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +85 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (3/3)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}			0.8SMV_{DD}		SMV_{DD}	V
Input voltage, low	V_{IL1}			0		0.5SMV_{DD}	V
Input hysteresis width Note 1	V_{IHYS1}			0.1	0.19	0.29	V
Output voltage, high	V_{OH1}	T_A = -40 °C	I_{OH} = -52 mA	SMV_{DD} - 0.5		SMV_{DD}	V
		T_A = +25 °C	I_{OH} = -39 mA				
		T_A = +85 °C	I_{OH} = -32 mA				
Output voltage, low	V_{OL1}	T_A = -40 °C	I_{OL} = 52 mA	0		0.5	V
		T_A = +25 °C	I_{OL} = 39 mA				
		T_A = +85 °C	I_{OL} = 32 mA				
Output voltage deviation Note 2	V_{DEV}			0		50	mV
Input leakage current, high	I_{LIH1}	V_I = SMV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	V_I = SMV_{SS}				-1	μA
On chip pull-up resistance Note 3	R_U	V_I = SMV_{SS}		10	20	100	kΩ
On chip pull-down resistance Note 4	R_D	V_I = SMV_{DD}		100			kΩ

Notes 1. This specification is guaranteed by design. It is not tested when shipment.

2. Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (|V_{OHx}-V_{OHy}|, |V_{OLx}-V_{OLy}|) @I_{OHx} = I_{OHy}, I_{OLx} = I_{OLy}.
X and y denote any combination of two pins of the following pin groups: (P80-P83, P84-P87, P90-P93, P94-P97)

3. Pull-up resistance is connected by software when pin is set to input mode.

4. LCD segment shared pins only. Pull-down resistance is connected during reset.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 4.0 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (1/3)

Parameter	Symbols	Conditions				Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin			T_A = -40 °C			-30	mA
					T_A = +25 °C			-25	mA
					T_A = +85 °C			-23	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A		T_A = -40 °C			-90	mA
					T_A = +25 °C			-75	mA
					T_A = +85 °C			-69	mA
			Group 3B		T_A = -40 °C			-90	mA
					T_A = +25 °C			-75	mA
					T_A = +85 °C			-69	mA
			Group 3C	128-pin, 100-pin 80-pin	T_A = -40 °C			-90	mA
					T_A = +25 °C			-75	mA
					T_A = +85 °C			-69	mA
				64-pin 48-pin	T_A = -40 °C			-90	mA
					T_A = +25 °C			-75	mA
					T_A = +85 °C			-69	mA
			Group 3D (128-pin, 100-pin, 80-pin)		T_A = -40 °C			-90	mA
					T_A = +25 °C			-75	mA
					T_A = +85 °C			-69	mA
			Group 3E (64-pin, 48-pin)		T_A = -40 °C			-90	mA
					T_A = +25 °C			-75	mA
					T_A = +85 °C			-69	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -75.0 mA

Total output current of pins = (-75.0 × 0.7)/(80 × 0.01) ≈ -65.6 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 4.0 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (2/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, low	I_{OL1}	Per pin		T_A = -40 °C			30	mA
				T_A = +25 °C			23	mA
				T_A = +85 °C			20	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
			Group 3B	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
			Group 3C	128-pin, 100-pin 80-pin T_A = -40 °C			90	mA
				128-pin, 100-pin 80-pin T_A = +25 °C			69	mA
				128-pin, 100-pin 80-pin T_A = +85 °C			60	mA
				64-pin 48-pin T_A = -40 °C			90	mA
				64-pin 48-pin T_A = +25 °C			69	mA
				64-pin 48-pin T_A = +85 °C			60	mA
			Group 3D (128-pin, 100-pin, 80-pin)	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
			Group 3E (64-pin, 48-pin)	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 69.0 mA
Total output current of pins = (69.0 × 0.7)/(80 × 0.01) ≈ 60.3 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 4.0 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (3/3)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}			0.8SMV_{DD}		SMV_{DD}	V
Input voltage, low	V_{IL1}			0		0.4SMV_{DD}	V
Input hysteresis width Note 1	V_{IHYS1}			0.05		0.21	V
Output voltage, high	V_{OH1}	T_A = -40 °C	I_{OH} = -30 mA	SMV_{DD} - 0.5		SMV_{DD}	V
		T_A = +25 °C	I_{OH} = -25 mA				
		T_A = +85 °C	I_{OH} = -23 mA				
Output voltage, low	V_{OL1}	T_A = -40 °C	I_{OL} = 30 mA	0		0.5	V
		T_A = +25 °C	I_{OL} = 23 mA				
		T_A = +85 °C	I_{OL} = 20 mA				
Output voltage deviation Note 2	V_{DEV}			0		50	mV
Input leakage current, high	I_{LIH1}	V_I = SMV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	V_I = SMV_{SS}				-1	μA
On chip pull-up resistance Note 3	R_U	V_I = SMV_{SS}		10	20	100	kΩ
On chip pull-down resistance Note 4	R_D	V_I = SMV_{DD}		100			kΩ

Notes 1. This speccification is guaranteed by design. It is not tested when shipment.

2. Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (|V_{OHx}-V_{OHy}|, |V_{OLx}-V_{OLy}|) @I_{OHx} = I_{OHy}, I_{OLx} = I_{OLy}.
X and y denote any combination of two pins of the following pin groups: (P80-P83, P84-P87, P90-P93, P94-P97)

3. Pull-up resistance is connected by software when pin is set to input mode.

4. LCD segment shared pins only. Pull-down resistance is connected during reset.

3.4.4 Pin group 4 (OSC, reset and P137 pins)

T_A = -40 to +85 °C, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.8V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$		0.65V_{DD}		V_{DD}	V
	V_{IH3}	P137		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0		0.2V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$		0		0.35V_{DD}	V
	V_{IL3}	P137		0		0.5V_{DD}	V
Input hysteresis width Note 2	V_{IHYS1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.1	0.7		V
	V_{IHYS2}	$\overline{\text{RESET}}$		0.15	0.59	0.84	V
Input leakage current, high	I_{LIH1}	P121, P122, P123, P124 $V_I = V_{DD}$	Port			1	μA
			EXCLK Note 1			1	μA
			OSC			10	μA
	I_{LIH2}	$\overline{\text{RESET}}$, $V_I = V_{DD}$				1	μA
	I_{LIH3}	P137, $V_I = V_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P121, P122, P123, P124 $V_I = V_{SS}$	Port			-1	μA
			EXCLK Note 1			-1	μA
			OSC			-10	μA
	I_{LIL2}	$\overline{\text{RESET}}$, $V_I = V_{SS}$				-1	μA
	I_{LIL3}	P137, $V_I = V_{SS}$				-1	μA

Notes 1. P122(EXCLK) only.

2. This speccification is guaranteed by design. It is not tested when shipment.

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 4.0 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.8V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH3}	P137		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0		0.2V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$		0		0.3V_{DD}	V
	V_{IL3}	P137		0		0.4V_{DD}	V
Input hysteresis width Note 2	V_{IHYS1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.08			V
	V_{IHYS2}	$\overline{\text{RESET}}$		0.08			V
Input leakage current, high	I_{LIH1}	P121, P122, P123, P124 $V_I = V_{DD}$	Port			1	μA
			EXCLK Note 1			1	μA
			OSC			10	μA
	I_{LIH2}	$\overline{\text{RESET}}$, $V_I = V_{DD}$				1	μA
	I_{LIH3}	P137, $V_I = V_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P121, P122, P123, P124 $V_I = V_{SS}$	Port			-1	μA
			EXCLK Note 1			-1	μA
			OSC			-10	μA
	I_{LIL2}	$\overline{\text{RESET}}$, $V_I = V_{SS}$				-1	μA
	I_{LIL3}	P137, $V_I = V_{SS}$				-1	μA

Notes 1. P122(EXCLK) only.

2. This speccification is guaranteed by design. It is not tested when shipment.

3.5 AC characteristics

3.5.1 Basic operation

T_A = -40 to +85 °C,

2.7 V ≤ = EV_{DD0} = EV_{DD1} ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock operation (Including PLL)	High speed main run		0.03125 Note 1		1	μs
		Sub system clock operation	SDIV = 0		1/f_{XT} (Typ. 30.5)			μs
External main system clock frequency	f_{EX}	Square wave input to EXCLK			2		20	MHz
External main system clock (square wave) input high/low level width	t_{EXH} t_{EXL}	Square wave input to EXCLK			24			ns
Timer input high/low level width	t_{TIH} t_{TIL}	TI00 to TI07, TI10 to TI17, TI20 to TI27			1/f_{MCK}+10 Note 2			ns
Port output frequency	f_{GPO}	P80 to P87, P90 to P97	C = 30 pF	4.0 V ≤ SMV_{DD}			2	MHz
		P20 to P27, P150 to P152	C = 30 pF	4.0 V ≤ V_{DD}			2	MHz
		P73,P135	C = 30 pF	4.0 V ≤ EV_{DD}			8	MHz
		Other than the above	C = 30 pF	4.0 V ≤ EV_{DD}			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
External interrupt input high/low level width Note 3	t_{INIH} t_{INIL}	INTP0 to INTP5, INTPLR0, INTPLR1			1			μs
$\overline{RESET}$ input low level width Note 3	t_{RSL}	$\overline{RESET}$			10			μs
Analog noise filter rejection pulse width Note 4	t_{WRJ}	INTP0 to INTP5, INTPLR0, INTPLR1, ADTRG			30	50	1000	ns
ADTRG input high level width	t_{ATH}	Without noise filter		AWC = 0	1/f_{CLK}+10			ns
				AWC = 1	10			ns
		With noise filter		AWC = 0	1/f_{CLK}+10 or t_{WRJ} (Note 5)			ns
				AWC = 1	t_{WRJ} (Note 5)			ns

Notes 1. Value is in case of f_{CLK} is 32.0 MHz. It is also allowed to exceed frequency up to +3%.

2. f_{MCK} shows the frequency value of operation clock for TAU. Usually, f_{MCK} is defined by MHz but this speccification is defined by ns. It is not defined by μs, so please be careful.

3. Pulses longer than this value will pass the input filter.

4. Pulses shorter than this value do not pass the input filters.

5. If the value of "1/f_{CLK}+10 [ns]" is less than t_{WRJ}, please use t_{WRJ} value instead of "1/f_{CLK} +10 [ns]".

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 3-1. AC Timing Test Points

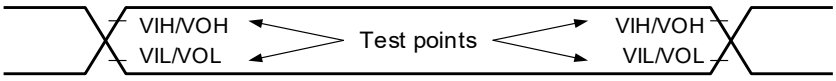


Figure 3-2. External Main System Clock Timing

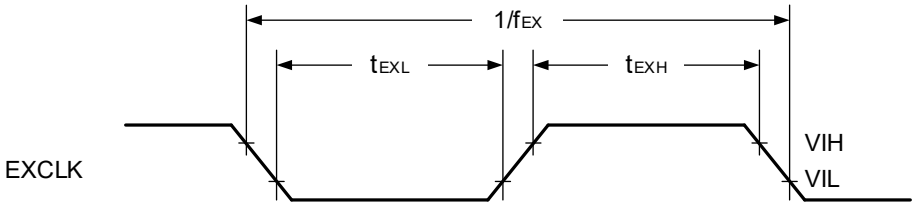


Figure 3-3. TI Timing

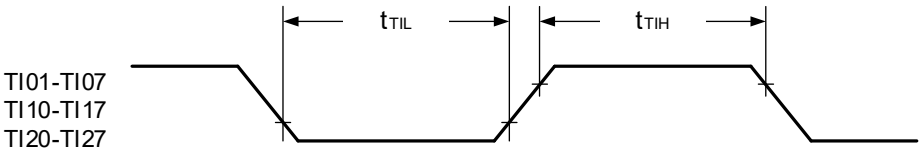


Figure 3-4. Interrupt Request Input Timing

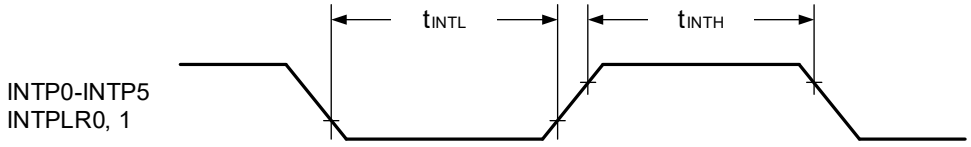
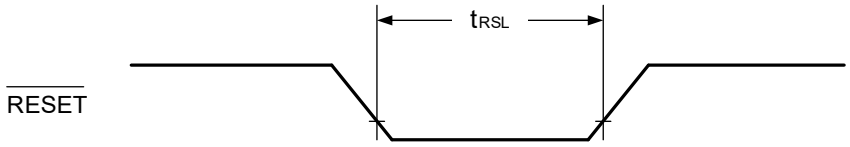


Figure 3-5. $\overline{\text{RESET}}$ Input Timing



3.5.2 Stepper motor controller/driver

T_A = -40 to +85 °C,
2.7 V ≤ SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Meter Controller/Driver input frequency	f_{MC} Note 1					32	MHz
PWM output rise time	t_R	10%-90% Note 2	4.0 V ≤ SMV_{DD} ≤ 5.5 V	15	60	100	ns
			2.7 V ≤ SMV_{DD} ≤ 4.0 V	20		500	ns
PWM output fall time	t_F	10%-90% Note 2	4.0 V ≤ SMV_{DD} ≤ 5.5 V	15	60	100	ns
			2.7 V ≤ SMV_{DD} ≤ 4.0 V	20		500	ns
Peak Cross Current Note 3	I_{CROSS}					50	ns
Output Pulse Width Note 4	t_{MO}	4.0 V≤SMV_{DD}≤5.5 V		250			ns
		2.7 V≤SMV_{DD}≤5.5 V		5000			ns
Output Pulse Length Deviation Note 5	t_{SMDEV}	4.0 V≤SMV_{DD}≤5.5 V		-65	-12	+10	ns
		2.7 V≤SMV_{DD}≤5.5 V		-100		+400	ns
Symmetry performance Note 6	ΔHSPmn	I_{OH} = -32 mA ΔHSPmn = | V_{OH}[(SMmn)max - (SMmn)min] |	2.7 V ≤ SMV_{DD} ≤ 5.5 V			50	mV
	ΔHSPmn	I_{OL} = 32 mA ΔHSPmn = | V_{OL}[(SMmn)max - (SMmn)min] |	4.0 V ≤ SMV_{DD} ≤ 5.5 V			50	mV
			2.7 V ≤ SMV_{DD} ≤ 5.5 V			100	mV

Notes 1. Source clock of the free-running counter.

2. t_R,t_F is not tested in production, specified by design.

3. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transition time t_R, t_F. It flows in addtion to the output current. The cross current is not tested,but derived from simulation.

4. The output buffer can not generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested,but derived from simulation.

5. The slew rate control function causes a deviation of output pulse time compared to the ideal selected output pulse setting. This value is not tested,but derived from simulation.

6. Indicates the dispersion of 16 PWM output voltages.(4 buffers' output voltage differences in the state of I_{OH}(I_{OL}) at the same time.) Not tested in production, specified by design.

Remark m = 1 to 4, n = 1 to 4

3.5.3 Sound generator

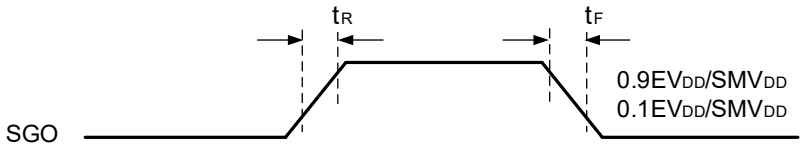
T_A = -40 to +85 °C,

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Sound generator input frequency	f_{SG}					32	MHz
SGO output rise time	t_R	C = 100 pF	P73, P135			200	ns
			P93			500	ns
SGO output fall time	t_F	C = 100 pF	P73, P135			200	ns
			P93			500	ns

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Sound Generator Output Timing



3.5.4 Serial interface: CSI operation

<Master mode>

T_A = -40 to +85 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.		Max.	Unit
SCK cycle time	t_{KCY1}	4.0≤V_{DD}	125	t_{KCY1}≥4/f_{CLK} Note		ns
		V_{DD}<4.0 V	250			ns
SCK high/low level width	t_{KH1} t_{KL1}	4.0≤V_{DD}	t_{KCY1}/2-12			ns
		V_{DD}<4.0 V	t_{KCY1}/2-18			ns
SI set up time	t_{SIK1}	4.0≤V_{DD}	44			ns
		V_{DD}<4.0 V	55			ns
SI hold time	t_{KSI1}		19			ns
SO output delay time	t_{KSO1}	C = 30 pF			25	ns

Note When CSI transfer is operated by DMA, it is necessary to concider DMA response time to decide cycle time.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

<Slave mode>

T_A = -40 to +85 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions		Min.	Max.	Unit
SCK cycle time	t_{KCY2}	4.0≤EV_{DD}	20 MHz<f_{MCK}	8/f_{MCK} Note		ns
			f_{MCK}≤20 MHz	6/f_{MCK} Note		ns
		EV_{DD}<4.0 V	16 MHz<f_{MCK}	8/f_{MCK} Note		ns
			f_{MCK}≤16 MHz	6/f_{MCK} Note		ns
SCK high/low level width	t_{KH2} t_{KL2}			t_{KCY2}/2-8		ns
SI set up time	t_{SIK2}	2.7≤EV_{DD}		1/f_{MCK}+20		ns
SI hold time	t_{KSI2}			1/f_{MCK}+31		ns
SO output delay time	t_{KSO2}	C = 30pF	4.0≤EV_{DD}		2/f_{MCK}+44	ns
			EV_{DD}<4.0 V		2/f_{MCK}+57	ns

Note When CSI transfer is operated by DMA, it is necessary to concider DMA response time to decide cycle time.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 3-6. CSI mode connection diagram

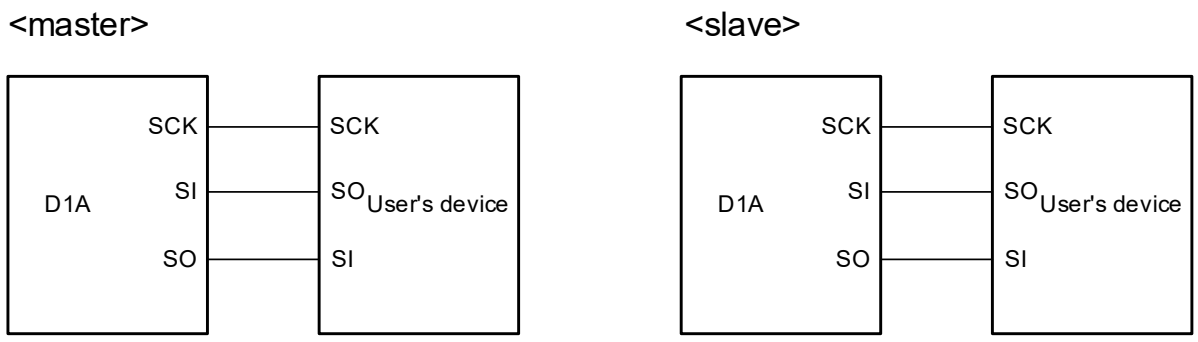


Figure 3-7. CSI mode serial transfer timing (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

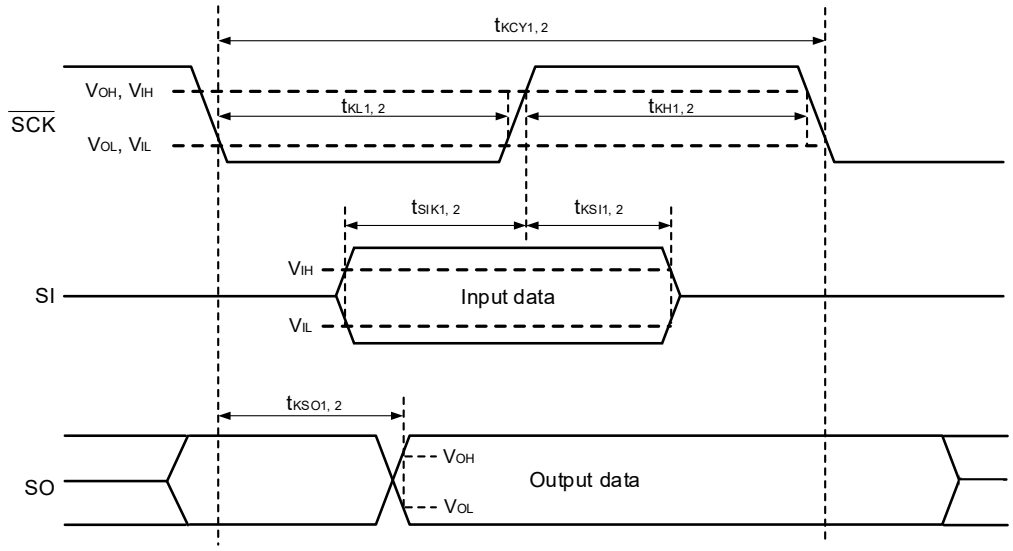
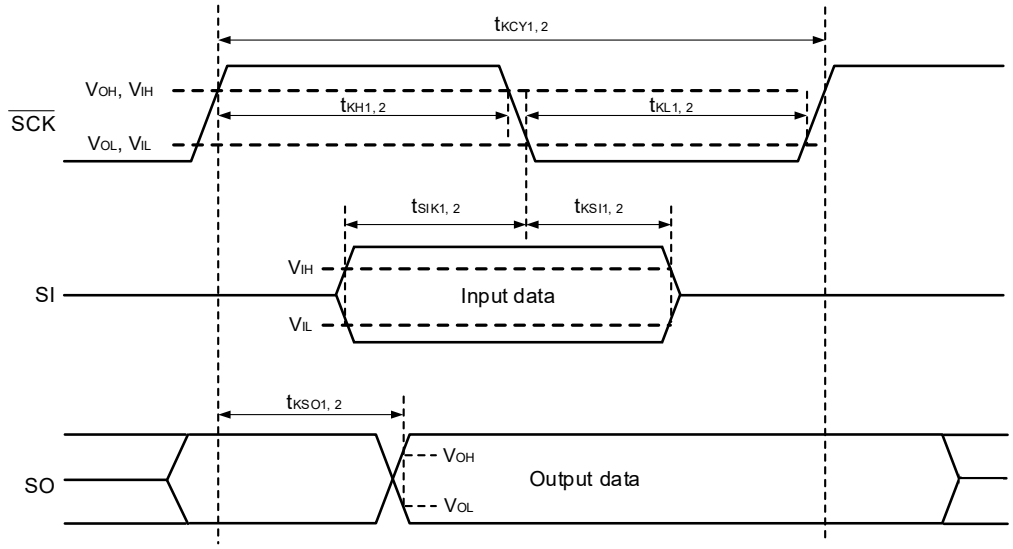


Figure 3-8. CSI mode serial transfer timing (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



3.5.5 Serial interface: UART operation (128-pin only)

T_A = -40 to +85 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} = ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Item	Symbol	Conditions	Min.	Max.	Unit
Transfer rate	T			$f_{MCK}/6$ Note	bps
		Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		5.3	Mbps

Note When CSI transfer is operated by DMA, it is necessary to concider DMA response time to decide cycle time.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 3-9 UART connection diagram

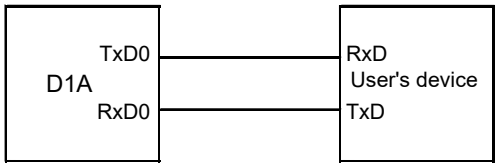
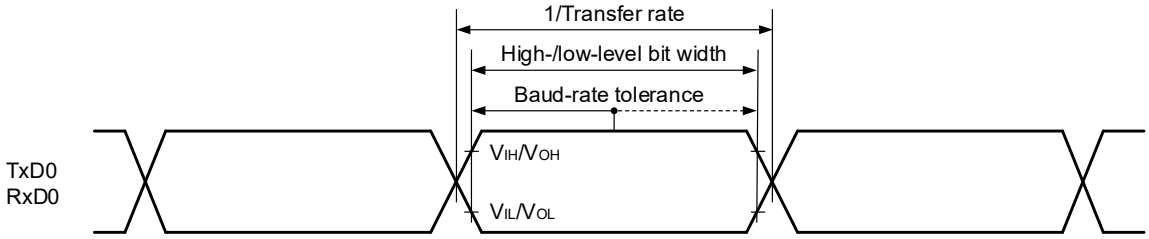


Figure 3-10. UART mode bit width (reference)



3.5.6 Serial interface: simplified I²C operation

T_A = -40 to +85 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} = ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	Rb = 3 kΩ, Cb = 100 pF		400	kHz
Hold time during SCL = ”L”	t_{LOW}	Rb = 3 kΩ, Cb = 100 pF	1150		ns
Hold time during SCL = ”H”	t_{HIGH}	Rb = 3kΩ, Cb = 100 pF	1150		ns
Data set up time (reception)	$t_{SU;DAT}$	Rb = 3 kΩ, Cb = 100 pF	1/f_{MCK}+85		ns
Data hold time (transmission)	$t_{HD;DAT}$	Rb = 3 kΩ, Cb = 100 pF	0	305	ns

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 3-11 simplified I²C connection diagram

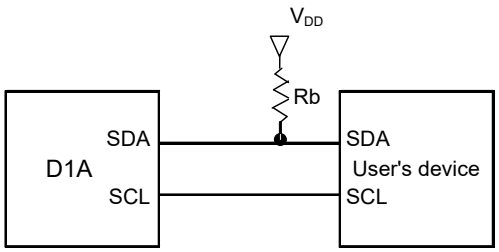
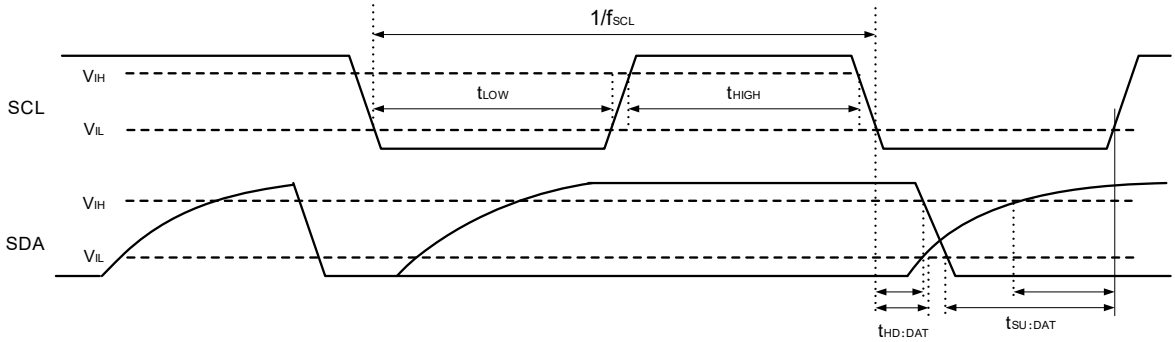


Figure 3-12. Simplified I²C mode serial transfer timing



3.5.7 Serial interface: LIN-UART(UARTF) operation

T_A = -40 to +85 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Item	Symbols	Conditions	Min.	Max.	Unit
Transfer rate	T			1.0	Mbps

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

3.5.8 Serial interface: CAN operation

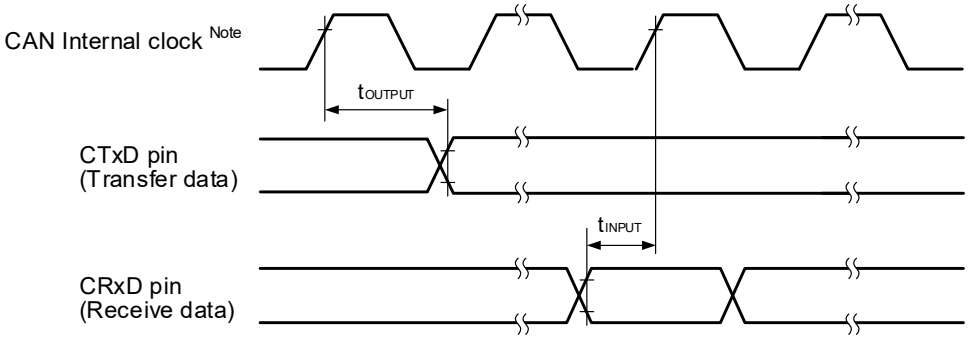
T_A = -40 to +85 °C,

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.	Max.	Unit
Transfer rate	T			1.0	Mbps
Internal delay time	t_{NODE}			100	ns
CRxD minimum pulse width for wake up	t_{CRXW}	Necessary width to detect wakeup signal	200		ns

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 3-13. Internal delay time of CAN



Internal delay time (t_{NODE}) = Internal Transfer Delay (t_{output}) + Internal Receive Delay (t_{Input})

Note CAN Internal clock (f_{CAN}): CAN baud rate clock

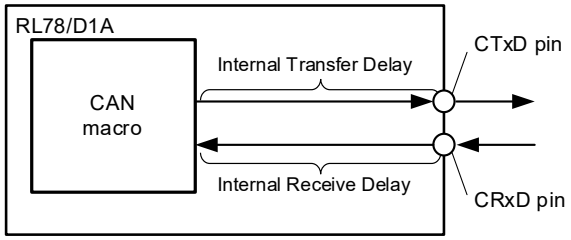


Image figure of Internal delay

3.6 LCD Bus Interface characteristics (128-pin products only)

T_A = -40 to +85 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} =EV_{SS1} =0 V

Items	Symbols	Conditions	MIN.	MAX.	Unit
Transfer frequency	F			8	MHz
CycleTime	t_{CYC}		LBCYC x T		ns
Control low pulse width	t_{CL}		(LBWST + 1)T - 1		ns
Enable active pulse width	t_{ELH}		(LBWST + 1)T - 5		ns
Control setup time	t_{RWS}		0.5T_S - 8		ns
Control hold time	t_{RWH}		0.5T - 3		ns
Data output setup time	t_{DOS}		0.5T_S - 6	0.5T_S + 17	ns
Data output hold time	t_{DOH}		{LBCYC - (LBWST + 1.5)} T - 27		ns
Data input setup time	t_{DIS}		50		ns
Data input hold time	t_{DIH}		0		ns
Output disable time	t_{OD}		0.5T - 14		ns

Remarks 1. T = (1/f_{CLK}) × n (n: LCD Bus Interface clock n divider setting)

2. T_S = (1/f_{CLK}) × N (N: LCD Bus Interface no clock divider N = 1, n divider N = n - 1)

3. F = 1/t_{CYC}

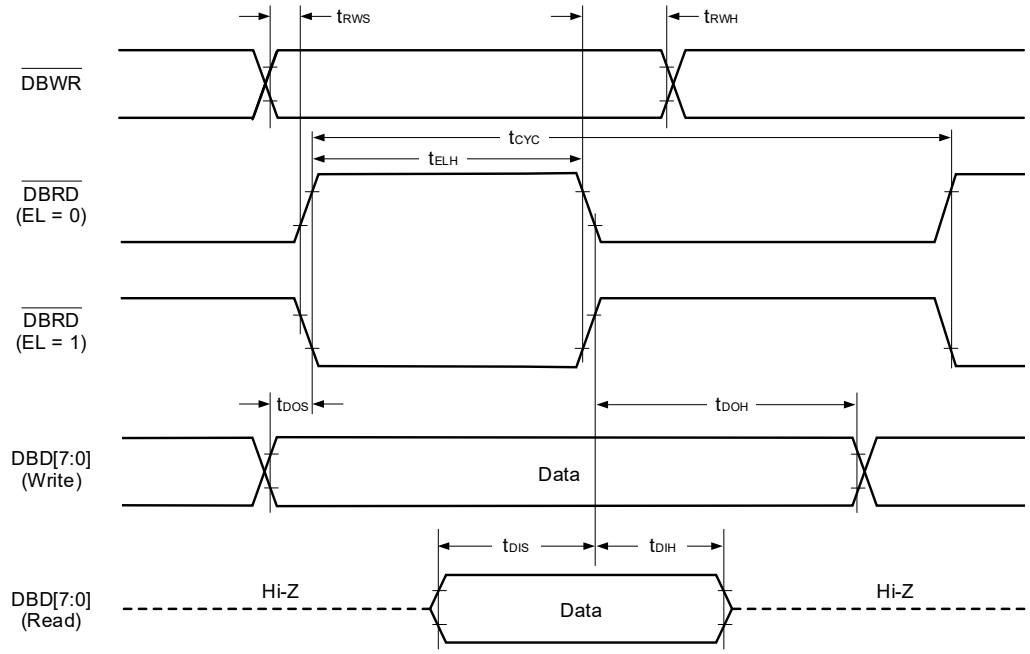
4. When EV_{DDx} = $SMV_{DD}x$ ≤ V_{DD}, LCD controller/driver related registers must be initial value (LCDON = 0, SCOC = 0, MDSET1 – 0 = 00, LCDPFx = 0).

5. The above table shows the timing of LCD bus interface with Schmitt1 input characteristic.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 3-14. LCD Bus Interface AC timing (1/2)

(a) LCDB mod68 mode timing



(b) mode68 turnaround timing

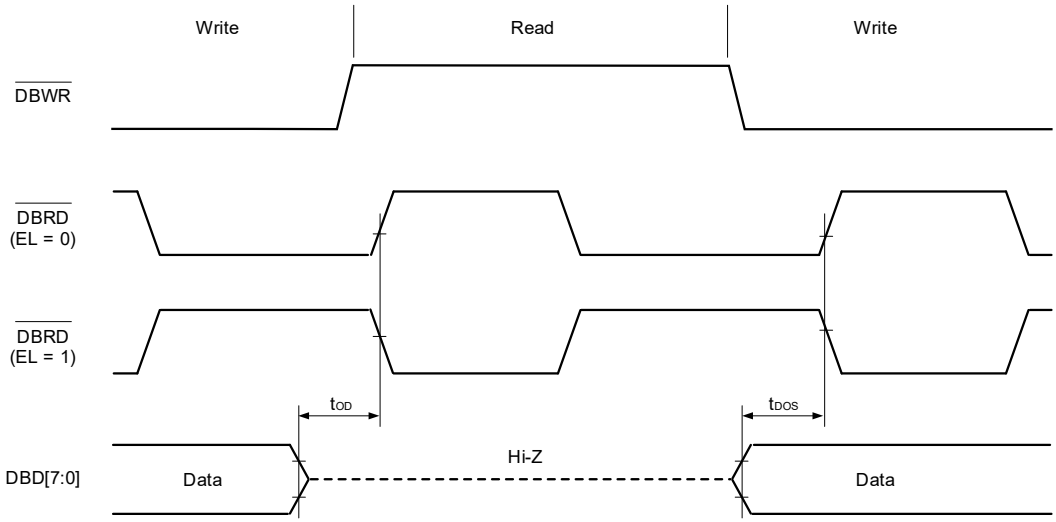
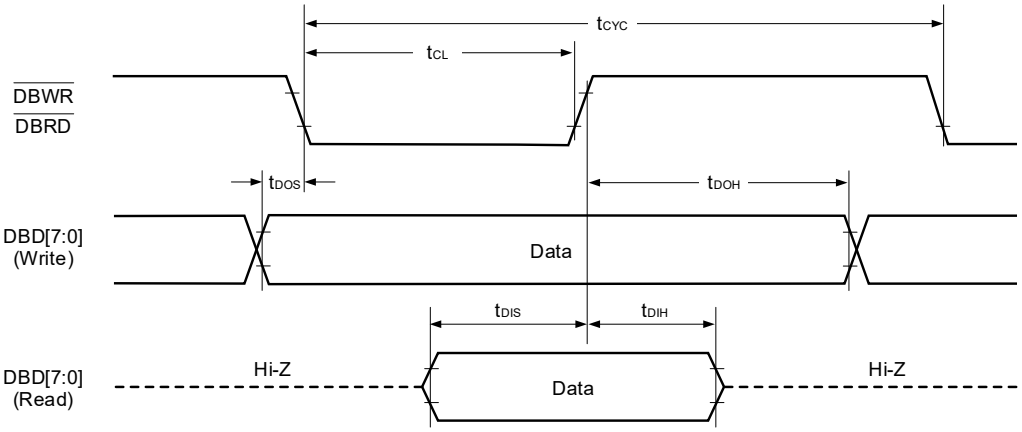
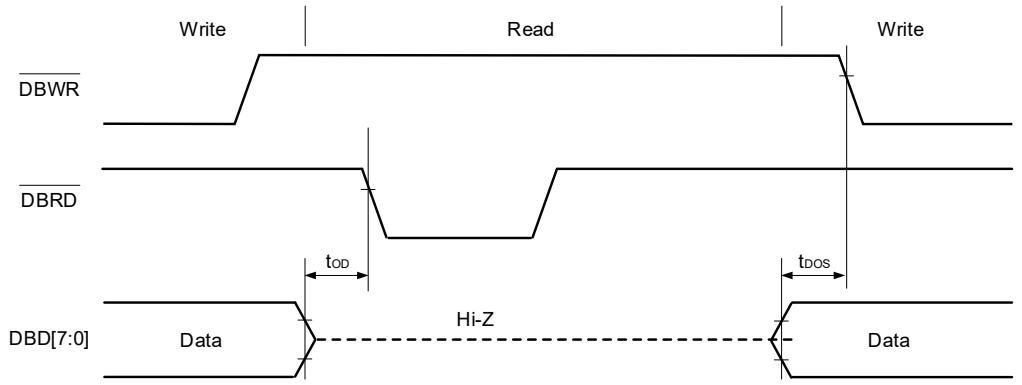


Figure 3-14. LCD Bus Interface AC timing (2/2)

(c) LCDB mod80 mode timing



(d) Mode80 turnaround timing



T_A = -40 to +85 °C, 3.2 V ≤ EV_{DD0} = EV_{DD1} = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
LCD division resistance Note 1	R_{LCD}				3	kΩ
LCD Segment output voltage (unloaded)	V_{ODS}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn} Note 2	V_{LCDn}+0.05	V
LCD Common output voltage (unloaded)	V_{ODC}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn}	V_{LCDn}+0.05	V
LCD Segment Output Voltage (loaded)	V_{ODSL0}	Io = ±10 μA, all segment pins at same time	V_{LCD0}-0.6	V_{LCD0}	V_{LCD0}+0.6	V
	V_{ODSL1}	Io = ±10 μA, all segment pins at same time	V_{LCD1}-0.6	V_{LCD1}	V_{LCD1}+0.6	V
	V_{ODSL2}	Io = ±10 μA, all segment pins at same time	V_{LCD2}-0.6	V_{LCD2}	V_{LCD2}+0.6	V
	V_{ODSL3}	Io = ±10 μA, all segment pins at same time	V_{LCD3}-0.6	V_{LCD3}	V_{LCD3}+0.6	V
LCD Common Output Voltage (loaded)	V_{ODCL0}	Io = ±40 μA, single pin	V_{LCD0}-0.2	V_{LCD0}	V_{LCD0}+0.2	V
	V_{ODCL1}	Io = ±40 μA, single pin	V_{LCD1}-0.2	V_{LCD1}	V_{LCD1}+0.2	V
	V_{ODCL2}	Io = ±40 μA, single pin	V_{LCD2}-0.2	V_{LCD2}	V_{LCD2}+0.2	V
	V_{ODCL3}	Io = ±40 μA, single pin	V_{LCD3}-0.2	V_{LCD3}	V_{LCD3}+0.2	V
LCD split voltage drive capability Note 1	V_{LC0}	Io = ±530 μA	V_{LCD0}-0.1	V_{LCD0}	V_{LCD0}+0.1	V
	V_{LC1}	Io = ±530 μA	V_{LCD1}-0.1	V_{LCD1}	V_{LCD1}+0.1	V
	V_{LC2}	Io = ±530 μA	V_{LCD2}-0.1	V_{LCD2}	V_{LCD2}+0.1	V
	V_{LC3}	Io = ±530 μA	V_{LCD3}-0.1	V_{LCD3}	V_{LCD3}+0.1	V
LCD output resistance (COM) Note 3	R_{ODC}				8	kΩ
LCD output resistance (SEG) Note 3	R_{ODS}				8	kΩ

Notes 1. Only internal connection. The vaule is design specification.

2. V_{LCDn} (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.

V_{LCDn}	no step-down transforming	step-down transforming
V_{LCD0}	V_{DD}	3/5 V_{DD}
V_{LCD1}	2/3 V_{DD}	2/5 V_{DD}
V_{LCD2}	1/3 V_{DD}	1/5 V_{DD}
V_{LCD3}	V_{SS}	V_{SS}

3. RODC is internal equivalent weight resistance from COM pin + COM IOBUF resistance.
RODS is internal equivalent weight resistance from SEG pin +SEG IOBUF resistance.

T_A = -40 to +85 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
LCD division resistance Note 1	R_{LCD}				3	kΩ
LCD Segment output voltage (unloaded)	V_{ODS}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn} Note 2	V_{LCDn}+0.05	V
LCD Common output voltage (unloaded)	V_{ODC}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn}	V_{LCDn}+0.05	V
LCD Segment Output Voltage (loaded)	V_{ODSL0}	Io = ±5 μA, all segment pins at same time	V_{LCD0}-0.6	V_{LCD0}	V_{LCD0}+0.6	V
	V_{ODSL1}	Io = ±5 μA, all segment pins at same time	V_{LCD1}-0.6	V_{LCD1}	V_{LCD1}+0.6	V
	V_{ODSL2}	Io = ±5 μA, all segment pins at same time	V_{LCD2}-0.6	V_{LCD2}	V_{LCD2}+0.6	V
	V_{ODSL3}	Io = ±5 μA, all segment pins at same time	V_{LCD3}-0.6	V_{LCD3}	V_{LCD3}+0.6	V
LCD Common Output Voltage (loaded)	V_{ODCL0}	Io = ±25 μA, single pin	V_{LCD0}-0.2	V_{LCD0}	V_{LCD0}+0.2	V
	V_{ODCL1}	Io = ±25 μA, single pin	V_{LCD1}-0.2	V_{LCD1}	V_{LCD1}+0.2	V
	V_{ODCL2}	Io = ±25 μA, single pin	V_{LCD2}-0.2	V_{LCD2}	V_{LCD2}+0.2	V
	V_{ODCL3}	Io = ±25 μA, single pin	V_{LCD3}-0.2	V_{LCD3}	V_{LCD3}+0.2	V
LCD split voltage drive capability	V_{LC0}	Io = ±530 μA	V_{LCD0}-0.1	V_{LCD0}	V_{LCD0}+0.1	V
	V_{LC1}	Io = ±530 μA	V_{LCD1}-0.1	V_{LCD1}	V_{LCD1}+0.1	V
	V_{LC2}	Io = ±530 μA	V_{LCD2}-0.1	V_{LCD2}	V_{LCD2}+0.1	V
	V_{LC3}	Io = ±530 μA	V_{LCD3}-0.1	V_{LCD3}	V_{LCD3}+0.1	V
LCD output resistance (COM) Note 3	R_{ODC}				10	kΩ
LCD output resistance (SEG) Note 3	R_{ODS}				10	kΩ

Notes 1. V_{LCDn} (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.

V_{LCDn}	no step-down transforming
V_{LCD0}	V_{DD}
V_{LCD1}	2/3 V_{DD}
V_{LCD2}	1/3 V_{DD}
V_{LCD3}	V_{SS}

2. Only internal connection. The vaule is design specification.

3. RODC is internal equivalent weight resistance from COM pin + COM IOBUF resistance.
RODS is internal equivalent weight resistance from SEG pin +SEG IOBUF resistance.

3.7 Analog characteristics

3.7.1 A/D converter characteristics

T_A = -40 to +85 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} =0 V
Reference voltage (+) = AV_{REFP}, Reference voltage(–) = AV_{REFM}

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	Bit
Overall error Note 1,2	AINL	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V			1.2	±3.5	LSB
Conversion time	Tconv	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V	3.6 V≤V_{DD}<5.5 V	2.125		39	μs
			2.7 V≤V_{DD}<5.5 V	3.1875		39	μs
Zero-scale error Note 1, 2	E_{ZS}	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				0.25	%FSR
Full-scale error Note 1, 2	E_{FS}	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				0.25	%FSR
Integral non-linearity error Note 1	ILE	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				±2.5	LSB
Differential non-linearityerror Note 1	DLE	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				±1.5	LSB
REF voltage(+)	AV_{REFP}			2.7		V_{DD}	V
REF voltage(-)	AV_{REFM}			V_{SS}			V
Analog input voltage	V_{AIN}			AV_{REFM}		AV_{REFP}	V
REF supply Current	I_{REF}	AV_{REFP} = 3 V			38	60	μA
		AV_{REFP} = 5 V			63	100	μA

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Minimum V_{DD}-0.5 V is allowed for AV_{REFP} to keep characteristic values

Remark When reference voltage(+) is not AV_{REFP} pin or reference voltage(-) is not AV_{REFM} pin, the accuracy will become worse.
Renesas recommends to use A/D converter with AV_{REFP} and AV_{REFM} though other reference can be functionally selected.

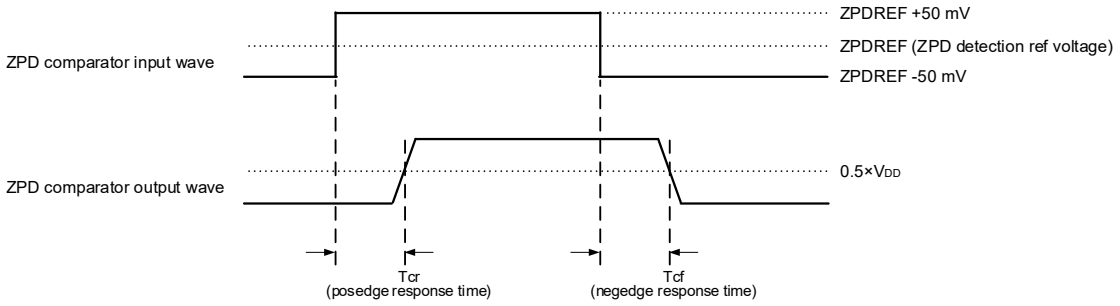
3.7.2 ZPD characteristics

T_A = -40 to +85 °C,

2.7 V ≤ EV_{DD0} = EV_{DD1} = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Threshhold voltage	V_{ZPD}	0 Point detection voltage set = 000		6/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 001		10/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 010		14/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 011		18/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 100		22/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 101		9/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 110		11/200*SMV_{DD}±40 mv			V
Detection delay	T_{ZPDD}	100 mV Step, 50 mV Overdrive (refer to the below figure)	SMV_{DD} = 4.75 V to 5.25 V			100	ns
			SMV_{DD} = 2.7 V to 5.5 V			100	ns
Operation Stabilization wait time	T_{ZPDW}	Ref voltage Stabilization +ZPD comparator Stabilization				1+5 = 6	µs

Figure 3-15. ZPD timing



3.7.3 POR characteristics

T_A = -40 to +85 °C

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}		1.45	1.51	1.57	V
	V_{PDR}		1.44	1.5	1.56	V
Detection delay	T_{PD}				300	μs
Minimum pulse width	T_{PW}	Necessary width of internal voltage drop down below V_{PDR}	300			μs

Caution LVD reset or external $\overline{\text{RESET}}$ must be used during power supply rising up to 2.7 V.

3.7.4 LVD characteristics

T_A = -40 to +85 °C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
RESET and INTMODE	V_{LVI5}	VPOC0,1,2 = 0,1,1 Power down Reset Voltage: 2.7 V		2.70	2.75	2.81	V
	V_{LVI4}	LVIS0,1 = 1,0 (+0.1 V)	Power on Reset Release Voltage	2.86	2.92	2.97	V
			Power down Interrupt Voltage	2.80	2.86	2.91	V
	V_{LVI3}	LVIS0,1 = 0,1 (+0.2 V)	Power on Reset Release Voltage	2.96	3.02	3.08	V
			Power down Interrupt Voltage	2.90	2.96	3.02	V
	V_{LVI0}	LVIS0,1 = 0,0 (+1.2 V)	Power on Reset Release Voltage	3.98	4.06	4.14	V
			Power down Interrupt Voltage	3.90	3.98	4.06	V
Detection delay time	T_{LD}					300	μs
Minimum pulse width	T_{LW}	Necessary width of V_{DD} drop down below selected V_{LVIx} (x = 0, 3 to 5)		300			μs

Caution LVD reset or external $\overline{\text{RESET}}$ must be used during power supply rising up to 2.7 V.

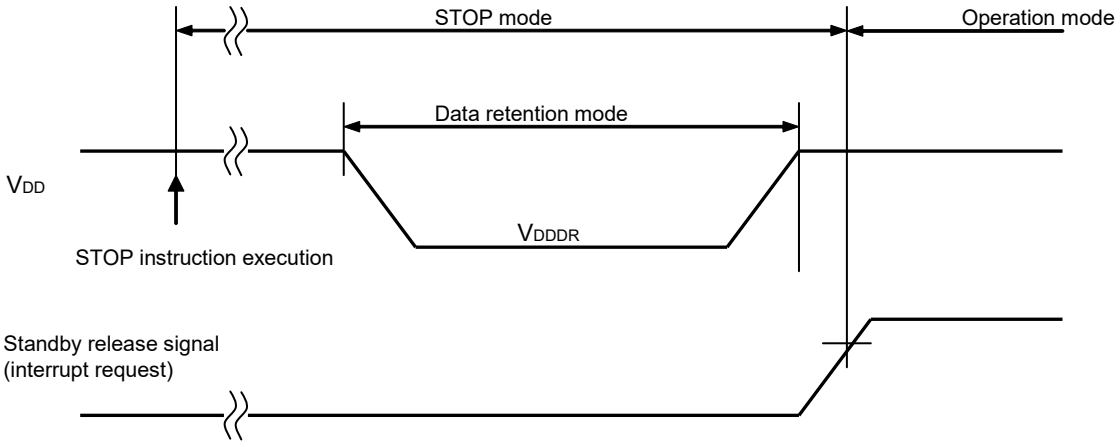
3.8 RAM Data Retention Characteristics

T_A = -40 to +85 °C

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note1		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained until a POR reset is effected, but data is not retained when a POR reset is effected.

Figure 3-16. STOP Mode Data Retention timming



3.9 Capacitance Connected to REGC

T_A = -40 to +85 °C

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Capacitance	C_{REG}		0.47		1.0	μF

3.10 Flash programming characteristics

T_A = -40 to +85 °C, 2.7 ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	Programming current			12.2	mA
System Clcok frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	2		32	MHz
Number of Code Flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	1000			Times
Number of Data Flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	10000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

4. ELECTRICAL SPECIFICATIONS (L GRADE PRODUCT)

Cautions 1. These specifications show target values, which may change after device evaluation.

2. The RL78/D1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Definition of Pin Groups

Definition of pin groups described in this chapter is shown in the following table.

Pin groups		Pin names				
		48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Pin group 1	Group 1R	P40	P40, P70, P71	P40, P70, P71	P40, P70, P71, P130 to P135, P140	P40 to P44, P70, P71, P100 to P103, P130 to P135, P140
	Group 1L	P00 to P01, P10 to P14, P30 to P33, P54 to P57, P60, P61, P72 to P75	P00 to P05, P07, P10 to P15, P17, P30 to P33, P54 to P57, P60, P61, P72 to P75	P00 to P07, P10 to P17, P30 to P37, P54 to P57,P60, P61, P65, P66, P72 to P75	P00 to P07, P10 to P17, P30 to P37, P50 to P57, P72 to P75, P136	P00 to P07, P10 to P17, P30 to P37, P45 to P47, P50 to P57, P72 to P75, P104 to P107, P110 to P117, P125 to P127 P136
	Group 1C	-	-	-	P60 to P66	P60 to P66
Pin group 2 (ANI pins)		P20 to P23, P27	P20 to P23, P27	P20 to P27	P20 to P27, P150	P20 to P27, P150 to P152
Pin group 3 (SMC pins)	Group 3A	P80 to P83	P80 to P83	P80 to P83	P80 to P83	P80 to P83
	Group 3B	-	P84 to P87	P84 to P87	P84 to P87	P84 to P87
	Group 3C	P90 to P94	P90 to P94	P90 to P93	P90 to P93	P90 to P93
	Group 3D	-	-	P94 to P97	P94 to P97	P94 to P97
	Group 3E	P90 to P94	P84 to P87, P90 to P94	-	-	-
Pin group 4 (System pins)		P121 to P122, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137	P121 to P124, $\overline{\text{RESET}}$, P137

Definition of Product Groups

Definition of product groups described in this chapter is shown in the following table.

Product groups	Product names				
	48-pin products	64-pin products	80-pin products	100-pin products	128-pin products
Product Group A	R5F10CGBLFB R5F10CGCLFB R5F10CGDLFB R5F10DGCLFB R5F10DGDLFB R5F10DGELFB	R5F10CLDLFB R5F10DLDLFB R5F10DLELFB	R5F10CMDLFB R5F10CMELFB R5F10DMDLFB R5F10DMELFB R5F10DMFLFB R5F10DMGLFB R5F10DMJLFB	R5F10DPELFB R5F10DPFLFB R5F10DPGLFB R5F10DPJLFB R5F10TPJLFB	-
Product Group B	-	-	-	R5F10DPKLFB R5F10DPLLFB	R5F10DSJLFB R5F10DSKLFB R5F10DSLLFB

4.1 Absolute Maximum Ratings

T_A = +25 °C

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	-0.5 to +6.5	V
	EV_{DD0} EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5 and -0.5 to V_{DD} + 0.3	V
	SMV_{DD0} SMV_{DD1}	$SMV_{DD0} = SMV_{DD1}$	-0.5 to +6.5 and -0.5 to V_{DD} + 0.3	V
	V_{SS}	V_{SS}	-0.5 to +0.3	V
	EV_{SS0} EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
	SMV_{SS0} SMV_{SS1}	$SMV_{SS0} = SMV_{SS1}$	-0.5 to +0.3	V
Supply voltage up/down ramp	V_{DDRAMP}		≤50	V/ms
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note1	V
Input voltage	V_{I1}	Pin group 1	-0.3 to +6.5 and -0.3 to EV_{DD0}(EV_{DD1}) + 0.3	V
	V_{I2}	Pin group 2	-0.3 to +6.5 and -0.3 to V_{DD} + 0.3	V
	V_{I3}	Pin group 3	-0.3 to +6.5 and -0.3 to SMV_{DD0}(SMV_{DD1}) + 0.3	V
	V_{I4}	Pin group 4	-0.3 to +6.5 and -0.3 to V_{DD} + 0.3	V

(Continue to next page)

T_A = +25 °C

Parameter	Symbols	Conditions			Ratings	Unit
Output voltage	V_{O1}	Pin group 1			-0.3 to EV_{DD0} (EV_{DD1}) + 0.3	V
	V_{O2}	Pin group 2			-0.3 to V_{DD} + 0.3	V
	V_{O3}	Pin group 3			-0.3 to SMV_{DD0} (SMV_{DD1}) + 0.3	V
	V_{COM}	COM0 to COM3			-0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin	Pin group 1		-20	mA
		Total	Pin group 1		-150	mA
				Pin group 1L	-60	mA
				Pin group 1R	-55	mA
				Pin group 1C	-40	mA
	I_{OH2}	Per pin	Pin group 2		-0.5	mA
		Total			-2.0	mA
	I_{OH3}	Per pin	Pin group 3		-58	mA
		Total	Pin group 3	48-pin, 64-pin	-270	mA
				80-pin, 100-pin, 128-pin	-480	mA
				Pin group 3A	-120	mA
				Pin group 3B	-120	mA
				Pin group 3C	-120	mA
				Pin group 3D	-120	mA
				Pin group 3E	-150	mA
	I_{OHCOM}	Per pin	COM0 to COM3		-0.5	mA
		Total	COM0 to COM3		-1.0	mA
Output current, low	I_{OL1}	Per pin	Pin group 1		20	mA
		Total	Pin group 1		150	mA
				Pin group 1L	60	mA
				Pin group 1R	50	mA
				Pin group 1C	40	mA
	I_{OL2}	Per pin	Pin group 2		1.0	mA
		Total			5.0	mA
	I_{OL3}	Per pin	Pin group 3		58	mA
		Total	Pin group 3	48-pin, 64-pin	270	mA
				80-pin, 100-pin, 128-pin	480	mA
				Pin group 3A	120	mA
				Pin group 3B	120	mA
				Pin group 3C	120	mA
				Pin group 3D	120	mA
				Pin group 3E	150	mA
	I_{OLCOM}	Per pin	COM0 to COM3		0.5	mA
		Total	COM0 to COM3		1.0	mA
Operating ambient temperature	T_A	for normal operation mode			-40 to +105	°C
		for code flash programming			-40 to +105	°C
		for data flash programming			-40 to +105	°C
Storage temperature	T_{stg}				-65 to +150	°C

Note Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

4.2 Power consumption characteristics

4.2.1 Product group A

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, run mode	I_{DD1} Note 1	High speed MAIN RUN Note 2, 3, 4	f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	4.2	18	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	3.8	16	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	2.1	11	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	1.6	9	mA
				f_X = 4 MHz			
		SUB RUN Note 2, 3, 5	f_{CLK} = f_{XT} = 32.768 kHz		6	500	μA

Notes 1. The common condition for I_{DD1}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The program is running in the code flash.

2. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

3. The maximum value is that when all peripheral devices are operating. But the A/D converter, RTC, LCD circuit and stepper motor circuit are stopped, and the data flash and the code flash are stated to read mode. The 16-bit wakeup timer operates with f_{LOCO}.

4. In case of I_{DD1} of "f_X = 4/8 MHz with PLL", the high speed on-chip oscillator (HOCO) is stopped.

5. f_X and f_{HOCO} are stopped.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, halt mode	I_{DD2} Note 1	High speed MAIN HALT Note 3, 4, 5	f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	0.8	6.9	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	0.7	6.0	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	0.4	4.3	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	0.35	3.6	mA
				f_X = 4 MHz			
		SUB HALT Note 3, 4, 6	f_{CLK} = f_{XT} = 32.768 kHz	RTC is stopped	1.0	190	μA
				RTC is operated by f_{XT} = 32.768 kHz	1.2		
Supply current, stop mode	I_{DD3} Note 2	STOP Note 3, 4	RTC and f_{XT} are stopped		0.4	120	μA
			RTC is operated by f_{XT} = 32.768 kHz		0.8		

Notes 1. The common condition for I_{DD2}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The HALT instruction is executed by the program in the code flash.
- The specification shows the stable current during HALT mode.

2. The common condition for I_{DD3}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The STOP instruction is executed by the program in the code flash during MAIN RUN operation.
- The spec shows the stable current during STOP mode.

3. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

4. The maximum value is that when all peripheral devices are operating. But the A/D converter, LCD circuit, stepper motor circuit, the data flash and the code flash are stopped. The 16-bit wakeup timer operates with f_{LOCO}.

5. Either f_X or f_{HOCO} which is selected for f_{CLK} is operated. The other is stopped.

6. f_X and f_{HOCO} are stopped.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Typ.	Max.	Unit
WDT operating current Note 1	I_{WDT}			0.25	2.0	μA
ADC operating current Note 2	I_{ADC}	Normal mode	V_{DD} = 5.0 V	1.3	1.7	mA
		Low voltage mode	V_{DD} = 3.0 V	0.5	0.7	mA
LCD operating Current Note 3	I_{LCD}	f_{LCD} = f_{SUB}, LCD clock = 512 Hz	V_{DD} = 5.0 V	100	210	μA
			V_{DD} = 3.0 V	90	200	μA
ZPD operating current Note 4	I_{ZPD}	One ZPD operated	V_{DD} = 5.0 V	150	600	μA
			V_{DD} = 3.0 V	100	500	μA
		Four ZPDs operated	V_{DD} = 5.0 V	500	2000	μA
			V_{DD} = 3.0 V	400	1600	μA

Notes
1. Current flowing only to the watchdog timer. The maximum specification of I_{DD1}, I_{DD2} and I_{DD3} include I_{WDT}.
2. Current flowing only to the A/D converter.The current value of the RL78/D1A is the sum of I_{DD} and I_{ADC} when the A/D converter operates.
3. Current flowing only to the LCD controller/driver circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{LCD} when the LCD controller/driver circuit operates.
4. Current flowing only to the ZPD circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{ZPD} when the ZPD circuit operates.

4.2.2 Product group B

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, run mode	I_{DD1} Note 1	High speed MAIN RUN Note 2, 3, 4, 5	f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	4.7	20	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	4.3	17.5	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	2.4	12	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	1.8	9.5	mA
				f_X = 4 MHz			
		SUB RUN Note 2, 3, 6	f_{CLK} = f_{XT} = 32.768 kHz		7	560	μA

Notes 1. The common condition for I_{DD1}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The program is running in the code flash.

2. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

3. The maximum value is that when all peripheral devices are operating. But the A/D converter, RTC, LCD circuit and stepper motor circuit are stopped, and the data flash and the code flash are stated to read mode. The 16-bit wakeup timer operates with f_{LOCO}.

4. In case of I_{DD1} of "f_X = 4/8 MHz with PLL", the high speed on-chip oscillator (HOCO) is stopped.

5. At 128-pin products, the value of I_{DD1} does not include the LCDB (P11x, P46-7) pin toggle current.
I_{DD1} condition of LCDB macro is f_{CLK}=24MHz, mod8 mode, data rate=6MHz, 4cycle, 16bit write/read.

6. f_X and f_{HOCO} are stopped.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions			Typ.	Max.	Unit
Supply current, halt mode	I_{DD2} Note 1	High speed MAIN HALT Note 3, 4, 5	f_{CLK} = 24 MHz	f_{HOCO} = 24 MHz	0.8	7.5	mA
				f_{HOCO} = 4 MHz with PLL			
				f_X = 4 MHz with PLL			
				f_X = 8 MHz with PLL			
			f_{CLK} = 20 MHz	f_X = 20 MHz	0.7	6.5	mA
			f_{CLK} = 8 MHz	f_{HOCO} = 8 MHz	0.4	4.5	mA
				f_X = 8 MHz			
			f_{CLK} = 4 MHz	f_{HOCO} = 4 MHz	0.35	3.8	mA
				f_X = 4 MHz			
		SUB HALT Note 3, 4, 6	f_{CLK} = f_{XT} = 32.768 kHz	RTC is stopped	1.0	200	μA
				RTC is operated by f_{XT} = 32.768 kHz	1.2		
Supply current, stop mode	I_{DD3} Note 2	STOP Note 3, 4	RTC and f_{XT} are stopped		0.4	130	μA
			RTC is operated by f_{XT} = 32.768 kHz		0.8		

Notes 1. The common condition for I_{DD2}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The HALT instruction is executed by the program in the code flash.
- The specification shows the stable current during HALT mode.

2. The common condition for I_{DD3}:
- I_{DD} includes the total current flowing into whole power pins, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}.
- The STOP instruction is executed by the program in the code flash during MAIN RUN operation.
- The spec shows the stable current during STOP mode.

3. The typical value is that when Ta=+25deg.C and V_{DD}=5.0 V. Peripheral devices and the data flash are stopped.

4. The maximum value is that when all peripheral devices are operating. But the A/D converter, LCD circuit, stepper motor circuit, the data flash and the code flash are stopped. The 16-bit wakeup timer operates with f_{LOCO}.

5. Either f_X or f_{HOCO} which is selected for f_{CLK} is operated. The other is stopped.

6. f_X and f_{HOCO} are stopped.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Typ.	Max.	Unit
WDT operating current Note 1	I_{WDT}			0.25	1.0	μA
ADC operating current Note 2	I_{ADC}	Normal mode	V_{DD} = 5.0 V	1.3	1.7	mA
		Low voltage mode	V_{DD} = 3.0 V	0.5	0.7	mA
LCD operating Current Note 3	I_{LCD}	f_{LCD} = f_{SUB}, LCD clock = 512 Hz	V_{DD} = 5.0 V	100	140	μA
			V_{DD} = 3.0 V	90	130	μA
ZPD operating current Note 4	I_{ZPD}	One ZPD operated	V_{DD} = 5.0 V	150	600	μA
			V_{DD} = 3.0 V	100	500	μA
		Four ZPDs operated	V_{DD} = 5.0 V	500	2000	μA
			V_{DD} = 3.0 V	400	1600	μA

Notes
1. Current flowing only to the watchdog timer. The maximum specification of I_{DD1}, I_{DD2} and I_{DD3} include I_{WDT}.
2. Current flowing only to the A/D converter.The current value of the RL78/D1A is the sum of I_{DD} and I_{ADC} when the A/D converter operates.
3. Current flowing only to the LCD controller/driver circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{LCD} when the LCD controller/driver circuit operates.
4. Current flowing only to the ZPD circuit. The current value of the RL78/D1A is the sum of I_{DD} and I_{ZPD} when the ZPD circuit operates.

4.3 Oscillator characteristics

4.3.1 Main(X1) oscillator characteristics

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Main(X1) clock oscillation frequency	f_X	Ceramic resonator	1.0		20.0	MHz
		Crystal resonator	1.0		20.0	MHz

Remark Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.3.2 High speed on chip oscillator characteristics

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
HOCO oscillation frequency	f_{HOCO}	4 MHz mode	3.88	4.00	4.12	MHz
		8 MHz mode	7.76	8.00	8.24	MHz
		16 MHz mode	15.52	16.00	16.48	MHz
		24 MHz mode	23.28	24.00	24.72	MHz

Remark Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.3.3 Low speed on chip oscillator characteristics

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
LOCO oscillation frequency	f_{LOCO}		12.75	15.0	17.25	kHz

4.3.4 Sub(XT1) oscillator characteristics

T_A = -40 to +105 °C, 2.7 V≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Sub(XT1) clock oscillation frequency	f_{XT}	Possible to oscillate	29.0	32.768	35.0	kHz

Remark Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.4 DC characteristics

4.4.1 Pin group 1

T_A = -40 to +105 °C, 4.0 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V (1/2)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin				-5.0	mA
	I_{OH2}	Per pin, P73 or P135 (SG port)				-13.0	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note 2])	Group 1L			-40.0	mA
			Group 1R			-40.0	mA
			Group 1C (128-pin, 100-pin)			-30.0	mA
		for 128-pin, 100-pin				-110.0	mA
		for 80-pin, 64-pin, 48-pin				-60.0	mA
Output current, low	I_{OL1}	Per pin				8.5	mA
	I_{OL2}	Per pin, P73 or P135 (SG ports)				13.0	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note 3])	Group 1L			40.0	mA
			Group 1R			35.0	mA
			Group 1C (128-pin, 100-pin)			40.0	mA
		for 128-pin, 100-pin				115.0	mA
		for 80-pin, 64-pin, 48-pin				60.0	mA

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins ($I_{OH} \times 0.7$)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -30.0 mA

Total output current of pins = (-30.0 × 0.7)/(80 × 0.01) ≈ -26.2 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins ($I_{OL} \times 0.7$)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 40.0 mA

Total output current of pins = (40.0 × 0.7)/(80 × 0.01) = 35.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

T_A = -40 to +105 °C, 4.0 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V (2/2)

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Input voltage, high Note 2	V_{IH1}	Schmitt3 mode	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	Schmitt1 mode Note 3	0.65EV_{DD}		EV_{DD}	V
Input voltage, low Note 2	V_{IL1}	Schmitt3 mode	0		0.5EV_{DD}	V
	V_{IL2}	Schmitt1 mode Note 3	0		0.35EV_{DD}	V
Input hysteresis width Note 2, 4	V_{IHYS1}	Schmitt3 mode	0.1	0.19	0.29	V
	V_{IHYS2}	Schmitt1 mode Note 3	0.15	0.59	0.84	V
Output voltage, high Note 1	V_{OH1}	I_{OH} = -5.0 mA	EV_{DD}-1.0		EV_{DD}	V
		I_{OH} = -3.0 mA up to 6 pins	EV_{DD}-0.5		EV_{DD}	V
	V_{OH2}	I_{OH} = -13.0 mA, P73 or P135 (SG port)	EV_{DD}-0.7		EV_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 8.5 mA	0		0.7	V
		I_{OL} = 3.0 mA up to 6 pins	0		0.5	V
	V_{OL2}	I_{OL} = 13.0 mA, P73 or P135 (SG port)	0		0.7	V
Input leakage current, high	I_{LIH1}	V_I = EV_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = EV_{SS}			-1	μA
On chip pull-up resistance Note 5	R_U	V_I = EV_{SS}	10	20	100	kΩ
On chip pull-down resistance Note 6	R_D	V_I = EV_{DD}	100			kΩ

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. Except P130 because it is output only port.

3. P01, P10, P11, P17, P31, P40, P50 to P52, P55 to P57, P61, P63, P70, P110 to P117, P135 only.

4. This value is defined by evaluation result.

5. Except P130 and P137. Pull-up resistance is connected by software when pin is set to input mode.

6. LCD segment shared pins only. Pull-down resistance is connected during reset.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

T_A = -40 to +105 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ 4.0 V, EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, VSS = EV_{SS0} = EV_{SS} = 0 V (1/2)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin				-1.0	mA
	I_{OH2}	Per pin, P73 or P135 (SG port)				-7.5	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note 2])	Group 1L			-15.0	mA
			Group 1R			-30.0	mA
			Group 1C (128-pin, 100-pin)			-7.0	mA
		for 128-pin, 100-pin				-52.0	mA
		for 80-pin, 64-pin, 48-pin				-33.0	mA
Output current, low	I_{OL1}	Per pin				1.5	mA
	I_{OL2}	Per pin, P73 or P135 (SG ports)				7.0	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note 3])	Group 1L			18.0	mA
			Group 1R			30.0	mA
			Group 1C (128-pin, 100-pin)			10.0	mA
		for 128-pin, 100-pin				58.0	mA
		for 80-pin, 64-pin, 48-pin				35.0	mA

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -7.0 mA

Total output current of pins = (-7.0 × 0.7)/(80 × 0.01) ≈ -6.1 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

T_A = -40 to +105 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ 4.0 V, EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, VSS = EV_{SS0} = EV_{SS} = 0 V (2/2)

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Input voltage, high Note 2	V_{IH1}	Schmitt3 mode	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	Schmitt1 mode Note 3	0.7EV_{DD}		EV_{DD}	V
Input voltage, low Note 2	V_{IL1}	Schmitt3 mode	0		0.4EV_{DD}	V
	V_{IL2}	Schmitt1 mode Note 3	0		0.3EV_{DD}	V
Input hysterisis width Note 2, 4	V_{IHYS1}	Schmitt3 mode	0.05		0.21	V
	V_{IHYS2}	Schmitt1 mode Note 3	0.08		0.53	V
Output voltage, high Note 1	V_{OH1}	I_{OH} = -1.0 mA	EV_{DD}-0.5		EV_{DD}	V
	V_{OH2}	I_{OH} = -7.5 mA, P73 or P135 (SG port)	EV_{DD}-0.7		EV_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 1.5 mA	0		0.5	V
	V_{OL2}	I_{OL}= 7.0 mA, P73 or P135 (SG port)	0		0.7	V
Input leakage current, high	I_{LIH1}	V_I = EV_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = EV_{SS}			-1	μA
On chip pull-up resistance Note 5	R_U	V_I = EV_{SS}	10	20	100	kΩ
On chip pull-down resistance Note 6	R_D	V_I = EV_{DD}	100			kΩ

Notes 1. When P60 or P61 is set to Nch open drain mode, it does not drive high level output.

2. Except P130 because it is output only port.

3. P01, P10, P11, P17, P31, P40, P50 to P52, P55 to P57, P61, P63, P70, P110 to P117, P135 only.

4. This value is defined by evaluation result.

5. Except P130 and P137. Pull-up resistance is connected by software when pin is set to input mode.

6. LCD segment shared pins only. Pull-down resistance is connected during reset.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

4.4.2 Pin group 2 (ANI pins)

T_A = -40 to +105 °C, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin			-0.1	mA
	$I_{OHTOTAL}$	Total			-0.8	mA
Output current, low	I_{OL1}	Per pin			0.4	mA
	$I_{OLTOTAL}$	Total			3.2	mA
Input voltage, high	V_{IH1}		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}		0		0.5V_{DD}	V
Input hysteresis width Note	V_{IHYS1}		0.1	0.19	0.29	V
Output voltage, high	V_{OH1}	I_{OH} = -0.1 mA	V_{DD}-0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 0.4 mA	0		0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = V_{SS}			-1	μA

Note This specification is guaranteed by design. It is not tested when shipment.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 4.0 V, V_{SS} = 0 V

Parameter	Symbols	Conditions	Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin			-0.1	mA
	$I_{OHTOTAL}$	Total			-0.8	mA
Output current, low	I_{OL1}	Per pin			0.4	mA
	$I_{OLTOTAL}$	Total			3.2	mA
Input voltage, high	V_{IH1}		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}		0		0.4V_{DD}	V
Input hysteresis width Note	V_{IHYS1}		0.05		0.21	V
Output voltage, high	V_{OH1}	I_{OH} = -0.1 mA	V_{DD}-0.5		V_{DD}	V
Output voltage, low	V_{OL1}	I_{OL} = 0.4 mA	0		0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}			1	μA
Input leakage current, low	I_{LIL1}	V_I = V_{SS}			-1	μA

Note This specification is guaranteed by design. It is not tested when shipment.

4.4.3 Pin group 3 (SMC pins)

T_A = -40 to +105 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (1/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin		T_A = -40 °C			-52	mA
				T_A = +25 °C			-39	mA
				T_A = +85 °C			-32	mA
				T_A = +105 °C			-32	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			-96	mA
			Group 3B	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			-96	mA
			Group 3C 128-pin, 100-pin 80-pin	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			-96	mA
			Group 3C 64-pin 48-pin	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			-96	mA
			Group 3D (128-pin, 100-pin, 80-pin)	T_A = -40 °C			-118	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			-96	mA
			Group 3E (64-pin, 48-pin)	T_A = -40 °C			-148	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			-96	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%. The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins $(I_{OH} \times 0.7)/(n \times 0.01)$

<Example> Where n = 80% and I_{OH} = -118.0 mA

Total output current of pins = $(-118.0 \times 0.7)/(80 \times 0.01) \approx -103.2$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +105 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (2/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, low	I_{OL1}	Per pin		T_A = -40 °C			52	mA
				T_A = +25 °C			39	mA
				T_A = +85 °C			32	mA
				T_A = +105 °C			32	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A	T_A = -40 °C			118	mA
				T_A = +25 °C			118	mA
				T_A = +85 °C			96	mA
				T_A = +105 °C			96	mA
			Group 3B	T_A = -40 °C			118	mA
				T_A = +25 °C			118	mA
				T_A = +85 °C			96	mA
				T_A = +105 °C			96	mA
			Group 3C	128-pin, 100-pin 80-pin T_A = -40 °C			118	mA
				128-pin, 100-pin 80-pin T_A = +25 °C			118	mA
				128-pin, 100-pin 80-pin T_A = +85 °C			96	mA
				128-pin, 100-pin 80-pin T_A = +105 °C			96	mA
				64-pin 48-pin T_A = -40 °C			118	mA
				64-pin 48-pin T_A = +25 °C			118	mA
				64-pin 48-pin T_A = +85 °C			96	mA
				64-pin 48-pin T_A = +105 °C			96	mA
			Group 3D (128-pin, 100-pin, 80-pin)	T_A = -40 °C			118	mA
				T_A = +25 °C			118	mA
				T_A = +85 °C			96	mA
				T_A = +105 °C			96	mA
			Group 3E (64-pin, 48-pin)	T_A = -40 °C			-148	mA
				T_A = +25 °C			-118	mA
				T_A = +85 °C			-96	mA
				T_A = +105 °C			96	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 118.0 mA
Total output current of pins = (118.0 × 0.7)/(80 × 0.01) ≈ 103.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +105 °C, 4.0 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (3/3)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}			0.8SMV_{DD}		SMV_{DD}	V
Input voltage, low	V_{IL1}			0		0.5SMV_{DD}	V
Input hysteresis width Note 1	V_{IHYS1}			0.1	0.19	0.29	V
Output voltage, high	V_{OH1}	T_A = -40 °C	I_{OH} = -52 mA	SMV_{DD} - 0.5		SMV_{DD}	V
		T_A = +25 °C	I_{OH} = -39 mA				
		T_A = +85 °C	I_{OH} = -32 mA				
		T_A = +105 °C	I_{OH} = -32 mA				
Output voltage, low	V_{OL1}	T_A = -40 °C	I_{OL} = 52 mA	0		0.5	V
		T_A = +25 °C	I_{OL} = 39 mA				
		T_A = +85 °C	I_{OL} = 32 mA				
		T_A = +105 °C	I_{OL} = 32 mA				
Output voltage deviation Note 2	V_{DEV}			0		50	mV
Input leakage current, high	I_{LIH1}	V_I = SMV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	V_I = SMV_{SS}				-1	μA
On chip pull-up resistance Note 3	R_U	V_I = SMV_{SS}		10	20	100	kΩ
On chip pull-down resistance Note 4	R_D	V_I = SMV_{DD}		100			kΩ

Notes 1. This specification is guaranteed by design. It is not tested when shipment.

2. Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (|V_{OHx}-V_{OHy}|, |V_{OLx}-V_{OLy}|) @I_{OHx} = I_{OHy}, I_{OLx} = I_{OLy}.
X and y denote any combination of two pins of the following pin groups: (P80-P83, P84-P87, P90-P93, P94-P97)

3. Pull-up resistance is connected by software when pin is set to input mode.

4. LCD segment shared pins only. Pull-down resistance is connected during reset.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 4.0 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (1/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, high	I_{OH1}	Per pin		T_A = -40 °C			-30	mA
				T_A = +25 °C			-25	mA
				T_A = +85 °C			-23	mA
				T_A = +105 °C			-22	mA
	$I_{OHTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A	T_A = -40 °C			-90	mA
				T_A = +25 °C			-75	mA
				T_A = +85 °C			-69	mA
				T_A = +105 °C			-66	mA
			Group 3B	T_A = -40 °C			-90	mA
				T_A = +25 °C			-75	mA
				T_A = +85 °C			-69	mA
				T_A = +105 °C			-66	mA
			Group 3C 128-pin, 100-pin 80-pin	T_A = -40 °C			-90	mA
				T_A = +25 °C			-75	mA
				T_A = +85 °C			-69	mA
				T_A = +105 °C			-66	mA
			Group 3C 64-pin 48-pin	T_A = -40 °C			-90	mA
				T_A = +25 °C			-75	mA
				T_A = +85 °C			-69	mA
				T_A = +105 °C			-66	mA
			Group 3D (128-pin, 100-pin, 80-pin)	T_A = -40 °C			-90	mA
				T_A = +25 °C			-75	mA
				T_A = +85 °C			-69	mA
				T_A = +105 °C			-66	mA
			Group 3E (64-pin, 48-pin)	T_A = -40 °C			-90	mA
				T_A = +25 °C			-75	mA
				T_A = +85 °C			-69	mA
				T_A = +105 °C			-66	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -75.0 mA

Total output current of pins = (-75.0 × 0.7)/(80 × 0.01) ≈ -65.6 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 4.0 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (2/3)

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Output current, low	I_{OL1}	Per pin		T_A = -40 °C			30	mA
				T_A = +25 °C			23	mA
				T_A = +85 °C			20	mA
				T_A = +105 °C			17	mA
	$I_{OLTOTAL}$	Total (for duty factors ≤ 70%[Note])	Group 3A	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
				T_A = +105 °C			51	mA
			Group 3B	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
				T_A = +105 °C			51	mA
			Group 3C	128-pin, 100-pin 80-pin T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
				T_A = +105 °C			51	mA
				64-pin 48-pin T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
				T_A = +105 °C			51	mA
			Group 3D (128-pin, 100-pin, 80-pin)	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
				T_A = +105 °C			51	mA
			Group 3E (64-pin, 48-pin)	T_A = -40 °C			90	mA
				T_A = +25 °C			69	mA
				T_A = +85 °C			60	mA
				T_A = +105 °C			51	mA

Note These output current values are obtained under the condition that the duty factor is no greater than 70%.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 69.0 mA
Total output current of pins = (69.0 × 0.7)/(80 × 0.01) ≈ 60.3 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 4.0 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V (3/3)

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}			0.8SMV_{DD}		SMV_{DD}	V
Input voltage, low	V_{IL1}			0		0.4SMV_{DD}	V
Input hysteresis width Note 1	V_{IHYS1}			0.05		0.21	V
Output voltage, high	V_{OH1}	T_A = -40 °C	I_{OH} = -30 mA	SMV_{DD} -0.5		SMV_{DD}	V
		T_A = +25 °C	I_{OH} = -25 mA				
		T_A = +85 °C	I_{OH} = -23 mA				
		T_A = +105 °C	I_{OH} = -22 mA				
Output voltage, low	V_{OL1}	T_A = -40 °C	I_{OL} = 30 mA	0		0.5	V
		T_A = +25 °C	I_{OL} = 23 mA				
		T_A = +85 °C	I_{OL} = 20 mA				
		T_A = +105 °C	I_{OL} = 17 mA				
Output voltage deviation Note 2	V_{DEV}			0		50	mV
Input leakage current, high	I_{LIH1}	V_I = SMV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	V_I = SMV_{SS}				-1	μA
On chip pull-up resistance Note 3	R_U	V_I = SMV_{SS}		10	20	100	kΩ
On chip pull-down resistance Note 4	R_D	V_I = SMV_{DD}		100			kΩ

Notes 1. This specification is guaranteed by design. It is not tested when shipment.

2. Output voltage deviation defines the difference of the outputs levels of the same stepper motor.
V_{DEV} = max (|V_{OHx}-V_{OHy}|, |V_{OLx}-V_{OLy}|) @I_{OHx} = I_{OHy}, I_{OLx} = I_{OLy}.
X and y denote any combination of two pins of the following pin groups: (P80-P83, P84-P87, P90-P93, P94-P97)

3. Pull-up resistance is connected by software when pin is set to input mode.

4. LCD segment shared pins only. Pull-down resistance is connected during reset.

4.4.4 Pin group 4 (OSC, reset and P137 pins)

T_A = -40 to +105 °C, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.8V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$		0.65V_{DD}		V_{DD}	V
	V_{IH3}	P137		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0		0.2V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$		0		0.35V_{DD}	V
	V_{IL3}	P137		0		0.5V_{DD}	V
Input hysteresis width Note 2	V_{IHYS1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.1	0.7		V
	V_{IHYS2}	$\overline{\text{RESET}}$		0.15	0.59	0.84	V
Input leakage current, high	I_{LIH1}	P121, P122, P123, P124 $V_I = V_{DD}$	Port			1	μA
			EXCLK Note 1			1	μA
			OSC			10	μA
	I_{LIH2}	$\overline{\text{RESET}}$, $V_I = V_{DD}$				1	μA
	I_{LIH3}	P137, $V_I = V_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P121, P122, P123, P124 $V_I = V_{SS}$	Port			-1	μA
			EXCLK Note 1			-1	μA
			OSC			-10	μA
	I_{LIL2}	$\overline{\text{RESET}}$, $V_I = V_{SS}$				-1	μA
	I_{LIL3}	P137, $V_I = V_{SS}$				-1	μA

Notes 1. P122(EXCLK) only.

2. This specification is guaranteed by design. It is not tested when shipment.

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 4.0 V, V_{SS} = 0 V

Parameter	Symbols	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.8V_{DD}		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$		0.7V_{DD}		V_{DD}	V
	V_{IH3}	P137		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0		0.2V_{DD}	V
	V_{IL2}	$\overline{\text{RESET}}$		0		0.3V_{DD}	V
	V_{IL3}	P137		0		0.4V_{DD}	V
Input hysteresis width Note 2	V_{IHYS1}	P121, P122, P123, P124 (Port or EXCLK Note 1)		0.08			V
	V_{IHYS2}	$\overline{\text{RESET}}$		0.08		0.53	V
Input leakage current, high	I_{LIH1}	P121, P122, P123, P124 $V_I = V_{DD}$	Port			1	μA
			EXCLK Note 1			1	μA
			OSC			10	μA
	I_{LIH2}	$\overline{\text{RESET}}$, $V_I = V_{DD}$				1	μA
	I_{LIH3}	P137, $V_I = V_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P121, P122, P123, P124 $V_I = V_{SS}$	Port			-1	μA
			EXCLK Note 1			-1	μA
			OSC			-10	μA
	I_{LIL2}	$\overline{\text{RESET}}$, $V_I = V_{SS}$				-1	μA
	I_{LIL3}	P137, $V_I = V_{SS}$				-1	μA

Notes 1. P122(EXCLK) only.

2. This specification is guaranteed by design. It is not tested when shipment.

4.5 AC characteristics

4.5.1 Basic operation

T_A = -40 to +105 °C,

2.7 V ≤ = EV_{DD0} = EV_{DD1} ≤ V_{DD} = SMV_{DD0} = SMV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Parameter	Symbols	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock operation (Including PLL)	High speed main run		0.04166 Note 1		1	μs
		Sub system clock operation	SDIV = 0		1/f_{XT} (Typ. 30.5)			μs
External main system clock frequency	f_{EX}	Square wave input to EXCLK			2		20	MHz
External main system clock (square wave) input high/low level width	t_{EXH} t_{EXL}	Square wave input to EXCLK			24			ns
Timer input high/low level width	t_{TIH} t_{TIL}	TI00 to TI07, TI10 to TI17, TI20 to TI27			1/f_{MCK}+10 Note 2			ns
Port output frequency	f_{GPO}	P80 to P87, P90 to P97	C = 30 pF	4.0 V ≤ SMV_{DD}			2	MHz
		P20 to P27, P150 to P152	C = 30 pF	4.0 V ≤ V_{DD}			2	MHz
		P73,P135	C = 30 pF	4.0 V ≤ EV_{DD}			8	MHz
		Other than the above	C = 30 pF	4.0 V ≤ EV_{DD}			16	MHz
				2.7 V ≤ EV_{DD} < 4.0 V			8	MHz
External interrupt input high/low level width Note 3	t_{INIH} t_{INIL}	INTP0 to INTP5, INTPLR0, INTPLR1			1			μs
$\overline{RESET}$ input low level width Note 3	t_{RSL}	$\overline{RESET}$			10			μs
Analog noise filter rejection pulse width Note 4	t_{WRJ}	INTP0 to INTP5, INTPLR0, INTPLR1, ADTRG			30	50	1000	ns
ADTRG input high level width	t_{ATH}	Without noise filter		AWC=0	1/f_{CLK}+10			ns
				AWC=1	10			ns
		With noise filter		AWC=0	1/f_{CLK}+10 or t_{WRJ} (Note 5)			ns
				AWC=1	t_{WRJ} (Note 5)			ns

Notes 1. Value is in case of f_{CLK} is 24.0 MHz. It is also allowed to exceed frequency up to +3%.

2. f_{MCK} shows the frequency value of operation clock for TAU. Usually, f_{MCK} is defined by MHz but this specification is defined by ns. It is not defined by μs, so please be careful.

3. Pulses longer than this value will pass the input filter.

4. Pulses shorter than this value do not pass the input filters.

5. If the value of "1/f_{CLK}+10 [ns]" is less than tWRJ, please use t_{WRJ} value instead of "1/f_{CLK} +10 [ns]".

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 4-1. AC Timing Test Points

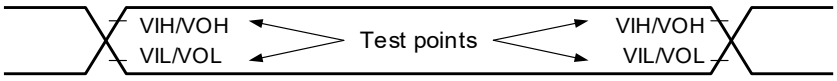


Figure 4-2. External Main System Clock Timing

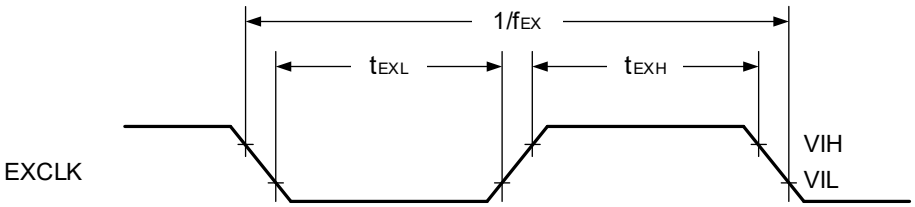


Figure 4-3. TI Timing

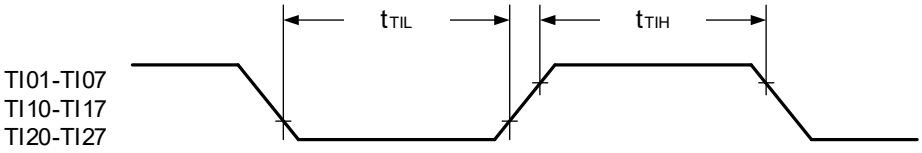


Figure 4-4. Interrupt Request Input Timing

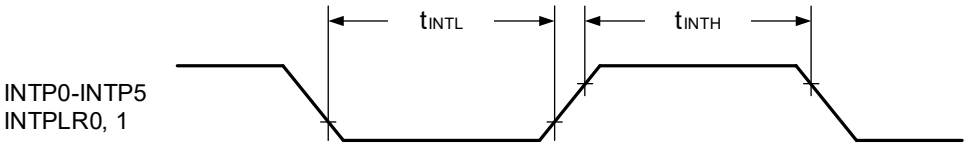
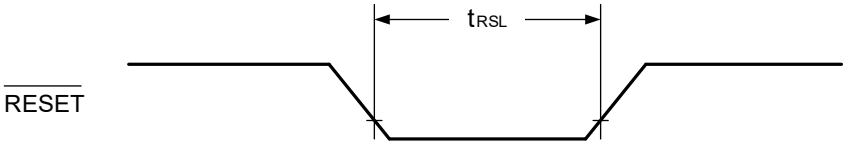


Figure 4-5. $\overline{\text{RESET}}$ Input Timing



4.5.2 Stepper motor controller/driver

T_A = -40 to +105 °C,

2.7 V ≤ = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Meter Controller/Driver input frequency	f_{MC} Note 1					24	MHz
PWM output rise time	t_R	10%-90% Note 2	4.0 V ≤ SMV_{DD} ≤ 5.5 V	15	60	100	ns
			2.7 V ≤ SMV_{DD} ≤ 4.0 V	20		500	ns
PWM output fall time	t_F	10%-90% Note 2	4.0 V ≤ SMV_{DD} 5.5 V	15	60	100	ns
			2.7 V ≤ SMV_{DD} ≤ 4.0 V	20		500	ns
Peak Cross Current Note 3	I_{CROSS}					50	ns
Output Pulse Width Note 4	t_{MO}	4.0 V ≤ SMV_{DD} ≤ 5.5 V		250			ns
		2.7 V ≤ SMV_{DD} ≤ 5.5 V		5000			ns
Output Pulse Length Deviation Note 5	t_{SMDEV}	4.0 V ≤ SMV_{DD} ≤ 5.5 V		-65	-12	+10	ns
		2.7 V ≤ SMV_{DD} ≤ 5.5 V		-100		+400	ns
Symmetry performance Note 6	ΔHSPmn	IOH = -32 mA ΔHSPmn = | VOH[(SMmn)max - (SMmn)min] |	2.7 V ≤ SMV_{DD} ≤ 5.5 V			50	mV
	ΔHSPmn	IOL = 32 mA ΔHSPmn = | VOL[(SMmn)max - (SMmn)min] |	4.0 V ≤ SMV_{DD} ≤ 5.5 V			50	mV
			2.7 V ≤ SMV_{DD} ≤ 5.5 V			100	mV

Notes 1. Source clock of the free-running counter.

2. t_R,t_F is not tested in production, specified by design.

3. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transition time t_R, t_F. It flows in addtion to the output current. The cross current is not tested,but derived from simulation.

4. The output buffer can not generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested,but derived from simulation.

5. The slew rate control function causes a deviation of output pulse time compared to the ideal selected output pulse setting. This value is not tested,but derived from simulation.

6. Indicates the dispersion of 16 PWM output voltages.(4 buffers' output voltage differences in the state of I_{OH}(I_{OL}) at the same time.) Not tested in production, specified by design.

Remark m = 1 to 4, n = 1 to 4

4.5.3 Sound generator

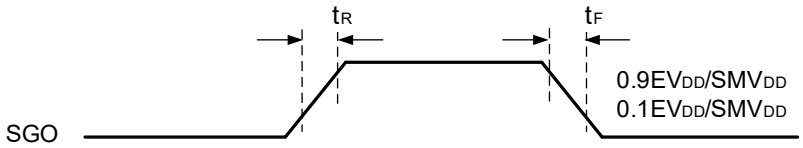
T_A = -40 to +105 °C,

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Sound generator input frequency	f_{SG}					24	MHz
SGO output rise time	t_R	C = 100 pF	P73, P135			200	ns
			P93			500	ns
SGO output fall time	t_F	C = 100 pF	P73, P135			200	ns
			P93			500	ns

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Sound Generator Output Timing



4.5.4 Serial interface: CSI operation

<Master mode>

T_A = -40 to +105 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.		Max.	Unit
SCK cycle time	t_{KCY1}	4.0≤V_{DD}	167	t_{KCY1}≥4/f_{CLK} Note		ns
		V_{DD}<4.0 V	250			ns
SCK high/low level width	t_{KH1}	4.0≤V_{DD}	t_{KCY1}/2-12			ns
	t_{KL1}	V_{DD}<4.0 V	t_{KCY1}/2-18			ns
SI set up time	t_{SIK1}	4.0≤V_{DD}	44			ns
		V_{DD}<4.0 V	55			Ns
SI hold time	t_{KSI1}		19			ns
SO output delay time	t_{KSO1}	C = 30 pF			25	ns

Note When CSI transfer is operated by DMA, it is necessary to concider DMA response time to decide cycle time.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

<Slave mode>

T_A = -40 to +105 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions		Min.	Max.	Unit
SCK cycle time	t_{KCY2}	4.0≤EV_{DD}	20 MHz<f_{MCK}	8/f_{MCK}		ns
			f_{MCK}≤20 MHz	6/f_{MCK}		ns
		EV_{DD}<4.0 V	16 MHz<f_{MCK}	8/f_{MCK}		ns
			f_{MCK}≤16 MHz	6/f_{MCK}		ns
SCK high/low level width	t_{KH2}			t_{KCY2}/2		ns
	t_{KL2}					
SI set up time	t_{SIK2}	2.7≤EV_{DD}		1/f_{MCK}+40		ns
SI hold time	t_{KSI2}			1/f_{MCK}+62		ns
SO output delay time	t_{KSO2}	C = 30pF	4.0≤EV_{DD}		2/f_{MCK}+44	ns
			EV_{DD}<4.0 V		2/f_{MCK}+57	ns

Note When CSI transfer is operated by DMA, it is necessary to concider DMA response time to decide cycle time.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 4-6. CSI mode connection diagram

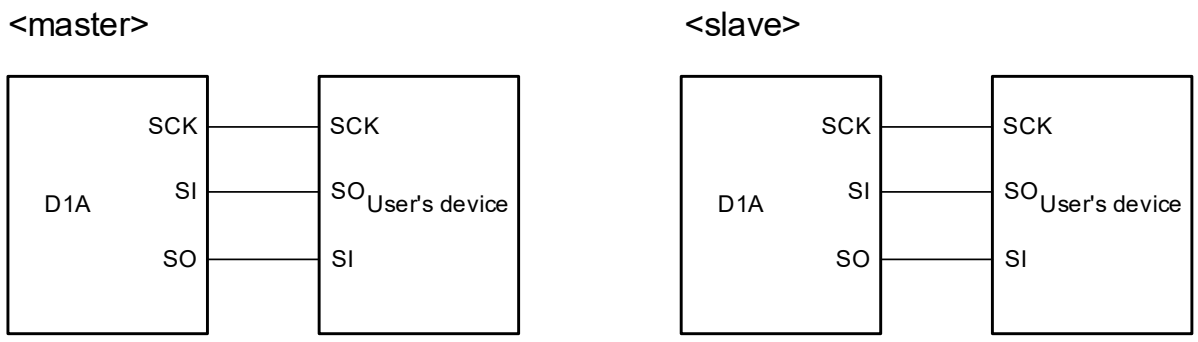


Figure 4-7. CSI mode serial transfer timing (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

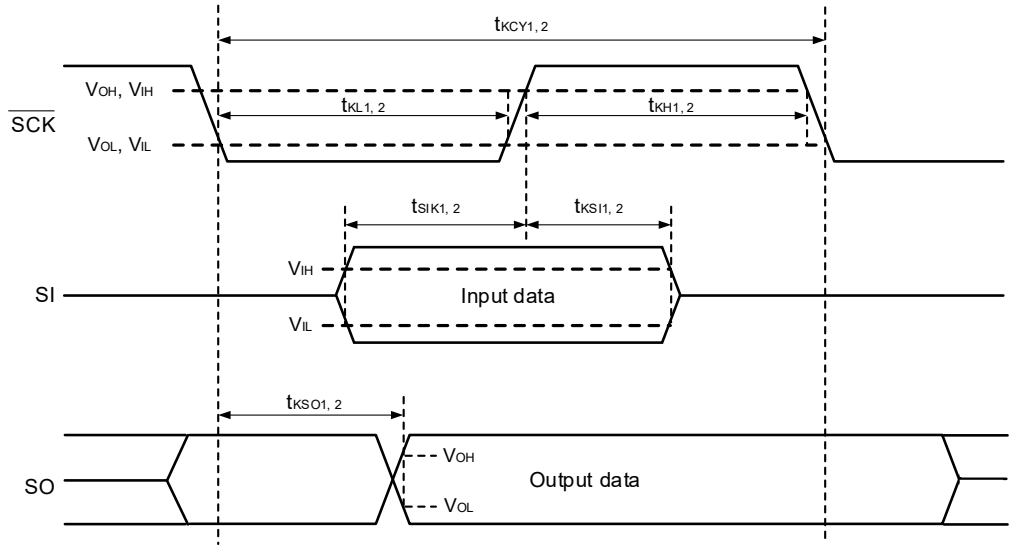
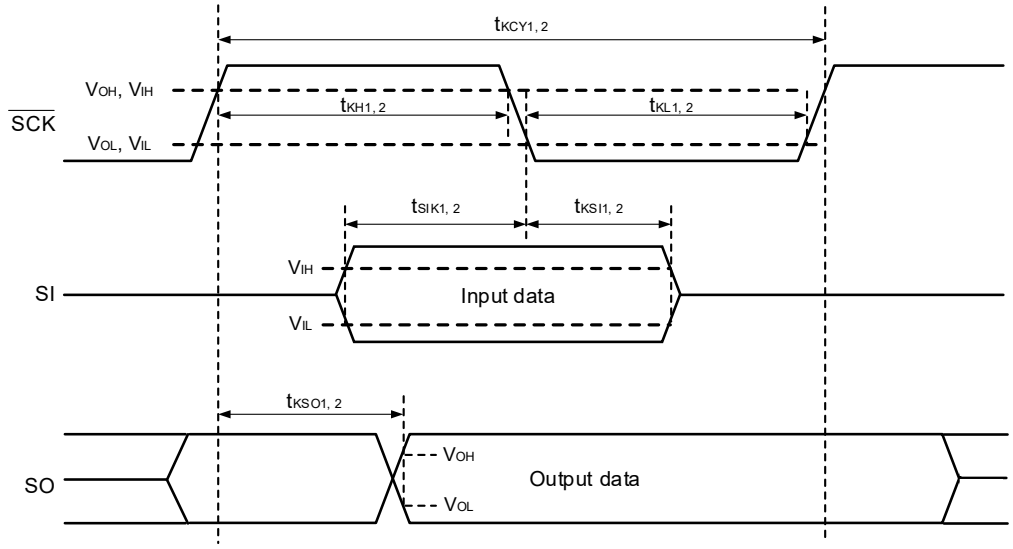


Figure 4-8. CSI mode serial transfer timing (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



4.5.5 Serial interface: UART operation (128-pin only)

T_A = -40 to +105 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} = ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Item	Symbol	Conditions	Min.	Max.	Unit
Transfer rate	T			f_{MCK}/12 Note	bps
		Theoretical value of the maximum transfer rate f_{CLK} = 24 MHz, f_{MCK} = f_{CLK}		2	Mbps

Note When CSI transfer is operated by DMA, it is necessary to concider DMA response time to decide cycle time.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 4-9 UART connection diagram

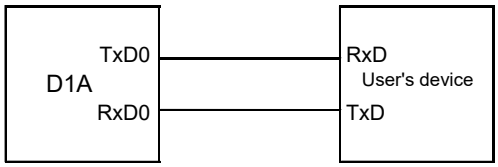
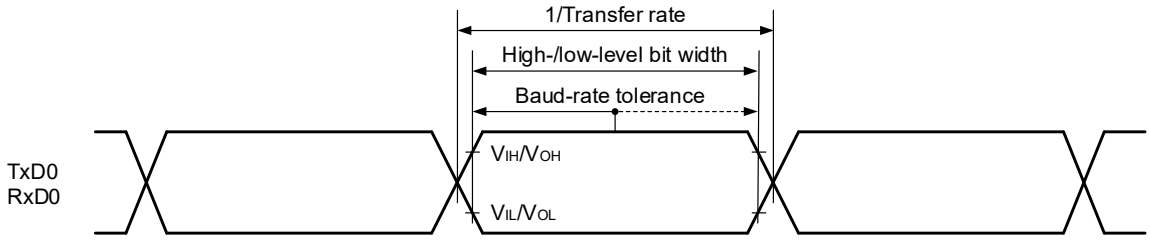


Figure 4-10. UART mode bit width (reference)



4.5.6 Serial interface: simplified I²C operation

T_A = -40 to +105 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} = ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	Rb = 3 kΩ, Cb = 100 pF		400	kHz
Hold time during SCL = ”L”	t_{LOW}	Rb = 3 kΩ, Cb = 100 pF	1150		ns
Hold time during SCL = ”H”	t_{HIGH}	Rb = 3kΩ, Cb = 100 pF	1150		ns
Data set up time (reception)	$t_{SU;DAT}$	Rb = 3 kΩ, Cb = 100 pF	1/f_{MCK}+270		ns
Data hold time (transmission)	$t_{HD;DAT}$	Rb = 3 kΩ, Cb = 100 pF	0	355	ns

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 4-11 simplified I I²C connection diagram

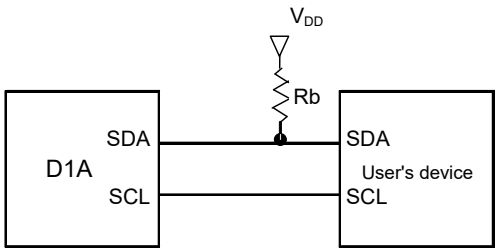
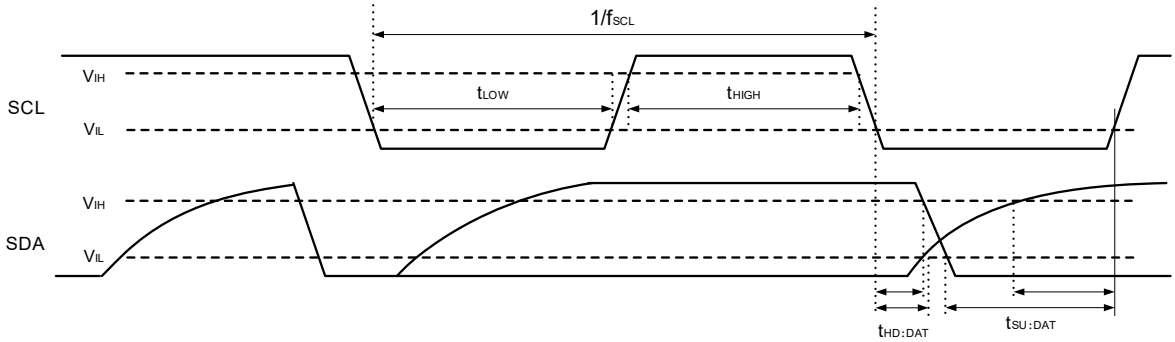


Figure 4-12. Simplified I²C mode serial transfer timing



4.5.7 Serial interface: LIN-UART(UARTF) operation

T_A = -40 to +105 °C

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.	Max.	Unit
Transfer rate	T			1.0	Mbps

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

4.5.8 Serial interface: CAN operation

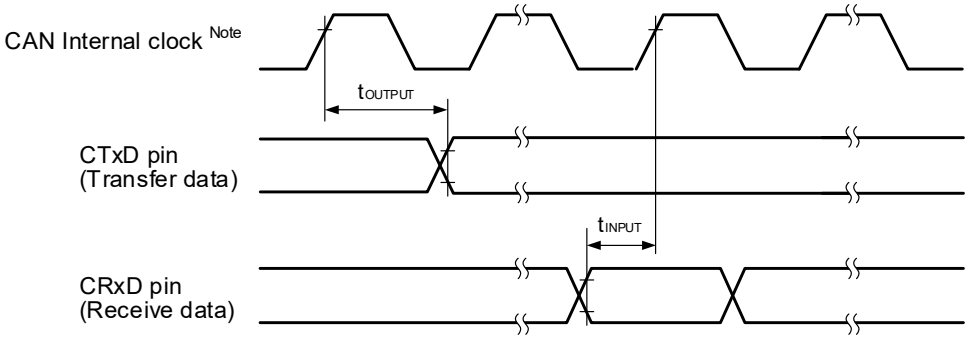
T_A = -40 to +105 °C,

2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	Min.	Max.	Unit
Transfer rate	T			1.0	Mbps
Internal delay time	t_{NODE}			100	ns
CRxD minimum pulse width for wake up	t_{CRXW}	Necessary width to detect wakeup signal	200		ns

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 4-13. Internal delay time of CAN



Internal delay time (t_{NODE}) = Internal Transfer Delay (t_{output}) + Internal Receive Delay (t_{Input})

Note CAN Internal clock (f_{CAN}): CAN baud rate clock

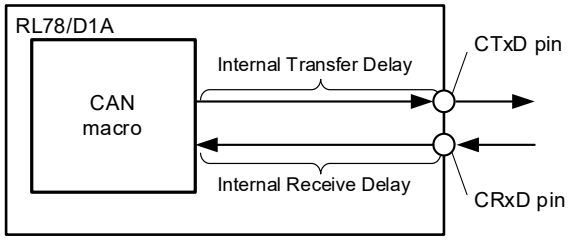


Image figure of Internal delay

4.6 LCD Bus Interface characteristics (128-pin products only)

T_A = -40 to +105 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} =EV_{SS1} =0 V

Items	Symbols	Conditions	MIN.	MAX.	Unit
Transfer frequency	F			8	MHz
CycleTime	t_{CYC}		LBCYC x T		ns
Control low pulse width	t_{CL}		(LBWST + 1)T - 1		ns
Enable active pulse width	t_{ELH}		(LBWST + 1)T - 5		ns
Control setup time	t_{RWS}		0.5T_S - 8		ns
Control hold time	t_{RWH}		0.5T - 3		ns
Data output setup time	t_{DOS}		0.5T_S - 6	0.5T_S + 17	ns
Data output hold time	t_{DOH}		{LBCYC - (LBWST + 1.5)} T - 27		ns
Data input setup time	t_{DIS}		50		ns
Data input hold time	t_{DIH}		0		ns
Output disable time	t_{OD}		0.5T - 14		ns

Remarks 1. T = (1/f_{CLK}) × n (n: LCD Bus Interface clock n divider setting)

2. T_S = (1/f_{CLK}) × N (N: LCD Bus Interface no clock divider N = 1, n divider N = n - 1)

3. F = 1/t_{CYC}

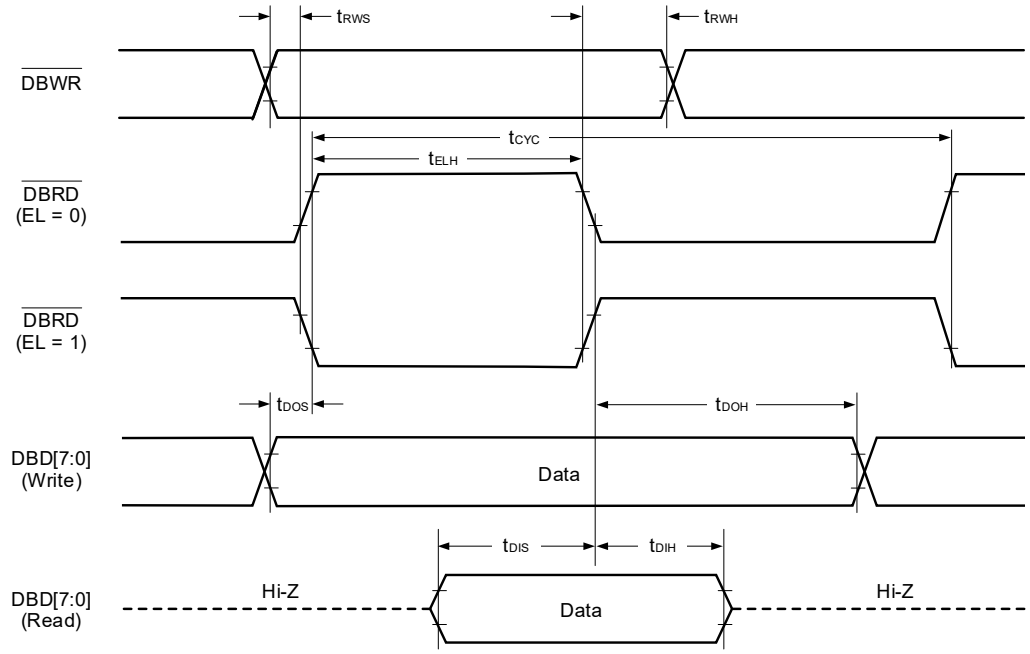
4. When EV_{DDx} = $SMV_{DD}x$ ≤ V_{DD}, LCD controller/driver related registers must be initial value (LCDON = 0, SCOC = 0, MDSET1 – 0 = 00, LCDPFx = 0).

5. The above table shows the timing of LCD bus interface with Schmitt1 input characteristic.

Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

Figure 4-14. LCD Bus Interface AC timing (1/2)

(a) LCDB mod68 mode timing



(b) mode68 turnaround timing

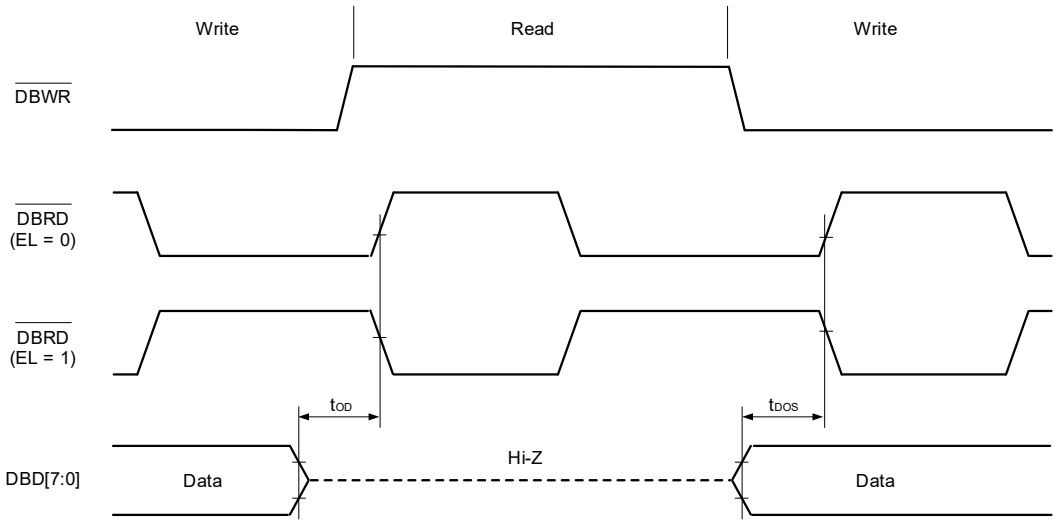
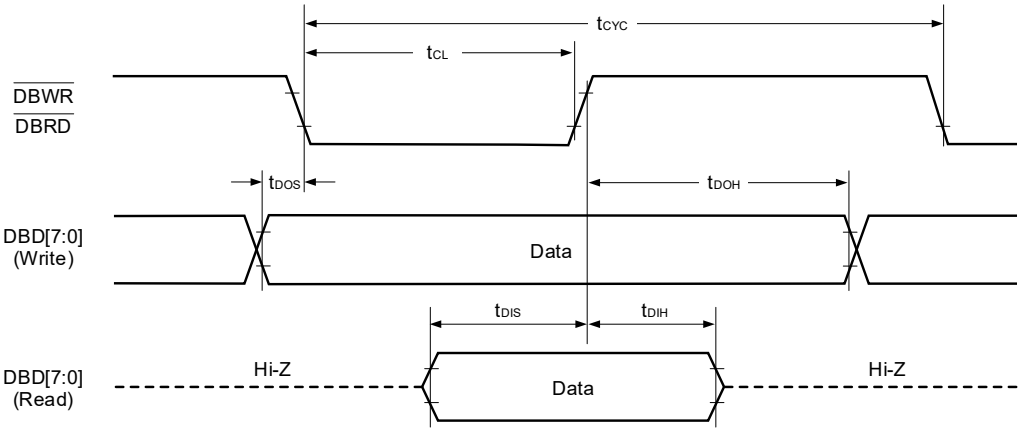
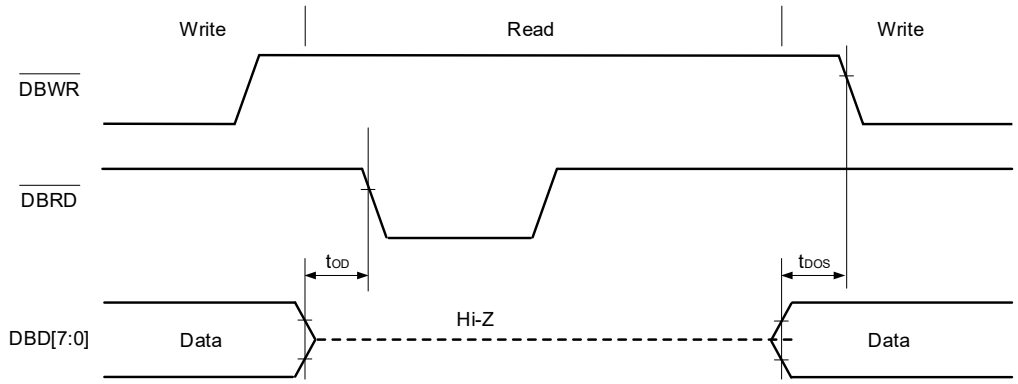


Figure 4-14. LCD Bus Interface AC timing (2/2)

(c) LCDB mod80 mode timing



(d) Mode80 turnaround timing



T_A = -40 to +105 °C, 3.2 V ≤ EV_{DD0} = EV_{DD1} = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
LCD division resistance Note 1	R_{LCD}				3	kΩ
LCD Segment output voltage (unloaded)	V_{ODS}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn} Note 2	V_{LCDn}+0.05	V
LCD Common output voltage (unloaded)	V_{ODC}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn}	V_{LCDn}+0.05	V
LCD Segment Output Voltage (loaded)	V_{ODSL0}	Io = ±10 μA, all segment pins at same time	V_{LCD0}-0.6	V_{LCD0}	V_{LCD0}+0.6	V
	V_{ODSL1}	Io = ±10 μA, all segment pins at same time	V_{LCD1}-0.6	V_{LCD1}	V_{LCD1}+0.6	V
	V_{ODSL2}	Io = ±10 μA, all segment pins at same time	V_{LCD2}-0.6	V_{LCD2}	V_{LCD2}+0.6	V
	V_{ODSL3}	Io = ±10 μA, all segment pins at same time	V_{LCD3}-0.6	V_{LCD3}	V_{LCD3}+0.6	V
LCD Common Output Voltage (loaded)	V_{ODCL0}	Io = ±40 μA, single pin	V_{LCD0}-0.2	V_{LCD0}	V_{LCD0}+0.2	V
	V_{ODCL1}	Io = ±40 μA, single pin	V_{LCD1}-0.2	V_{LCD1}	V_{LCD1}+0.2	V
	V_{ODCL2}	Io = ±40 μA, single pin	V_{LCD2}-0.2	V_{LCD2}	V_{LCD2}+0.2	V
	V_{ODCL3}	Io = ±40 μA, single pin	V_{LCD3}-0.2	V_{LCD3}	V_{LCD3}+0.2	V
LCD split voltage drive capability Note 1	V_{LC0}	Io = ±530 μA	V_{LCD0}-0.1	V_{LCD0}	V_{LCD0}+0.1	V
	V_{LC1}	Io = ±530 μA	V_{LCD1}-0.1	V_{LCD1}	V_{LCD1}+0.1	V
	V_{LC2}	Io = ±530 μA	V_{LCD2}-0.1	V_{LCD2}	V_{LCD2}+0.1	V
	V_{LC3}	Io = ±530 μA	V_{LCD3}-0.1	V_{LCD3}	V_{LCD3}+0.1	V
LCD output resistance (COM) Note 3	R_{ODC}				8	kΩ
LCD output resistance (SEG) Note 3	R_{ODS}				8	kΩ

Notes 1. Only internal connection. The vaule is design specification.

2. V_{LCDn} (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.

V_{LCDn}	no step-down transforming	step-down transforming
V_{LCD0}	V_{DD}	3/5 V_{DD}
V_{LCD1}	2/3 V_{DD}	2/5 V_{DD}
V_{LCD2}	1/3 V_{DD}	1/5 V_{DD}
V_{LCD3}	V_{SS}	V_{SS}

3. RODC is internal equivalent weight resistance from COM pin + COM IOBUF resistance.
RODS is internal equivalent weight resistance from SEG pin +SEG IOBUF resistance.

T_A = -40 to +105 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
LCD division resistance Note 1	R_{LCD}				3	kΩ
LCD Segment output voltage (unloaded)	V_{ODS}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn} Note 2	V_{LCDn}+0.05	V
LCD Common output voltage (unloaded)	V_{ODC}	Io = ±1 μA	V_{LCDn}-0.05	V_{LCDn}	V_{LCDn}+0.05	V
LCD Segment Output Voltage (loaded)	V_{ODSL0}	Io = ±5 μA, all segment pins at same time	V_{LCD0}-0.6	V_{LCD0}	V_{LCD0}+0.6	V
	V_{ODSL1}	Io = ±5 μA, all segment pins at same time	V_{LCD1}-0.6	V_{LCD1}	V_{LCD1}+0.6	V
	V_{ODSL2}	Io = ±5 μA, all segment pins at same time	V_{LCD2}-0.6	V_{LCD2}	V_{LCD2}+0.6	V
	V_{ODSL3}	Io = ±5 μA, all segment pins at same time	V_{LCD3}-0.6	V_{LCD3}	V_{LCD3}+0.6	V
LCD Common Output Voltage (loaded)	V_{ODCL0}	Io = ±25 μA, single pin	V_{LCD0}-0.2	V_{LCD0}	V_{LCD0}+0.2	V
	V_{ODCL1}	Io = ±25 μA, single pin	V_{LCD1}-0.2	V_{LCD1}	V_{LCD1}+0.2	V
	V_{ODCL2}	Io = ±25 μA, single pin	V_{LCD2}-0.2	V_{LCD2}	V_{LCD2}+0.2	V
	V_{ODCL3}	Io = ±25 μA, single pin	V_{LCD3}-0.2	V_{LCD3}	V_{LCD3}+0.2	V
LCD split voltage drive capability	V_{LC0}	Io = ±530 μA	V_{LCD0}-0.1	V_{LCD0}	V_{LCD0}+0.1	V
	V_{LC1}	Io = ±530 μA	V_{LCD1}-0.1	V_{LCD1}	V_{LCD1}+0.1	V
	V_{LC2}	Io = ±530 μA	V_{LCD2}-0.1	V_{LCD2}	V_{LCD2}+0.1	V
	V_{LC3}	Io = ±530 μA	V_{LCD3}-0.1	V_{LCD3}	V_{LCD3}+0.1	V
LCD output resistance (COM) Note 3	R_{ODC}				10	kΩ
LCD output resistance (SEG) Note 3	R_{ODS}				10	kΩ

Notes 1. V_{LCDn} (n= 0..3) represents one of the four possible voltage levels at the LCD pins. See table below for reference.

V_{LCDn}	no step-down transforming
V_{LCD0}	V_{DD}
V_{LCD1}	2/3 V_{DD}
V_{LCD2}	1/3 V_{DD}
V_{LCD3}	V_{SS}

2. Only internal connection. The vaule is design specification.

3. RODC is internal equivalent weight resistance from COM pin + COM IOBUF resistance.
RODS is internal equivalent weight resistance from SEG pin +SEG IOBUF resistance.

4.7 Analog characteristics

4.7.1 A/D converter characteristics

T_A = -40 to +105 °C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} =0 V
Reference voltage (+) = AV_{REFP}, Reference voltage(–) = AV_{REFM}

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	Bit
Overall error Note 1,2	AINL	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V			1.2	±3.5	LSB
Conversion time	Tconv	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V	3.6 V≤V_{DD}<5.5 V	2.125		39	μs
			2.7 V≤V_{DD}<5.5 V	3.1875		39	μs
Zero-scale error Note 1, 2	E_{ZS}	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				0.25	%FSR
Full-scale error Note 1, 2	E_{FS}	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				0.25	%FSR
Integral non-linearity error Note 1	ILE	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				±2.5	LSB
Differential non-linearityerror Note 1	DLE	10 bit Resolution AV_{REFP} = V_{DD} Note 3 AV_{REFM} = 0 V				±1.5	LSB
REF voltage(+)	AV_{REFP}			2.7		V_{DD}	V
REF voltage(-)	AV_{REFM}			V_{SS}			V
Analog input voltage	V_{AIN}			AV_{REFM}		AV_{REFP}	V
REF supply Current	I_{REF}	AV_{REFP} = 3 V			38	60	μA
		AV_{REFP} = 5 V			63	100	μA

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Minimum V_{DD}-0.5 V is allowed for AV_{REFP} to keep characteristic values

Remark When reference voltage(+) is not AV_{REFP} pin or reference voltage(-) is not AV_{REFM} pin, the accuracy will become worse.
Renesas recommends to use A/D converter with AV_{REFP} and AV_{REFM} though other reference can be functionally selected.

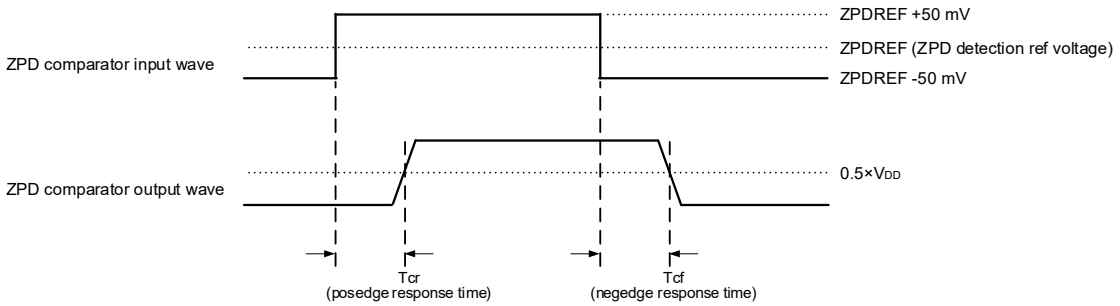
4.7.2 ZPD characteristics

T_A = -40 to +105 °C,

2.7 V ≤ EV_{DD0} = EV_{DD1} = SMV_{DD0} = SMV_{DD1} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = SMV_{SS0} = SMV_{SS1} = 0 V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
Threshhold voltage	V_{ZPD}	0 Point detection voltage set = 000		6/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 001		10/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 010		14/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 011		18/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 100		22/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 101		9/200*SMV_{DD}±40 mv			V
		0 Point detection voltage set = 110		11/200*SMV_{DD}±40 mv			V
Detection delay	T_{ZPDD}	100 mV Step, 50 mV Overdrive (refer to the below figure)	SMV_{DD} = 4.75 V to 5.25 V			100	ns
			SMV_{DD} = 2.7 V to 5.5 V			100	ns
Operation Stabilization wait time	T_{ZPDW}	Ref voltage Stabilization +ZPD comparator Stabilization				1+5 = 6	μs

Figure 4-15. ZPD timing



4.7.3 POR characteristics

T_A = -40 to +105 °C

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}		1.45	1.51	1.57	V
	V_{PDR}		1.44	1.5	1.56	V
Detection delay	T_{PD}				300	μs
Minimum pulse width	T_{PW}	Necessary width of internal voltage drop down below V_{PDR}	300			μs

Caution LVD reset or external $\overline{\text{RESET}}$ must be used during power supply rising up to 2.7 V.

4.7.4 LVD characteristics

T_A = -40 to +105 °C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V

Items	Symbols	Conditions		MIN.	TYP.	MAX.	Unit
RESET and INTMODE	V_{LVI5}	VPOC0,1,2 = 0,1,1 Power down Reset Voltage: 2.7 V		2.70	2.75	2.81	V
	V_{LVI4}	LVIS0,1 = 1,0 (+0.1 V)	Power on Reset Release Voltage	2.86	2.92	2.97	V
			Power down Interrupt Voltage	2.80	2.86	2.91	V
	V_{LVI3}	LVIS0,1 = 0,1 (+0.2 V)	Power on Reset Release Voltage	2.96	3.02	3.08	V
			Power down Interrupt Voltage	2.90	2.96	3.02	V
	V_{LVI0}	LVIS0,1 = 0,0 (+1.2 V)	Power on Reset Release Voltage	3.98	4.06	4.14	V
			Power down Interrupt Voltage	3.90	3.98	4.06	V
Detection Delay time	T_{LD}					200	μs
Minimum pulse width	T_{LW}	Necessary width of V_{DD} drop down below selected V_{LVIx} (x = 0, 3 to 5)		300			μs

Caution LVD reset or external $\overline{\text{RESET}}$ must be used during power supply rising up to 2.7 V.

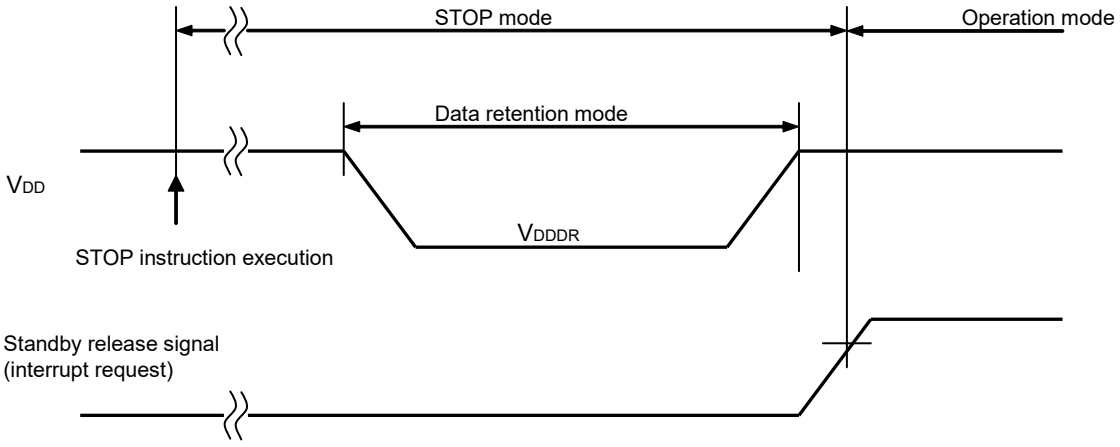
4.8 Data Retention Characteristics

T_A = -40 to +105 °C

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 Note1		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained until a POR reset is effected, but data is not retained when a POR reset is effected.

Figure 4-16. STOP Mode Data Retention timming



4.9 Capacitance Connected to REGC

T_A = -40 to +105 °C

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
Capacitance	C_{REG}		0.47		1.0	μF

4.10 Flash programming characteristics

T_A = -40 to +105 °C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Items	Symbols	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	Programming current			12.2	mA
System Clcok frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	2		24	MHz
Number of Code Flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years, T_A = +85 °C Note 4	1000			Times
Number of Data Flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years, T_A = +85 °C Note 4	10000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The specified data retention time is given under the condition that the average temperature (T_A) is 85°C or below.

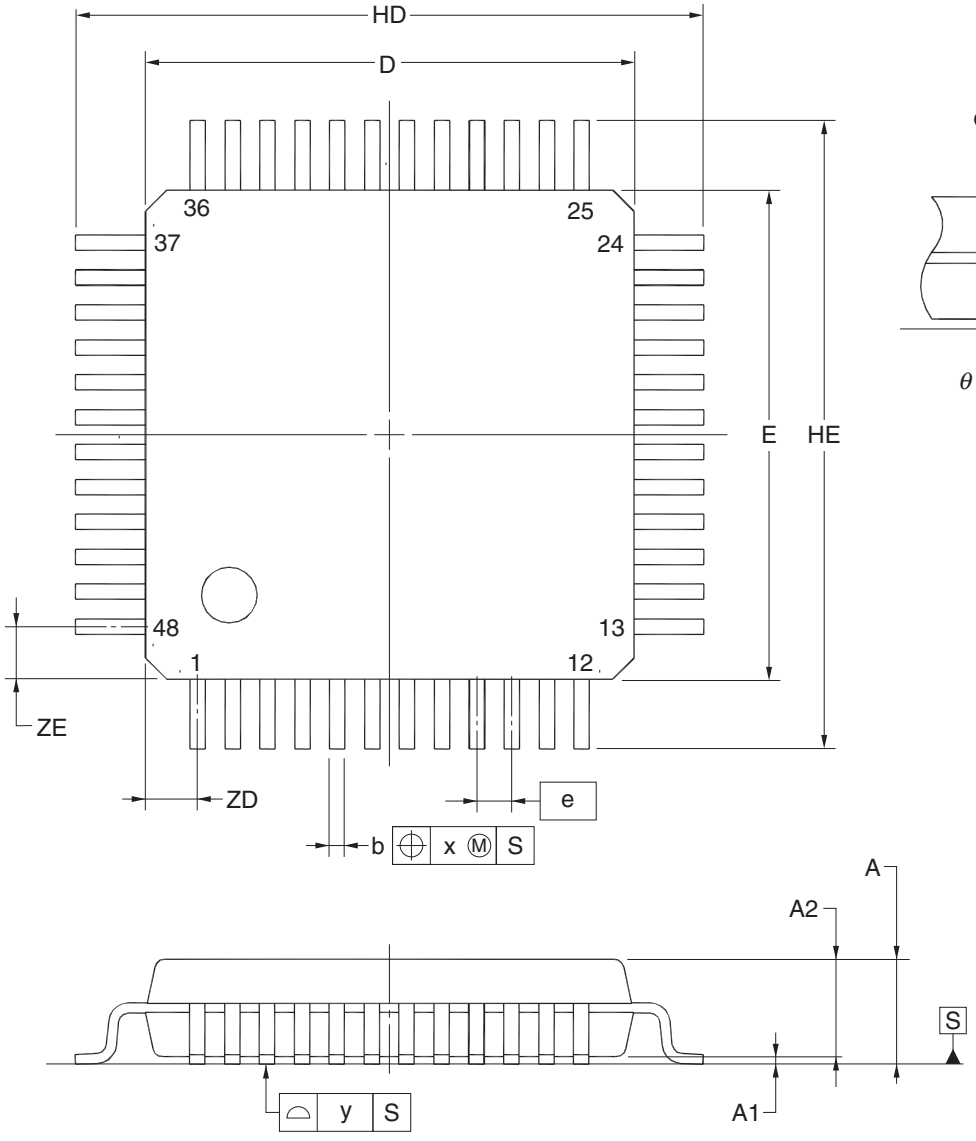
Caution Different voltage between EV_{DD} and V_{DD} is allowed only when LCDM register is initial value.

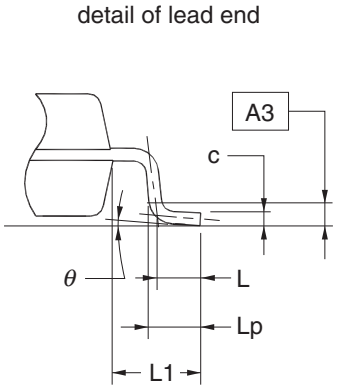
5. PACKAGE DRAWINGS

5.1 48-pin products

R5F10CGBxFB, R5F10CGCxFB, R5F10CGDxFB, R5F10DGCxFB, R5F10DGDxFB, R5F10DGExFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16





(UNIT:mm)

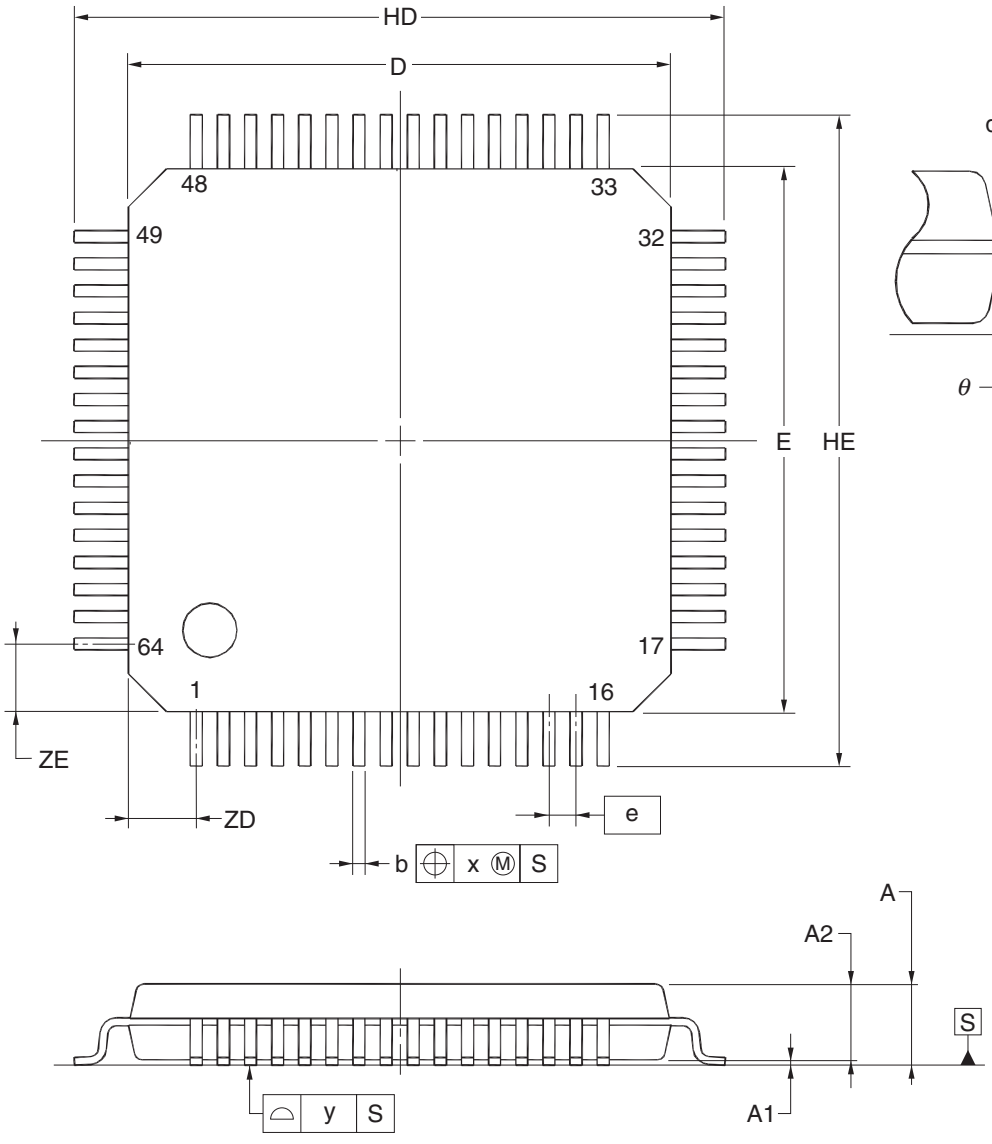
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

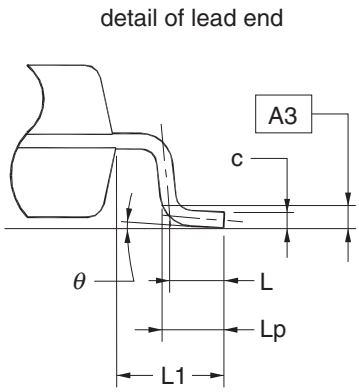
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

5.2 64-pin products

R5F10CLDxFB, R5F10DLDxFB, R5F10DLExFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35





(UNIT:mm)

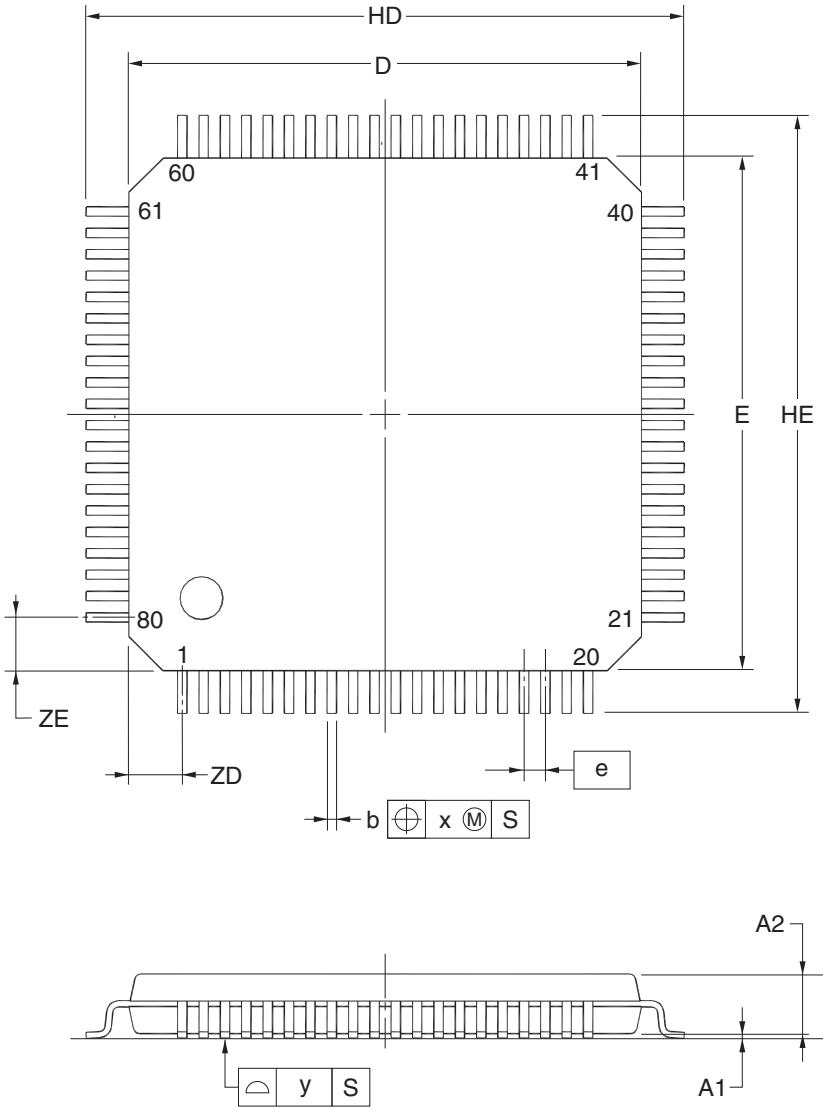
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

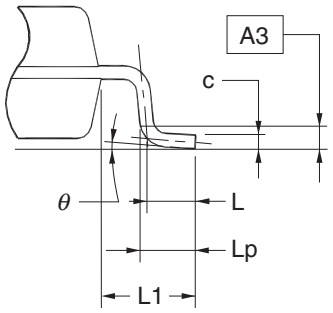
5.3 80-pin products

R5F10CMDxFB, R5F10CMExFB, R5F10DMDxFB, R5F10DMExFB, R5F10DMFxFB, R5F10DMGxFB, R5F10DMJxFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



detail of lead end



(UNIT:mm)

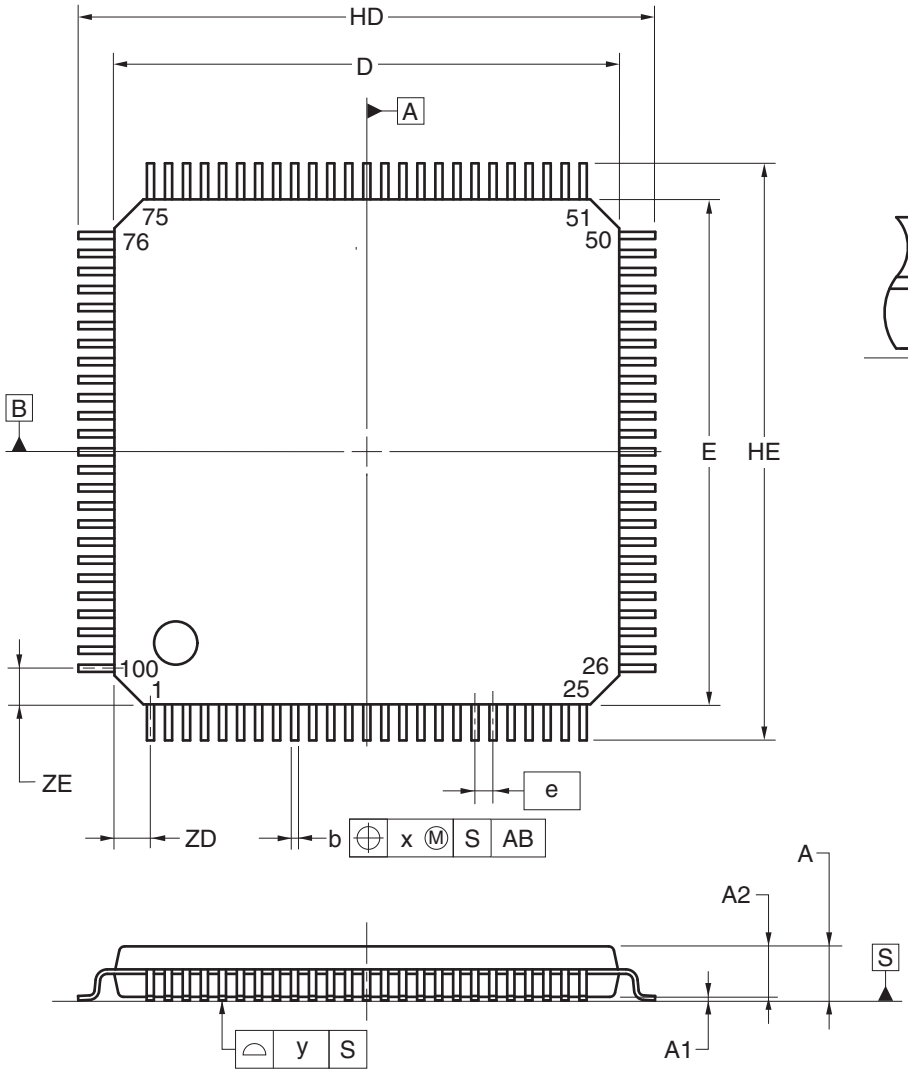
ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

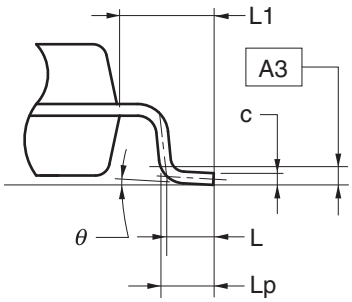
5.4 100-pin products

R5F10DPExFB, R5F10DPFxFB, R5F10DPGxFB, R5F10TPJxFB, R5F10DPJxFB, R5F10DPLxFB, R5F10DPKxFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



detail of lead end



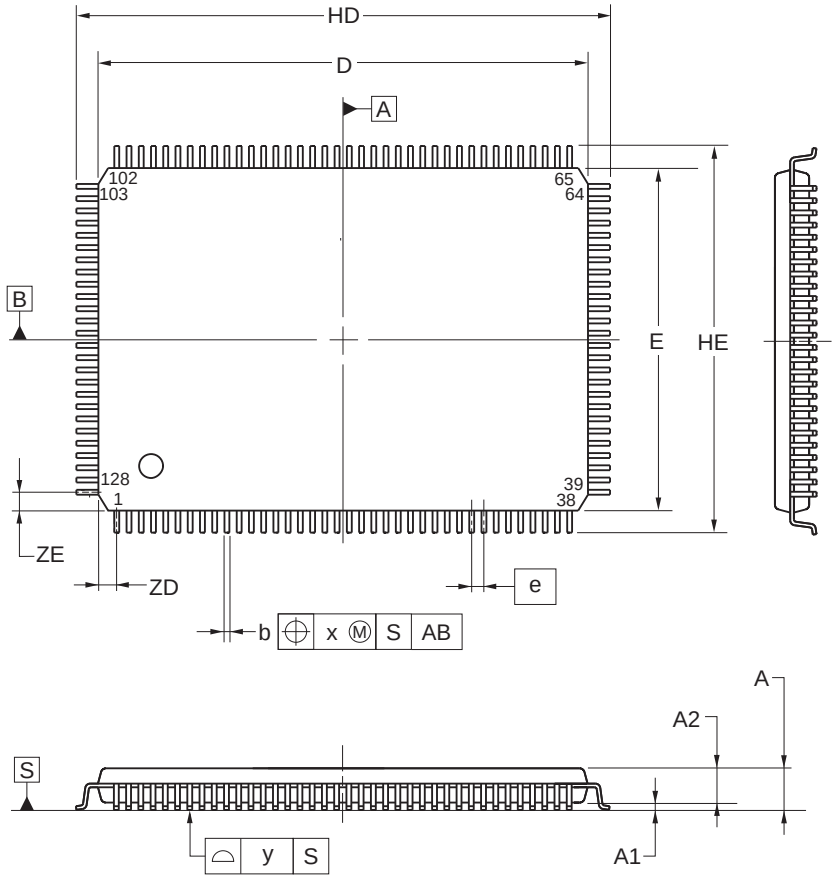
(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

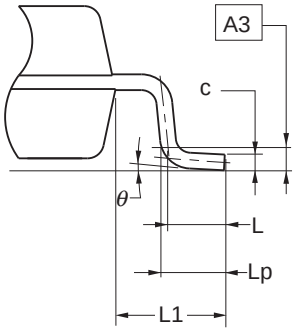
5.5 128-pin products

R5F10DSJxFB, R5F10DSKxFB, R5F10DSLxFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

REVISION HISTORY	RL78/D1A Datasheet

Rev	Date	Description	
		Page	Summary
1.10	Dec 27, 2024	–	First edition issued.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.