RL78/F22, F25

RENESAS MCU

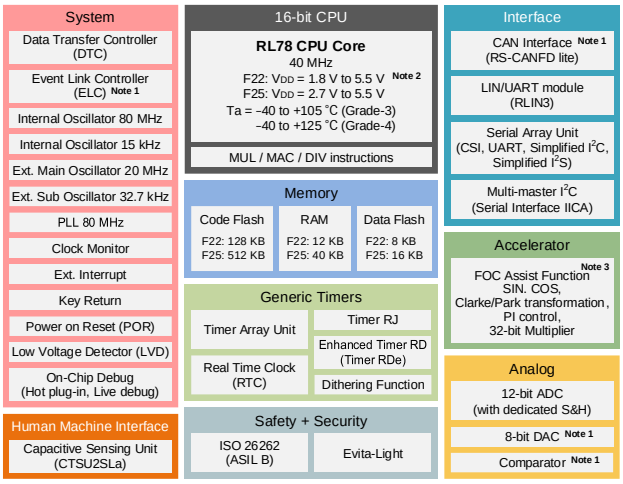
R01DS0490EJ0120
Rev.1.20
Jun 30, 2025

The RL78/F22, F25 microcontrollers are ideal for realizing future highly reliable smart actuators and sensors, as well as low-end body ECUs. RL78/F22, F25 products are designed according to ISO 26262 and support functional safety (FuSa) up to ASIL B. They support up to the EVITA-Light security standard or more. An AES crypto module can handle key lengths of up to 256 bits and supports secure boot and authentication. The RL78/F22, F25 products are also the first capacitive touch sensing unit (CTSU) in the RL78 automotive product. To respond to the E/E automotive architecture trend, the RL78/F25 is equipped with a CAN-FD interface (2 channels). RL78/F2x MCUs are fully hardware and software compatible with RL78/F1x, enabling software reuse. Please refer to the User's Manual: Hardware (R01UH1061EJ) for product details.

1. OVERVIEW

1.1 Features

- Minimum instruction execution time can be changed from high speed (0.025 µs: @40 MHz operation with high-speed on-chip oscillator clock or PLL clock) to ultra low-speed (66.6 µs: @15 kHz operation with low-speed on-chip oscillator clock)
- General-purpose register: 8 bits × 32 registers (8 bits × 8 registers × 4 banks)
- ROM: 128 KB/512 KB
- RAM: 12 KB/40 KB
- Data flash memory: 8 KB/16 KB
- High-speed on-chip oscillator clock:
  - Selectable from 40 MHz (Typ.), 32 MHz (Typ.), 20 MHz (Typ.), 16 MHz (Typ.), 8 MHz (Typ.), 4 MHz (Typ.), and 2 MHz (Typ.) (Selectable from 80 MHz (Typ.) and 64 MHz (Typ.) when using Timer RDe and RS-CANFD lite)
- Low-speed on-chip oscillator clock: 15 kHz × 2 channels (one for WWDT and one for CPU and peripherals other than WWDT)
- On-chip PLL
- On-chip single-power-supply flash memory (with prohibition of block erase/writing function)
- Self-programming (with boot swap function/flash shield window function)
- On-chip debug function
- On-chip power-on-reset (POR) circuit and voltage detector (LVD)
- On-chip watchdog timer (operable with the dedicated low-speed on-chip oscillator clock)
- Multiply/divide/multiply & accumulate instructions are supported
  - 16 bits × 16 bits = 32 bits (Unsigned or signed)
  - 32 bits ÷ 32 bits = 32 bits (Unsigned)
  - 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)
- On-chip key interrupt function
- On-chip clock output/buzzer output controller
- On-chip BCD adjustment
- I/O ports: 18 to 90 (including one input-only pin)
- Timer
  - 16-bit timer array unit: 12 channels/16 channels
  - 16-bit timer RDe: 2 channels (with PWMOPA and Dithering / Gate function)
  - 16-bit timer RJ: 1 channel
  - Watchdog timer: 1 channel
  - Real-time clock: 1 channel
- Application accelerator unit
- Serial interface
  - CSI
  - UART/UART (LIN-bus supported)
  - LIN module (master/slave supported)
  - I^2C/simplified I^2C
  - Simplified I^2S
  - CAN interface (RS-CANFD lite) **Note 1**
- 12-bit resolution A/D converter: 4 to 29 channels
- DTC (Max. 49 sources)
- ELC (Max. 26 channels for event link source, Max. 10 channels for event link destination) **Note 1**
- Functional safety (CRC calculation, Clock monitor, A/D test, etc.)
- Security functions (Secure boot, Crypto engine (AES-128, 192, 256), Random Number Generator (TRNG))
- 8-bit D/A converter **Note 1**
- On-chip comparator: 1 unit (input pin: 4 channels) **Note 1**
- Capacitive sensing unit: 7 to 31 channels
- Power supply voltage:
  - RL78/F22: V_{DD} = 1.8 to 5.5 V
  - RL78/F25: V_{DD} = 2.7 to 5.5 V
- Operating ambient temperature:
  - T_A = −40°C to 105°C (grade-3)
  - T_A = −40°C to 125°C (grade-4)
- ASIL level: ASIL-B



RL78/F22, F25 Block Diagram

Notes 1. Only available in the RL78/F25 product.
2. Only Grade-3 product. For Grade-4 product, V_{DD} = 2.7 V to 5.5 V.
3. FOC: Field Oriented Control (BLDC motor vector control method).

Applications

General automotive electrical applications (motor control, door control, headlight control, etc.), motorcycle engine control.

1.2 Product Lineup

Table 1-1. RL78/F22, F25 Lineup (Grade-3)

Operating Temperature (T_A)	Package	Pin	RL78/F22 Code Flash/Data Flash/RAM 128 KB/8 KB/12 KB	RL78/F25 Code Flash/Data Flash/RAM 512 KB/16 KB/40 KB
−40°C to 105°C	QFN	24	R7F122F7G3ANP-C	–
		32	R7F122FBG3ANP-C	–
	QFP	48	R7F122FGG3AFB-C	R7F125FGL3AFB-C
		64	–	R7F125FLL3AFB-C
		80	–	R7F125FML3AFB-C
		100	–	R7F125FPL3AFB-C

Table 1-2. RL78/F22, F25 Lineup (Grade-4)

Operating Temperature (T_A)	Package	Pin	RL78/F22 Code Flash/Data Flash/RAM 128 KB/8 KB/12 KB	RL78/F25 Code Flash/Data Flash/RAM 512 KB/16 KB/40 KB
−40°C to 125°C	QFN	24	R7F122F7G4ANP-C	–
		32	R7F122FBG4ANP-C	–
	QFP	48	R7F122FGG4AFB-C	R7F125FGL4AFB-C
		64	–	R7F125FLL4AFB-C
		80	–	R7F125FML4AFB-C
		100	–	R7F125FPL4AFB-C

1.3 Function Overview

1.3.1 RL78/F25 Functions List

Table 1-3. RL78/F25 Functions List (1/2)

Function Items			Series Name	R7F125FPL	R7F125FML	R7F125FLL	R7F125FGL
			Pin Count	100 pins	80 pins	64 pins	48 pins
Code flash				512 KB			
Data flash				16 KB			
RAM				40 KB			
Supply voltage range				2.7 V to 5.5 V			
Maximum operation frequency				40 MHz			
System clock	Main system clock oscillator	Crystal / ceramic / square wave		2 to 20 MHz (operating at 2.7 V to 5.5 V)			
	High-speed on-chip oscillator	Normal high accuracy		40 MHz (Typ.)			
	Low-speed on-chip oscillator	For low-speed operation		15 kHz (Typ.)			
	Subsystem clock oscillator			32.768 kHz			
	PLL			Yes			
Clock for peripherals	Low-speed on-chip oscillator	For peripherals other than WDT		15 kHz (Typ.)			
		For WDT		15 kHz (Typ.)			
POR				1.50 V (Typ.)			
LVD	V_{DD} voltage detection	LVD0		When power supply is rising: 2.97 V and 3.96 V (2 steps) When power supply is falling: 2.91 V and 3.88 V (2 steps)			
		LVD1		When power supply is rising: 2.82 V to 4.16 V (8 steps) When power supply is falling: 2.76 V to 4.08 V (8 steps)			
Functional safety **Note 6**	WWDT (window watchdog timer)			Yes			
	Flash memory fast CRC operation function			Yes			
	General purpose CRC operation			Yes			
	Code flash memory 1-bit error correction function			Yes			
	Code flash memory 2-bit error detection function			Yes			
	RAM 1-bit error correction function			Yes			
	RAM 2-bit error detection function			Yes			
	RS-CANFD lite RAM 1-bit error correction function			Yes			
	RS-CANFD lite RAM 2-bit error detection function			Yes			
	Invalid memory access detection function			Yes			
	Frequency detection function			Yes			
	Clock monitor function			Yes			
	Stack pointer monitor function			Yes			
	A/D test function			Yes			
I/O ports	Input/Output	CMOS		84 ch	66 ch	50 ch	36 ch
	Output	CMOS		1 ch			
	Input	Shared with oscillator pins		4 ch			
		Input only		1ch			
Power supply pins	For internal circuits			V_{DD}, V_{SS}, REGC			
	For I/O ports			EV_{DD0}, EV_{SS0} EV_{DD1}, EV_{SS1}	EV_{DD0}, EV_{SS0}		None
	For analog circuits (A/D, D/A, COMP)			AV_{DD}, AV_{SS} (AV_{REFP}, AV_{REFM} for A/D)			
Multiply/divide and multiply-accumulate functions	Multiply			16 bits × 16 bits (signed)			
				16 bits × 16 bits (unsigned)			
	Divide			32 bits ÷ 32 bits (unsigned)			
	Multiply-accumulate			16 bits × 16 bits + 32 bits (signed)			
				16 bits × 16 bits + 32 bits (unsigned)			
	Arithmetic instructions (extended instruction set)			Yes			
Vectored interrupt sources	External			17 ch **Notes 3, 4**	17 ch **Notes 3, 4**	16 ch **Notes 2, 4**	15 ch **Note 1, 5**
	Internal			63 ch **Note 3**	63 ch **Note 3**	63 ch **Note 2**	63 ch **Note 1**
Key return detection				8 ch			
DTC				49 sources			
Timer	TAU			16 bits (8 ch × 2)			
	RTC			1 ch			
	Timer RJ			16 bits × 1			
	Timer RDe			16 bits × 2 (with PWMOPA and dithering / gate function)			

(**Notes** are listed on the next page.)

Table 1-3. RL78/F25 Functions List (2/2)

Function Items			Series Name	R7F125FPL	R7F125FML	R7F125FLL	R7F125FGL
			Pin Count	100 pins	80 pins	64 pins	48 pins
Serial I/F	CSI / simplified I^2C / UART			4 ch / 4 ch / 2 ch			
		SPI		Yes			
	Multimaster I^2C			1 ch			
	Simplified I^2S			1 ch			
	LIN/UART module (RLIN3)			3 ch			
	CAN interface (RS-CANFD lite)			2 ch			
A/D converter 12 bit	High speed			16 ch	16 ch	15 ch	11 ch
	Normal speed			13 ch	7 ch	7 ch	6 ch
	Internal			1 ch (Internal reference voltage)			
D/A converter	8-bit			1 ch			
Comparator				1 unit (input 4 ch)			
Capacitive sensing unit				31 ch	31 ch	23 ch	15 ch
ELC				Link source: 26 ch Link destination: 10 ch			
PCLBUZ				1 ch			
Application accelerator unit				Yes			
Self-programming				Yes			
On-chip debug	Trace			Yes			
	Hot plug-in			Yes			
Option byte				Yes			
Security functions	AESEA			ECB/CBC mode and CMAC (AES-128, 192, 256)			
	Random number generator (TRNG)			Yes			

Notes 1. The following pairs of internal and external sources are each counted as a single source in this number:
INTP4 / INTSPM, INTP5 / INTCMP0, INTP6 / INTTM11H, INTP7 / INTTM13H,
INTP8 / INTRTC, INTP9 / INTTM01H

2. The following pairs of internal and external sources are each counted as a single source in this number:
INTP4 / INTSPM, INTP5 / INTCMP0, INTP6 / INTTM11H, INTP7 / INTTM13H,
INTP8 / INTRTC, INTP9 / INTTM01H, INTP10 / INTTM03H

3. The following pairs of internal and external sources are each counted as a single source in this number:
INTP4 / INTSPM, INTP5 / INTCMP0, INTP6 / INTTM11H, INTP7 / INTTM13H,
INTP8 / INTRTC, INTP9 / INTTM01H, INTP10 / INTTM03H, INTP13 / INTCLM

4. Both sources in the following pairs are counted as a single external interrupt source in this number:
INTP11 / INTLIN0WUP, INTP12 / INTLIN1WUP, INTP6 / INTLIN2WUP

5. Both sources in the following pairs are counted as a single external interrupt source in this number:
INTP6 / INTLIN2WUP

6. These functions are provided but they are not Safety Mechanism.
- Illegal instruction execution detection function
- SFR/RAM guard function
- I/O port output signal level detection function

1.3.2 RL78/F22 Functions List

Table 1-4. RL78/F22 Functions List (1/2)

Function Items			Series Name	R7F122FGG	R7F122FBG	R7F122F7G
			Pin Count	48 pins	32 pins	24 pins
Code flash				128 KB		
Data flash				8 KB		
RAM				12 KB		
Supply voltage range				1.8 V to 5.5 V		
Maximum operation frequency				40 MHz		
System clock	Main system clock oscillator	Crystal / ceramic / square wave		2 to 20 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V operation), 2 to 16 MHz (1.8 V ≤ V_{DD} < 2.7 V operation) *Grade 3 products only		
	High-speed on-chip oscillator	Normal high accuracy		40 MHz (Typ.)		
	Low-speed on-chip oscillator	For low-speed operation		15 kHz (Typ.)		
	Subsystem clock oscillator			32.768 kHz	None	
	PLL			Yes		
Clock for peripherals	Low-speed on-chip oscillator	For peripherals other than WDT		15 kHz (Typ.)		
		For WDT		15 kHz (Typ.)		
POR				1.50 V (Typ.)		
LVD	V_{DD} voltage detection	LVD0		When power supply is rising: 1.90 V to 3.96 V (3 steps) When power supply is falling: 1.86 V to 3.88 V (3 steps)		
		LVD1		When power supply is rising: 1.88 V to 4.16 V (11 steps) When power supply is falling: 1.84 V to 4.08 V (11 steps)		
Functional safety **Note 3**	WWDT (window watchdog timer)			Yes		
	Flash memory fast CRC operation function			Yes		
	General purpose CRC operation			Yes		
	Code flash memory 1-bit error correction function			Yes		
	Code flash memory 2-bit error detection function			Yes		
	RAM 1-bit error correction function			Yes		
	RAM 2-bit error detection function			Yes		
	Invalid memory access detection function			Yes		
	Frequency detection function			Yes		
	Clock monitor function			Yes		
	Stack pointer monitor function			Yes		
	A/D test function			Yes		
I/O ports	Input/Output	CMOS		36 ch	23 ch	15 ch
	Output	CMOS		1 ch	None	
	Input	Shared with oscillator pins		4 ch	2 ch	
		Input only		1 ch		
Power supply pins	For internal circuits			V_{DD}, V_{SS}, REGC		
	For I/O ports			None		
	For analog circuits (A/D)			AV_{DD}, AV_{SS} (AV_{REFP}, AV_{REFM} for A/D)		
Multiply/divide and multiply-accumulate functions	Multiply			16 bits × 16 bits (signed)		
				16 bits × 16 bits (unsigned)		
	Divide			32 bits ÷ 32 bits (unsigned)		
	Multiply-accumulate			16 bits × 16 bits + 32 bits (signed)		
				16 bits × 16 bits + 32 bits (unsigned)		
	Arithmetic instructions (extended instruction set)			Yes		
Vectored interrupt sources	External			12 ch **Note 2**	8 ch **Note 1**	7 ch **Note 1**
	Internal			39 ch **Note 2**	39 ch **Note 1**	39 ch **Note 1**
Key return detection				8 ch	6 ch	3 ch
DTC				37 sources	36 sources	35 sources
Timer	TAU			16 bits (8 ch + 4 ch)		
	RTC			1 ch		
	Timer RJ			16 bits × 1		
	Timer RDe			16 bits × 2 (with PWMOPA and dithering / gate function)		

(**Notes** are listed on the next page.)

Table 1-4. RL78/F22 Functions List (2/2)

Function Items		Series Name	R7F122FGG	R7F122FBG	R7F122F7G
		Pin Count	48 pins	32 pins	24 pins
Serial I/F	CSI/simplified I^2C /UART		4 ch / 4 ch / 2 ch	3 ch / 3 ch / 2 ch	2 ch / 2 ch / 2 ch
		SPI	Yes		
	Multimaster I^2C		1 ch		
	Simplified I^2S		1 ch		
	LIN/UART module (RLIN3)		1 ch		
	CAN interface (RS-CANFD lite)		None		
A/D converter 12 bit	High Speed		11 ch	6 ch	3 ch
	Normal Speed		6 ch	2 ch	1 ch
	Internal		1 ch (Internal reference voltage)		
D/A converter	8-bit		None		
Comparator			None		
Capacitive sensing unit			12 ch	10 ch	7 ch
ELC			None		
PCLBUZ			1 ch	None	
Application accelerator unit			Yes		
Self-programming			Yes		
On-chip debug	Trace		Yes		
	Hot plug-in		Yes		
Option byte			Yes		
Security Functions	AESEA		ECB/CBC mode and CMAC (AES-128, 192, 256)		
	Random Number Generator (TRNG)		Yes		

Notes 1. The following pairs of internal and external sources are each counted as a single source in this number:
INTP4 / INTSPM

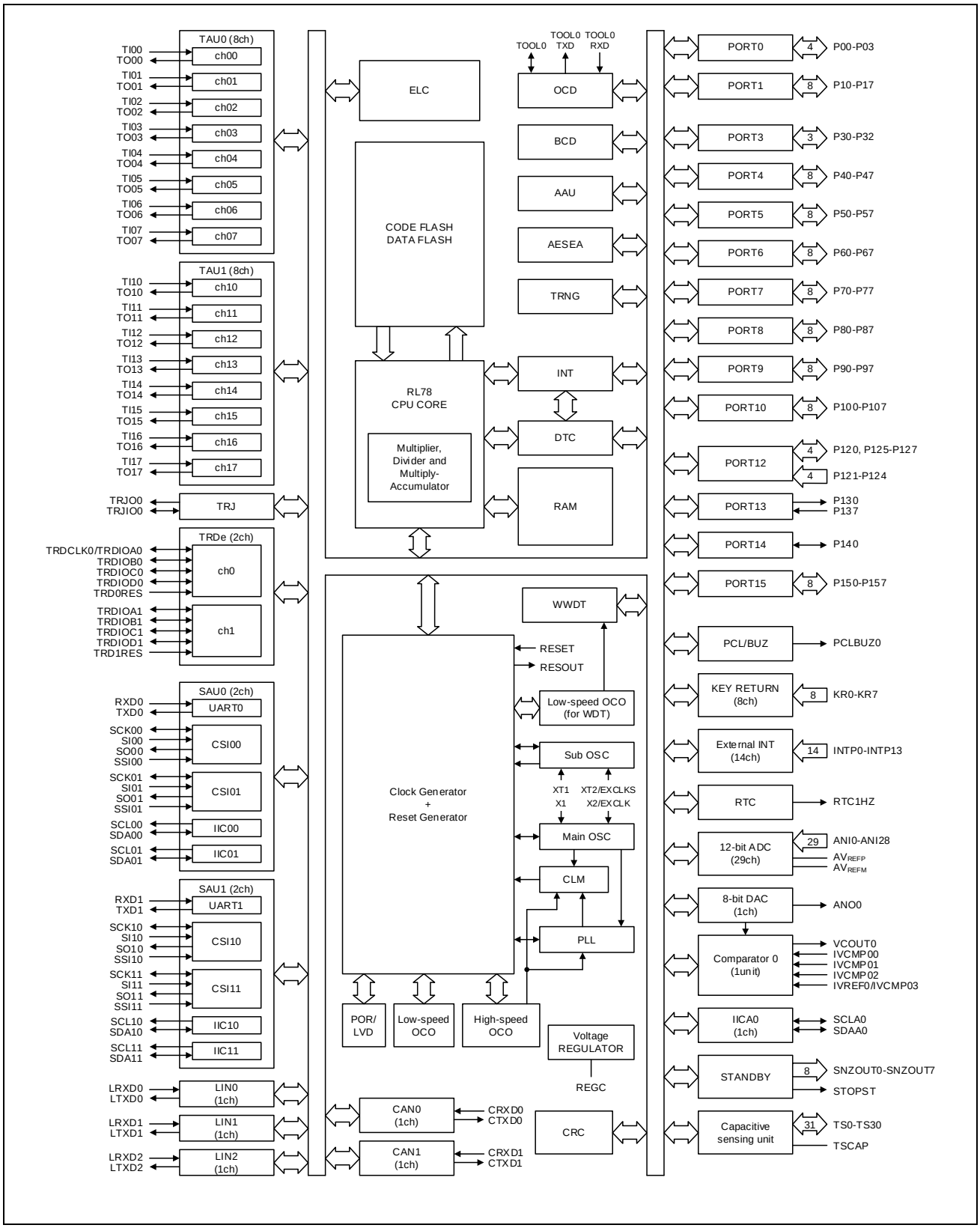
2. The following pairs of internal and external sources are each counted as a single source in this number:
INTP4 / INTSPM, INTP6 / INTTM11H, INTP7 / INTTM13H, INTP8 / INTRTC, INTP9 / INTTM01H

3. These functions are provided but they are not Safety Mechanism.
- Illegal instruction execution detection function
- SFR/RAM guard function
- I/O port output signal level detection function

1.4 Block Diagram

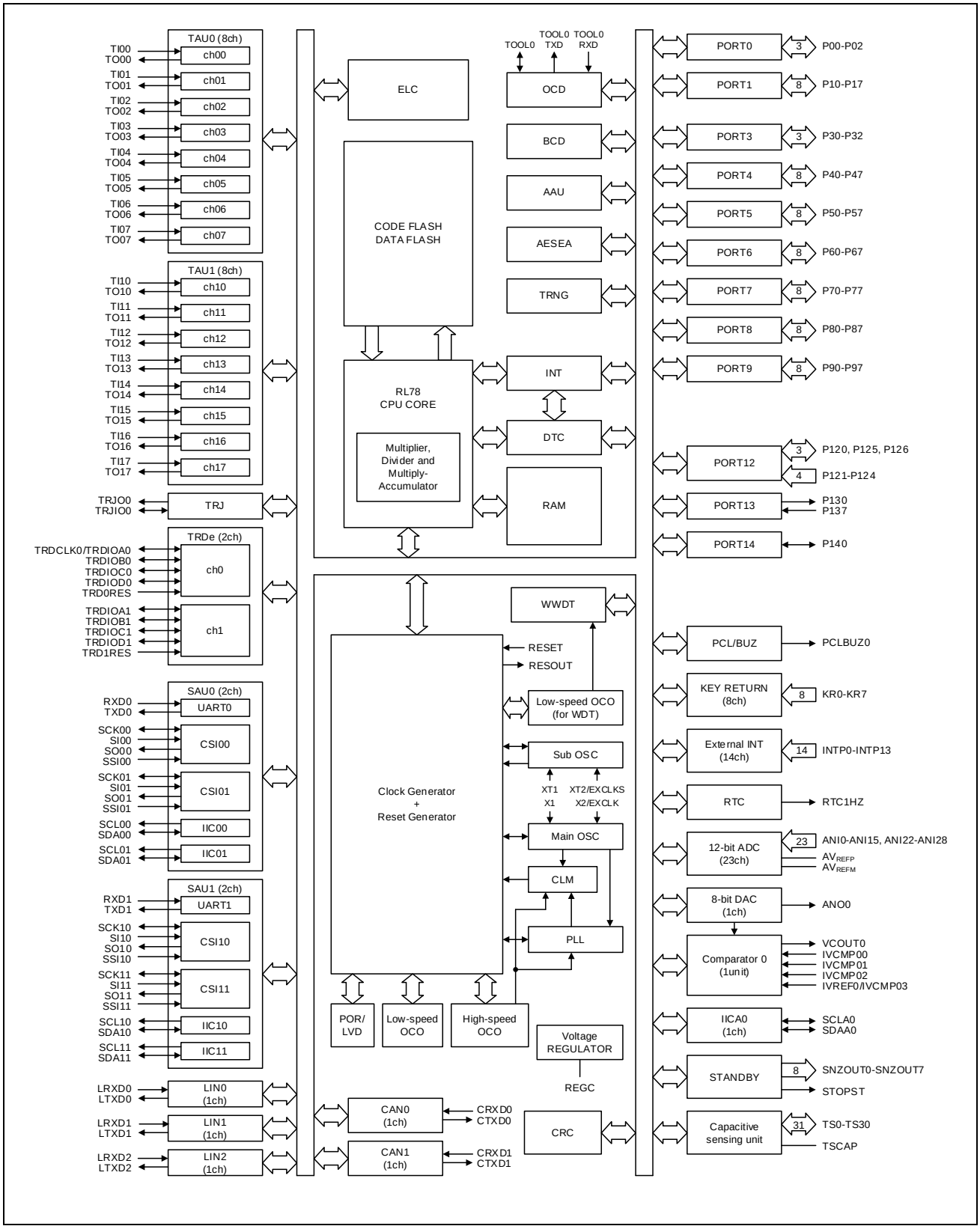
1.4.1 RL78/F25: Block Diagram of R7F125FPL 100-pin Products

Figure 1-1. Block Diagram



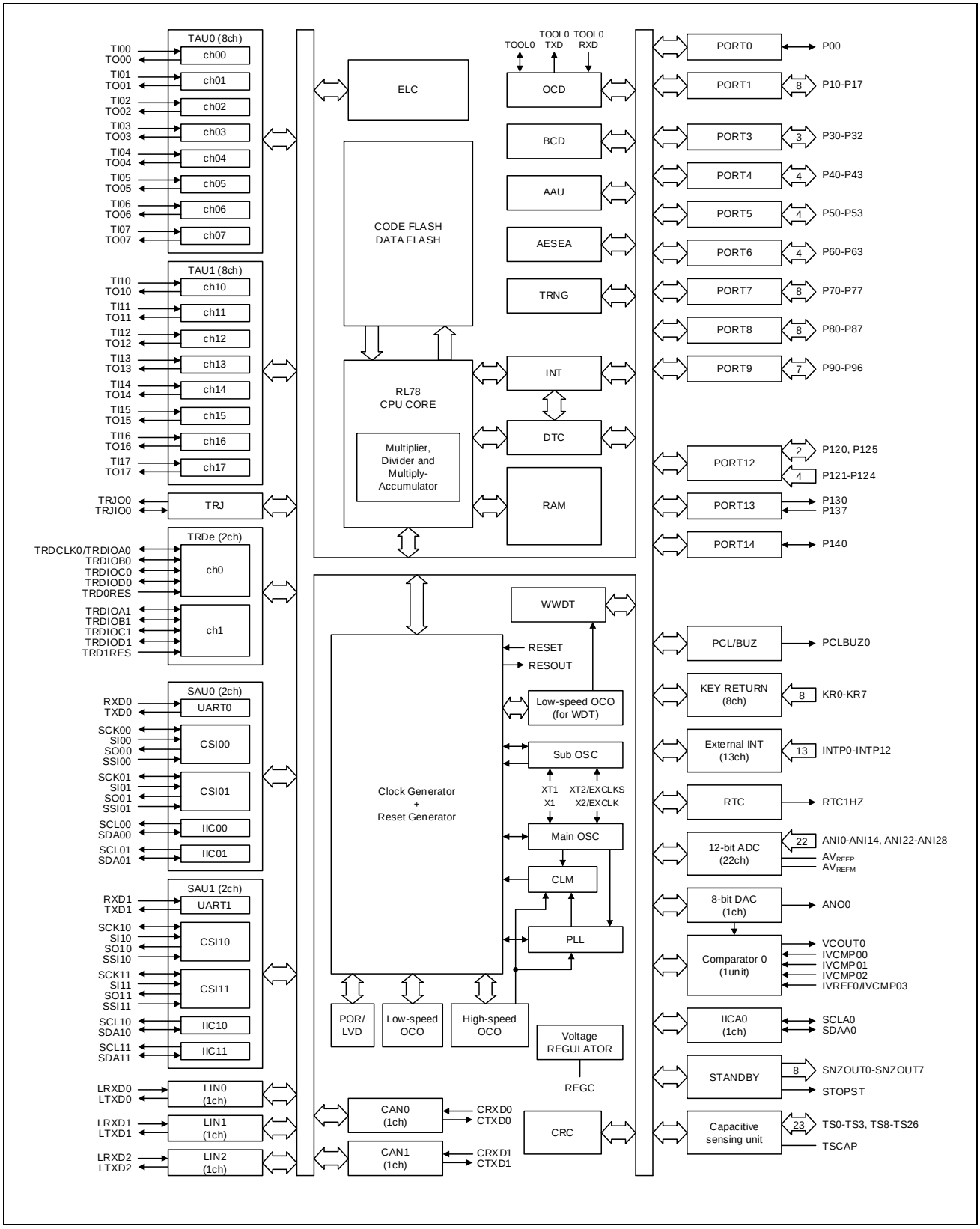
1.4.2 RL78/F25: Block Diagram of R7F125FML 80-pin Products

Figure 1-2. Block Diagram



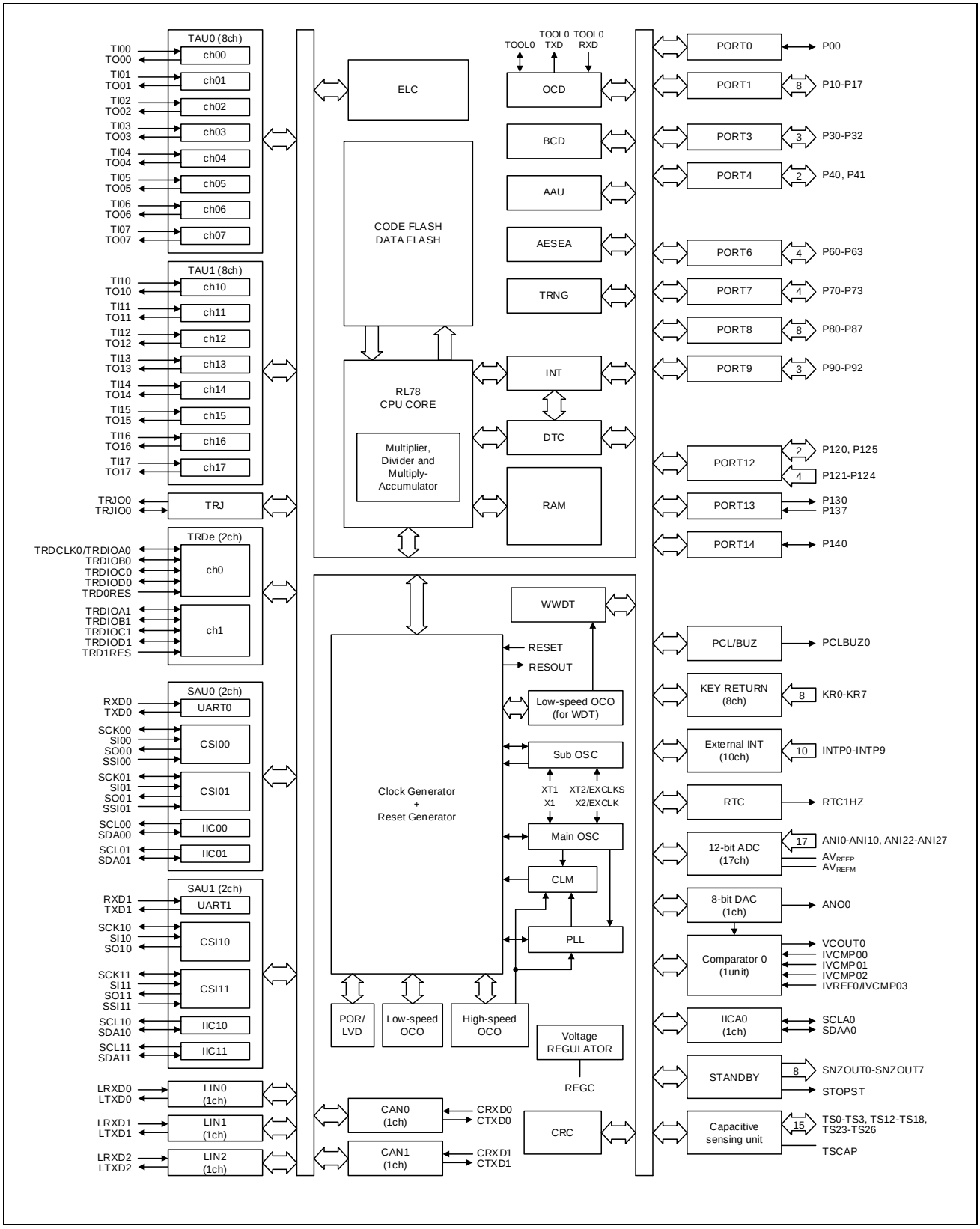
1.4.3 RL78/F25: Block Diagram of R7F125FLL 64-pin Products

Figure 1-3. Block Diagram



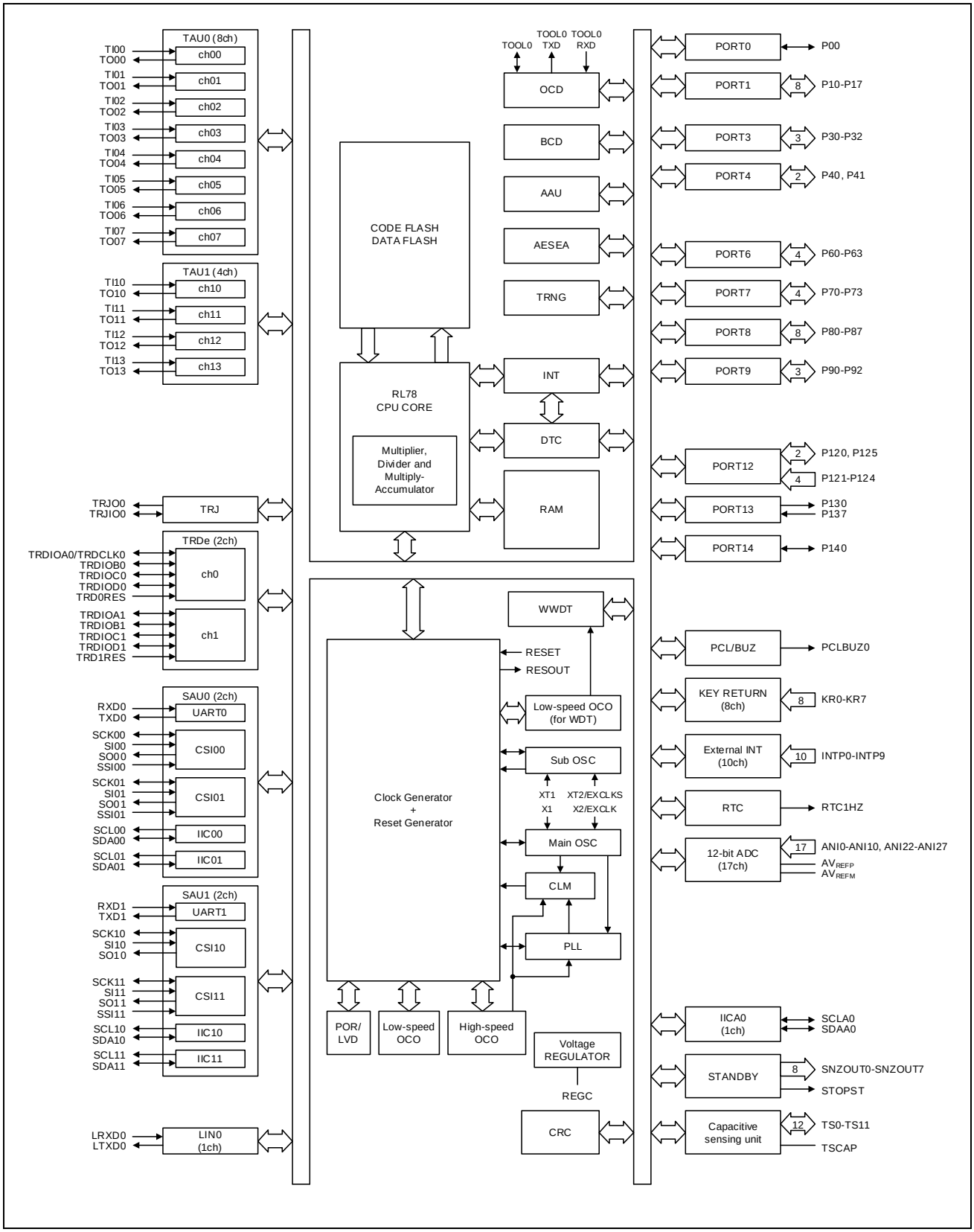
1.4.4 RL78/F25: Block Diagram of R7F125FGL 48-pin Products

Figure 1-4. Block Diagram



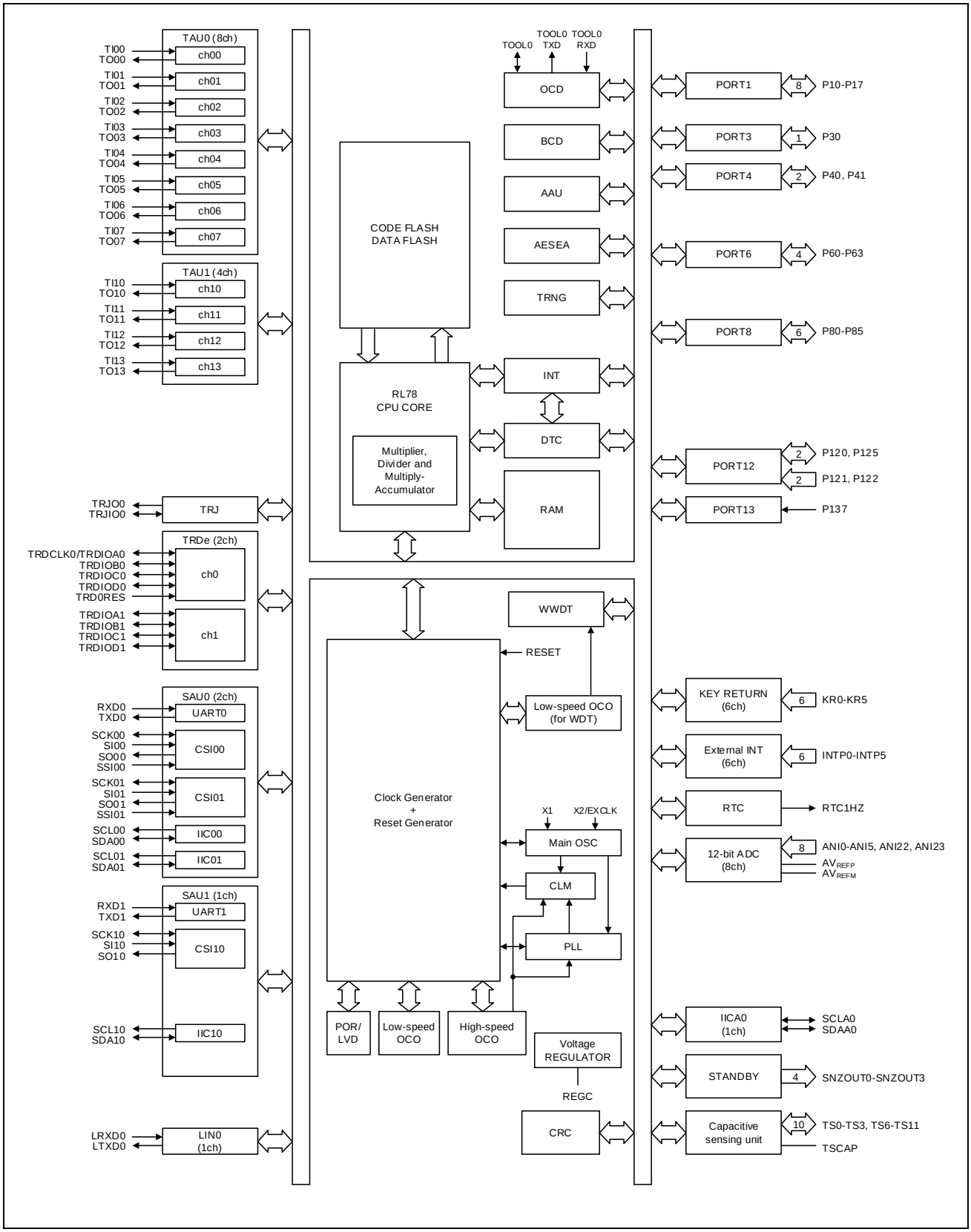
1.4.5 RL78/F22: Block Diagram of R7F122FGG 48-pin Products

Figure 1-5. Block Diagram



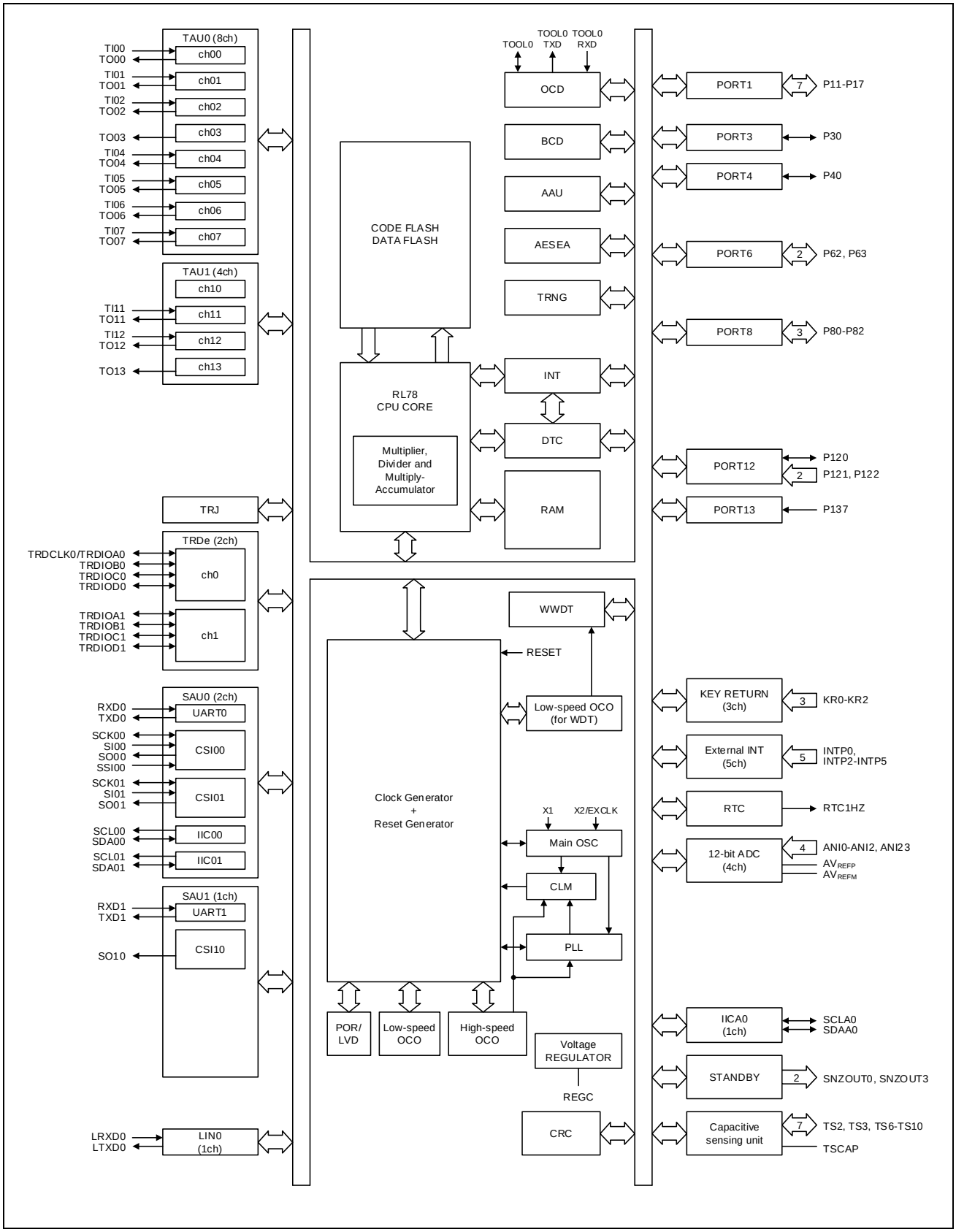
1.4.6 RL78/F22: Block Diagram of R7F122FBG 32-pin Products

Figure 1-6. Block Diagram



1.4.7 RL78/F22: Block Diagram of R7F122F7G 24-pin Products

Figure 1-7. Block Diagram

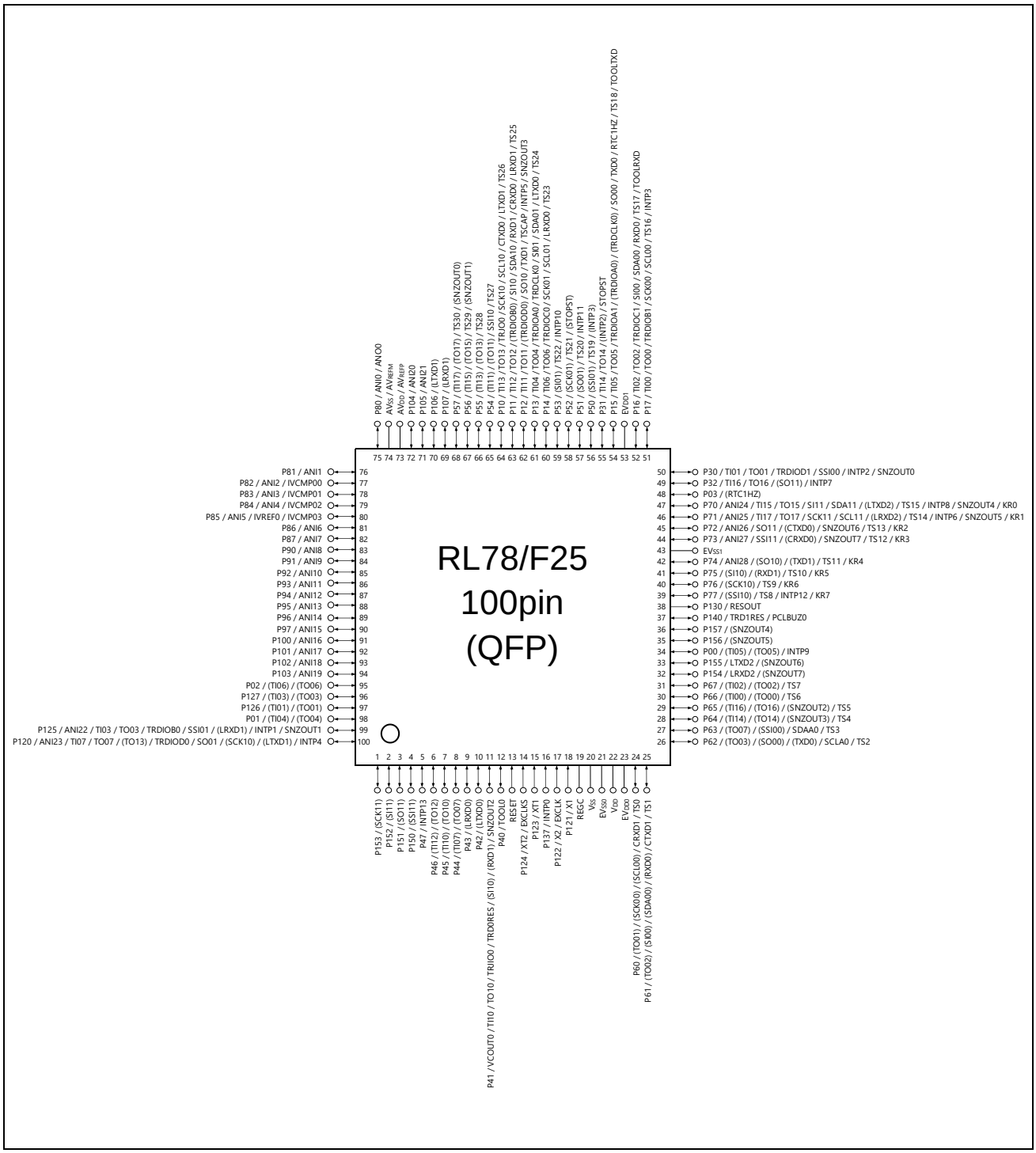


1.5 Pin Configurations

1.5.1 RL78/F25 Pin Configuration for 100-pin Products

- RL78/F25: 100-pin Plastic QFP (Fine Pitch) (14 × 14)

Figure 1-8. RL78/F25 Pin Configuration for 100-pin Products

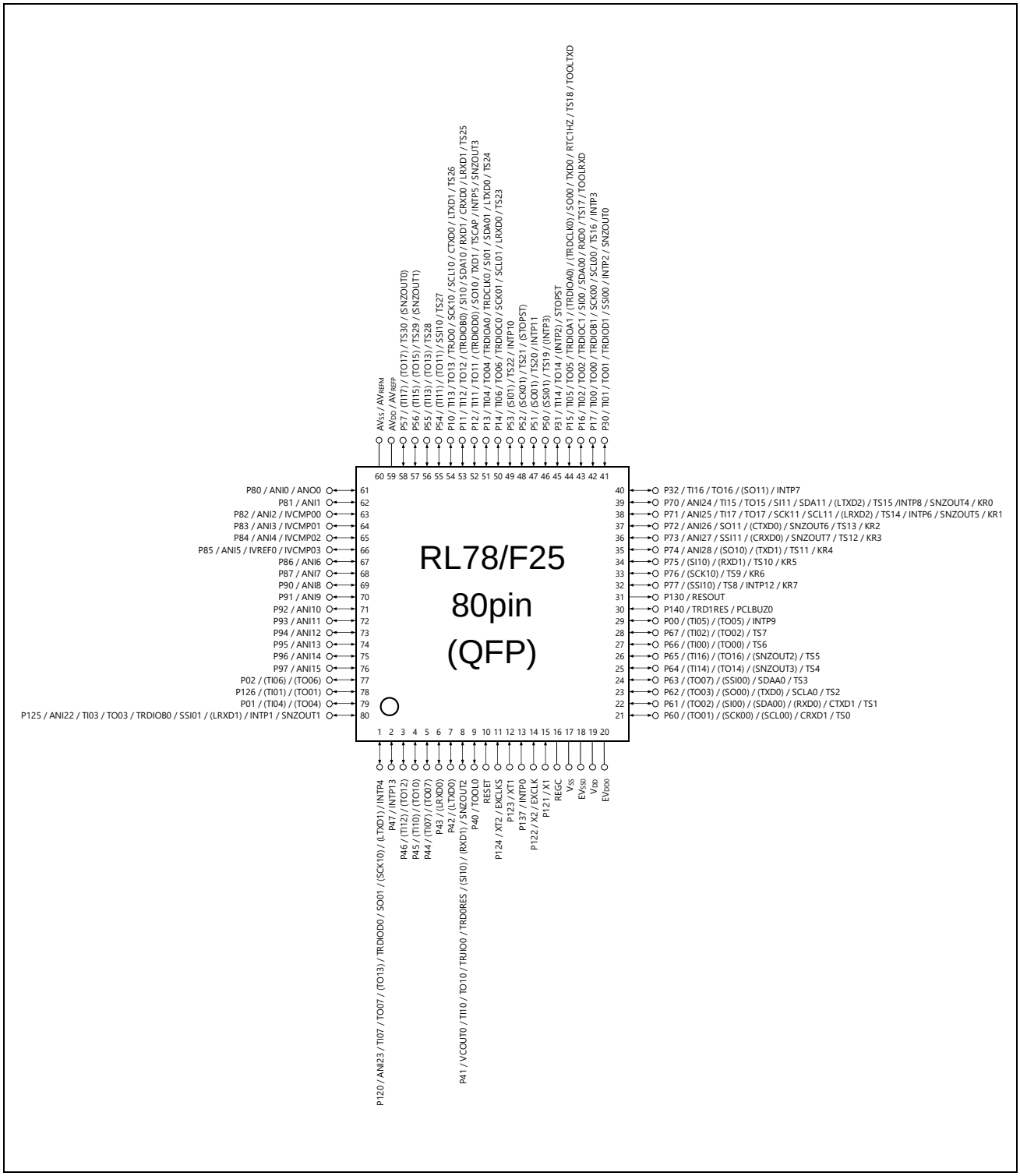


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

1.5.2 RL78/F25 Pin Configuration for 80-pin Products

- RL78/F25: 80-pin Plastic QFP (Fine Pitch) (12 × 12)

Figure 1-9. RL78/F25 Pin Configuration for 80-pin Products

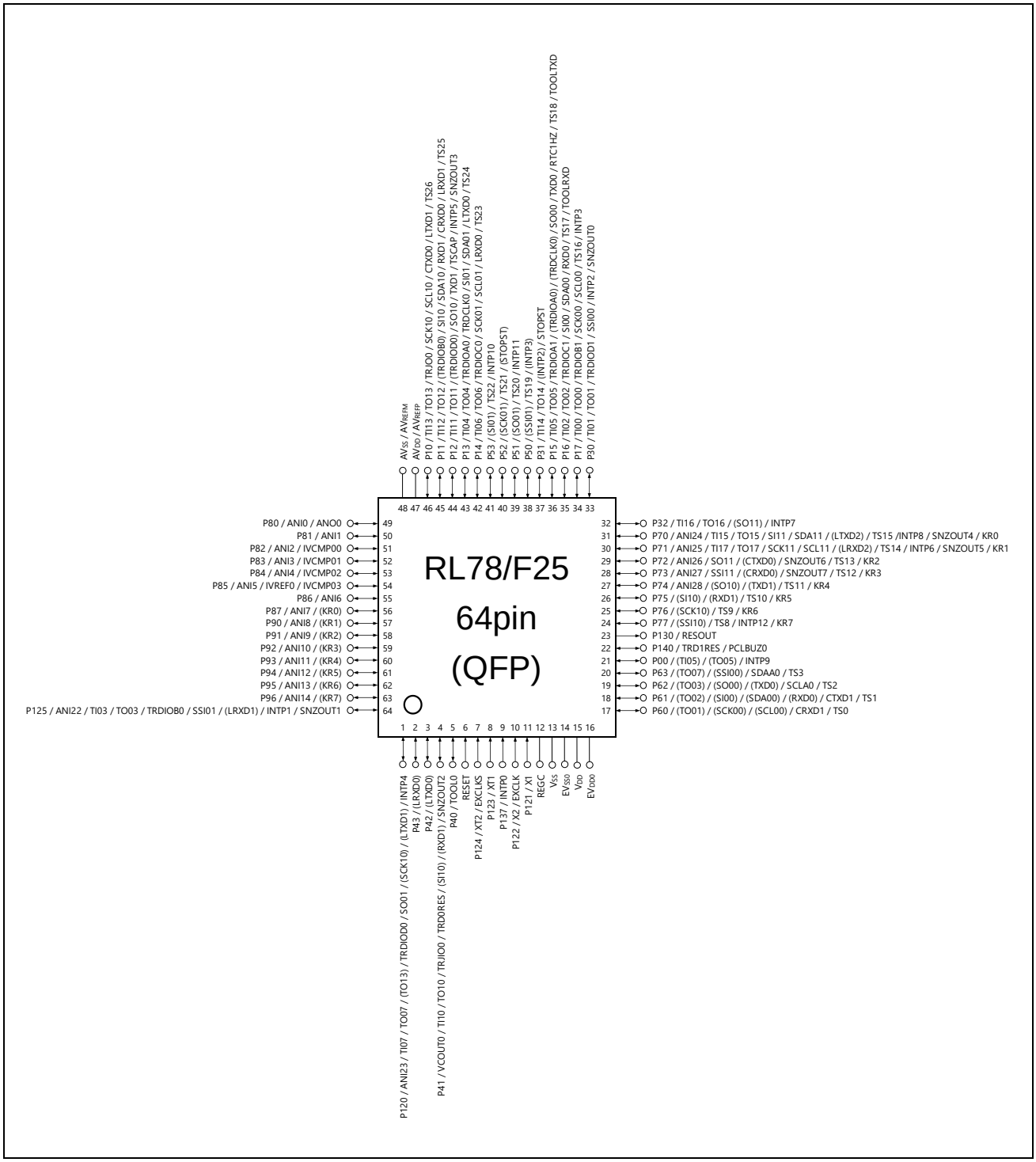


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

1.5.3 RL78/F25 Pin Configuration for 64-pin Products

- RL78/F25: 64-pin Plastic QFP (Fine Pitch) (10 × 10)

Figure 1-10. RL78/F25 Pin Configuration for 64-pin Products

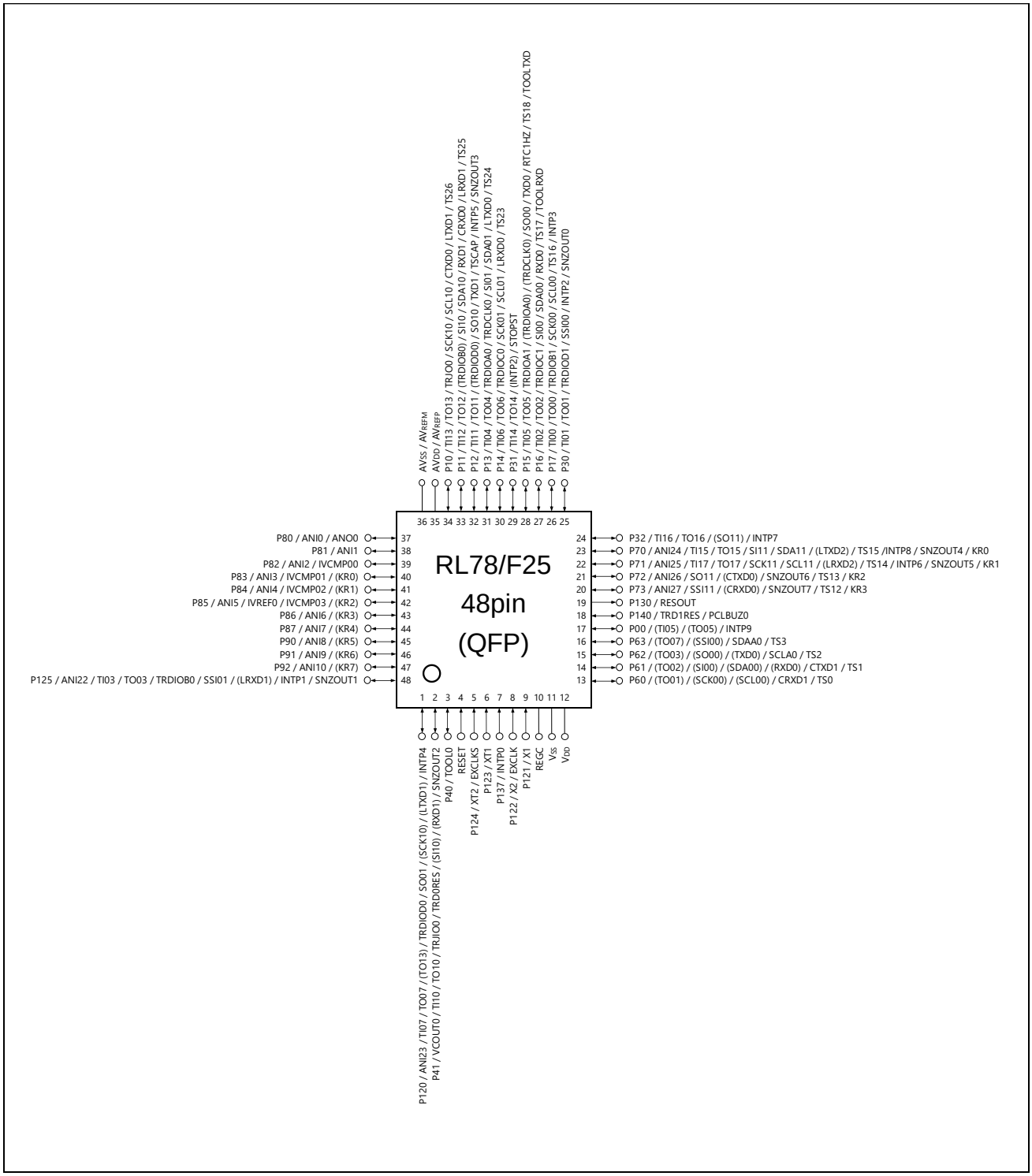


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

1.5.4 RL78/F25 Pin Configuration for 48-pin Products

- RL78/F25: 48-pin Plastic QFP

Figure 1-11. RL78/F25 Pin Configuration for 48-pin Products

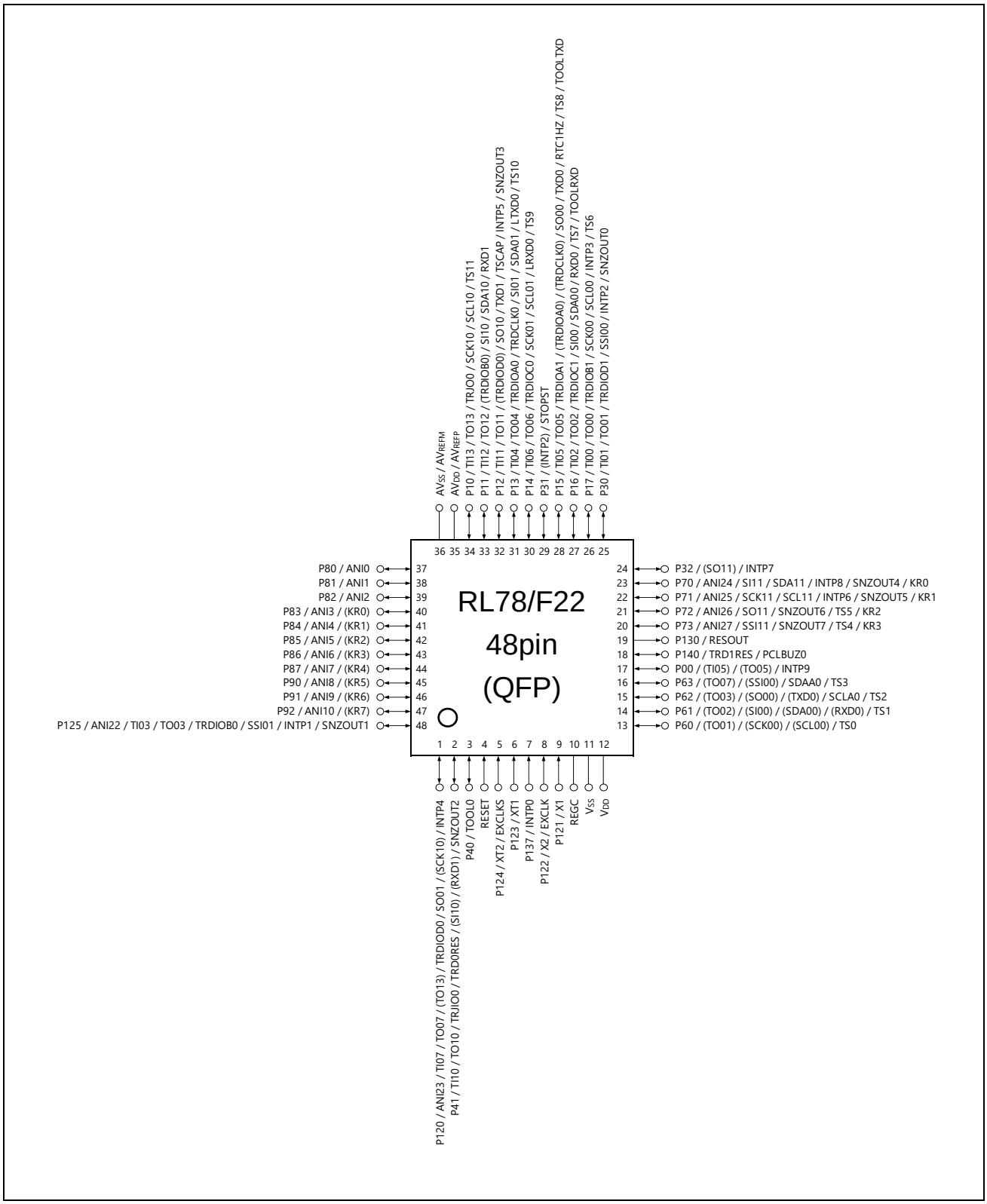


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx).

1.5.5 RL78/F22 Pin Configuration for 48-pin Products

- RL78/F22: 48-pin Plastic QFP

Figure 1-12. RL78/F22 Pin Configuration for 48-pin Products

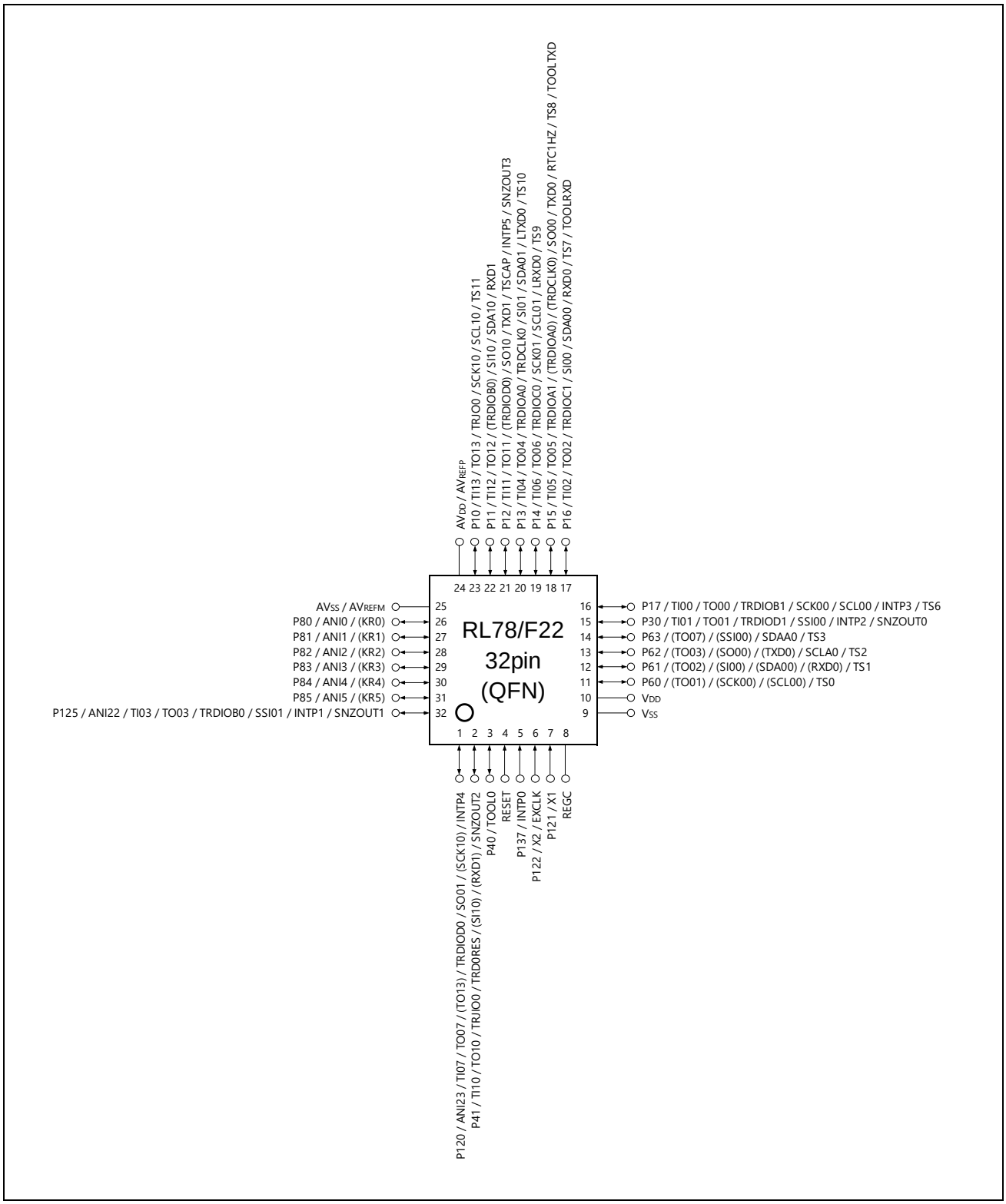


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx).

1.5.6 RL78/F22 Pin Configuration for 32-pin Products

- RL78/F22: 32-pin Plastic QFN

Figure 1-13. RL78/F22 Pin Configuration for 32-pin Products

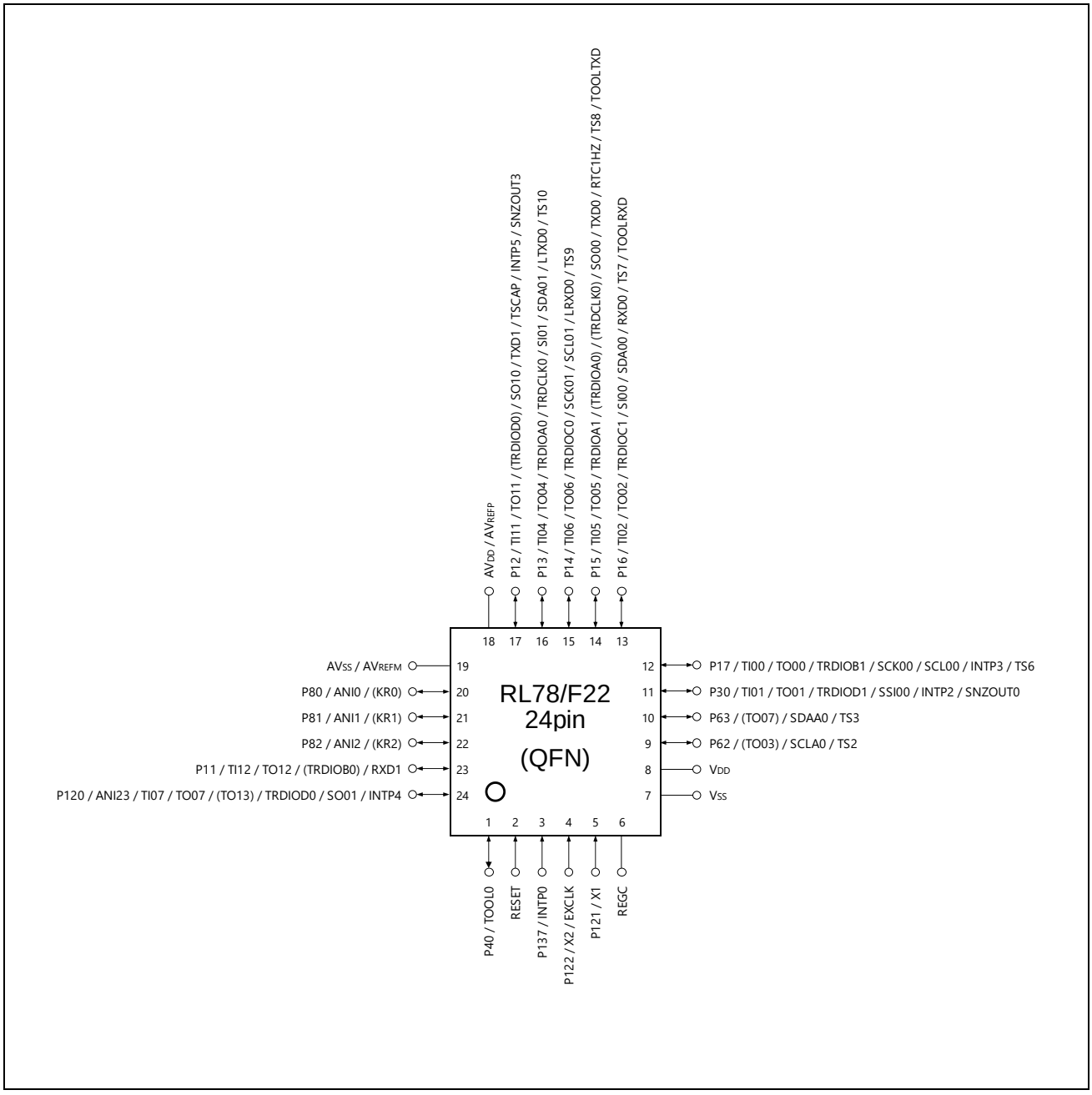


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx).

1.5.7 RL78/F22 Pin Configuration for 24-pin Products

- RL78/F22: 24-pin Plastic QFN

Figure 1-14. RL78/F22 Pin Configuration for 24-pin Products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers (PIORx).

2. PIN FUNCTIONS

2.1 Pin Function List

Pin I/O buffer power supplies depend on the product. **Tabel 2-1** shows the relationship between these power supplies and the pins. EV_{DD} indicates EV_{DD0} and EV_{DD1}.

Tabel 2-1. Pin I/O Buffer Power Supplies

(1) 24-pin products

Power Supply	Corresponding Pins
V_{DD}	• Port pins other than P80 to P82
AV_{DD}	• P80 to P82

(2) 32-pin products

Power Supply	Corresponding Pins
V_{DD}	• Port pins other than P80 to P85
AV_{DD}	• P80 to P85

(3) 48-pin products

Power Supply	Corresponding Pins
V_{DD}	• Port pins other than P80 to P87, P90 to P92
AV_{DD}	• P80 to P87, P90 to P92

(4) 64-pin products

Power Supply	Corresponding Pins
EV_{DD0}	• Port pins other than P80 to P87, P90 to P96, P121 to P124, P137
V_{DD}	• P121 to P124, P137 • Pins other than ports
AV_{DD}	• P80 to P87, P90 to P96

(5) 80-pin products

Power Supply	Corresponding Pins
EV_{DD0}	• Port pins other than P80 to P87, P90 to P97, P121 to P124, P137
V_{DD}	• P121 to P124, P137 • Pins other than ports
AV_{DD}	• P80 to P87, P90 to P97

(6) 100-pin products

Power Supply	Corresponding Pins
EV_{DD0}, EV_{DD1}	• Port pins other than P80 to P87, P90 to P97, P100 to P105, P121 to P124, P137
V_{DD}	• P121 to P124, P137 • Pins other than ports
AV_{DD}	• P80 to P87, P90 to P97, P100 to P105

This subchapter describes the 100-pin products of RL78/F25 and the 48-pin products of RL78/F22 as examples.

2.1.1 RL78/F25 100-pin Products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 • Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P01				(TI04)/(TO04)
P02				(TI06)/(TO06)
P03				(RTC1HZ)
P10	I/O	Port 1 • Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. • Use of an on-chip pull-up resistor can be specified by a software setting. • Output from P10 to P17 can be set to N-ch open-drain output. • For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJO0/SCK10/SCL10/ LTXD1/CTXD0/TS26
P11				TI12/TO12/(TRDIOB0)/SI10/ SDA10/RXD1/LRXD1/CRXD0/TS25
P12				TI11/TO11/(TRDIOD0)/INTP5/ SO10/TXD1/SNZOUT3/TSCAP
P13				TI04/TO04/TRDIOA0/TRDCLK0/ SI01/SDA01/LTXD0/TS24
P14				TI06/TO06/TRDIOC0/SCK01/ SCL01/LRXD0/TS23
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/ (TRDCLK0)/SO00/TXD0/ TOOLTXD/RTC1HZ/TS18
P16				TI02/TO02/TRDIOC1/SI00/ SDA00/RXD0/TOOLRXD/TS17
P17				TI00/TO00/TRDIOB1/SCK00/ SCL00/INTP3/TS16
P30	I/O	Port 3 • Input of P30 can be set to TTL input buffer. • Output from P32 can be set to N-ch open-drain output. • For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. • For input to P30, the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/SSI00/ INTP2/SNZOUT0
P31				TI14/TO14/STOPST/(INTP2)
P32				TI16/TO16/(SO11)/INTP7
P40	I/O	Port 4 • Use of an on-chip pull-up resistor can be specified by a software setting. • For input to P41 and P43, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/TRD0RES/ (SI10)/(RXD1)/VCOUT0/SNZOUT2
P42				(LTXD0)
P43				(LRXD0)
P44				(TI07)/(TO07)
P45				(TI10)/(TO10)
P46				(TI12)/(TO12)
P47				INTP13
P50	I/O	Port 5 • Input of P54 can be set to TTL input buffer. • Use of an on-chip pull-up resistor can be specified by a software setting. • For input to P50 and P52 to P54, the threshold level can be specified.	Input port	(SSI01)/(INTP3)/TS19
P51				(SO01)/INTP11/TS20
P52				(SCK01)/(STOPST)/TS21
P53				(SI01)/INTP10/TS22
P54				(TI11)/(TO11)/SSI10/TS27
P55				(TI13)/(TO13)/TS28
P56				(TI15)/(TO15)/(SNZOUT1)/TS29
P57				(TI17)/(TO17)/(SNZOUT0)/TS30
P60	I/O	Port 6 • Input of P62 and P63 can be set to TTL input buffer. Use of an on-chip pull-up resistor can be specified by a software setting. • Output from P60 to P63 can be set to N-ch open-drain output. • For input to P60 to P63, the threshold level can be specified.	Input port	(TO01)/(SCK00)/(SCL00)/CRXD1/TS0
P61				(TO02)/(SI00)/(SDA00)/(RXD0)/ CTXD1/TS1
P62				(TO03)/(SO00)/(TXD0)/SCLA0/TS2
P63				(TO07)/(SSI00)/SDAA0/TS3
P64				(TI14)/(TO14)/(SNZOUT3)/TS4
P65				(TI16)/(TO16)/(SNZOUT2)/TS5
P66				(TI00)/(TO00)/TS6
P67				(TI02)/(TO02)/TS7

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIORx). Only the STOPST function of P52 can be assigned via settings in the STOP status output control register (STPSTC).

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 • Input of P70, P71, and P73 can be set to TTL input buffer. • P70 to P74 can be set to analog input. • Use of an on-chip pull-up resistor can be specified by a software setting. • Output from P70 to P72 can be set to N-ch open-drain output. • For input to P70, P71, P73, and P75 to P77, the threshold level can be specified.	Analog input port	ANI24/KR0/TI15/TO15/INTP8/SI11/SDA11/(LTXD2)/SNZOUT4/TS15
P71				ANI25/KR1/TI17/TO17/INTP6/SCK11/SCL11/(LRXD2)/SNZOUT5/TS14
P72				ANI26/KR2/(CTXD0)/SO11/SNZOUT6/TS13
P73				ANI27/KR3/(CRXD0)/SSI11/SNZOUT7/TS12
P74				ANI28/KR4/(SO10)/(TXD1)/TS11
P75			Input port	KR5/(SI10)/(RXD1)/TS10
P76				KR6/(SCK10)/TS9
P77				KR7/(SSI10)/INTP12/TS8
P80	I/O	Port 8 • P80 to P87 can be set to analog input.	Analog input port	ANI0/ANO0
P81				ANI1
P82				ANI2/IVCMP00
P83				ANI3/IVCMP01
P84				ANI4/IVCMP02
P85				ANI5/IVCMP03/IVREF0
P86				ANI6
P87				ANI7
P90	I/O	Port 9 • P90 to P97 can be set to analog input.	Analog input port	ANI8
P91				ANI9
P92				ANI10
P93				ANI11
P94				ANI12
P95				ANI13
P96				ANI14
P97				ANI15
P100	I/O	Port 10 • P100 to P105 can be set to analog input. • For P106 and P107, use of an on-chip pull-up resistor can be specified by a software setting. • For input to P107, the threshold level can be specified.	Analog input port	ANI16
P101				ANI17
P102				ANI18
P103				ANI19
P104				ANI20
P105				ANI21
P106			Input port	(LTXD1)
P107				(LRXD1)
P120	I/O	Port 12 • Input of P125 can be set to TTL input buffer. • P120 and P125 can be set to analog input. • For P120 and P125 to P127, use of an on-chip pull-up resistor can be specified by a software setting. • Output from P120 can be set to N-ch open-drain output. • For input to P120 and P125, the threshold level can be specified.	Analog input port	ANI23/TI07/TO07/(TO13)/TRDIOD0/SO01/(SCK10)/(LTXD1)/INTP4
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O		Analog input port	ANI22/TI03/TO03/TRDIOB0/SSI01/(LRXD1)/INTP1/SNZOUT1
P126			Input port	(TI01)/(TO01)
P127				(TI03)/(TO03)
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	• Port 14 Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TRD1RES/PCLBUZ0
P150	I/O	Port 15 • Use of an on-chip pull-up resistor can be specified by a software setting. • For input to P150, P152, P153, and P154, the threshold level can be specified.	Input port	(SSI11)
P151				(SO11)
P152				(SI11)
P153				(SCK11)
P154				LRXD2/(SNZOUT7)
P155				LTXD2/(SNZOUT6)
P156				(SNZOUT5)
P157				(SNZOUT4)

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIORx).

2.1.2 RL78/F22 48-pin Products

(1/2)

Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0 • Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	(TI05)/(TO05)/INTP9
P10	I/O	Port 1 • Input of P10, P11, P13, P14, P16, and P17 can be set to TTL input buffer. • Use of an on-chip pull-up resistor can be specified by a software setting. • Output from P10 to P17 can be set to N-ch open-drain output. • For input to P10, P11, P13, P14, P16, and P17, the threshold level can be specified.	Input port	TI13/TO13/TRJO0/SCK10/SCL10/TS11
P11				TI12/TO12/(TRDIOB0)/SI10/SDA10/ RXD1
P12				TI11/TO11/(TRDIOD0)/INTP5/SO10/ TXD1/SNZOUT3/TSCAP
P13				TI04/TO04/TRDIOA0/TRDCLK0/SI01/ SDA01/LTXD0/TS10
P14				TI06/TO06/TRDIOC0/SCK01/SCL01/ LRXD0/TS9
P15				TI05/TO05/TRDIOA1/(TRDIOA0)/ (TRDCLK0)/SO00/TXD0/TOOLTXD/ RTC1HZ/TS8
P16				TI02/TO02/TRDIOC1/SI00/SDA00/ RXD0/TOOLRXD/TS7
P17				TI00/TO00/TRDIOB1/SCK00/SCL00/ INTP3/TS6
P30	I/O	Port 3 • Input of P30 can be set to TTL input buffer. • Output from P32 can be set to N-ch open-drain output. • For input to P30 to P32, use of an on-chip pull-up resistor can be specified by a software setting. • For input to P30, the threshold level can be specified.	Input port	TI01/TO01/TRDIOD1/SSI00/INTP2/ SNZOUT0
P31				STOPST/(INTP2)
P32				(SO11)/INTP7
P40	I/O	Port 4 • Use of an on-chip pull-up resistor can be specified by a software setting. • For input to P41, the threshold level can be specified.	Input port	TOOL0
P41				TI10/TO10/TRJIO0/TRD0RES/ (SI10)/(RXD1)/SNZOUT2
P60	I/O	Port 6 • Input of P62 and P63 can be set to TTL input buffer. • Use of an on-chip pull-up resistor can be specified by a software setting. • Output from P60 to P63 can be set to N-ch open-drain output. • For input to P60 to P63, the threshold level can be specified.	Input port	(TO01)/(SCK00)/(SCL00)/TS0
P61				(TO02)/(SI00)/(SDA00)/(RXD0))/TS1
P62				(TO03)/(SO00)/(TXD0)/SCLA0/TS2
P63				(TO07)/(SSI00)/SDAA0/TS3
P70	I/O	Port 7 • Input of P70, P71, and P73 can be set to TTL input buffer. • P70 to P73 can be set to analog input. • Use of an on-chip pull-up resistor can be specified by a software setting. • Output from P70 to P72 can be set to N-ch open-drain output. • For input to P70, P71, and P73, the threshold level can be specified.	Analog input port	ANI24/KR0/INTP8/SI11/SDA11/ SNZOUT4
P71				ANI25/KR1/INTP6/SCK11/SCL11/ SNZOUT5
P72				ANI26/KR2/SO11/SNZOUT6/TS5
P73				ANI27/KR3/SSI11/SNZOUT7/TS4
P80	I/O	Port 8 • P80 to P87 can be set to analog input.	Analog input port	ANI0
P81				ANI1
P82				ANI2
P83				ANI3
P84				ANI4
P85				ANI5
P86				ANI6
P87				ANI7
P90	I/O	Port 9 • P90 to P92 can be set to analog input.	Analog input port	ANI8
P91				ANI9
P92				ANI10

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIORx).

(2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P120	I/O	Port 12 • Input of P125 can be set to TTL input buffer. • P120 and P125 can be set to analog input. • For P120 and P125, use of an on-chip pull-up resistor can be specified by a software setting. • Output from P120 can be set to N-ch open-drain output. • For input to P120 and P125, the threshold level can be specified.	Analog input port	ANI23/TI07/TO07/(TO13)/TRDIOD0/ SO01/(SCK10)/INTP4
P121	Input		Input port	X1
P122				X2/EXCLK
P123				XT1
P124				XT2/EXCLKS
P125	I/O		Analog input port	ANI22/TI03/TO03/TRDIOB0/ SSI01/INTP1/SNZOUT1
P130	Output	Port 13	Output port	RESOUT
P137	Input		Input port	INTP0
P140	I/O	Port 14 • Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TRD1RES/PCLBUZ0

Remark Functions in parentheses in the above table can be assigned via settings in the peripheral I/O redirection registers (PIORx).

2.1.3 Pins for Each Product (Pins Other Than Port Pins)

This subchapter shows the pins other than the ports shown in **Table 2-2** and **Table 2-3** for each product.
√ indicates the pin that is provided in the product and – indicates the pin that is not provided.

Table 2-2. List of RL78/F25 Pins Other than Port Pins (1/6)

Pin Function	I/O	Function	Pin Count			
			100-pin	80-pin	64-pin	48-pin
ANI0	Input	A/D converter analog input (high-speed)	√	√	√	√
ANI1	Input		√	√	√	√
ANI2	Input		√	√	√	√
ANI3	Input		√	√	√	√
ANI4	Input		√	√	√	√
ANI5	Input		√	√	√	√
ANI6	Input		√	√	√	√
ANI7	Input		√	√	√	√
ANI8	Input		√	√	√	√
ANI9	Input		√	√	√	√
ANI10	Input		√	√	√	√
ANI11	Input		√	√	√	–
ANI12	Input		√	√	√	–
ANI13	Input		√	√	√	–
ANI14	Input		√	√	√	–
ANI15	Input		√	√	–	–
ANI16	Input	A/D converter analog input (normal-speed)	√	–	–	–
ANI17	Input		√	–	–	–
ANI18	Input		√	–	–	–
ANI19	Input		√	–	–	–
ANI20	Input		√	–	–	–
ANI21	Input		√	–	–	–
ANI22	Input		√	√	√	√
ANI23	Input		√	√	√	√
ANI24	Input		√	√	√	√
ANI25	Input		√	√	√	√
ANI26	Input		√	√	√	√
ANI27	Input		√	√	√	√
ANI28	Input		√	√	√	–
IVCMP00	Input	Comparator analog voltage input	√	√	√	√
IVCMP01	Input		√	√	√	√
IVCMP02	Input		√	√	√	√
IVCMP03	Input		√	√	√	√
IVREF0	Input	Comparator reference voltage input	√	√	√	√

Table 2-2. List of RL78/F25 Pins Other than Port Pins (2/6)

Pin Function	I/O	Function	Pin Count			
			100-pin	80-pin	64-pin	48-pin
TS0	I/O	Electrostatic capacitance measurement pins (touch sensor)	√	√	√	√
TS1	I/O		√	√	√	√
TS2	I/O		√	√	√	√
TS3	I/O		√	√	√	√
TS4	I/O		√	√	–	–
TS5	I/O		√	√	–	–
TS6	I/O		√	√	–	–
TS7	I/O		√	√	–	–
TS8	I/O		√	√	√	–
TS9	I/O		√	√	√	–
TS10	I/O		√	√	√	–
TS11	I/O		√	√	√	–
TS12	I/O		√	√	√	√
TS13	I/O		√	√	√	√
TS14	I/O		√	√	√	√
TS15	I/O		√	√	√	√
TS16	I/O		√	√	√	√
TS17	I/O		√	√	√	√
TS18	I/O		√	√	√	√
TS19	I/O		√	√	√	–
TS20	I/O		√	√	√	–
TS21	I/O		√	√	√	–
TS22	I/O		√	√	√	–
TS23	I/O		√	√	√	√
TS24	I/O		√	√	√	√
TS25	I/O		√	√	√	√
TS26	I/O		√	√	√	√
TS27	I/O		√	√	–	–
TS28	I/O		√	√	–	–
TS29	I/O		√	√	–	–
TS30	I/O		√	√	–	–
TSCAP	–	Pin for connecting a power supply stabilization capacitor for the touch sensor interface. Connect this pin to V_{SS} via a capacitor (10 nF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.	√	√	√	√

Table 2-2. List of RL78/F25 Pins Other than Port Pins (3/6)

Pin Function	I/O	Function	Pin Count			
			100-pin	80-pin	64-pin	48-pin
KR0	Input	Key interrupt input	√	√	√	√
KR1	Input		√	√	√	√
KR2	Input		√	√	√	√
KR3	Input		√	√	√	√
KR4	Input		√	√	√	√
KR5	Input		√	√	√	√
KR6	Input		√	√	√	√
KR7	Input		√	√	√	√
ANO0	Output	D/A converter output	√	√	√	√
VCOUT0	Output	Comparator output	√	√	√	√
TI00	Input	16-bit timer 00 input	√	√	√	√
TI01	Input	16-bit timer 01 input (8-bit mode available)	√	√	√	√
TI02	Input	16-bit timer 02 input	√	√	√	√
TI03	Input	16-bit timer 03 input (8-bit mode available)	√	√	√	√
TI04	Input	16-bit timer 04 input	√	√	√	√
TI05	Input	16-bit timer 05 input	√	√	√	√
TI06	Input	16-bit timer 06 input	√	√	√	√
TI07	Input	16-bit timer 07 input	√	√	√	√
TI10	Input	16-bit timer 10 input	√	√	√	√
TI11	Input	16-bit timer 11 input (8-bit mode available)	√	√	√	√
TI12	Input	16-bit timer 12 input	√	√	√	√
TI13	Input	16-bit timer 13 input (8-bit mode available)	√	√	√	√
TI14	Input	16-bit timer 14 input	√	√	√	√
TI15	Input	16-bit timer 15 input	√	√	√	√
TI16	Input	16-bit timer 16 input	√	√	√	√
TI17	Input	16-bit timer 17 input	√	√	√	√
TO00	Output	16-bit timer 00 output	√	√	√	√
TO01	Output	16-bit timer 01 output (8-bit mode available)	√	√	√	√
TO02	Output	16-bit timer 02 output	√	√	√	√
TO03	Output	16-bit timer 03 output (8-bit mode available)	√	√	√	√
TO04	Output	16-bit timer 04 output	√	√	√	√
TO05	Output	16-bit timer 05 output	√	√	√	√
TO06	Output	16-bit timer 06 output	√	√	√	√
TO07	Output	16-bit timer 07 output	√	√	√	√
TO10	Output	16-bit timer 10 output	√	√	√	√
TO11	Output	16-bit timer 11 output (8-bit mode available)	√	√	√	√
TO12	Output	16-bit timer 12 output	√	√	√	√
TO13	Output	16-bit timer 13 output (8-bit mode available)	√	√	√	√
TO14	Output	16-bit timer 14 output	√	√	√	√
TO15	Output	16-bit timer 15 output	√	√	√	√
TO16	Output	16-bit timer 16 output	√	√	√	√
TO17	Output	16-bit timer 17 output	√	√	√	√

Table 2-2. List of RL78/F25 Pins Other than Port Pins (4/6)

Pin Function	I/O	Function	Pin Count			
			100-pin	80-pin	64-pin	48-pin
TRJIO0	I/O	Timer RJ input/output	√	√	√	√
TRJO0	Output	Timer RJ output	√	√	√	√
TRDCLK0	Input	Timer RDe external clock input	√	√	√	√
TRDIOA0	I/O	Timer RDe0 input/output	√	√	√	√
TRDIOB0	I/O		√	√	√	√
TRDIOC0	I/O		√	√	√	√
TRDIOD0	I/O		√	√	√	√
TRDIOA1	I/O	Timer RDe1 input/output	√	√	√	√
TRDIOB1	I/O		√	√	√	√
TRDIOC1	I/O		√	√	√	√
TRDIOD1	I/O		√	√	√	√
TRD0RES	Input	Timer RDe0 external timer counter clear trigger input	√	√	√	√
TRD1RES	Input	Timer RDe1 external timer counter clear trigger input	√	√	√	√
RXD0	Input	Serial data input to UART0	√	√	√	√
RXD1	Input	Serial data input to UART1	√	√	√	√
TXD0	Output	Serial data output from UART0	√	√	√	√
TXD1	Output	Serial data output from UART1	√	√	√	√
SCLA0	I/O	Clock input/output for IICA0	√	√	√	√
SCL00	Output	Clock output from simplified I^2C	√	√	√	√
SCL01	Output		√	√	√	√
SCL10	Output		√	√	√	√
SCL11	Output		√	√	√	√
SDAA0	I/O	Serial data input/output for IICA0	√	√	√	√
SDA00	I/O	Serial data input/output for simplified I^2C	√	√	√	√
SDA01	I/O		√	√	√	√
SDA10	I/O		√	√	√	√
SDA11	I/O		√	√	√	√
SCK00	I/O	Clock input/output for CSI00	√	√	√	√
SCK01	I/O	Clock input/output for CSI01	√	√	√	√
SCK10	I/O	Clock input/output for CSI10	√	√	√	√
SCK11	I/O	Clock input/output for CSI11	√	√	√	√
SI00	Input	Serial data input to CSI00	√	√	√	√
SI01	Input	Serial data input to CSI01	√	√	√	√
SI10	Input	Serial data input to CSI10	√	√	√	√
SI11	Input	Serial data input to CSI11	√	√	√	√
SO00	Output	Serial data output from CSI00	√	√	√	√
SO01	Output	Serial data output from CSI01	√	√	√	√
SO10	Output	Serial data output from CSI10	√	√	√	√
SO11	Output	Serial data output from CSI11	√	√	√	√
SSI00	Input	Slave select input to CSI00 (SPI00)	√	√	√	√
SSI01	Input	Slave select input to CSI01 (SPI01)	√	√	√	√
SSI10	Input	Slave select input to CSI10 (SPI10)	√	√	√	–
SSI11	Input	Slave select input to CSI11 (SPI11)	√	√	√	√

Table 2-2. List of RL78/F25 Pins Other than Port Pins (5/6)

Pin Function	I/O	Function	Pin Count			
			100-pin	80-pin	64-pin	48-pin
CRXD0	Input	Serial data input to CAN	√	√	√	√
CRXD1	Input		√	√	√	√
CTXD0	Output	Serial data output from CAN	√	√	√	√
CTXD1	Output		√	√	√	√
LRXD0	Input	Serial data input to LIN	√	√	√	√
LRXD1	Input		√	√	√	√
LRXD2	Input		√	√	√	√
LTXD0	Output	Serial data output from LIN	√	√	√	√
LTXD1	Output		√	√	√	√
LTXD2	Output		√	√	√	√
INTP0	Input	External interrupt input	√	√	√	√
INTP1	Input		√	√	√	√
INTP2	Input		√	√	√	√
INTP3	Input		√	√	√	√
INTP4	Input		√	√	√	√
INTP5	Input		√	√	√	√
INTP6	Input		√	√	√	√
INTP7	Input		√	√	√	√
INTP8	Input		√	√	√	√
INTP9	Input		√	√	√	√
INTP10	Input		√	√	√	–
INTP11	Input		√	√	√	–
INTP12	Input		√	√	√	–
INTP13	Input		√	√	–	–
PCLBUZ0	Output	Clock output/buzzer output 0	√	√	√	√
RESOUT	Output	Reset output	√	√	√	√
STOPST	Output	STOP status output	√	√	√	√
SNZOUT0	Output	SNOOZE status output	√	√	√	√
SNZOUT1	Output		√	√	√	√
SNZOUT2	Output		√	√	√	√
SNZOUT3	Output		√	√	√	√
SNZOUT4	Output		√	√	√	√
SNZOUT5	Output		√	√	√	√
SNZOUT6	Output		√	√	√	√
SNZOUT7	Output		√	√	√	√
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√	√

Table 2-2. List of RL78/F25 Pins Other than Port Pins (6/6)

Pin Function	I/O	Function	Pin Count			
			100-pin	80-pin	64-pin	48-pin
EXCLK	Input	External clock input for main system clock	√	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	√	√	√
X1	–	Resonator connection for main system clock	√	√	√	√
X2	–		√	√	√	√
XT1	–	Resonator connection for subsystem clock	√	√	√	√
XT2	–		√	√	√	√
RESET	Input	External reset input	√	√	√	√
REGC	–	Regulator output stabilization capacitance connection for internal operation. Connect to Vss via the capacitor (0.47 to 1 µF).	√	√	√	√
V_{DD}	–	Positive power supply for the P121 to P124, P137, and RESET pins	√	√	√	√
AV_{DD}	–	Positive power supply for the A/D converter, D/A converter, comparator, P80 to P87, P90 to P97, and P100 to P105	√	√	√	√
EV_{DD0}	–	Positive power supply for the pins that are not connected to V_{DD} and AV_{DD}	√	√	√	–
EV_{DD1}	–		√	–	–	–
AV_{REFP}	Input	A/D converter reference voltage (+ side) input	√	√	√	√
AV_{REFM}	Input	A/D converter reference voltage (− side) input	√	√	√	√
V_{SS}	–	Ground potential for the P121 to P124, P137, and RESET pins	√	√	√	√
AV_{SS}	–	Ground potential for the A/D converter, D/A converter, comparator, P80 to P87, P90 to P97, and P100 to P105	√	√	√	√
EV_{SS0}	–	Ground potential for the pins that are not connected to V_{SS} and AV_{SS}	√	√	√	–
EV_{SS1}	–		√	–	–	–
TOOLRXD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√	√
TOOLTXD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√	√
TOOL0	I/O	Data input/output for flash memory programmer/debugger	√	√	√	√

Table 2-3. List of RL78/F22 Pins Other than Port Pins (1/6)

Pin Function	I/O	Function	Pin Count		
			48-pin	32-pin	24-pin
ANI0	Input	A/D converter analog input (high-speed)	√	√	√
ANI1	Input		√	√	√
ANI2	Input		√	√	√
ANI3	Input		√	√	–
ANI4	Input		√	√	–
ANI5	Input		√	√	–
ANI6	Input		√	–	–
ANI7	Input		√	–	–
ANI8	Input		√	–	–
ANI9	Input		√	–	–
ANI10	Input		√	–	–
ANI22	Input	A/D converter analog input (normal-speed)	√	√	–
ANI23	Input		√	√	√
ANI24	Input		√	–	–
ANI25	Input		√	–	–
ANI26	Input		√	–	–
ANI27	Input		√	–	–
KR0	Input	Key interrupt input	√	√	√
KR1	Input		√	√	√
KR2	Input		√	√	√
KR3	Input		√	√	–
KR4	Input		√	√	–
KR5	Input		√	√	–
KR6	Input		√	–	–
KR7	Input		√	–	–

Table 2-3. List of RL78/F22 Pins Other than Port Pins (2/6)

Pin Function	I/O	Function	Pin Count		
			48-pin	32-pin	24-pin
TS0	I/O	Electrostatic capacitance measurement pins (touch sensor)	√	√	–
TS1	I/O		√	√	–
TS2	I/O		√	√	√
TS3	I/O		√	√	√
TS4	I/O		√	–	–
TS5	I/O		√	–	–
TS6	I/O		√	√	√
TS7	I/O		√	√	√
TS8	I/O		√	√	√
TS9	I/O		√	√	√
TS10	I/O		√	√	√
TS11	I/O		√	√	–
TSCAP	–	Pin for connecting a power supply stabilization capacitor for the touch sensor interface. Connect this pin to V_{SS} via a capacitor (10 nF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.	√	√	√

Table 2-3. List of RL78/F22 Pins Other than Port Pins (3/6)

Pin Function	I/O	Function	Pin Count		
			48-pin	32-pin	24-pin
TI00	Input	16-bit timer 00 input	√	√	√
TI01	Input	16-bit timer 01 input (8-bit mode available)	√	√	√
TI02	Input	16-bit timer 02 input	√	√	√
TI03	Input	16-bit timer 03 input (8-bit mode available)	√	√	–
TI04	Input	16-bit timer 04 input	√	√	√
TI05	Input	16-bit timer 05 input	√	√	√
TI06	Input	16-bit timer 06 input	√	√	√
TI07	Input	16-bit timer 07 input	√	√	√
TI10	Input	16-bit timer 10 input	√	√	–
TI11	Input	16-bit timer 11 input (8-bit mode available)	√	√	√
TI12	Input	16-bit timer 12 input	√	√	√
TI13	Input	16-bit timer 13 input (8-bit mode available)	√	√	–
TO00	Output	16-bit timer 00 output	√	√	√
TO01	Output	16-bit timer 01 output (8-bit mode available)	√	√	√
TO02	Output	16-bit timer 02 output	√	√	√
TO03	Output	16-bit timer 03 output (8-bit mode available)	√	√	√
TO04	Output	16-bit timer 04 output	√	√	√
TO05	Output	16-bit timer 05 output	√	√	√
TO06	Output	16-bit timer 06 output	√	√	√
TO07	Output	16-bit timer 07 output	√	√	√
TO10	Output	16-bit timer 10 output	√	√	–
TO11	Output	16-bit timer 11 output (8-bit mode available)	√	√	√
TO12	Output	16-bit timer 12 output	√	√	√
TO13	Output	16-bit timer 13 output (8-bit mode available)	√	√	√
TRJIO0	I/O	Timer RJ input/output	√	√	–
TRJO0	Output	Timer RJ output	√	√	–
TRDCLK0	Input	Timer RDe external clock input	√	√	√
TRDIOA0	I/O	Timer RDe0 input/output	√	√	√
TRDIOB0	I/O		√	√	√
TRDIOC0	I/O		√	√	√
TRDIOD0	I/O		√	√	√
TRDIOA1	I/O	Timer RDe1 input/output	√	√	√
TRDIOB1	I/O		√	√	√
TRDIOC1	I/O		√	√	√
TRDIOD1	I/O		√	√	√
TRD0RES	Input	Timer RDe0 external timer counter clear trigger input	√	√	–
TRD1RES	Input	Timer RDe1 external timer counter clear trigger input	√	–	–

Table 2-3. List of RL78/F22 Pins Other than Port Pins (4/6)

Pin Function	I/O	Function	Pin Count		
			48-pin	32-pin	24-pin
RXD0	Input	Serial data input to UART0	√	√	√
RXD1	Input	Serial data input to UART1	√	√	√
TXD0	Output	Serial data output from UART0	√	√	√
TXD1	Output	Serial data output from UART1	√	√	√
SCLA0	I/O	Clock input/output for IICA0	√	√	√
SCL00	Output	Clock output from simplified I^2C	√	√	√
SCL01	Output		√	√	√
SCL10	Output		√	√	–
SCL11	Output		√	–	–
SDAA0	I/O	Serial data input/output for IICA0	√	√	√
SDA00	I/O	Serial data input/output for simplified I^2C	√	√	√
SDA01	I/O		√	√	√
SDA10	I/O		√	√	–
SDA11	I/O		√	–	–
SCK00	I/O	Clock input/output for CSI00	√	√	√
SCK01	I/O	Clock input/output for CSI01	√	√	√
SCK10	I/O	Clock input/output for CSI10	√	√	–
SCK11	I/O	Clock input/output for CSI11	√	–	–
SI00	Input	Serial data input to CSI00	√	√	√
SI01	Input	Serial data input to CSI01	√	√	√
SI10	Input	Serial data input to CSI10	√	√	–
SI11	Input	Serial data input to CSI11	√	–	–
SO00	Output	Serial data output from CSI00	√	√	√
SO01	Output	Serial data output from CSI01	√	√	√
SO10	Output	Serial data output from CSI10	√	√	√
SO11	Output	Serial data output from CSI11	√	–	–
SSI00	Input	Slave select input to CSI00 (SPI00)	√	√	√
SSI01	Input	Slave select input to CSI01 (SPI01)	√	√	–
SSI11	Input	Slave select input to CSI11 (SPI11)	√	–	–
LRXD0	Input	Serial data input to LIN	√	√	√
LTXD0	Output	Serial data output from LIN	√	√	√

Table 2-3. List of RL78/F22 Pins Other than Port Pins (5/6)

Pin Function	I/O	Function	Pin Count		
			48-pin	32-pin	24-pin
INTP0	Input	External interrupt input	√	√	√
INTP1	Input		√	√	–
INTP2	Input		√	√	√
INTP3	Input		√	√	√
INTP4	Input		√	√	√
INTP5	Input		√	√	√
INTP6	Input		√	–	–
INTP7	Input		√	–	–
INTP8	Input		√	–	–
INTP9	Input		√	–	–
PCLBUZ0	Output	Clock output/buzzer output 0	√	–	–
RESOUT	Output	Reset output	√	–	–
STOPST	Output	STOP status output	√	–	–
SNZOUT0	Output	SNOOZE status output	√	√	√
SNZOUT1	Output		√	√	–
SNZOUT2	Output		√	√	–
SNZOUT3	Output		√	√	√
SNZOUT4	Output		√	–	–
SNZOUT5	Output		√	–	–
SNZOUT6	Output		√	–	–
SNZOUT7	Output		√	–	–
RTC1HZ	Output	Real-time clock correction clock (1 Hz) output	√	√	√

Table 2-3. List of RL78/F22 Pins Other than Port Pins (6/6)

Pin Function	I/O	Function	Pin Count		
			48-pin	32-pin	24-pin
EXCLK	Input	External clock input for main system clock	√	√	√
EXCLKS	Input	External clock input for subsystem clock	√	–	–
X1	–	Resonator connection for main system clock	√	√	√
X2	–		√	√	√
XT1	–	Resonator connection for subsystem clock	√	–	–
XT2	–		√	–	–
RESET	Input	External reset input	√	√	√
REGC	–	Regulator output stabilization capacitance connection for internal operation. Connect to Vss via the capacitor (0.47 to 1 μF).	√	√	√
V_{DD}	–	Positive power supply for port pins (except pins connected to AV_{DD}) and RESET pins	√	√	√
AV_{DD}	–	Positive power supply for the A/D converter, P80 to P87 and P90 to P92	√	√	√
AV_{REFP}	Input	A/D converter reference voltage (+ side) input	√	√	√
AV_{REFM}	Input	A/D converter reference voltage (− side) input	√	√	√
V_{SS}	–	Ground potential for port pins (except pins connected to AV_{SS}) and RESET pins	√	√	√
AV_{SS}	–	Ground potential for the A/D converter, P80 to P87 and P90 to P92	√	√	√
TOOLRXD	Input	UART reception pin for the external device connection used during flash memory programming	√	√	√
TOOLTXD	Output	UART transmission pin for the external device connection used during flash memory programming	√	√	√
TOOL0	I/O	Data input/output for flash memory programmer/debugger	√	√	√

3. ELECTRICAL SPECIFICATIONS (RL78/F25)

Cautions 1. RL78/F25 has an on-chip debug function for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

3. The pins mounted depending on the product. For details, refer to "1.5 Pin Configurations" and "2.1 Pin Function List".

3.1 Absolute Maximum Ratings

(1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	$V_{DD} = AV_{DD}$	−0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1} = V_{DD}$	−0.5 to +6.5	V
	V_{SS}, AV_{SS}	$V_{SS} = AV_{SS}$	−0.5 to +0.3	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to + 2.1 and −0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157	−0.3 to EV_{DD0} + 0.3 and −0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P80 to P87, P90 to P97, P100 to P105	−0.3 to AV_{DD} + 0.3 Note 2	V
	V_{I3}	P121 to P124, P137, RESET	−0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157	−0.3 to EV_{DD0} + 0.3 and −0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P80 to P87, P90 to P97, P100 to P105	−0.3 to AV_{DD} + 0.3	V
Analog input voltage	V_{AI1}	ANI22 to ANI28	−0.3 to EV_{DD0} + 0.3 and −0.3 to AV_{DD} + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI21	−0.3 to AV_{DD} + 0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. For pins to be used in A/D conversion, the voltage should not exceed the value AV_{DD} + 0.3.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157	−40	mA
		Total of all pins −170 mA	P01, P02, P40 to P47, P120, P125 to P127, P150 to P153	−70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	−100	mA
	I_{OH2}	Per pin	P80 to P87, P90 to P97, P100 to P105	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157	40	mA
		Total of all pins 170 mA	P01, P02, P40 to P47, P120, P125 to P127, P150 to P153	70	mA
			P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157	100	mA
	I_{OL2}	Per pin	P80 to P87, P90 to P97, P100 to P105	1	mA
		Total of all pins		5	mA

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/3)

Parameter	Symbol	Conditions			Ratings	Unit
Positive injected current ($V_I > V_{DD}$) Note	I_{INJP}	Per pin	P00 to P03, P10, P11, P13 to P17, P30 to P32, P41 to P47, P50 to P57, P60 to P67, P75 to P77, P106, P107, P126, P127, P140, P150 to P157		5	mA
			P70 to P74, P80 to P87, P90 to P97, P100 to P105, P120, P125		2	mA
Negative injected current ($V_I < V_{SS}$) Note	I_{INJN}	Per pin	P00 to P03, P10, P11, P13 to P17, P30 to P32, P41 to P47, P50 to P57, P60 to P67, P75 to P77, P106, P107, P126, P127, P140, P150 to P157		−5	mA
			P70 to P74, P80 to P87, P90 to P97, P100 to P105, P120, P125		−0.5	mA
Sum of all positive injected currents Note	ΣI_{INJP}	Total of all pins	P00 to P03, P10, P11, P13 to P17, P30 to P32, P41 to P47, P50 to P57, P60 to P67, P75 to P77, P106, P107, P126, P127, P140, P150 to P157		40	mA
			P70 to P74, P80 to P87, P90 to P97, P100 to P105, P120, P125		10	mA
Sum of all negative injected currents Note	ΣI_{INJN}	Total of all pins	P00 to P03, P10, P11, P13 to P17, P30 to P32, P41 to P47, P50 to P57, P60 to P67, P75 to P77, P106, P107, P126, P127, P140, P150 to P157		−40	mA
			P70 to P74, P80 to P87, P90 to P97, P100 to P105, P120, P125		−2	mA
Total of all injected currents Note	$\Sigma\|I_{INJP}\| + \Sigma\|I_{INJN}\|$	Total of all pins	P00 to P03, P10, P11, P13 to P17, P30 to P32, P41 to P47, P50 to P57, P60 to P67, P75 to P77, P106, P107, P126, P127, P140, P150 to P157		40	mA
			P70 to P74, P80 to P87, P90 to P97, P100 to P105, P120, P125		10	mA
Operating ambient temperature	T_A	In normal operation mode		Grade 3 products	−40 to +105	°C
				Grade 4 products	−40 to +125	
		In flash memory programming mode		Grade 3 products	−40 to +105	°C
				Grade 4 products	−40 to +125	
Operating temperature	T_{OPR}			Grade 3 products	−40 to +105	°C
				Grade 4 products	−40 to +125	
Storage temperature	T_{stg}				−65 to +150	°C

Note Conditions: 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

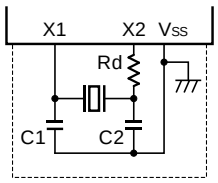
Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. V_I: Input voltage level to the port pins.

3.2 Oscillator Characteristics

3.2.1 Main System Clock Oscillator Characteristics

($T_A = T_{OPR}$, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

3.2.2 On-chip Oscillator Characteristics

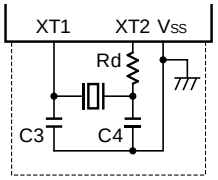
($T_A = T_{OPR}$, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}		2		80	MHz
High-speed on-chip oscillator clock frequency accuracy	–		−1.0		+1.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}, f_{WDT}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	–		−15		+15	%

Note High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/040C2H) and bits 0 to 2 of the HOCODIV register.

3.2.3 Subsystem Clock Oscillator Characteristics

($T_A = T_{OPR}$, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})	2.7 V ≤ V_{DD} ≤ 5.5 V	29.0	32.768	35.0	kHz

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption and thus required to be adequately evaluated on the system. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

3.2.4 PLL Circuit Characteristics

($T_A = T_{OPR}$, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
PLL input enable clock frequency Note 1	f_{PLLI}	f_{MAIN}: 4.0 MHz	FMAINDIV[1:0] = 00B	3.92	4.0	4.08	MHz
		f_{MAIN}: 8.0 MHz	FMAINDIV[1:0] = 00B	7.84	8.0	8.16	MHz
		f_{MAIN}: 16.0 MHz	FMAINDIV[1:0] = 10B	7.84	8.0	8.16	MHz
		f_{MAIN}: 20.0 MHz	FMAINDIV[1:0] = 11B	4.90	5.0	5.10	MHz
PLL output frequency (center value)	f_{PLL}	f_{MAIN}: 20 MHz, PLLMULA = 0, PLLMUL = 1	PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 16/2			MHz
			PLLDIV0 = 0, FPLLDIV = 1, PLLDIV1 = 1	f_{PLLI} × 16			MHz
		f_{MAIN}: 4 MHz, PLLMULA = 1, PLLMUL = 1	PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 20/2			MHz
			PLLDIV0 = 0, FPLLDIV = 1, PLLDIV1 = 1	f_{PLLI} × 20			MHz
		f_{MAIN}: 8 MHz or 16 MHz, PLLMULA = 0, PLLMUL = 0	PLLDIV0 = 1, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 12/4			MHz
			PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 1	f_{PLLI} × 12/2			MHz
		f_{MAIN}: 8 MHz or 16 MHz, PLLMULA = 0, PLLMUL = 1	PLLDIV0 = 1, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 16/4			MHz
			PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 1	f_{PLLI} × 16/2			MHz
		f_{MAIN}: 8 MHz or 16 MHz, PLLMULA = 1, PLLMUL = 0	PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 10/2			MHz
			PLLDIV0 = 0, FPLLDIV = 1, PLLDIV1 = 1	f_{PLLI} × 10			MHz
Long-term jitter Note 2	t_{LJ}	term = 1 μs		−1		+1	ns
		term = 10 μs		−1		+1	ns
		term = 20 μs		−2		+2	ns

Notes 1. X1 clock or external main system clock can be selected as the PLL input clock.

2. Guaranteed by design, but not tested before shipment.

Remark f_{MAIN}: Main system clock frequency.

3.3 DC Characteristics

3.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **2. PIN FUNCTIONS**.

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) **(1/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for: P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			−5.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			−3.0	mA
		Per pin for: P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			−0.6	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			−0.2	mA
		Total of: P01, P02, P40 to P47, P120, P125 to P127, P150 to P153 (for duty factors ≤ 70% Note 2)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			−20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			−10.0	mA
		Total of: P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70% Note 2)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			−30.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			−19.0	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	Grade 3 products: 4.0 V ≤ EV_{DD0} ≤ 5.5 V			−50.0	mA
			Grade 3 products: 2.7 V ≤ EV_{DD0} < 4.0 V			−29.0	mA
			Grade 4 products: 4.0 V ≤ EV_{DD0} ≤ 5.5 V			−42.0	mA
			Grade 4 products: 2.7 V ≤ EV_{DD0} < 4.0 V			−29.0	mA
	I_{OH2}	Per pin for: P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ AV_{DD} ≤ 5.5 V			−0.1	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	2.7 V ≤ AV_{DD} ≤ 5.5 V			−2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from EV_{DD0}, EV_{DD1}, AV_{DD}, and V_{DD} pins to an output pin.

2. These output current values are obtained under the condition that the duty factor is 70% or less.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins $(I_{OH} \times 0.7) / (n \times 0.01)$

<Example> Where I_{OH} = −10.0 mA and n = 80%
Total output current of pins = $(-10.0 \times 0.7) / (80 \times 0.01) \approx -8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution P10 to P17, P32, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) **(2/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for: P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157	4.0 V ≤ EV_{DD0} ≤ 5.5 V			8.5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			4.0	mA
		Per pin for: P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			0.59	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			0.07	mA
		Total of: P01, P02, P40 to P47, P120, P125 to P127, P150 to P153 (for duty factors ≤ 70% Note 2)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			20.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
		Total of: P00, P03, P10 to P17, P30 to P32, P50 to P57, P60 to P67, P70 to P77, P106, P107, P130, P140, P154 to P157 (for duty factors ≤ 70% Note 2)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			45.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			65.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			50.0	mA
	I_{OL2}	Per pin for: P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ AV_{DD} ≤ 5.5 V			0.4	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	2.7 V ≤ AV_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1}, AV_{SS}, and V_{SS} pins.

2. These output current values are obtained under the condition that the duty factor is 70% or less.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins $(I_{OL} \times 0.7) / (n \times 0.01)$
  <Example> Where I_{OL} = 10.0 mA and n = 80%
  Total output current of pins = $(10.0 \times 0.7) / (80 \times 0.01) \approx 8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) **(3/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.65 EV_{DD0}		EV_{DD0} Note	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.7 EV_{DD0}		EV_{DD0} Note	V
	V_{IH2}	P10, P11, P13, P14, P16, P17, P30, P41, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P120, P125, P150, P152, P153, P154 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0.8 EV_{DD0}		EV_{DD0} Note	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0.85 EV_{DD0}		EV_{DD0} Note	V
	V_{IH3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0} Note	V
			2.7 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0} Note	V
	V_{IH4}	P80 to P87, P90 to P97, P100 to P105 (fixed to Schmitt 3 mode)	4.0 V ≤ AV_{DD} ≤ 5.5 V	0.8 AV_{DD}		AV_{DD}	V
			2.7 V ≤ AV_{DD} < 4.0 V	0.85 AV_{DD}		AV_{DD}	V
	V_{IH5}	RESET (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.65 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.7 V_{DD}		V_{DD}	V
	V_{IH6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.8 V_{DD}		V_{DD}	V
	V_{IH7}	P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.85 V_{DD}		V_{DD}	V

Note The maximum value of V_{IH} of the pins P10 to P17, P32, P60 to P63, P70 to P72, and P120 is EV_{DD0}, even in N-ch open-drain mode and set to high-level output.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) **(4/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157 (Schmitt 1 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.35 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.3 EV_{DD0}	V
	V_{IL2}	P10, P11, P13, P14, P16, P17, P30, P41, P43, P50, P52 to P54, P60 to P63, P70, P71, P73, P75 to P77, P107, P120, P125, P150, P152, P153, P154 (Schmitt 3 mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.5 EV_{DD0}	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.4 EV_{DD0}	V
	V_{IL3}	P10, P11, P13, P14, P16, P17, P30, P54, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			2.7 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
	V_{IL4}	P80 to P87, P90 to P97, P100 to P105 (fixed to Schmitt 3 mode)	4.0 V ≤ AV_{DD} ≤ 5.5 V	0		0.5 AV_{DD}	V
			2.7 V ≤ AV_{DD} < 4.0 V	0		0.4 AV_{DD}	V
	V_{IL5}	RESET (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.35 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.3 V_{DD}	V
	V_{IL6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V
	V_{IL7}	P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.5 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.4 V_{DD}	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) **(5/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = −5.0 mA	EV_{DD0} − 0.9			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = −3.0 mA	EV_{DD0} − 0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = −1.0 mA	EV_{DD0} − 0.5			V
	V_{OH2}	P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ AV_{DD} ≤ 5.5 V I_{OH2} = −100 µA	AV_{DD} − 0.5			V
	V_{OH3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = −0.6 mA	EV_{DD0} − 0.8			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH3} = −0.2 mA	EV_{DD0} − 0.5			V
Output voltage, low	V_{OL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 4.0 mA			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
	V_{OL2}	P80 to P87, P90 to P97, P100 to P105	2.7 V ≤ AV_{DD} ≤ 5.5 V I_{OL2} = 400 µA			0.4	V
	V_{OL3}	P10, P12, P14, P30, P120, P140 (special slew rate)	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.6 mA			0.8	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 0.07 mA			0.5	V

Caution P10 to P17, P32, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) **(6/6)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157	$V_I = EV_{DD0}$				1	μA
	I_{LIH2}	P80 to P87, P90 to P97, P100 to P105	$V_I = AV_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P137, RESET	$V_I = V_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157	$V_I = EV_{SS0}$				−1	μA
	I_{LIL2}	P80 to P87, P90 to P97, P100 to P105	$V_I = AV_{SS}$				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
	I_{LIL4}	P137, RESET	$V_I = V_{SS}$				−1	μA
Positive injected current Note	$I_{INJPRMS}$	P00 to P03, P10, P11, P13 to P17, P30 to P32, P41 to P47, P50 to P57, P60 to P67, P75 to P77, P106, P107, P126, P127, P140, P150 to P157	Per pin, $V_I > EV_{DD0}$				0.4	mA
			Total of all pins, $V_I > EV_{DD0}$				4	mA
		P70 to P74, P80 to P87, P90 to P97, P100 to P105, P120, P125	Per pin, $V_I > V_{DD} = AV_{DD}$				0.15	mA
			Total of all pins, $V_I > V_{DD} = AV_{DD}$				1	mA
On-chip pull-up resistance	R_U	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P140, P150 to P157	$V_I = EV_{SS0}$, in input port		10	20	100	kΩ

Note Guaranteed by design, but not tested before shipment.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. V_I: Input voltage level to the port pins.

3.3.2 Supply Current Characteristics

(1) RL78/F25 (Grade 3 Products)

(T_A = −40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(1/2)**

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Notes 3, 4		6.8	15.0	mA
					f_{IH} = 40 MHz	f_{CLK} = f_{IH} Notes 3, 4		6.5	13.5	mA
					f_{IH} = 2 MHz	f_{CLK} = f_{IH} Notes 3, 4		1.0	2.3	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		3.7	7.5	mA
					f_{MX} = 2 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.9	2.1	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		6.8	15.0	mA
					f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		6.6	13.5	mA
					f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Notes 3, 6		6.4	13.0	mA
				Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7		12.3	550	µA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8		9.8	550	µA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, 3	I_{DD2}	HALT mode Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Note 5		2.0	10.0	mA
				f_{IH} = 40 MHz	f_{CLK} = f_{IH} Note 5		1.7	8.5	mA
				f_{IH} = 2 MHz	f_{CLK} = f_{IH} Note 5		0.5	1.8	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Note 6		1.0	5.0	mA
				f_{MX} = 2 MHz	f_{CLK} = f_{MX} Note 6		0.3	1.8	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		2.0	10.0	mA
				f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		1.9	8.5	mA
				f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Note 7		1.7	8.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 8		7.1	160	µA
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 9		7.1	160	µA
	I_{DD3}	STOP mode Note 4	T_A = +25°C				0.6		µA
			T_A = +50°C					10.5	
			T_A = +70°C					27	
			T_A = +105°C					125	
	I_{SNOZ}	SNOOZE mode	DTC operation				6.0		mA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, A/D converter, D/A converter, and comparator are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped. When the RAMSDMD bit and RAMSDS bit of the PSMCR register are set to 11B (shutdown mode).

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{WDT} = 15 kHz			0.3		µA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	AV_{DD} = V_{DD} = 5.0 V		1.3	1.6	mA
		When internal reference voltage is selected Note 4			128		µA
Sample-and-hold circuit operating current	I_{ADSH} Note 5				0.8	1.2	mA
LVD operating current	I_{LVD} Note 6				0.045		µA
D/A converter operating current	I_{DAC}				0.4	0.5	mA
Comparator operating current	I_{CMP}				100		µA
BGO operating current	I_{BGO} Note 7				2.5	12.2	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

5. Operating current that increases when the sample-and-hold circuit is used. This current flows for each analog input channel.

6. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

7. Current increased by the BGO operation. The current value is the sum of I_{DD1} and I_{BGO} when the BGO operates in operation mode.

(2) RL78/F25 (Grade 4 Products)

(T_A = −40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V) **(1/2)**

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Notes 3, 4		6.8	15.0	mA
					f_{IH} = 40 MHz	f_{CLK} = f_{IH} Notes 3, 4		6.5	13.5	mA
					f_{IH} = 2 MHz	f_{CLK} = f_{IH} Notes 3, 4		1.0	2.6	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		3.7	7.5	mA
					f_{MX} = 2 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.9	2.4	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		6.8	15.0	mA
					f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		6.6	13.5	mA
					f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Notes 3, 6		6.4	13.0	mA
				Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7		12.3	800	µA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8		9.8	800	µA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit and A/D converter are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, 3	I_{DD2}	HALT mode Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Note 5		2.0	10.0	mA
				f_{IH} = 40 MHz	f_{CLK} = f_{IH} Note 5		1.7	8.5	mA
				f_{IH} = 2 MHz	f_{CLK} = f_{IH} Note 5		0.5	2.0	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Note 6		1.0	5.0	mA
				f_{MX} = 2 MHz	f_{CLK} = f_{MX} Note 6		0.3	2.0	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		2.0	10.0	mA
				f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		1.9	8.5	mA
				f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Note 7		1.7	8.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 8		7.1	330	µA
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 9		7.1	330	µA
	I_{DD3}	STOP mode Note 4	T_A = +25°C				0.6		µA
			T_A = +50°C					10.5	
			T_A = +70°C					27	
			T_A = +105°C					125	
			T_A = +125°C					290	
	I_{SNOZ}	SNOOZE mode	DTC operation				6.0		mA

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, V_{SS}, or EV_{SS0}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, and A/D converter are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped. When the RAMSDMD bit and RAMSDS bit of the PSMCR register are set to 11B (shutdown mode).

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +125°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{WDT} = 15 kHz			0.3		µA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	AV_{DD} = V_{DD} = 5.0 V		1.3	1.6	mA
		When internal reference voltage is selected Note 4			128		µA
Sample-and-hold circuit operating current	I_{ADSH} Note 5				0.8	1.2	mA
LVD operating current	I_{LVD} Note 6				0.045		µA
D/A converter operating current	I_{DAC}				0.4	0.5	mA
Comparator operating current	I_{CMP}				100		µA
BGO operating current	I_{BGO} Note 7				2.5	12.2	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

5. Operating current that increases when the sample-and-hold circuit is used. This current flows for each analog input channel.

6. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

7. Current increased by the BGO operation. The current value is the sum of I_{DD1} and I_{BGO} when the BGO operates in operation mode.

3.4 AC Characteristics

3.4.1 Basic Operation

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	High-speed on-chip oscillator clock operation		0.025		0.5	μs
		High-speed system clock operation		0.05		0.5	μs
		PLL clock operation		0.025		0.5	μs
		Subsystem clock operation		28.5	30.5	34.5	μs
		Low-speed on-chip oscillator clock operation			66.6		μs
		In self programming mode		0.025		0.5	μs
CPU/peripheral hardware clock frequency	f_{CLK}			0.025		66.6	μs
External system clock frequency	f_{EX}			2.0		20.0	MHz
	f_{EXS}			29		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}			$1/f_{MCK}$ + 10			ns
TO00 to TO07, TO10 to TO17, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRJIO0, TRJO0 output frequency	f_{TO}	Normal slew rate, C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		TO01, TO06, TO07, TO11, TO13, TRDIOC0, TRDIOD0, TRDIOD1, TRJO0 only, Special slew rate, C = 30 pF				2	MHz
PCLBUZ0 output frequency	f_{PCL}	Normal slew rate, C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
		Special slew rate, C = 30 pF				2	MHz
Timer RJ input cycle	t_C	TRJIO0		100			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0		40			ns
Timer RDe input high-level, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRDCLK0, TRD0RES, TRD1RES		$3/f_{TRD}$			ns
Timer RDe pulse output forced cutoff signal low-level width	t_{TDSIL}	P137/INTP0	2 MHz < f_{CLK} ≤ 40 MHz	1			μs
			f_{CLK} ≤ 2 MHz	$1/f_{CLK}$ + 1			μs

Caution Excluding the error in oscillation frequency accuracy.

Remark f_{MCK}: Timer array unit operation clock frequency
f_{TRD}: Timer RDe operation clock frequency

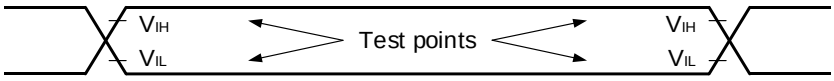
($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP13 Note 1		1			µs
KR0 to KR7 key interrupt input low-level width	t_{KR}			250			ns
RESET low-level width	t_{RSL}	Note 1		10			µs
Port output rise time, port output fall time	t_{RO}, t_{FO}	P00 to P03, P10 to P17, P30 to P32, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P106, P107, P120, P125 to P127, P130, P140, P150 to P157 (normal slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V			25	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			55	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) C = 30 pF	4.0 V ≤ EV_{DD0} ≤ 5.5 V		25 Note 2	60	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			100	ns

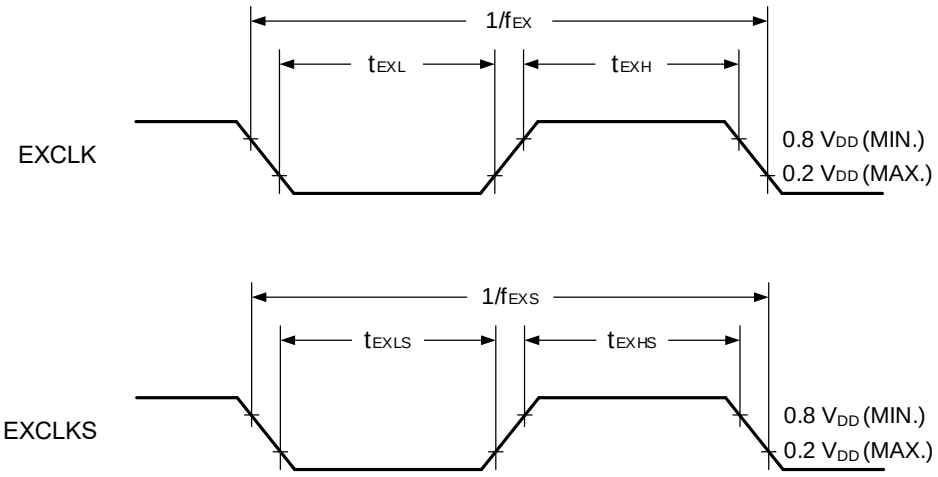
Notes 1. Pins RESET, INTP0 to INTP3, INTP12, and INTP13 have noise filters for transient levels lasting less than 100 ns.

2. T_A = +25°C, E_{VDD0} = 5.0 V

AC Timing Test Points

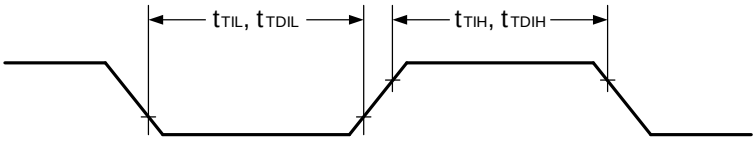


External System Clock Timing

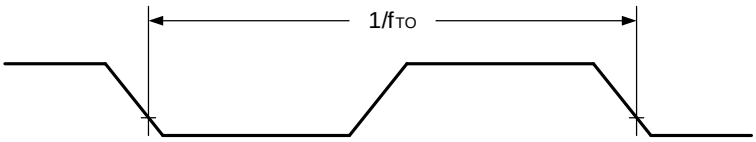


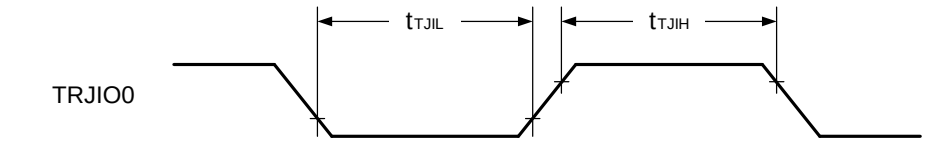
TI/TO Timing

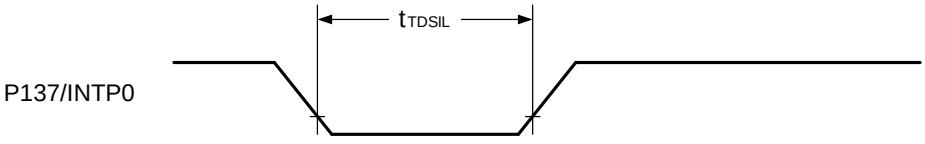
TI00 to TI07, TI10 to TI17, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRDCLK0, TRD0RES, TRD1RES



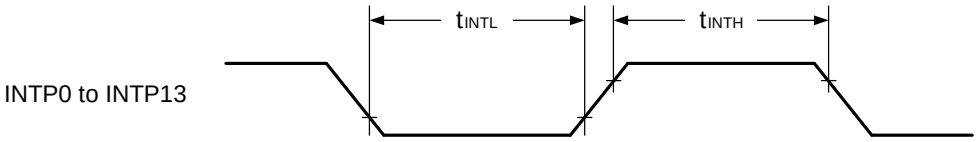
TO00 to TO07, TO10 to TO17, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRJIO0, TRJO0



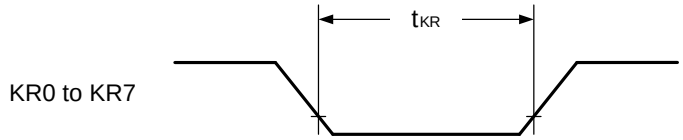




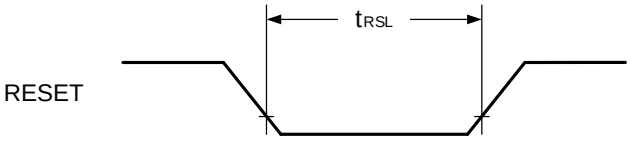
Interrupt Request Input Timing



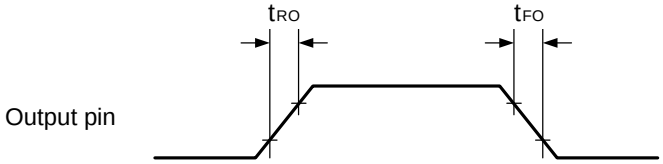
Key Interrupt Input Timing



RESET Input Timing



Output Rising and Falling Timing



3.5 Peripheral Functions Characteristics

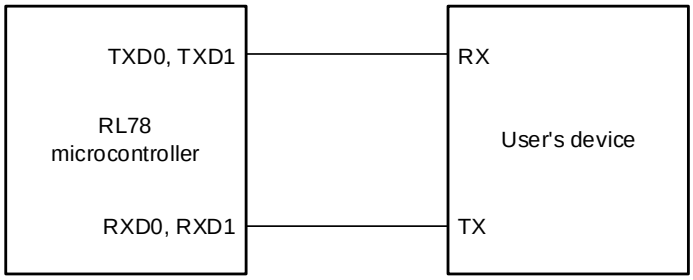
3.5.1 Serial Array Unit

(1) During Communication at Same Potential (UART mode) (Dedicated Baud Rate Generator Output)

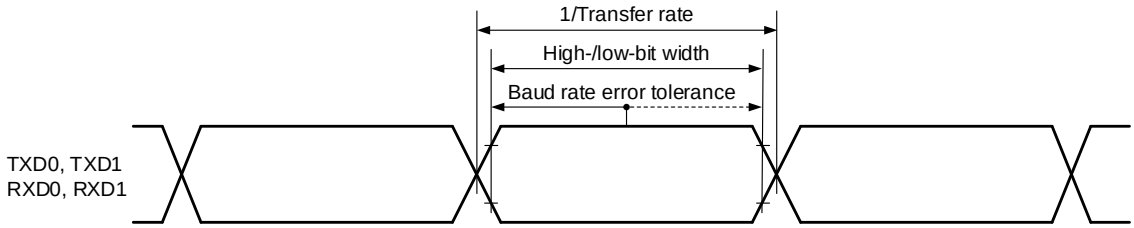
($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	–					f_{MCK}/6	bps
		f_{CLK} = 40 MHz, $f_{MCK} = f_{CLK}$	Normal slew rate			6.6	Mbps
			Special slew rate			2	Mbps

UART Mode Connection Diagram (During Communication at Same Potential)



UART Mode Bit Width (During Communication at Same Potential) (Reference)



Caution Select normal input buffer for the RXD0 and RXD1 pins, and select normal output mode for the TXD0 and TXD1 pins.

Remark f_{MCK}: Serial array unit operation clock frequency

(2) During Communication at Same Potential (CSI mode) (Master Mode, SCKp … Internal Clock Output, Normal Slew Rate)

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	Grade 3 products		100 Note 5			ns
		Grade 4 products		150 Note 5			ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 − 12			ns
		2.7 V ≤ EV_{DD0} < 4.0 V		t_{KCY1}/2 − 18			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	Grade 3 products	4.0 V ≤ EV_{DD0} ≤ 5.5 V	33			ns
			2.7 V ≤ EV_{DD0} < 4.0 V	44			ns
		Grade 4 products	4.0 V ≤ EV_{DD0} ≤ 5.5 V	44			ns
			2.7 V ≤ EV_{DD0} < 4.0 V	55			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			30			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4				30	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

5. $t_{KCY1} \geq 4/f_{MCK}$ must also be satisfied.

Caution Select normal input buffer for the SIp pin, and select normal output mode for the SOp and SCKp pins.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(3) During Communication at Same Potential (CSI mode) (Master Mode, SCKp … Internal Clock Output, Special Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}		500 Note 5			ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 − 60			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}		120			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		80			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			90	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

5. $t_{KCY1} \geq 4/f_{MCK}$ must also be satisfied.

Caution Select normal input buffer for the SIp pin, and select normal output mode and special slew rate for the SOp and SCKp pins.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(4) During Communication at Same Potential (CSI mode) (Slave Mode, SCKp … External Clock Input, Normal Slew Rate)

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	f_{MCK} > 32 MHz		10/f_{MCK}			ns
		f_{MCK} ≤ 32 MHz		8/f_{MCK}			ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}			1/f_{MCK} + 20			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	4.0 V ≤ EV_{DD0} ≤ 5.5 V			2/f_{MCK} + 44	ns
			2.7 V ≤ EV_{DD0} < 4.0 V			2/f_{MCK} + 57	ns
SSIp setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
SSIp hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select normal input buffer for the SIp, SCKp and SSIp pins, and select normal output mode for the SOp pin.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

(5) During Communication at Same Potential (CSI mode) (Slave Mode, SCKp … External Clock Input, Special Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	20 MHz < f_{MCK}	10/f_{MCK}			ns
		10 MHz < f_{MCK} ≤ 20 MHz	8/f_{MCK}			ns
		f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2			ns
SIp setup time (to SCKp↑) Note1	t_{SIK2}		1/f_{MCK} + 50			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}		1/f_{MCK} + 50			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4			2/f_{MCK} + 80	ns
SSIp setup time	t_{SSIK}	DAP = 0	120			ns
		DAP = 1	1/f_{MCK} + 120			ns
SSIp hold time	t_{KSSI}	DAP = 0	1/f_{MCK} + 120			ns
		DAP = 1	120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

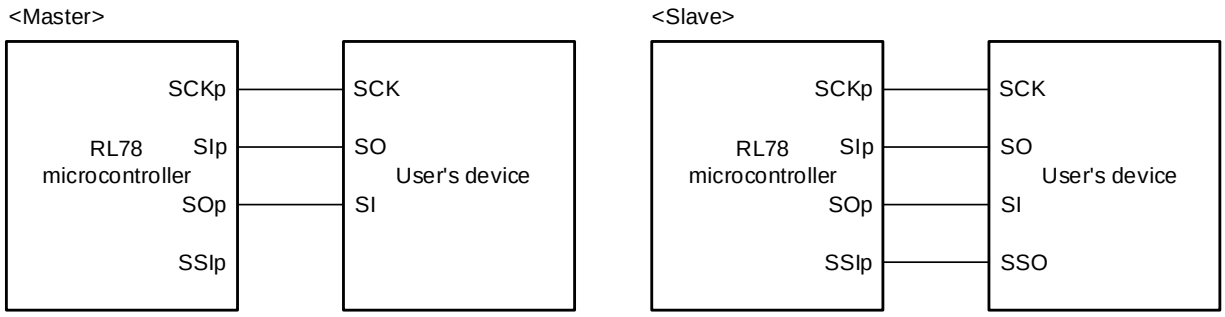
4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select normal input buffer for the SIp, SCKp and SSIp pins, and select normal output mode and special slew rate for the SOp pin.

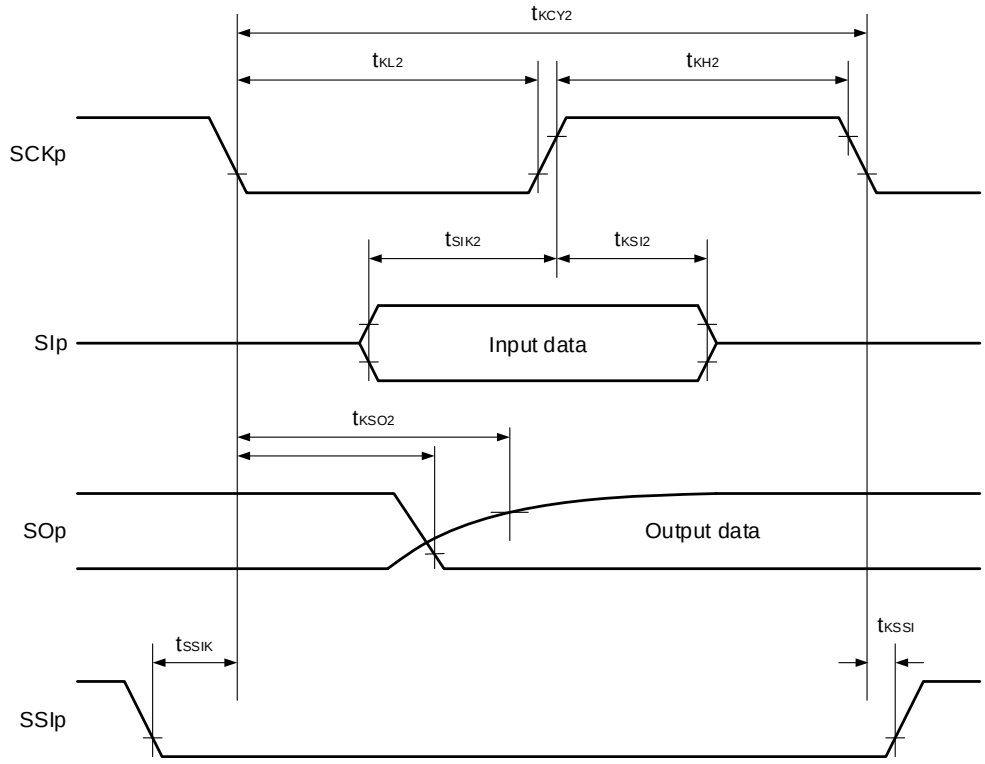
Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

CSI Mode Connection Diagram (During Communication at Same Potential)

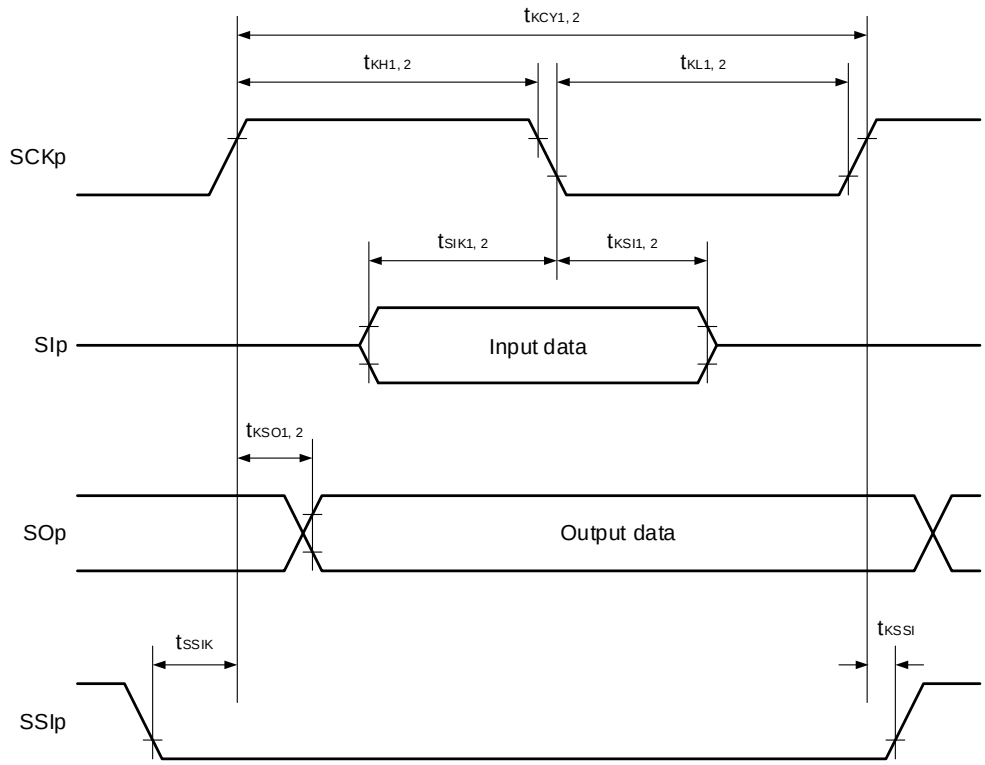


CSI Mode Serial Transfer Timing (During Communication at Same Potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

CSI Mode Serial Transfer Timing (During Communication at Same Potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

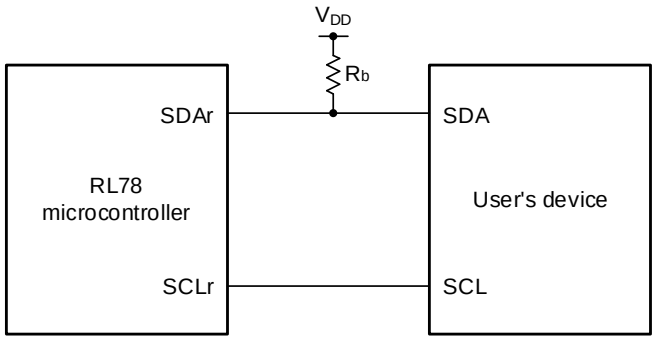
(6) During Communication at Same Potential (Simplified I^2C Mode) (SDAr: N-ch Open-drain Output (EV_{DD} Tolerance) Mode, SCLr: Normal Output Mode)

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

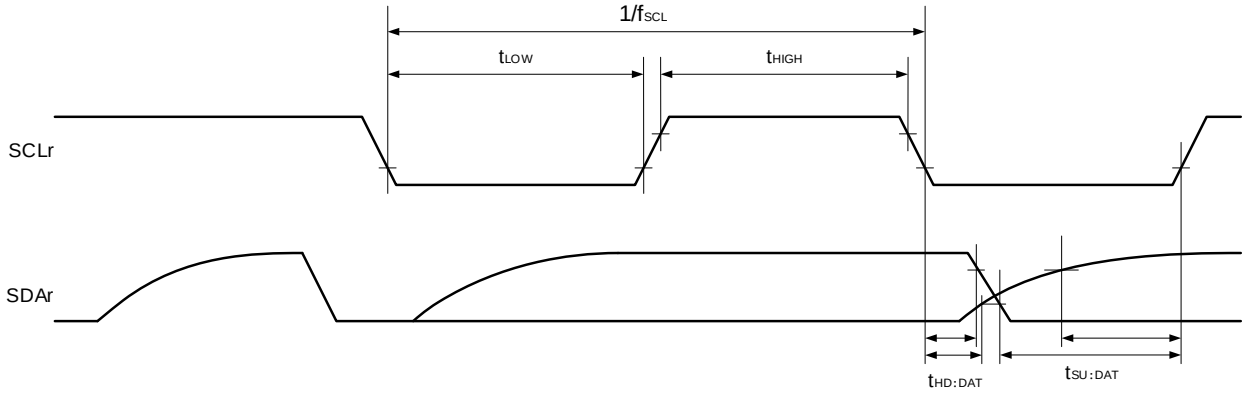
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f_{SCL}				1000 Note	kHz
Hold time when SCLr = "L"	t_{LOW}		475			ns
Hold time when SCLr = "H"	t_{HIGH}		475			ns
Data setup time (reception)	$t_{SU:DAT}$		1/f_{MCK} + 85			ns
Data hold time (transmission)	$t_{HD:DAT}$	C_b = 50 pF, R_b = 2.7 kΩ	0		305	ns

Note $f_{SCL} \leq f_{MCK}/4$ must also be satisfied.

Simplified I^2C Mode Connection Diagram (During Communication at Same Potential)



Simplified I^2C Mode Serial Transfer Timing (During Communication at Same Potential)



Caution Select normal input buffer and N-ch open-drain output mode for the SDAr pin, and select normal output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance,
C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

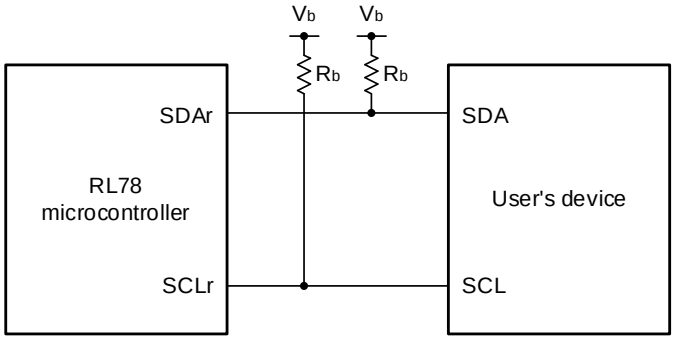
(7) During Communication at Same Potential (Simplified I^2C Mode) (SDAr and SCLr: N-ch Open-drain Output (EV_{DD} Tolerance) Mode)

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}			400 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1300		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	600		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1/f_{MCK} + 120		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 270		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	0	300	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			

Note $f_{SCL} \le f_{MCK}/4$ must also be satisfied.

Simplified I^2C Mode Connection Diagram (During Communication at Same Potential)



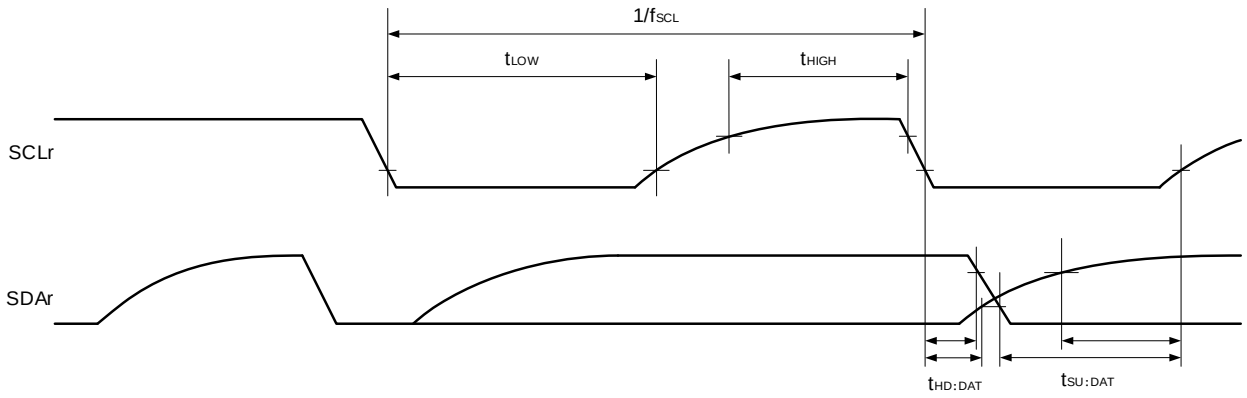
Caution Select normal input buffer and N-ch open-drain output mode for the SDAr and SCLr pins.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance,
C_b [F]: Communication line (SDAr, SCLr) load capacitance,
V_b [V]: Communication line voltage

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

Simplified I²C Mode Serial Transfer Timing (During Communication at Same Potential)



Remark r: IICr (r = 00, 01, 10, 11)

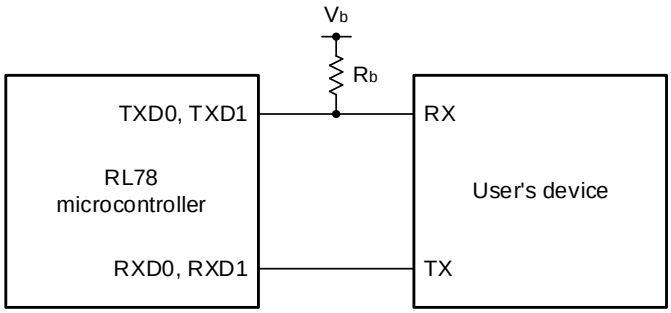
(8) Communication at Different Potential (UART mode) (TXD Output Buffer: N-ch Open-drain, RXD Input Buffer: TTL)

($T_A = T_{OPR}$, 4.0 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

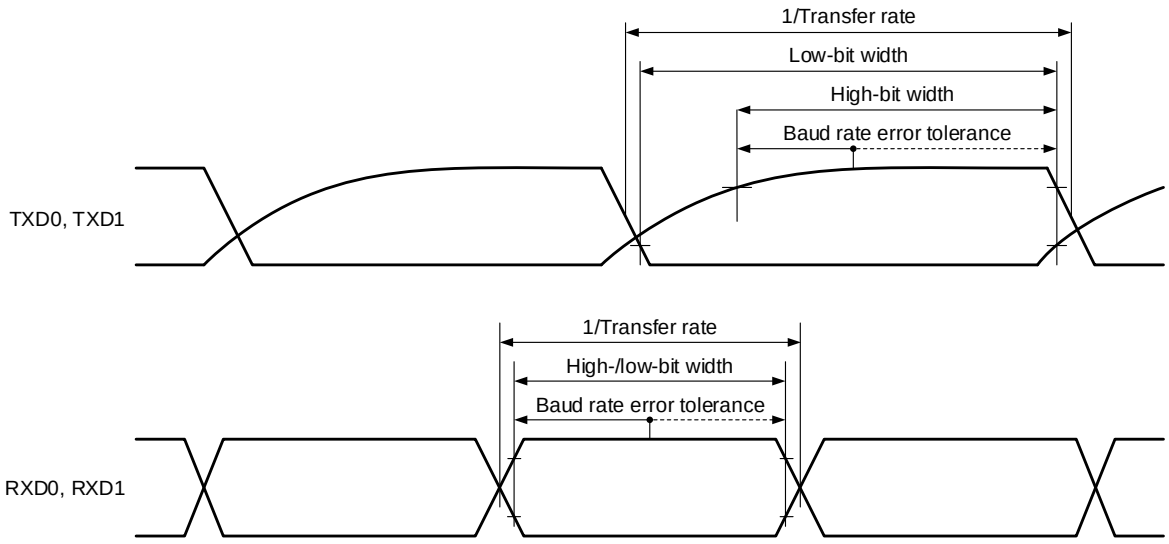
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Transfer rate	–	Reception	2.7 V ≤ V_b ≤ EV_{DD0}, V_{IH} = 2.2 V, V_{IL} = 0.8 V					f_{MCK}/6	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF)	Grade 3 products			5.3	Mbps
					Grade 4 products			4.0	
		Transmission	2.7 V ≤ V_b ≤ EV_{DD0}, V_{OH} = 2.2 V, V_{OL} = 0.8 V					Smaller number of the values given by f_{MCK}/6 and (Expression 1) is applicable.	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF) Normal slew rate	Grade 3 products			5.3	Mbps
					Grade 4 products			4.0	

Note (Expression 1): maximum transfer rate = $1 / [\{ -C_b \times R_b \times \ln(1 - 2.2 / V_b) \} \times 3]$

UART Mode Connection Diagram (During Communication at Different Potential)



UART Mode Bit Width (During Communication at Different Potential) (Reference)



Caution Select TTL input buffer for the RXD0 and RXD1 pins, and select N-ch open-drain output mode for the TXD0 and TXD1 pins.

Remarks 1. R_b [Ω]: Communication line (TXD) pull-up resistance,
C_b [F]: Communication line (TXD) load capacitance,
V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

(9) During Communication at Different Potential (3 V Supply System) (CSI Mode) (Master Mode, SCKp … Internal Clock Output, Normal Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

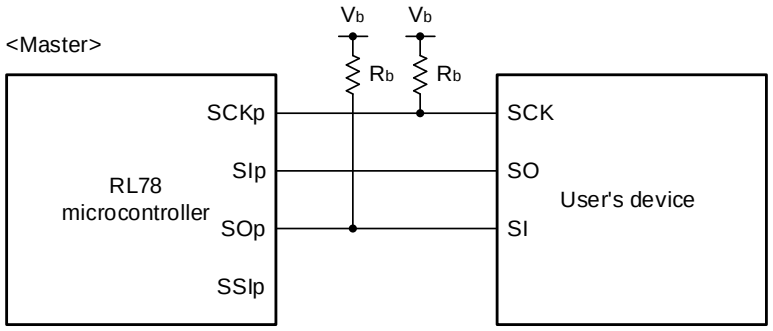
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	400 Note3			ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 − 75			ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 − 20			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
Delay time from SCKp↓ to SOp output Note1	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
Delay time from SCKp↑ to SOp output Note2	t_{KSO1}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. $t_{KCY1} \geq 4/f_{MCK}$ must also be satisfied.

CSI Mode Connection Diagram (During Communication at Different Potential)



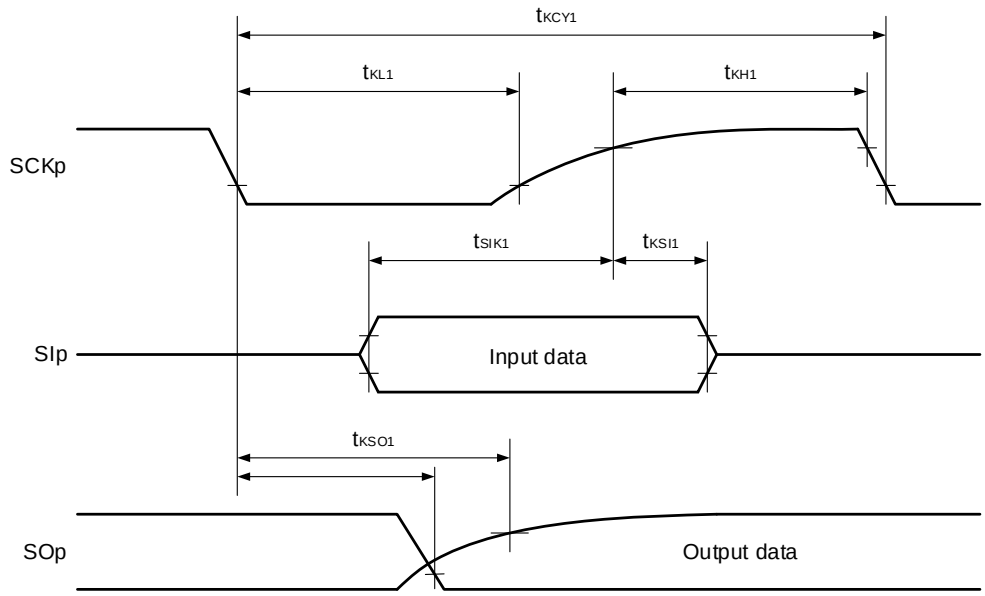
Caution Select TTL input buffer for the SIp pin, and select N-ch open-drain output mode for the SOp and SCKp pins.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance,
C_b [F]: Communication line (SOp, SCKp) load capacitance,
V_b [V]: Communication line voltage

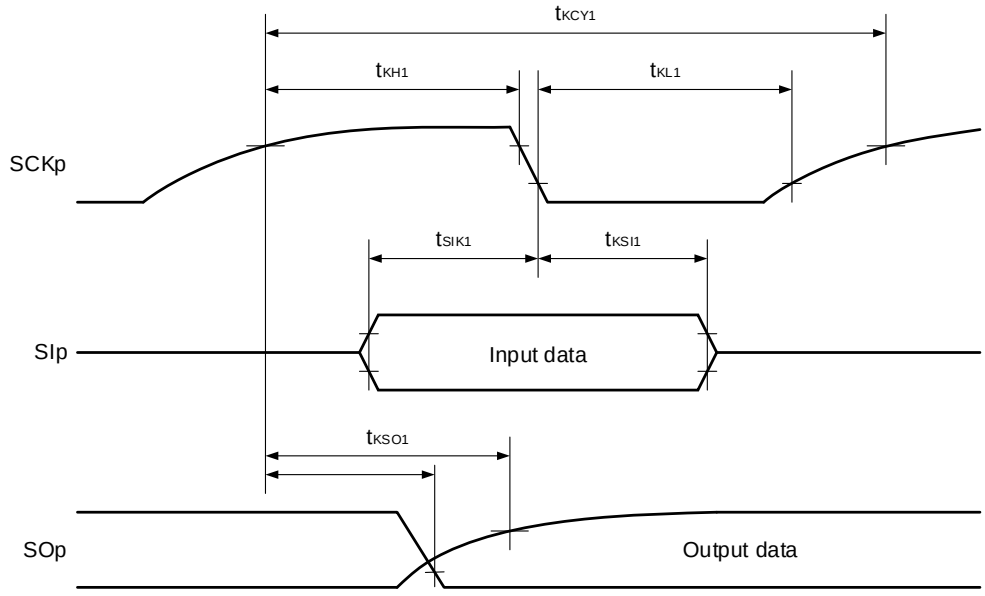
2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

CSI Mode Serial Transfer Timing (Master Mode) (During Communication at Different Potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI Mode Serial Transfer Timing (Master Mode) (During Communication at Different Potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(10) During Communication at Different Potential (3 V Supply System) (CSI Mode) (Slave Mode, SCKp … External Clock Input, Normal Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

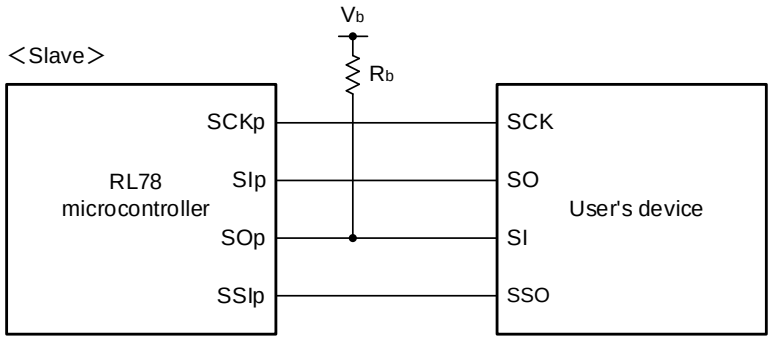
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_b ≤ EV_{DD0}	32 MHz < f_{MCK}				
			Grade 3 products	18/f_{MCK}			ns
			Grade 4 products	20/f_{MCK}			ns
			24 MHz < f_{MCK} ≤ 32 MHz				
			Grade 3 products	14/f_{MCK}			ns
			Grade 4 products	16/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz				
			Grade 3 products	12/f_{MCK}			ns
			Grade 4 products	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz				
			Grade 3 products	10/f_{MCK}			ns
			Grade 4 products	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz				
			Grade 3 products	8/f_{MCK}			ns
			Grade 4 products	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz				
			Grade 3 products	6/f_{MCK}			ns
			Grade 4 products	6/f_{MCK}			ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_b ≤ EV_{DD0}		t_{KCY2}/2 − 20			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}			90			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	2.7 V ≤ V_b ≤ EV_{DD0}, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
SSIp setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
SSIp hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI Mode Connection Diagram (During Communication at Different Potential)



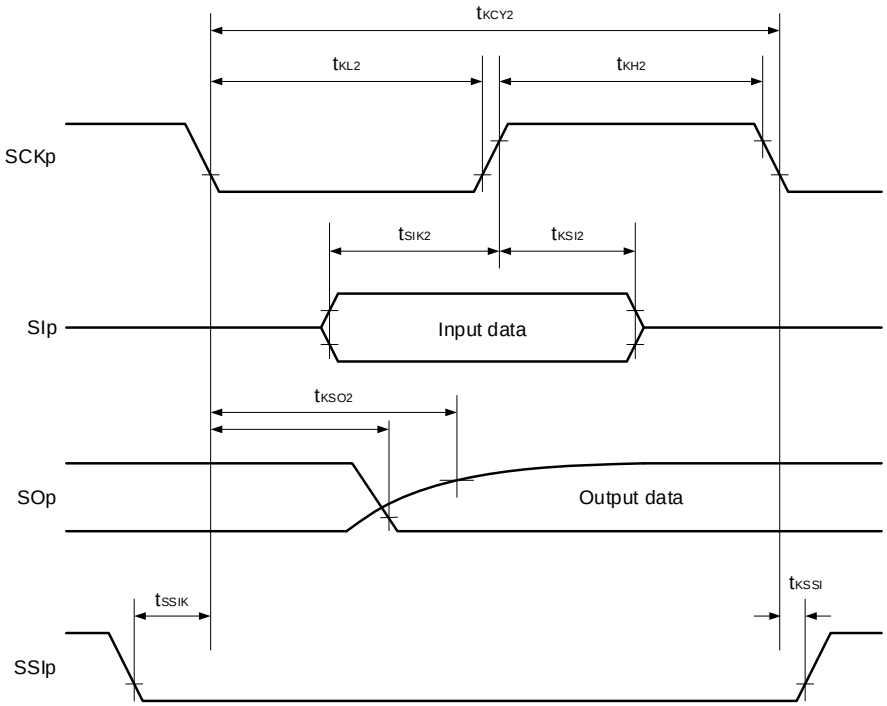
Caution Select TTL input buffer for the SIp, SCKp and SSIp pins, and select N-ch open-drain output mode for the SOp pin.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance,
C_b [F]: Communication line (SOp) load capacitance,
V_b [V]: Communication line voltage

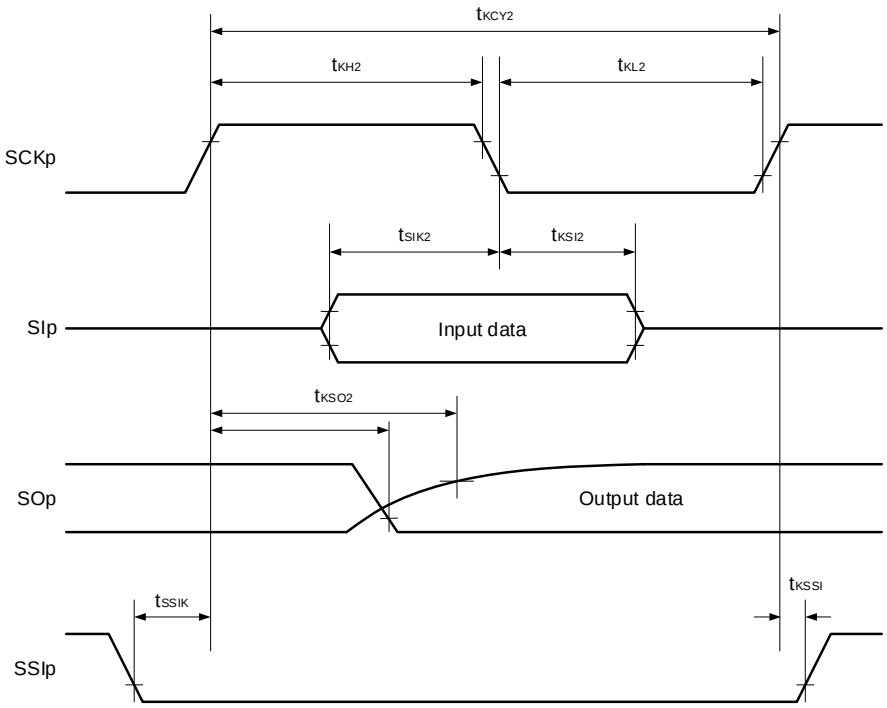
2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

CSI Mode Serial Transfer Timing (Slave Mode) (During Communication at Different Potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI Mode Serial Transfer Timing (Slave Mode) (During Communication at Different Potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

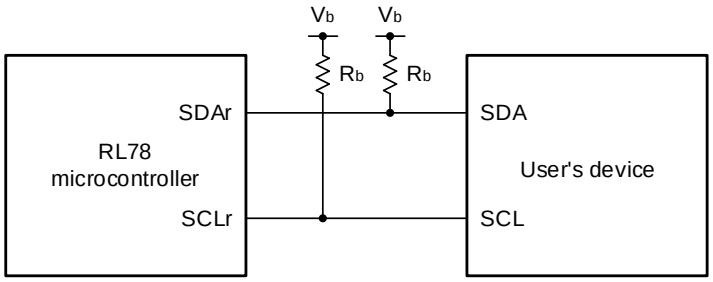
(11) During Communication at Different Potential (3 V Supply System) (Simplified I^2C Mode) (SDAr: TTL Input Buffer Mode and N-ch Open-drain Output (EV_{DD} tolerance) Mode, SCLr: N-ch Open-drain Output (EV_{DD} Tolerance) Mode)

($T_A = T_{OPR}$, 4.0 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

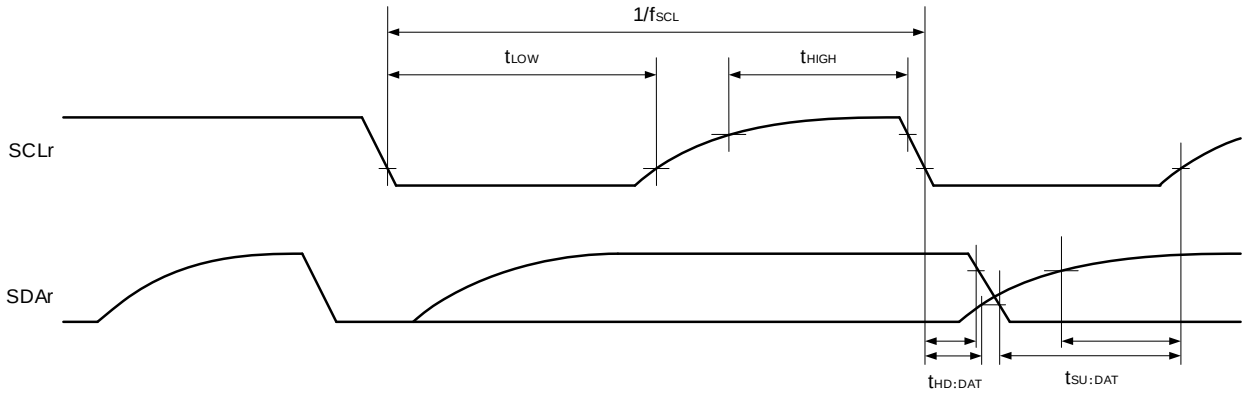
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	135 + 1/f_{MCK}		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	140	ns

Note $f_{SCL} \le f_{MCK}/4$ must also be satisfied.

Simplified I^2C Mode Connection Diagram (During Communication at Different Potential)



Simplified I^2C Mode Serial Transfer Timing (During Communication at Different Potential)



Caution Select TTL input buffer and N-ch open-drain output mode for the SDAr pin, and select N-ch open-drain output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance,
C_b [F]: Communication line (SDAr, SCLr) load capacitance,
V_b [V]: Communication line voltage

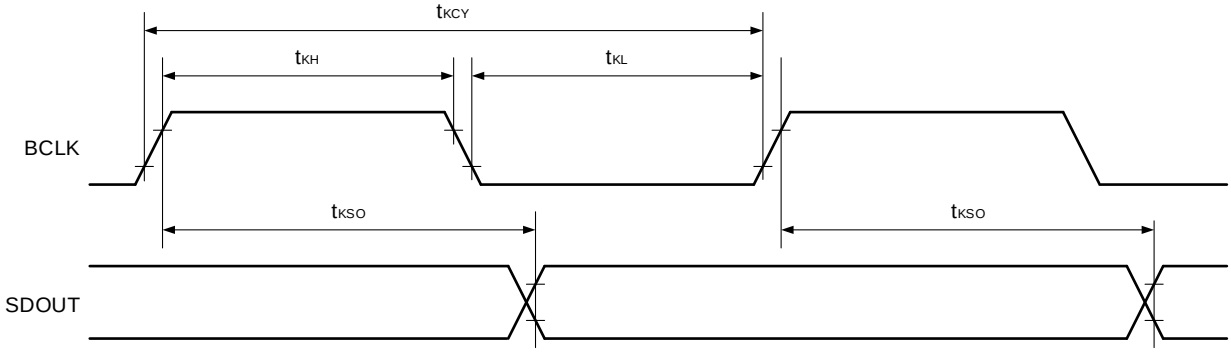
2. f_{MCK}: Serial array unit operation clock frequency

(12) During Communication at Same Potential (Simplified I²S Master Transmission) (CSI Mode, Slave Transmission Mode)

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions Note	MIN.	TYP.	MAX.	Unit
BCLK cycle time	t_{KCY}	Data rate = 2.5 MHz		400		ns
BCLK high-level width, low-level width	t_{KH}, t_{KL}		Value greater than 0.35 t_{KCY}			ns
SDOUT output delay time	t_{KSO}				Value less than 0.80 t_{KCY}	ns

Note The CPU/peripheral hardware clock frequency (f_{CLK}) must satisfy the condition of 8 MHz to 40 MHz.



Caution Set the I2SEN bit in the I2SER register to 1 (enable simple I2S communication function) and the TO121 and TO120 bits in the PWMDLY2 register to 01B (TO12 output is delayed by one cycle of f_{CLK}).

Remarks 1. BCLK: TO12 output of timer array unit 1, channel 2
SDOUT: SO10 output of serial array unit 1, channel 0
LRCLK: TO13 output of timer array unit 1, channel 3

2. Serial array unit 1, channel 0: CSI mode, slave transmission mode
Timer array unit 1, channel 2: Interval timer mode
Timer array unit 1, channel 3: External event counter mode

3.5.2 Serial Interface IICA

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: 10 MHz ≤ f_{MCK}					0	1000	kHz
		Fast mode: 3.5 MHz ≤ f_{MCK}			0	400			kHz
		Normal mode: 1 MHz ≤ f_{MCK}	0	100					kHz
Setup time of restart condition Note 1	$t_{SU:STA}$		4.7		0.6		0.26		µs
Hold time	$t_{HD:STA}$		4.0		0.6		0.26		µs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		0.5		µs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		0.26		µs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	0	0.9	0		µs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		µs
Bus-free time	t_{BUF}		4.7		1.3		0.5		µs

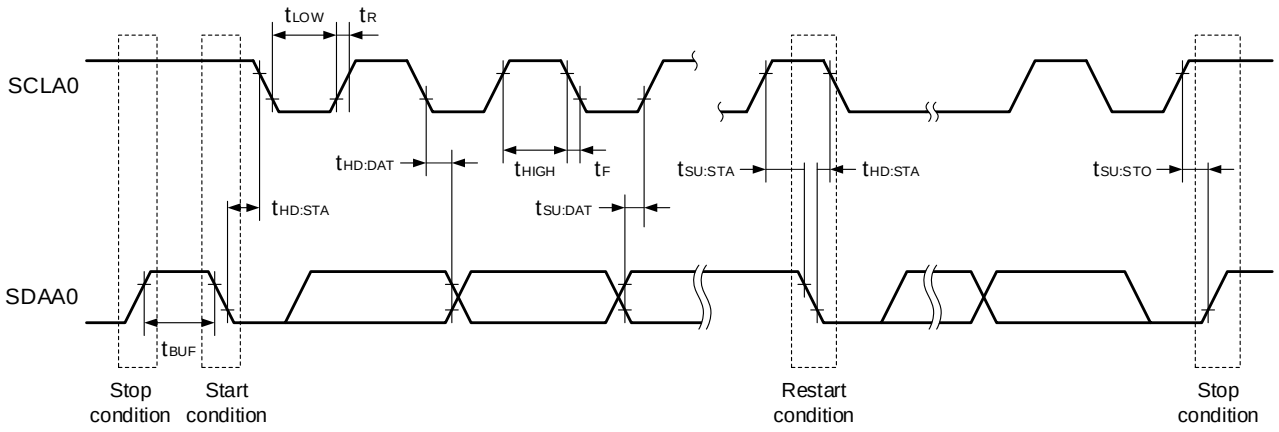
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA Serial Transfer Timing



3.5.3 On-chip Debug (UART)

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	–		115.2 k		1 M	bps

3.5.4 LIN/UART Module (RLIN3) UART Mode

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	–	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 MHz to 40 MHz			4000	kbps
		SNOOZE mode	LIN communication clock source (f_{CLK}): 2 MHz to 40 MHz			9.6	

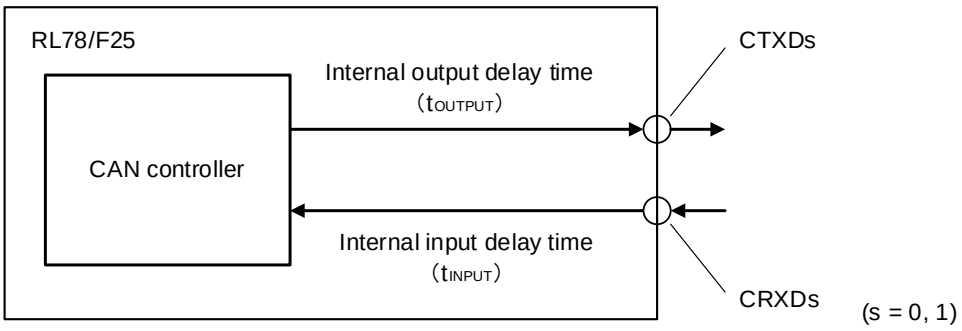
3.5.5 CAN-FD Communication Interface (RS-CANFD lite) Timing

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	–	Classical CAN mode				1	Mbps
		CAN-FD mode	Data bit rate			5	Mbps
		CAN-FD mode	Nominal bit rate			1	Mbps
Internal delay time Note	t_{NODE}					50	ns

Note t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})

Image of Internal Delay



3.6 Analog Characteristics

3.6.1 A/D Converter Characteristics

- When Reference voltage (+) = AV_{REFP}, Reference voltage (−) = AV_{REFM} = 0 V.
- Target ANI pin: ANI0 to ANI28, Internal reference voltage (+).
- Conversion mode: High-speed conversion mode

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V, Reference Voltage (+) = AV_{REFP}, Reference Voltage (−) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				12	bit
Overall error Note 1	ABS	ANI0 to ANI21 Note 2, [4.5 V ≤ AV_{REFP}/AV_{DD} ≤ 5.5 V]			±5.0	LSB
		ANI0 to ANI21 Note 2, [2.7 V ≤ AV_{REFP}/AV_{DD} < 4.5 V]			±5.0	LSB
		ANI1, ANI2 Note 3, [4.5 V ≤ AV_{REFP}/AV_{DD} ≤ 5.5 V] [0.25 V ≤ V_{AIN} ≤ AV_{DD} − 0.25 V]			±6.0	LSB
		ANI1, ANI2 Note 3, [2.7 V ≤ AV_{REFP}/AV_{DD} < 4.5 V] [0.25 V ≤ V_{AIN} ≤ AV_{DD} − 0.25 V]			±8.0	LSB
		ANI22 to ANI28, [4.5 V ≤ AV_{REFP}/AV_{DD} ≤ 5.5 V]			±11	LSB
		ANI22 to ANI28, [2.7 V ≤ AV_{REFP}/AV_{DD} < 4.5 V]			±13	LSB
Integral linearity error Note 1	INL	ANI0 to ANI21			±3.0	LSB
		ANI22 to ANI28			±7.0	LSB
Differential linearity error Note 1	DNL	ANI0 to ANI21			±1.5	LSB
		ANI22 to ANI28			±3.5	LSB
Zero-scale error Note 1	ZSE	ANI0 to ANI21 Note 2			±4.5	LSB
		ANI22 to ANI28			±8.5	LSB
Full-scale error Note 1	FSE	ANI0 to ANI21 Note 2			±4.5	LSB
		ANI22 to ANI28			±8.5	LSB
Reference voltage (+)	AV_{REFP}		2.7		V_{DD}	V
Analog input voltage	V_{AIN}	ANI0 to ANI28	0		AV_{REFP}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V	1.42	1.48	1.54	V
Analog input slew rate	SR				0.4	V/µs
Operation clock	f_{AD}		2		40	MHz
Conversion time Note 4 (per 1 channel)	t_{CONV}	ADCLK = 40 MHz, input impedance ≤ 0.5 kΩ				
		ANI0 to ANI15 Note 2	1.125			µs
		ANI16 to ANI28	1.8			µs
		ANI1, ANI2 Note 3	1.85			µs

Notes 1. Excludes quantization error (±1/2 LSB).

2. In case that dedicated sample & hold circuit is not used.

3. In case that dedicated sample & hold circuit is used.

4. The A/D conversion processing time (t_{CONV}) consists of sampling time and time for conversion by successive approximation.

3.6.2 D/A Converter Characteristics

($T_A = T_{OPR}$, $2.7\ V \le EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} \le 5.5\ V$, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	2.7 V ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	2.7 V ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ AV_{DD} ≤ 5.5 V			3	µs

3.6.3 Comparator Characteristics

($T_A = T_{OPR}$, $2.7\ V \le EV_{DD0} = EV_{DD1} = AV_{DD} = V_{DD} \le 5.5\ V$, $V_{SS} = AV_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±40	mV
Input voltage range	V_{IVCMP}	IVCMP00 to IVCMP03	0		AV_{DD}	V
	V_{IVREF}	IVREF0	0		AV_{DD}	V
Input voltage slope Note 4	S_{IVCMP}	IVCMP00 to IVCMP03			±3	V/µs
Response time	t_{CR}, t_{CF}	Input amplitude ±100 mV		50	100	ns
Stabilization wait time during input channel switching Note 1	t_{WAIT}	Input amplitude ±100 mV	300			ns
Operation stabilization wait time Note 2, 3	t_{CMP}	2.7 V ≤ AV_{DD} ≤ 5.5 V	1			µs

Notes 1. Period of time from when the comparator input channel is switched until the comparator is switched to output.

2. Period of time from when the comparator operation is enabled (HCMPON bit in CMPCTL is set to 1) until the comparator satisfies the DC/AC characteristics.

3. When the D/A converter output is selected as the reference voltage, this is the time it takes for the comparator to satisfy the DC/AC characteristics after the D/A converter output value is changed.

4. Input voltage slope without noise filter.

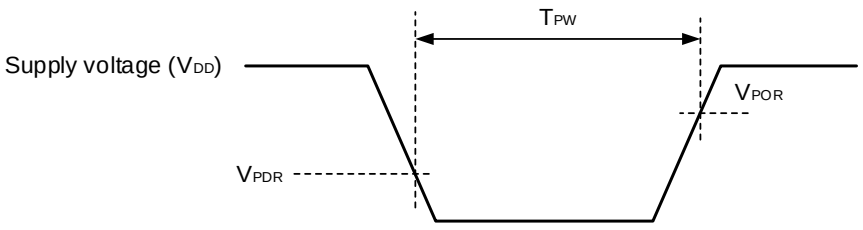
3.6.4 POR Circuit Characteristics

($T_A = T_{OPR}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage Note 1	V_{POR}, V_{PDR}		1.43	1.50	1.57	V
Minimum pulse width Note 2	T_{PW}		300			µs
Detection delay time	T_{PD}				350	µs

Notes 1. This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (2.7 V).

2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}.



3.6.5 LVD Circuit Characteristics

(1) LVD0 Detection Voltage of Reset Mode

($T_A = T_{OPR}$, $V_{PDR} \le EV_{DD0} = EV_{DD1} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD00}	Power supply rise time	3.84	3.96	4.08	V
			Power supply fall time	3.76	3.88	4.00	V
		V_{LVD01}	Power supply rise time	2.88	2.97	3.06	V
			Power supply fall time	2.82	2.91	3.00	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time		t_{LD}				500	µs

(2) LVD1 Detection Voltage of Interrupt and Reset Mode

($T_A = T_{OPR}$, $V_{PDR} \le EV_{DD0} = EV_{DD1} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD10}	Power supply rise time	4.08	4.16	4.24	V
			Power supply fall time	4.00	4.08	4.16	V
		V_{LVD11}	Power supply rise time	3.88	3.96	4.04	V
			Power supply fall time	3.80	3.88	3.96	V
		V_{LVD12}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD13}	Power supply rise time	3.48	3.55	3.62	V
			Power supply fall time	3.40	3.47	3.54	V
		V_{LVD14}	Power supply rise time	3.28	3.35	3.42	V
			Power supply fall time	3.20	3.27	3.34	V
		V_{LVD15}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD16}	Power supply rise time	2.91	2.97	3.03	V
			Power supply fall time	2.85	2.91	2.97	V
		V_{LVD17}	Power supply rise time	2.76	2.82	2.87	V
			Power supply fall time	2.70	2.76	2.81	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time		t_{LD}				500	µs

3.7 Power Supply Voltage Rising Time

($T_A = T_{OPR}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope Note 1	S_{vrmax}	0 V → V_{DD} (LVD0ENB = 0 or 1 Note 2)			50 Note 3	V/ms

Notes 1. Maintain the reset state by the voltage detection circuit (LVD0) or external reset up to the operating voltage range.

2. These values indicate setting values of option bytes.

3. If the power supply drops below V_{PDR} and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to 0 V.

3.8 Regulator Output Voltage Characteristics

($T_A = T_{OPR}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

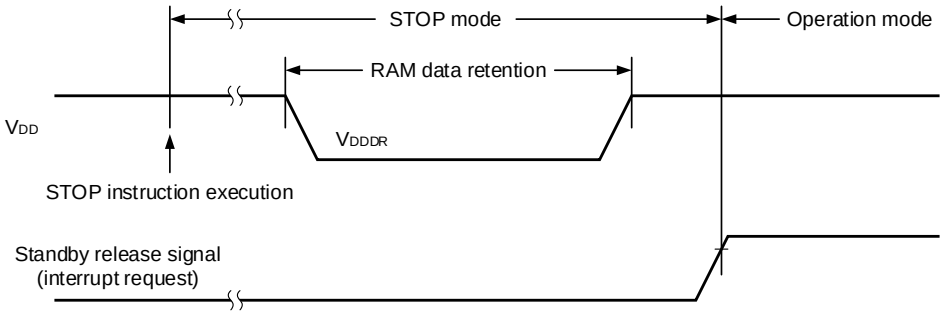
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
REGC output voltage	V_{OREGC}	C = 0.47 to 1 µF	1.45	1.50	1.56	V

3.9 RAM Data Retention Characteristics

($T_A = T_{OPR}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.10 Flash Memory Programming Characteristics

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		2		40	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years, T_A = +85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 20 years, T_A = +85°C Note 4	10,000			
		Retained for 5 years, T_A = +85°C Note 4	100,000			
Erase time	Terasa	Block erase	5			ms
Write time	Twrwa	1 word write	10			µs

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.

2. When using flash memory programmer and Renesas Electronics self programming code.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The average temperature for data retention.

(1) Code Flash Memory Processing Time

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Item		f_{CLK} = 2 MHz		f_{CLK} = 4 MHz		f_{CLK} = 8 MHz		f_{CLK} = 16 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	4 bytes	52.0	470.0	43.0	400.0	38.0	360.0	36.0	340.0	µs
Erasure time	2 KB	7.8	265.0	6.5	240.0	5.9	225.0	5.8	220.0	ms
Blank checking time	4 bytes	–	19.2	–	13.2	–	10.3	–	9.1	µs
	2 KB	–	1310.0	–	660.0	–	335.0	–	270.0	µs

Item		f_{CLK} = 20 MHz		f_{CLK} = 32 MHz		f_{CLK} = 40 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	4 bytes	36.0	340.0	35.0	330.0	35.0	330.0	µs
Erasure time	2 KB	5.8	220.0	5.7	220.0	5.7	220.0	ms
Blank checking time	4 bytes	–	8.9	–	8.5	–	8.5	µs
	2 KB	–	270.0	–	245.0	–	245.0	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

(2) Data Flash Memory Processing Time

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Item		f_{CLK} = 2 MHz		f_{CLK} = 4 MHz		f_{CLK} = 8 MHz		f_{CLK} = 16 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	1 byte	52.0	470.0	43.0	400.0	38.0	360.0	36.0	340.0	µs
Erasure time	1 KB	10.4	320.0	7.8	265.0	6.5	240.0	6.3	235.0	ms
Blank checking time	1 byte	–	19.2	–	13.2	–	10.3	–	9.1	µs
	1 KB	–	2605.0	–	1305.0	–	660.0	–	530.0	µs

Item		f_{CLK} = 20 MHz		f_{CLK} = 32 MHz		f_{CLK} = 40 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	1 byte	36.0	340.0	35.0	330.0	35.0	330.0	µs
Erasure time	1 KB	6.3	235.0	6.2	230.0	6.2	230.0	ms
Blank checking time	1 byte	–	8.9	–	8.5	–	8.5	µs
	1 KB	–	530.0	–	475.0	–	475.0	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

3.11 Dedicated Flash Memory Programmer Communication (UART)

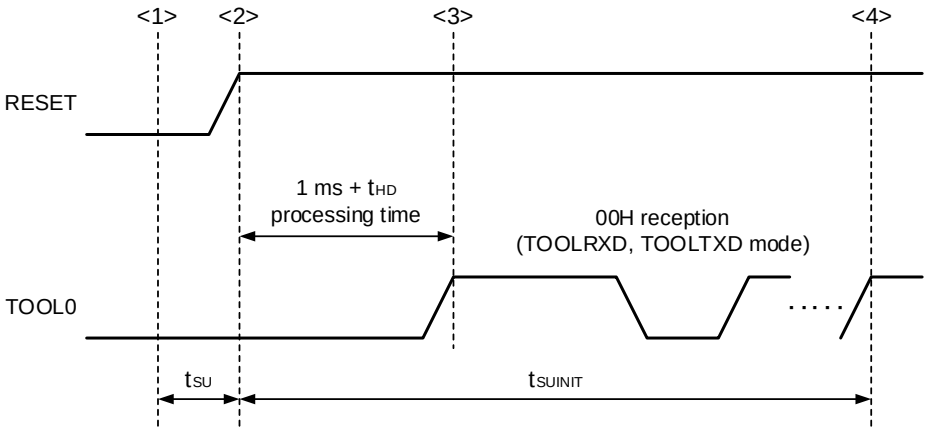
($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	–	During serial programming	115.2 k		1 M	bps

3.12 Timing of Entry to Flash Memory Programming Modes

($T_A = T_{OPR}$, 2.7 V ≤ $EV_{DD0} = EV_{DD1} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

4. ELECTRICAL SPECIFICATIONS (RL78/F22)

Cautions 1. RL78/F22 has an on-chip debug function for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depending on the product. For details, refer to "1.5 Pin Configurations" and "2.1 Pin Function List".

3. The power supply voltage condition of 1.8 V ≤ AV_{DD} = V_{DD} < 2.7 V in each item applies to RL78/F22 Grade 3 products. In that case, the maximum operating clock (f_{CLK}) is 16 MHz.

4.1 Absolute Maximum Ratings

(1/3)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	V_{DD} = AV_{DD}	−0.5 to +6.5	V
	V_{SS}, AV_{SS}	V_{SS} = AV_{SS}	−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to + 2.1 and −0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P140	−0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P80 to P87, P90 to P92	−0.3 to AV_{DD} + 0.3 Note 2	V
	V_{I3}	P121 to P124, P137, RESET	−0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140	−0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P80 to P87, P90 to P92	−0.3 to AV_{DD} + 0.3	V
Analog input voltage	V_{AI1}	ANI22 to ANI27	−0.3 to V_{DD} + 0.3 and −0.3 to AV_{DD} + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI10	−0.3 to AV_{DD} + 0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. For pins to be used in A/D conversion, the voltage should not exceed the value AV_{DD} + 0.3.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/3)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140	−40	mA
		Total of all pins −170 mA	P40, P41, P120, P125	−70	mA
			P00, P10 to P17, P30 to P32, P60 to P63, P70 to P73, P130, P140	−100	mA
	I_{OH2}	Per pin	P80 to P87, P90 to P92	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140	40	mA
		Total of all pins 170 mA	P40, P41, P120, P125	70	mA
			P00, P10 to P17, P30 to P32, P60 to P63, P70 to P73, P130, P140	100	mA
	I_{OL2}	Per pin	P80 to P87, P90 to P92	1	mA
		Total of all pins		5	mA

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/3)

Parameter	Symbol	Conditions		Ratings	Unit
Positive injected current ($V_I > V_{DD}$) Note	I_{INJP}	Per pin	P00, P10, P11, P13 to P17, P30 to P32, P41, P60 to P63, P140	5	mA
			P70 to P73, P80 to P87, P90 to P92, P120, P125	2	mA
Negative injected current ($V_I < V_{SS}$) Note	I_{INJN}	Per pin	P00, P10, P11, P13 to P17, P30 to P32, P41, P60 to P63, P140	−5	mA
			P70 to P73, P80 to P87, P90 to P92, P120, P125	−0.5	mA
Sum of all positive injected currents Note	ΣI_{INJP}	Total of all pins	P00, P10, P11, P13 to P17, P30 to P32, P41, P60 to P63, P140	40	mA
			P70 to P73, P80 to P87, P90 to P92, P120, P125	10	mA
Sum of all negative injected currents Note	ΣI_{INJN}	Total of all pins	P00, P10, P11, P13 to P17, P30 to P32, P41, P60 to P63, P140	−40	mA
			P70 to P73, P80 to P87, P90 to P92, P120, P125	−2	mA
Total of all injected currents Note	$\Sigma\|I_{INJP}\| + \Sigma\|I_{INJN}\|$	Total of all pins	P00, P10, P11, P13 to P17, P30 to P32, P41, P60 to P63, P140	40	mA
			P70 to P73, P80 to P87, P90 to P92, P120, P125	10	mA
Operating ambient temperature	T_A	In normal operation mode	Grade 3 products	−40 to +105	°C
			Grade 4 products	−40 to +125	
		In flash memory programming mode	Grade 3 products	−40 to +105	°C
			Grade 4 products	−40 to +125	
Operating temperature	T_{OPR}		Grade 3 products	−40 to +105	°C
			Grade 4 products	−40 to +125	
Storage temperature	T_{stg}			−65 to +150	°C

Note Conditions: 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

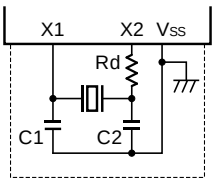
Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. V_I: Input voltage level to the port pins.

4.2 Oscillator Characteristics

4.2.1 Main System Clock Oscillator Characteristics

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator/ Crystal resonator		X1 clock oscillation frequency (fx)	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V (Grade 3 products)	2.0		16.0	

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant. Customers are also requested to adequately evaluate the oscillation on their system. Determine the X1 clock oscillation stabilization time using the oscillation stabilization time of the oscillation stabilization time counter status register (OSTC) and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

4.2.2 On-chip Oscillator Characteristics

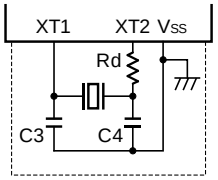
($T_A = T_{OPR}$, $1.8\ V \le V_{DD} \le 5.5\ V$, $V_{SS} = 0\ V$)

Oscillators	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	$2.7\ V \le V_{DD} \le 5.5\ V$	2		80	MHz
		$1.8\ V \le V_{DD} < 2.7\ V$ (Grade 3 products)	2		16	
High-speed on-chip oscillator clock frequency accuracy	–		−1.0		+1.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}, f_{WDT}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy	–		−15		+15	%

Note High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/040C2H) and bits 0 to 2 of the HOCODIV register.

4.2.3 Subsystem Clock Oscillator Characteristics

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})	1.8 V ≤ V_{DD} ≤ 5.5 V	29.0	32.768	35.0	kHz

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption and thus required to be adequately evaluated on the system. Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

4.2.4 PLL Circuit Characteristics

($T_A = T_{OPR}$, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
PLL input enable clock frequency Note 1	f_{PLLI}	f_{MAIN}: 4.0 MHz	FMAINDIV[1:0] = 00B	3.92	4.0	4.08	MHz
		f_{MAIN}: 8.0 MHz	FMAINDIV[1:0] = 00B	7.84	8.0	8.16	MHz
		f_{MAIN}: 16.0 MHz	FMAINDIV[1:0] = 10B	7.84	8.0	8.16	MHz
		f_{MAIN}: 20.0 MHz	FMAINDIV[1:0] = 11B	4.90	5.0	5.10	MHz
PLL output frequency (center value)	f_{PLL}	f_{MAIN}: 20 MHz, PLLMULA = 0, PLLMUL = 1	PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 16/2			MHz
			PLLDIV0 = 0, FPLLDIV = 1, PLLDIV1 = 1	f_{PLLI} × 16			MHz
		f_{MAIN}: 4 MHz, PLLMULA = 1, PLLMUL = 1	PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 20/2			MHz
			PLLDIV0 = 0, FPLLDIV = 1, PLLDIV1 = 1	f_{PLLI} × 20			MHz
		f_{MAIN}: 8 MHz or 16 MHz, PLLMULA = 0, PLLMUL = 0	PLLDIV0 = 1, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 12/4			MHz
			PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 1	f_{PLLI} × 12/2			MHz
		f_{MAIN}: 8 MHz or 16 MHz, PLLMULA = 0, PLLMUL = 1	PLLDIV0 = 1, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 16/4			MHz
			PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 1	f_{PLLI} × 16/2			MHz
		f_{MAIN}: 8 MHz or 16 MHz, PLLMULA = 1, PLLMUL = 0	PLLDIV0 = 0, FPLLDIV = 0, PLLDIV1 = 0	f_{PLLI} × 10/2			MHz
			PLLDIV0 = 0, FPLLDIV = 1, PLLDIV1 = 1	f_{PLLI} × 10			MHz
Long-term jitter Note 2	t_{LJ}	term = 1 μs		−1		+1	ns
		term = 10 μs		−1		+1	ns
		term = 20 μs		−2		+2	ns

Notes 1. X1 clock or external main system clock can be selected as the PLL input clock.

2. Guaranteed by design, but not tested before shipment.

Caution When using Grade 3 products with 1.8 V ≤ V_{DD} < 2.7 V, the PLL circuit cannot be used.

Remark f_{MAIN}: Main system clock frequency.

4.3 DC Characteristics

4.3.1 Pin Characteristics

For the relationship between the port pins shown in the following tables and the products, refer to **2. PIN FUNCTIONS**.

($T_A = T_{OPR}$, 1.8 V ≤ $V_{DD} = AV_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS}$ = 0 V) **(1/6)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for: P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140		4.0 V ≤ V_{DD} ≤ 5.5 V			−5.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			−3.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			−0.5	mA
		Per pin for: P10, P12, P14, P30, P120, P140 (special slew rate)		4.0 V ≤ V_{DD} ≤ 5.5 V			−0.6	mA
				2.7 V ≤ V_{DD} < 4.0 V			−0.2	mA
				1.8 V ≤ V_{DD} < 2.7 V			−0.2	mA
		Total of: P40, P41, P120, P125 (for duty factors ≤ 70% Note 2)		4.0 V ≤ V_{DD} ≤ 5.5 V			−20.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			−10.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			−5.0	mA
		Total of: P00, P10 to P17, P30 to P32, P60 to P63, P70 to P73, P130, P140 (for duty factors ≤ 70% Note 2)		4.0 V ≤ V_{DD} ≤ 5.5 V			−30.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			−19.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			−10.0	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	Grade 3 products	4.0 V ≤ V_{DD} ≤ 5.5 V			−50.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			−29.0	mA
				1.8 V ≤ V_{DD} < 2.7 V			−15.0	mA
			Grade 4 products	4.0 V ≤ V_{DD} ≤ 5.5 V			−42.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			−29.0	mA
	I_{OH2}	Per pin for: P80 to P87, P90 to P92		1.8 V ≤ AV_{DD} ≤ 5.5 V			−0.1	mA
		Total of all pins (for duty factors ≤ 70% Note 2)		1.8 V ≤ AV_{DD} ≤ 5.5 V			−2.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} and AV_{DD} pins to an output pin.

2. These output current values are obtained under the condition that the duty factor is 70% or less.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins $(I_{OH} \times 0.7) / (n \times 0.01)$

<Example> Where I_{OH} = −10.0 mA and n = 80%
Total output current of pins = $(-10.0 \times 0.7) / (80 \times 0.01) \approx -8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Cautions 1. P10 to P17, P32, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

2. Operating voltage condition: 1.8 V ≤ $V_{DD} = AV_{DD}$ < 2.7 V is only available for Grade 3 products.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, $1.8\ V \le V_{DD} = AV_{DD} \le 5.5\ V$, $V_{SS} = AV_{SS} = 0\ V$) **(2/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for: P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140	$4.0\ V \le V_{DD} \le 5.5\ V$			8.5	mA
			$2.7\ V \le V_{DD} < 4.0\ V$			4.0	mA
			$1.8\ V \le V_{DD} < 2.7\ V$			0.6	mA
		Per pin for: P10, P12, P14, P30, P120, P140 (special slew rate)	$4.0\ V \le V_{DD} \le 5.5\ V$			0.59	mA
			$2.7\ V \le V_{DD} < 4.0\ V$			0.07	mA
			$1.8\ V \le V_{DD} < 2.7\ V$			0.07	mA
		Total of: P40, P41, P120, P125 (for duty factors ≤ 70% Note 2)	$4.0\ V \le V_{DD} \le 5.5\ V$			20.0	mA
			$2.7\ V \le V_{DD} < 4.0\ V$			15.0	mA
			$1.8\ V \le V_{DD} < 2.7\ V$			9.0	mA
		Total of: P00, P10 to P17, P30 to P32, P60 to P63, P70 to P73, P130, P140 (for duty factors ≤ 70% Note 2)	$4.0\ V \le V_{DD} \le 5.5\ V$			45.0	mA
			$2.7\ V \le V_{DD} < 4.0\ V$			35.0	mA
			$1.8\ V \le V_{DD} < 2.7\ V$			20.0	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	$4.0\ V \le V_{DD} \le 5.5\ V$			65.0	mA
			$2.7\ V \le V_{DD} < 4.0\ V$			50.0	mA
			$1.8\ V \le V_{DD} < 2.7\ V$			29.0	mA
	I_{OL2}	Per pin for: P80 to P87, P90 to P92	$1.8\ V \le AV_{DD} \le 5.5\ V$			0.4	mA
		Total of all pins (for duty factors ≤ 70% Note 2)	$1.8\ V \le AV_{DD} \le 5.5\ V$			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} and AV_{SS} pins.

2. These output current values are obtained under the condition that the duty factor is 70% or less.
The output current values when the duty factor is changed to a value greater than 70% can be calculated from the following expression (when the duty factor is changed to n%).

- Total output current of pins $(I_{OL} \times 0.7) / (n \times 0.01)$

<Example> Where I_{OL} = 10.0 mA and n = 80%
Total output current of pins = $(10.0 \times 0.7) / (80 \times 0.01) \approx 8.7$ mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution Operating voltage condition: $1.8\ V \le V_{DD} = AV_{DD} < 2.7\ V$ is only available for Grade 3 products.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 1.8 V ≤ $V_{DD} = AV_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS}$ = 0 V) **(3/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P140 (Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.65 V_{DD}		V_{DD} Note	V
			2.7 V ≤ V_{DD} < 4.0 V	0.7 V_{DD}		V_{DD} Note	V
			1.8 V ≤ V_{DD} < 2.7 V	0.7 V_{DD}		V_{DD} Note	V
	V_{IH2}	P10, P11, P13, P14, P16, P17, P30, P41, P60 to P63, P70, P71, P73, P120, P125 (Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD} Note	V
			2.7 V ≤ V_{DD} < 4.0 V	0.85 V_{DD}		V_{DD} Note	V
			1.8 V ≤ V_{DD}< 2.7 V	0.85 V_{DD}		V_{DD} Note	V
	V_{IH3}	P10, P11, P13, P14, P16, P17, P30, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD} Note	V
			2.7 V ≤ V_{DD} < 4.0 V	2.0		V_{DD} Note	V
			1.8 V ≤ V_{DD}< 2.7 V	1.5		V_{DD} Note	V
	V_{IH4}	P80 to P87, P90 to P92 (fixed to Schmitt 3 mode)	4.0 V ≤ AV_{DD} ≤ 5.5 V	0.8 AV_{DD}		AV_{DD}	V
			2.7 V ≤ AV_{DD} < 4.0 V	0.85 AV_{DD}		AV_{DD}	V
			1.8 V ≤ AV_{DD} < 2.7 V	0.85 AV_{DD}		AV_{DD}	V
	V_{IH5}	RESET (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.65 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.7 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.7 V_{DD}		V_{DD}	V
	V_{IH6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.8 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.8 V_{DD}		V_{DD}	V
	V_{IH7}	P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0.85 V_{DD}		V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0.85 V_{DD}		V_{DD}	V

Note For pins P10 to P17, P32, P60 to P63, P70 to P72, and P120, the maximum V_{IH} value is V_{DD} even when the pins are in N-ch open-drain mode and set to high-level output.

Caution Operating voltage condition: 1.8 V ≤ $V_{DD} = AV_{DD}$ < 2.7 V is only available for Grade 3 products.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 1.8 V ≤ $V_{DD} = AV_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS}$ = 0 V) **(4/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P140 (Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.35 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.3 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.3 V_{DD}	V
	V_{IL2}	P10, P11, P13, P14, P16, P17, P30, P41, P60 to P63, P70, P71, P73, P120, P125 (Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.5 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.4 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.4 V_{DD}	V
	V_{IL3}	P10, P11, P13, P14, P16, P17, P30, P62, P63, P70, P71, P73, P125 (TTL mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.5	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.32	V
	V_{IL4}	P80 to P87, P90 to P92 (fixed to Schmitt 3 mode)	4.0 V ≤ AV_{DD} ≤ 5.5 V	0		0.5 AV_{DD}	V
			2.7 V ≤ AV_{DD} < 4.0 V	0		0.4 AV_{DD}	V
			1.8 V ≤ AV_{DD} < 2.7 V	0		0.4 AV_{DD}	V
	V_{IL5}	RESET (fixed to Schmitt 1 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.35 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.3 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.3 V_{DD}	V
	V_{IL6}	P121 to P124, EXCLK, EXCLKS (fixed to Schmitt 2 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.2 V_{DD}	V
	V_{IL7}	P137 (fixed to Schmitt 3 mode)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.5 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.4 V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.4 V_{DD}	V

Caution Operating voltage condition: 1.8 V ≤ $V_{DD} = AV_{DD}$ < 2.7 V is only available for Grade 3 products.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, $1.8\ V \le V_{DD} = AV_{DD} \le 5.5\ V$, $V_{SS} = AV_{SS} = 0\ V$) **(5/6)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140 (normal slew rate)	$4.0\ V \le V_{DD} \le 5.5\ V$, $I_{OH1} = -5.0\ mA$	$V_{DD} - 0.9$			V
			$2.7\ V \le V_{DD} \le 5.5\ V$, $I_{OH1} = -3.0\ mA$	$V_{DD} - 0.7$			V
			$2.7\ V \le V_{DD} \le 5.5\ V$, $I_{OH1} = -1.0\ mA$	$V_{DD} - 0.5$			V
			$1.8\ V \le V_{DD} \le 5.5\ V$, $I_{OH1} = -0.5\ mA$	$V_{DD} - 0.5$			V
	V_{OH2}	P80 to P87, P90 to P92	$1.8\ V \le AV_{DD} \le 5.5\ V$ $I_{OH2} = -100\ \mu A$	$AV_{DD} - 0.5$			V
	V_{OH3}	P10, P12, P14, P30, P120, P140 (special slew rate)	$4.0\ V \le V_{DD} \le 5.5\ V$, $I_{OH3} = -0.6\ mA$	$V_{DD} - 0.8$			V
			$2.7\ V \le V_{DD} \le 5.5\ V$, $I_{OH3} = -0.2\ mA$	$V_{DD} - 0.5$			V
			$1.8\ V \le V_{DD} \le 5.5\ V$, $I_{OH3} = -0.2\ mA$	$V_{DD} - 0.5$			V
Output voltage, low	V_{OL1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140 (normal slew rate)	$4.0\ V \le V_{DD} \le 5.5\ V$, $I_{OL1} = 8.5\ mA$			0.7	V
			$4.0\ V \le V_{DD} \le 5.5\ V$, $I_{OL1} = 4.0\ mA$			0.4	V
			$2.7\ V \le V_{DD} \le 5.5\ V$, $I_{OL1} = 4.0\ mA$			0.7	V
			$2.7\ V \le V_{DD} \le 5.5\ V$, $I_{OL1} = 1.5\ mA$			0.4	V
			$1.8\ V \le V_{DD} \le 5.5\ V$ $I_{OL1} = 0.6\ mA$			0.4	V
	V_{OL2}	P80 to P87, P90 to P92	$1.8\ V \le AV_{DD} \le 5.5\ V$ $I_{OL2} = 400\ \mu A$			0.4	V
	V_{OL3}	P10, P12, P14, P30, P120, P140 (special slew rate)	$4.0\ V \le V_{DD} \le 5.5\ V$, $I_{OL3} = 0.6\ mA$			0.8	V
			$2.7\ V \le V_{DD} \le 5.5\ V$, $I_{OL3} = 0.07\ mA$			0.5	V
			$1.8\ V \le V_{DD} \le 5.5\ V$, $I_{OL3} = 0.07\ mA$			0.5	V

Cautions 1. P10 to P17, P32, P60 to P63, P70 to P72, and P120 do not output high level in N-ch open-drain mode.

2. Operating voltage condition: $1.8\ V \le V_{DD} = AV_{DD} < 2.7\ V$ is only available for Grade 3 products.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = T_{OPR}$, 1.8 V ≤ $V_{DD} = AV_{DD}$ ≤ 5.5 V, $V_{SS} = AV_{SS}$ = 0 V) **(6/6)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P140	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P80 to P87, P90 to P92	$V_I = AV_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P137, RESET	$V_I = V_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P140	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P80 to P87, P90 to P92	$V_I = AV_{SS}$				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
	I_{LIL4}	P137, RESET	$V_I = V_{SS}$				−1	μA
Positive injected current Note	$I_{INJPRMS}$	P00, P10, P11, P13 to P17, P30 to P32, P41, P60 to P63, P140	Per pin, $V_I > V_{DD}$				0.4	mA
			Total of all pins, $V_I > V_{DD}$				4	mA
		P70 to P73, P80 to P87, P90 to P92, P120, P125	Per pin, $V_I > V_{DD} = AV_{DD}$				0.15	mA
			Total of all pins, $V_I > V_{DD} = AV_{DD}$				1	mA
On-chip pull-up resistance	R_U	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P140	$V_I = V_{SS}$, in input port		10	20	100	kΩ

Note Guaranteed by design, but not tested before shipment.

Caution Operating voltage condition: 1.8 V ≤ $V_{DD} = AV_{DD}$ < 2.7 V is only available for Grade 3 products.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. V_I : Input voltage level to the port pins.

4.3.2 Supply Current Characteristics

(1) RL78/F22 (Grade 3 Products)

(T_A = −40 to +105°C, 1.8 V ≤ V_{DD} = AV_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V) **(1/2)**

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Notes 3, 4		5.5	11.0	mA
					f_{IH} = 40 MHz	f_{CLK} = f_{IH} Notes 3, 4		5.3	10.0	mA
					f_{IH} = 16 MHz	f_{CLK} = f_{IH} Notes 3, 4		2.5	4.9	mA
					f_{IH} = 2 MHz	f_{CLK} = f_{IH} Notes 3, 4		0.85	1.9	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		2.9	5.6	mA
					f_{MX} = 16 MHz	f_{CLK} = f_{MX} Notes 3, 5		2.4	4.8	mA
					f_{MX} = 2 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.75	1.8	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		5.6	11.0	mA
					f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		5.4	10.0	mA
					f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Notes 3, 6		5.2	9.5	mA
				Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7		10.5	220	µA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8		8.6	220	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit and A/D converter are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Caution When 1.8 V ≤ V_{DD} < 2.7 V, the maximum operating clock (f_{CLK}) is 16 MHz.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +105°C, 1.8 V ≤ V_{DD} = AV_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, 3	I_{DD2}	HALT mode Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Note 5		1.8	6.5	mA
				f_{IH} = 40 MHz	f_{CLK} = f_{IH} Note 5		1.5	5.5	mA
				f_{IH} = 16 MHz	f_{CLK} = f_{IH} Note 5		0.8	3.0	mA
				f_{IH} = 2 MHz	f_{CLK} = f_{IH} Note 5		0.4	1.6	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Note 6		0.9	3.4	mA
				f_{MX} = 16 MHz	f_{CLK} = f_{MX} Note 6		0.75	3.0	mA
				f_{MX} = 2 MHz	f_{CLK} = f_{MX} Note 6		0.3	1.6	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		1.8	6.5	mA
				f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		1.7	5.5	mA
				f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Note 7		1.5	5.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 8		6.5	120	μA
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 9		6.5	120	μA
	I_{DD3}	STOP mode Note 4	T_A = +25°C				0.5		μA
			T_A = +50°C					8.0	
			T_A = +70°C					18.0	
			T_A = +105°C					75.0	
	I_{SNOZ}	SNOOZE mode	DTC operation				4.0		mA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, and A/D converter are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped. When the RAMSDMD bit and RAMSDS bit of the PSMCR register are set to 11B (shutdown mode).

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Caution When 1.8 V ≤ V_{DD} < 2.7 V, the maximum operating clock (f_{CLK}) is 16 MHz.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +105°C, 1.8 V ≤ V_{DD} = AV_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{WDT} = 15 kHz			0.3		µA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	AV_{DD} = V_{DD} = 5.0 V		1.3	1.6	mA
		When low current conversion	AV_{DD} = V_{DD} = 2.7 V		0.8	1.0	mA
		When internal reference voltage is selected Note 4			128		µA
Sample-and-hold circuit operating current	I_{ADSH} Note 5				0.8	1.2	mA
LVD operating current	I_{LVD} Note 6				0.045		µA
BGO operating current	I_{BGO} Note 7				2.5	12.2	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

5. Operating current that increases when the sample-and-hold circuit is used. This current flows for each analog input channel.

6. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

7. Current increased by the BGO operation. The current value is the sum of I_{DD1} and I_{BGO} when the BGO operates in operation mode.

(2) RL78/F22 (Grade 4 Products)

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} = AV_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V) **(1/2)**

Items	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Notes 3, 4		5.5	11.0	mA
					f_{IH} = 40 MHz	f_{CLK} = f_{IH} Notes 3, 4		5.3	10.0	mA
					f_{IH} = 2 MHz	f_{CLK} = f_{IH} Notes 3, 4		0.85	2.0	mA
				Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Notes 3, 5		2.9	5.6	mA
					f_{MX} = 2 MHz	f_{CLK} = f_{MX} Notes 3, 5		0.75	1.9	mA
				Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		5.6	11.0	mA
					f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Notes 3, 6		5.4	10.0	mA
					f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Notes 3, 6		5.2	9.5	mA
				Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 7		10.5	400	µA
				Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 8		8.6	400	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. Current drawn when all the CPU instructions are executed.

3. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, the LVD circuit and A/D converter are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

5. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

8. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} = AV_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V) **(2/2)**

Items	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, 3	I_{DD2}	HALT mode Note 2	High-speed on-chip oscillator clock operation	f_{IH} = 80 MHz	f_{CLK} = 40 MHz Note 5		1.8	6.5	mA
				f_{IH} = 40 MHz	f_{CLK} = f_{IH} Note 5		1.5	5.5	mA
				f_{IH} = 2 MHz	f_{CLK} = f_{IH} Note 5		0.4	1.7	mA
			Resonator operation	f_{MX} = 20 MHz	f_{CLK} = f_{MX} Note 6		0.9	3.4	mA
				f_{MX} = 2 MHz	f_{CLK} = f_{MX} Note 6		0.3	1.7	mA
			Resonator operation (PLL operation) (PLL input clock = f_{MX})	f_{PLL} = 80 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		1.8	6.5	mA
				f_{PLL} = 40 MHz, f_{MX} = 20 MHz	f_{CLK} = 40 MHz Note 7		1.7	5.5	mA
				f_{PLL} = 40 MHz, f_{MX} = 4 MHz	f_{CLK} = 40 MHz Note 7		1.5	5.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz	f_{CLK} = f_{SUB} Note 8		6.5	210	μA
			Low-speed on-chip oscillator clock operation	f_{IL} = 15 kHz	f_{CLK} = f_{IL} Note 9		6.5	210	μA
	I_{DD3}	STOP mode Note 4	T_A = +25°C				0.5		μA
			T_A = +50°C					8.0	
			T_A = +70°C					18.0	
			T_A = +105°C					75.0	
			T_A = +125°C					175.0	
	I_{SNOZ}	SNOOZE mode	DTC operation				4.0		mA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, not including the current flowing into the I/O buffer and on-chip pull-up/pull-down resistors.

2. When HALT mode is entered during fetch from the flash memory.

3. The values below the MAX. column include the peripheral operation current and STOP leakage current. However, the watchdog timer, LVD circuit, and A/D converter are stopped.

4. When high-speed system clock, subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped. When the RAMSDMD bit and RAMSDS bit of the PSMCR register are set to 11B (shutdown mode).

5. When high-speed system clock, subsystem clock, PLL clock, and low-speed on-chip oscillator clock are stopped.

6. When subsystem clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

7. When subsystem clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped.

8. When high-speed system clock, PLL clock, high-speed on-chip oscillator clock, and low-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

9. When high-speed system clock, subsystem clock, PLL clock, and high-speed on-chip oscillator clock are stopped, and with setting of ADCEN = 0 or ADSLP = 1.

Remark f_{MX}: High-speed system clock frequency
f_{SUB}: Subsystem clock frequency
f_{PLL}: PLL clock frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency

(T_A = −40 to +125°C, 2.7 V ≤ V_{DD} = AV_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Window watchdog timer operating current	I_{WDT} Notes 1, 2	f_{WDT} = 15 kHz			0.3		µA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	AV_{DD} = V_{DD} = 5.0 V		1.3	1.6	mA
		When internal reference voltage is selected Note 4			128		µA
Sample-and-hold circuit operating current	I_{ADSH} Note 5				0.8	1.2	mA
LVD operating current	I_{LVD} Note 6				0.045		µA
BGO operating current	I_{BGO} Note 7				2.5	12.2	mA

Notes 1. When the high-speed on-chip oscillator clock and high-speed system clock are stopped.

2. Current flowing only to the watchdog timer (including the operation current of the 15 kHz on-chip oscillator). The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

3. Current flowing only to the A/D converter. The current value is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in operation mode or HALT mode.

4. Operating current that increases when the internal reference voltage is selected. This current flows even when conversion is stopped.

5. Operating current that increases when the sample-and-hold circuit is used. This current flows for each analog input channel.

6. Current flowing only to the LVD circuit. The current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD} when the LVD circuit operates in operation mode, HALT mode, or STOP mode.

7. Current increased by the BGO operation. The current value is the sum of I_{DD1} and I_{BGO} when the BGO operates in operation mode.

4.4 AC Characteristics

4.4.1 Basic Operation

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	High-speed on-chip oscillator clock operation		0.025		0.5	μs
		High-speed system clock operation		0.05		0.5	μs
		PLL clock operation		0.025		0.5	μs
		Subsystem clock operation		28.5	30.5	34.5	μs
		Low-speed on-chip oscillator clock operation			66.6		μs
		In self programming mode		0.025		0.5	μs
CPU/peripheral hardware clock frequency	f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.025		66.6	μs
		1.8 V ≤ V_{DD} < 2.7 V		0.0625		66.6	μs
External system clock frequency	f_{EX}			2.0		20.0	MHz
	f_{EXS}			29		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}			24			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI13 input high-level width, low-level width	t_{TIH}, t_{TIL}			1/f_{MCK} + 10			ns
TO00 to TO07, TO10 to TO13, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRJIO0, TRJO0 output frequency	f_{TO}	Normal slew rate, C = 30 pF	4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
			2.7 V ≤ V_{DD} < 4.0 V			8	MHz
			1.8 V ≤ V_{DD} < 2.7 V			4	MHz
		TO01, TO06, TO07, TO11, TO13, TRDIOC0, TRDIOD0, TRDIOD1, TRJO0 only, Special slew rate, C = 30 pF				2	MHz
PCLBUZ0 output frequency	f_{PCL}	Normal slew rate, C = 30 pF	4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
			2.7 V ≤ V_{DD} < 4.0 V			8	MHz
			1.8 V ≤ V_{DD} < 2.7 V			4	MHz
		Special slew rate, C = 30 pF				2	MHz
Timer RJ input cycle	t_C	TRJIO0		100			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0		40			ns
Timer RDe input high-level, low-level width	t_{TDIH}, t_{TDIL}	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRDCLK0, TRD0RES, TRD1RES		3/f_{TRD}			ns
Timer RDe pulse output forced cutoff signal low-level width	t_{TDSIL}	P137/INTP0	2 MHz < f_{CLK} ≤ 40 MHz	1			μs
			f_{CLK} ≤ 2 MHz	1/f_{CLK} + 1			μs

Cautions 1. Excluding the error in oscillation frequency accuracy.

2. Operating voltage condition: 1.8 V ≤ V_{DD} = AV_{DD} < 2.7 V is only available for Grade 3 products.

Remark f_{MCK}: Timer array unit operation clock frequency

f_{TRD}: Timer RDe operation clock frequency

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

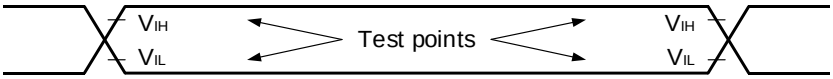
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP9 Note 1		1			µs
KR0 to KR7 key interrupt input low-level width	t_{KR}			250			ns
RESET low-level width	t_{RSL}	Note 1		10			µs
Port output rise time, port output fall time	t_{RO}, t_{FO}	P00, P10 to P17, P30 to P32, P40, P41, P60 to P63, P70 to P73, P120, P125, P130, P140 (normal slew rate) C = 30 pF	4.0 V ≤ V_{DD} ≤ 5.5 V			25	ns
			2.7 V ≤ V_{DD} < 4.0 V			55	ns
			1.8 V ≤ V_{DD} < 2.7 V			65	ns
		P10, P12, P14, P30, P120, P140 (special slew rate) C = 30 pF	4.0 V ≤ V_{DD} ≤ 5.5 V		25 Note 2	60	ns
			2.7 V ≤ V_{DD} < 4.0 V			100	ns
			1.8 V ≤ V_{DD} < 2.7 V			120	ns

Notes 1. Pins RESET, INTP0 to INTP3 have noise filters for transient levels lasting less than 100 ns.

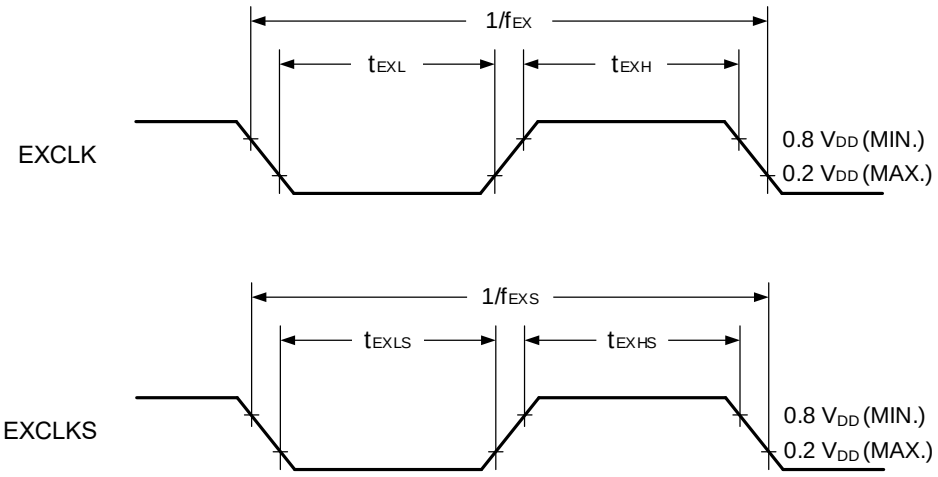
2. T_A = +25°C, V_{DD} = 5.0 V

Caution Operating voltage condition: 1.8 V ≤ V_{DD} = AV_{DD} < 2.7 V is only available for Grade 3 products.

AC Timing Test Points

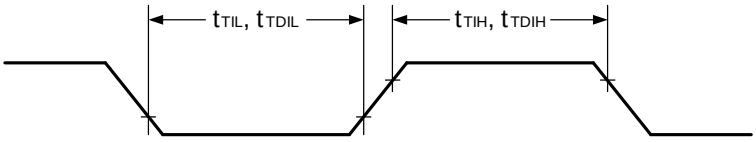


External System Clock Timing

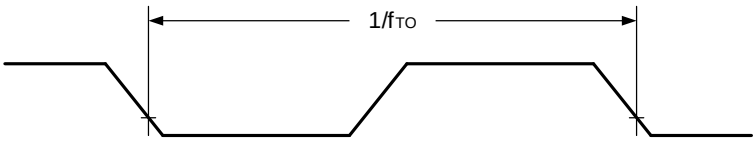


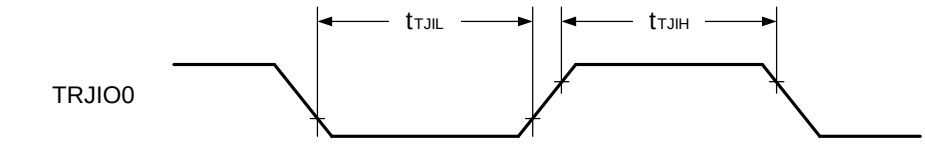
TI/TO Timing

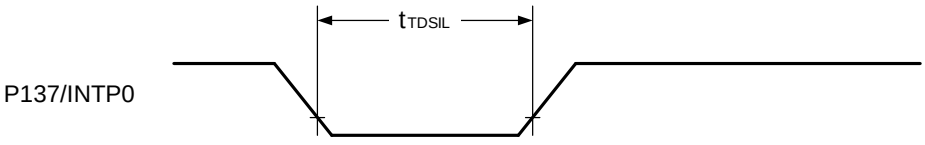
TI00 to TI07, TI10 to TI13, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRDCLK0, TRD0RES, TRD1RES



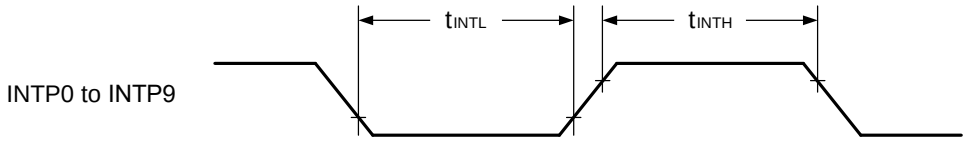
TO00 to TO07, TO10 to TO13, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRJIO0, TRJO0



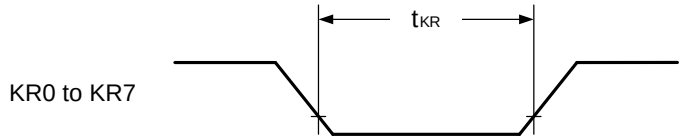




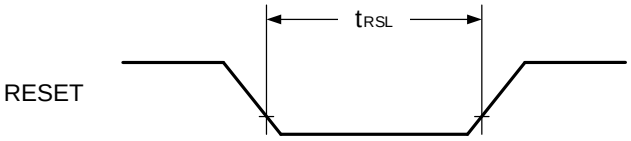
Interrupt Request Input Timing



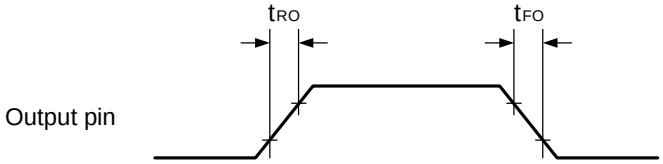
Key Interrupt Input Timing



RESET Input Timing



Output Rising and Falling Timing



4.5 Peripheral Functions Characteristics

4.5.1 Serial Array Unit

(1) During Communication at Same Potential (UART mode) (Dedicated Baud Rate Generator Output)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

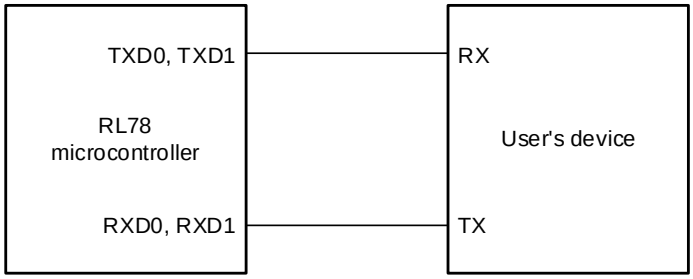
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate	–					f_{MCK}/6	bps
		f_{CLK} = 40 MHz, $f_{MCK} = f_{CLK}$ Note	Normal slew rate			6.6	Mbps
			Special slew rate			2	Mbps

Note The operating frequency and maximum transfer rate (normal slew rate) of the CPU/peripheral hardware clock (f_{CLK}) for each product are shown below.

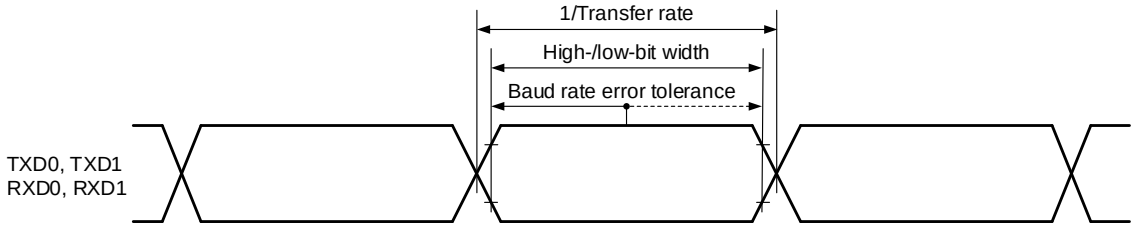
Grade 3 products: 40 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), transfer rate: MAX. 6.6 Mbps
16 MHz (1.8 V ≤ V_{DD} < 2.7 V), transfer rate: MAX. 2.6 Mbps

Grade 4 products: 40 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), transfer rate: MAX. 6.6 Mbps

UART Mode Connection Diagram (During Communication at Same Potential)



UART Mode Bit Width (During Communication at Same Potential) (Reference)



Caution Select normal input buffer for the RXD0 and RXD1 pins, and select normal output mode for the TXD0 and TXD1 pins.

Remark f_{MCK}: Serial array unit operation clock frequency

(2) During Communication at Same Potential (CSI mode) (Master Mode, SCKp … Internal Clock Output, Normal Slew Rate)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	Grade 3 products		100 Note 5			ns
		Grade 4 products		150 Note 5			ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 − 12			ns
		2.7 V ≤ V_{DD} < 4.0 V		t_{KCY1}/2 − 18			ns
		1.8 V ≤ V_{DD} < 2.7 V		t_{KCY1}/2 − 50			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	Grade 3 products	4.0 V ≤ V_{DD} ≤ 5.5 V	33			ns
			2.7 V ≤ V_{DD} < 4.0 V	44			ns
			1.8 V ≤ V_{DD} < 2.7 V	110			ns
		Grade 4 products	4.0 V ≤ V_{DD} ≤ 5.5 V	44			ns
			2.7 V ≤ V_{DD} < 4.0 V	55			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			30			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4				30	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

5. $t_{KCY1} \geq 4/f_{MCK}$ must also be satisfied.
Grade 3 products: 40 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), transfer rate: MAX. 10.0 Mbps (f_{MCK} = 40 MHz, t_{KCY1} = 100 ns)
16 MHz (1.8 V ≤ V_{DD} < 2.7 V), transfer rate: MAX. 4.0 Mbps (f_{MCK} = 16 MHz, t_{KCY1} = 250 ns)
Grade 4 products: 40 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), transfer rate: MAX. 6.6 Mbps (f_{MCK} = 40 MHz, t_{KCY1} = 150 ns)

Cautions 1. Select normal input buffer for the SIp pin, and select normal output mode for the SOp and SCKp pins.

2. Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(3) During Communication at Same Potential (CSI mode) (Master Mode, SCKp … Internal Clock Output, Special Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}		500 Note 5			ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 − 60			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}		120			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		80			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			90	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

5. $t_{KCY1} \geq 4/f_{MCK}$ must also be satisfied.

Caution Select normal input buffer for the SIp pin, and select normal output mode and special slew rate for the SOp and SCKp pins.

Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(4) During Communication at Same Potential (CSI mode) (Slave Mode, SCKp … External Clock Input, Normal Slew Rate)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} < 5.5 V	f_{MCK} > 32 MHz	10/f_{MCK} Note 5			ns
			f_{MCK} ≤ 32 MHz	8/f_{MCK} Note 5			ns
		1.8 V ≤ V_{DD} < 2.7 V	f_{MCK} ≤ 16 MHz	6/f_{MCK} and 750 Note 5			ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}			1/f_{MCK} + 20			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 44	ns
			2.7 V ≤ V_{DD} < 4.0 V			2/f_{MCK} + 57	ns
			1.8 V ≤ V_{DD} < 2.7 V			2/f_{MCK} + 110	ns
SSIp setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
SSIp hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

5. The operating frequency and maximum transfer rate for each product are shown below.
Grade 3 products: 40 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), transfer rate: MAX. 4.0 Mbps (f_{MCK} = 40 MHz, t_{KCY2} = 250 ns)
16 MHz (1.8 V ≤ V_{DD} < 2.7 V), transfer rate: MAX. 1.3 Mbps (f_{MCK} = 16 MHz, t_{KCY1} = 750 ns)
Grade 4 products: 40 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V), transfer rate: MAX. 4.0 Mbps (f_{MCK} = 40 MHz, t_{KCY1} = 250 ns)

Cautions 1. Select normal input buffer for the SIp, SCKp and SSIp pins, and select normal output mode for the SOp pin.

2. Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

(5) During Communication at Same Potential (CSI mode) (Slave Mode, SCKp … External Clock Input, Special Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	20 MHz < f_{MCK}	10/f_{MCK}			ns
		10 MHz < f_{MCK} ≤ 20 MHz	8/f_{MCK}			ns
		f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2			ns
SIp setup time (to SCKp↑) Note1	t_{SIK2}		1/f_{MCK} + 50			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}		1/f_{MCK} + 50			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4			2/f_{MCK} + 80	ns
SSIp setup time	t_{SSIK}	DAP = 0	120			ns
		DAP = 1	1/f_{MCK} + 120			ns
SSIp hold time	t_{KSSI}	DAP = 0	1/f_{MCK} + 120			ns
		DAP = 1	120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

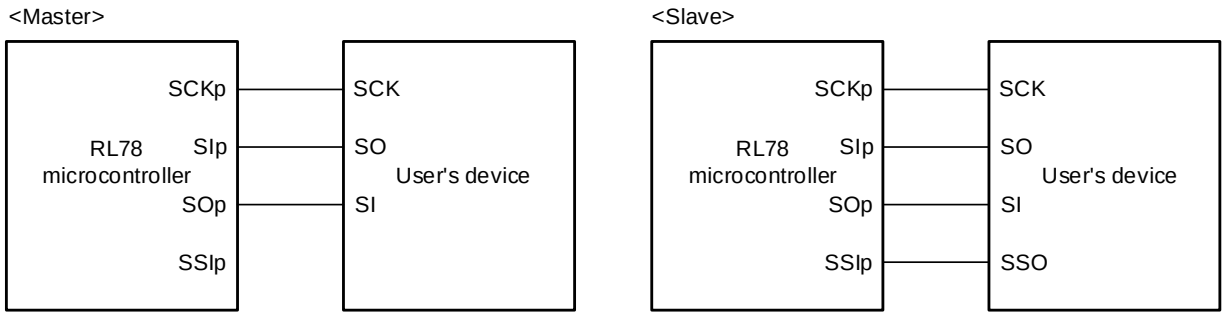
4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select normal input buffer for the SIp, SCKp and SSIp pins, and select normal output mode and special slew rate for the SOp pin.

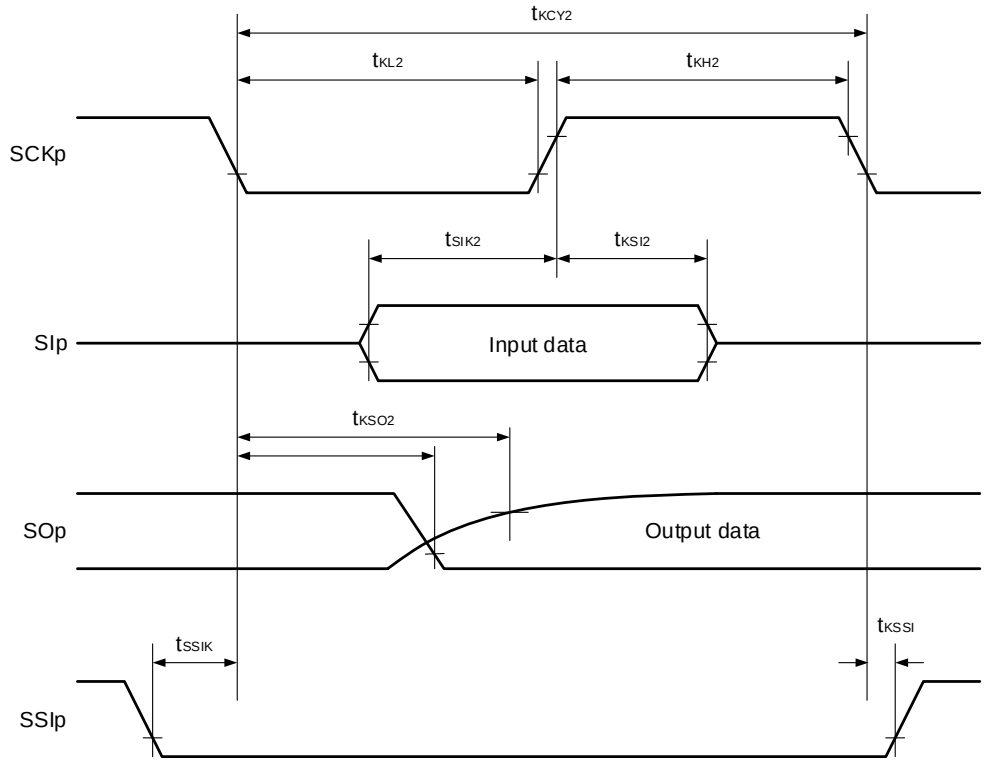
Remarks 1. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

CSI Mode Connection Diagram (During Communication at Same Potential)

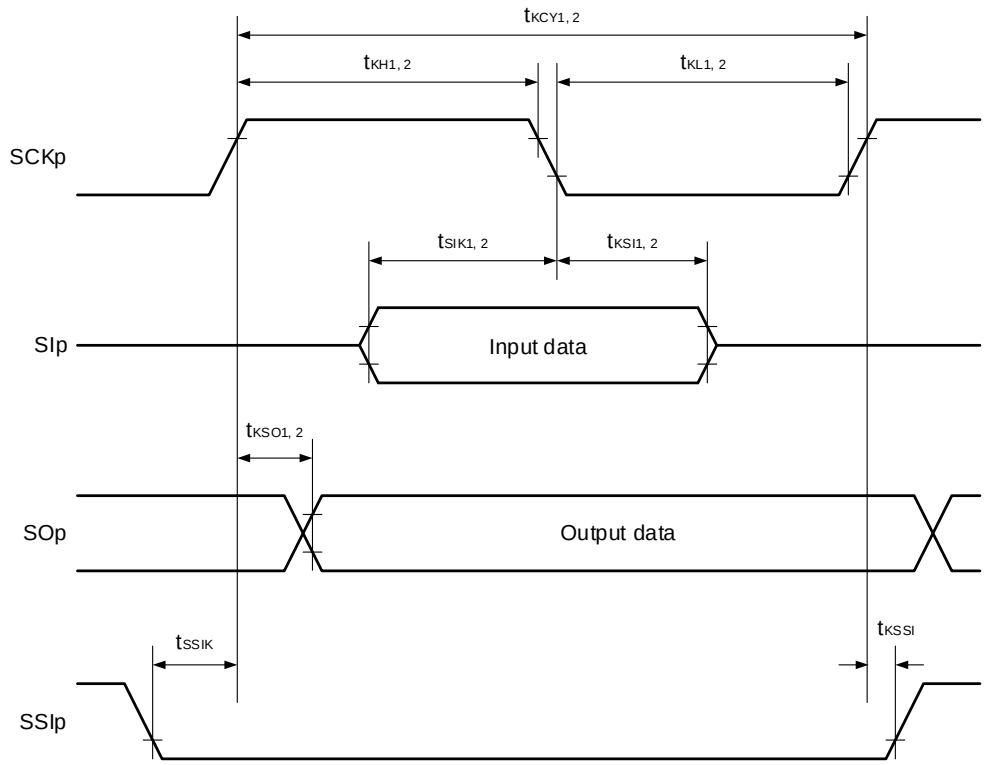


CSI Mode Serial Transfer Timing (During Communication at Same Potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

CSI Mode Serial Transfer Timing (During Communication at Same Potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

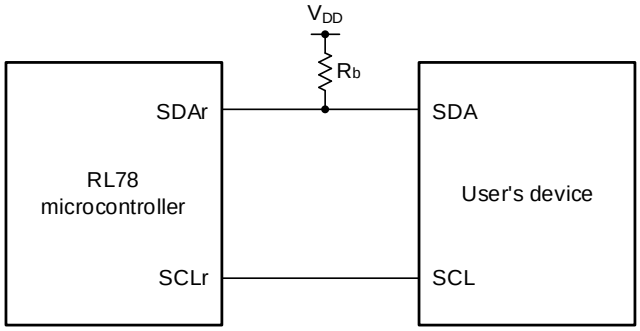
(6) During Communication at Same Potential (Simplified I²C Mode) (SDAr: N-ch Open-drain Output (EV_{DD} Tolerance) Mode, SCLr: Normal Output Mode)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

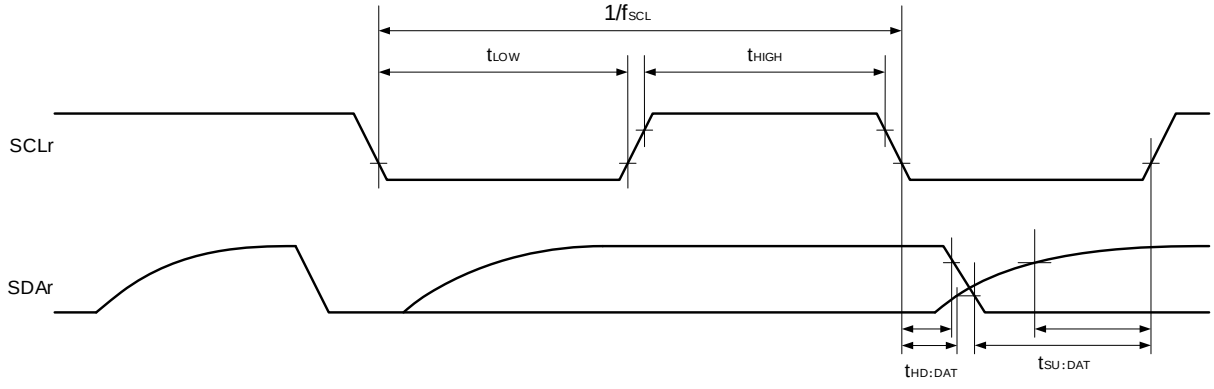
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V	C_b = 50 pF, R_b = 2.7 kΩ			1000 Note	kHz
		1.8 V ≤ V_{DD} < 2.7 V	C_b = 100 pF, R_b = 3.0 kΩ			400 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V	C_b = 50 pF, R_b = 2.7 kΩ	475			ns
		1.8 V ≤ V_{DD} < 2.7 V	C_b = 100 pF, R_b = 3.0 kΩ	1150			ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V	C_b = 50 pF, R_b = 2.7 kΩ	475			ns
		1.8 V ≤ V_{DD} < 2.7 V	C_b = 100 pF, R_b = 3.0 kΩ	1150			ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V	C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85			ns
		1.8 V ≤ V_{DD} < 2.7 V	C_b = 100 pF, R_b = 3.0 kΩ	1/f_{MCK} + 145			ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V	C_b = 50 pF, R_b = 2.7 kΩ	0		305	ns
		1.8 V ≤ V_{DD} < 2.7 V	C_b = 100 pF, R_b = 3.0 kΩ	0		355	ns

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

Simplified I²C Mode Connection Diagram (During Communication at Same Potential)



Simplified I²C Mode Serial Transfer Timing (During Communication at Same Potential)



Cautions 1. Select normal input buffer and N-ch open-drain output mode for the SDAr pin, and select normal output mode for the SCLr pin.

2. Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance,
C_b [F]: Communication line (SCLr, SDAr) load capacitance

2. r: IICr (r = 00, 01, 10, 11)

3. f_{MCK}: Serial array unit operation clock frequency

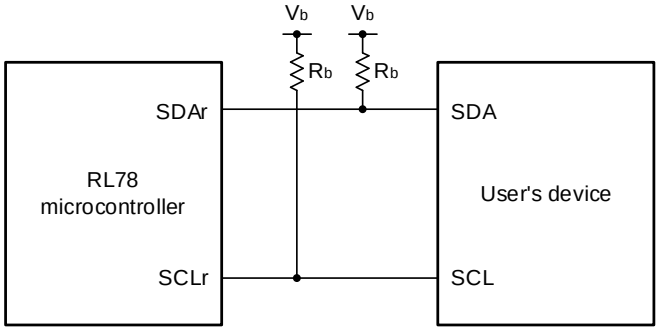
(7) During Communication at Same Potential (Simplified I^2C Mode) (SDAr and SCLr: N-ch Open-drain Output (EV_{DD} Tolerance) Mode)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}			400 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1300		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 3.0 kΩ	1300		ns
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	600		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 3.0 kΩ	400		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	1/f_{MCK} + 120		ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 270		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 3.0 kΩ	1/f_{MCK} + 290		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 1.7 kΩ	0	300	ns
		2.7 V ≤ V_{DD} < 4.0 V, C_b = 100 pF, R_b = 2.7 kΩ			
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 3.0 kΩ	0	300	ns

Note f_{SCL} ≤ f_{MCK}/4 must also be satisfied.

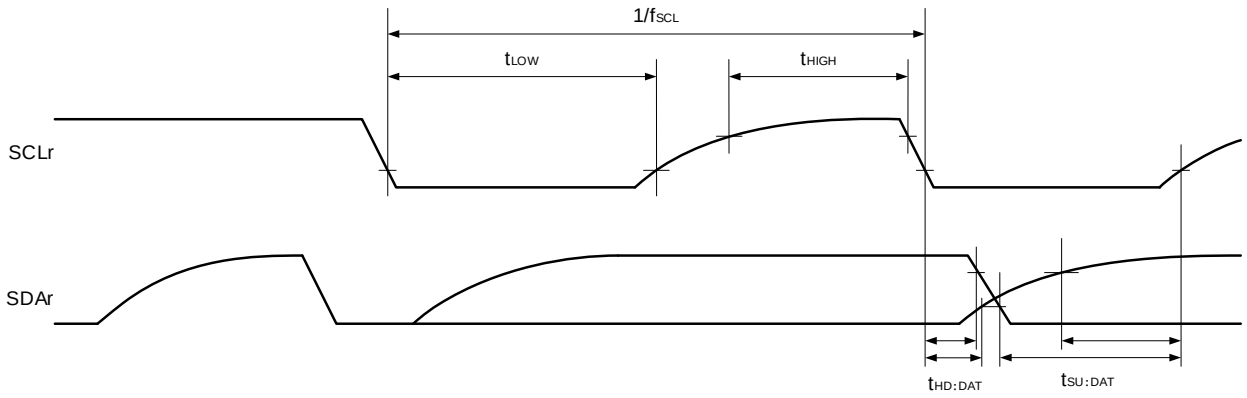
Simplified I^2C Mode Connection Diagram (During Communication at Same Potential)



Cautions 1. Select normal input buffer and N-ch open-drain output mode for the SDAr and SCLr pins.
2. Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance,
C_b [F]: Communication line (SDAr, SCLr) load capacitance,
V_b [V]: Communication line voltage
2. r: IICr (r = 00, 01, 10, 11)
3. f_{MCK}: Serial array unit operation clock frequency

Simplified I²C Mode Serial Transfer Timing (During Communication at Same Potential)



Remark r: IICr (r = 00, 01, 10, 11)

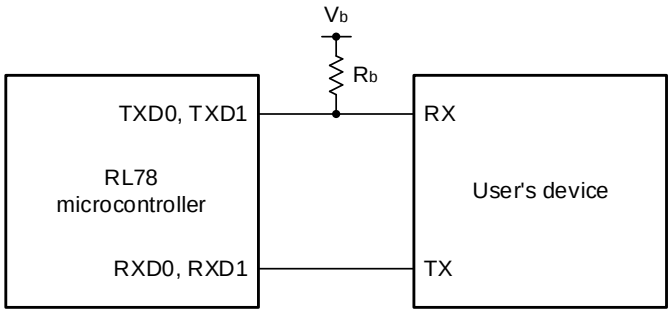
(8) Communication at Different Potential (UART mode) (TXD Output Buffer: N-ch Open-drain, RXD Input Buffer: TTL)

($T_A = T_{OPR}$, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

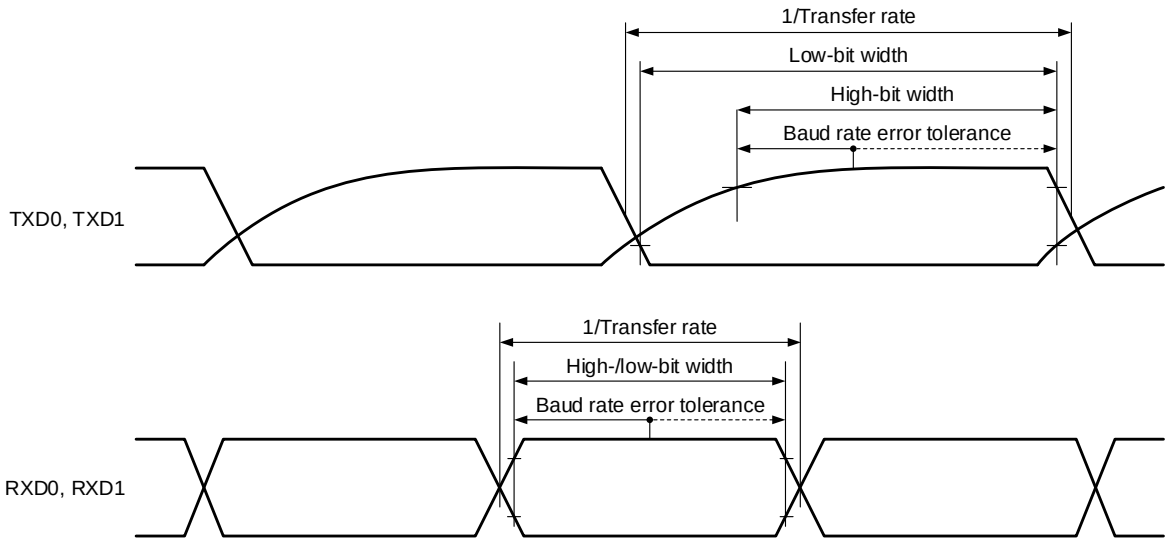
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Transfer rate	–	Reception	2.7 V ≤ V_b ≤ V_{DD}, V_{IH} = 2.2 V, V_{IL} = 0.8 V					f_{MCK}/6	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF)	Grade 3 products			5.3	Mbps
					Grade 4 products			4.0	
		Transmission	2.7 V ≤ V_b ≤ V_{DD}, V_{OH} = 2.2 V, V_{OL} = 0.8 V					Smaller number of the values given by f_{MCK}/6 and (Expression 1) is applicable.	bps
				Theoretical value of the maximum transfer rate Note (C_b = 30 pF) Normal slew rate	Grade 3 products			5.3	Mbps
					Grade 4 products			4.0	

Note (Expression 1): maximum transfer rate = $1/[\{-C_b \times R_b \times \ln(1-2.2/V_b)\} \times 3]$

UART Mode Connection Diagram (During Communication at Different Potential)



UART Mode Bit Width (During Communication at Different Potential) (Reference)



Caution Select TTL input buffer for the RXD0 and RXD1 pins, and select N-ch open-drain output mode for the TXD0 and TXD1 pins.

Remarks 1. R_b [Ω]: Communication line (TXD) pull-up resistance,
C_b [F]: Communication line (TXD) load capacitance,
V_b [V]: Communication line voltage

2. f_{MCK}: Serial array unit operation clock frequency

(9) During Communication at Different Potential (3 V Supply System) (CSI Mode) (Master Mode, SCKp … Internal Clock Output, Normal Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

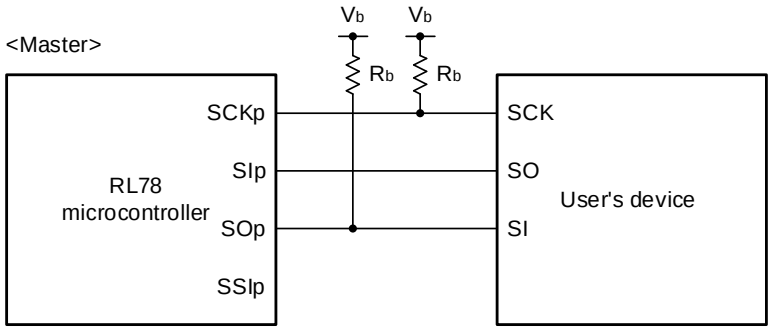
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	400 Note3			ns
SCKp high-level width	t_{KH1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 − 75			ns
SCKp low-level width	t_{KL1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 − 20			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	70			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
Delay time from SCKp↓ to SOp output Note1	t_{KSO1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
Delay time from SCKp↑ to SOp output Note2	t_{KSO1}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ			40	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. $t_{KCY1} \geq 4/f_{MCK}$ must also be satisfied.

CSI Mode Connection Diagram (During Communication at Different Potential)



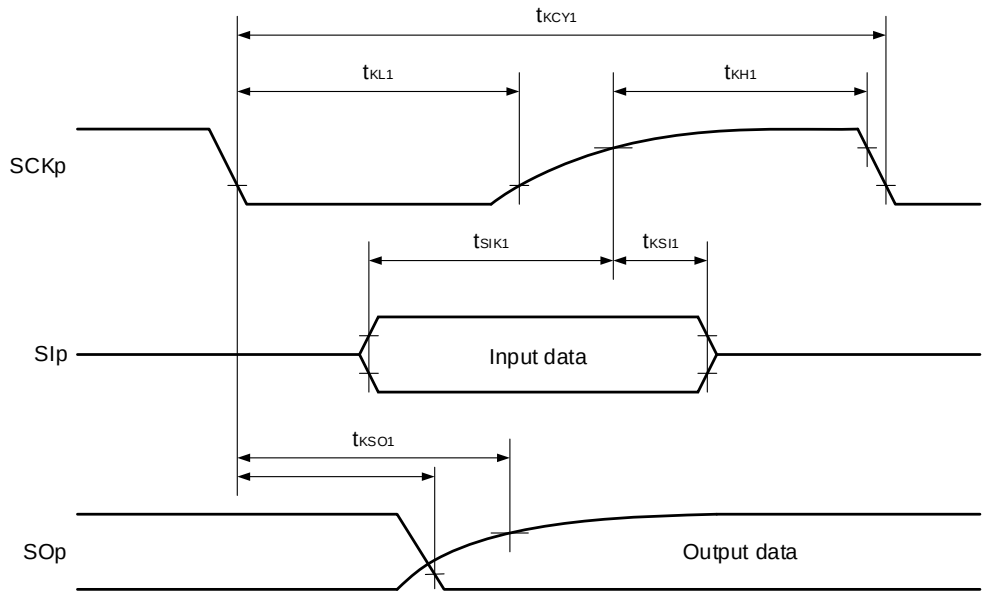
Caution Select TTL input buffer for the SIp pin, and select N-ch open-drain output mode for the SOp and SCKp pins.

Remarks 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance,
C_b [F]: Communication line (SOp, SCKp) load capacitance,
V_b [V]: Communication line voltage

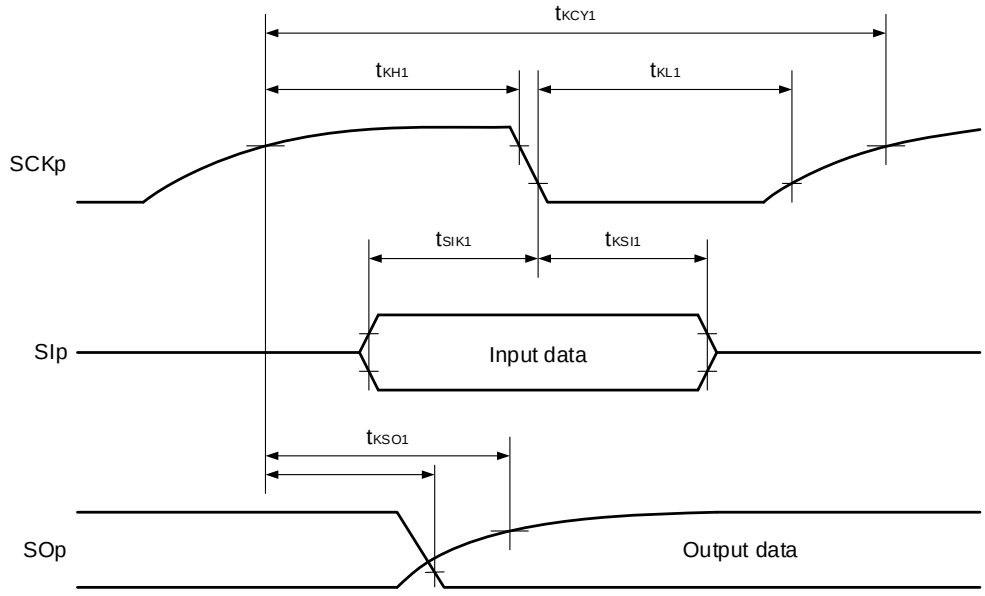
2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

CSI Mode Serial Transfer Timing (Master Mode) (During Communication at Different Potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI Mode Serial Transfer Timing (Master Mode) (During Communication at Different Potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

(10) During Communication at Different Potential (3 V Supply System) (CSI Mode) (Slave Mode, SCKp … External Clock Input, Normal Slew Rate)

($T_A = T_{OPR}$, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

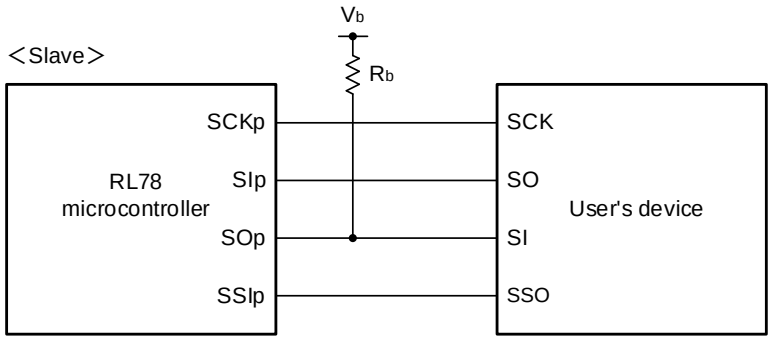
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_b ≤ V_{DD}	32 MHz < f_{MCK}				
			Grade 3 products	18/f_{MCK}			ns
			Grade 4 products	20/f_{MCK}			ns
			24 MHz < f_{MCK} ≤ 32 MHz				
			Grade 3 products	14/f_{MCK}			ns
			Grade 4 products	16/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz				
			Grade 3 products	12/f_{MCK}			ns
			Grade 4 products	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz				
			Grade 3 products	10/f_{MCK}			ns
			Grade 4 products	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz				
			Grade 3 products	8/f_{MCK}			ns
			Grade 4 products	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz				
			Grade 3 products	6/f_{MCK}			ns
			Grade 4 products	6/f_{MCK}			ns
SCKp high-level width, low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_b ≤ V_{DD}		t_{KCY2}/2 − 20			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}			90			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	2.7 V ≤ V_b ≤ V_{DD}, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
SSIp setup time	t_{SSIK}	DAP = 0		120			ns
		DAP = 1		1/f_{MCK} + 120			ns
SSIp hold time	t_{KSSI}	DAP = 0		1/f_{MCK} + 120			ns
		DAP = 1		120			ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI Mode Connection Diagram (During Communication at Different Potential)



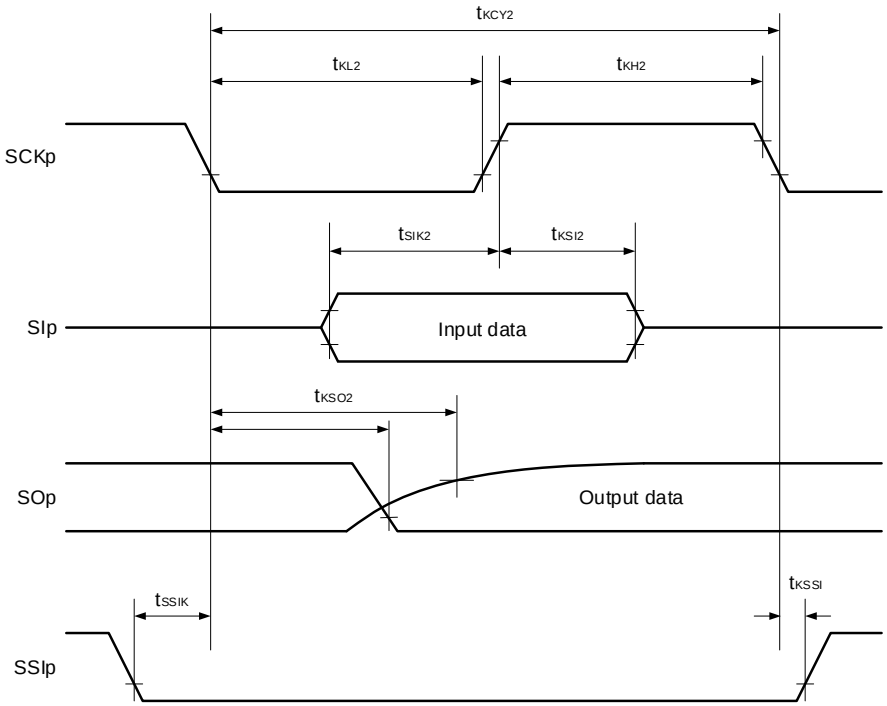
Caution Select TTL input buffer for the SIp, SCKp and SSIp pins, and select N-ch open-drain output mode for the SOp pin.

Remarks 1. R_b [Ω]: Communication line (SOp) pull-up resistance,
C_b [F]: Communication line (SOp) load capacitance,
V_b [V]: Communication line voltage

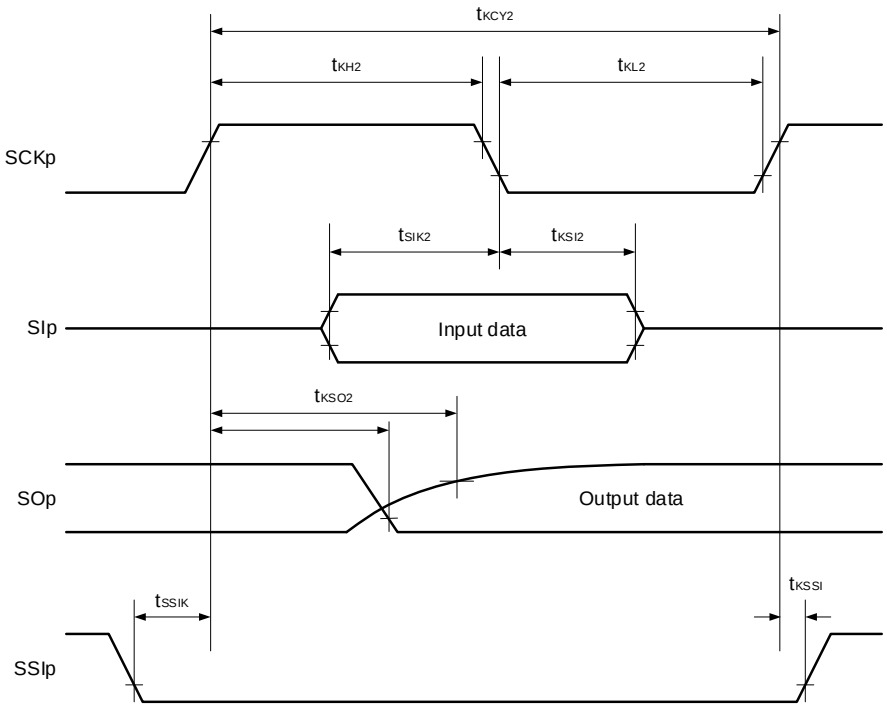
2. p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

3. AC characteristics of the serial array unit during communication at different potential in CSI mode are measured with the V_{IH} and V_{IL} below:
When 4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

CSI Mode Serial Transfer Timing (Slave Mode) (During Communication at Different Potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI Mode Serial Transfer Timing (Slave Mode) (During Communication at Different Potential)
(When DAPmn= 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



Remark p: CSIp (p = 00, 01, 10, 11), m: Unit m (m = 0, 1), n: Channel n (n = 0, 1)

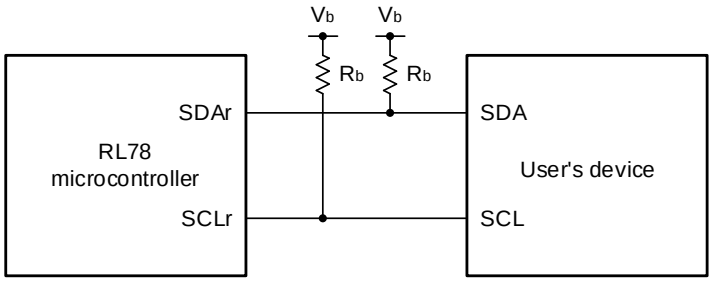
(11) During Communication at Different Potential (3 V Supply System) (Simplified I^2C Mode) (SDAr: TTL Input Buffer Mode and N-ch Open-drain Output (EV_{DD} tolerance) Mode, SCLr: N-ch Open-drain Output (EV_{DD} Tolerance) Mode)

($T_A = T_{OPR}$, 4.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

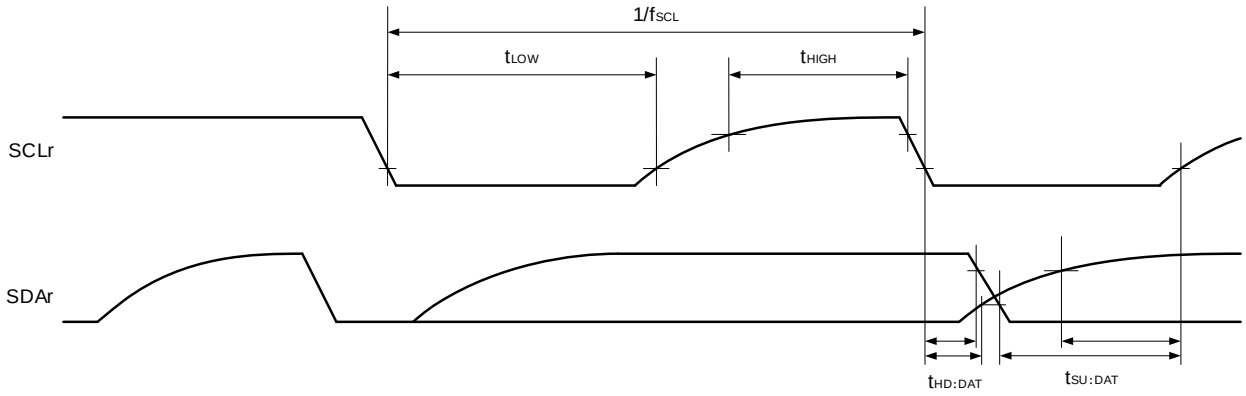
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ		400 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	1200		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	135 + 1/f_{MCK}		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 1.4 kΩ	0	140	ns

Note $f_{SCL} \le f_{MCK}/4$ must also be satisfied.

Simplified I^2C Mode Connection Diagram (During Communication at Different Potential)



Simplified I^2C Mode Serial Transfer Timing (During Communication at Different Potential)



Caution Select TTL input buffer and N-ch open-drain output mode for the SDAr pin, and select N-ch open-drain output mode for the SCLr pin.

Remarks 1. R_b [Ω]: Communication line (SDAr, SCLr) pull-up resistance,
C_b [F]: Communication line (SDAr, SCLr) load capacitance,
V_b [V]: Communication line voltage

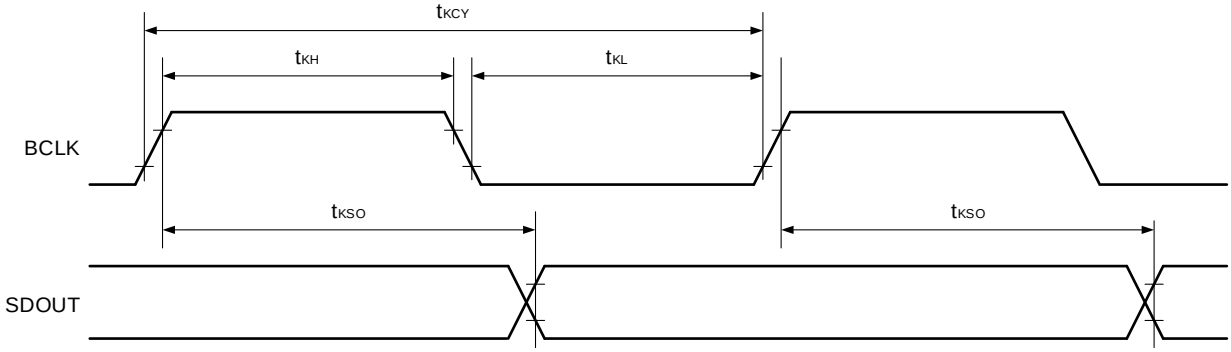
2. f_{MCK}: Serial array unit operation clock frequency

(12) During Communication at Same Potential (Simplified I²S Master Transmission) (CSI Mode, Slave Transmission Mode)

($T_A = T_{OPR}$, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions Note	MIN.	TYP.	MAX.	Unit
BCLK cycle time	t_{KCY}	Data rate = 2.5 MHz		400		ns
BCLK high-level width, low-level width	t_{KH}, t_{KL}		Value greater than 0.35 t_{KCY}			ns
SDOUT output delay time	t_{KSO}				Value less than 0.80 t_{KCY}	ns

Note The CPU/peripheral hardware clock frequency (f_{CLK}) must satisfy the condition of 8 MHz to 40 MHz.



Caution Set the I2SEN bit in the I2SER register to 1 (enable simple I2S communication function) and the TO121 and TO120 bits in the PWMDLY2 register to 01B (TO12 output is delayed by one cycle of f_{CLK}).

Remarks 1. BCLK: TO12 output of timer array unit 1, channel 2
SDOUT: SO10 output of serial array unit 1, channel 0
LRCLK: TO13 output of timer array unit 1, channel 3

2. Serial array unit 1, channel 0: CSI mode, slave transmission mode
Timer array unit 1, channel 2: Interval timer mode
Timer array unit 1, channel 3: External event counter mode

4.5.2 Serial Interface IICA

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Normal Mode		Fast Mode		Fast Mode Plus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus Note 3: 10 MHz ≤ f_{MCK}					0	1000	kHz
		Fast mode: 3.5 MHz ≤ f_{MCK}			0	400			kHz
		Normal mode: 1 MHz ≤ f_{MCK}	0	100					kHz
Setup time of restart condition Note 1	$t_{SU:STA}$		4.7		0.6		0.26		µs
Hold time	$t_{HD:STA}$		4.0		0.6		0.26		µs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		0.5		µs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		0.26		µs
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$		0	3.45	0	0.9	0		µs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		µs
Bus-free time	t_{BUF}		4.7		1.3		0.5		µs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

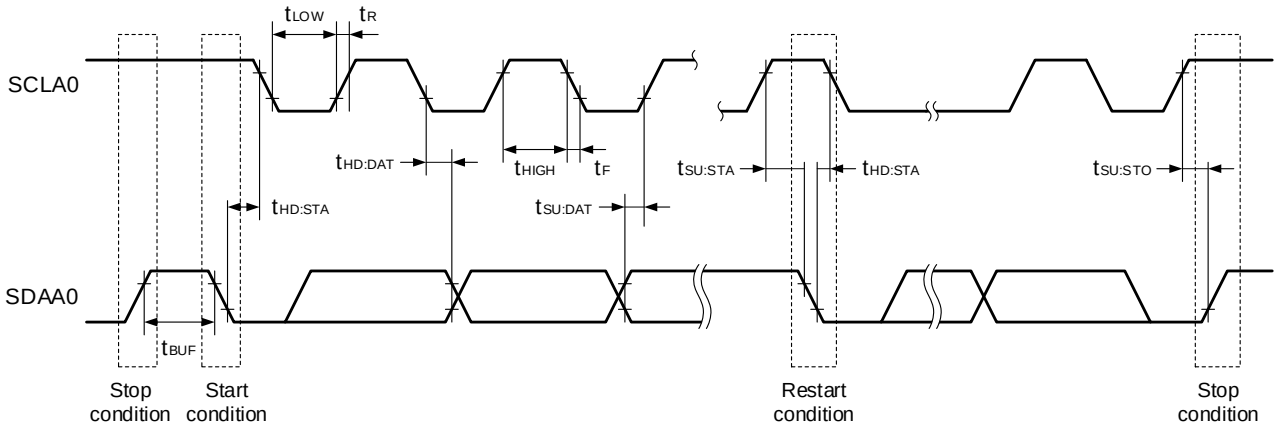
3. Fast mode plus is only available when 2.7 V ≤ V_{DD} ≤ 5.5 V.

Caution Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA Serial Transfer Timing



4.5.3 On-chip Debug (UART)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	–		115.2 k		1 M	bps

Caution Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

4.5.4 LIN/UART Module (RLIN3) UART Mode

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate	–	2.7 V ≤ V_{DD} ≤ 5.5 V	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 MHz to 40 MHz			4000	kbps
			SNOOZE mode	LIN communication clock source (f_{CLK}): 2 MHz to 40 MHz			9.6	
		1.8 V ≤ V_{DD} < 2.7 V	Operation mode, HALT mode	LIN communication clock source (f_{CLK} or f_{MX}): 4 MHz to 16 MHz			2666	
			SNOOZE mode	LIN communication clock source (f_{CLK}): 2 MHz to 16 MHz			9.6	

Caution Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

4.6 Analog Characteristics

4.6.1 A/D Converter Characteristics

- When Reference voltage (+) = AV_{REFP}, Reference voltage (−) = AV_{REFM} = 0 V.
- Target ANI pin: ANI0 to ANI10, ANI22 to ANI27, Internal reference voltage (+).
- Conversion mode: High-speed conversion mode, Low-current conversion mode

(1) High-speed Conversion Mode

($T_A = T_{OPR}$, 2.7 V ≤ $AV_{DD} = V_{DD}$ ≤ 5.5 V, $AV_{SS} = V_{SS}$ = 0 V, Reference Voltage (+) = AV_{REFP}, Reference Voltage (−) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				12	bit
Overall error Note 1	ABS	ANI0 to ANI10 Note 2, [4.5 V ≤ AV_{REFP}/AV_{DD} ≤ 5.5 V]			±5.0	LSB
		ANI0 to ANI10 Note 2, [2.7 V ≤ AV_{REFP}/AV_{DD} < 4.5 V]			±5.0	LSB
		ANI1, ANI2 Note 3, [4.5 V ≤ AV_{REFP}/AV_{DD} ≤ 5.5 V] [0.25 V ≤ V_{AIN} ≤ AV_{DD} − 0.25 V]			±6.0	LSB
		ANI1, ANI2 Note 3, [2.7 V ≤ AV_{REFP}/AV_{DD} < 4.5 V] [0.25 V ≤ V_{AIN} ≤ AV_{DD} − 0.25 V]			±8.0	LSB
		ANI22 to ANI27, [4.5 V ≤ AV_{REFP}/AV_{DD} ≤ 5.5 V]			±11	LSB
		ANI22 to ANI27, [2.7 V ≤ AV_{REFP}/AV_{DD} < 4.5 V]			±13	LSB
Integral linearity error Note 1	INL	ANI0 to ANI10			±3.0	LSB
		ANI22 to ANI27			±7.0	LSB
Differential linearity error Note 1	DNL	ANI0 to ANI10			±1.5	LSB
		ANI22 to ANI27			±3.5	LSB
Zero-scale error Note 1	ZSE	ANI0 to ANI10 Note 2			±4.5	LSB
		ANI22 to ANI27			±8.5	LSB
Full-scale error Note 1	FSE	ANI0 to ANI10 Note 2			±4.5	LSB
		ANI22 to ANI27			±8.5	LSB
Reference voltage (+)	AV_{REFP}		2.7		V_{DD}	V
Analog input voltage	V_{AIN}	ANI0 to ANI10, ANI22 to ANI27	0		AV_{REFP}	V
Internal reference voltage (+)	V_{BGR}	2.7 V ≤ V_{DD} ≤ 5.5 V	1.42	1.48	1.54	V
Analog input slew rate	SR				0.4	V/µs
Operation clock	f_{AD}		2		40	MHz
Conversion time Note 4 (per 1 channel)	t_{CONV}	ADCLK = 40 MHz, input impedance ≤ 0.5 kΩ				
		ANI0 to ANI10 Note 2	1.125			µs
		ANI22 to ANI27	1.8			µs
		ANI1, ANI2 Note 3	1.85			µs

Notes 1. Excludes quantization error (±1/2 LSB).

2. In case that dedicated sample & hold circuit is not used.

3. In case that dedicated sample & hold circuit is used.

4. The A/D conversion processing time (t_{CONV}) consists of sampling time and time for conversion by successive approximation.

(2) Low-current Conversion Mode

($T_A = T_{OPR}$, $1.8\ V \le AV_{DD} = V_{DD} < 2.7\ V$, $AV_{SS} = V_{SS} = 0\ V$, Reference Voltage (+) = AV_{REFP}, Reference Voltage (−) = $AV_{REFM} = 0\ V$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				12	bit
Overall error Note 1	ABS	ANI0 to ANI10, [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			9.0	LSB
		ANI22 to ANI27, [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			13	LSB
Integral linearity error Note 1	INL	ANI0 to ANI10, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			4.0	LSB
		ANI22 to ANI27, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			7.0	LSB
Differential linearity error Note 1	DNL	ANI0 to ANI10, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			2.5	LSB
		ANI22 to ANI27, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			3.5	LSB
Zero-scale error Note 1	ZSE	ANI0 to ANI10 Note 2, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			8.0	LSB
		ANI22 to ANI27, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			10.5	LSB
Full-scale error Note 1	FSE	ANI0 to ANI10 Note 2, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			8.0	LSB
		ANI22 to ANI27, [$AV_{REFP} = V_{DD}$], [1.8 V ≤ $AV_{REFP} = AV_{DD}$ < 2.7 V]			10.5	LSB
Reference voltage (+)	AV_{REFP}		1.8		V_{DD}	V
Analog input voltage	V_{AIN}	ANI0 to ANI10, ANI22 to ANI27	0		AV_{REFP}	V
Internal reference voltage (+)	V_{BGR}	1.8 V ≤ V_{DD} < 2.7 V	1.42	1.48	1.54	V
Operation clock	f_{AD}		2		8	MHz
Conversion time Note 2 (per 1 channel)	t_{CONV}	ADCLK = 8 MHz, input impedance ≤ 0.5 kΩ				
		ANI0 to ANI10	6.75			µs
		ANI22 to ANI27	7.63			µs

Notes 1. Excludes quantization error (±1/2 LSB).

2. The A/D conversion processing time (t_{CONV}) consists of sampling time and time for conversion by successive approximation.

Cautions 1. Operating voltage condition: $1.8\ V \le AV_{DD} = V_{DD} < 2.7\ V$ is only available for Grade 3 products.

2. The sample and hold circuit cannot be used when $1.8\ V \le V_{DD} < 2.7\ V$.

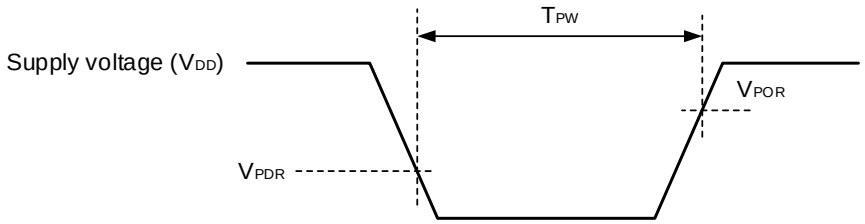
4.6.2 POR Circuit Characteristics

($T_A = T_{OPR}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage Note 1	V_{POR}, V_{PDR}		1.43	1.50	1.57	V
Minimum pulse width Note 2	T_{PW}		300			µs
Detection delay time	T_{PD}				350	µs

Notes 1. This indicates the POR circuit characteristics, and normal operation is not guaranteed under the condition of less than lower limit operation voltage (1.8 V).

2. Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}.



4.6.3 LVD Circuit Characteristics

(1) LVD0 Detection Voltage of Reset Mode

($T_A = T_{OPR}$, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD00}	Power supply rise time	3.84	3.96	4.08	V
			Power supply fall time	3.76	3.88	4.00	V
		V_{LVD01}	Power supply rise time	2.88	2.97	3.06	V
			Power supply fall time	2.82	2.91	3.00	V
		V_{LVD02} Note	Power supply rise time	1.84	1.90	1.95	V
			Power supply fall time	1.80	1.86	1.91	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time		t_{LD}				500	µs

Note This setting is available only for Grade 3 products (T_A = −40 to +105°C) and when used with $f_{CLK} \le 16$ MHz.

(2) LVD1 Detection Voltage of Interrupt Mode

($T_A = T_{OPR}$, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD10}	Power supply rise time	4.08	4.16	4.24	V
			Power supply fall time	4.00	4.08	4.16	V
		V_{LVD11}	Power supply rise time	3.88	3.96	4.04	V
			Power supply fall time	3.80	3.88	3.96	V
		V_{LVD12}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD13}	Power supply rise time	3.48	3.55	3.62	V
			Power supply fall time	3.40	3.47	3.54	V
		V_{LVD14}	Power supply rise time	3.28	3.35	3.42	V
			Power supply fall time	3.20	3.27	3.34	V
		V_{LVD15}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD16}	Power supply rise time	2.91	2.97	3.03	V
			Power supply fall time	2.85	2.91	2.97	V
		V_{LVD17}	Power supply rise time	2.76	2.82	2.87	V
			Power supply fall time	2.70	2.76	2.81	V
		V_{LVD113} Note	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD114} Note	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD115} Note	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time		t_{LD}				500	µs

Note This setting is available only for Grade 3 products (T_A = −40 to +105°C) and when used with $f_{CLK} \le 16$ MHz.

4.7 Power Supply Voltage Rising Time

($T_A = T_{OPR}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum power supply voltage rising slope Note 1	S_{vrmax}	0 V → V_{DD} (LVD0ENB = 0 or 1 Note 2)			50 Note 3	V/ms

Notes 1. Maintain the reset state by the voltage detection circuit (LVD0) or external reset up to the operating voltage range.

2. These values indicate setting values of option bytes.

3. If the power supply drops below V_{PDR} and a POR reset is effected, this specification is also applied when the power supply is recovered without dropping to 0 V.

4.8 Regulator Output Voltage Characteristics

($T_A = T_{OPR}$, V_{SS} = 0 V)

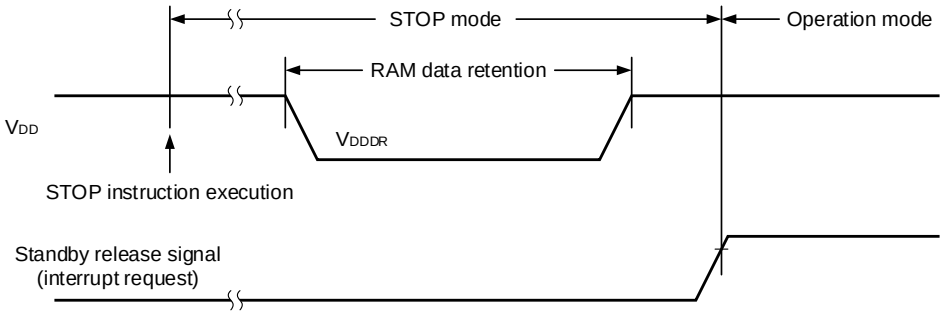
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
REGC output voltage	V_{OREGC}	C = 0.47 to 1 µF	1.45	1.50	1.56	V

4.9 RAM Data Retention Characteristics

($T_A = T_{OPR}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 Note		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



4.10 Flash Memory Programming Characteristics

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		2		40	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years, T_A = +85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 20 years, T_A = +85°C Note 4	10,000			
		Retained for 5 years, T_A = +85°C Note 4	100,000			
Erase time	Terasa	Block erase	5			ms
Write time	Twrwa	1 word write	10			µs

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The starting point of the retaining years are after the erase.

2. When using flash memory programmer and Renesas Electronics self programming code.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

4. The average temperature for data retention.

Caution Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

(1) Code Flash Memory Processing Time

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		f_{CLK} = 2 MHz		f_{CLK} = 4 MHz		f_{CLK} = 8 MHz		f_{CLK} = 16 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	4 bytes	52.0	470.0	43.0	400.0	38.0	360.0	36.0	340.0	µs
Erasure time	2 KB	7.8	265.0	6.5	240.0	5.9	225.0	5.8	220.0	ms
Blank checking time	4 bytes	–	19.2	–	13.2	–	10.3	–	9.1	µs
	2 KB	–	1310.0	–	660.0	–	335.0	–	270.0	µs

Item		f_{CLK} = 20 MHz		f_{CLK} = 32 MHz		f_{CLK} = 40 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	4 bytes	36.0	340.0	35.0	330.0	35.0	330.0	µs
Erasure time	2 KB	5.8	220.0	5.7	220.0	5.7	220.0	ms
Blank checking time	4 bytes	–	8.9	–	8.5	–	8.5	µs
	2 KB	–	270.0	–	245.0	–	245.0	µs

Cautions 1. The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2. Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

(2) Data Flash Memory Processing Time

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		f_{CLK} = 2 MHz		f_{CLK} = 4 MHz		f_{CLK} = 8 MHz		f_{CLK} = 16 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	1 byte	52.0	470.0	43.0	400.0	38.0	360.0	36.0	340.0	µs
Erasure time	1 KB	10.4	320.0	7.8	265.0	6.5	240.0	6.3	235.0	ms
Blank checking time	1 byte	–	19.2	–	13.2	–	10.3	–	9.1	µs
	1 KB	–	2605.0	–	1305.0	–	660.0	–	530.0	µs

Item		f_{CLK} = 20 MHz		f_{CLK} = 32 MHz		f_{CLK} = 40 MHz		Unit
	Conditions	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.	
Programming time	1 byte	36.0	340.0	35.0	330.0	35.0	330.0	µs
Erasure time	1 KB	6.3	235.0	6.2	230.0	6.2	230.0	ms
Blank checking time	1 byte	–	8.9	–	8.5	–	8.5	µs
	1 KB	–	530.0	–	475.0	–	475.0	µs

Cautions 1. The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2. Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

4.11 Dedicated Flash Memory Programmer Communication (UART)

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate	–	During serial programming	115.2 k		1 M	bps

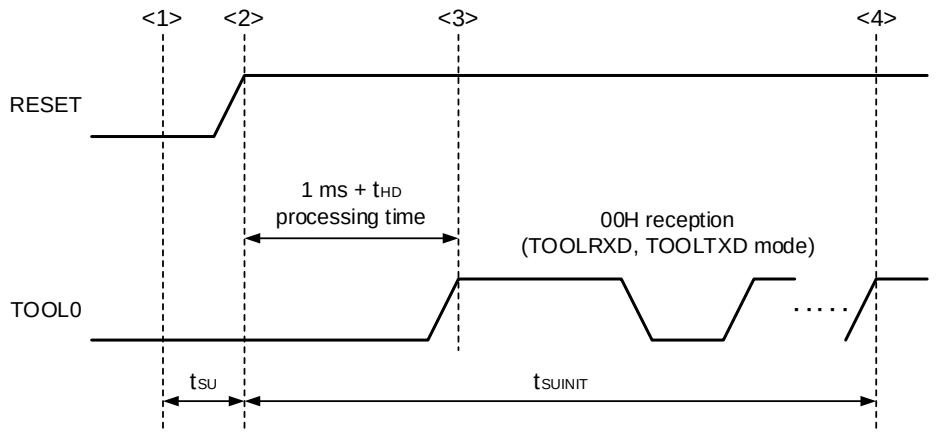
Caution Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.

4.12 Timing of Entry to Flash Memory Programming Modes

($T_A = T_{OPR}$, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms

Caution Operating voltage condition: 1.8 V ≤ V_{DD} < 2.7 V is only available for Grade 3 products.



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period

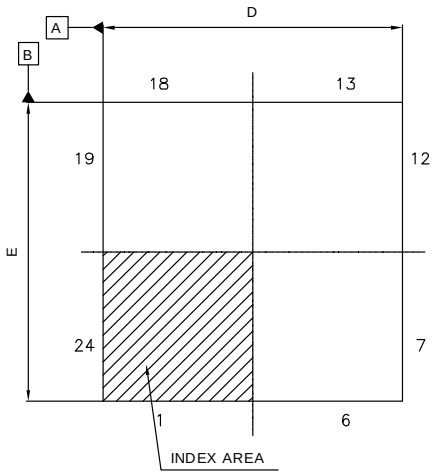
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

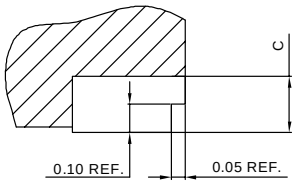
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

5. PACKAGE DRAWINGS

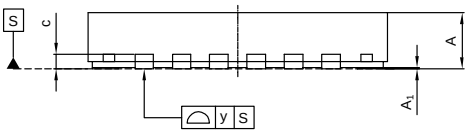
5.1 24-pin Products

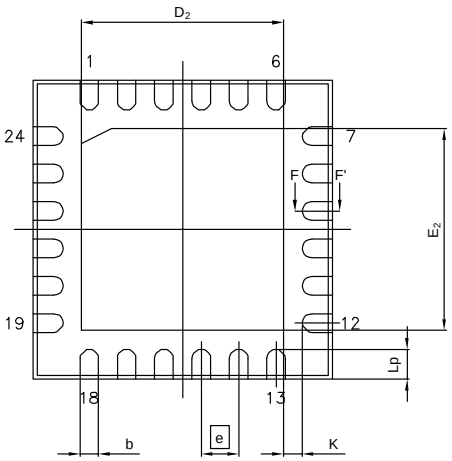
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KJ-A	0.04





TERMINAL CROSS SECTION F-F'

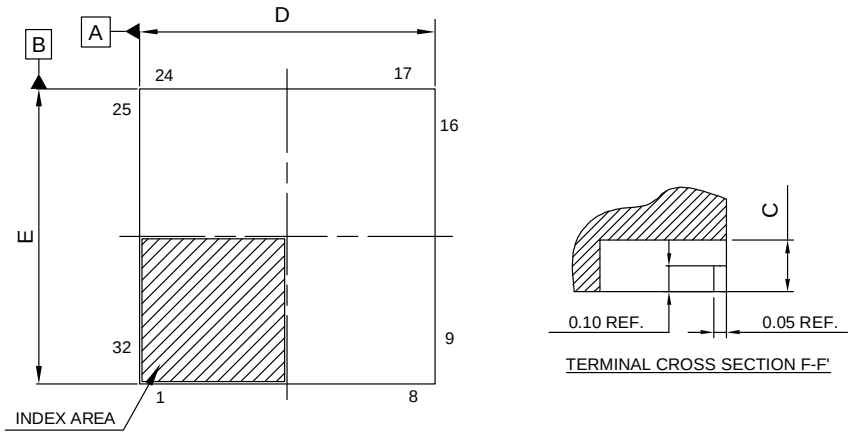


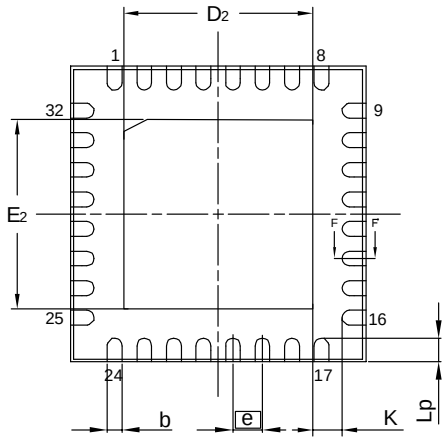


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	3.85	4.00	4.15
E	3.85	4.00	4.15
A	—	—	0.80
A_1	0.00	—	0.05
b	0.18	0.25	0.30
e		0.50 BSC	
Lp	0.35	0.40	0.45
y	—	—	0.08
c	—	0.20	—
K	0.20	—	—
D_2	—	2.70	—
E_2	—	2.70	—

5.2 32-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KH-A	0.06

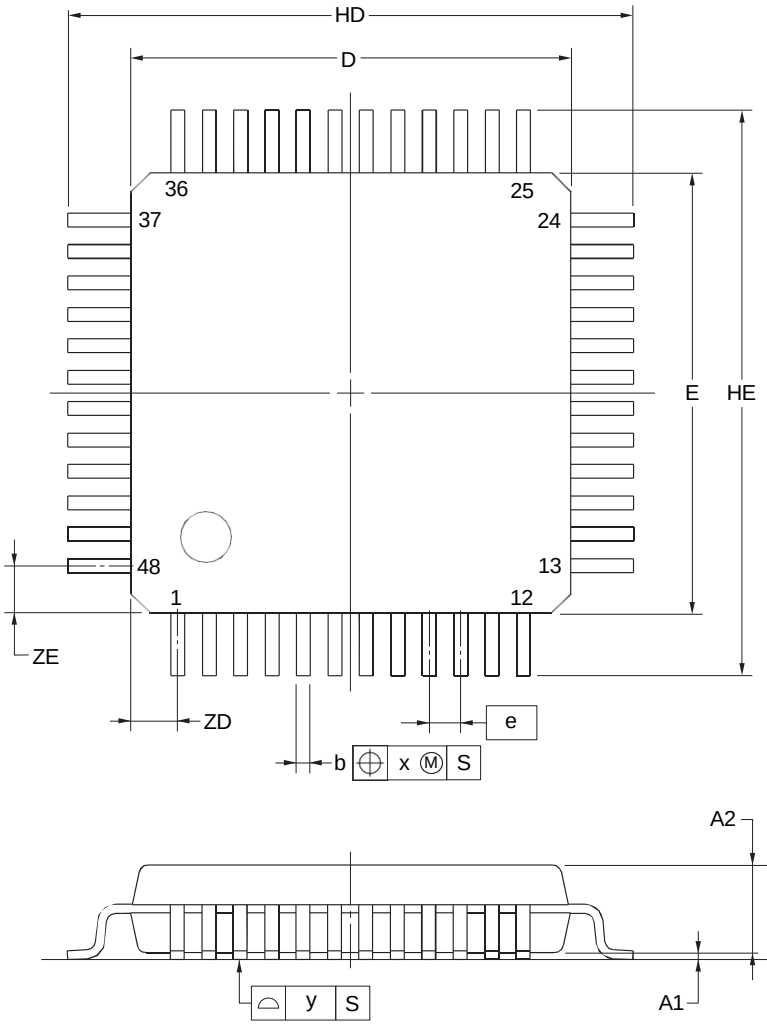


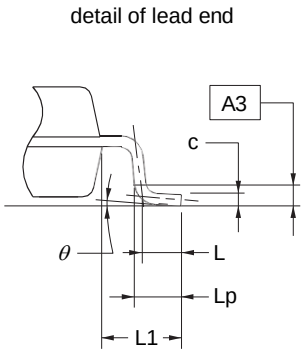


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	4.85	5.00	5.15
E	4.85	5.00	5.15
A	—	—	0.80
A_1	0.00	—	0.05
b	0.18	0.25	0.30
e	0.50 BSC		
Lp	0.35	0.40	0.45
y	—	—	0.08
c	—	0.20	—
K	0.20	—	—
D_2	—	3.20	—
E_2	—	3.20	—

5.3 48-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16





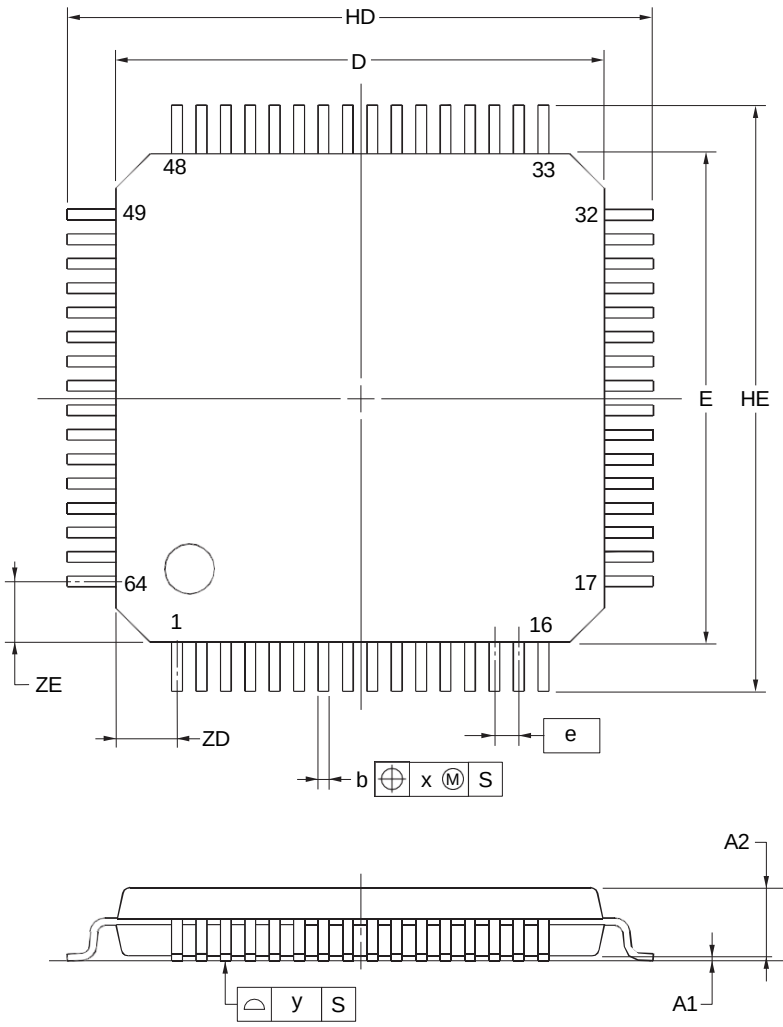
(UNIT:mm)

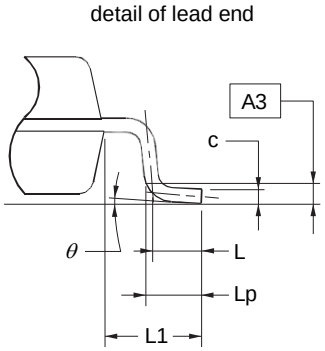
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

5.4 64-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35





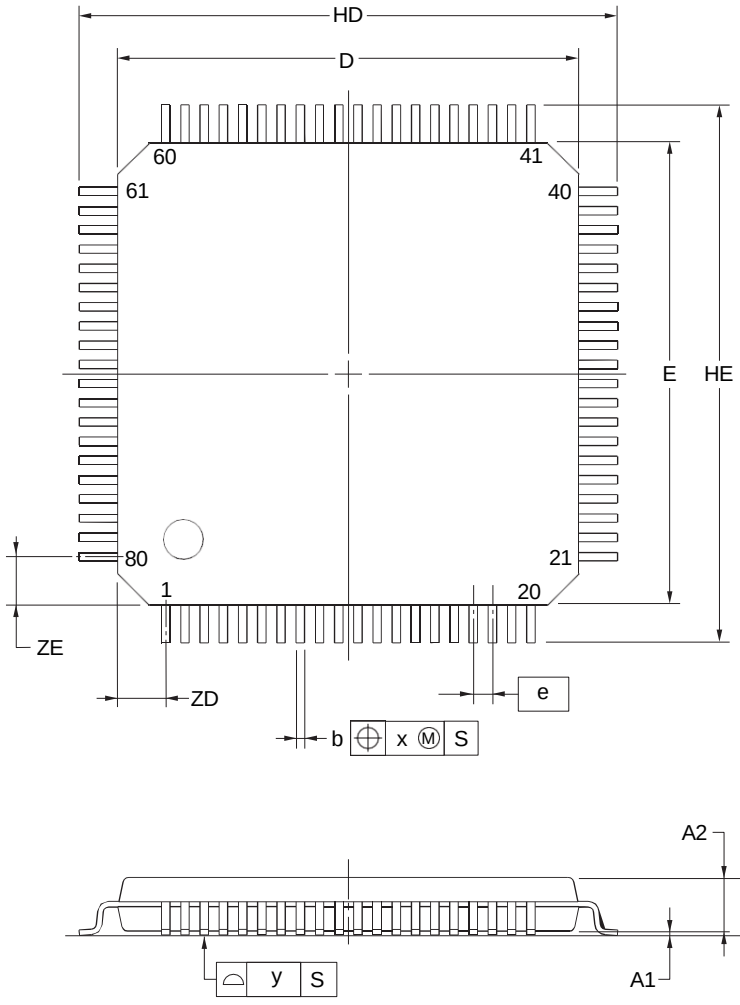
(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

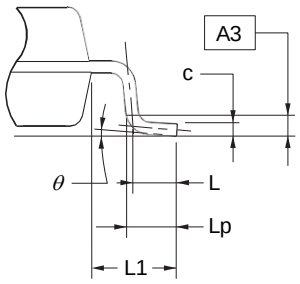
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

5.5 80-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



detail of lead end



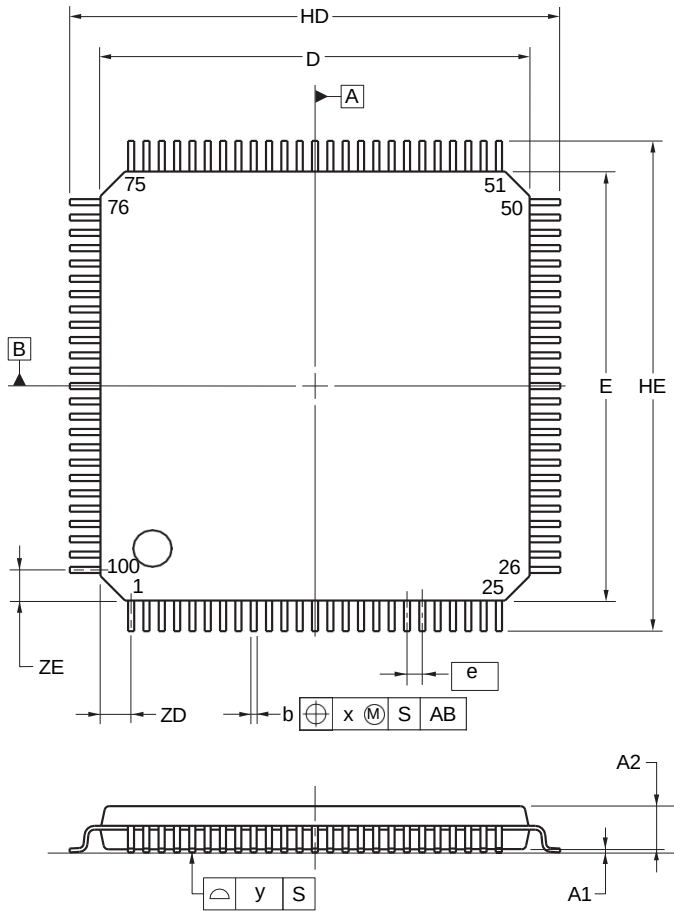
(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

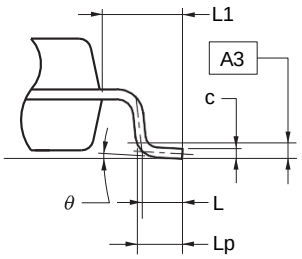
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

5.6 100-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22 ±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

REVISION HISTORY	RL78/F22, F25 Datasheet

Rev	Date	Description	
		Page	Summary
1.20	Jun 30, 2025	p.50	3.3.1 (6/6), corrected corresponding pins for positive injected current, and deleted “Note 2” below the table.
		p.83	3.6.3, corrected the description in the comparator characteristics table.
		p.101	4.3.1 (6/6), corrected corresponding pins for positive injected current.
1.10	Mar 31, 2025	–	First edition issued.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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