

RL78/G21

R01DS0517EJ0100

RENESAS MCU

Rev.1.00

May 20, 2026

True low-power platform, 34.4- μ A/MHz operating current, 230-nA stop current, 128- to 256-KB code flash memory and 8-KB RAM, from 20 to 64 pins, 1.6- to 5.5-V operation

1. Outline

1.1 Features

Ultra-low power consumption technology

- Operation from a single power supply (VDD) within the 1.6-V to 5.5-V range
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- The minimum instruction execution time can be changed from high to ultra-low speed.
 - High speed: 0.03125 μ s at 32-MHz operation with the high-speed on-chip oscillator clock
 - Ultra-low speed: 30.5 μ s at 32.768-kHz operation with the subsystem clock
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register $\times$ 8) $\times$ 4 banks
- On-chip RAM: 8 KB

Code flash memory

- Code flash memory: 128 or 256 KB
- Block size: 2 KB
- Security function: Prohibition of block erase and rewriting
- On-chip debugging
- Self-programming with boot swapping and flash shield window

Data flash memory

- Data flash memory: 4 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator

- Selectable from among 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: $\pm 1.0\%$
(VDD = 1.6 to 5.5 V, TA = -40 to +105°C)

Low-speed on-chip oscillator

- 32.768 kHz (typ.)

Operating ambient temperature

- TA = -40 to +105°C
(3Z: Industrial and consumer applications)

Power management and reset function

- Power-on-reset circuit (POR)
- Voltage detectors (LVD0 and LVD1)

Serial interface

- Simplified SPI (CS|**Note 1**): 2 to 6 channels
- UART/UART (LIN-bus supported)/UARTA: 4 channels
- I²C/Simplified I²C: 2 to 7 channels

Timers

- 16-bit timer: 8 channels
- 32-bit interval timer:
 - 1 channel in 32-bit counter mode
 - 2 channels in 16-bit counter mode
 - 4 channels in 8-bit counter mode
- Watchdog timer: 1 channel (operates with the low-speed on-chip oscillator clock)

A/D converter

- 8-/10-bit resolution
- Analog input: 6 to 12 channels
- Internal reference voltage (1.48 V (typ.)) and temperature sensor

Input/output port pins

- Number of port pins: 17 to 59
- N-ch open-drain I/O (withstand voltage of 6 V):
0 to 2
N-ch open-drain I/O (withstand voltage of V_{DD} ^{Note 2}/withstand voltage of EV_{DD} ^{Note 3}):
5 to 19
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8, 2.5, or 3 V)

Others

- Key interrupt input
- Binary-coded decimal (BCD) correction circuit

Note 1. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Note 2. This applies to the 20- to 48-pin products.

Note 3. This applies to the 64-pin products.

Remark The functions mounted depend on the product. For details, see **1.6 Outline of Functions**.

O ROM, RAM capacities

Code flash memory	Data flash memory	RAM	RL78/G21				
			20 pins	32 pins	44 pins	48 pins	64 pins
256 KB	4 KB	8 KB	R7F103G6J	R7F103GBJ	R7F103GFJ	R7F103GGJ	R7F103GLJ
128 KB	4 KB	8 KB	R7F103G6G	R7F103GBG	R7F103GFG	R7F103GGG	R7F103GLG

1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G21

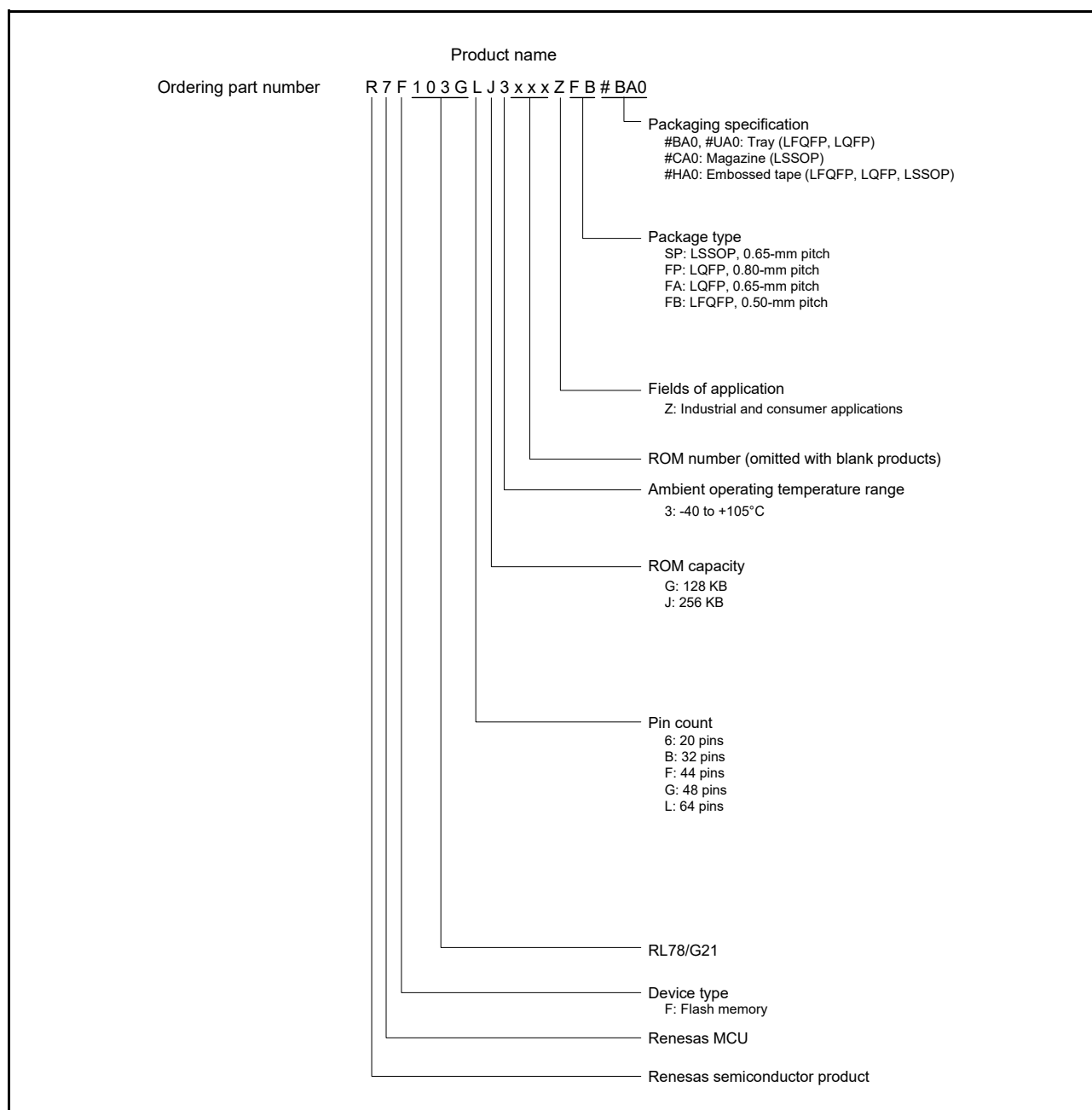


Table 1 - 1 List of Ordering Part Numbers

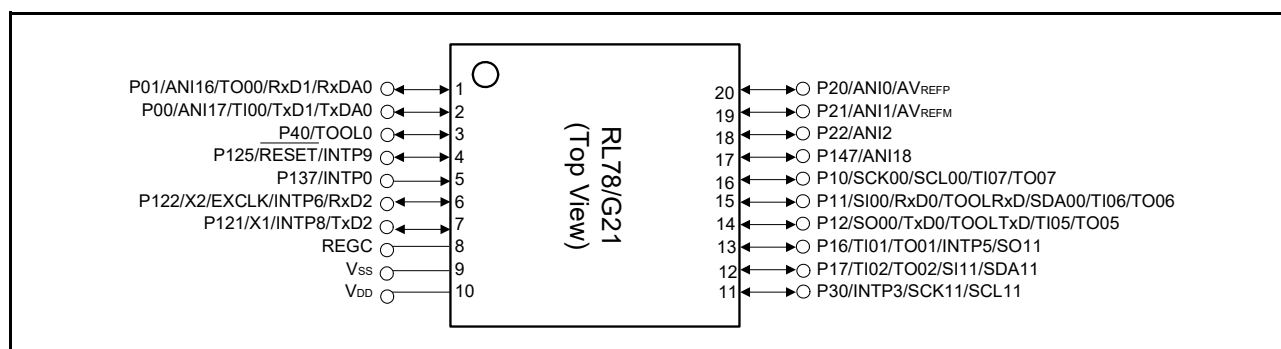
Pin Count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
20	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)	Z	R7F103G6J3ZSP, R7F103G6G3ZSP	#CA0, #HA0	PLSP0020JB-A
32	32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)	Z	R7F103GBJ3ZFP, R7F103GBG3ZFP	#BA0, #UA0, #HA0	PLQP0032GB-A
44	44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)	Z	R7F103GFJ3ZFP, R7F103GFG3ZFP	#BA0, #UA0, #HA0	PLQP0044GF-A
48	48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)	Z	R7F103GGJ3ZFB, R7F103GGG3ZFB	#BA0, #UA0, #HA0	PLQP0048KB-B
64	64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)	Z	R7F103GLJ3ZFA, R7F103GLG3ZFA	#BA0, #UA0, #HA0	PLQP0064JB-A
	64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)	Z	R7F103GLJ3ZFB, R7F103GLG3ZFB	#BA0, #UA0, #HA0	PLQP0064KB-C

Note For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G21**.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

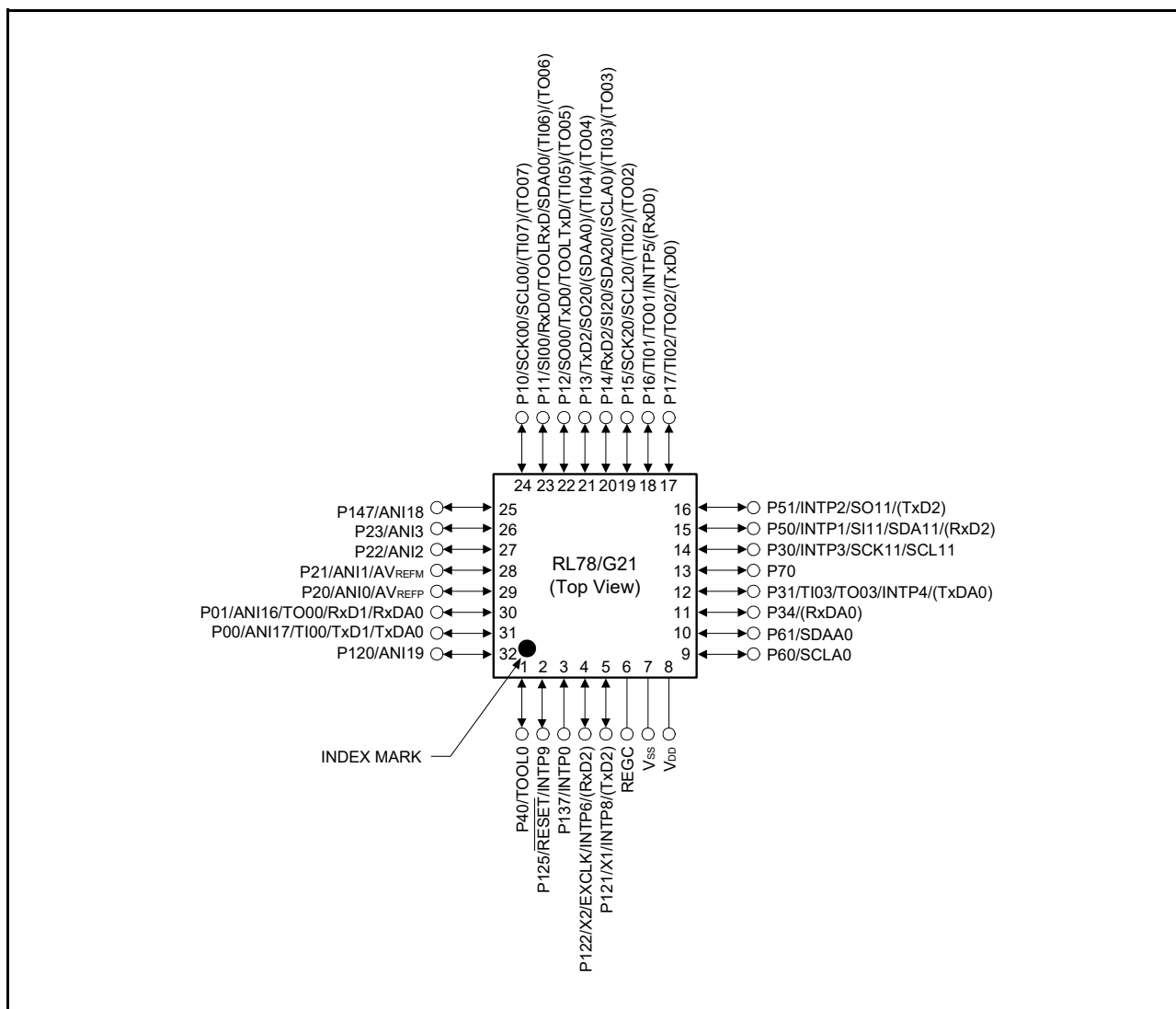
Remark For pin identification, see 1.4 Pin Identification.

Table 1 - 2 Multiplexed Pin Functions of the 20-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
20LSSOP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P01	—	ANI16	—	—	TO00	RxD1	—	RxDA0
2	P00	—	ANI17	—	—	TI00	TxD1	—	TxDA0
3	P40	TOOL0	—	—	—	—	—	—	—
4	P125	RESET	—	INTP9	—	—	—	—	—
5	P137	—	—	INTP0	—	—	—	—	—
6	P122	X2/EXCLK	—	INTP6	—	—	RxD2	—	—
7	P121	X1	—	INTP8	—	—	TxD2	—	—
8	—	REGC	—	—	—	—	—	—	—
9	—	Vss	—	—	—	—	—	—	—
10	—	VDD	—	—	—	—	—	—	—
11	P30	—	—	INTP3	—	—	SCK11/SCL11	—	—
12	P17	—	—	—	—	TI02/TO02	SI11/SDA11	—	—
13	P16	—	—	INTP5	—	TI01/TO01	SO11	—	—
14	P12	TOOLTxD	—	—	—	TI05/TO05	SO00/TxD0	—	—
15	P11	TOOLRxD	—	—	—	TI06/TO06	SI00/RxD0/ SDA00	—	—
16	P10	—	—	—	—	TI07/TO07	SCK00/SCL00	—	—
17	P147	—	ANI18	—	—	—	—	—	—
18	P22	—	ANI2	—	—	—	—	—	—
19	P21	—	ANI1/AVREFM	—	—	—	—	—	—
20	P20	—	ANI0/AVREFP	—	—	—	—	—	—

1.3.2 32-pin products

- 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

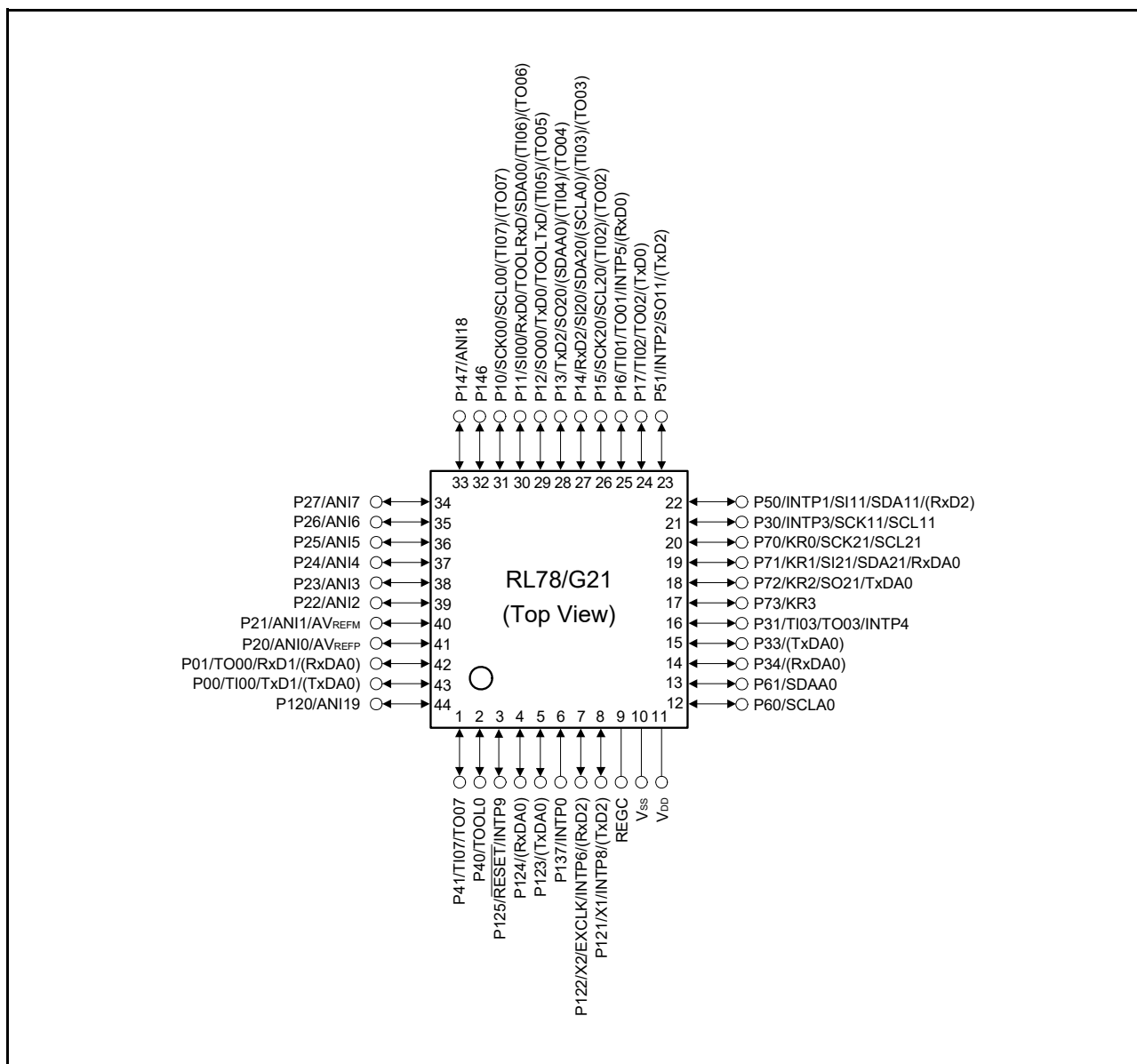
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the corresponding peripheral I/O redirection register (PIORx). For details, see 4.3.8 Peripheral I/O redirection registers (PIORx) in the RL78/G21 User's Manual.

Table 1 - 3 Multiplexed Pin Functions of the 32-pin Products

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
32LQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	TOOL0	—	—	—	—	—	—	—
2	P125	RESET	—	INTP9	—	—	—	—	—
3	P137	—	—	INTP0	—	—	—	—	—
4	P122	X2/EXCLK	—	INTP6	—	—	(RxD2)	—	—
5	P121	X1	—	INTP8	—	—	(TxD2)	—	—
6	—	REGC	—	—	—	—	—	—	—
7	—	Vss	—	—	—	—	—	—	—
8	—	VDD	—	—	—	—	—	—	—
9	P60	—	—	—	—	—	—	SCLA0	—
10	P61	—	—	—	—	—	—	SDAA0	—
11	P34	—	—	—	—	—	—	—	(RxDA0)
12	P31	—	—	INTP4	—	TI03/TO03	—	—	(TxDA0)
13	P70	—	—	—	—	—	—	—	—
14	P30	—	—	INTP3	—	—	SCK11/SCL11	—	—
15	P50	—	—	INTP1	—	—	SI11/SDA11/ (RxD2)	—	—
16	P51	—	—	INTP2	—	—	SO11/(TxD2)	—	—
17	P17	—	—	—	—	TI02/TO02	(TxD0)	—	—
18	P16	—	—	INTP5	—	TI01/TO01	(RxD0)	—	—
19	P15	—	—	—	—	(TI02)/(TO02)	SCK20/SCL20	—	—
20	P14	—	—	—	—	(TI03)/(TO03)	SI20/RxD2/ SDA20	(SCLA0)	—
21	P13	—	—	—	—	(TI04)/(TO04)	SO20/TxD2	(SDAA0)	—
22	P12	TOOLTxD	—	—	—	(TI05)/(TO05)	SO00/TxD0	—	—
23	P11	TOOLRxD	—	—	—	(TI06)/(TO06)	SI00/RxD0/ SDA00	—	—
24	P10	—	—	—	—	(TI07)/(TO07)	SCK00/SCL00	—	—
25	P147	—	ANI18	—	—	—	—	—	—
26	P23	—	ANI3	—	—	—	—	—	—
27	P22	—	ANI2	—	—	—	—	—	—
28	P21	—	ANI1/AVREFM	—	—	—	—	—	—
29	P20	—	ANI0/AVREFP	—	—	—	—	—	—
30	P01	—	ANI16	—	—	TO00	RxD1	—	RxDA0
31	P00	—	ANI17	—	—	TI00	TxD1	—	TxDA0
32	P120	—	ANI19	—	—	—	—	—	—

1.3.3 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the corresponding peripheral I/O redirection register (PIORx). For details, see 4.3.8 Peripheral I/O redirection registers (PIORx) in the RL78/G21 User's Manual.

Table 1 - 4 Multiplexed Pin Functions of the 44-pin Products (1/2)

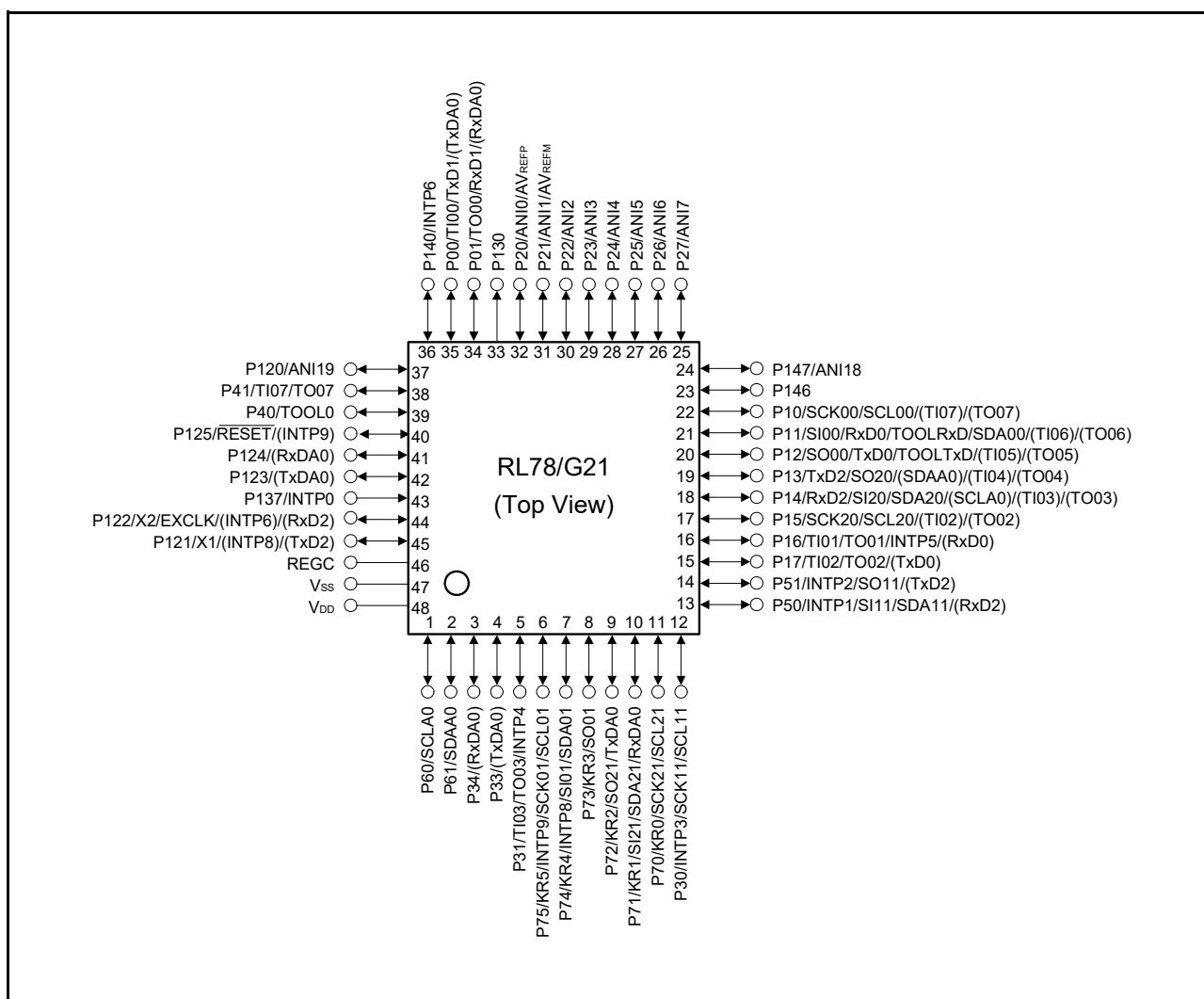
Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
44LQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P41	—	—	—	—	TI07/TO07	—	—	—
2	P40	TOOL0	—	—	—	—	—	—	—
3	P125	RESET	—	INTP9	—	—	—	—	—
4	P124	—	—	—	—	—	—	—	(RxDA0)
5	P123	—	—	—	—	—	—	—	(TxDA0)
6	P137	—	—	INTP0	—	—	—	—	—
7	P122	X2/EXCLK	—	INTP6	—	—	(Rx2D)	—	—
8	P121	X1	—	INTP8	—	—	(Tx2D)	—	—
9	—	REGC	—	—	—	—	—	—	—
10	—	Vss	—	—	—	—	—	—	—
11	—	VDD	—	—	—	—	—	—	—
12	P60	—	—	—	—	—	—	SCLA0	—
13	P61	—	—	—	—	—	—	SDAA0	—
14	P34	—	—	—	—	—	—	—	(RxDA0)
15	P33	—	—	—	—	—	—	—	(TxDA0)
16	P31	—	—	INTP4	—	TI03/TO03	—	—	—
17	P73	—	—	—	KR3	—	—	—	—
18	P72	—	—	—	KR2	—	SO21	—	TxDA0
19	P71	—	—	—	KR1	—	SI21/SDA21	—	RxDA0
20	P70	—	—	—	KR0	—	SCK21/SCL21	—	—
21	P30	—	—	INTP3	—	—	SCK11/SCL11	—	—
22	P50	—	—	INTP1	—	—	SI11/SDA11/ (Rx2D)	—	—
23	P51	—	—	INTP2	—	—	SO11/(Tx2D)	—	—
24	P17	—	—	—	—	TI02/TO02	(Tx0)	—	—
25	P16	—	—	INTP5	—	TI01/TO01	(Rx0)	—	—
26	P15	—	—	—	—	(TI02)/(TO02)	SCK20/SCL20	—	—
27	P14	—	—	—	—	(TI03)/(TO03)	SI20/RxD2/ SDA20	(SCLA0)	—
28	P13	—	—	—	—	(TI04)/(TO04)	SO20/TxD2	(SDAA0)	—
29	P12	TOOLTxD	—	—	—	(TI05)/(TO05)	SO00/TxD0	—	—
30	P11	TOOLRxD	—	—	—	(TI06)/(TO06)	SI00/RxD0/ SDA00	—	—
31	P10	—	—	—	—	(TI07)/(TO07)	SCK00/SCL00	—	—
32	P146	—	—	—	—	—	—	—	—
33	P147	—	ANI18	—	—	—	—	—	—
34	P27	—	ANI7	—	—	—	—	—	—
35	P26	—	ANI6	—	—	—	—	—	—
36	P25	—	ANI5	—	—	—	—	—	—

Table 1 - 4 Multiplexed Pin Functions of the 44-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
44LQFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
37	P24	—	ANI4	—	—	—	—	—	—
38	P23	—	ANI3	—	—	—	—	—	—
39	P22	—	ANI2	—	—	—	—	—	—
40	P21	—	ANI1/AVREFM	—	—	—	—	—	—
41	P20	—	ANI0/AVREFP	—	—	—	—	—	—
42	P01	—	—	—	—	TO00	RxD1	—	(RxDA0)
43	P00	—	—	—	—	TI00	TxD1	—	(TxDA0)
44	P120	—	ANI19	—	—	—	—	—	—

1.3.4 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the corresponding peripheral I/O redirection register (PIORx). For details, see 4.3.8 Peripheral I/O redirection registers (PIORx) in the RL78/G21 User's Manual.

Table 1 - 5 Multiplexed Pin Functions of the 48-pin Products (1/2)

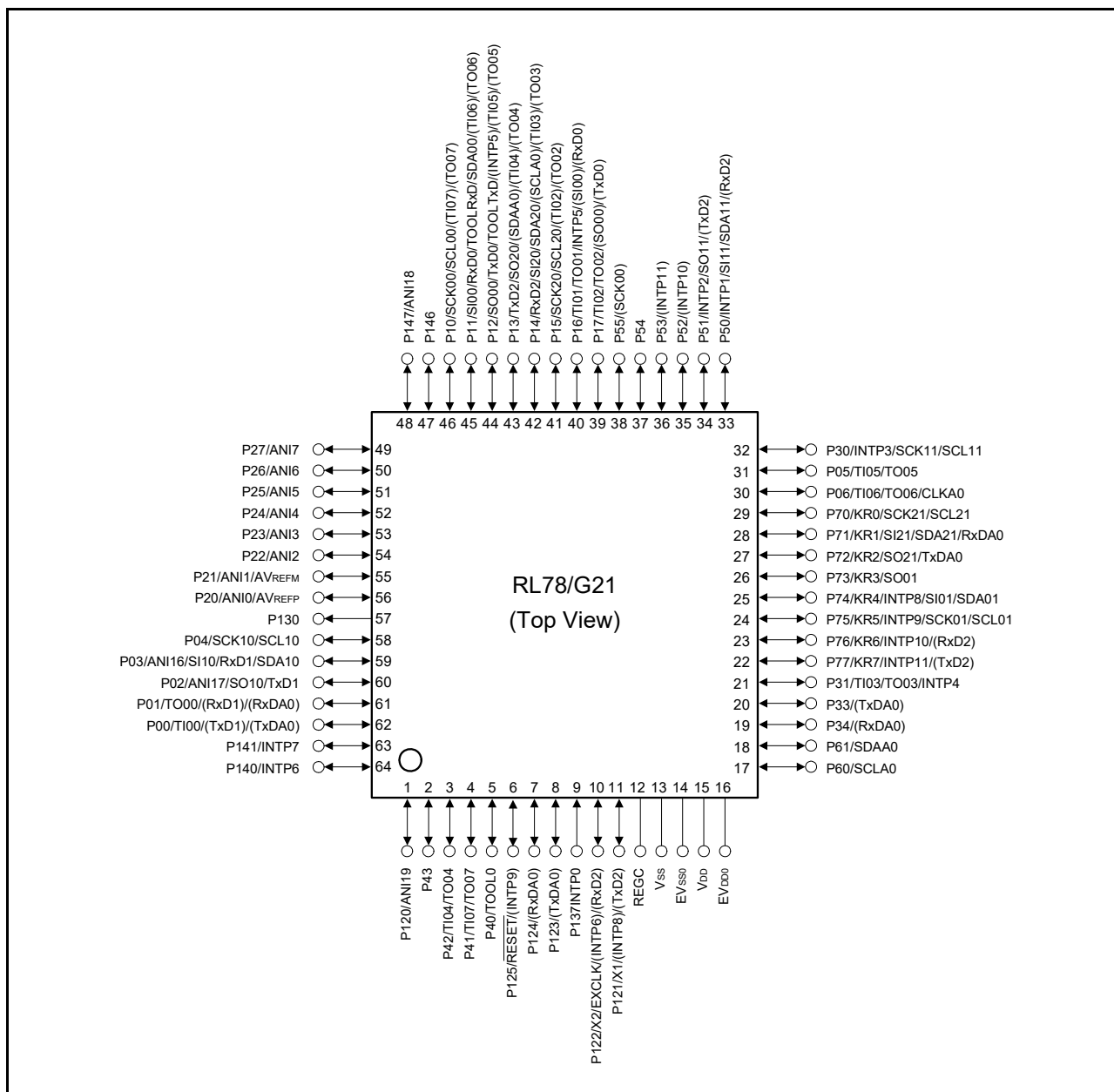
Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
48LFGFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P60	—	—	—	—	—	—	SCLA0	—
2	P61	—	—	—	—	—	—	SDAA0	—
3	P34	—	—	—	—	—	—	—	(RxD A0)
4	P33	—	—	—	—	—	—	—	(TxD A0)
5	P31	—	—	INTP4	—	TI03/TO03	—	—	—
6	P75	—	—	INTP9	KR5	—	SCK01/SCL01	—	—
7	P74	—	—	INTP8	KR4	—	SI01/SDA01	—	—
8	P73	—	—	—	KR3	—	SO01	—	—
9	P72	—	—	—	KR2	—	SO21	—	TxD A0
10	P71	—	—	—	KR1	—	SI21/SDA21	—	RxD A0
11	P70	—	—	—	KR0	—	SCK21/SCL21	—	—
12	P30	—	—	INTP3	—	—	SCK11/SCL11	—	—
13	P50	—	—	INTP1	—	—	SI11/SDA11/ (RxD2)	—	—
14	P51	—	—	INTP2	—	—	SO11/(TxD2)	—	—
15	P17	—	—	—	—	TI02/TO02	(TxD0)	—	—
16	P16	—	—	INTP5	—	TI01/TO01	(RxD0)	—	—
17	P15	—	—	—	—	(TI02)/(TO02)	SCK20/SCL20	—	—
18	P14	—	—	—	—	(TI03)/(TO03)	SI20/RxD2/ SDA20	(SCLA0)	—
19	P13	—	—	—	—	(TI04)/(TO04)	SO20/TxD2	(SDAA0)	—
20	P12	TOOLTxD	—	—	—	(TI05)/(TO05)	SO00/TxD0	—	—
21	P11	TOOLRxD	—	—	—	(TI06)/(TO06)	SI00/RxD0/ SDA00	—	—
22	P10	—	—	—	—	(TI07)/(TO07)	SCK00/SCL00	—	—
23	P146	—	—	—	—	—	—	—	—
24	P147	—	ANI18	—	—	—	—	—	—
25	P27	—	ANI7	—	—	—	—	—	—
26	P26	—	ANI6	—	—	—	—	—	—
27	P25	—	ANI5	—	—	—	—	—	—
28	P24	—	ANI4	—	—	—	—	—	—
29	P23	—	ANI3	—	—	—	—	—	—
30	P22	—	ANI2	—	—	—	—	—	—
31	P21	—	ANI1/AVREFM	—	—	—	—	—	—
32	P20	—	ANI0/AVREFP	—	—	—	—	—	—
33	P130	—	—	—	—	—	—	—	—
34	P01	—	—	—	—	TO00	RxD1	—	(RxD A0)
35	P00	—	—	—	—	TI00	TxD1	—	(TxD A0)
36	P140	—	—	INTP6	—	—	—	—	—

Table 1 - 5 Multiplexed Pin Functions of the 48-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
48LFGFP	Digital port		A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
37	P120	—	ANI19	—	—	—	—	—	—
38	P41	—	—	—	—	TI07/TO07	—	—	—
39	P40	TOOL0	—	—	—	—	—	—	—
40	P125	RESET	—	(INTP9)	—	—	—	—	—
41	P124	—	—	—	—	—	—	—	(RxDA0)
42	P123	—	—	—	—	—	—	—	(TxDA0)
43	P137	—	—	INTP0	—	—	—	—	—
44	P122	X2/EXCLK	—	(INTP6)	—	—	(RxD2)	—	—
45	P121	X1	—	(INTP8)	—	—	(TxD2)	—	—
46	—	REGC	—	—	—	—	—	—	—
47	—	Vss	—	—	—	—	—	—	—
48	—	VDD	—	—	—	—	—	—	—

1.3.5 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)



Caution 1. Connect the EVSS0 pin to the same ground as the Vss pin.

Caution 2. Make sure that the voltage on the VDD pin is no less than that on the EVDD0 pin.

Caution 3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the corresponding peripheral I/O redirection register (PIORx). For details, see 4.3.8 Peripheral I/O redirection registers (PIORx) in the RL78/G21 User's Manual.

Table 1 - 6 Multiplexed Pin Functions of the 64-pin Products (1/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
			A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P120	—	ANI19	—	—	—	—	—	—
2	P43	—	—	—	—	—	—	—	—
3	P42	—	—	—	—	TI04/TO04	—	—	—
4	P41	—	—	—	—	TI07/TO07	—	—	—
5	P40	TOOL0	—	—	—	—	—	—	—
6	P125	RESET	—	(INTP9)	—	—	—	—	—
7	P124	—	—	—	—	—	—	—	(RxDA0)
8	P123	—	—	—	—	—	—	—	(TxDA0)
9	P137	—	—	INTP0	—	—	—	—	—
10	P122	X2/EXCLK	—	(INTP6)	—	—	(RxD2)	—	—
11	P121	X1	—	(INTP8)	—	—	(TxD2)	—	—
12	—	REGC	—	—	—	—	—	—	—
13	—	Vss	—	—	—	—	—	—	—
14	—	EVss0	—	—	—	—	—	—	—
15	—	VDD	—	—	—	—	—	—	—
16	—	EVDD0	—	—	—	—	—	—	—
17	P60	—	—	—	—	—	—	SCLA0	—
18	P61	—	—	—	—	—	—	SDAA0	—
19	P34	—	—	—	—	—	—	—	(RxDA0)
20	P33	—	—	—	—	—	—	—	(TxDA0)
21	P31	—	—	INTP4	—	TI03/TO03	—	—	—
22	P77	—	—	INTP11	KR7	—	(TxD2)	—	—
23	P76	—	—	INTP10	KR6	—	(RxD2)	—	—
24	P75	—	—	INTP9	KR5	—	SCK01/SCL01	—	—
25	P74	—	—	INTP8	KR4	—	SI01/SDA01	—	—
26	P73	—	—	—	KR3	—	SO01	—	—
27	P72	—	—	—	KR2	—	SO21	—	TxDA0
28	P71	—	—	—	KR1	—	SI21/SDA21	—	RxDA0
29	P70	—	—	—	KR0	—	SCK21/SCL21	—	—
30	P06	—	—	—	—	TI06/TO06	—	—	CLKA0
31	P05	—	—	—	—	TI05/TO05	—	—	—
32	P30	—	—	INTP3	—	—	SCK11/SCL11	—	—
33	P50	—	—	INTP1	—	—	SI11/SDA11/ (RxD2)	—	—
34	P51	—	—	INTP2	—	—	SO11/(TxD2)	—	—
35	P52	—	—	(INTP10)	—	—	—	—	—
36	P53	—	—	(INTP11)	—	—	—	—	—
37	P54	—	—	—	—	—	—	—	—

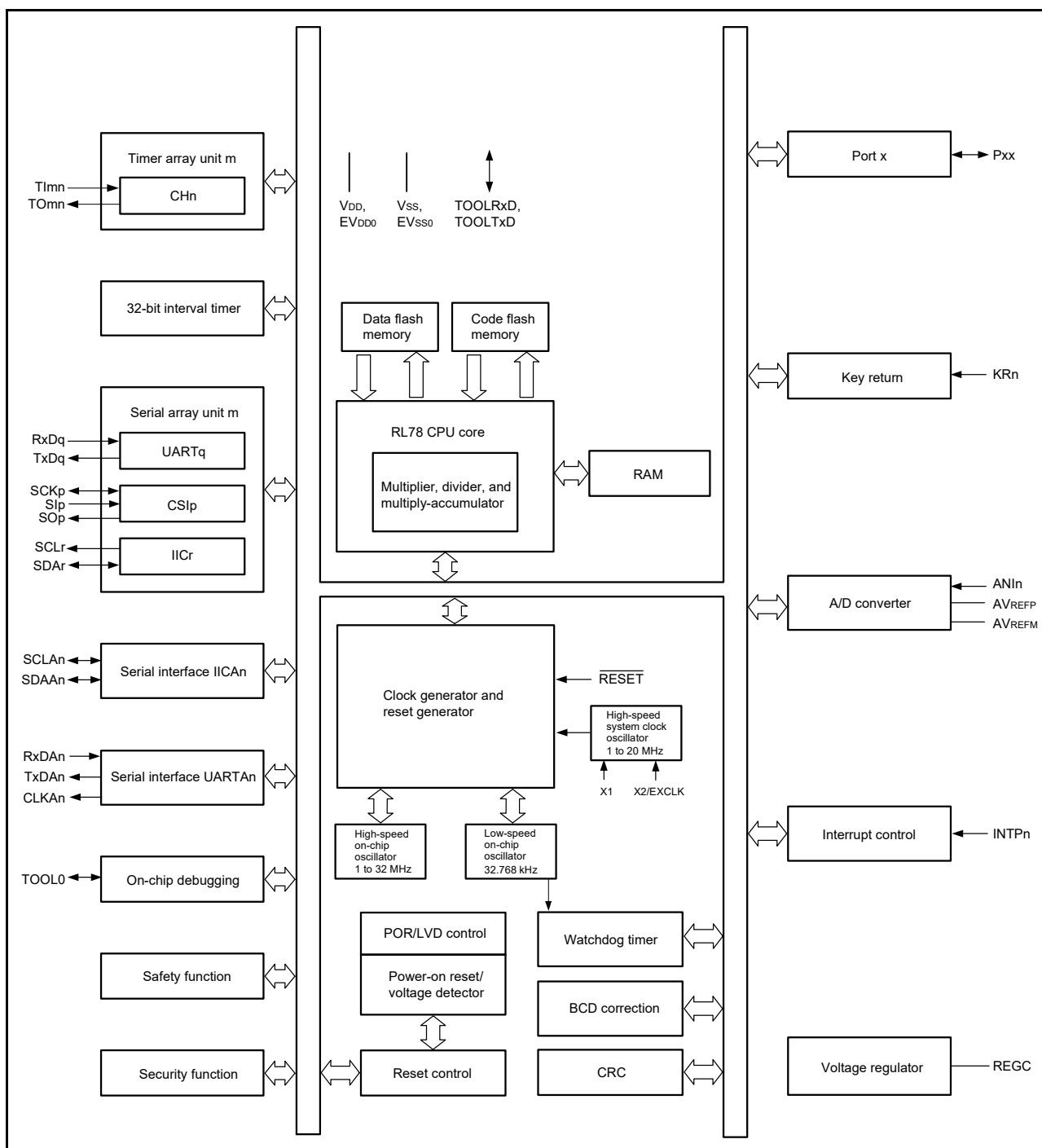
Table 1 - 6 Multiplexed Pin Functions of the 64-pin Products (2/2)

Pin Number	I/O	Power supply, system clock, and debugging	Analog Circuit	HMI		Timer	Communications Interfaces		
			A/D converter (ADC)	Interrupt	Key interrupt	Timer array unit (TAU)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
38	P55	—	—	—	—	—	(SCK00)	—	—
39	P17	—	—	—	—	TI02/TO02	(SO00)/(TxD0)	—	—
40	P16	—	—	INTP5	—	TI01/TO01	(SI00)/(RxD0)	—	—
41	P15	—	—	—	—	(TI02)/(TO02)	SCK20/SCL20	—	—
42	P14	—	—	—	—	(TI03)/(TO03)	SI20/RxD2/SDA20	(SCLA0)	—
43	P13	—	—	—	—	(TI04)/(TO04)	SO20/TxD2	(SDAA0)	—
44	P12	TOOLTxD	—	(INTP5)	—	(TI05)/(TO05)	SO00/TxD0	—	—
45	P11	TOOLRxD	—	—	—	(TI06)/(TO06)	SI00/RxD0/SDA00	—	—
46	P10	—	—	—	—	(TI07)/(TO07)	SCK00/SCL00	—	—
47	P146	—	—	—	—	—	—	—	—
48	P147	—	ANI18	—	—	—	—	—	—
49	P27	—	ANI7	—	—	—	—	—	—
50	P26	—	ANI6	—	—	—	—	—	—
51	P25	—	ANI5	—	—	—	—	—	—
52	P24	—	ANI4	—	—	—	—	—	—
53	P23	—	ANI3	—	—	—	—	—	—
54	P22	—	ANI2	—	—	—	—	—	—
55	P21	—	ANI1/AVREFM	—	—	—	—	—	—
56	P20	—	ANI0/AVREFP	—	—	—	—	—	—
57	P130	—	—	—	—	—	—	—	—
58	P04	—	—	—	—	—	SCK10/SCL10	—	—
59	P03	—	ANI16	—	—	—	SI10/RxD1/SDA10	—	—
60	P02	—	ANI17	—	—	—	SO10/TxD1	—	—
61	P01	—	—	—	—	TO00	(RxD1)	—	(RxDA0)
62	P00	—	—	—	—	TI00	(TxD1)	—	(TxDA0)
63	P141	—	—	INTP7	—	—	—	—	—
64	P140	—	—	INTP6	—	—	—	—	—

1.4 Pin Identification

ANI0 to ANI7,		$\overline{\text{RESET}}$:	Reset
ANI16 to ANI19:	Analog input	RxD0 to RxD2, RxDA0:	Receive data
AVREFM:	Analog reference voltage minus	SCLA0,	
AVREFP:	Analog reference voltage plus	SCK00, SCK01, SCK10,	
CLKA0:	Asynchronous serial clock output	SCK11, SCK20, SCK21:	Serial clock input/output
EVDb0:	Power supply for port	SCL00, SCL01, SCL10,	
EVSS0:	Ground for port	SCL11, SCL20, SCL21:	Serial clock output
EXCLK:	External clock input (main system clock)	SDAA0, SDA00, SDA01,	
		SDA10, SDA11,	
INTP0 to INTP11:	Interrupt request from peripheral	SDA20, SDA21:	Serial data input/output
KR0 to KR7:	Key return input	SI00, SI01, SI10, SI11,	
P00 to P06:	Port 0	SI20, SI21:	Serial data input
P10 to P17:	Port 1	SO00, SO01, SO10,	
P20 to P27:	Port 2	SO11, SO20, SO21:	Serial data output
P30, P31, P33, P34:	Port 3	TI00 to TI07:	Timer input
P40 to P43:	Port 4	TO00 to TO07:	Timer output
P50 to P55:	Port 5	TOOL0:	Data input/output for tool
P60, P61:	Port 6	TOOLRxD, TOOLTxD:	Data input/output for external device
P70 to P77:	Port 7	TxD0 to TxD2, TxDA0:	Transmit data
P120 to P125:	Port 12	VDD:	Power supply
P130, P137:	Port 13	VSS:	Ground
P140, P141, P146, P147:	Port 14	X1, X2:	Crystal oscillator (main system clock)
REGC:	Regulator capacitance		

1.5 Block Diagram



Caution 44- to 64-pin products incorporate the key return function.

Remark m: Unit number, n: Channel number, p: Simplified SPI (CSI) number, q: UART number, r: Simplified I²C number, xx: Port number

1.6 Outline of Functions

[20- to 64-pin products]

Caution This outline describes the functions at the time when the corresponding peripheral I/O redirection register (PIORx) is set to 00H.

(1/3)

Item		20-pin	32-pin	44-pin	48-pin	64-pin
		R7F103G6x	R7F103GBx	R7F103GFx	R7F103GGx	R7F103GLx
Code flash memory		128 or 256 KB				
Data flash memory		4 KB				
RAM		8 KB				
Address space		1 MB				
CPU/peripheral hardware clock frequency (fCLK)	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (VDD = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz ^{Note 1} (VDD = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (VDD = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz ^{Note 1} (VDD = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz ^{Note 2} (VDD = 1.6 to 5.5 V)				
	Subsystem clock	SUB mode: 32.768 kHz (VDD = 1.6 to 5.5 V)				
Main system clock	High-speed system clock (fMX)	1 to 20 MHz				
	High-speed on-chip oscillator clock (fIH)	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz				
Subsystem clock	Low-speed on-chip oscillator clock (fIL)	32.768 kHz (typ.)				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (fIH))				
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.				
I/O port	Total number of pins	17	29	41	45	59
	CMOS I/O	16 (N-ch open-drain I/O [withstand voltage of VDD]: 5)	26 (N-ch open-drain I/O [withstand voltage of VDD]: 11)	38 (N-ch open-drain I/O [withstand voltage of VDD]: 14)	41 (N-ch open-drain I/O [withstand voltage of VDD]: 15)	55 (N-ch open-drain I/O [withstand voltage of VDD]: 19)
	CMOS input	1				
	CMOS output	0	0	0	1	1
	N-ch open-drain I/O (withstand voltage: 6 V)	0	2	2	2	2

(2/3)

Item		20-pin	32-pin	44-pin	48-pin	64-pin	
		R7F103G6x	R7F103GBx	R7F103GFx	R7F103GGx	R7F103GLx	
Timers	16-bit timer	8 channels					
	Watchdog timer	1 channel					
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode					
	Timer output	6 channels (PWM outputs: 5 ^{Note 3})	4 channels (PWM outputs: 3 ^{Note 3}), 8 channels (PWM outputs: 7 ^{Note 3}) ^{Note 4}	5 channels (PWM outputs: 3 ^{Note 3}), 8 channels (PWM outputs: 7 ^{Note 3}) ^{Note 4}		8 channels (PWM outputs: 7 ^{Note 3})	
8-/10-bit resolution A/D converter		6 channels	8 channels	10 channels	10 channels	12 channels	
Serial interface		[20-pin products] • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Single UART, and not usable for simplified SPI (CSI) or simplified I ² C [32-pin products] • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Single simplified SPI (CSI) or simplified I ² C channel, or single UART also supporting the LIN bus [44-pin products] • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Two simplified SPI (CSI) or simplified I ² C channels, or single UART also supporting the LIN bus [48-pin products] • Two simplified SPI (CSI) or simplified I ² C channels, or single UART • Single simplified SPI (CSI) or simplified I ² C channel, or single UART • Two simplified SPI (CSI) or simplified I ² C channels, or single UART also supporting the LIN bus [64-pin products] • Two simplified SPI (CSI) or simplified I ² C channels, or single UART • Two simplified SPI (CSI) or simplified I ² C channels, or single UART • Two simplified SPI (CSI) or simplified I ² C channels, or single UART also supporting the LIN bus					
		UARTA	1 channel				
		I ² C bus	—	1 channel			
Vectored interrupt sources	Internal	23	26	26	26	26	
	External	6	9	10	10	13	
Key interrupt		—		4	6	8	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution ^{Note 5} • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		Detection voltage • 1.50 V (typ.)					

(3/3)

Item		20-pin	32-pin	44-pin	48-pin	64-pin
		R7F103G6x	R7F103GBx	R7F103GFx	R7F103GGx	R7F103GLx
Voltage detector	LVD0	Detection voltage • Rising edge: 1.69 V to 3.96 V (6 stages) • Falling edge: 1.65 V to 3.88 V (6 stages)				
	LVD1	Detection voltage • Rising edge: 1.67 V to 4.16 V (18 stages) • Falling edge: 1.63 V to 4.08 V (18 stages)				
On-chip debugging		Available (tracing supported)				
Power supply voltage		VDD = 1.6 to 5.5 V				
Operating ambient temperature		TA = -40 to +105°C (3Z: Industrial and consumer applications)				

Note 1. Ensure that the operating voltage is at least 1.8 V during overwriting of the flash memory.

Note 2. When the flash memory is to be overwritten, switch to high-speed main (HS) mode or low-speed main (LS) mode.

Note 3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G21 User's Manual.

Note 4. This applies when the corresponding bit in the peripheral I/O redirection register (PIOR0) is set to 1.

Note 5. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the on-chip debugging emulator.

2. Electrical Characteristics

This section describes the electrical characteristics of the following products.

- 3Z: Industrial and consumer applications, $T_A = -40$ to $+105^{\circ}\text{C}$
R7F103Gxx3Zxx

Caution 1. This MCU has on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.

Caution 2. For products that do not have an EVDD0 or EVSS0 pin, read EVDD0 as VDD, and EVSS0 as VSS.

Caution 3. The present pins differ depending on the products. For details, see section 2.1 Functions of Port Pins through section 2.2.1 Functions for each product in the RL78/G21 User's Manual.

2.1 Absolute Maximum Ratings

(1/2)

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0}		-0.5 to +6.5	V
	EV _{SS0}		-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.1 and -0.3 to V _{DD} + 0.3 ^{Note 1}	V
Input voltage	V _{I1}	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	-0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{I2}	P60, P61 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P125, P137, EXCLK, RESET	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Output voltage	V _{O1}	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	-0.3 to EV _{DD0} + 0.3 and -0.3 to V _{DD} + 0.3 ^{Note 2}	V
	V _{O2}	P20 to P27, P121 to P125	-0.3 to V _{DD} + 0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI19	-0.3 to EV _{DD0} + 0.3 and -0.3 to AV _{REFP} + 0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI7	-0.3 to V _{DD} + 0.3 and -0.3 to AV _{REFP} + 0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2. This voltage must be no higher than 6.5 V.

Note 3. The voltage on a pin in use for A/D conversion must not exceed AV_{REFP} + 0.3.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. AV_{REFP} refers to the positive reference voltage of the A/D converter.

Remark 3. The reference voltage is V_{SS}.

(2/2)

Item	Symbols	Conditions		Ratings	Unit
High-level output current	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	-70	mA
			P05, P06, P10 to P17, P30, P31, P33, P34, P50 to P55, P70 to P77, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P121 to P125	-5	mA
		Total of all pins		-20	mA
Low-level output current	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P60, P61, P70 to P77, P120, P130, P140, P141, P146, P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P17, P30, P31, P33, P34, P50 to P55, P60, P61, P70 to P77, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P121 to P125	10	mA
		Total of all pins		20	mA
Ambient operating temperature	TA	In normal operation mode	3Z: Industrial and consumer applications	-40 to +105	°C
		In flash memory programming mode	3Z: Industrial and consumer applications	-40 to +105	
Storage temperature	T _{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.2 Characteristics of the Oscillators

2.2.1 Characteristics of the X1 oscillator

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time ^{Note}	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to **2.4 AC**

Characteristics for instruction execution time.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

2.2.2 Characteristics of the on-chip oscillators

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f _{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy (HIPREC = 1)		-40 to +105°C	1.6 V ≤ VDD ≤ 5.5 V	-1		+1	%
High-speed on-chip oscillator clock correction resolution					0.05		%
Low-speed on-chip oscillator clock frequency ^{Note}	f _{IL}				32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note The listed values only indicate the characteristics of the oscillators. Refer to **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Characteristics of pins

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/6)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Allowable high-level output current ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	1.6 V ≤ EVDD0 ≤ 5.5 V		-10.0 Note 2	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (when duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-55.0 Note 4	mA
			2.7 V ≤ EVDD0 < 4.0 V		-10.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		-5.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P33, P34, P50 to P55, P70 to P77, P146, P147 (when duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		-80.0 Note 5	mA
			2.7 V ≤ EVDD0 < 4.0 V		-19.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		-10.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		-5.0	mA
		Total of all pins (when duty ≤ 70% ^{Note 3})	1.6 V ≤ EVDD0 ≤ 5.5 V		-100.0 Note 6	mA
	IOH2	Per pin for P20 to P27, P121 to P125	4.0 V ≤ VDD ≤ 5.5 V		-3.0 Note 2	mA
			2.7 V ≤ VDD < 4.0 V		-1.0 Note 2	mA
			1.8 V ≤ VDD < 2.7 V		-1.0 Note 2	mA
			1.6 V ≤ VDD < 1.8 V		-0.5 Note 2	mA
		Total of all pins (when duty ≤ 70% ^{Note 3})	4.0 V ≤ VDD ≤ 5.5 V		-20.0	mA
			2.7 V ≤ VDD < 4.0 V		-10.0	mA
			1.8 V ≤ VDD < 2.7 V		-5.0	mA
			1.6 V ≤ VDD < 1.8 V		-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the EVDD0 or VDD pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

$$\bullet \text{ Total output current from the listed pins} = (\text{IOH} \times 0.7) / (n \times 0.01)$$

Example when n = 80% and IOH = -10.0 mA

$$\text{Total output current from the listed pins} = (-10.0 \times 0.7) / (80 \times 0.01) \approx -8.7 \text{ mA}$$

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -30 mA with an ambient operating temperature range of +85°C to +105°C.

Note 5. The maximum value is -50 mA with an ambient operating temperature range of +85°C to +105°C.

Note 6. The maximum value is -60 mA with an ambient operating temperature range of +85°C to +105°C.

(Caution and Remark continue on the next page.)

Caution The following pins are not capable of the output of high-level signals in the N-ch open-drain output mode.
P00, P02 to P04, P10 to P15, P17, P31, P33, P50, P51, P55, P71, P72, and P74

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/6)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Allowable low-level output current ^{Note 1}	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147			20.0 Note 2	mA
		Per pin for P60, P61			15.0 Note 2	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (when duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		70.0 Note 4	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P33, P34, P50 to P55, P60, P61, P70 to P77, P146, P147 (when duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		80.0 Note 4	mA
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA
			1.8 V ≤ EVDD0 < 2.7 V		20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V		10.0	mA
		Total of all pins (when duty ≤ 70% ^{Note 3})			150.0 Note 5	mA
	IOL2	Per pin for P20 to P27, P121 to P125	4.0 V ≤ VDD ≤ 5.5 V		8.5 Note 2	mA
			2.7 V ≤ VDD < 4.0 V		1.5 Note 2	mA
			1.8 V ≤ VDD < 2.7 V		0.6 Note 2	mA
			1.6 V ≤ VDD < 1.8 V		0.4 Note 2	mA
		Total of all pins (when duty ≤ 70% ^{Note 3})	4.0 V ≤ VDD ≤ 5.5 V		20	mA
			2.7 V ≤ VDD < 4.0 V		20	mA
			1.8 V ≤ VDD < 2.7 V		15	mA
			1.6 V ≤ VDD < 1.8 V		10	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0 or VSS pin.**Note 2.** The combination of these and other pins must also not exceed the value for maximum total current.**Note 3.** The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

$$\bullet \text{ Total output current from the listed pins} = (IOL \times 0.7)/(n \times 0.01)$$

Example when n = 80% and IOL = 10.0 mA

$$\text{Total output current from the listed pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is 40 mA with an ambient operating temperature range of +85°C to +105°C.**Note 5.** The maximum value is 80 mA with an ambient operating temperature range of +85°C to +105°C.**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(3/6)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	VIH1	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	VIH2	P01, P03, P04, P10, P11, P13 to P17, P34, P50, P55, P71	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	VIH3	P20 to P27		0.7 VDD		VDD	V
	VIH4	P60, P61		0.7 EVDD0		6.0	V
	VIH5	P121 to P125, P137, EXCLK		0.8 VDD		VDD	V
Input voltage, low	VIL1	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0		0.2 EVDD0	V
	VIL2	P01, P03, P04, P10, P11, P13 to P17, P34, P50, P55, P71	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0		0.32	V
	VIL3	P20 to P27		0		0.3 VDD	V
	VIL4	P60, P61		0		0.3 EVDD0	V
	VIL5	P121 to P125, P137, EXCLK		0		0.2 VDD	V

Caution The maximum value of VIH of pins P00, P02 to P04, P10 to P15, P17, P31, P33, P50, P51, P55, P71, P72, and P74 is EVDD0, even in the N-ch open-drain output mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(4/6)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -10.0 mA	EVDD0 - 1.5		V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7		V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -2.0 mA	EVDD0 - 0.6		V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA	EVDD0 - 0.5		V
			1.6 V ≤ EVDD0 < 5.5 V, IOH1 = -1.0 mA	EVDD0 - 0.5		V
	VOH2	P20 to P27, P121 to P125	4.0 V ≤ VDD ≤ 5.5 V, IOH2 = -3.0 mA	VDD - 0.7		V
			2.7 V ≤ VDD < 4.0 V, IOH2 = -1.0 mA	VDD - 0.5		V
			1.8 V ≤ VDD < 2.7 V, IOH2 = -1.0 mA	VDD - 0.5		V
			1.6 V ≤ VDD < 1.8 V, IOH2 = -0.5 mA	VDD - 0.5		V

Caution The following pins are not capable of the output of high-level signals in the N-ch open-drain output mode.
P00, P02 to P04, P10 to P15, P17, P31, P33, P50, P51, P55, P71, P72, and P74

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(5/6)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit	
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 20.0 mA			1.3	V	
			4.0 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 8.5 mA			0.7	V	
			2.7 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 3.0 mA			0.6	V	
			2.7 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 1.5 mA			0.4	V	
			1.8 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 0.6 mA			0.4	V	
			1.6 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 0.3 mA			0.4	V	
	VOL2	P20 to P27, P121 to P125	4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 8.5 mA					0.7	V
			2.7 V ≤ VDD < 4.0 V, IOL2 = 1.5 mA					0.5	V
			1.8 V ≤ VDD < 2.7 V, IOL2 = 0.6 mA					0.4	V
			1.6 V ≤ VDD < 1.8 V, IOL2 = 0.4 mA					0.4	V
	VOL3	P60, P61	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA					2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA					0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA					0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA					0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 1.0 mA					0.4	V

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(6/6)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input leakage current, high	ILI _{H1}	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P60, P61, P70 to P77, P120, P140, P141, P146, P147			0.5	μA
	ILI _{H2}	P20 to P27, P137			0.5	μA
	ILI _{H3}	P121 to P125 (X1, X2, EXCLK)			0.5	μA
Input leakage current, low	ILI _{L1}	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P60, P61, P70 to P77, P120, P140, P141, P146, P147			-0.5	μA
	ILI _{L2}	P20 to P27, P137			-0.5	μA
	ILI _{L3}	P121 to P125 (X1, X2, EXCLK)			-0.5	μA
On-chip pull-up resistance	RU	P00 to P06, P10 to P17, P30, P31, P33, P34, P40 to P43, P50 to P55, P70 to P77, P120 to P125, P140, P141, P146, P147	10	20	100	kΩ
	RU2	P137	70	100	140	kΩ

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Characteristics of the supply current

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	V _{DD} = 5.0 V		1.1	—	mA
						V _{DD} = 1.8 V		1.1	—	
					Normal operation	V _{DD} = 5.0 V		2.6	4.5	mA
						V _{DD} = 1.8 V		2.6	4.5	
			LS (low-speed main) mode	f _{IH} = 24 MHz ^{Note 2}	Normal operation	V _{DD} = 5.0 V		1.9	3.4	mA
						V _{DD} = 1.8 V		1.9	3.4	
				f _{IH} = 16 MHz ^{Note 2}	Normal operation	V _{DD} = 5.0 V		1.4	2.4	mA
						V _{DD} = 1.8 V		1.4	2.4	
				f _{IH} = 4 MHz ^{Note 2}	Normal operation	V _{DD} = 5.0 V		0.6	1.0	mA
						V _{DD} = 1.6 V		0.6	0.9	
			LP (low-power main) mode	f _{IH} = 2 MHz ^{Note 2}	Normal operation	V _{DD} = 5.0 V		435	625	μA
						V _{DD} = 1.6 V		432	622	
				f _{IH} = 1 MHz ^{Note 2}	Normal operation	V _{DD} = 5.0 V		358	489	μA
						V _{DD} = 1.6 V		355	485	
		HS (high-speed main) mode	f _{MX} = 20 MHz ^{Note 3} , square wave input	Normal operation	V _{DD} = 5.0 V		1.7	2.9	mA	
					V _{DD} = 1.8 V		1.6	2.8		
		LS (low-speed main) mode	f _{MX} = 20 MHz ^{Note 3} , square wave input	Normal operation	V _{DD} = 5.0 V		1.5	2.7	mA	
					V _{DD} = 1.8 V		1.5	2.6		
			f _{MX} = 20 MHz ^{Note 3} , resonator connection	Normal operation	V _{DD} = 5.0 V		1.7	2.9	mA	
					V _{DD} = 1.8 V		1.7	2.9		
			f _{MX} = 10 MHz ^{Note 3} , square wave input	Normal operation	V _{DD} = 5.0 V		0.8	1.4	mA	
					V _{DD} = 1.8 V		0.8	1.4		
			f _{MX} = 10 MHz ^{Note 3} , resonator connection	Normal operation	V _{DD} = 5.0 V		0.9	1.5	mA	
					V _{DD} = 1.8 V		0.9	1.5		
			f _{MX} = 8 MHz ^{Note 3} , square wave input	Normal operation	V _{DD} = 5.0 V		0.7	1.1	mA	
					V _{DD} = 1.8 V		0.6	1.1		
			f _{MX} = 8 MHz ^{Note 3} , resonator connection	Normal operation	V _{DD} = 5.0 V		0.8	1.3	mA	
					V _{DD} = 1.8 V		0.7	1.2		

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.
- The currents in the "Max." column include the operating currents of the TAU, SAU, and IICA modules.

Note 2. The listed currents apply when the high-speed system clock and low-speed on-chip oscillator are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator and low-speed on-chip oscillator are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 3. The typical value for the ambient operating temperature (TA) is +25°C unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation mode	fsUB = 32.768 kHzNote 2, low-speed on-chip oscillator operation	Normal operation	TA = -40°C		2.8	5.4	μA
						TA = +25°C		3.1	5.7	
						TA = +50°C		3.3	8.8	
						TA = +70°C		3.6	14.0	
						TA = +85°C		4.1	23.3	
						TA = +105°C		5.4	48.3	

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. In the subsystem clock operation mode, the currents in both the "Typ." and "Max." columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the high-speed on-chip oscillator and high-speed system clock are stopped.

Remark 1. fIL: Low-speed on-chip oscillator clock frequency

Remark 2. fsUB: Subsystem clock frequency

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz Note 3	VDD = 5.0 V		0.46	1.85	mA
					VDD = 1.8 V		0.45	1.84	
			LS (low-speed main) mode	f _{IH} = 24 MHz Note 3	VDD = 5.0 V		0.39	1.44	mA
					VDD = 1.8 V		0.38	1.43	
				f _{IH} = 16 MHz Note 3	VDD = 5.0 V		0.39	1.13	mA
					VDD = 1.8 V		0.38	1.11	
				f _{IH} = 4 MHz Note 3	VDD = 5.0 V		0.34	0.58	mA
					VDD = 1.6 V		0.33	0.57	
			LP (low-power main) mode	f _{IH} = 2 MHz Note 3	VDD = 5.0 V		289	442	μA
					VDD = 1.6 V		287	440	
				f _{IH} = 1 MHz Note 3	VDD = 5.0 V		285	398	μA
					VDD = 1.6 V		282	394	
			HS (high-speed main) mode	f _{MX} = 20 MHz Note 4 , square wave input	VDD = 5.0 V		0.19	1.03	mA
					VDD = 1.8 V		0.16	0.99	
			LS (low-speed main) mode	f _{MX} = 20 MHz Note 4 , square wave input	VDD = 5.0 V		0.19	1.03	mA
					VDD = 1.8 V		0.16	0.99	
				f _{MX} = 20 MHz Note 4 , resonator connection	VDD = 5.0 V		0.39	1.28	mA
					VDD = 1.8 V		0.37	1.27	
				f _{MX} = 10 MHz Note 4 , square wave input	VDD = 5.0 V		0.12	0.54	mA
					VDD = 1.8 V		0.10	0.52	
				f _{MX} = 10 MHz Note 4 , resonator connection	VDD = 5.0 V		0.23	0.68	mA
					VDD = 1.8 V		0.22	0.67	
				f _{MX} = 8 MHz Note 4 , square wave input	VDD = 5.0 V		0.10	0.45	mA
					VDD = 1.8 V		0.09	0.43	
				f _{MX} = 8 MHz Note 4 , resonator connection	VDD = 5.0 V		0.20	0.57	mA
					VDD = 1.8 V		0.19	0.56	

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.
- The currents in the "Max." column include the operating currents of the TAU, SAU, and IICA modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock and low-speed on-chip oscillator are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator and low-speed on-chip oscillator are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 3. The typical value for the ambient operating temperature (TA) is +25°C unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	Subsystem clock operation mode	fSUB = 32.768 kHzNote 3, low-speed on-chip oscillator operation	TA = -40°C		0.45	2.70	μA	
					TA = +25°C		0.55	2.78		
					TA = +50°C		0.65	5.80		
					TA = +70°C		0.86	10.86		
					TA = +85°C		1.95	21.52		
					TA = +105°C		3.25	46.67		
	IDD3	STOP modeNote 4				TA = -40°C		0.16	2	μA
						TA = +25°C		0.23	2	
						TA = +50°C		0.50	5	
						TA = +70°C		0.85	10	
						TA = +85°C		1.50	19	
						TA = +105°C		2.90	44	

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. In the subsystem clock operation mode or the STOP mode, the currents in both the "Typ." and "Max." columns do not include the operating currents of the peripheral modules.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 4. The listed currents apply when the low-speed on-chip oscillator is stopped. For the currents when operating the low-speed on-chip oscillator in the STOP mode, refer to the currents when operating the subsystem clock in the HALT mode.

Remark 1. fIL: Low-speed on-chip oscillator clock frequency

Remark 2. fSUB: Subsystem clock frequency

Peripheral Functions (Common to all products)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I _{FIH} Note 1					320		μA
Low-speed on-chip oscillator operating current	I _{FIL} Note 1					0.2		μA
32-bit interval timer operating current	I _{IT} Notes 1, 2, 3					0.04		μA
Watchdog timer operating current	I _{WDT} Notes 1, 2, 4	f _{IL} = 32.768 kHz (typ.)				0.32		μA
A/D converter operating current	I _{ADC} Notes 1, 5	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V			1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V			0.5	0.7	mA
A/D converter internal reference voltage current	I _{ADREF} Note 1					100		μA
Temperature sensor operating current	I _{TMPS} Note 1					114		μA
LVD operating current	I _{LVD0} Notes 1, 6					0.02		μA
	I _{LVD1} Notes 1, 6					0.02		μA
Self-programming operating current	I _{FSP} Notes 1, 7					2.5	12.2	mA
Data flash memory rewrite operating current	I _{BGO} Notes 1, 8					2.5	12.2	mA
SNOOZE operating current	I _{SNOZ} Note 1	f _{IH} = 32 MHz	ADC to be in use	The ADC is shifting from the STOP mode to the SNOOZE mode. Note 9		0.50	0.70	mA
				The ADC is operating in the low-voltage mode. AVREFP = VDD = 3.0 V		0.90	1.40	
			Simplified SPI (CSI)/UART to be in use				0.70	0.92

Note 1. This current flows into VDD.**Note 2.** The listed currents apply when the high-speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator. The supply current of this MCU is the sum of either IDD1 or IDD2, and IIT, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current.**Note 4.** This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of this MCU is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.**Note 5.** This current only flows to the A/D converter. The supply current of this MCU is the sum of IDD1 or IDD2 and IADC when the A/D converter is operating or in the HALT mode.**Note 6.** This current only flows to the LVD circuit. The supply current of this MCU is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.**Note 7.** This current only flows during self programming.**Note 8.** This current only flows while the data flash memory is being rewritten.**Note 9.** For shift time to the SNOOZE mode, see **16.3.3 SNOOZE mode** in the RL78/G21 User's Manual.

(Remarks are listed on the next page.)

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

2.4 AC Characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.5		1	μs
		Subsystem clock (fSUB) operation			1.6 V ≤ VDD ≤ 5.5 V		30.5	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
External system clock frequency	fEX	1.8 V ≤ VDD ≤ 5.5 V			1.0		20.0	MHz
		1.6 V ≤ VDD < 1.8 V			1.0		4.0	MHz
External system clock input high-level width, low-level width	tEXH, tEXL	1.8 V ≤ VDD ≤ 5.5 V			24			ns
		1.6 V ≤ VDD < 1.8 V			120			ns
TI00 to TI07 input high-level width, low-level width	tTIH, tTIL				1/fMCK + 10			ns ^{Note}
TO00 to TO07 output frequency	fTO	HS (high-speed main) mode LS (low-speed main) mode		4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
				2.7 V ≤ EVDD0 < 4.0 V			8	MHz
				1.8 V ≤ EVDD0 < 2.7 V			4	MHz
				1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ EVDD0 ≤ 5.5 V			2	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 and INTPx multiplexed with P121, P122, or P125		1.6 V ≤ VDD ≤ 5.5 V	1			μs
		INTP1 to INTP11 (however INTPx multiplexed with P121, P122, or P125 is not applicable)		1.6 V ≤ EVDD0 ≤ 5.5 V	1			μs
Key interrupt input high- level width, low-level width	tKRH, tKRL	KR0 to KR7		1.8 V ≤ EVDD0 ≤ 5.5 V	250			ns
				1.6 V ≤ EVDD0 < 1.8 V	1			μs
RESET low-level width	tRSL				10			μs

Note The following conditions are required for low voltage interface when EVDD0 < VDD.

1.8 V ≤ EVDD0 < 2.7 V: 125 ns min.

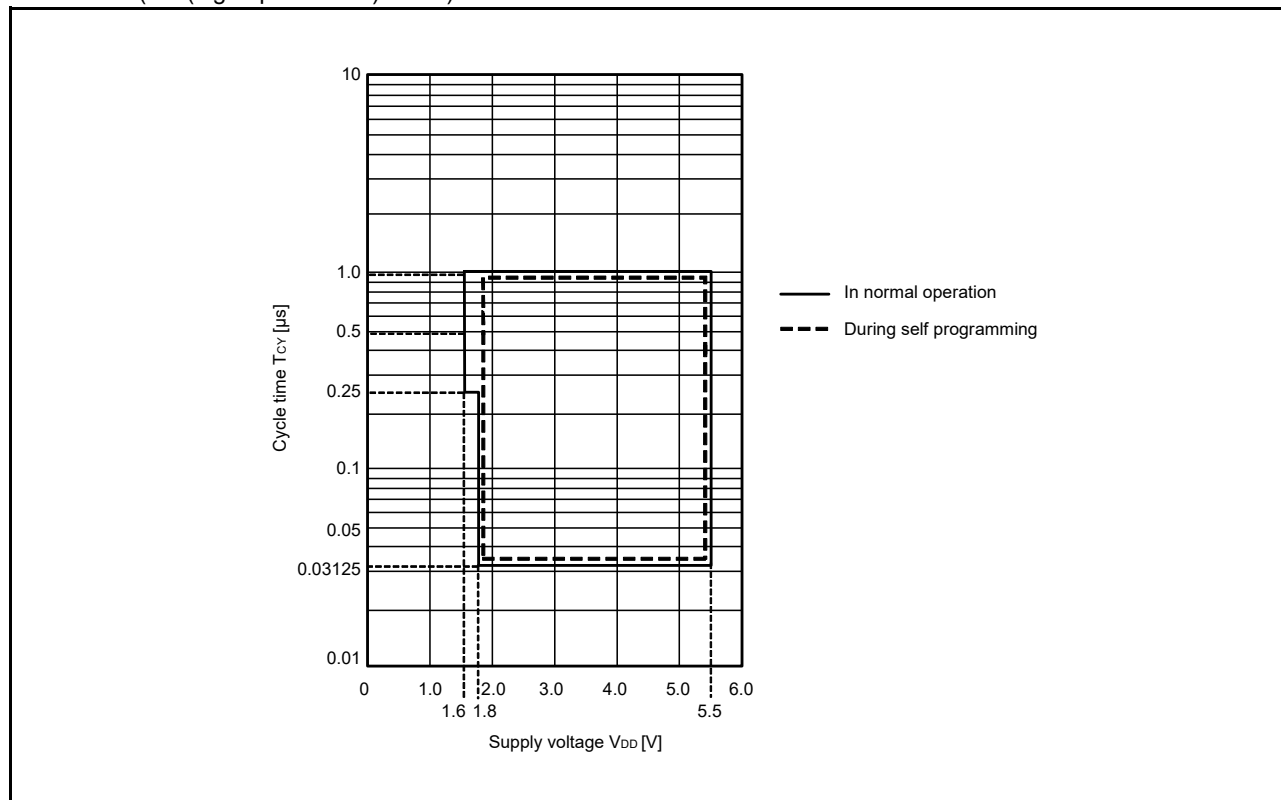
1.6 V ≤ EVDD0 < 1.8 V: 250 ns min.

Remark fMCK: Timer array unit operating clock frequency

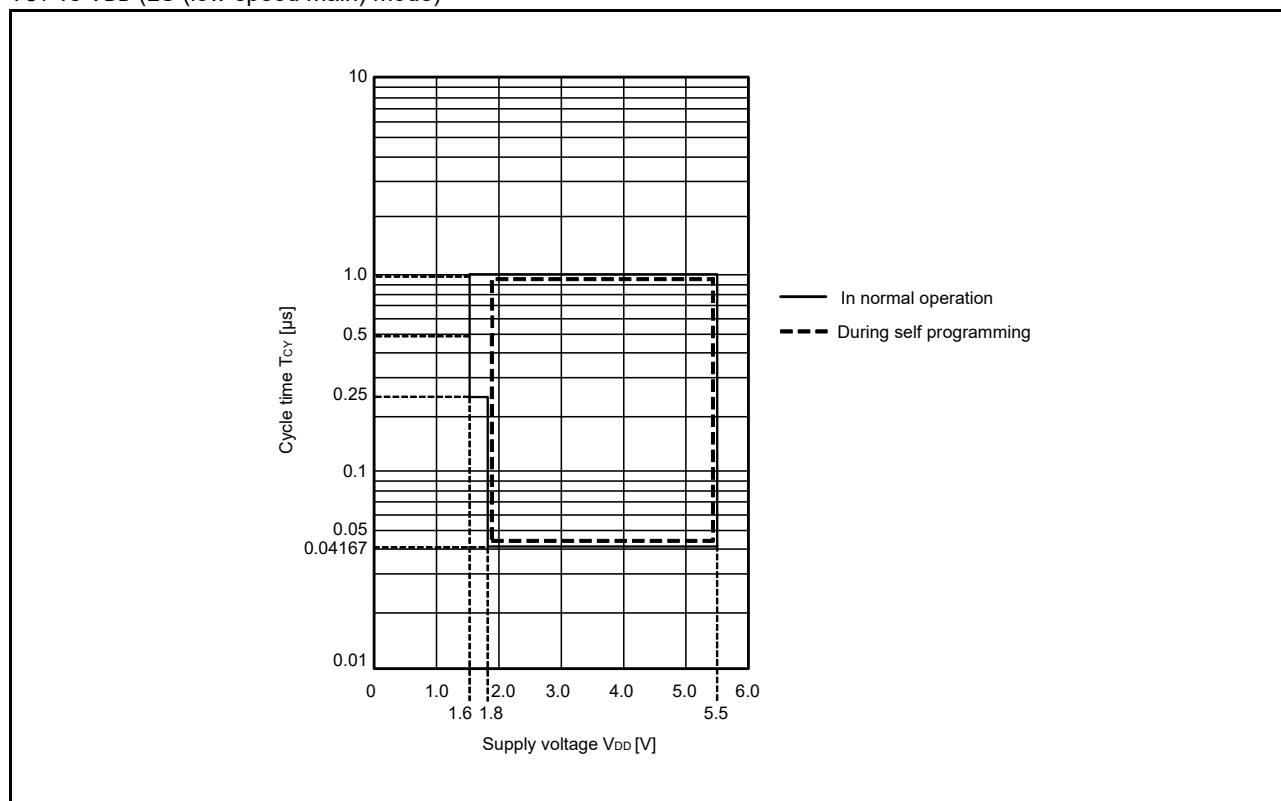
(To set this operating clock, use the CKSMn0 and CKSMn1 bits of the timer mode register mn (TMRmn) (m: Unit number (m = 0), n: Channel number (n = 0 to 7).)

Minimum Instruction Execution Time during Main System Clock Operation

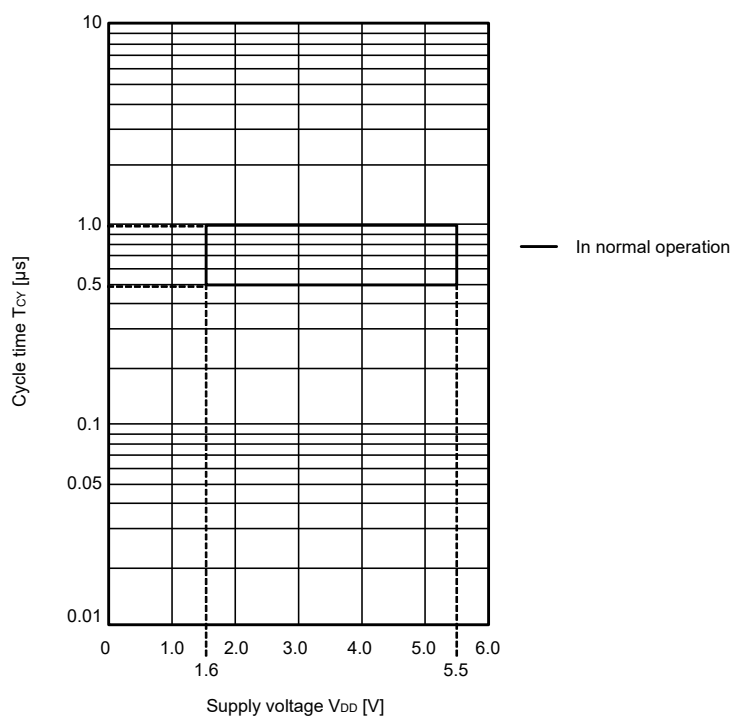
TCY vs VDD (HS (high-speed main) mode)



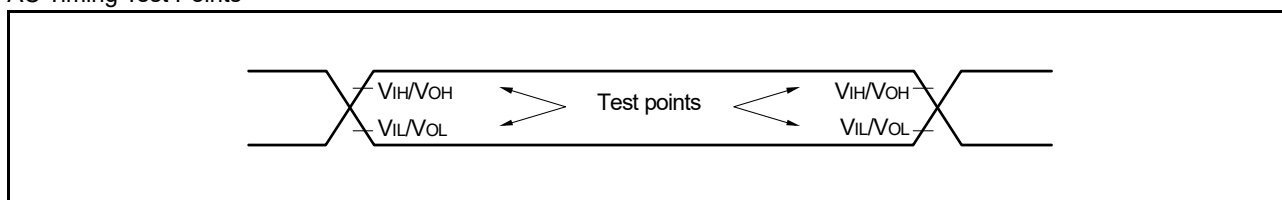
TCY vs VDD (LS (low-speed main) mode)



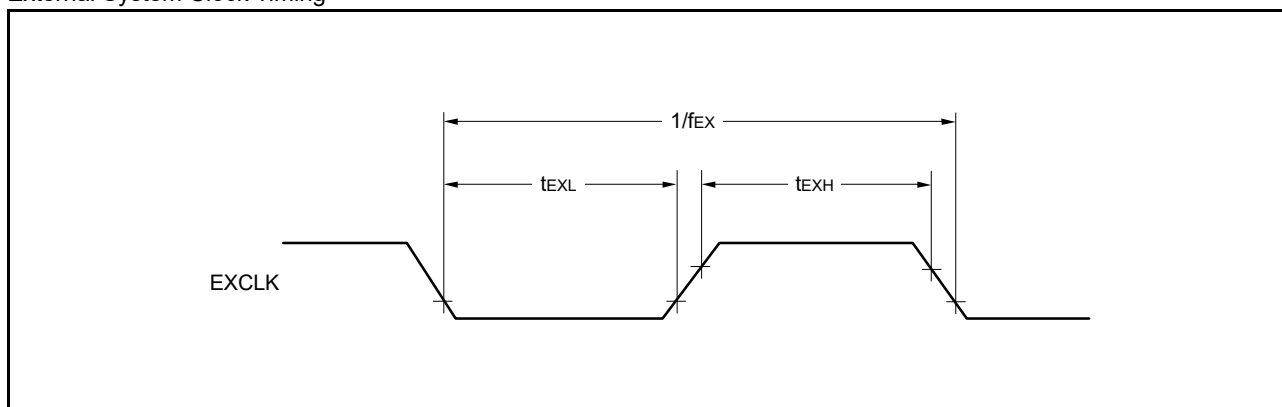
TCY vs VDD (LP (low-power main) mode)



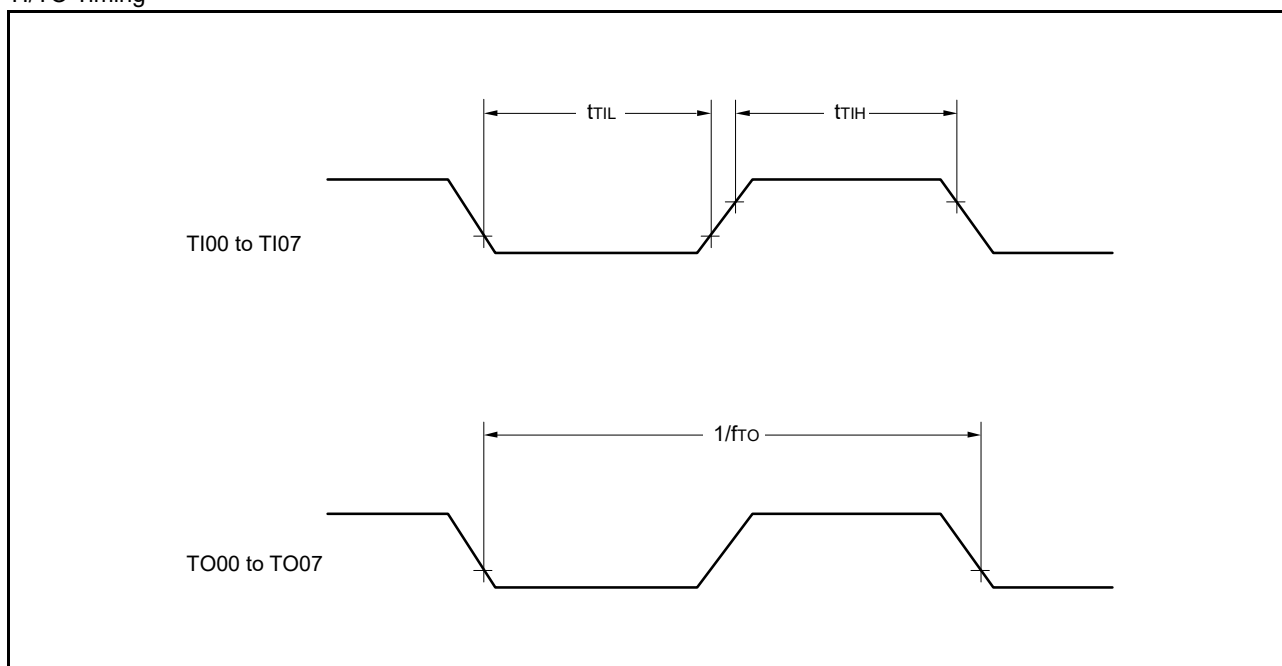
AC Timing Test Points



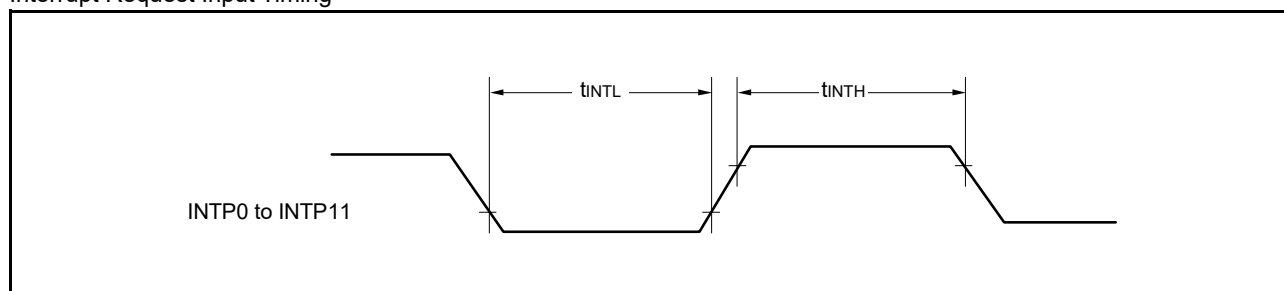
External System Clock Timing



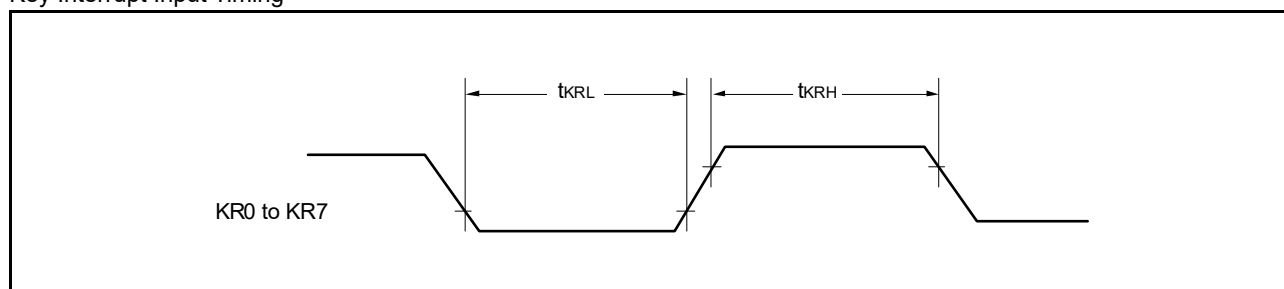
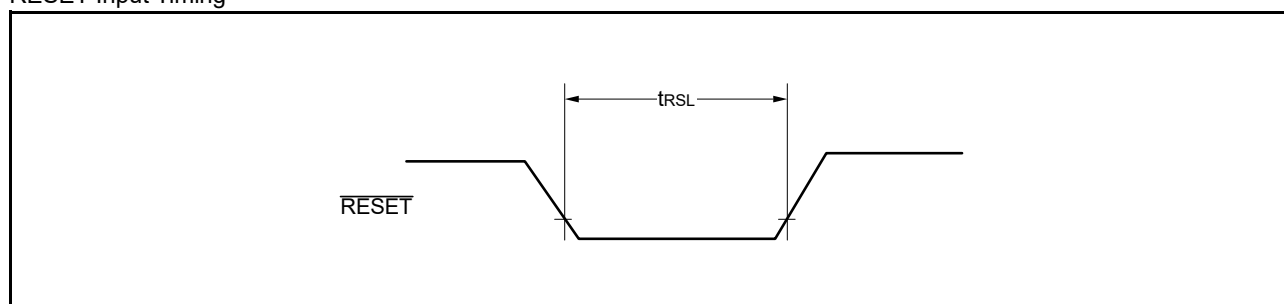
TI/TO Timing



Interrupt Request Input Timing

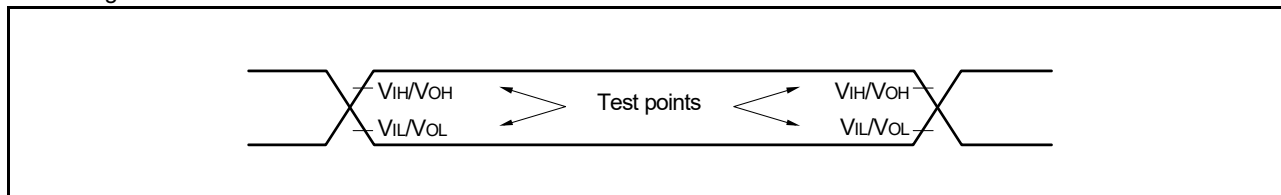


Key Interrupt Input Timing

 $\overline{\text{RESET}}$ Input Timing

2.5 Characteristics of the Peripheral Functions

AC Timing Test Points



2.5.1 Serial array unit

1. In UART communications with devices operating at same voltage levels

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate Note 1		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		fMCK/6 Note 2		fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLKNote 3		5.3		4		0.33	Mbps

Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The following conditions are required for low voltage interface when $\text{EVDD0} < \text{VDD}$.

$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$: 2.6 Mbps max.

$1.8\text{ V} \leq \text{EVDD0} < 2.4\text{ V}$: 1.3 Mbps max.

$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$: 0.6 Mbps max.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are as follows.

HS (high-speed main) mode: 32 MHz ($1.8\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

4 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

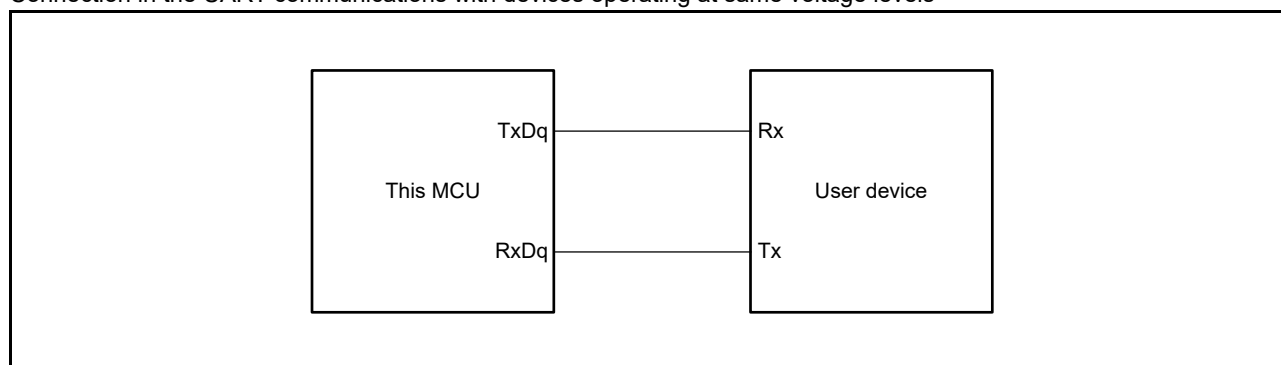
LS (low-speed main) mode: 24 MHz ($1.8\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

4 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

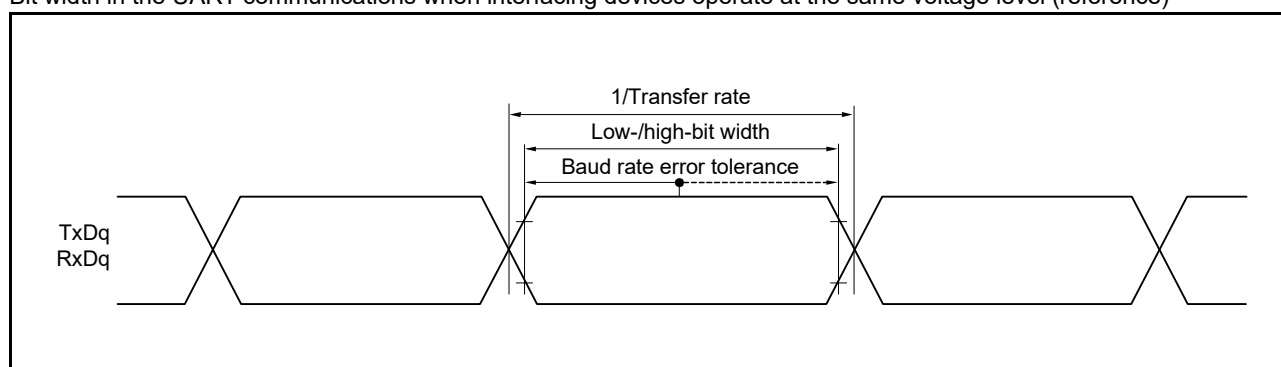
LP (low-power main) mode: 2 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using a port input mode register (PIMg) and port output mode register (POMg).

Connection in the UART communications with devices operating at same voltage levels



Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)



Remark 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5)

Remark 2. fMCK: Serial array unit operation clock frequency

(To set this operating clock, set the CKSMn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00 to 03, 10, 11).)

2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	$\text{tkCY1} \geq 2/\text{fCLK}$	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	62.5		83.3		1000		ns
			$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	83.3		125		1000		ns
SCKp high-level width, low-level width	tkH1, tkL1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY1/2 - 7		tkCY1/2 - 10		tkCY1/2 - 50		ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY1/2 - 10		tkCY1/2 - 15		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) Note 1	tSIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		23		33		110		ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		33		50		110		ns
Slp hold time (from SCKp↑) Note 1	tKS1	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 2	tkSO1	$C = 20\text{ pF}$ Note 3			10		10		10	ns

Note 1. The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg).

Remark 1. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00).)

3. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	$\text{tkCY1} \geq 4/\text{fCLK}$	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	125		166		2000	ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	250		250		2000	ns
			$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	500		500		2000	ns
			$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	1000		1000		2000	ns
SCKp high-level width, low-level width	tkH1, tkL1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 12		tkCY1/2 - 21		tkCY1/2 - 50		ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 18		tkCY1/2 - 25		tkCY1/2 - 50		ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 38		tkCY1/2 - 38		tkCY1/2 - 50		ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	tkCY1/2 - 100		tkCY1/2 - 100		tkCY1/2 - 100		ns
Slp setup time (to SCKp↑) Note 1	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	44		54		110		ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	44		54		110		ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	75		75		110		ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	110		110		110		ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	220		220		220		ns
Slp hold time (from SCKp↑) Note 1	tkSI1	$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 2	tkSO1	$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$ $C = 30\text{ pF}$ Note 3		25		25		25	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 5, 7)

Remark 2. fMCK: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10, 11).)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time Note 1	tkCY2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$20\text{ MHz} < \text{fMCK}$	8/fMCK		8/fMCK		—		ns
			$\text{fMCK} \leq 20\text{ MHz}$	6/fMCK		6/fMCK		6/fMCK		ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$16\text{ MHz} < \text{fMCK}$	8/fMCK		8/fMCK		—		ns
			$\text{fMCK} \leq 16\text{ MHz}$	6/fMCK		6/fMCK		6/fMCK		ns
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		6/fMCK and 500		6/fMCK and 500		6/fMCK and 500		ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		6/fMCK and 750		6/fMCK and 750		6/fMCK and 750		ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		6/fMCK and 1500		6/fMCK and 1500		6/fMCK and 1500		ns
SCKp high-level width, low-level width	tkH2, tkL2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 7		tkCY2/2 - 7		tkCY2/2 - 7		ns
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 8		tkCY2/2 - 8		tkCY2/2 - 8		ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 18		ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 66		tkCY2/2 - 66		tkCY2/2 - 66		ns

(Notes, Caution, and Remarks are listed on the next page.)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(2/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp $\uparrow$) Note 2	tsIK2	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 20		$1/\text{fMCK}$ + 30		$1/\text{fMCK}$ + 30		ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 30		$1/\text{fMCK}$ + 30		$1/\text{fMCK}$ + 30		ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 40		$1/\text{fMCK}$ + 40		$1/\text{fMCK}$ + 40		ns
Slp hold time (from SCKp $\uparrow$) Note 2	tKSI2	$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 31		$1/\text{fMCK}$ + 31		$1/\text{fMCK}$ + 31		ns
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 250		$1/\text{fMCK}$ + 250		$1/\text{fMCK}$ + 250		ns
Delay time from SCKp $\downarrow$ to SOp output Note 3	tKSO2	$C = 30\text{ pF}$ Note 4	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$2/\text{fMCK}$ + 44		$2/\text{fMCK}$ + 110		$2/\text{fMCK}$ + 110	ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$2/\text{fMCK}$ + 75		$2/\text{fMCK}$ + 110		$2/\text{fMCK}$ + 110	ns
			$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$2/\text{fMCK}$ + 110		$2/\text{fMCK}$ + 110		$2/\text{fMCK}$ + 110	ns
			$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$2/\text{fMCK}$ + 220		$2/\text{fMCK}$ + 220		$2/\text{fMCK}$ + 220	ns

Note 1. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp $\downarrow$ ” and that for the Slp hold time becomes “from SCKp $\downarrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp $\uparrow$ ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output line.

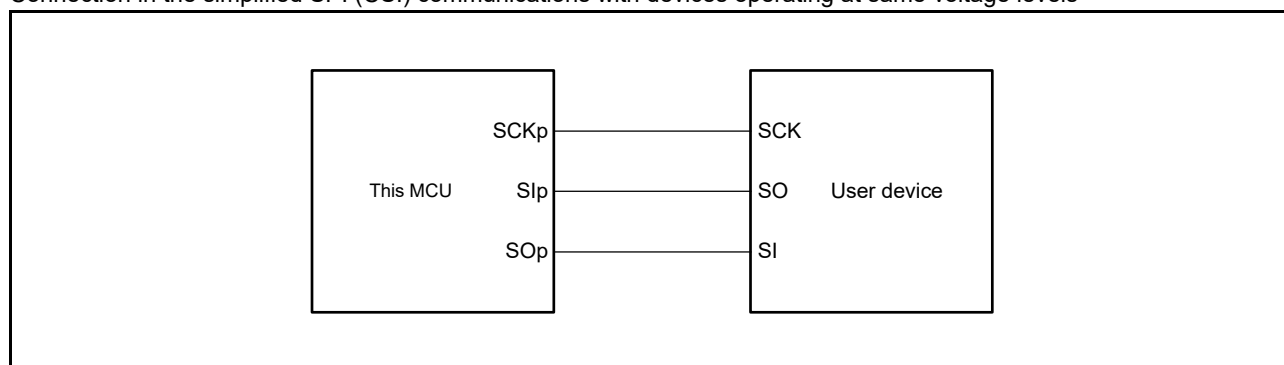
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using a port input mode register (PIMg) and port output mode register (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 5, 7)

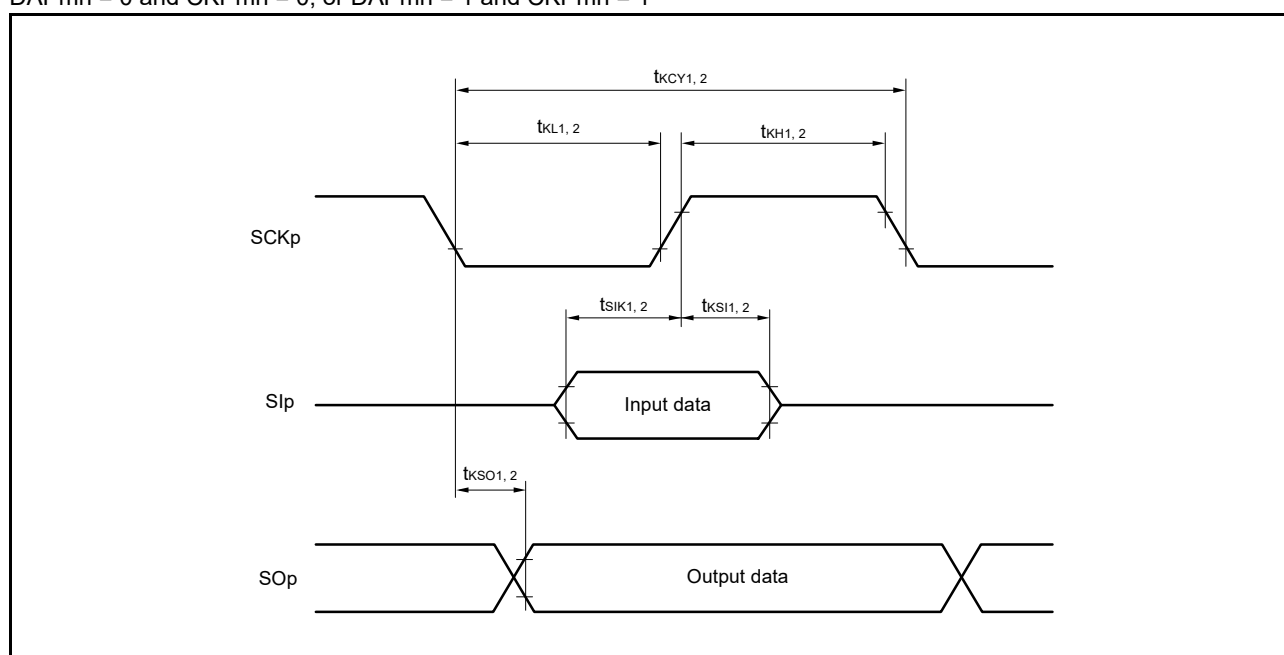
Remark 2. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10, 11).)

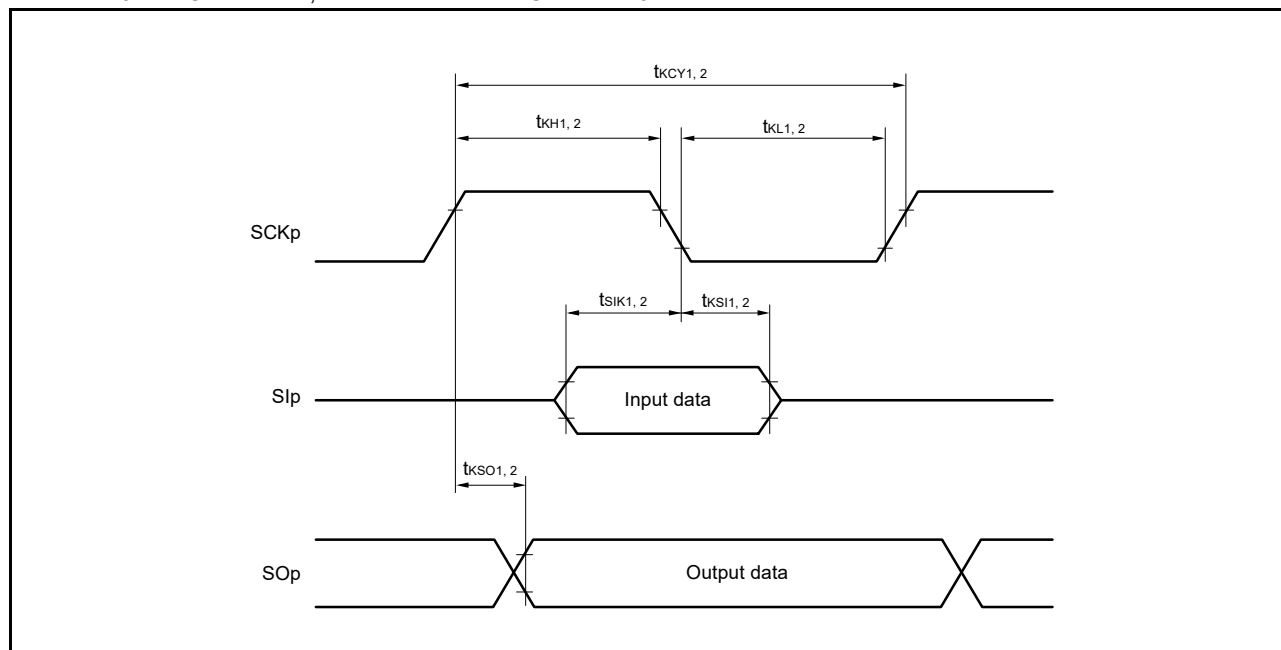
Connection in the simplified SPI (CSI) communications with devices operating at same voltage levels



Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

5. In simplified I²C communications with devices operating at same voltage levels

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	fSCL	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		400Note 1	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400Note 1		400Note 1		400Note 1	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300Note 1		300Note 1		300Note 1	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250Note 1		250Note 1		250Note 1	kHz
Hold time when SCLr is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 56.)

5. In simplified I²C communications with devices operating at same voltage levels(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

(2/2)

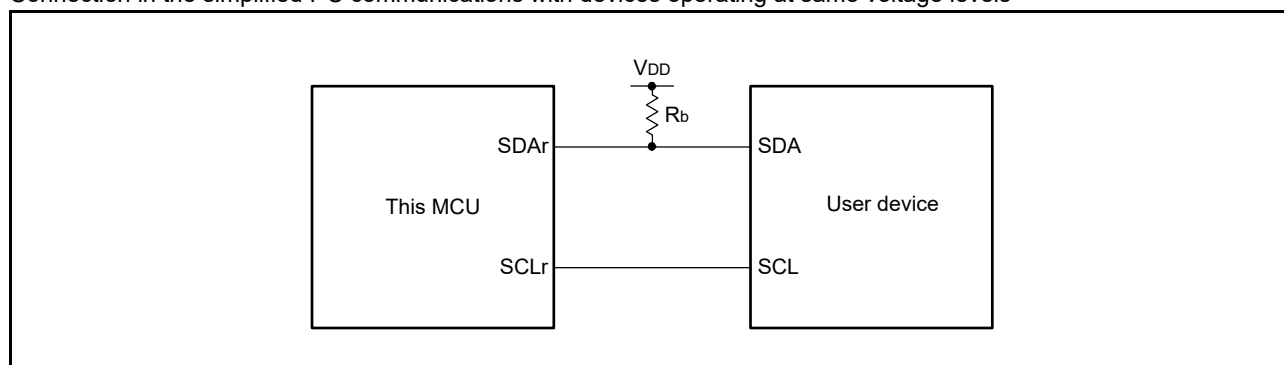
Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note 2		1/f _{MCK} + 85 Note 2		1/f _{MCK} + 145 Note 2		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note 2		1/f _{MCK} + 145 Note 2		1/f _{MCK} + 145 Note 2		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 Note 2		1/f _{MCK} + 230 Note 2		1/f _{MCK} + 230 Note 2		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 Note 2		1/f _{MCK} + 290 Note 2		1/f _{MCK} + 290 Note 2		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.**Note 2.** Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

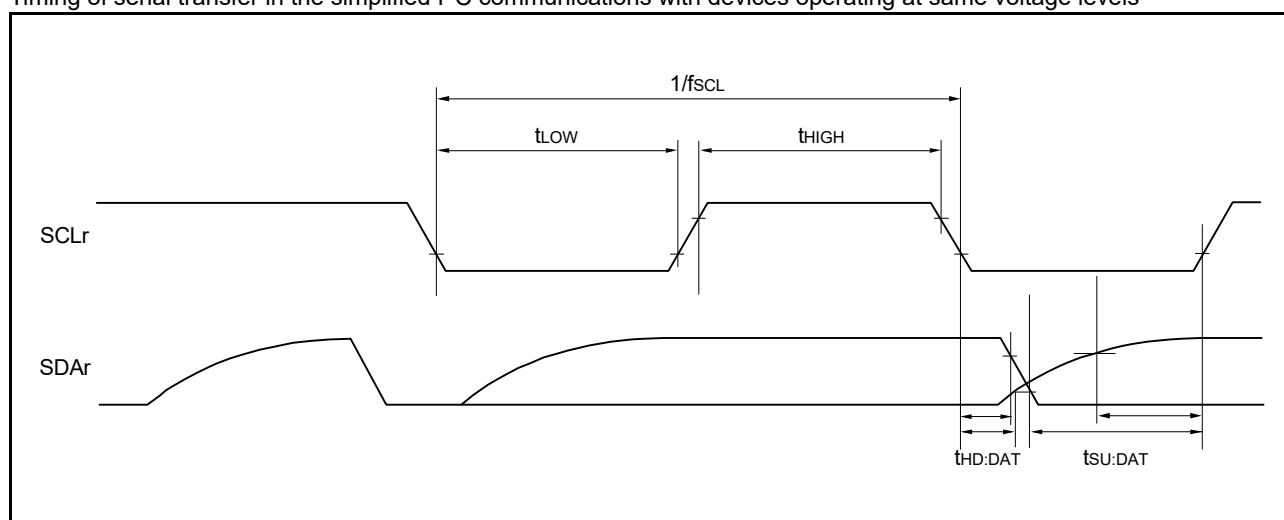
Caution Select the normal input buffer and the N-ch open drain output (withstand voltage of V_{DD} (for the 20- to 48-pin products)/withstand voltage of EV_{DD} (for the 64-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using a port input mode register (PIMg) and port output mode register (POMh).

(Remarks are listed on the next page.)

Connection in the simplified I²C communications with devices operating at same voltage levels



Timing of serial transfer in the simplified I²C communications with devices operating at same voltage levels



Remark 1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 5, 7), h: POM number (g = 0, 1, 5, 7)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(To set this operating clock, use the CKSMn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10, 11).)

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V			fMCK/6 Note 1		fMCK/6 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLKNote 2			5.3		4	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V			fMCK/6 Note 1		fMCK/6 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLKNote 2			5.3		4	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			fMCK/6 Notes 1, 3, 4		fMCK/6 Notes 1, 3	bps
			Theoretical value of the maximum transfer rate fMCK = fCLKNote 2			5.3		4	Mbps

Note 1. Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (1.8 V ≤ VDD ≤ 5.5 V)

4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 24 MHz (1.8 V ≤ VDD ≤ 5.5 V)

4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

LP (low-power main) mode: 2 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Note 3. Use this rate with EVDD0 ≥ Vb.**Note 4.** The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: 2.6 Mbps (max.)

1.8 V ≤ EVDD0 < 2.4 V: 1.3 Mbps (max.)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (withstand voltage of VDD (for the 20- to 48-pin products)/withstand voltage of EVDD (for the 64-pin products)) mode for the TxDq pin by using a port input mode register (PIMg) and port output mode register (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Vb[V]: Communication line voltage**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5)**Remark 3.** fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10, 11).)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of the PIOR15 and PIOR14 bits of the peripheral I/O redirection register (PIOR1) is 01B or 11B.

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V			Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V			2.8Note 2		2.8Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V			Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V			1.2Note 4		1.2Note 4	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V			Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V			0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

(Notes and Caution continue in the next page.)

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use this rate with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

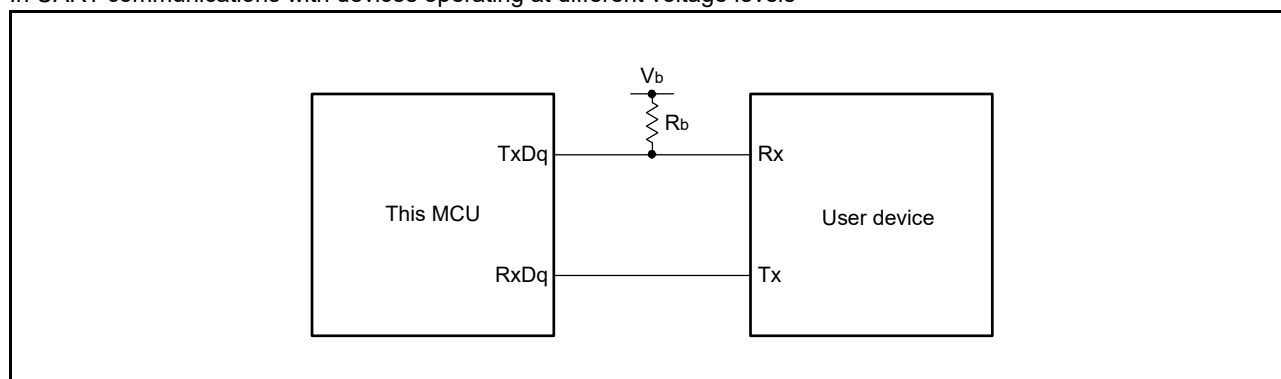
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

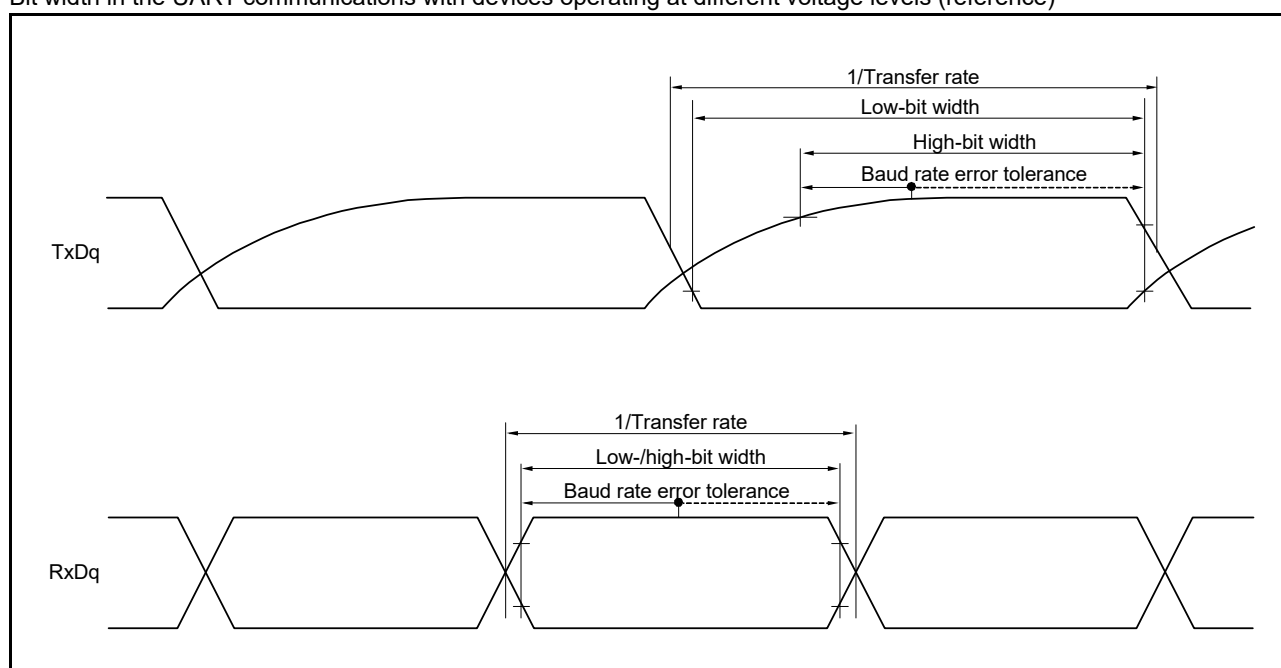
Note 7. This rate is calculated as an example when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (withstand voltage of V_{DD} (for the 20- to 48-pin products)/withstand voltage of EV_{DD} (for the 64-pin products)) mode for the TxDq pin by using a port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

In UART communications with devices operating at different voltage levels



Bit width in the UART communications with devices operating at different voltage levels (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10, 11).)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of the PIOR15 and PIOR14 bits of the peripheral I/O redirection register (PIOR1) is 01B or 11B.

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 $\geq$ 2/fCLK	4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ Vb $\leq$ 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω	200		200		2300		ns
			2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω	300		300		2300		ns
SCKp high-level width	tkH1	4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ Vb $\leq$ 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω		tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω		tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1	4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ Vb $\leq$ 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω		tkCY1/2 - 7		tkCY1/2 - 7		tkCY1/2 - 50		ns
		2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω		tkCY1/2 - 10		tkCY1/2 - 10		tkCY1/2 - 50		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	tsIK1	4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ Vb $\leq$ 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω		58		58		479		ns
		2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω		121		121		479		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	tkSI1	4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ Vb $\leq$ 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω		10		10		10		ns
		2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω		10		10		10		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 1}	tkSO1	4.0 V $\leq$ EVDD0 $\leq$ 5.5 V, 2.7 V $\leq$ Vb $\leq$ 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω			60		60		60	ns
		2.7 V $\leq$ EVDD0 $<$ 4.0 V, 2.3 V $\leq$ Vb $\leq$ 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω			130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) ^{Note 2}	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	23		23		110		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	33		33		110		ns
Slp hold time (from SCKp↓) ^{Note 2}	tKSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	10		10		10		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	10		10		10		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	tKSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		10		10		10	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 20\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		10		10		10	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (for the 20- to 48-pin products)/withstand voltage of EVDD (for the 64-pin products)) mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).)

Remark 4. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/3)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tKCY1	tKCY1 ≥ 4/fCLK	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	300		300		2300		ns
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	500		500		2300		ns
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note} , Cb = 30 pF, Rb = 5.5 kΩ	1150		1150		2300		ns
SCKp high-level width	tKH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		tKCY1/2 - 75		tKCY1/2 - 75		tKCY1/2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		tKCY1/2 - 170		tKCY1/2 - 170		tKCY1/2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note} , Cb = 30 pF, Rb = 5.5 kΩ		tKCY1/2 - 458		tKCY1/2 - 458		tKCY1/2 - 458		ns
SCKp low-level width	tKL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		tKCY1/2 - 12		tKCY1/2 - 12		tKCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		tKCY1/2 - 18		tKCY1/2 - 18		tKCY1/2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note} , Cb = 30 pF, Rb = 5.5 kΩ		tKCY1/2 - 50		tKCY1/2 - 50		tKCY1/2 - 50		ns

Note Use this setting with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of VDD (for the 20- to 48-pin products)/withstand voltage of EVDD (for the 64-pin products)) mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on page 66.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(2/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	81		81		479		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	177		177		479		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	479		479		479		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	tkSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	19		19		19		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	19		19		19		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	19		19		19		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 1}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		100		100		100	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		195		195		195	ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		483		483		483	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use this setting with $\text{EVDD0} \geq \text{Vb}$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (for the 20- to 48-pin products)/withstand voltage of EVDD (for the 64-pin products)) mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on page 66.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(3/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) ^{Note 1}	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	44		44		110		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	44		44		110		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	110		110		110		ns
Slp hold time (from SCKp↓) ^{Note 1}	tkSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	19		19		19		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	19		19		19		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	19		19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 1}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		25		25		25	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		25		25		25	ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		25		25		25	ns

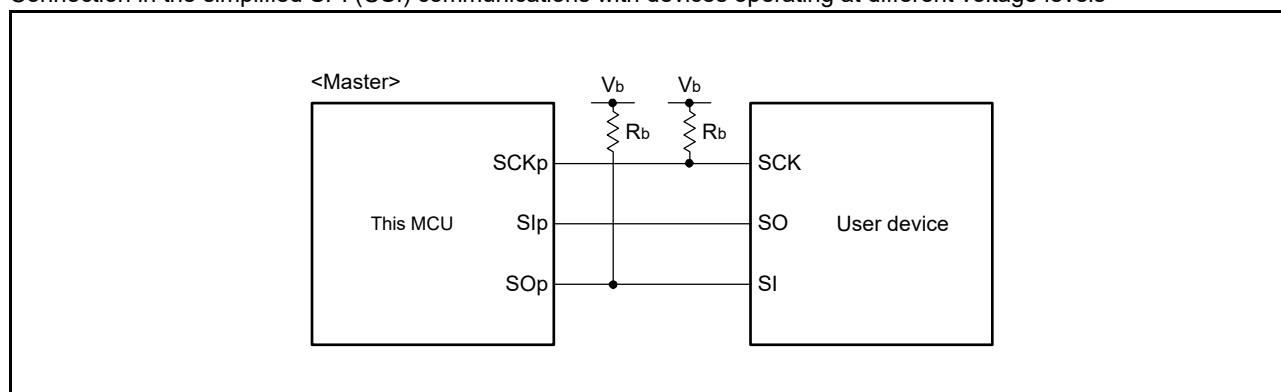
Note 1. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use this setting with $\text{EVDD0} \geq \text{Vb}$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (for the 20- to 48-pin products)/withstand voltage of EVDD (for the 64-pin products)) mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels



Remark 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

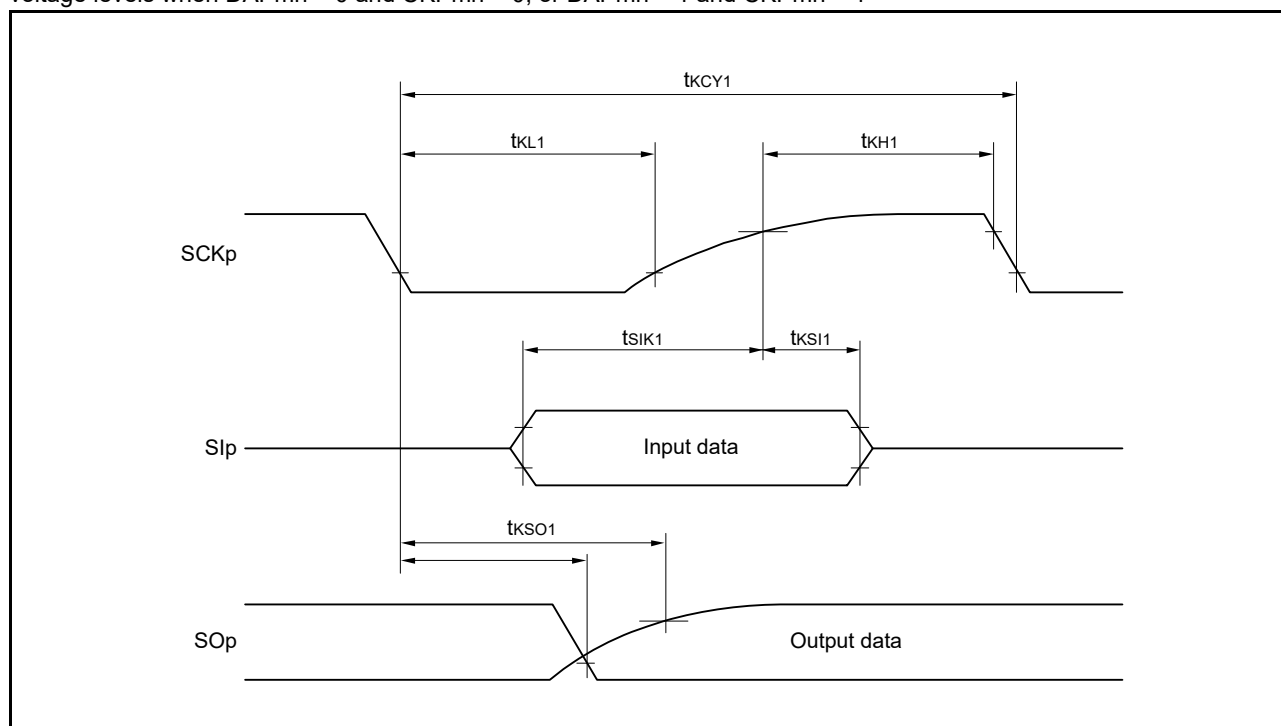
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

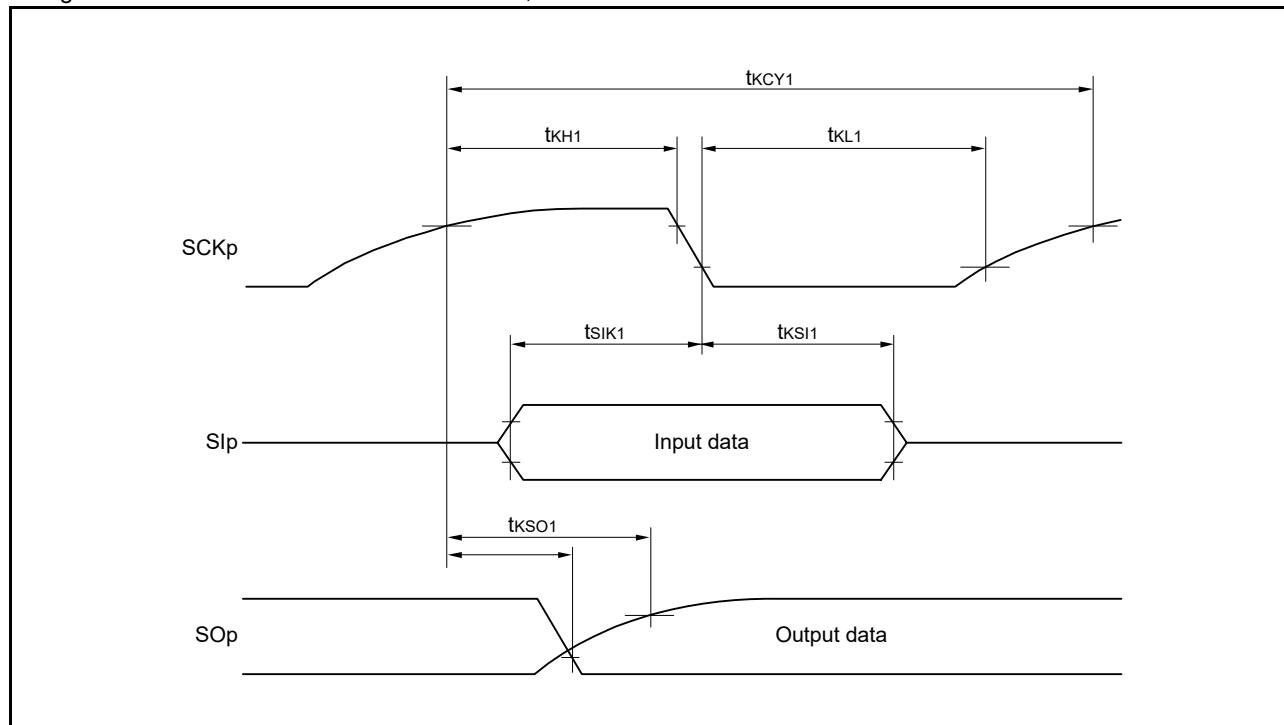
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 02, 10).)

Remark 4. Communications by using CSI01, CSI11, and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$



Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

Remark 2. Communications by using CSI01, CSI11, and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time Note 1	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fMCK	14/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	12/fMCK		12/fMCK		—		ns
			8 MHz < fMCK ≤ 20 MHz	10/fMCK		10/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		8/fMCK		—		ns
			fMCK ≤ 4 MHz	6/fMCK		6/fMCK		10/fMCK		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V,	24 MHz < fMCK	20/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	16/fMCK		16/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		14/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		12/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		8/fMCK		—		ns
			fMCK ≤ 4 MHz	6/fMCK		6/fMCK		10/fMCK		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	24 MHz < fMCK	48/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	36/fMCK		36/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	32/fMCK		32/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	26/fMCK		26/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		16/fMCK		—		ns
			fMCK ≤ 4 MHz	10/fMCK		10/fMCK		10/fMCK		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 70.)

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp high-level width, low-level width	tkH2, tkL2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	tkCY2/2 - 12		tkCY2/2 - 12		tkCY2/2 - 50		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 50		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ Note 2	tkCY2/2 - 50		tkCY2/2 - 50		tkCY2/2 - 50		ns
Slp setup time (to SCKp↑) Note 3	tsIK2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ Note 2	1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns
Slp hold time (from SCKp↑) Note 3	tsIS2		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp↓ to SOp output Note 4	tkSO2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		2/fMCK + 120		2/fMCK + 120		2/fMCK + 573	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		2/fMCK + 214		2/fMCK + 214		2/fMCK + 573	ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ Note 2 , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		2/fMCK + 573		2/fMCK + 573		2/fMCK + 573	ns

Note 1. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Note 2. Use this setting with $\text{EVDD0} \geq \text{Vb}$.

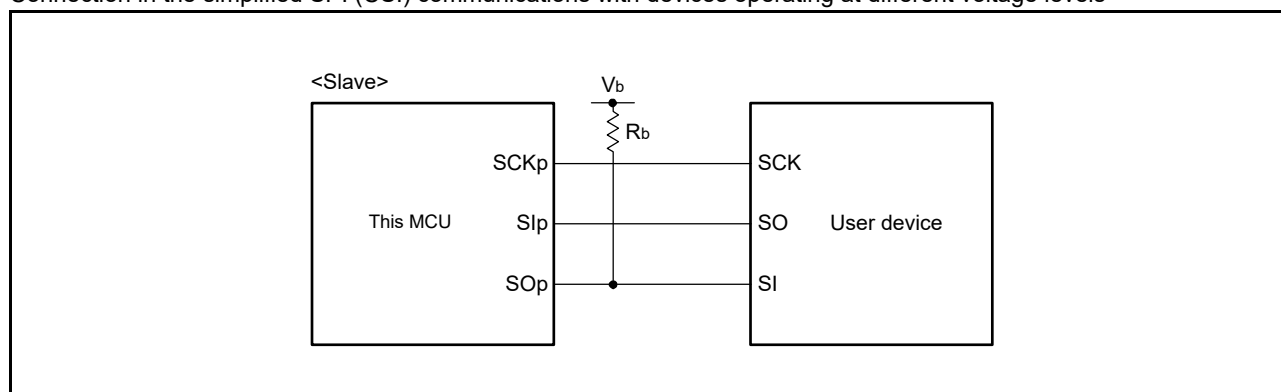
Note 3. This setting applies when $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp↓” and Slp hold time becomes “from SCKp↓” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

Note 4. This setting applies when $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp↑” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (for the 20- to 48-pin products)/withstand voltage of EVDD (for the 64-pin products)) mode for the SOp pin and SCKp pin by using a port input mode register (PIMg) and port output mode register (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels



Remark 1. $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage

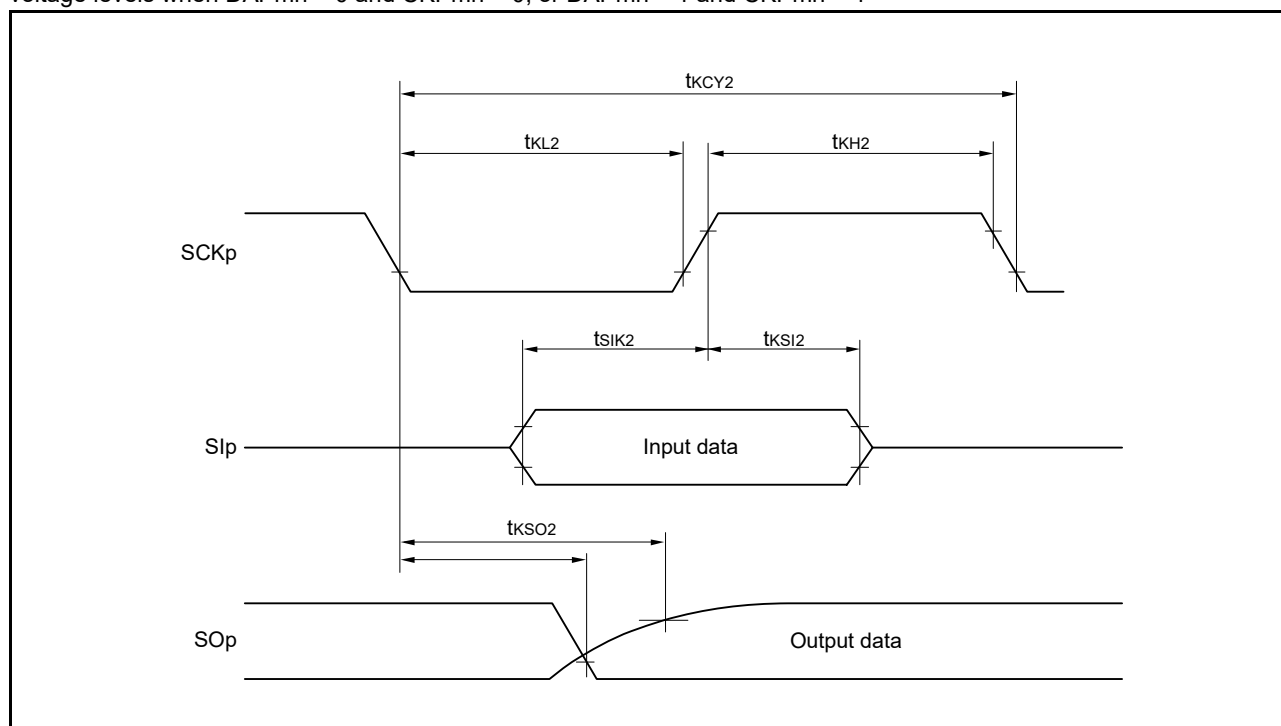
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

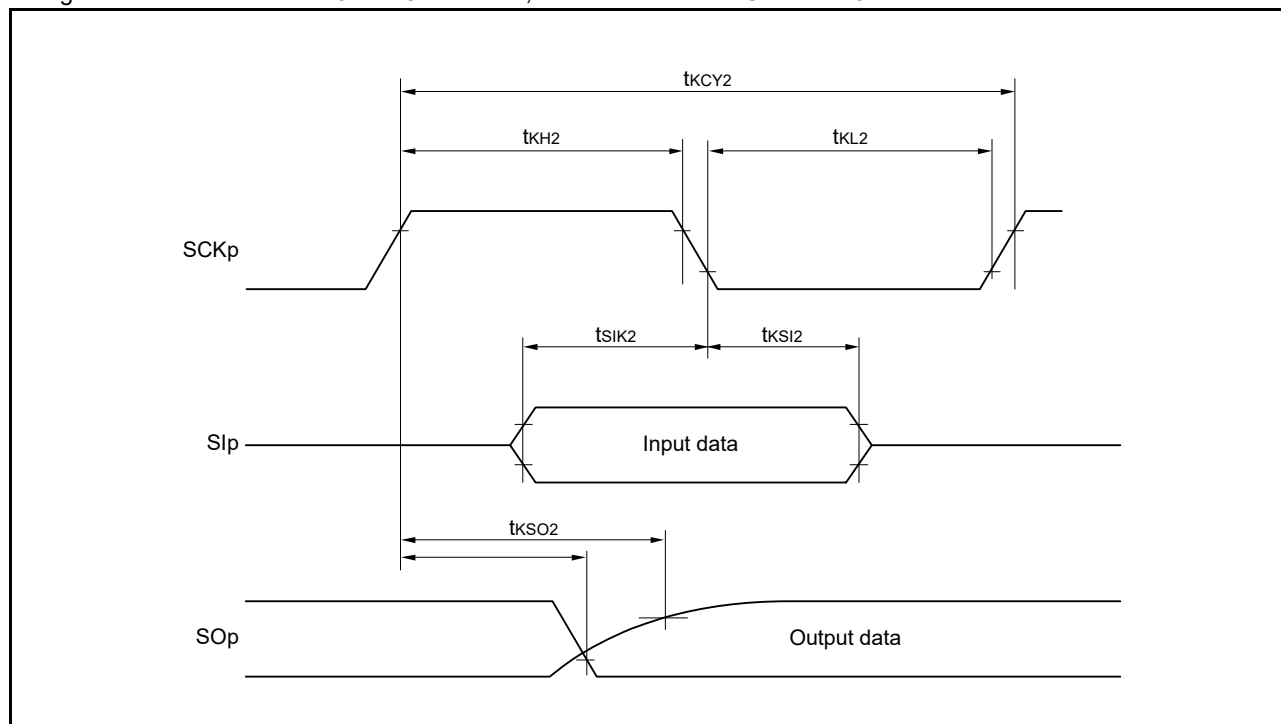
(To set this operating clock, use the CKS_{mn} bit in the serial mode register mn (SMR_{mn}) (m: Unit number, n: Channel number = 00, 02, 10).)

Remark 4. Communications by using CSI01, CSI11, and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1



Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 02, 10), g: PIM and POM number (g = 0, 1)

Remark 2. Communications by using CSI01, CSI11, and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr is low	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr is high	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		600		610		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		ns

10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, and 3 V)(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V)

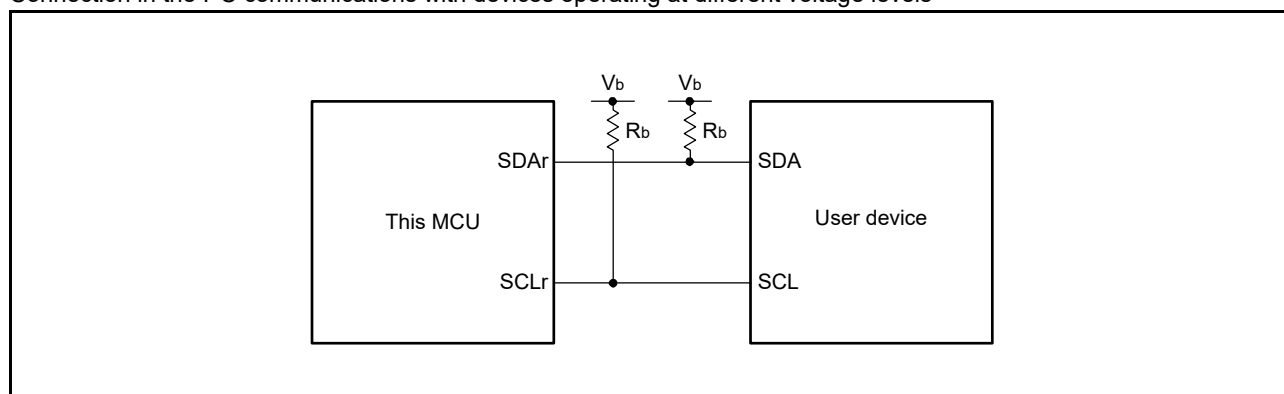
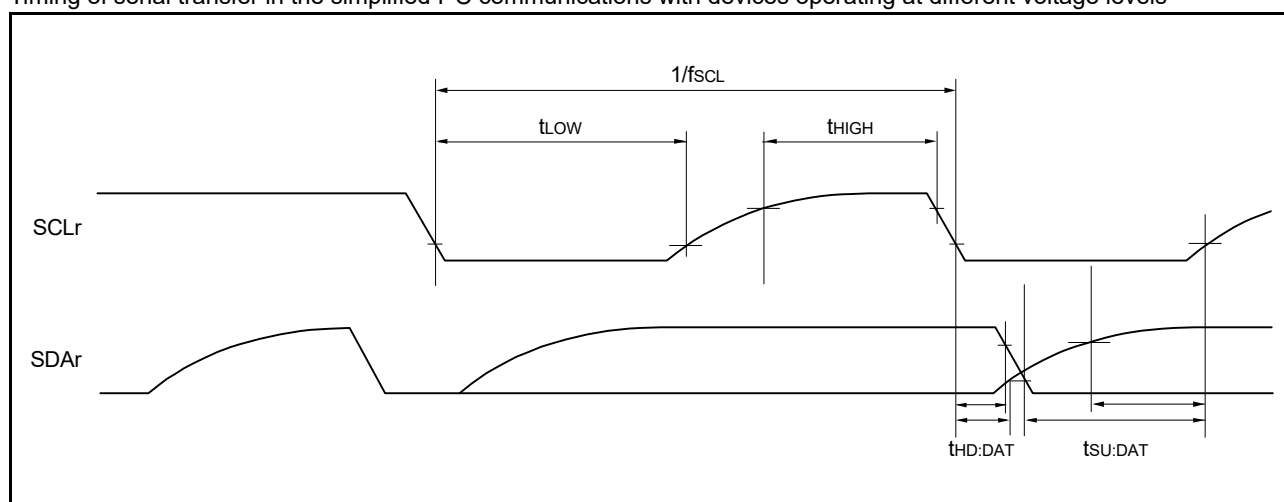
(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	tsu:DAT	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 3		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
Data hold time (transmission)	t _{HD} :DAT	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.**Note 2.** Use this setting with EV_{DD0} ≥ V_b.**Note 3.** Set f_{MCK} so that it will not exceed the hold time when SCL_r is low or high.

Caution Select the TTL input buffer and the N-ch open drain output (withstand voltage of V_{DD} (for the 20- to 48-pin products)/withstand voltage of EV_{DD} (for the 64-pin products)) mode for the SDA_r pin and the N-ch open drain output (withstand voltage of V_{DD} (for the 20- to 48-pin products)/withstand voltage of EV_{DD} (for the 64-pin products)) mode for the SCL_r pin by using a port input mode register (PIMg) and port output mode register (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the I²C communications with devices operating at different voltage levelsTiming of serial transfer in the simplified I²C communications with devices operating at different voltage levels

Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM and POM number (g = 0, 1)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 02, 10).)

2.5.2 Serial interface UARTA

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	153600	bps

Caution Select the normal input buffer for the RxDAn pin and the normal output mode for the TxDAn pin by using a port input mode register (PIMg) and port output mode register (POMg).

Remark 1. g: PIM number (g = 0, 3, 7), h: POM number (h = 0, 3, 7)

Remark 2. n: Unit number (n = 0)

2.5.3 Serial interface IICA

1. I²C standard mode

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Standard mode: fCLK ≥ 1 MHz	0		100	kHz
Setup time of restart condition	tSU:STA		4.7			μs
Hold time ^{Note 1}	tHD:STA		4.0			μs
Hold time when SCLA0 is low	tLOW		4.7			μs
Hold time when SCLA0 is high	tHIGH		4.0			μs
Data setup time (reception)	tSU:DAT		250			ns
Data hold time (transmission) ^{Note 2}	tHD:DAT		0		3.45	μs
Setup time of stop condition	tSU:STO		4.0			μs
Bus-free time	tBUF		4.7			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The listed frequency and times apply even when the PIOR02 bit in the peripheral I/O redirection register (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
Cb = 400 pF, Rb = 2.7 kΩ

2. I²C fast mode(T_A = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz 1.8 V ≤ EVDD0 ≤ 5.5 V	0		400	kHz
Setup time of restart condition	tSU:STA	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Hold time ^{Note 1}	tHD:STA	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Hold time when SCLA0 is low	tLOW	1.8 V ≤ EVDD0 ≤ 5.5 V	1.3			μs
Hold time when SCLA0 is high	tHIGH	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Data setup time (reception)	tSU:DAT	1.8 V ≤ EVDD0 ≤ 5.5 V	100			ns
Data hold time (transmission) ^{Note 2}	tHD:DAT	1.8 V ≤ EVDD0 ≤ 5.5 V	0		0.9	μs
Setup time of stop condition	tSU:STO	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Bus-free time	tBUF	1.8 V ≤ EVDD0 ≤ 5.5 V	1.3			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when the PIOR02 bit in the peripheral I/O redirection register (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 320 pF, R_b = 1.1 kΩ

3. I²C fast mode plus(T_A = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

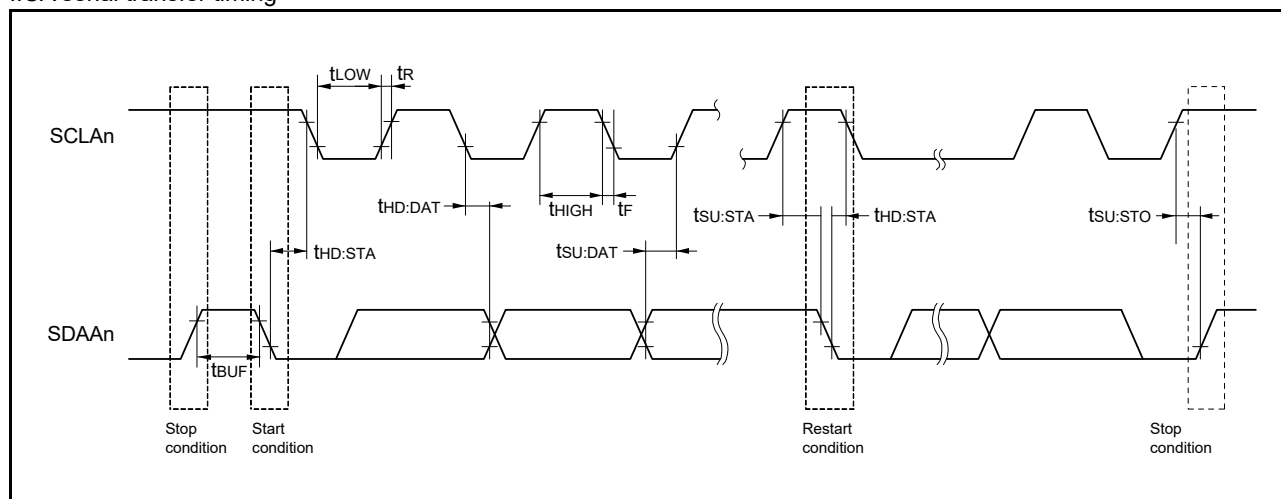
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK ≥ 10 MHz 2.7 V ≤ EVDD0 ≤ 5.5 V	0		1000	kHz
Setup time of restart condition	tSU:STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Hold time ^{Note 1}	tHD:STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Hold time when SCLA0 is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5			μs
Hold time when SCLA0 is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Data setup time (reception)	tSU:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	50			ns
Data hold time (transmission) ^{Note 2}	tHD:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0		0.45	μs
Setup time of stop condition	tSU:STO	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when the PIOR02 bit in the peripheral I/O redirection register (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing

**Remark** n = 0

2.6 Characteristics of the Analog Circuits

2.6.1 Characteristics of the A/D converter for $T_A = -40$ to 85°C

Reference for the characteristics of the A/D converter

Reference voltage	Reference voltage (+) = AV_{REFP}	Reference voltage (+) = V_{DD}	Reference voltage (+) = $VBGR$
Input Channel	Reference voltage (–) = AV_{REFM}	Reference voltage (–) = V_{SS}	Reference voltage (–) = AV_{REFM}
ANI0 to ANI7	See 2.6.1 (1)	See 2.6.1 (3)	See 2.6.1 (4)
ANI16 to ANI19	See 2.6.1 (2)		
Internal reference voltage, temperature sensor output voltage	See 2.6.1 (1)		—

- (1) Reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), conversion target: ANI2 to ANI7, internal reference voltage, temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, reference voltage (+) = AV_{REFP} , reference voltage (–) = $AV_{REFM} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}	1.2	± 7.0	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI2 to ANI7	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 4}	Ezs	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.25	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 0.50	%FSR
Full-scale error ^{Notes 1, 4}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.25	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 5.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 1.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 2.0	LSB
Analog input voltage	VAIN	ANI2 to ANI7	0		AV_{REFP}	V
		Internal reference voltage ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)	$VBGR$ ^{Note 5}			V
		Temperature sensor output voltage ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)	$VTMP25$ ^{Note 5}			V

(Notes are listed on the next page.)

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. When $AV_{REFP} < V_{DD}$, the maximum values are as follows.

- Overall error: Add ± 1.0 LSB to the maximum value when $V_{DD} = AV_{REFP}$.
- Zero-scale/full-scale error: Add $\pm 0.05\%$ FSR to the maximum value when $V_{DD} = AV_{REFP}$.
- Integral linearity error and differential linearity error: Add ± 0.5 LSB to the maximum value when $V_{DD} = AV_{REFP}$.

Note 3. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μ s and 95 μ s.

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 5. See **2.6.3 Characteristics of the temperature sensor and internal reference voltage**.

- (2) Reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), conversion target: ANI16 to ANI19

($T_A = -40$ to $+85^{\circ}\text{C}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, reference voltage (+) = AV_{REFP} , reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}	1.2	± 8.5	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI16 to ANI19	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error ^{Notes 1, 4}	Ezs	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 0.60	%FSR
Full-scale error ^{Notes 1, 4}	Efs	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 6.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 3}		± 2.5	LSB
Analog input voltage	VAIN	ANI16 to ANI19	0		AV_{REFP}	V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. When $AV_{REFP} < V_{DD}$, the maximum values are as follows.

- Overall error: Add ± 4.0 LSB to the maximum value when $V_{DD} = AV_{REFP}$.
- Zero-scale/full-scale error: Add $\pm 0.20\%$ FSR to the maximum value when $V_{DD} = AV_{REFP}$.
- Integral linearity error/differential linearity error: Add ± 2.0 LSB to the maximum value when $V_{DD} = AV_{REFP}$.

Note 3. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs .

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

- (3) Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), conversion target: ANI0 to ANI7, ANI16 to ANI19, internal reference voltage^{Note 1}, temperature sensor output voltage^{Note 1}

($T_A = -40$ to $+85^{\circ}\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, reference voltage (+) = AV_{REFP} , reference voltage (-) = V_{SS})

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 2}	AINL	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ^{Note 3}		1.2	± 10.5	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI0 to ANI7, ANI16 to ANI19	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 2, 4}	Ezs	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ^{Note 3}			± 0.85	%FSR
Full-scale error ^{Notes 2, 4}	EFS	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ^{Note 3}			± 0.85	%FSR
Integral linearity error ^{Note 2}	ILE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ^{Note 3}			± 6.0	LSB
Differential linearity error ^{Note 2}	DLE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ^{Note 3}			± 2.5	LSB
Analog input voltage	VAIN	ANI0 to ANI7, ANI16 to ANI19		0		V_{DD}	V
		Internal reference voltage ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)		V_{BGR} ^{Note 5}			V
		Temperature sensor output voltage ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)		V_{TMPS25} ^{Note 5}			V

Note 1. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, V_{DD} must be at least 1.8 V.

Note 2. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 3. The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57 μs and 95 μs .

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 5. See 2.6.3 Characteristics of the temperature sensor and internal reference voltage.

- (4) Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI0, ANI2 to ANI7, ANI16 to ANI19

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = VBGR^{Note 1}, reference voltage (-) = AVREFM^{Note 2} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			bit
Conversion time	tCONV		17		39	μs
Zero-scale error ^{Notes 3, 4}	Ezs				±0.60	%FSR
Integral linearity error ^{Note 3}	ILE				±2.0	LSB
Differential linearity error ^{Note 3}	DLE				±1.0	LSB
Analog input voltage	VAIN		0		VBGR ^{Note 1}	V

Note 1. See 2.6.3 Characteristics of the temperature sensor and internal reference voltage.

Note 2. When reference voltage (-) = VSS, the maximum values are as follows.

- Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (-) = AVREFM.
- Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (-) = AVREFM.
- Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (-) = AVREFM.

Note 3. This value does not include the quantization error (±1/2 LSB).

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

2.6.2 Characteristics of the A/D converter for $T_A = -40$ to 105°C

Reference for the characteristics of the A/D converter

Reference voltage	Reference voltage (+) = AVREFP	Reference voltage (+) = VDD	Reference voltage (+) = VBGR
Input Channel	Reference voltage (–) = AVREFM	Reference voltage (–) = VSS	Reference voltage (–) = AVREFM
ANI0 to ANI7	See 2.6.2 (1)	See 2.6.2 (3)	See 2.6.2 (4)
ANI16 to ANI19	See 2.6.2 (2)		
Internal reference voltage, temperature sensor output voltage	See 2.6.2 (1)		—

- (1) Reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI7, internal reference voltage, temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{AVREFP} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$, reference voltage (+) = AVREFP, reference voltage (–) = AVREFM = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AVREFP = VDD ^{Note 2} $2.4\text{ V} \leq \text{AVREFP} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI2 to ANI7	$3.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	17	39	μs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage	$3.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 3}	EZS	10-bit resolution AVREFP = VDD ^{Note 2} $2.4\text{ V} \leq \text{AVREFP} \leq 5.5\text{ V}$			± 0.25	%FSR
Full-scale error ^{Notes 1, 3}	EFS	10-bit resolution AVREFP = VDD ^{Note 2} $2.4\text{ V} \leq \text{AVREFP} \leq 5.5\text{ V}$			± 0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AVREFP = VDD ^{Note 2} $2.4\text{ V} \leq \text{AVREFP} \leq 5.5\text{ V}$			± 2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AVREFP = VDD ^{Note 2} $2.4\text{ V} \leq \text{AVREFP} \leq 5.5\text{ V}$			± 1.5	LSB
Analog input voltage	VAIN	ANI2 to ANI7	0		AVREFP	V
		Internal reference voltage	VBGR ^{Note 4}			V
		Temperature sensor output voltage	VTMP25 ^{Note 4}			V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. When AVREFP < VDD, the maximum values are as follows.

- Overall error: Add ± 1.0 LSB to the maximum value when $\text{VDD} = \text{AVREFP}$.
- Zero-scale/full-scale error: Add $\pm 0.05\%$ FSR to the maximum value when $\text{VDD} = \text{AVREFP}$.
- Integral linearity error and differential linearity error: Add ± 0.5 LSB to the maximum value when $\text{VDD} = \text{AVREFP}$.

Note 3. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 4. See 2.6.3 Characteristics of the temperature sensor and internal reference voltage.

- (2) Reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), conversion target: ANI16 to ANI19

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, reference voltage (+) = AV_{REFP} , reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	± 5.0	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI16 to ANI19	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 3}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.35	%FSR
Full-scale error ^{Notes 1, 3}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 2}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	VAIN	ANI16 to ANI19		0		AV_{REFP}	V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. When $AV_{REFP} < V_{DD}$, the maximum values are as follows.

- Overall error: Add ± 4.0 LSB to the maximum value when $V_{DD} = AV_{REFP}$.
- Zero-scale/full-scale error: Add $\pm 0.20\%$ FSR to the maximum value when $V_{DD} = AV_{REFP}$.
- Integral linearity error/differential linearity error: Add ± 2.0 LSB to the maximum value when $V_{DD} = AV_{REFP}$.

Note 3. This value is indicated as a ratio (%FSR) to the full-scale value.

- (3) Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0),
conversion target: ANI0 to ANI7, ANI16 to ANI19, internal reference voltage, temperature sensor output voltage

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, reference voltage (+) = V_{DD} , reference voltage (-) = V_{SS})

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	tCONV	10-bit resolution conversion target: ANI0 to ANI7, ANI16 to ANI19	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution conversion target: Internal reference voltage, temperature sensor output voltage	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI7, ANI16 to ANI19		0		V_{DD}	V
		Internal reference voltage		V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage		V_{TMPS25} ^{Note 3}			V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. See 2.6.3 Characteristics of the temperature sensor and internal reference voltage.

- (4) Reference voltage (+) = Internal reference voltage (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI0, ANI2 to ANI7, ANI16 to ANI19

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = VBGR^{Note 1}, reference voltage (-) = AVREFM^{Note 2} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			bit
Conversion time	tCONV		17		39	μs
Zero-scale error ^{Notes 3, 4}	Ezs				±0.60	%FSR
Integral linearity error ^{Note 3}	ILE				±2.0	LSB
Differential linearity error ^{Note 3}	DLE				±1.0	LSB
Analog input voltage	VAIN		0		VBGR ^{Note 1}	V

Note 1. See 2.6.3 Characteristics of the temperature sensor and internal reference voltage.

Note 2. When reference voltage (-) = VSS, the maximum values are as follows.

- Zero-scale error: Add ±0.35%FSR to the maximum value when reference voltage (-) = AVREFM.
- Integral linearity error: Add ±0.5 LSB to the maximum value when reference voltage (-) = AVREFM.
- Differential linearity error: Add ±0.2 LSB to the maximum value when reference voltage (-) = AVREFM.

Note 3. This value does not include the quantization error (±1/2 LSB).

Note 4. This value is indicated as a ratio (%FSR) to the full-scale value.

2.6.3 Characteristics of the temperature sensor and internal reference voltage

($T_A = -40$ to $+105^{\circ}\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

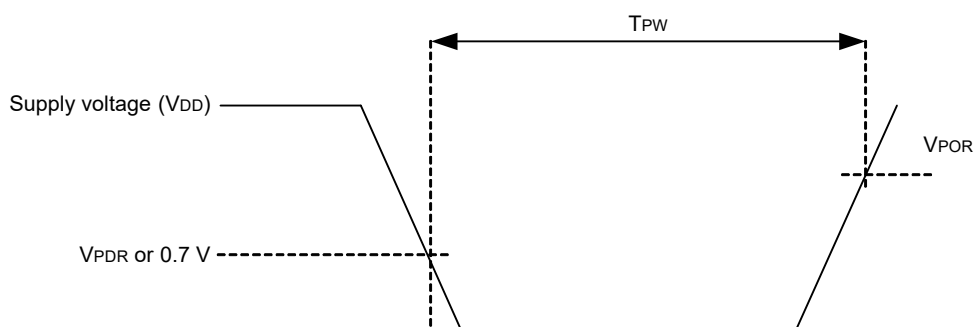
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, $T_A = +25^{\circ}\text{C}$		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.42	1.48	1.54	V
Temperature coefficient	FVTMPS	Temperature dependency of the temperature sensor voltage		-3.3		mV/ $^{\circ}\text{C}$
Operation stabilization wait time	tAMP		5			μs

2.6.4 Characteristics of the POR circuit

($T_A = -40$ to $+105^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	VPOR, VPDR		1.43	1.50	1.57	V
Minimum pulse width ^{Note}	TPW		300			μs

Note This width is the minimum time required for a POR reset when V_{DD} falls below V_{PDR} . This width is also the minimum time required for a POR reset from when V_{DD} falls below 0.7 V to when V_{DD} exceeds V_{POR} in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.5 Characteristics of the LVD circuit

1. LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

($T_A = -40$ to $+105^{\circ}\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	VLVD00	The power supply voltage is rising.	3.84	3.96	4.08	V
			The power supply voltage is falling.	3.76	3.88	4.00	V
		VLVD01	The power supply voltage is rising.	2.88	2.97	3.06	V
			The power supply voltage is falling.	2.82	2.91	3.00	V
		VLVD02	The power supply voltage is rising.	2.59	2.67	2.75	V
			The power supply voltage is falling.	2.54	2.62	2.70	V
		VLVD03	The power supply voltage is rising.	2.31	2.38	2.45	V
			The power supply voltage is falling.	2.26	2.33	2.40	V
		VLVD04	The power supply voltage is rising.	1.84	1.90	1.95	V
			The power supply voltage is falling.	1.80	1.86	1.91	V
		VLVD05	The power supply voltage is rising.	1.64	1.69	1.74	V
			The power supply voltage is falling.	1.60	1.65	1.70	V
Minimum pulse width		tLW		500			μs
Detection delay time						500	μs

2. LVD1 Detection Voltage in the Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	VLVD10	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		VLVD11	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		VLVD12	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		VLVD13	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.47	3.54	V
		VLVD14	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		VLVD15	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		VLVD16	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		VLVD17	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
		VLVD18	The power supply voltage is rising.	2.61	2.66	2.71	V
			The power supply voltage is falling.	2.55	2.60	2.65	V
		VLVD19	The power supply voltage is rising.	2.45	2.50	2.55	V
			The power supply voltage is falling.	2.40	2.45	2.50	V
		VLVD110	The power supply voltage is rising.	2.35	2.40	2.45	V
			The power supply voltage is falling.	2.30	2.35	2.40	V
		VLVD111	The power supply voltage is rising.	2.25	2.30	2.34	V
			The power supply voltage is falling.	2.20	2.25	2.29	V
		VLVD112	The power supply voltage is rising.	2.15	2.20	2.24	V
			The power supply voltage is falling.	2.10	2.15	2.19	V
		VLVD113	The power supply voltage is rising.	2.05	2.09	2.13	V
			The power supply voltage is falling.	2.00	2.04	2.08	V
		VLVD114	The power supply voltage is rising.	1.94	1.98	2.02	V
			The power supply voltage is falling.	1.90	1.94	1.98	V
		VLVD115 Note	The power supply voltage is rising.	1.84	1.88	1.91	V
			The power supply voltage is falling.	1.80	1.84	1.87	V
		VLVD116 Note	The power supply voltage is rising.	1.74	1.78	1.81	V
			The power supply voltage is falling.	1.70	1.74	1.77	V
		VLVD117 Note	The power supply voltage is rising.	1.64	1.67	1.70	V
			The power supply voltage is falling.	1.60	1.63	1.66	V
Minimum pulse width		tLW		500			μs
Detection delay time						500	μs

Note This setting can only be used when LVD0 is disabled.

2.6.6 Characteristics of the rising slope of the power supply voltage

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

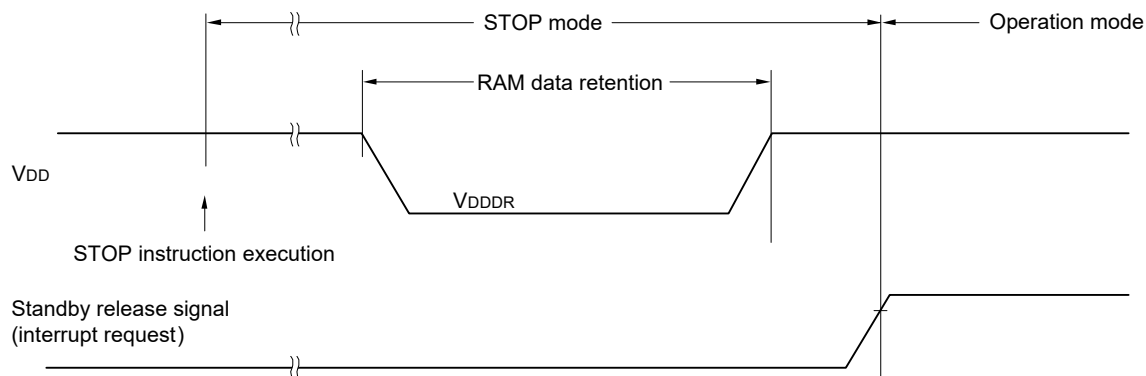
Caution **Make sure to keep the internal reset state by LVD0 or an external reset until VDD reaches the operating voltage range shown in AC characteristics.**

2.7 Characteristics of Retention of RAM Data

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	VDDDR		1.43 ^{Note}		5.5	V

Note This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.8 Characteristics of Flash Memory Programming

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
CPU/peripheral hardware clock frequency	fCLK		1		32	MHz	
Number of code flash memory rewrites ^{Notes 1, 2, 3}	Cerwr	Retained for 10 years TA = +85°C	10,000			Times	
		Retained for 20 years TA = +85°C	1,000				
Number of data flash memory rewrites ^{Notes 1, 2, 3}		Retained for 1 year TA = +25°C		1,000,000			
		Retained for 5 years TA = +85°C	100,000				
		Retained for 20 years TA = +85°C	10,000				

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when using flash memory programmer and Renesas Electronics self programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

1. Code flash memory

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	tP4	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs
Erase time	2 Kbytes	tE2K	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	2 Kbytes	tBC2K	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	μs
Time taken to forcibly stop the erasure		tSED	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
Security setting time		tAWSSAS	—	18.2	526.2	—	14.4	469.2	—	12.5	441.1	—	11.6	427.1	—	11.3	422.6	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2. Data flash memory

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	tP4	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs
Erase time	256 bytes	tE2K	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	256 bytes	tBC2K	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	μs
Time taken to forcibly stop the erasure		tSED	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
Time until reading starts following setting DFLCTL.DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	μs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Dedicated Flash Memory Programmer Communication (UART)

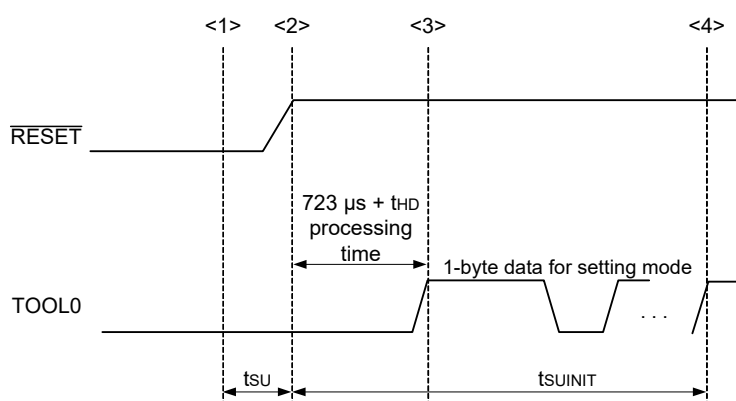
($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	tsuINIT	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	tsu	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	tHD	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.

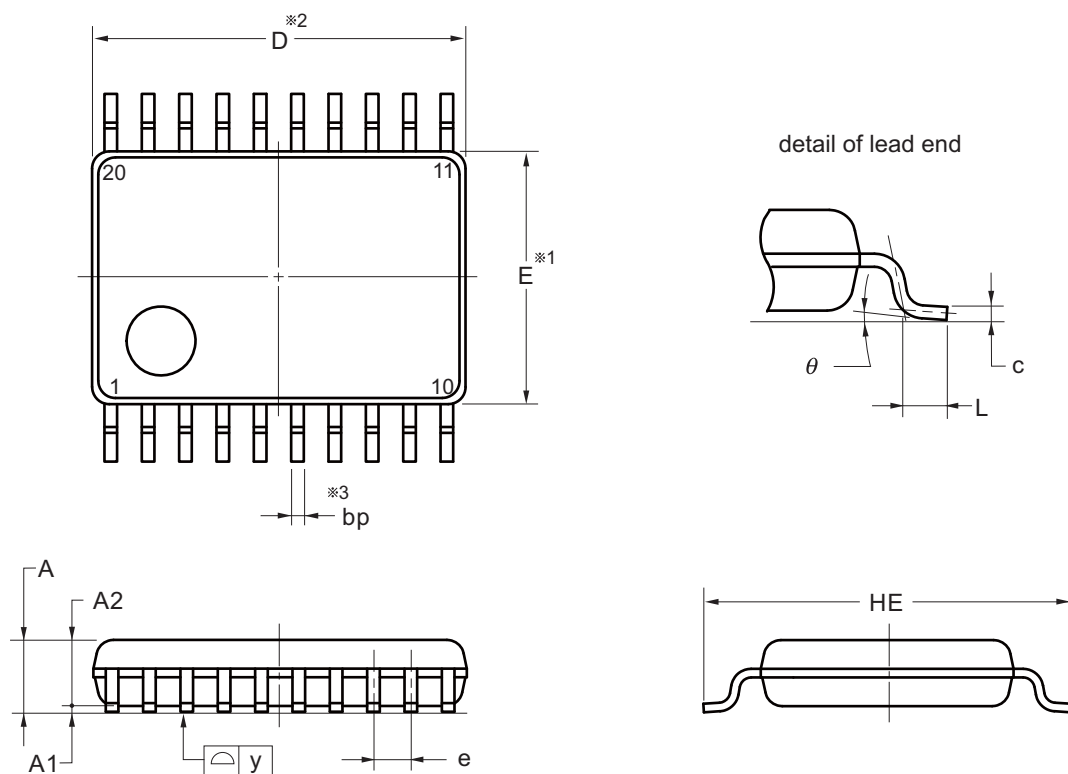
tsu: Time to release the external reset after the TOOL0 pin is set to the low level

tHD: Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

3. Package Drawings

3.1 20-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



NOTE

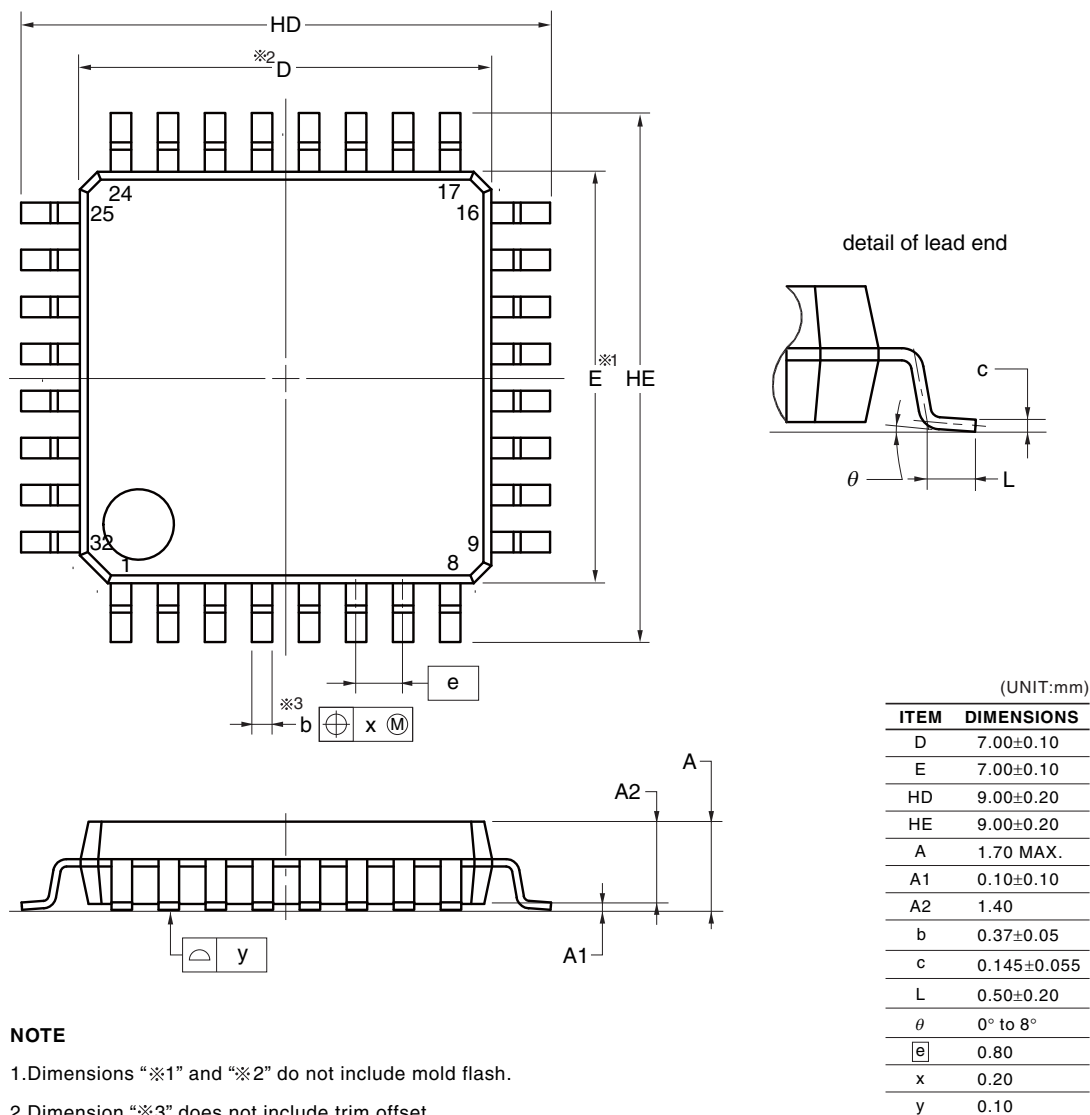
1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

(UNIT:mm)	
ITEM	DIMENSIONS
D	6.50±0.10
E	4.40±0.10
HE	6.40±0.20
A	1.45 MAX.
A1	0.10±0.10
A2	1.15
e	0.65±0.12
bp	0.22 ^{+0.10} _{-0.05}
c	0.15 ^{+0.05} _{-0.02}
L	0.50±0.20
y	0.10
θ	0° to 10°

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3.2 32-pin Products

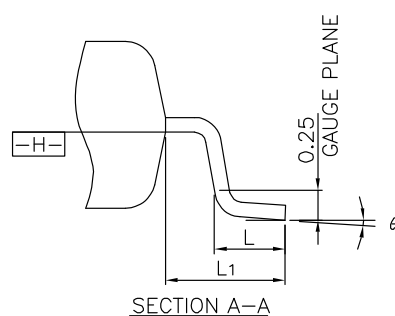
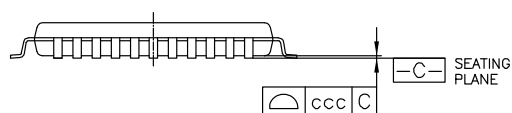
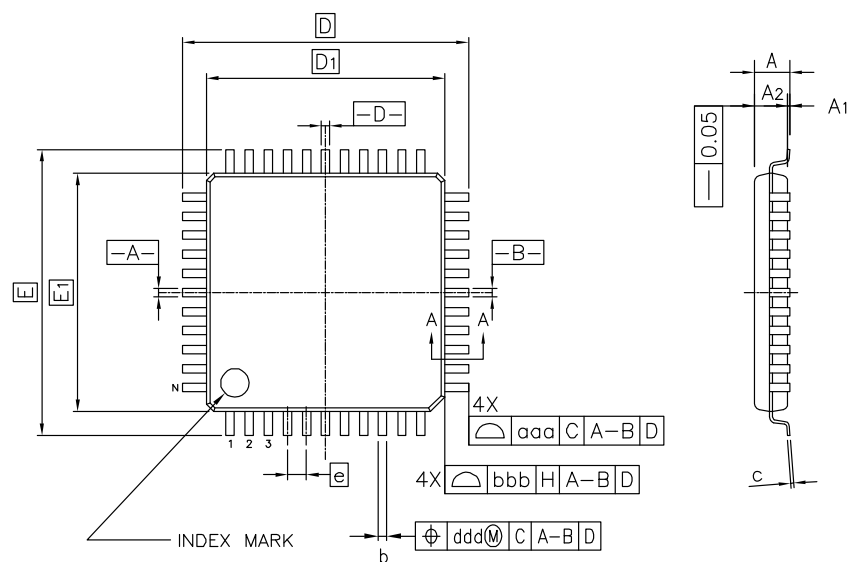
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



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3.3 44-pin Products

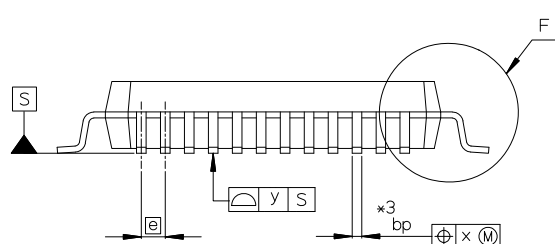
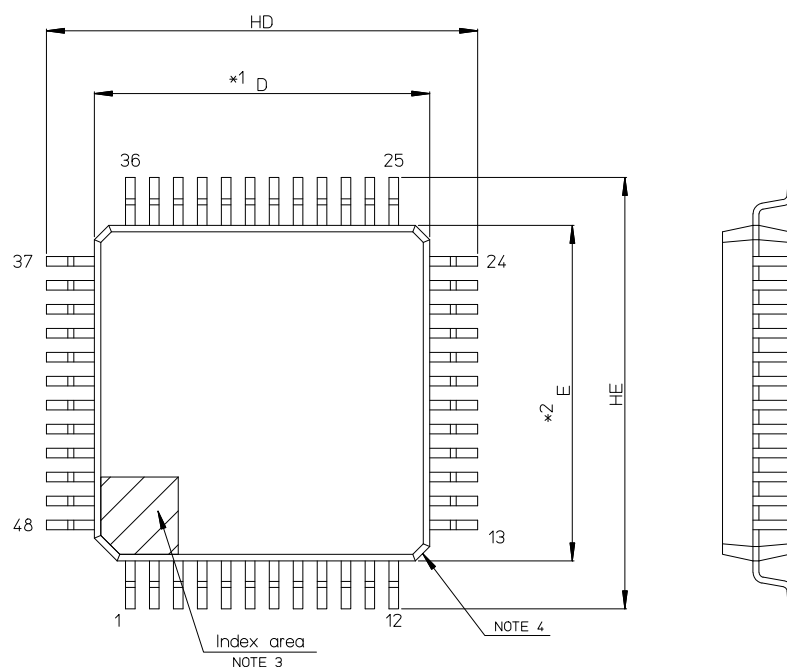
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP44-10x10-0.80	PLQP0044GF-A	0.3



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.70
A ₁	0.05	—	0.15
A ₂	1.35	1.40	1.45
D	12.00 BSC.		
D ₁	10.00 BSC.		
E	12.00 BSC.		
E ₁	10.00 BSC.		
N	—	44	—
e	0.80 BSC.		
b	0.30	0.37	0.45
c	0.09	—	0.20
θ	0°	3.5°	8°
L	0.45	0.60	0.75
L ₁	1.00 REF.		
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.10
ddd	—	—	0.20

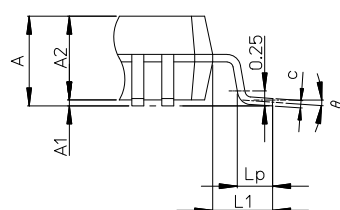
3.4 48-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2g



NOTE)

1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

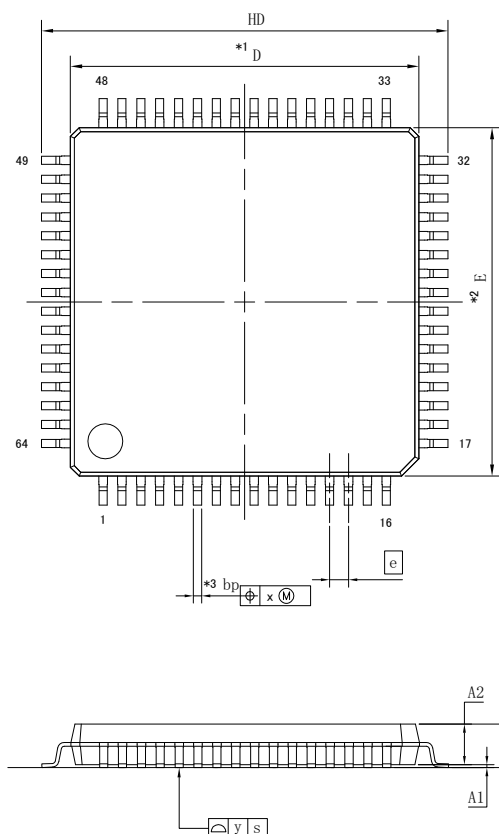


Detail F

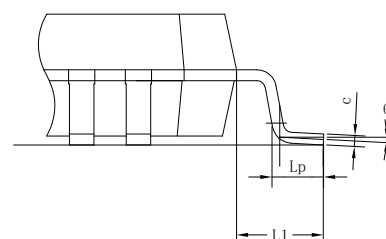
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	—	1.4	—
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

3.5 64-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP64-12x12-0.65	PLQP0064JB-A	0.50



detail of lead end



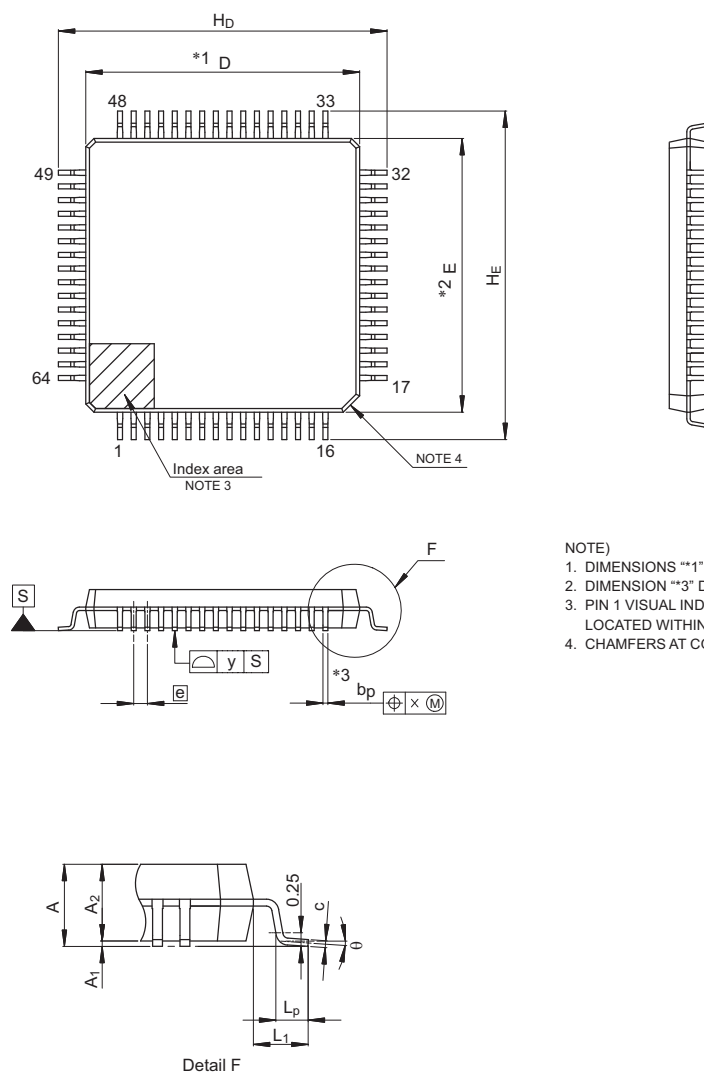
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	11.90	12.00	12.10
D	11.90	12.00	12.10
A ₂	—	1.40	—
H _D	13.80	14.00	14.20
H _E	13.80	14.00	14.20
A	—	—	1.70
A ₁	0.05	—	0.15
L _p	0.45	0.60	0.75
L ₁	—	1.00	—
b _p	0.27	0.32	0.37
c	0.09	—	0.20
e	—	0.65	—
θ	0.00	3.50	8.00
x	—	—	0.08
y	—	—	0.08

NOTE

- 1.DIMENSIONS "*1" AND "*2"DO NOT INCLUDE MOLD FLASH.
- 2.DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



NOTE)

1. DIMENSIONS "**1" AND "**2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "**3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A ₂	—	1.4	—
H _D	11.8	12.0	12.2
H _E	11.8	12.0	12.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

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Revision History	RL78/G21 Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	May 20, 2026	—	First edition issued

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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