

RL78/I1C (512 KB)

R01DS0382EJ0112

RENESAS MCU

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Ultra-low-power platform with 1.6-V to 5.5-V operation, featuring a 24-bit $\Delta\Sigma$ A/D converter, an RTC with independent power supply, a hardware AES, a 32-bit multiply-accumulator, and 512 Kbytes of code flash memory (256 Kbytes x 2 banks) for use in electric-power, gas, and water meter applications

1. OUTLINE

1.1 Features

Target applications

- Power, gas, and water meters

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μ s: @ 32 MHz selection with high-speed on-chip oscillator) to ultra-low speed (66.6 μ s: @ 15 kHz operation with low-speed on-chip oscillator)
- 16-bit multiplication, 16-bit multiply-accumulation, and 32-bit division are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register x 8) x 4 banks
- On-chip RAM: 32 KB

Code flash memory

- Code flash memory: 512 KB (256 KB x 2 banks)
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with flash shield window function)
- Bank programming function: Enables updating of the user program while it is running.

Data flash memory

- Data flash memory: 2 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

PLL clock

- 32 MHz is selectable ($\Delta\Sigma$ A/D converter is operable even when the PLL clock is selected as a CPU clock.)

High-speed on-chip oscillator

- Select from 1 to 32 MHz (TYP.). However when it is used as a clock for the $\Delta\Sigma$ A/D converter, select from 24 MHz (TYP.), 12 MHz (TYP.), 6 MHz (TYP.), or 3 MHz (TYP.).
- High accuracy: $\pm 1.0\%$ (V_{DD} = 1.8 to 5.5 V, T_A = -20 to $+85^\circ\text{C}$)
- On-chip high-speed on-chip oscillator clock frequency correction function

Middle-speed on-chip oscillator

- Select from 4 MHz/2 MHz/1 MHz (However $\Delta\Sigma$ A/D converter is disabled.)

Operating ambient temperature

- T_A = -40 to $+85^\circ\text{C}$

Power management and reset function

- On-chip power-on-reset (POR) circuit for Internal V_{DD} power supply
- On-chip RTC power-on-reset (RTCPOR) circuit for VRTC power supply
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

Voltage detective circuit

- Detective voltage for V_{DD} pin (Select interrupt from 6 levels)
- Detective voltage for LVDVBAT pin (Select interrupt from 7 levels)
- Detective voltage for VRTC pin (Select interrupt from 4 levels)
- Detective voltage for EXLVD pin (Select interrupt from 1 level)

Data transfer controller (DTC)

- Transfer mode: Normal mode, repeat mode, block mode
- Activation source: Start by interrupt sources
- Chain transfer function

Event link controller (ELC)

- Event signals of 30 types can be linked to the specified peripheral function.

On-chip 32-bit multiplier and multiply-accumulator

- 32 bits × 32 bits = 64 bits (Unsigned or signed)
- 32 bits × 32 bits + 64 bits = 64 bits (Unsigned or signed)
- The results of multiply-and-accumulate operations (cumulative values) can be retained in any of 24 selectable buffer channels.

Serial interface

- Simplified SPI (CSI): 2 to 3 channels
- UART/UART (LIN-bus supported): 2 or 4 channels
- UART/IrDA: 1 channel
- Simplified I²C communication: 2 to 3 channels
- I²C communication: 1 channel
- Serial interface UARTMG (9600 bps @ 38.4 kHz): 2 channels

Timer

- 16-bit timer: 10 channels (timer array unit (TAU): 8 channels, timer RJ: 2 channels)
- 12-bit interval timer: 1 channel
- 8-bit interval timer: 8 channels
- Independent power supply RTC: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel
- Sampling output timer detector (SMOTD): 2 units (6 channels for input, 6 channels for output)
- Oscillation stop detection circuit: 1 channel

LCD controller/driver

- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable
- Segment signal output: 34 (30)^{Note} to 42 (38)^{Note}
- Common signal output: 4 (8)^{Note}

A/D converter

- 24-Bit $\Delta\Sigma$ A/D converter: 3 or 4 channels
- 12-bit resolution A/D converter ($AV_{DD} = 1.8$ to 5.5 V): 4 or 6 channels
Simultaneous sample-and-hold function: Three sample-and-hold circuits are installed.
- Internal reference voltage (1.45 V) and temperature sensor
- The voltage reference output voltage can be used as the reference voltage for the 12-bit A/D converter.
- The voltage reference output voltage can be selected from among 1.5 V (typ.), 2.0 V (typ.), and 2.5 V (typ.).

I/O port

- I/O port: 60 or 76 (N-ch open drain I/O [6 V tolerance]: 6, N-ch open drain I/O [E_{VDD} tolerance]: 13 or 18)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip clock output/buzzer output controller
- On-chip key interrupt function

AES circuit

- Cipher modes of operation: GCM/ECB/CBC
- Encryption key length: 128/192/256 bits

Others

- On-chip BCD (binary-coded decimal) correction circuit

Note The values in parentheses are the number of signal outputs when 8 com is used.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

O ROM, RAM capacities

Code Flash	Data Flash	RAM	AES Function	RL78/I1C (512 KB)	
				80 pins	100 pins
512 KB	2 KB	32 KB ^{Note}	Mounted	R5F10NML	R5F10NPL

Note This is about 31 KB when the self-programming function is used. (For details, refer to **CHAPTER 3** in the RL78/I1C (512 KB) User's Manual.)

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/I1C (512 KB)

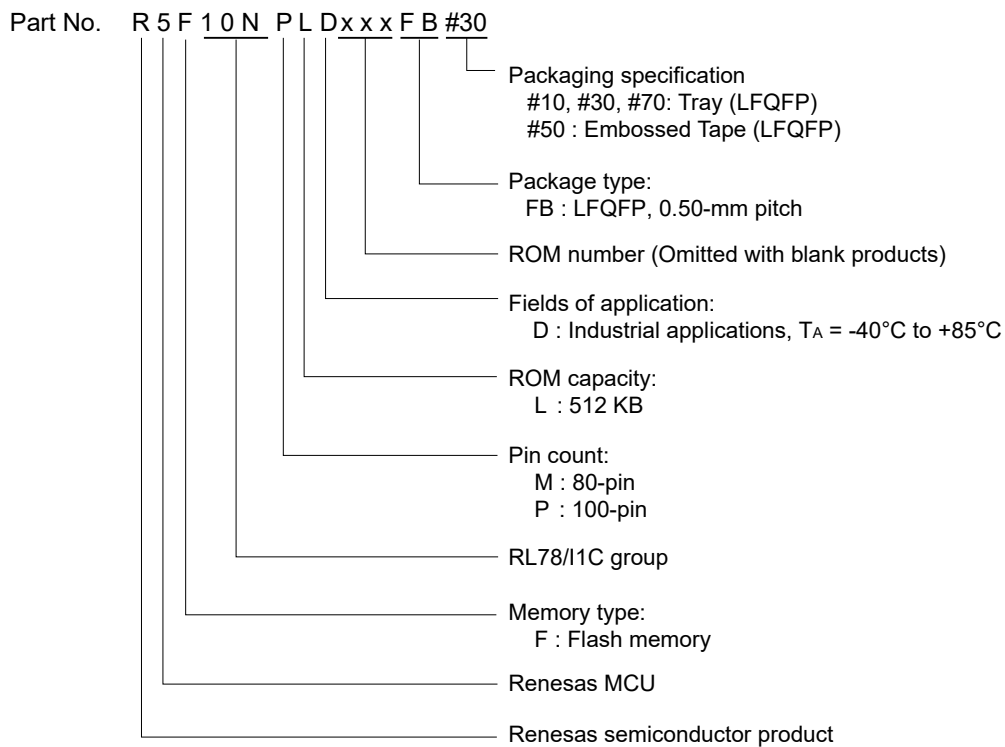


Table 1-1. List of Ordering Part Numbers

Pin Count	Package	Data Flash	AES Function	Fields of Application ^{Note}	Ordering Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5-mm pitch)	Mounted	Mounted	D	R5F10NMLDFB#10, R5F10NMLDFB#30, R5F10NMLDFB#50, R5F10NMLDFB#70
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch)	Mounted	Mounted	D	R5F10NPLDFB#10, R5F10NPLDFB#30, R5F10NPLDFB#50, R5F10NPLDFB#70

Note For the fields of application, see **Figure 1-1 Part Number, Memory Size, and Package of RL78/I1C (512 KB)**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 80-pin product

- 80-pin plastic LFQFP (12 × 12 mm, 0.5-mm pitch)

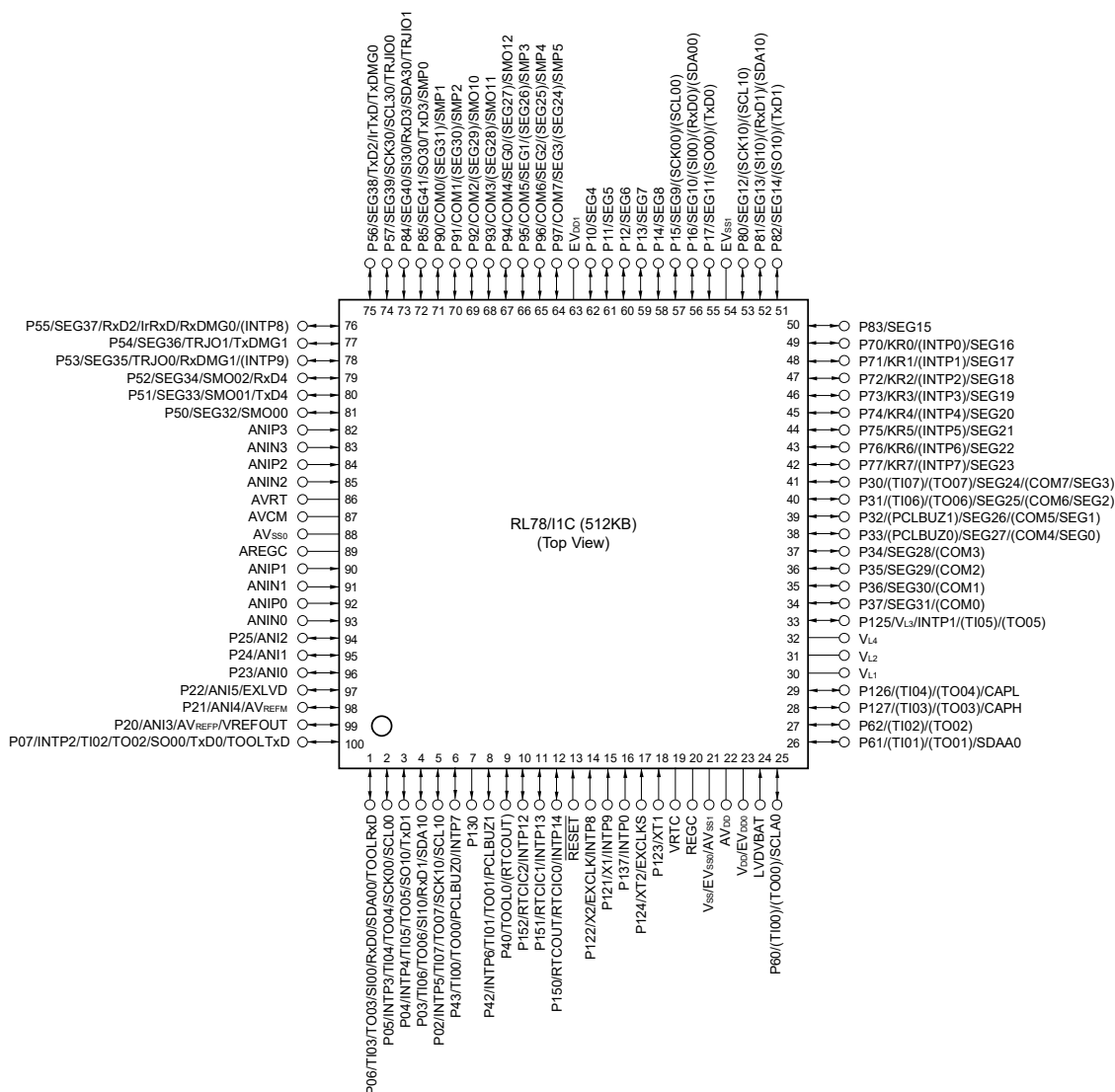


- Caution**
1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).
 2. Make the voltage on the AV_{DD} pin the same as that on the V_{DD} and EV_{DD0} pins.
 3. When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or V_{RTC}, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6 V.

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See Figure 4-7 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C (512 KB) User's Manual.

1.3.2 100-pin product

- 100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch)



- Cautions**
1. Make the voltage on the EV_{SS1} pin the same as that on the V_{SS}, EV_{SS0}, and AV_{SS1} pins.
 2. Make the voltage on the EV_{DD1} pin the same as that on the V_{DD} and EV_{DD0} pins.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).
 4. Make the voltage on the AV_{DD} pin the same as that on the V_{DD} and EV_{DD0} pins.
 5. When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or V_{RTC}, whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6 V.

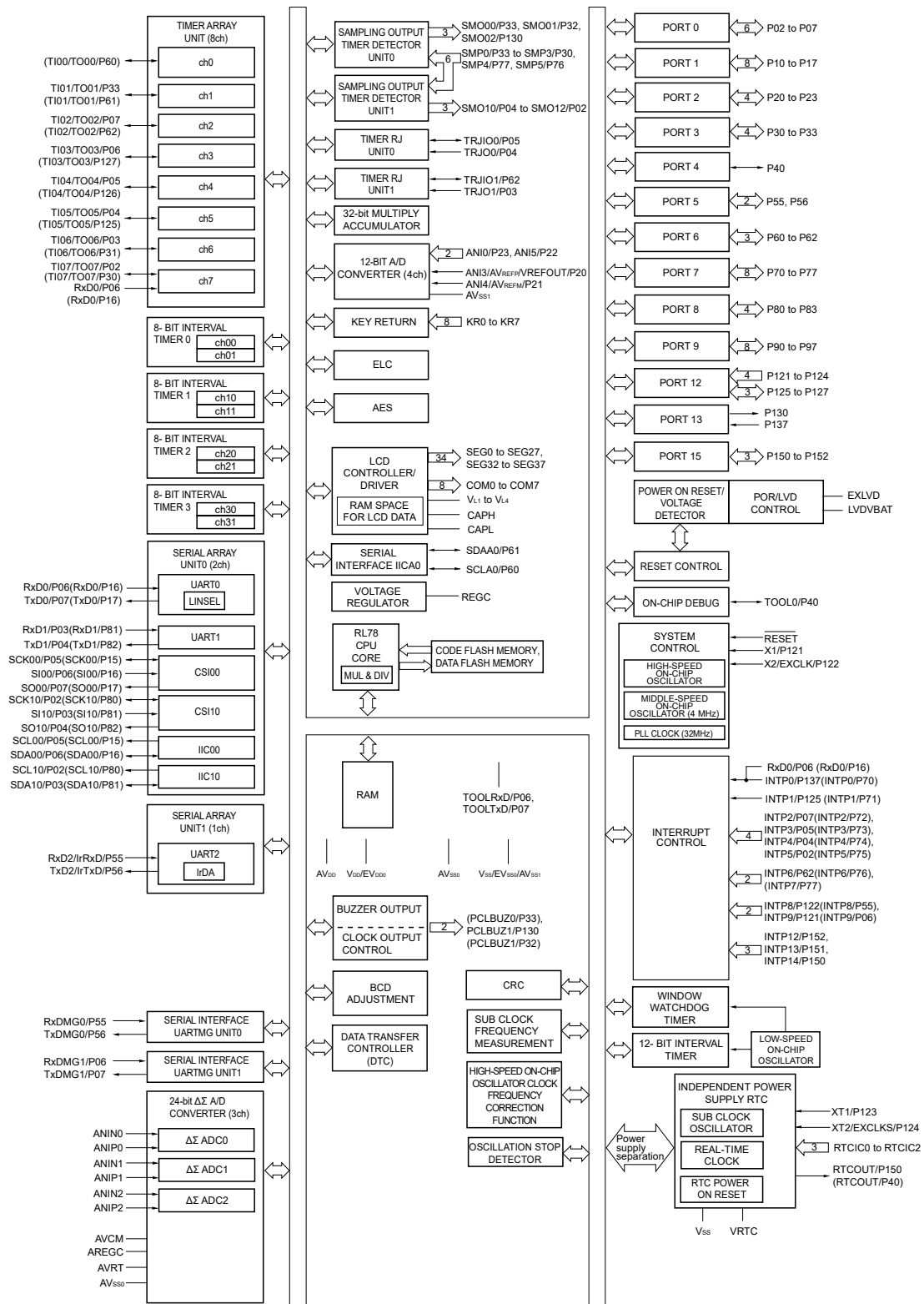
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD1} pins and connect the V_{SS} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See Figure 4-7 Format of Peripheral I/O Redirection Register (PIOR0) in the RL78/I1C (512 KB) User's Manual.

1.4 Pin Identification

ANI0 to ANI5:	Analog Input	P130, P137:	Port 13
ANIN0 to ANIN3, ANIP0 to ANIP3:	Analog Input for $\Delta\Sigma$ ADC	P150 to P152:	Port 15
AREGC:	Regulator Capacitance for $\Delta\Sigma$ ADC	PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
AVCM:	Control for $\Delta\Sigma$ ADC	REGC:	Regulator Capacitance
AV _{DD} :	Analog Power Supply	RESET:	Reset
AV _{REFM} :	12-bit A/D Converter Reference Potential (– side) Input	RTCOUT:	Real-time Clock Correction Clock (1 Hz/64 Hz) Output
AV _{REFP} :	12-bit A/D Converter Reference Potential (+ side) Input	RTCIC0 to RTCIC2:	RTC Time Capture Event Input
AVRT:	Reference Potential for $\Delta\Sigma$ ADC	RxD0 to RxD4:	Receive Data for UART
AV _{SS0} :	Ground for $\Delta\Sigma$ ADC	RxDMG0, RxDMG1:	Receive Data for UARTMG
AV _{SS1} :	Ground for 12-bit A/D Converter	SCL00, SCL10, SCL30:	Serial Clock Output for Simplified IIC
CAPH, CAPL:	Capacitor Connection for LCD Controller/Driver	SDA00, SDA10, SDA30:	Serial Data Input/Output for Simplified IIC
COM0 to COM7:	Common Signal Output for LCD Controller/Driver	SCLA0 :	Serial Clock Input/Output for IICA0
EV _{DD0} , EV _{DD1} :	Power Supply for Port	SDAA0:	Serial Data Input/Output for IICA0
EV _{SS0} , EV _{SS1} :	Ground for Port	SCK00, SCK10, SCK30:	Serial Clock Input/Output for CSI
EXCLK:	External Clock Input (Main System Clock)	SEG0 to SEG41:	Segment Signal Output for LCD Controller/Driver
EXCLKS:	External Clock Input (Subsystem clock)	SI00, SI10, SI30:	Serial Data Input for CSI
EXLVD:	External Input for Low Voltage Detector	SMP0 to SMP5:	Sampling Input
INTP0 to INTP9, INTP12 to INTP14:	Interrupt Request From Peripheral	SMO00 to SMO02, SMO10 to SMO12:	Sampling Clock Output
IrRxD:	Receive Data for IrDA	SO00, SO10, SO30:	Serial Data Output for CSI
IrTxD:	Transmit Data for IrDA	TI00 to TI07:	Timer Input
KR0 to KR7:	Key Return	TO00 to TO07, TRJ00, TRJ01:	Timer Output
LVDVBAT:	Battery Backup Power Supply for Voltage Detector	TOOL0:	Data Input/Output for Tool
P02 to P07:	Port 0	TOOLRxD, TOOLTxD:	Data Input/Output for External Device
P10 to P17:	Port 1	TRJIO0, TRJIO1:	Timer Input/Output
P20 to P25:	Port 2	TxD0 to TxD4:	Transmit Data for UART
P30 to P37:	Port 3	TxDMG0, TxDMG1:	Transmit Data for UARTMG
P40, P42, P43:	Port 4	V _{DD} :	Power Supply
P50 to P57:	Port 5	V _{L1} to V _{L4} :	Voltage for Driving LCD
P60 to P62:	Port 6	VREFOUT:	Analog Reference Voltage Output
P70 to P77:	Port 7	VRTC:	RTC Power Supply
P80 to P85:	Port 8	V _{SS} :	Ground
P90 to P97:	Port 9	X1, X2:	Crystal Oscillator (Main System Clock)
P121 to P127:	Port 12	XT1, XT2:	Crystal Oscillator (Subsystem Clock)

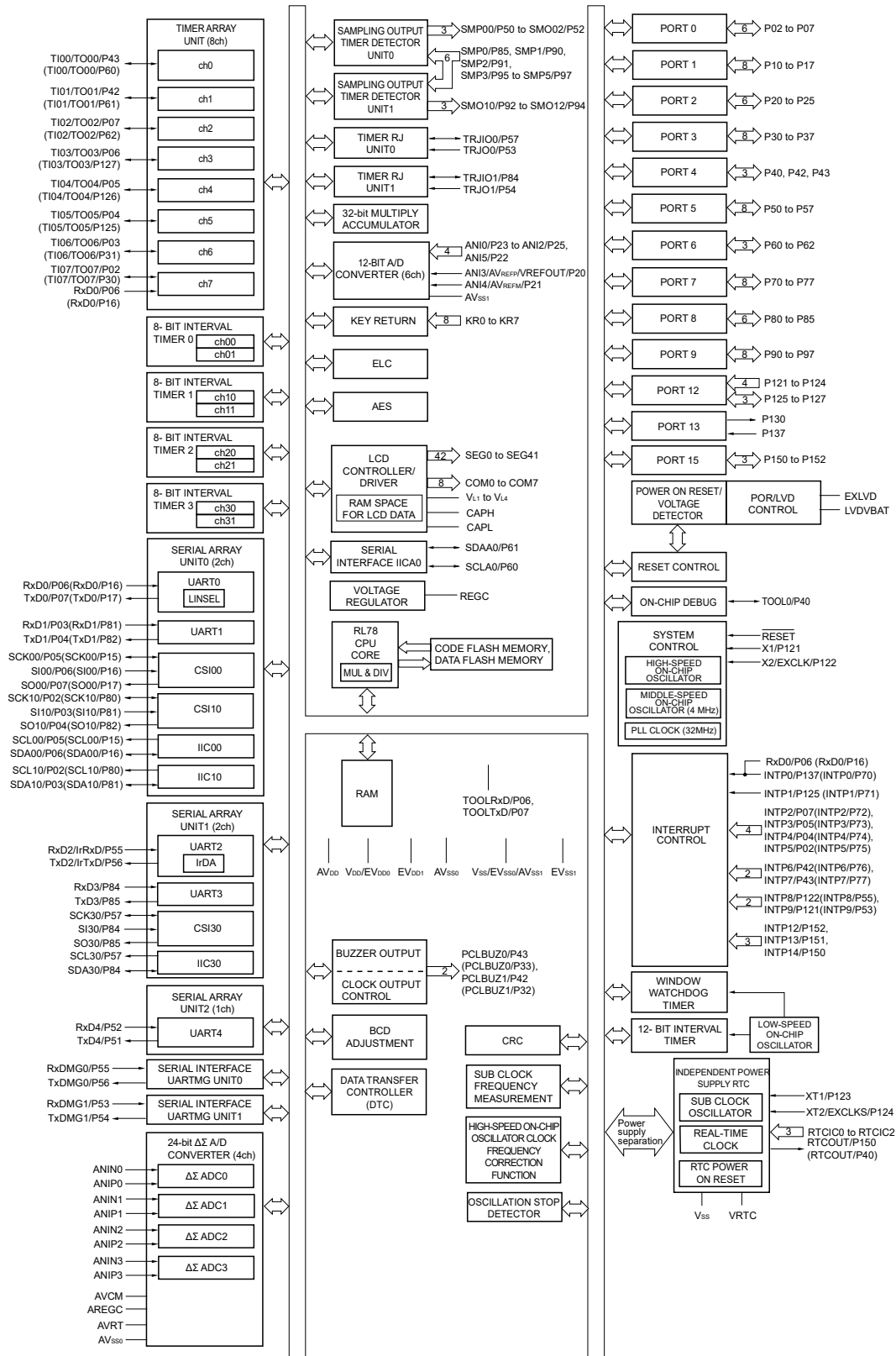
1.5 Block Diagram

1.5.1 80-pin product



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-7 Format of Peripheral I/O Redirection Register (PIOR0)** in the RL78/I1C (512 KB) User's Manual.

1.5.2 100-pin product



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-7 Format of Peripheral I/O Redirection Register (PIOR0)** in the RL78/I1C (512 KB) User's Manual.

1.6 Outline of Functions

(1/3)

Item		80-pin	100-pin
		R5F10NMLDFB	R5F10NPLDFB
Code flash memory		512 KB (256 KB × 2 banks)	
Data flash memory		2 KB	
RAM		32 KB ^{Note}	
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), HS (high-speed main) mode: 1 to 6 MHz ($V_{DD} = 2.1$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V), LP (low-power main) mode: 1 MHz ($V_{DD} = 1.8$ to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH}) Max.: 32 MHz	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), HS (high-speed main) mode: 1 to 6 MHz ($V_{DD} = 2.1$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V), LP (low-power main) mode: 1 MHz ($V_{DD} = 1.8$ to 5.5 V)	
	Middle-speed on-chip oscillator clock (f_{IM}) Max.: 4 MHz	LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V), LP (low-power main) mode: 1 MHz ($V_{DD} = 1.8$ to 5.5 V)	
	PLL clock (f_{PLL})	HS (high-speed main) mode: 32 MHz ($V_{DD} = 2.7$ to 5.5 V)	
Subsystem clock	Subsystem clock oscillator clock (f_{SX})	XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (typ.): $V_{DD} = 1.6$ to 5.5 V 38.4 kHz (typ.): $V_{DD} = 1.6$ to 5.5 V	
	Low-speed on-chip oscillator clock (f_{IL})	15 kHz (typ.): $V_{DD} = 1.6$ to 5.5 V	
High-speed on-chip oscillator clock frequency correction function		Correct the frequency of the high-speed on-chip oscillator clock by the subsystem clock.	
General-purpose register		8 bits × 8 registers × 4 banks	
Minimum instruction execution time		0.03125 μ s (PLL clock: $f_{PLL} = 32$ MHz selection)	
		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)	
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
		66.6 μ s (Low-speed on-chip oscillator: $f_{IL} = 15$ kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (16 bits × 16 bits), division (32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and boolean operation), etc. 	
I/O port	Total	60	76
	CMOS I/O	48	64
	CMOS input	5	5
	CMOS output	1	1
	N-ch O.D I/O (6 V tolerance)	6	6

Note This is about 31 KB when the self-programming function is used.

(2/3)

Item		80-pin	100-pin
		R5F10NMLDFB	R5F10NPLDFB
Timer	16-bit timer TAU	8 channels	
	Watchdog timer	1 channel	
	12-bit interval timer	1 channel	
	8/16-bit interval timer	8 channels (8-bit)/4 channels (16-bit)	
	Independent power supply realtime clock (RTC)	1 channel	
	16-bit timer RJ	2 channels	
	Sampling output timer detector (SMOTD)	6 channels for input, 6 channels for output	
	Oscillation stop detection circuit	1 channel	
	Timer output	Timer outputs: 8 channels, PWM outputs: 7 ^{Note}	
	RTC output	1 channel • 1 Hz/64 Hz (sub clock: $f_{sx} = 32.768$ kHz)	
	RTC time capture input	3 channels	
Clock output/buzzer output		2 • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Sub clock: $f_{sx} = 32.768$ kHz operation)	
12-bit resolution A/D converter		4 channels	6 channels
	Simultaneous sampling for 3 channels	—	3 channels
	Voltage reference voltage output	1.5 V/2.0 V/2.5 V	
24-bit $\Delta\Sigma$ A/D converter		3 channels	4 channels
	SNDR	Typ. 80 dB (gain $\times 1$) Min. 69 dB (gain $\times 16$) Min. 65 dB (gain $\times 32$)	
	Sampling frequency	3.906 kHz/1.953 kHz	
	PGA	$\times 1, \times 2, \times 4, \times 8, \times 16, \times 32$	
Serial interface	Simplified SPI (CSI)/UART/simplified I ² C	2 channels	3 channels
	UART/IrDA	1 channel	
	UART	—	1 channel
	I ² C bus	1 channel	
	UARTMG	2 channels	
32-bit multiplier and multiply-accumulator		32 bits \times 32 bits = 64 bits (Unsigned or signed) (5 clock) 32 bits \times 32 bits + 64 bits = 64 bits (Unsigned or signed) (5 clock) 24 cumulative buffer channels	
Data transfer controller (DTC)		46 sources	50 sources

Note The number of outputs varies, depending on the setting of channels in use and the number of the master (see **8.9.3 Operation as multiple PWM output function** in the RL78/I1C (512 KB) User's Manual).

(3/3)

Item		80-pin	100-pin
		R5F10NMLDFB	R5F10NPLDFB
Event link controller (ELC)	Event input	7	
	Event trigger input	30	
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.	
	Segment signal output	34 (30) ^{Note 1}	42 (38) ^{Note 1}
	Common signal output	4 (8) ^{Note 1}	
Vectored interrupt sources	Internal	41	47
	External	14	14
Key interrupt input		8	
AES circuit		Cipher modes of operation: GCM/ECB/CBC Encryption key length: 128/192/256-bit	
Reset	MCU	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset of V_{DD} power supply • Internal reset by voltage detector of V_{DD} power supply • Internal reset by illegal instruction execution^{Note 2} • Internal reset by RAM parity error • Internal reset by illegal-memory access 	
	RTC	<ul style="list-style-type: none"> • RTC circuit reset by RTC Power-on-reset 	
Power-on-reset circuit	V _{DD}	<ul style="list-style-type: none"> • Power-on-reset: 1.51 V (typ.) • Power-down-reset: 1.50 V (typ.) 	
	V _{RTC}	<ul style="list-style-type: none"> • RTC Power-on-reset: 1.52 V (typ.) • RTC Power-down-reset: 1.50 V (typ.) 	
Voltage detector	V _{DD}	<ul style="list-style-type: none"> • Rising edge: 1.67 V to 4.06 V (14 stages) • Falling edge: 1.63 V to 3.98 V (14 stages) 	
	V _{DD}	<ul style="list-style-type: none"> • Rising edge: 2.53 V to 3.77 V (6 stages) • Falling edge: 2.46 V to 3.70 V (6 stages) 	
	LVDVBAT	<ul style="list-style-type: none"> • Rising edge: 2.23 V to 3.13 V (7 stages) • Falling edge: 2.17 V to 3.07 V (7 stages) 	
	V _{RTC}	<ul style="list-style-type: none"> • Rising edge: 2.22 V to 2.84 V (4 stages) • Falling edge: 2.16 V to 2.78 V (4 stages) 	
	EXLVD	<ul style="list-style-type: none"> • Rising edge: 1.33 V • Falling edge: 1.28 V 	
On-chip debug function		Provided	
Bank programming function		Provided	
Power supply voltage		V _{DD} = 1.6 to 5.5 V	
Operating ambient temperature		T _A = -40 to +85°C	

Notes 1. The values in parentheses are the number of signal outputs when 8 com is used.

2. This reset occurs when instruction code FFH is executed.

This reset does not occur during emulation using an in-circuit emulator or an on-chip debugging emulator.

2. ELECTRICAL SPECIFICATIONS

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. The pins mounted depend on the product. See 2.1 Port Function to 2.2.1 Functions mounted on the products with different numbers of pins in the RL78/I1C (512 KB) User's Manual.

Remark In the descriptions in this chapter, read EV_{DD} as EV_{DD0} and EV_{DD1} , and EV_{SS} as EV_{SS0} and EV_{SS1} .

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD}		-0.5 to +6.5	V
	V _{RTC}		-0.5 to +6.5	V
	AV _{DD}	AV _{DD} = V _{DD}	-0.5 to +6.5	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 ^{Note 1}	V
Input voltage	V _{I1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	-0.3 to EV _{DD} +0.3 and -0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{I2}	P60 to P62, P150 to P152 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P121, P122, P137, EXCLK	-0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{I4}	RESET	-0.3 to +6.5	V
	V _{I5}	P123, P124, EXCLKS	-0.3 to V _{RTC} +0.3 ^{Note 2}	V
	V _{I6}	P20 to P25	-0.3 to AV _{DD} +0.3 ^{Note 2}	V
Output voltage	V _{O1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130, P150 to P152	-0.3 to EV _{DD} +0.3 and -0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{O2}	P20 to P25	-0.3 to AV _{DD} +0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI0 to ANI5	-0.3 to AV _{DD} +0.3 and -0.3 to AV _{REF(+)} +0.3 ^{Notes 2, 3}	V
	V _{AI2}	ANIP0 to ANIP3, ANIN0 to ANIN3	-0.6 to +2.8 and -0.6 to AREGC +0.3 ^{Note 4}	V
Reference supply voltage	V _{IDSAD}	AREGC, AVCM, AVRT	-0.3 to +2.8 and -0.3 to AV _{DD} +0.3 ^{Note 5}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF(+)} + 0.3 V in case of A/D conversion target pin.

4. The ΔΣ A/D conversion target pin must not exceed AREGC +0.3 V.

5. Connect AREGC, AVCM, and AVRT terminals to V_{SS} via capacitor (0.47 μF).

This value defines the absolute maximum rating of AREGC, AVCM, and AVRT terminal. Do not use with voltage applied.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF(+)}: Positive reference voltage of the 12-bit A/D converter

3. V_{SS}: Reference voltage

Absolute Maximum Ratings (2/3)

Parameter	Symbols	Conditions	Ratings	Unit
LCD voltage	V _{LI1}	V _{L1} voltage ^{Note 1}	-0.3 to 2.8 and -0.3 to V _{L4} +0.3	V
	V _{LI2}	V _{L2} voltage ^{Note 1}	-0.3 to V _{L4} +0.3 ^{Note 2}	V
	V _{LI3}	V _{L3} voltage ^{Note 1}	-0.3 to V _{L4} +0.3 ^{Note 2}	V
	V _{LI4}	V _{L4} voltage ^{Note 1}	-0.3 to +6.5	V
	V _{LCAP}	CAPL, CAPH voltage ^{Note 1}	-0.3 to V _{L4} +0.3 ^{Note 2}	V
	V _{OUT}	COM0 to COM7, SEG0 to SEG41, output voltage	External resistance division method Capacitor split method Internal voltage boosting method	-0.3 to V _{DD} +0.3 ^{Note 2} -0.3 to V _{DD} +0.3 ^{Note 2} -0.3 to V _{L4} +0.3 ^{Note 2}

Notes 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark V_{SS}: Reference voltage

Absolute Maximum Ratings (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130	-40	mA
		Total of all pins -170 mA	P02 to P07, P40, P42, P43, P130	-70	mA
			P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	-100	mA
	I_{OH2}	Per pin	P20 to P25	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	I_{OL1}	Per pin	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130	40
Total of all pins 170 mA			P02 to P07, P40, P42, P43, P130	70	mA
			P10 to P17, P30 to P37, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P90 to P97, P125 to P127	100	mA
I_{OL2}		Per pin	P20 to P25	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T_A	In normal operation mode		-40 to +85
	In flash memory programming mode				
Storage temperature	T_{stg}			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
		$1.8\text{ V} \leq V_{DD} < 2.4\text{ V}$	1.0		8.0	MHz
		$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	1.0		4.0	MHz

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{RTC} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
XT1 clock oscillation frequency (f_{XT}) ^{Note}	Crystal resonator	$1.6\text{ V} \leq V_{RTC} \leq 5.5\text{ V}$	32	32.768	35	kHz
			31	38.4	39	kHz

Note Indicates only permissible oscillator frequency ranges. See **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, see **6.4 System Clock Oscillator** in the RL78/I1C (512 KB) User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _H			1.0		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.0		+1.0	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.0		+5.0	%
		-40 to -20°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.5		+5.5	%
Middle-speed on-chip oscillator clock frequency ^{Note 2}	f _M			1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy		1.8 V ≤ V _{DD} ≤ 5.5 V		-12		+12	%
Low-speed on-chip oscillator clock frequency	f _L				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by using bits 0 to 3 of option byte (000C2H/400C2H) and bits 0 to 2 of the HOCODIV register.

2. This indicates the oscillator characteristics only. See **2.4 AC Characteristics** for the instruction execution time.

2.2.3 PLL oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency ^{Note}	f_{PLLIN}	f_{IH}		4		MHz
PLL output frequency ^{Note}	f_{PLL}			32		MHz
Lockup wait time		Wait time from PLL output enable to frequency stabilization	40			μs
Interval wait time		Wait time from PLL stop to PLL restart setting	4			μs
Setting wait time		Wait time from PLL input clock stabilization and PLL setting fixedness to start-up setting	1			μs

Note Indicates only permissible oscillator frequency ranges.

2.3 DC Characteristics

2.3.1 Pin characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Output current, high ^{Note 1}	I _{OH1}	Per pin for P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130	1.6 V ≤ EV _{DD} ≤ 5.5 V			-10.0 ^{Note 2}	mA	
		Total of P02 to P07, P40, P42, P43, P130 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-55.0	mA	
			2.7 V ≤ EV _{DD} < 4.0 V			-10.0	mA	
			1.8 V ≤ EV _{DD} < 2.7 V			-5.0	mA	
			1.6 V ≤ EV _{DD} < 1.8 V			-2.5	mA	
		Total of P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD} ≤ 5.5 V			-80.0	mA	
			2.7 V ≤ EV _{DD} < 4.0 V			-19.0	mA	
			1.8 V ≤ EV _{DD} < 2.7 V			-10.0	mA	
			1.6 V ≤ EV _{DD} < 1.8 V			-5.0	mA	
		Total of all pins (When duty ≤ 70% ^{Note 3})				-100.0	mA	
		I _{OH2}	Per pin for P20 to P25	1.6 V ≤ AV _{DD} ≤ 5.5 V			-0.1 ^{Note 2}	mA
			Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ AV _{DD} ≤ 5.5 V			-0.6	mA

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD}, V_{DD}, and AV_{DD} pins to an output pin.
 - Do not exceed the total current value.
 - Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P02 to P07, P15 to P17, P51, P54, P56, P57, P80 to P82, P84, and P85 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, I_{OL} ^{Note 1}	I_{OL1}	Per pin for P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130			20.0 ^{Note 2}	mA	
		Per pin for P60 to P62, P150 to P152			15.0 ^{Note 2}	mA	
		Total of P02 to P07, P40, P42, P43, P130 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$			70.0	mA
			$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$			15.0	mA
			$1.8\text{ V} \leq EV_{DD} < 2.7\text{ V}$			9.0	mA
			$1.6\text{ V} \leq EV_{DD} < 1.8\text{ V}$			4.5	mA
		Total of P10 to P17, P30 to P37, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P90 to P97, P125 to P127 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$			80.0	mA
			$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$			35.0	mA
			$1.8\text{ V} \leq EV_{DD} < 2.7\text{ V}$			20.0	mA
			$1.6\text{ V} \leq EV_{DD} < 1.8\text{ V}$			10.0	mA
	Total of all pins (When duty $\leq 70\%$ ^{Note 3})				150.0	mA	
	I_{OL2}	Per pin for P20 to P25	$1.6\text{ V} \leq AV_{DD} \leq 5.5\text{ V}$			0.4 ^{Note 2}	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$1.6\text{ V} \leq AV_{DD} \leq 5.5\text{ V}$			2.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} , V_{SS} , and AV_{SS} pins.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to $n\%$).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V_{IH1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	Normal input buffer	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH2}	P02, P03, P05, P06, P15, P16, P42, P43, P52, P53, P55, P57, P80, P81, P84	TTL input buffer $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$	2.2		EV_{DD}	V
			TTL input buffer $3.3\text{ V} \leq EV_{DD} < 4.0\text{ V}$	2.0		EV_{DD}	V
			TTL input buffer $1.6\text{ V} \leq EV_{DD} < 3.3\text{ V}$	1.5		EV_{DD}	V
	V_{IH3}	P20 to P25		$0.7AV_{DD}$		AV_{DD}	V
	V_{IH4}	P60 to P62		$0.7EV_{DD}$		6.0	V
	V_{IH5}	P121, P122, P137, P150 to P152, EXCLK		$0.8V_{DD}$		V_{DD}	V
	V_{IH6}	$\overline{\text{RESET}}$		$0.8V_{DD}$		6.0	V
	V_{IH7}	P123, P124, EXCLKS		$0.8V_{RTC}$		V_{RTC}	V
V_{IH8}	P150 to P152 ^{Note}		$0.8V_{DD}$		6.0	V	
V_{IH9}	RTCIC0 to RTCIC2 ^{Note}		$0.8V_{RTC}$		6.0	V	
Input voltage, low	V_{IL1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	Normal input buffer	0		$0.2EV_{DD}$	V
	V_{IL2}	P02, P03, P05, P06, P15, P16, P42, P43, P52, P53, P55, P57, P80, P81, P84	TTL input buffer $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$	0		0.8	V
			TTL input buffer $3.3\text{ V} \leq EV_{DD} < 4.0\text{ V}$	0		0.5	V
			TTL input buffer $1.6\text{ V} \leq EV_{DD} < 3.3\text{ V}$	0		0.32	V
	V_{IL3}	P20 to P25		0		$0.3AV_{DD}$	V
	V_{IL4}	P60 to P62		0		$0.3EV_{DD}$	V
	V_{IL5}	P121, P122, P137, P150 to P152, EXCLK, $\overline{\text{RESET}}$		0		$0.2V_{DD}$	V
	V_{IL6}	P123, P124, EXCLKS		0		$0.2V_{RTC}$	V
	V_{IL7}	P150 to P152 ^{Note}		0		$0.2V_{DD}$	V
V_{IL8}	RTCIC0 to RTCIC2 ^{Note}		0		$0.2V_{RTC}$	V	

Caution The maximum value of V_{IH} of pins P02 to P07, P15 to P17, P51, P54, P56, P57, P80 to P82, P84, and P85 is EV_{DD} , even in the N-ch open-drain mode.

Note When a high-level signal is to be input to any pin among pins P150 to P152 (including if the pin is in use for a multiplexed pin function rather than for GPIO), the pin should always be individually connected via a resistor to V_{DD} or V_{RTC} , whichever of the voltages is higher at the time, or to a voltage higher than both but no higher than 6 V.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130	4.0 V ≤ EVDD ≤ 5.5 V, IOH1 = -10.0 mA	EVDD - 1.5		V
			4.0 V ≤ EVDD ≤ 5.5 V, IOH1 = -3.0 mA	EVDD - 0.7		V
			2.7 V ≤ EVDD ≤ 5.5 V, IOH1 = -2.0 mA	EVDD - 0.6		V
			1.8 V ≤ EVDD ≤ 5.5 V, IOH1 = -1.5 mA	EVDD - 0.5		V
			1.6 V ≤ EVDD ≤ 5.5 V, IOH1 = -1.0 mA	EVDD - 0.5		V
	VOH2	P20 to P25	1.6 V ≤ AVDD ≤ 5.5 V, IOH2 = -100 μA	AVDD - 0.5		V
Output voltage, low	VOL1	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127, P130	4.0 V ≤ EVDD ≤ 5.5 V, IOL1 = 20 mA		1.3	V
			4.0 V ≤ EVDD ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ EVDD ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			1.8 V ≤ EVDD ≤ 5.5 V, IOL1 = 0.6 mA		0.4	V
			1.6 V ≤ EVDD ≤ 5.5 V, IOL1 = 0.3 mA		0.4	V
	VOL2	P150 to P152	4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 15.0 mA		2.0	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 5.0 mA		0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL2 = 3.0 mA		0.4	V
			1.8 V ≤ VDD ≤ 5.5 V, IOL2 = 2.0 mA		0.4	V
			1.6 V ≤ VDD ≤ 5.5 V, IOL2 = 1.0 mA		0.4	V
	VOL3	P60 to P62	4.0 V ≤ EVDD ≤ 5.5 V, IOL3 = 15.0 mA		2.0	V
			4.0 V ≤ EVDD ≤ 5.5 V, IOL3 = 5.0 mA		0.4	V
			2.7 V ≤ EVDD ≤ 5.5 V, IOL3 = 3.0 mA		0.4	V
			1.8 V ≤ EVDD ≤ 5.5 V, IOL3 = 2.0 mA		0.4	V
			1.6 V ≤ EVDD ≤ 5.5 V, IOL3 = 1.0 mA		0.4	V
	VOL4	P20 to P25	1.6 V ≤ AVDD ≤ 5.5 V, IOL4 = -100 μA		0.4	V

(Caution and Remark are listed on the next page.)

Caution P02 to P07, P15 to P17, P51, P54, P56, P57, P80 to P82, P84, and P85 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LIH1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P60 to P62, P70 to P77, P80 to P85, P90 to P97, P125 to P127	V _I = EV _{DD}		1	μA		
	I _{LIH2}	P137, P150 to P152, RESET	V _I = V _{DD}		1	μA		
	I _{LIH3}	P121, P122 (X1, X2, EXCLK)	V _I = V _{DD}	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
	I _{LIH4}	P123, P124 (XT1, XT2, EXCLKS)	V _I = V _{RTC}	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
I _{LIH5}	P20 to P25	V _I = AV _{DD}		1	μA			
Input leakage current, low	I _{LIL1}	P02 to P07, P10 to P17, P30 to P37, P40, P42, P43, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	V _I = EV _{SS}		-1	μA		
	I _{LIL2}	P137, P150 to P152, RESET	V _I = V _{SS}		-1	μA		
	I _{LIL3}	P121, P122 (X1, X2, EXCLK)	V _I = V _{SS}	In input port or external clock input		-1	μA	
				In resonator connection		-10	μA	
	I _{LIL4}	P123, P124 (XT1, XT2, EXCLKS)	V _I = V _{SS}	In input port or external clock input		-1	μA	
				In resonator connection		-10	μA	
I _{LIL5}	P20 to P25	V _I = AV _{SS1}		-1	μA			
On-chip pull-up resistance	R _{U1}	P10 to P17, P30 to P37, P50 to P57, P70 to P77, P80 to P85, P90 to P97, P125 to P127	V _I = EV _{SS}	2.4 V ≤ EV _{DD} ≤ 5.5 V	10	20	100	kΩ
				1.6 V ≤ EV _{DD} < 2.4 V	10	30	100	kΩ
	R _{U2}	P02 to P07, P40, P42, P43	V _I = EV _{SS}		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(TA = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

(1/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 32 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V		2.5		mA
						V _{DD} = 3.0 V		2.5		mA
				Normal operation	V _{DD} = 5.0 V		5.6	9.1	mA	
					V _{DD} = 3.0 V		5.6	9.1	mA	
				f _{CLK} = 32 MHz ^{Note 3} PLL operation	Normal operation	V _{DD} = 5.0 V		5.8	9.0	mA
						V _{DD} = 3.0 V		5.8	9.0	mA
				f _{IH} = 24 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		4.5	7.3	mA
						V _{DD} = 3.0 V		4.5	7.3	mA
				f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		3.2	5.8	mA
						V _{DD} = 3.0 V		3.2	5.8	mA
				f _{IH} = 12 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		2.6	4.9	mA
						V _{DD} = 3.0 V		2.6	4.9	mA
			f _{IH} = 6 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		1.9	3.0	mA	
					V _{DD} = 3.0 V		1.9	3.0	mA	
			f _{IH} = 3 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		1.5	2.4	mA	
					V _{DD} = 3.0 V		1.5	2.4	mA	
			LS (low-speed main) mode ^{Note 5} (MCSEL = 0)	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.5	2.5	mA
						V _{DD} = 2.0 V		1.5	2.5	mA
				f _{IH} = 6 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.2	2.3	mA
						V _{DD} = 2.0 V		1.2	2.3	mA
				f _{IH} = 3 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		0.8	1.6	mA
						V _{DD} = 2.0 V		0.8	1.6	mA
			LS (low-speed main) mode ^{Note 5} (MCSEL = 1)	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.0	1.7	mA
						V _{DD} = 2.0 V		1.0	1.7	mA
f _{IM} = 4 MHz ^{Note 6}	Normal operation	V _{DD} = 3.0 V			0.8	1.5	mA			
		V _{DD} = 2.0 V			0.8	1.5	mA			
LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.7	2.8	mA			
			V _{DD} = 2.0 V		1.7	2.8	mA			
LP (low-power main) mode ^{Note 5} (MCSEL = 1)	f _{IH} = 1 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		330	550	μA			
			V _{DD} = 2.0 V		330	550	μA			
	f _{IM} = 1 MHz ^{Note 6}	Normal operation	V _{DD} = 3.0 V		170	360	μA			
			V _{DD} = 2.0 V		170	360	μA			

(Notes and Remarks are listed on the page after the next page.)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0 V)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	IDD1	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	6.4	mA
						Resonator connection		3.7	6.5	mA
				f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		3.4	6.4	mA
						Resonator connection		3.7	6.5	mA
				f _{MX} = 12 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		2.4	4.6	mA
						Resonator connection		2.6	4.7	mA
				f _{MX} = 12 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		2.4	4.6	mA
						Resonator connection		2.6	4.7	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	4.1	mA
						Resonator connection		2.4	4.1	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	4.1	mA
						Resonator connection		2.4	4.1	mA
			LS (low-speed main) mode ^{Note 5} (MCSEL = 0)	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.4	mA
						Resonator connection		1.3	2.4	mA
				f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.4	mA
						Resonator connection		1.3	2.4	mA
			LS (low-speed main) mode ^{Note 5} (MCSEL = 1)	f _{MX} = 4 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		0.8	1.6	mA
						Resonator connection		0.8	1.5	mA
				f _{MX} = 4 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		0.8	1.6	mA
						Resonator connection		0.8	1.5	mA
			LP (low-power main) mode ^{Note 5} (MCSEL = 1)	f _{IH} = 1 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		150	320	μA
						Resonator connection		190	360	μA
				f _{IH} = 1 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		150	320	μA
						Resonator connection		190	360	μA
			Sub clock operation	f _{SUB} = 32.768 kHz ^{Note 4} , T _A = -40°C	Normal operation	Square wave input		5.7	11.0	μA
						Resonator connection		5.9	11.1	μA
				f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +25°C	Normal operation	Square wave input		6.1	8.0	μA
						Resonator connection		6.4	8.1	μA
f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +50°C	Normal operation	Square wave input			6.3	9.3	μA			
		Resonator connection			6.6	9.4	μA			
f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +70°C	Normal operation	Square wave input			6.9	12.6	μA			
		Resonator connection			7.1	12.7	μA			
f _{SUB} = 32.768 kHz ^{Note 4} , T _A = +85°C	Normal operation	Square wave input			7.8	21.7	μA			
		Resonator connection			7.9	21.8	μA			
f _{IL} = 15 kHz, T _A = -40°C ^{Note 7}	Normal operation			2.8	9	μA				
f _{IL} = 15 kHz, T _A = +25°C ^{Note 7}	Normal operation			3.1	9	μA				
f _{IL} = 15 kHz, T _A = +85°C ^{Note 7}	Normal operation			5.0	13	μA				

(Notes and Remarks are listed on the next page.)

- Notes**
- Total current flowing into V_{DD} , EV_{DD} , and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD} , V_{RTC} or V_{SS} , EV_{SS} . The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.
 - The currents in the "TYP." column do not include the operating currents of the peripheral modules.
 - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, 12-bit A/D converter, $\Delta\Sigma$ A/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.
 - When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
 - When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
 - When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1).
 - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 $2.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }6\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LP (low-power main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
 - When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
 - When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

- Remarks**
- f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - f_{IH} : High-speed on-chip oscillator clock frequency
 - f_{IM} : Middle-speed on-chip oscillator clock frequency
 - f_{IL} : Low-speed on-chip oscillator clock frequency
 - f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 - Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(TA = -40 to +85°C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode ^{Note 7}	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V	0.69	1.9	mA
					V _{DD} = 3.0 V	0.68	1.9	mA
				f _{CLK} = 32 MHz ^{Note 4} , PLL operation	V _{DD} = 5.0 V	1.2	2.2	mA
					V _{DD} = 3.0 V	1.2	2.2	mA
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V	0.56	1.5	mA
					V _{DD} = 3.0 V	0.56	1.5	mA
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V	0.49	1.2	mA
					V _{DD} = 3.0 V	0.49	1.2	mA
				f _{IH} = 12 MHz ^{Note 4}	V _{DD} = 5.0 V	0.41	1.0	mA
					V _{DD} = 3.0 V	0.41	1.0	mA
				f _{IH} = 6 MHz ^{Note 4}	V _{DD} = 5.0 V	0.36	0.8	mA
					V _{DD} = 3.0 V	0.36	0.8	mA
				f _{IH} = 3 MHz ^{Note 4}	V _{DD} = 5.0 V	0.33	0.7	mA
					V _{DD} = 3.0 V	0.33	0.7	mA
			LS (low-speed main) mode ^{Note 7} (MCSEL = 0)	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V	290	755	μA
					V _{DD} = 2.0 V	290	755	μA
				f _{IH} = 6 MHz ^{Note 4}	V _{DD} = 3.0 V	240	655	μA
					V _{DD} = 2.0 V	240	655	μA
				f _{IH} = 3 MHz ^{Note 4}	V _{DD} = 3.0 V	210	556	μA
					V _{DD} = 2.0 V	210	556	μA
			LS (low-speed main) mode ^{Note 7} (MCSEL = 1)	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V	220	450	μA
					V _{DD} = 2.0 V	220	450	μA
				f _{IM} = 4 MHz ^{Note 5}	V _{DD} = 3.0 V	60	350	μA
					V _{DD} = 2.0 V	60	350	μA
			LV (low-voltage main) mode ^{Note 7}	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V	625	1200	μA
					V _{DD} = 2.0 V	625	1200	μA
			LP (low-power main) mode ^{Note 7} (MCSEL = 1)	f _{IH} = 1 MHz ^{Note 4}	V _{DD} = 3.0 V	200	410	μA
					V _{DD} = 2.0 V	200	410	μA
				f _{IM} = 1 MHz ^{Note 5}	V _{DD} = 3.0 V	35	150	μA
					V _{DD} = 2.0 V	35	150	μA
HS (high-speed main) mode ^{Note 7}	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.31	1.15	mA			
		Resonator connection	0.53	1.35	mA			
	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.31	1.15	mA			
		Resonator connection	0.53	1.35	mA			
	f _{MX} = 12 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.23	0.85	mA			
		Resonator connection	0.41	0.95	mA			
	f _{MX} = 12 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.23	0.85	mA			
		Resonator connection	0.41	0.95	mA			
	f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.21	0.75	mA			
		Resonator connection	0.36	0.86	mA			
	f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.21	0.75	mA			
		Resonator connection	0.36	0.86	mA			

(Notes and Remarks are listed on the page after the next page.)

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$) (4/6)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit	
Supply current ^{Note 1}	I _{DD2} ^{Note 2}	HALT mode	LS (low-speed main) mode ^{Note 7} (MCSEL = 0)	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	113	420	μA	
				Resonator connection	176	485	μA		
			LS (low-speed main) mode ^{Note 7} (MCSEL = 1)	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input	113	420	μA	
				Resonator connection	176	485	μA		
			LS (low-speed main) mode ^{Note 7} (MCSEL = 1)	f _{MX} = 4 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	41	240	μA	
				Resonator connection	94	290	μA		
			LS (low-speed main) mode ^{Note 7} (MCSEL = 1)	f _{MX} = 4 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input	41	240	μA	
				Resonator connection	94	290	μA		
			LP (low-power main) mode ^{Note 7} (MCSEL = 1)	f _{MX} = 1 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	14	110	μA	
				Resonator connection	70	210	μA		
			LP (low-power main) mode ^{Note 7} (MCSEL = 1)	f _{MX} = 1 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input	14	110	μA	
				Resonator connection	70	210	μA		
		Sub clock operation	f _{SUB} = 32.768 kHz ^{Note 6} , T _A = -40°C	f _{SUB} = 32.768 kHz ^{Note 6} , T _A = -40°C	Square wave input	0.80	6.6	μA	
					Resonator connection	1.00	6.8	μA	
				f _{SUB} = 32.768 kHz ^{Note 6} , T _A = +25°C	Square wave input	1.0	4.1	μA	
					Resonator connection	1.4	4.3	μA	
				f _{SUB} = 32.768 kHz ^{Note 6} , T _A = +50°C	Square wave input	1.2	5.6	μA	
					Resonator connection	1.6	5.7	μA	
				f _{SUB} = 32.768 kHz ^{Note 6} , T _A = +70°C	Square wave input	1.6	9.0	μA	
					Resonator connection	2.0	10.6	μA	
				f _{SUB} = 32.768 kHz ^{Note 6} , T _A = +85°C	Square wave input	2.80	16.2	μA	
					Resonator connection	3.00	19.6	μA	
				f _{IL} = 15 kHz ^{Note 9} , T _A = -40°C	f _{IL} = 15 kHz ^{Note 9} , T _A = -40°C		0.83	1.85	μA
									μA
f _{IL} = 15 kHz ^{Note 9} , T _A = +25°C		1.07	2.25		μA				
					μA				
f _{IL} = 15 kHz ^{Note 9} , T _A = +85°C		2.68	28.1	μA					
				μA					
I _{DD3}	STOP mode ^{Note 8}	T _A = -40°C		0.47	0.95	μA			
		T _A = +25°C		0.66	1.60	μA			
		T _A = +50°C		0.84	4.80	μA			
		T _A = +70°C		1.22	10.60	μA			
		T _A = +85°C		1.94	13	μA			

(Notes and Remarks are listed on the next page.)

Notes 1. Total current flowing into V_{DD} , EV_{DD} , and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD} , V_{RTC} or V_{SS} , EV_{SS} .

The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, the 12-bit A/D converter, $\Delta\Sigma$ A/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
4. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
5. When high-speed on-chip oscillator system clock, low-speed on-chip oscillator, high-speed system clock, and Subsystem clock are stopped.
6. When operating independent power supply RTC and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 $2.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }6\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
 - LP (low-power main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
9. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

- Remarks 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{IM} : Middle-speed on-chip oscillator clock frequency
 4. f_{IL} : Low-speed on-chip oscillator clock frequency
 5. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 6. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Independent power supply RTC operating current	I _{RTC} ^{Note 2}	f _{SUB} = 32.768 kHz		0.70		μA	
12-bit interval timer operating current	I _{TMKA} ^{Notes 1, 3}	f _{SUB} = 38.4 kHz, f _{MAIN} is stopped		0.04		μA	
		f _{SUB} = 32.768 kHz, f _{MAIN} is stopped		0.04		μA	
8-bit interval timer operating current	I _{TMT} ^{Notes 1, 4}	f _{SUB} = 38.4 kHz, f _{MAIN} is stopped, per unit	8-bit counter mode × 2 ch operation		0.14		μA
			16-bit counter mode operation		0.12		μA
		f _{SUB} = 32.768 kHz, f _{MAIN} is stopped, per unit	8-bit counter mode × 2 ch operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	I _{WDT} ^{Notes 1, 5}	f _{IL} = 15 kHz, f _{MAIN} is stopped		0.22		μA	
LVD operating current	I _{LVD} ^{Note 6}			0.10		μA	
LVDVDD operating current	I _{LVDVDD}	Current flowing to V _{DD}		0.05		μA	
LVDVBAT operating current	I _{LVDVBAT}	Current flowing to LVDVBAT		0.04		μA	
		Current flowing to V _{DD}		0.05		μA	
LVDVRTC operating current	I _{LVDVRTC}	Current flowing to V _{RTC}		0.04		μA	
		Current flowing to V _{DD}		0.05		μA	
LVDEXLVD operating current	I _{LVDEXLVD}	Current flowing to EXLVD		0.16		μA	
		Current flowing to V _{DD}		0.05		μA	
Oscillation stop detection circuit operating current	I _{OSDC}			0.02		μA	
12-bit A/D converter operating current	I _{ADC} ^{Note 7}	AV _{REFP} = 5.0 V, when conversion at maximum speed ^{Note 8}		1.2	1.8	mA	
12-bit A/D converter AVREF(+) current	I _{ADREF} ^{Note 9}	AV _{REFP} = 5.0 V, HVSEL[1:0] = 01B ^{Note 10}		50	80	μA	
Temperature sensor operating current	I _{TMPS}			125		μA	
BGO operating current	I _{BGO} ^{Note 11}			2.00	12.20	mA	
Bank programming operating current	I _{BNKP}			5.60	12.20	mA	
Self-programming operating current	I _{FSP} ^{Note 12}			2.00	12.20	mA	

(Notes and Remarks are listed on the page after the next page.)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0 V)

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Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
24-Bit ΔΣ A/D Converter operating current	IDSAD ^{Note 13}	In 4 ch ΔΣ A/D converter operation				1.45	2.30	mA
		In 3 ch ΔΣ A/D converter operation				1.14	1.85	mA
		In 1 ch ΔΣ A/D converter operation				0.52	0.94	mA
SNOOZE operating current	ISNOZ ^{Note 14}	Simplified SPI (CSI)/UART operation				0.70	1.05	mA
		DTC operation				2.20		mA
LCD operating current	ILCD1 ^{Notes 15, 16}	External resistance division method	f _{LCD} = f _{SUB} (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices	V _{DD} = 5.0 V, V _{L4} = 5.0 V		0.06		μA
				V _{DD} = 3.0 V, V _{L4} = 3.0 V (VLCD = 04H)		0.85		μA
	ILCD2 ^{Note 15}	Internal voltage boosting method	f _{LCD} = f _{SUB} (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices	V _{DD} = 5.0 V, V _{L4} = 5.1 V (VLCD = 12H)		1.55		μA
				V _{DD} = 3.0 V, V _{L4} = 3.0 V		0.20		μA
ILCD3 ^{Note 15}	Capacitor split method	f _{LCD} = f _{SUB} (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices	V _{DD} = 3.0 V, V _{L4} = 3.0 V		0.20		μA	
Timer RJ operating current	ITMRJ ^{Note 17}	f _{SX} = 32.768 or 38.4 kHz, f _{MAIN} is stopped, per unit				0.10		μA
Serial interface UARTMG operating current	IUARTMG ^{Note 18}	f _{SX} = 38.4 kHz, f _{MAIN} is stopped, per unit				0.12		μA
Sampling output timer detector operating current	ISMOTD ^{Note 19}	f _{SX} = 32.768 or 38.4 kHz, f _{MAIN} is stopped, per unit				0.10		μA
VREFADC operating current	IVREFOUT ^{Note 20}	VREFAMPCNT.BGREN = 1 VREFAMPCNT.VREFADCEN = 1 ^{Note 8}				73	130	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. When high speed on-chip oscillator and high-speed system clock are stopped.
 2. Current flowing to V_{RTC} pin, including RTC power supply, subsystem clock oscillator circuit, and RTC.
 3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and XT1 oscillator). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{TMKA} , when the 12-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 4. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and XT1 oscillator). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{TMT} , when the 8-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} , I_{DD2} , or I_{DD3} , and I_{WDT} when the watchdog timer operates.
 6. Current flowing only to the LVD circuit. The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} , I_{DD2} , or I_{DD3} , and I_{LVD} when the LVD circuit operates.
 7. Current flowing only to the 12-bit A/D converter. The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{ADC} when the 12-bit A/D converter operates in the operating mode or HALT mode.
 8. Current flowing to AV_{DD} .
 9. Current flowing from the reference voltage source of the 12-bit A/D converter.
 10. Current flowing to AV_{REFF} .
 11. Current flowing only during rewrite of 1 KB data flash memory.
 12. Current flowing only during self programming.
 13. Current flowing only to the 24-bit $\Delta\Sigma$ A/D converter. The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{DSAD} when the 24-bit $\Delta\Sigma$ A/D converter operates.
 14. For shift time to the SNOOZE mode, see **29.3.3 SNOOZE mode** in the RL78/I1C (512 KB) User's Manual.
 15. Current flowing only to the LCD controller/driver. The supply of current to an RL78 microcontroller is the sum of the supply current (I_{DD1} or I_{DD2}) and the LCD operating current (I_{LCD1} , I_{LCD2} , or I_{LCD3}) when the LCD controller/driver operates in the operating mode or HALT mode. Not including the current that flows through the LCD panel. Conditions of the TYP. value and MAX. value are as follows.
 - Setting 20 pins as the segment function and blinking all
 - Selecting f_{SUB} for system clock when LCD clock = 128 Hz (LCDC0 = 07H)
 - Setting four time slices and 1/3 bias
 16. Not including the current flowing into the external division resistor when using the external resistance division method.
 17. Current flowing only to the timer RJ (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{TMRJ} , when the timer RJ operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
 18. Current flowing only to the serial interface UARTMG (excluding the operating current of the XT1 oscillator). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{UARTMG} , when the serial interface UARTMG operates in the operating mode or HALT mode.
 19. Current flowing only to the sampling output timer detector (excluding the operating current of the XT1 oscillator). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and I_{SMOTD} , when the sampling output timer detector operates in the operating mode or HALT mode.
 20. Current flowing only to the voltage reference (VREFADC). The supply of current to an RL78 microcontroller is the sum of the values of I_{DD1} or I_{DD2} , and $I_{VREFOUT}$, when the voltage reference operates in the operating mode or HALT mode.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

(1/2)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
				2.1 V ≤ V _{DD} < 2.4 V	0.16667		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
				LS (low-speed main) mode (MCSEL = 1)	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25		1
			LP (low-power main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	1			μs
		Subsystem clock (f _{SUB}) operation	f _{XT} = 38.4 kHz	1.8 V ≤ V _{DD} ≤ 5.5 V		26.0		μs
			f _{XT} = 32.768 kHz	1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
				2.1 V ≤ V _{DD} < 2.4 V	0.16667		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V		0.25		1	μs		
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V		1		20	MHz	
		2.4 V ≤ V _{DD} < 2.7 V		1		16	MHz	
		1.8 V ≤ V _{DD} < 2.4 V		1		8	MHz	
		1.6 V ≤ V _{DD} < 1.8 V		1		4	MHz	
	f _{EXS}	f _{EX} = 38.4 kHz		31		39	kHz	
		f _{EX} = 32.768 kHz		32		35	kHz	
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V		24			ns	
		2.4 V ≤ V _{DD} < 2.7 V		30			ns	
		1.8 V ≤ V _{DD} < 2.4 V		60			ns	
		1.6 V ≤ V _{DD} < 1.8 V		120			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
TI00 to TI07 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns	
Timer RJ input cycle	t _C	TRJIO0, TRJIO1	2.7 V ≤ V _{DD} ≤ 5.5 V	100			ns	
			1.8 V ≤ V _{DD} < 2.7 V	300			ns	
Timer RJ input high-level width, low-level width	t _{TRJH} , t _{TRJL}	TRJIO0, TRJIO1	2.7 V ≤ V _{DD} ≤ 5.5 V	40			ns	
			1.8 V ≤ V _{DD} < 2.7 V	120			ns	

(Remark is listed on the next page.)

(TA = -40 to +85°C, 1.6 V ≤ AVDD = EVDD = VDD ≤ 5.5 V, AVSS = VSS = EVSS = 0 V)

(2/2)

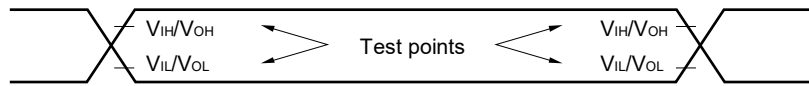
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer output frequency	f _{ro}	TO00 to TO07, TRJIO0, TRJIO1, TRJO0, TRJO1	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V		16	MHz
				2.7 V ≤ EV _{DD} < 4.0 V		8	MHz
				2.4 V ≤ EV _{DD} < 2.7 V		4	MHz
				2.1 V ≤ EV _{DD} < 2.4 V		4	MHz
			LS (low-speed main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V		4	MHz
			LP (low-power main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V		0.5	MHz
			LV (low-voltage main) mode	1.6 V ≤ EV _{DD} ≤ 5.5 V		2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ EV _{DD} ≤ 5.5 V		16	MHz	
			2.7 V ≤ EV _{DD} < 4.0 V		8	MHz	
			2.4 V ≤ EV _{DD} < 2.7 V		4	MHz	
			2.1 V ≤ EV _{DD} < 2.4 V		4	MHz	
			LS (low-speed main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V		4	MHz
			LP (low-power main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V		1	MHz
			LV (low-voltage main) mode	1.8 V ≤ EV _{DD} ≤ 5.5 V		4	MHz
1.6 V ≤ EV _{DD} < 1.8 V		2		MHz			
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0, INTP8, INTP9, INTP12 to INTP14	1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP7	1.6 V ≤ EV _{DD} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR7	1.8 V ≤ EV _{DD} ≤ 5.5 V	250			ns
			1.6 V ≤ EV _{DD} < 1.8 V	1			μs
RESET low-level width	t _{RSL}			10			μs

Remark f_{MCK}: Timer array unit operation clock frequency

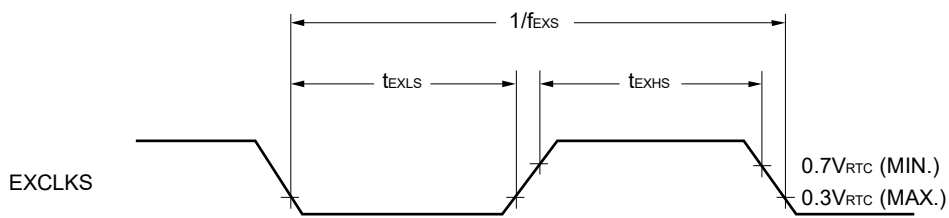
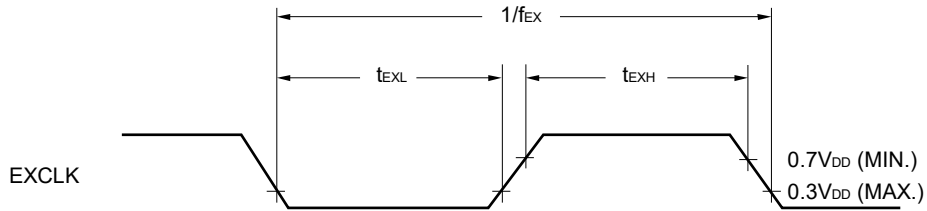
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn))

m: Unit number (m = 0), n: Channel number (n = 0 to 7))

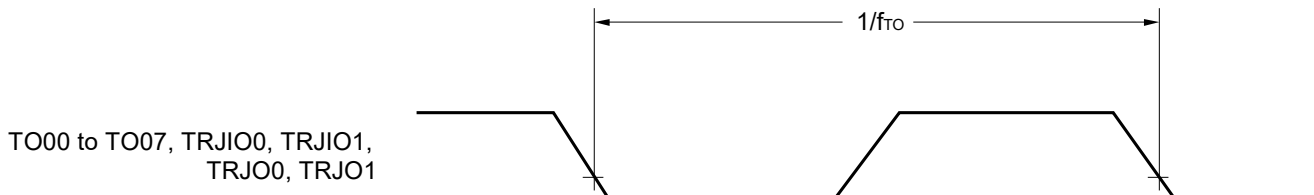
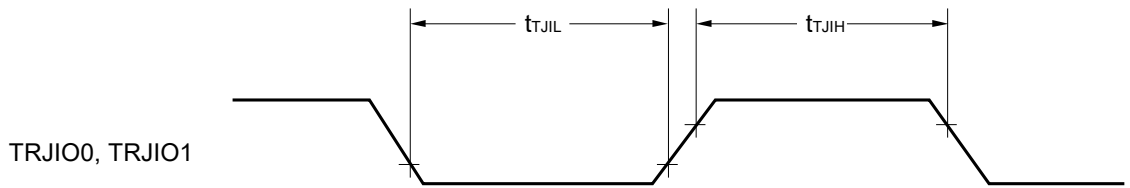
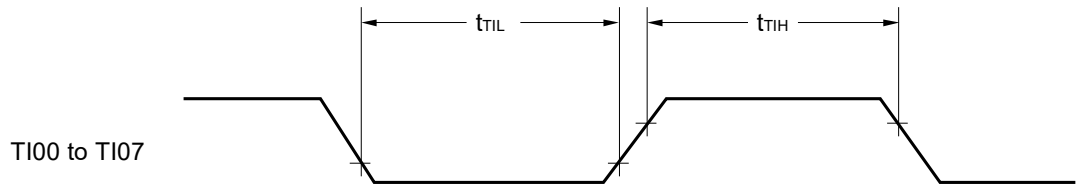
AC Timing Test Points



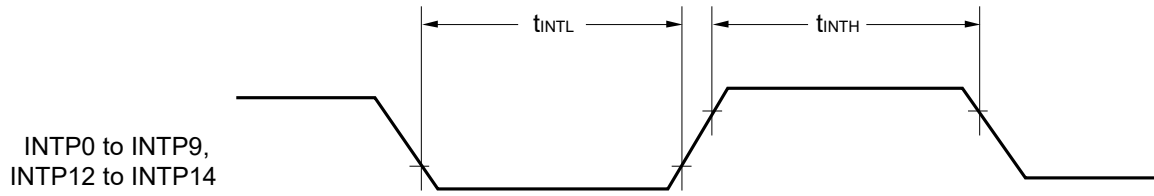
External System Clock Timing



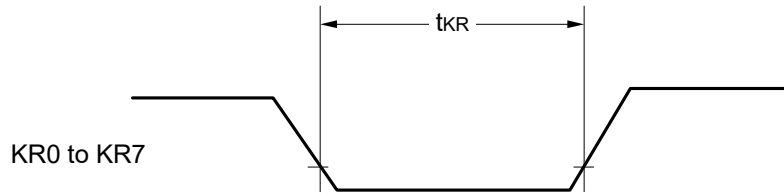
TI/TO Timing



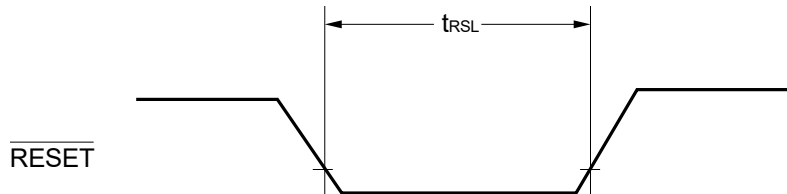
Interrupt Request Input Timing



Key interrupt Input Timing

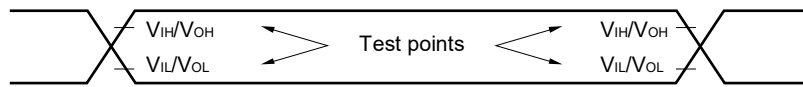


$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)
 ($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate ^{Note 1}		$2.7\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps	
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		5.3		1.3		0.1		0.6	Mbps	
		$2.4\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps	
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		4.0		1.3		0.1		0.6	Mbps	
		$2.1\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps	
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}		1.0		1.3		0.1		0.6	Mbps	
		$1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$					$f_{MCK}/6$		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}					1.3		0.1		0.6	Mbps
		$1.6\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$									$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 2}									0.6	Mbps

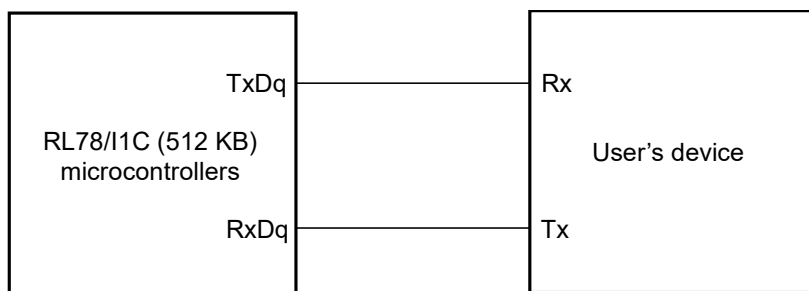
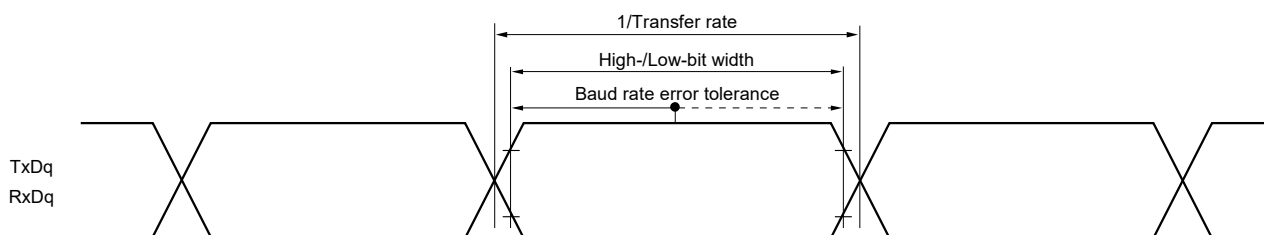
Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

- HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
 16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
 6 MHz ($2.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
- LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
- LP (low-power main) mode: 1 MHz ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
- LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks are listed on the next page.)

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

- Remarks**
1. q: UART number (q = 0 to 4), g: PIM and POM number (g = 0, 1, 5, 8)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13, 20, 21))

(2) During communication at same potential (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output)**(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	2.7 V ≤ EV _{DD} ≤ 5.5 V	125		500		4000		1000		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	250		500		4000		1000		ns
		2.1 V ≤ EV _{DD} ≤ 5.5 V	667		500		4000		1000		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			500		4000		1000		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V							1000		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} / 2 – 12		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		2.7 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} / 2 – 18		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} / 2 – 38		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		2.1 V ≤ EV _{DD} ≤ 5.5 V	t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V							t _{KCY1} / 2 – 100		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V	44		110		110		110		ns
		2.7 V ≤ EV _{DD} ≤ 5.5 V	44		110		110		110		ns
		2.4 V ≤ EV _{DD} ≤ 5.5 V	75		110		110		110		ns
		2.1 V ≤ EV _{DD} ≤ 5.5 V	110		110		110		110		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V			110		110		110		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI1}	1.8 V ≤ EV _{DD} ≤ 5.5 V	19		19		19		19		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V							19		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO1}	C = 30 pF ^{Note 3}	1.8 V ≤ EV _{DD} ≤ 5.5 V	25		25		25		25	ns
			1.6 V ≤ EV _{DD} ≤ 5.5 V							25	ns

Notes 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” and the Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10, 30), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),

g: PIM and POM numbers (g = 0, 1, 5, 8)

2. f_{MCK}: Serial array unit operation clock frequency

(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 02, 12))

(3) During communication at same potential (Simplified SPI (CSI) mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit	
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCKp cycle time ^{Note 4}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V	20 MHz < f _{MCK}	8/f _{MCK}		–		–		–		ns	
			f _{MCK} ≤ 20 MHz	6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		ns	
		2.7 V ≤ EV _{DD} ≤ 5.5 V	16 MHz < f _{MCK}	8/f _{MCK}		–		–		–		ns	
			f _{MCK} ≤ 16 MHz	6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		6/f _{MCK}		ns	
		2.4 V ≤ EV _{DD} ≤ 5.5 V			6/f _{MCK} and 500		6/f _{MCK} and 500		6/f _{MCK} and 500		6/f _{MCK} and 500		ns
		2.1 V ≤ EV _{DD} ≤ 5.5 V			6/f _{MCK} and 750		6/f _{MCK} and 750		6/f _{MCK} and 750		6/f _{MCK} and 750		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V					6/f _{MCK} and 750		6/f _{MCK} and 750		6/f _{MCK} and 750		ns
		1.6 V ≤ EV _{DD} ≤ 5.5 V									6/f _{MCK} and 1500		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V		t _{KCY2} / 2 – 7		t _{KCY2} / 2 – 7		t _{KCY2} / 2 – 7		t _{KCY2} / 2 – 7		ns	
		2.7 V ≤ EV _{DD} ≤ 5.5 V		t _{KCY2} / 2 – 8		t _{KCY2} / 2 – 8		t _{KCY2} / 2 – 8		t _{KCY2} / 2 – 8		ns	
		2.1 V ≤ EV _{DD} ≤ 5.5 V		t _{KCY2} / 2 – 18		t _{KCY2} / 2 – 18		t _{KCY2} / 2 – 18		t _{KCY2} / 2 – 18		ns	
		1.8 V ≤ EV _{DD} ≤ 5.5 V				t _{KCY2} / 2 – 18		t _{KCY2} / 2 – 18		t _{KCY2} / 2 – 18		ns	
		1.6 V ≤ EV _{DD} ≤ 5.5 V								t _{KCY2} / 2 – 66		ns	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} +20		1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		ns	
		2.1 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		ns	
		1.8 V ≤ EV _{DD} ≤ 5.5 V				1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		ns	
		1.6 V ≤ EV _{DD} ≤ 5.5 V								1/f _{MCK} +40		ns	
Slp hold time (from SCKp↑) ^{Note 1}	t _{SI2}	2.1 V ≤ EV _{DD} ≤ 5.5 V		1/f _{MCK} +31		1/f _{MCK} +31		1/f _{MCK} +31		1/f _{MCK} +31		ns	
		1.8 V ≤ EV _{DD} ≤ 5.5 V				1/f _{MCK} +31		1/f _{MCK} +31		1/f _{MCK} +31		ns	
		1.6 V ≤ EV _{DD} ≤ 5.5 V								1/f _{MCK} +250		ns	
Delay time from SCKp↓ to SOp output ^{Note 2}	t _{KS02}	C = 30 pF ^{Note 3}	2.7 V ≤ EV _{DD} ≤ 5.5 V			2/f _{MCK} + 44		2/f _{MCK} + 110		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			2.4 V ≤ EV _{DD} ≤ 5.5 V			2/f _{MCK} + 75		2/f _{MCK} + 110		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			2.1 V ≤ EV _{DD} ≤ 5.5 V			2/f _{MCK} + 100		2/f _{MCK} + 110		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.8 V ≤ EV _{DD} ≤ 5.5 V					2/f _{MCK} + 110		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.6 V ≤ EV _{DD} ≤ 5.5 V									2/f _{MCK} + 220	ns

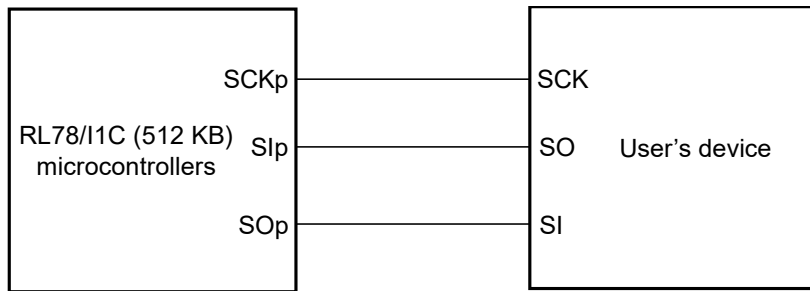
(Notes, Caution, and Remarks are listed on the next page.)

- Notes**
1. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The S_{lp} setup time becomes “to $SCK_{p\downarrow}$ ” and the S_{lp} hold time becomes “from $SCK_{p\downarrow}$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 2. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to S_{op} output becomes “from $SCK_{p\uparrow}$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 3. C is the load capacitance of the S_{Op} output lines.
 4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

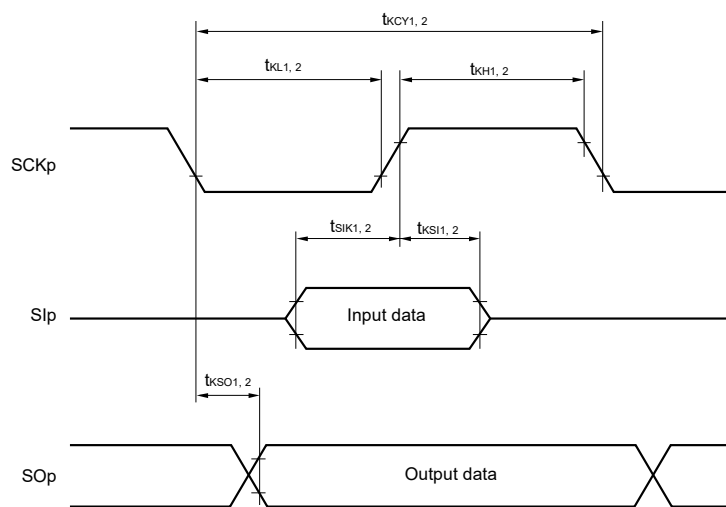
Caution Select the normal input buffer for the S_{lp} pin and SCK_{p} pin and the normal output mode for the S_{Op} pin by using port input mode register g (PIM g) and port output mode register g (POM g).

- Remarks**
1. p : CSI number ($p = 00, 10, 30$), m : Unit number ($m = 0, 1$), n : Channel number ($n = 0, 2$),
 g : PIM number ($g = 0, 1, 5, 8$)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPS m) and the CKS mn bit of serial mode register mn (SMR mn).
 m : Unit number, n : Channel number ($mn = 00, 02, 12$))

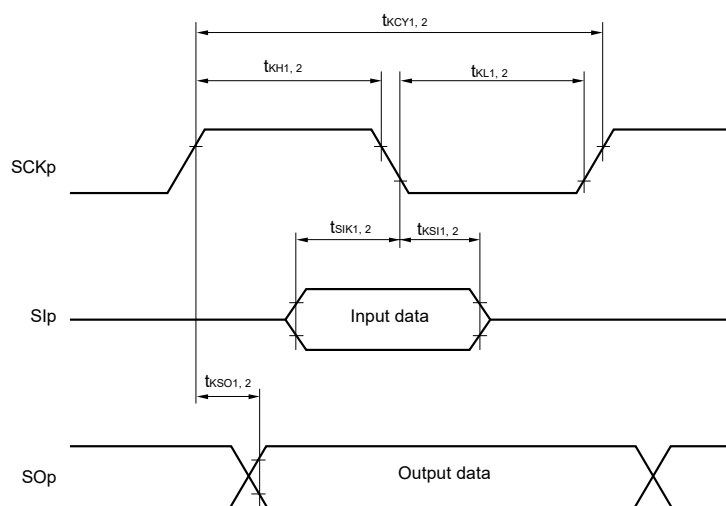
Simplified SPI (CSI) mode connection diagram (during communication at same potential)



**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)
(when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**



**Simplified SPI (CSI) mode serial transfer timing (during communication at same potential)
(when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)**



- Remarks**
1. p: CSI number (p = 00, 10, 30)
 2. m: Unit number, n: Channel number (mn = 00, 02, 12)

(4) During communication at same potential (simplified I²C mode)(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ EV _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}	kHz
		1.8 V ≤ EV _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}		400 ^{Note 1}	
		1.8 V ≤ EV _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ				300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	
		1.6 V ≤ EV _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ								250 ^{Note 1}	
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		1150		
		1.8 V ≤ EV _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ			1550		1550		1550		
		1.6 V ≤ EV _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ							1850		
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		1150		
		1.8 V ≤ EV _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ			1550		1550		1550		
		1.6 V ≤ EV _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ							1850		
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Notes 1, 2		1/f _{MCK} + 145 Notes 1, 2		1/f _{MCK} + 145 Notes 1, 2		1/f _{MCK} + 145 Notes 1, 2		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Notes 1, 2		1/f _{MCK} + 145 Notes 1, 2		1/f _{MCK} + 145 Notes 1, 2		1/f _{MCK} + 145 Notes 1, 2		
		1.8 V ≤ EV _{DD} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ			1/f _{MCK} + 230 Notes 1, 2		1/f _{MCK} + 230 Notes 1, 2		1/f _{MCK} + 230 Notes 1, 2		
		1.6 V ≤ EV _{DD} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ							1/f _{MCK} + 290 Notes 1, 2		

(Notes, Caution, and Remarks are listed on the next page.)

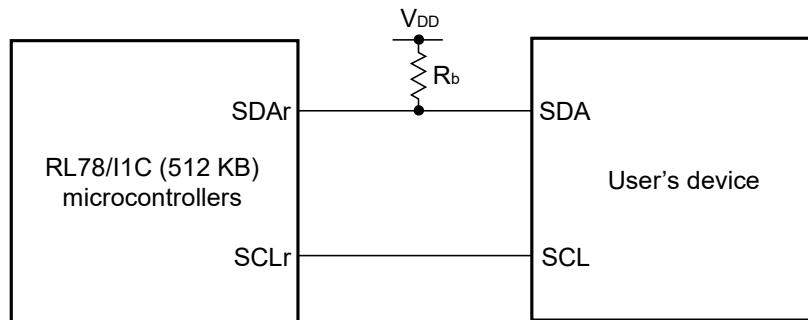
($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

(2/2)

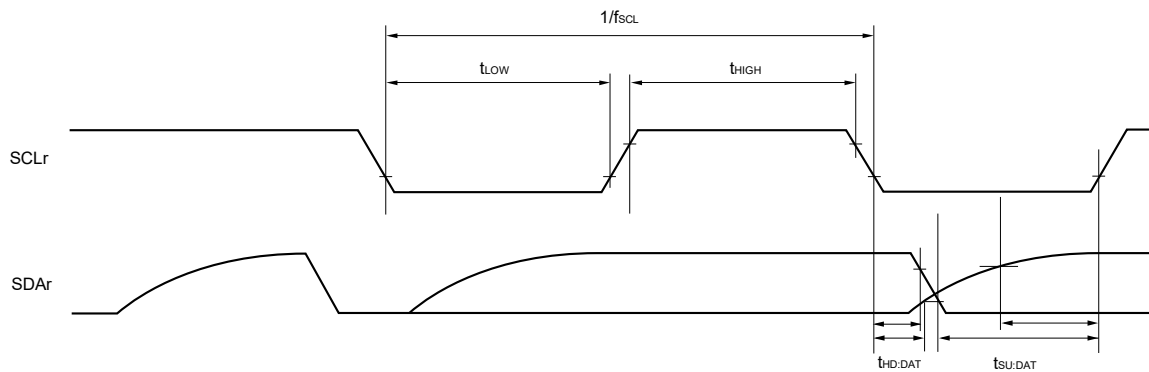
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data hold time (transmission)	$t_{HD:DAT}$	$2.7\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	0	305	ns
		$1.8\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	355	0	355	0	355	0	355	ns
		$1.8\text{ V} \leq EV_{DD} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$			0	405	0	405	0	405	ns
		$1.6\text{ V} \leq EV_{DD} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$							0	405	ns

- Notes**
- The value must also be equal to or less than $f_{MCK}/4$.
 - Set the f_{MCK} value to keep the hold time of $SCLr = "L"$ and $SCLr = "H"$.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the $SDAr$ pin and the normal output mode for the $SCLr$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
- $R_b[\Omega]$: Communication line ($SDAr$) pull-up resistance, $C_b[F]$: Communication line ($SDAr$, $SCLr$) load capacitance
 - r: IIC number (r = 00, 10, 30), g: PIM and POM number (g = 0, 1, 5, 8)
 - f_{MCK} : Serial array unit operation clock frequency (Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 12))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate		Reception	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}	bps
					5.3		1.3		0.1		0.6	Mbps
			2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}		f _{MCK} /6 ^{Note 1}	bps
					5.3		1.3		0.1		0.6	Mbps
			1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		f _{MCK} /6 ^{Notes 1, 2}		f _{MCK} /6 ^{Notes 1, 2}		f _{MCK} /6 ^{Notes 1, 2}		f _{MCK} /6 ^{Notes 1, 2}	bps
					5.3		1.3		0.1		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with EV_{DD} ≥ V_b.**3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V),16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V),6 MHz (2.1 V ≤ V_{DD} ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0 to 4), g: PIM and POM number (g = 0, 1, 5, 8)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13, 20, 21))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate	Transmission	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		Notes 1, 2		Notes 1, 2		Notes 1, 2		Notes 1, 2	bps
		Theoretical value of the maximum transfer rate ^{Note 9} C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.8 ^{Note 3}		2.8 ^{Note 3}		2.8 ^{Note 3}		2.8 ^{Note 3}	Mbps
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		Notes 2, 4		Notes 2, 4		Notes 2, 4		Notes 2, 4	bps
		Theoretical value of the maximum transfer rate ^{Note 9} C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 ^{Note 5}		1.2 ^{Note 5}		1.2 ^{Note 5}		1.2 ^{Note 5}	Mbps
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		Notes 2, 6, 7		Notes 2, 6, 7		Notes 2, 6, 7		Notes 2, 6, 7	bps
		Theoretical value of the maximum transfer rate ^{Note 9} C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 ^{Note 8}		0.43 ^{Note 8}		0.43 ^{Note 8}		0.43 ^{Note 8}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- Transfer rate in the SNOOZE mode is 4800 bps only.
- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- Notes**
- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.
 - Use it with $EV_{DD} \geq V_b$.
 - The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $1.8 \text{ V} \leq EV_{DD} < 3.3 \text{ V}$ and $1.6 \text{ V} \leq V_b \leq 2.0 \text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

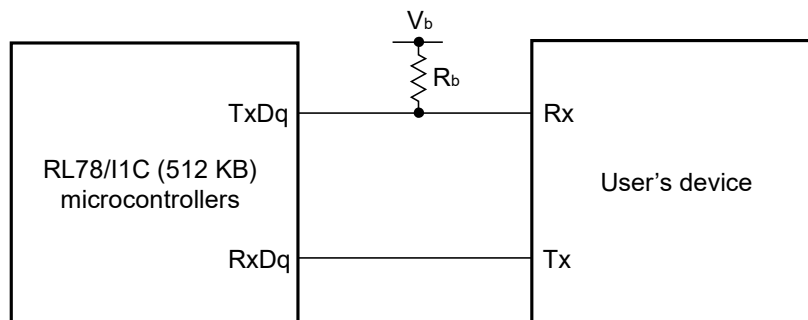
* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.
- The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
 HS (high-speed main) mode: 32 MHz ($2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$),
 16 MHz ($2.4 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$),
 6 MHz ($2.1 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$)
 LS (low-speed main) mode: 8 MHz ($1.8 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$)
 LP (low-power main) mode: 1 MHz ($1.8 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$)
 LV (low-voltage main) mode: 4 MHz ($1.6 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$)

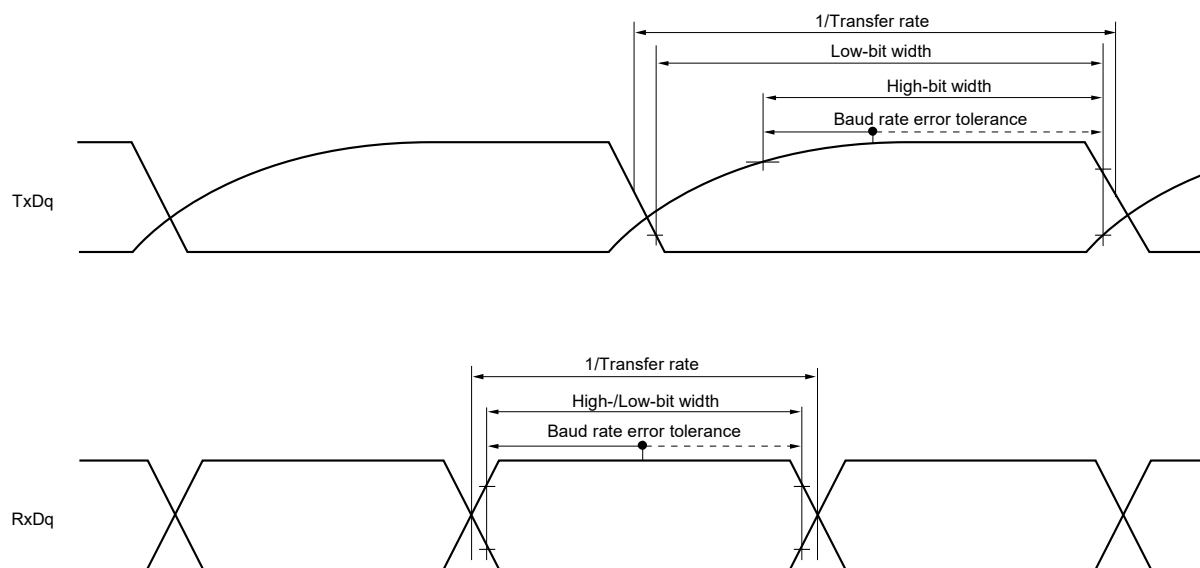
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
- $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
 - q: UART number (q = 0 to 4), g: PIM and POM number (g = 0, 1, 5, 8)
 - f_{MCK} : Serial array unit operation clock frequency
 (Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13, 20, 21))

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 4), g: PIM and POM number (g = 0, 1, 5, 8)

(6) Communication at different potential (2.5 V, 3 V) ($f_{MCK}/2$) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$ $4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	200		1150		1150		1150		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	300		1150		1150		1150		ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	58		479		479		479		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	121		479		479		479		ns
Slp hold time (from SCKp \uparrow) ^{Note 1}	t_{KSH1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	10		10		10		10		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	10		10		10		10		ns
Delay time from SCKp \downarrow to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		60	60		60		60		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		130	130		130		130		ns
Slp setup time (to SCKp \downarrow) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	23		110		110		110		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	33		110		110		110		ns

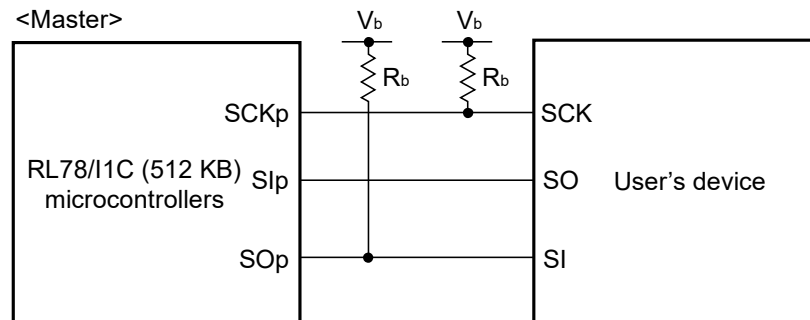
(Notes, Caution, and Remarks are listed on the next page.)

(6) Communication at different potential (2.5 V, 3 V) ($f_{MCK}/2$) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp hold time (from SCKp↓) ^{Note 2}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	10		10		10		10		ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	10		10		10		10		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		10		10		10		10	ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		10		10		10		10	ns

Notes 1. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$.2. When $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Simplified SPI (CSI) mode connection diagram (during communication at different potential)

Remarks 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage

2. p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12), g: PIM and POM number (g = 0, 1, 5, 8)

3. f_{MCK} : Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

4. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK/4}) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output) (1/2)(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK} 4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		1150		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		1150		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} / 2 – 75		t _{KCY1} / 2 – 75		t _{KCY1} / 2 – 75		t _{KCY1} / 2 – 75		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} / 2 – 170		t _{KCY1} / 2 – 170		t _{KCY1} / 2 – 170		t _{KCY1} / 2 – 170		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} / 2 – 458		t _{KCY1} / 2 – 458		t _{KCY1} / 2 – 458		t _{KCY1} / 2 – 458		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} / 2 – 12		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} / 2 – 18		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		t _{KCY1} / 2 – 50		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		479		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		479		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		479		ns

(Notes, Caution, and Remarks are listed on the page after the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) ($f_{MCK}/4$) (Simplified SPI (CSI) mode) (master mode, SCKp... internal clock output) (2/2)(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp hold time (from SCKp↑) ^{Note 1}	t _{KS1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		19		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		19		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KS01}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100		100	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195		195	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ		483		483		483		483	ns
Slp setup time (to SCKp↓) ^{Note 2}	t _{SIK1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	44		110		110		110		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	44		110		110		110		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	110		110		110		110		ns
Slp hold time (from SCKp↓) ^{Note 2}	t _{KS1}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		19		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		19		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	t _{KS01}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		25		25		25		25	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		25		25		25		25	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 3} , C _b = 30 pF, R _b = 5.5 kΩ		25		25		25		25	ns

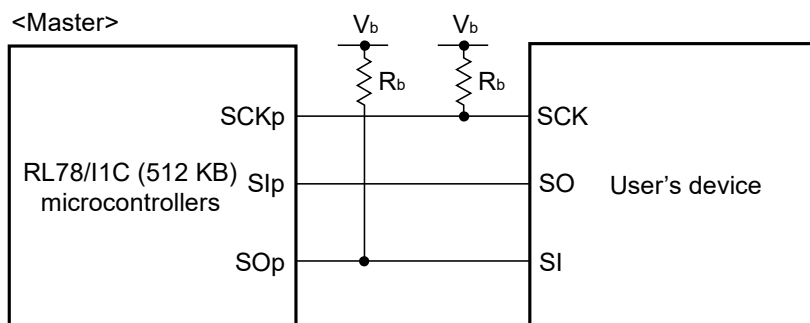
(Notes, Caution and Remarks are listed on the next page.)

- Notes**
1. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$.
 2. When $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 3. Use it with $EV_{DD} \geq V_b$.

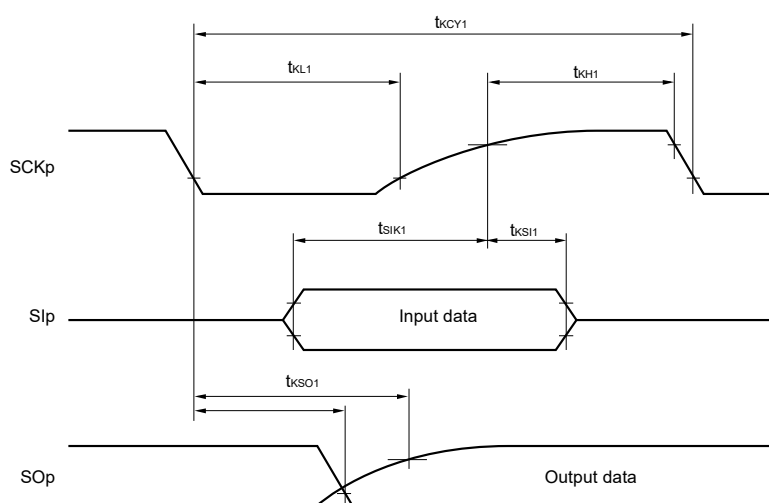
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and $SCKp$ pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line ($SCKp$, SOp) pull-up resistance, $C_b[F]$: Communication line ($SCKp$, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12), g: PIM and POM number (g = 0, 1, 5, 8)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the $CKSmn$ bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

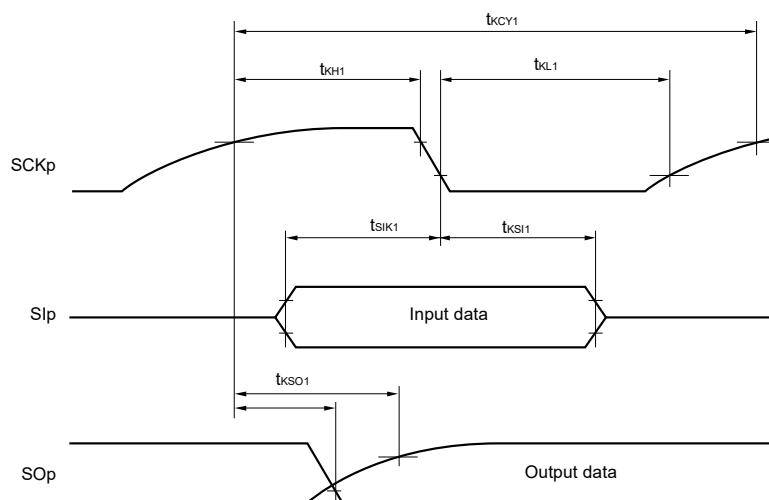
Simplified SPI (CSI) mode connection diagram (during communication at different potential)



Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential) (when $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$)



**Simplified SPI (CSI) mode serial transfer timing (master mode) (during communication at different potential)
(when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)**



Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remark p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12),
g: PIM and POM number (g = 0, 1, 5, 8)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI (CSI) mode) (slave mode, SCKp ... external clock input)**(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V) (1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	24 MHz < f _{MCK}	14/f _{MCK}		–		–		–		ns
			20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}		–		–		–		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		–		–		–		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		–		–		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/f _{MCK}		10/f _{MCK}		10/f _{MCK}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	24 MHz < f _{MCK}	20/f _{MCK}		–		–		–		ns
			20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}		–		–		–		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		–		–		–		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		–		–		–		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/f _{MCK}		–		–		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	24 MHz < f _{MCK}	48/f _{MCK}		–		–		–		ns
			20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}		–		–		–		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		–		–		–		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		–		–		–		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		16/f _{MCK}		–		–		ns
				f _{MCK} ≤ 4 MHz		10/f _{MCK}		10/f _{MCK}		10/f _{MCK}		10/f _{MCK}
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /		t _{KCY2} /		t _{KCY2} /		t _{KCY2} /		ns	
			2 – 12		2 – 50		2 – 50		2 – 50			
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /		t _{KCY2} /		t _{KCY2} /		t _{KCY2} /		ns	
			2 – 18		2 – 50		2 – 50		2 – 50			
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /		t _{KCY2} /		t _{KCY2} /		t _{KCY2} /		ns	
			2 – 50		2 – 50		2 – 50		2 – 50			
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	2.7 V ≤ EV _{DD} ≤ 5.5 V, 2.3 V ≤ V _b ≤ 4.0 V ^{Note 2}	1/f _{MCK}	+ 20	1/f _{MCK}	+ 30	1/f _{MCK}	+ 30	1/f _{MCK}	+ 30	ns	
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK}	+ 30	1/f _{MCK}	+ 30	1/f _{MCK}	+ 30	1/f _{MCK}	+ 30	ns	
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI2}	2.7 V ≤ EV _{DD} ≤ 5.5 V, 2.3 V ≤ V _b ≤ 4.0 V ^{Note 2}	1/f _{MCK}	+ 31	1/f _{MCK}	+ 31	1/f _{MCK}	+ 31	1/f _{MCK}	+ 31	ns	
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK}	+ 31	1/f _{MCK}	+ 31	1/f _{MCK}	+ 31	1/f _{MCK}	+ 31	ns	

(Notes, Caution and Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (Simplified SPI (CSI) mode) (slave mode, SCKp ... external clock input)

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = EV_{DD} = V_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$) (2/2)

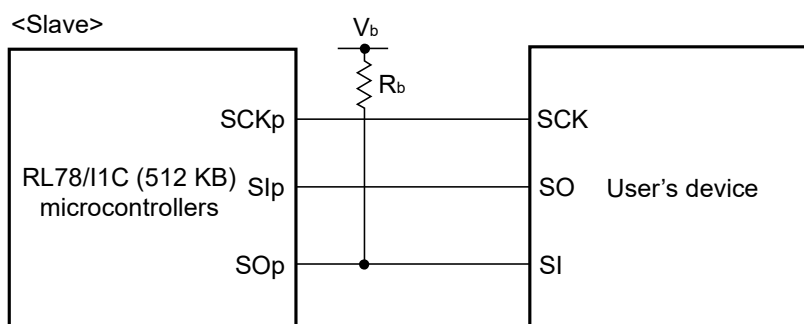
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Delay time from SCKp↓ to SOp output ^{Note 4}	t_{kSO2}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{MCK}$ + 120		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573	ns
		$2.7\text{ V} \leq EV_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{MCK}$ + 214		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573	ns
		$1.8\text{ V} \leq EV_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573		$2/f_{MCK}$ + 573	ns

- Notes**
1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
 2. Use it with $EV_{DD} \geq V_b$.
 3. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The SIp setup time becomes “to SCKp↓” and the SIp hold time becomes “from SCKp↓” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 4. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOp output becomes “from SCKp↑” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

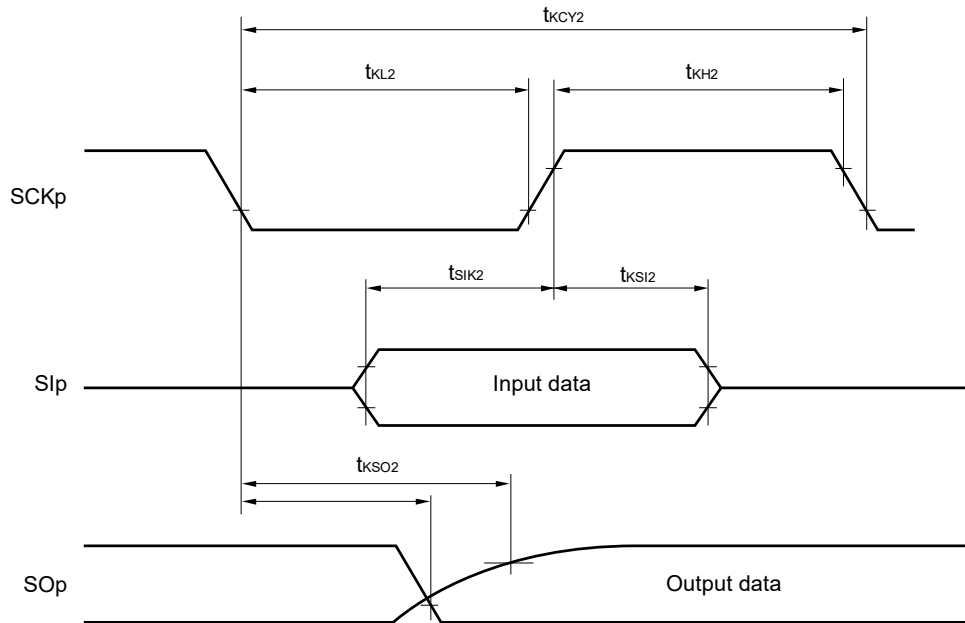
Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12), g: PIM and POM number (g = 0, 1, 5, 8)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

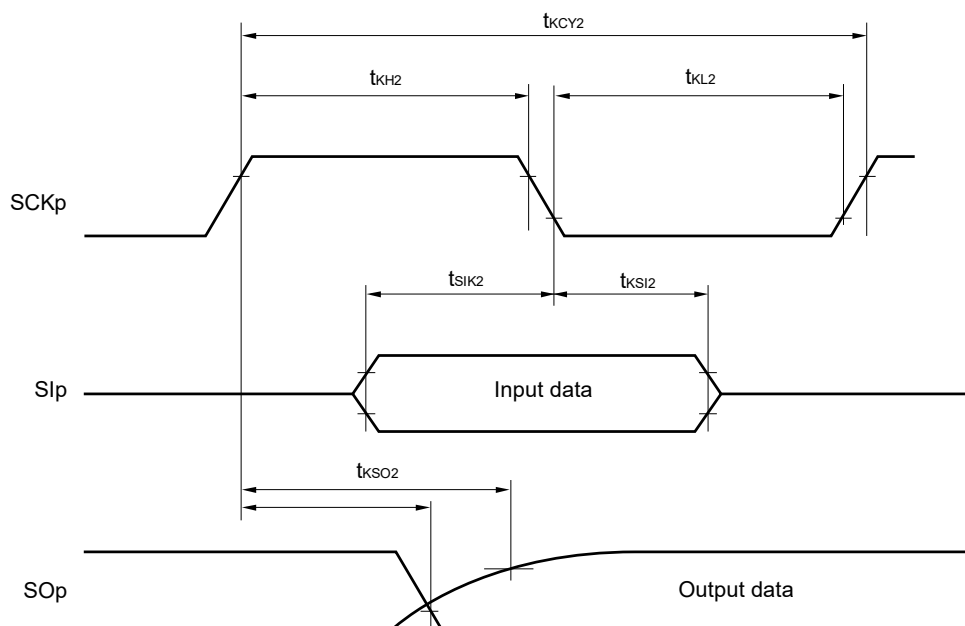
Simplified SPI (CSI) mode connection diagram (during communication at different potential)



**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential)
(when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)**



**Simplified SPI (CSI) mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Caution Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (E_{VDD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remark p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12), g: PIM and POM number (g = 0, 1, 5, 8)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}		300 ^{Note 1}	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		1550		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		1550		ns
		4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1150		1150		1150		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1150		1150		1150		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1150		1150		1150		1150		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		610		610		610		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		610		610		610		ns
		4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		610		610		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		610		610		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		610		ns

(Notes, Caution and Remarks are listed on the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)**

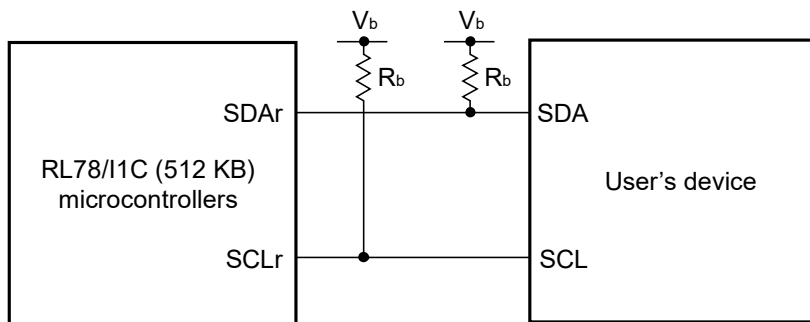
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU, DAT}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		ns
		4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		ns
Data hold time (transmission)	t _{HD, DAT}	4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		4.0 V ≤ EV _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	0	355	0	355	ns
		2.7 V ≤ EV _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.**2.** Use it with EV_{DD} ≥ V_b.**3.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

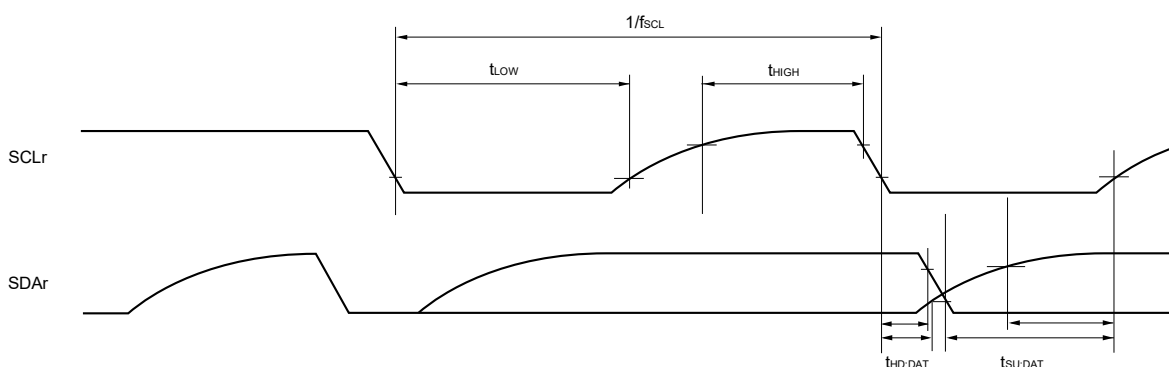
Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

- Remarks**
1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage
 2. r: IIC number (r = 00, 10, 30), g: PIM, POM number (g = 0, 1, 5, 8)
 3. f_{MCK}: Serial array unit operation clock frequency (Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

2.5.2 Serial interface UARTMG

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		f _{sx} = 38.4 kHz	200		9600	bps
		f _{sx} = 38.4 kHz (when the clock doubler is in use)	200		19200	bps

2.5.3 Serial interface IICA

(1) I²C standard mode (1/2)(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			2.1 V ≤ EV _{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	0	100	0	100	0	100	kHz
			1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs	
		2.1 V ≤ EV _{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	4.7		μs	
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs	
		2.1 V ≤ EV _{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	4.0		μs	
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs	
		2.1 V ≤ EV _{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	4.7		μs	
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs	
		2.1 V ≤ EV _{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	4.0		μs	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	250		250		250		250		μs	
		2.1 V ≤ EV _{DD} ≤ 5.5 V	250		250		250		250		μs	
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	250		250		250		μs	
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	250		μs	
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	0	3.45	μs	
		2.1 V ≤ EV _{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	0	3.45	μs	
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	0	3.45	0	3.45	0	3.45	μs	
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	0	3.45	μs	

(Notes and Remark are listed on the next page.)

(1) I²C standard mode (2/2)(T_A = -40 to +85°C, 1.6 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs
		2.1 V ≤ EV _{DD} ≤ 5.5 V	4.0		4.0		4.0		4.0		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	4.0		4.0		4.0		μs
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	4.0		μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs
		2.1 V ≤ EV _{DD} ≤ 5.5 V	4.7		4.7		4.7		4.7		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V	–	–	4.7		4.7		4.7		μs
		1.6 V ≤ EV _{DD} ≤ 5.5 V	–	–	–	–	–	–	4.7		μs

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	400	0	400	–	–	0	400	kHz
			1.8 V ≤ EV _{DD} ≤ 5.5 V	0	400	0	400	–	–	0	400	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		100		100		–	–	100		ns
		1.8 V ≤ EV _{DD} ≤ 5.5 V		100		100		–	–	100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0	0.9	0	0.9	–	–	0	0.9	μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		0	0.9	0	0.9	–	–	0	0.9	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		0.6		0.6		–	–	0.6		μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs
		1.8 V ≤ EV _{DD} ≤ 5.5 V		1.3		1.3		–	–	1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = EV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

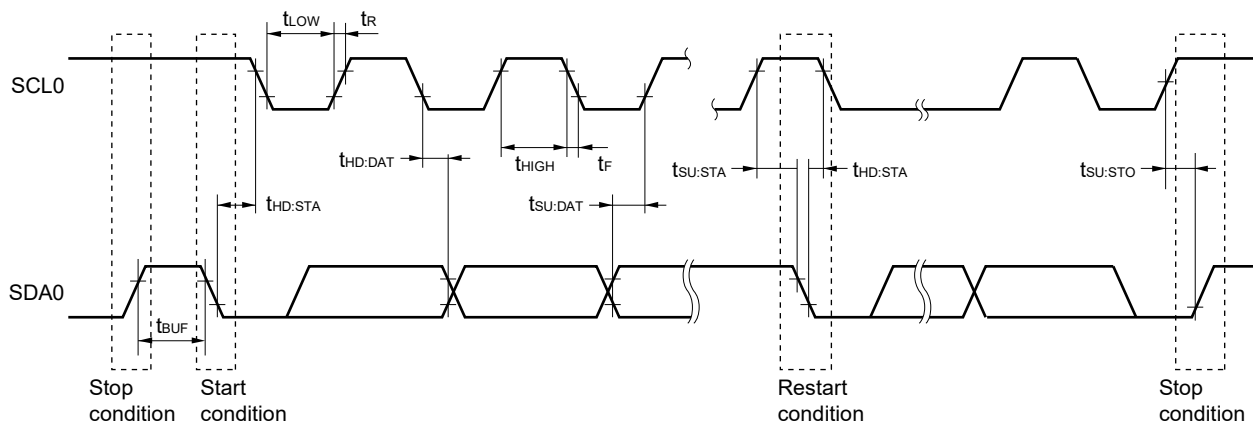
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz 2.7 V ≤ EV _{DD} ≤ 5.5 V	0	1000	-	-	-	-	-	-	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		-	-	-	-	-	-	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		-	-	-	-	-	-	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.5		-	-	-	-	-	-	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		-	-	-	-	-	-	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	50		-	-	-	-	-	-	ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0	0.45	-	-	-	-	-	-	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.26		-	-	-	-	-	-	μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD} ≤ 5.5 V	0.5		-	-	-	-	-	-	μs

- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a clock stretch state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 12-bit A/D converter characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS1} = V_{SS} = EV_{SS} = 0\text{ V}$, reference voltage (+) = AV_{REFP} , reference voltage (-) = $AV_{REFM} = 0\text{ V}$) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			–	–	12	bit
Analog capacitance	C_s			–	–	8	pF
Analog input resistance	R_s	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$		–	–	6.7	k Ω
		$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$		–	–	8.2	k Ω
		$1.6\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$		–	–	14.3	k Ω
Input capacitance ^{Note 1}	C_{in}	ANI0 to ANI5	$V_i = AV_{DD}$	–	8	–	pF
Internal reference voltage	V_{BGR}	$2.4\text{ V} \leq AV_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode		1.38	1.45	1.5	V
Frequency	ADCLK	High-speed mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	1	–	32	MHz
			$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	1	–	16	MHz
		Normal mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	1	–	24	MHz
			$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	1	–	16	MHz
			$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	1	–	8	MHz
Conversion time ^{Note 2}	t_{CONV}	High-speed mode ADCSR.ADHSC = 0 ADSSSTRn = 28 H	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$ Permissible signal source impedance max = 0.5 k Ω ADCLK = 32 MHz When the channel-dedicated sample- and-hold circuits are not in use.	2.3	–	–	μs
			$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$ Permissible signal source impedance max = 0.5 k Ω ADCLK = 32 MHz When the channel-dedicated sample- and-hold circuits are not in use. ^{Note 3}	3.3	–	–	μs
			$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$ Permissible signal source impedance max = 1.3 k Ω ADCLK = 16 MHz	4.5	–	–	μs
		Normal mode ADCSR.ADHSC = 1 ADSSSTRn = 28 H	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$ Permissible signal source impedance max = 1.1 k Ω ADCLK = 24 MHz When the channel-dedicated sample- and-hold circuits are not in use.	3.4	–	–	μs
			$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$ Permissible signal source impedance max = 1.1 k Ω ADCLK = 24 MHz When the channel-dedicated sample- and-hold circuits are not in use. ^{Note 3}	5	–	–	μs

- Notes**
- The value listed to the right is only for reference.
 - The conversion time is the sum of sampling time and comparison time. The values indicated in the table are those in the case of 40 clock cycles of ADCLK per sampling state.
 - When the channel-dedicated sample-and-hold circuits are in use, the input voltages on the ANIn ($n = 0, 1, 2$) pins must be kept within the following range.
 $0.25\text{ V} \leq ANIn \leq AV_{DD} - 0.25\text{ V}$

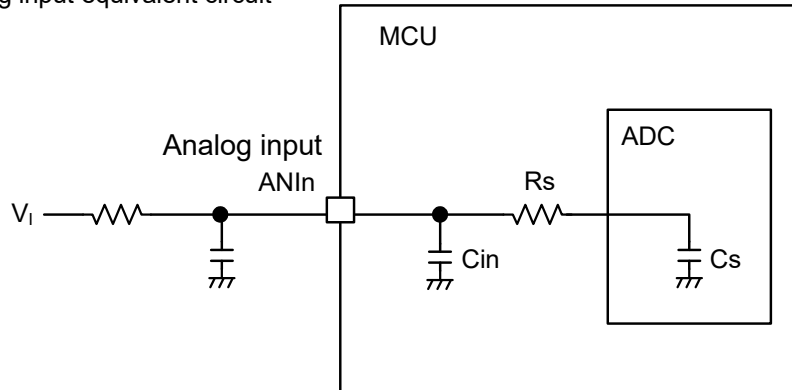
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS1} = V_{SS} = EV_{SS} = 0\text{ V}$, reference voltage (+) = AV_{REFP} , reference voltage (-) = $AV_{REFM} = 0\text{ V}$) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Conversion time ^{Note}	t_{CONV}	Normal mode	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	5.1	–	–	μs
		ADCSR.ADHSC = 1 ADSSTR _n = 28 H	Permissible signal source impedance max = 2.2 k Ω ADCLK = 16 MHz				
			$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	10.1	–	–	μs
			Permissible signal source impedance max = 5 k Ω ADCLK = 8 MHz				
Overall error	AINL	High-speed mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.25	± 5.0	LSB
		ADCSR.ADHSC = 0	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.25	± 5.0	LSB
		ADSSTR _n = 28 H					
		Normal mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.25	± 5.0	LSB
		ADCSR.ADHSC = 1	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.25	± 5.0	LSB
		ADSSTR _n = 28 H	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 3.0	± 8.0	LSB
Zero-scale error	EVS	High-speed mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.5	± 4.5	LSB
		ADCSR.ADHSC = 0	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.5	± 4.5	LSB
		ADSSTR _n = 28 H					
		Normal mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.5	± 4.5	LSB
		ADCSR.ADHSC = 1	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.5	± 4.5	LSB
		ADSSTR _n = 28 H	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1	± 7.5	LSB
Full-scale error	EFS	High-speed mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.75	± 4.5	LSB
		ADCSR.ADHSC = 0	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.75	± 4.5	LSB
		ADSSTR _n = 28 H					
		Normal mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.75	± 4.5	LSB
		ADCSR.ADHSC = 1	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 0.75	± 4.5	LSB
		ADSSTR _n = 28 H	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.5	± 7.5	LSB
DNL differential linearity error	DLE	High-speed mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	–	LSB
		ADCSR.ADHSC = 0	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	–	LSB
		ADSSTR _n = 28 H					
		Normal mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	–	LSB
		ADCSR.ADHSC = 1	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	–	LSB
		ADSSTR _n = 28 H	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	–	LSB
INL integral linearity error	ILE	High-speed mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	± 3.0	LSB
		ADCSR.ADHSC = 0	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	± 4.5	LSB
		ADSSTR _n = 28 H					
		Normal mode	$2.7\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	± 3.0	LSB
		ADCSR.ADHSC = 1	$2.4\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.0	± 3.0	LSB
		ADSSTR _n = 28 H	$1.8\text{ V} \leq AV_{REFP} \leq AV_{DD} \leq 5.5\text{ V}$	–	± 1.25	± 3.0	LSB

(Caution is listed on the next page.)

Caution The characteristics above only apply when pins other than those of the 12-bit A/D converter are not in use. Each of the overall error, offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error does not include the quantization error.

Analog input equivalent circuit



2.6.2 Voltage reference characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS1} = V_{SS} = EV_{SS} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage range	VREFAMPCNT.VREFADCG[1:0] = 0xb, AV _{DD} ≥ 1.8 V ^{Note 3}	1.41	1.5	1.59	V
	VREFAMPCNT.VREFADCG[1:0] = 10b, AV _{DD} ≥ 2.2 V ^{Note 4}	1.88	2.0	2.12	
	VREFAMPCNT.VREFADCG[1:0] = 11b, AV _{DD} ≥ 2.7 V ^{Note 5}	2.35	2.5	2.65	
Temperature coefficient for VREFOUT ^{Note 1}	1.8 V ≤ AV _{DD} = V _{DD} ≤ 5.5 V	–	50	–	ppm/°C
BGR stabilization time ^{Note 2} (after BGR is enabled)	VREFAMPCNT.BGREN = 1	–	–	150	μs
VREFAMP stabilization time ^{Note 2} (after VREFAMP is enabled)	VREFAMPCNT.VREFADGEN = 1	–	–	1500	μs
Overcurrent detection ^{Note 2}	VREFAMPCNT.OLDETEN = 1	–	20	40	mA
Load capacitance ^{Note 1}	–	0.75	1	1.25	μF

- Notes**
1. Connect capacitors as stabilization capacitance between the AV_{REFP}/VREFOUT and AV_{REFM} pins when the voltage reference (VREFADC) is in use.
 2. These values are based on simulation. They are not tested at the time of shipment.
 3. A value in the range listed to the right cannot be used as the high-potential reference voltage for the 12-bit A/D converter.
 4. When a value in the range listed to the right is in use as the high-potential reference voltage for the 12-bit A/D converter, the following conditions must be satisfied.
In normal mode: 2.2 V ≤ AV_{DD} ≤ 5.5 V and ADCLK = 1 MHz to 8 MHz
 5. When a value in the range listed to the right is in use as the high-potential reference voltage for the 12-bit A/D converter, the following conditions must be satisfied.
In normal mode: 2.7 V ≤ AV_{DD} ≤ 5.5 V and ADCLK = 1 MHz to 24 MHz
In high-speed mode: 2.7 V ≤ AV_{DD} ≤ 5.5 V and ADCLK = 1 MHz to 32 MHz

2.6.3 24-bit $\Delta\Sigma$ A/D converter characteristics

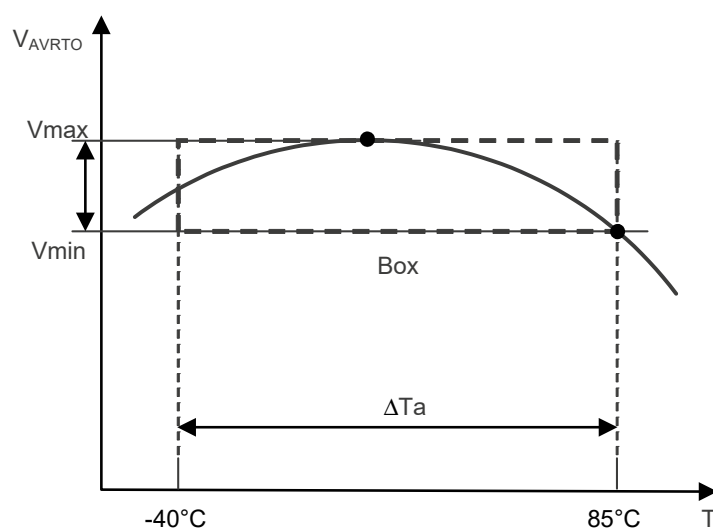
(1) Reference voltage

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS0} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{AVRTO}			0.8		V
Temperature coefficient for internal reference voltage ^{Note}	TC_{BOX}	0.47 μF capacitor connected to AREGC, AVRT, and AVCM pins		10		ppm/ $^\circ\text{C}$

Note This is as stipulated by the BOX method.

$$TC_{BOX} = \frac{1}{V_{min}} \cdot \frac{V_{max} - V_{min}}{\Delta T_a}$$



(2) Analog input

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS0} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range (differential voltage)	V _{AIN}	x1 gain	-500		500	mV
		x2 gain	-250		250	
		x4 gain	-125		125	
		x8 gain	-62.5		62.5	
		x16 gain	-31.25		31.25	
		x32 gain	-15.625		15.625	
Input gain	ainGAIN	x1 gain		1		Times
		x2 gain		2		
		x4 gain		4		
		x8 gain		8		
		x16 gain		16		
		x32 gain		32		
Input impedance	ainRIN	Differential voltage	150	360		kΩ
		Single-ended voltage	100	240		

(3) 4 kHz sampling mode

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS0} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation clock	f _{DSAD}	f _x oscillation clock, input external clock or high-speed on-chip oscillator clock is used		12		MHz
Sampling frequency	f _s			3906.25		Hz
Oversampling frequency	f _{OS}			1.5		MHz
Output data rate	T _{DATA}			256		μs
Data width	RES			24		bit
SNDR	SNDR	x1 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)		80		dB
		x16 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	69	74		
		x32 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	65	69		
Passband (low pass band)	f _{Chpf}	At -3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 00		0.607		Hz
		At -3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 01		1.214		Hz
		At -3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 10		2.429		Hz
		At -3 dB (phase in high pass filter not adjusted) Bits 7 and 6 of DSADHPFCR register (DSADCOF1, DSADCOF0) = 11		4.857		Hz
In-band ripple 1	rp1	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz	-0.01		0.01	dB
In-band ripple 2	rp2	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz	-0.1		0.1	
In-band ripple 3	rp3	45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz	-0.1		0.1	
Passband (high pass band)	f _{Cipf}	-3 dB		1672		Hz
Stopband (high pass band)	f _{att}	-80 dB		2545		Hz
Out-band attenuation	ATT1	f _s	-80			dB
	ATT2	2 f _s	-80			dB

(4) 2 kHz sampling mode

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS0} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation clock	f _{DSAD}	f _x oscillation clock, input external clock or high-speed on-chip oscillator clock is used		12		MHz
Sampling frequency	f _s			1953.125		Hz
Oversampling frequency	f _{OS}			0.75		MHz
Output data rate	T _{DATA}			512		μs
Data width	RES			24		bit
SNDR	SNDR	x1 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)		80		dB
		x16 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	69	74		
		x32 gain High-speed system clock is selected as operating clock of 24-bit ΔΣ A/D converter (bit 0 of PCKC register (DSADCK) = 1)	65	69		
Passband (low pass band)	f _{Chpf}	At -3 dB (phase in high pass filter not adjusted)		0.303		Hz
In-band ripple 1	rp1	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz	-0.01		0.01	dB
In-band ripple 2	rp2	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz	-0.1		0.1	
In-band ripple 3	rp3	45 Hz to 660 Hz @50 Hz 54 Hz to 550 Hz @60 Hz	-0.1		0.1	
Passband (high pass band)	f _{Cipf}	-3 dB		836		Hz
Stopband (high pass band)	f _{att}	-80 dB		1273		Hz
Out-band attenuation	ATT1	f _s	-80			dB
	ATT2	2 f _s	-80			dB

2.6.4 Temperature sensor 2 characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS1} = V_{SS} = EV_{SS} = 0 V, HS (high-speed main) mode)

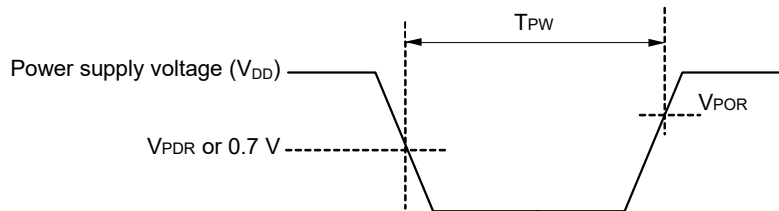
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor 2 output voltage	V _{OUT}			0.67		V
Temperature coefficient	F _{VTMPS2}	Temperature sensor that depends on the temperature	-11.7	-10.7	-9.7	mV/°C
Operation stabilization wait time	t _{TMPON}	Operable		15	50	μs
	t _{TMPCHG}	Switching mode		5	15	μs
Sampling time	-		5			μs

2.6.5 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	The power supply voltage is rising. ^{Note 1}	1.47	1.51	1.55	V
	V_{PDR}	The power supply voltage is falling. ^{Note 2}	1.46	1.50	1.54	V
Minimum pulse width ^{Note 3}	T_{PW}		300			μs

- Notes 1.** Be sure to maintain the reset state until the power supply voltage rises over the minimum V_{DD} value in the operating voltage range specified in **2.4 AC Characteristics**, by using the voltage detector or external reset pin.
- 2.** If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in **2.4 AC Characteristics**.
- 3.** This is the minimum time required for a power-on reset (POR) when V_{DD} has fallen below V_{PDR} . This is also the minimum time required for a POR following V_{DD} falling below 0.7 V to when V_{DD} exceeds V_{POR} while the chip is in STOP mode or the main system clock is stopped by the settings of bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.6 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, V_{PDR} ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVD0}	The power supply voltage is rising.	3.98	4.06	4.24	V
		The power supply voltage is falling.	3.90	3.98	4.16	V
	V _{LVD1}	The power supply voltage is rising.	3.68	3.75	3.92	V
		The power supply voltage is falling.	3.60	3.67	3.84	V
	V _{LVD2}	The power supply voltage is rising.	3.07	3.13	3.29	V
		The power supply voltage is falling.	3.00	3.06	3.22	V
	V _{LVD3}	The power supply voltage is rising.	2.96	3.02	3.18	V
		The power supply voltage is falling.	2.90	2.96	3.12	V
	V _{LVD4}	The power supply voltage is rising.	2.86	2.92	3.07	V
		The power supply voltage is falling.	2.80	2.86	3.01	V
	V _{LVD5}	The power supply voltage is rising.	2.76	2.81	2.97	V
		The power supply voltage is falling.	2.70	2.75	2.91	V
	V _{LVD6}	The power supply voltage is rising.	2.66	2.71	2.86	V
		The power supply voltage is falling.	2.60	2.65	2.80	V
	V _{LVD7}	The power supply voltage is rising.	2.56	2.61	2.76	V
		The power supply voltage is falling.	2.50	2.55	2.70	V
	V _{LVD8}	The power supply voltage is rising.	2.45	2.50	2.65	V
		The power supply voltage is falling.	2.40	2.45	2.60	V
	V _{LVD9}	The power supply voltage is rising.	2.05	2.09	2.23	V
		The power supply voltage is falling.	2.00	2.04	2.18	V
	V _{LVD10}	The power supply voltage is rising.	1.94	1.98	2.12	V
		The power supply voltage is falling.	1.90	1.94	2.08	V
	V _{LVD11}	The power supply voltage is rising.	1.84	1.88	2.01	V
		The power supply voltage is falling.	1.80	1.84	1.97	V
V _{LVD12}	The power supply voltage is rising.	1.74	1.77	1.81	V	
	The power supply voltage is falling.	1.70	1.73	1.77	V	
V _{LVD13}	The power supply voltage is rising.	1.64	1.67	1.70	V	
	The power supply voltage is falling.	1.60	1.63	1.66	V	
Minimum pulse width	t _{LW}		300			μs
Detection delay time					300	μs

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5$ V, $AV_{SS} = V_{SS} = EV_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Detection voltage	V_{LVD13}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0$, falling reset voltage	1.60	1.63	1.66	V	
	V_{LVD12}	$LVIS1, LVIS0 = 1, 0$ (+0.1 V)	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.91	V
	V_{LVD11}	$LVIS1, LVIS0 = 0, 1$ (+0.2 V)	Rising release reset voltage	1.84	1.88	1.87	V
			Falling interrupt voltage	1.80	1.84	2.97	V
	V_{LVD4}	$LVIS1, LVIS0 = 0, 0$ (+1.2 V)	Rising release reset voltage	2.86	2.92	2.91	V
			Falling interrupt voltage	2.80	2.86	3.22	V
	V_{LVD11}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1$, falling reset voltage	1.80	1.84	1.97	V	
	V_{LVD10}	$LVIS1, LVIS0 = 1, 0$ (+0.1 V)	Rising release reset voltage	1.94	1.98	2.12	V
			Falling interrupt voltage	1.90	1.94	2.08	V
	V_{LVD9}	$LVIS1, LVIS0 = 0, 1$ (+0.2 V)	Rising release reset voltage	2.05	2.09	2.23	V
			Falling interrupt voltage	2.00	2.04	2.18	V
	V_{LVD2}	$LVIS1, LVIS0 = 0, 0$ (+1.2 V)	Rising release reset voltage	3.07	3.13	3.29	V
			Falling interrupt voltage	3.00	3.06	3.22	V
	V_{LVD8}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0$, falling reset voltage	2.40	2.45	2.60	V	
	V_{LVD7}	$LVIS1, LVIS0 = 1, 0$	Rising release reset voltage	2.56	2.61	2.76	V
			Falling interrupt voltage	2.50	2.55	2.70	V
	V_{LVD6}	$LVIS1, LVIS0 = 0, 1$	Rising release reset voltage	2.66	2.71	2.86	V
			Falling interrupt voltage	2.60	2.65	2.80	V
	V_{LVD1}	$LVIS1, LVIS0 = 0, 0$	Rising release reset voltage	3.68	3.75	3.92	V
			Falling interrupt voltage	3.60	3.67	3.84	V
	V_{LVD5}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1$, falling reset voltage	2.70	2.75	2.91	V	
	V_{LVD4}	$LVIS1, LVIS0 = 1, 0$	Rising release reset voltage	2.86	2.92	3.07	V
			Falling interrupt voltage	2.80	2.86	3.01	V
V_{LVD3}	$LVIS1, LVIS0 = 0, 1$	Rising release reset voltage	2.96	3.02	3.18	V	
		Falling interrupt voltage	2.90	2.96	3.12	V	
V_{LVD0}	$LVIS1, LVIS0 = 0, 0$	Rising release reset voltage	3.98	4.06	4.24	V	
		Falling interrupt voltage	3.90	3.98	4.16	V	

2.6.7 Power supply voltage rising slope characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DDR} SV_{RTCR}				54	V/ms

Cautions 1. Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2. When the voltages for V_{DD} and AV_{DD} differ and they rise at different rates, if AV_{DD} is lower than 0.8 V at the time of the release from the internal reset state by the power-on reset (POR) circuit, the chip may not start normally.

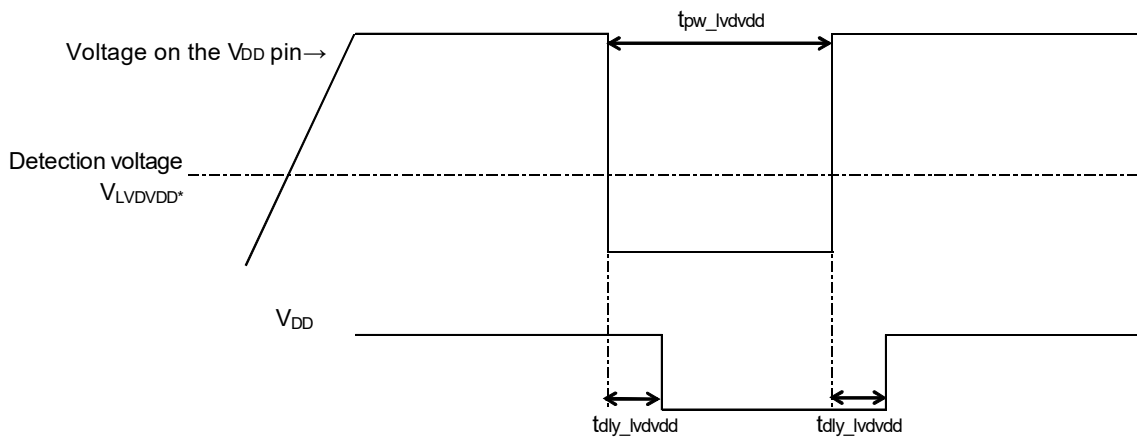
In such cases, apply either of the following countermeasures.

- Hold $AV_{DD} \geq 0.8$ V until $V_{DD} \geq 1.47$ V.
- Hold the RESET pin low until $V_{DD} \geq 1.47$ V and $AV_{DD} \geq 0.8$ V.

2.6.8 V_{DD} pin voltage detection characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

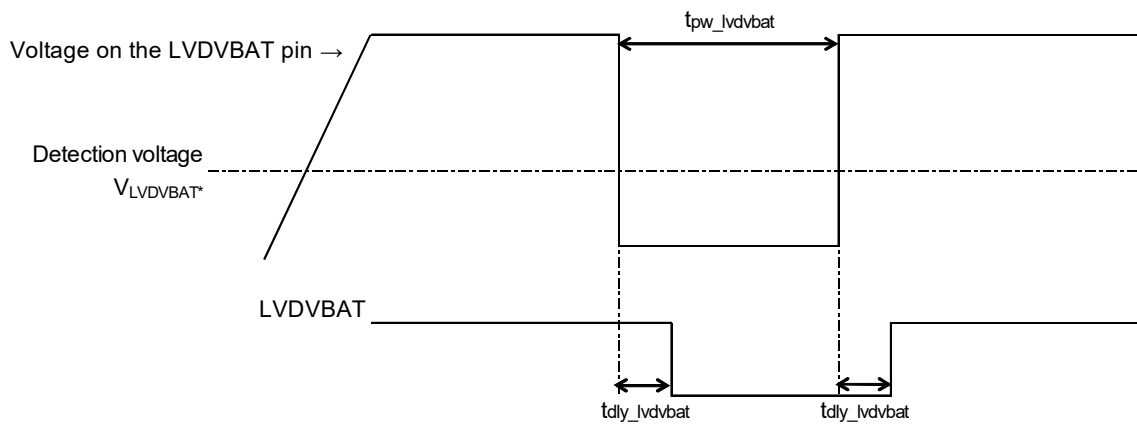
Parameter	Symbol	LVDVDD[2:0]	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVDVDD0}	000	Rising	2.40	2.53	2.65	V
			Falling	2.33	2.46	2.58	V
	V _{LVDVDD1}	001	Rising	2.60	2.74	2.86	V
			Falling	2.53	2.67	2.79	V
	V _{LVDVDD2}	010	Rising	2.79	2.94	3.07	V
			Falling	2.73	2.87	2.99	V
	V _{LVDVDD3}	011	Rising	3.00	3.15	3.28	V
			Falling	2.93	3.08	3.21	V
V _{LVDVDD4}	100	Rising	3.30	3.46	3.60	V	
		Falling	3.23	3.39	3.52	V	
V _{LVDVDD5}	101	Rising	3.59	3.77	3.91	V	
		Falling	3.53	3.70	3.84	V	
Minimum pulse width	t _{pw_lvdvdd}	—	—	300			μs
Detection delay time	t _{dly_lvdvdd}	—	—			300	μs



2.6.9 LVDVBAT pin voltage detection characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

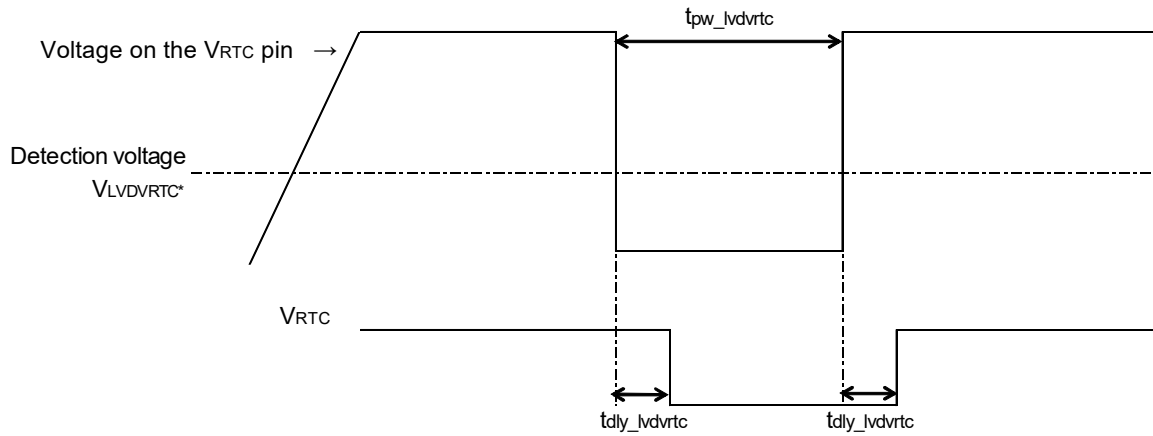
Parameter	Symbol	LVDVBAT[2:0]	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVDVBAT0}	000	Rising	2.11	2.23	2.34	V
			Falling	2.06	2.17	2.28	V
	V _{LVDVBAT1}	001	Rising	2.31	2.43	2.54	V
			Falling	2.25	2.37	2.48	V
	V _{LVDVBAT2}	010	Rising	2.51	2.63	2.74	V
			Falling	2.45	2.57	2.68	V
	V _{LVDVBAT3}	011	Rising	2.60	2.73	2.84	V
			Falling	2.54	2.67	2.78	V
	V _{LVDVBAT4}	100	Rising	2.69	2.83	2.95	V
			Falling	2.64	2.77	2.89	V
	V _{LVDVBAT5}	101	Rising	2.79	2.93	3.05	V
			Falling	2.73	2.87	2.99	V
V _{LVDVBAT6}	110	Rising	2.99	3.13	3.26	V	
		Falling	2.93	3.07	3.19	V	
Minimum pulse width	t _{pw_lvdvbat}	–	–	300			μs
Detection delay time	t _{dly_lvdvbat}	–	–			300	μs
Pin resistor	r _{in_lvdvbat}	–	LVDVBATEN = 1		109		MΩ



2.6.10 V_{RTC} pin voltage detection characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

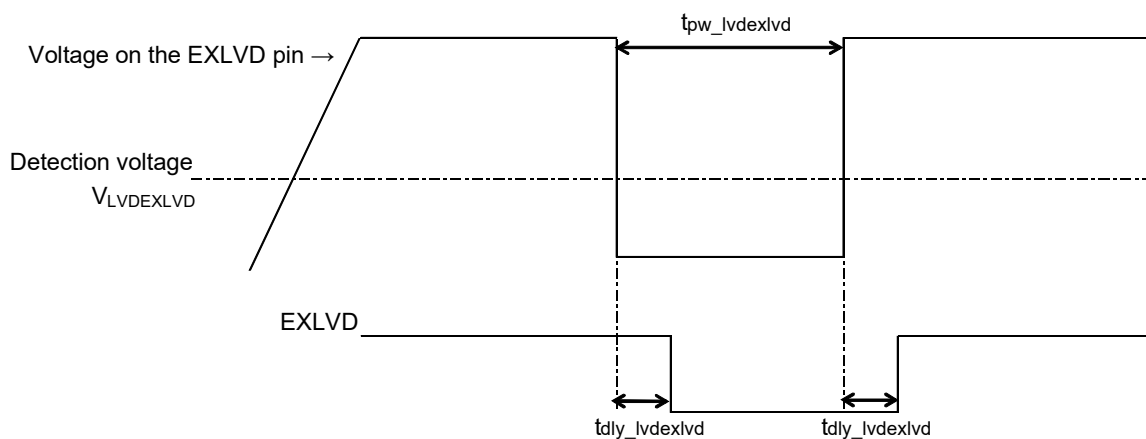
Parameter	Symbol	LVDVRTC[1:0]	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVDVRTC0}	00	Rising	2.16	2.22	2.28	V
			Falling	2.10	2.16	2.22	V
	V _{LVDVRTC1}	01	Rising	2.36	2.43	2.50	V
			Falling	2.30	2.37	2.44	V
	V _{LVDVRTC2}	10	Rising	2.56	2.63	2.70	V
			Falling	2.50	2.57	2.64	V
	V _{LVDVRTC3}	11	Rising	2.76	2.84	2.92	V
			Falling	2.70	2.78	2.86	V
Minimum pulse width	t _{pw_lvdvrtc}	—	—	300			μs
Detection delay time	t _{dly_lvdvrtc}	—	—			300	μs



2.6.11 EXLVD pin voltage detection

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{LVDEXLVD}$	Rising	1.25	1.33	1.41	V
		Falling	1.20	1.28	1.36	V
Minimum pulse width	$t_{pw_lvdexlvd}$	–	300			μs
Detection delay time	$t_{dly_lvdexlvd}$	–			300	μs
Pin resistor	r_{in_extlvd}	LVDEXLVDEN = 1		34		$\text{M}\Omega$



2.7 LCD Characteristics

2.7.1 Resistance division method

(1) Static display mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5 \text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5 \text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

($T_A = -40$ to $+85^\circ\text{C}$, $V_{L4} (\text{MIN.}) \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5 \text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0 \text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(TA = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} = EV_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	V _{L1}	C1 to C4 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
VLCD = 12H	1.60	1.70	1.78	V			
		VLCD = 13H Note 4	1.65	1.75	1.83	V	
Doubler output voltage	V _{L2}	C1 to C4 ^{Note 1} = 0.47 μF	2 V _{L1} -0.10	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L4}	C1 to C4 ^{Note 1} = 0.47 μF	3 V _{L1} -0.15	3 V _{L1}	3 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{VWAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{VWAIT2}	C1 to C4 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 μF±30%

- This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).
- This setting is only available when V_{DD} ≥ V_{L1}.

(2) 1/4 bias method**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
LCD output voltage variation range	V _{L1}	C1 to C5 ^{Note 1} = 0.47 μF	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V _{L2}	C1 to C5 ^{Note 1} = 0.47 μF	2 V _{L1} -0.08	2 V _{L1}	2 V _{L1}	V	
Tripler output voltage	V _{L3}	C1 to C5 ^{Note 1} = 0.47 μF	3 V _{L1} -0.12	3 V _{L1}	3 V _{L1}	V	
Quadruply output voltage	V _{L4}	C1 to C5 ^{Note 1} = 0.47 μF	4 V _{L1} -0.16	4 V _{L1}	4 V _{L1}	V	
Reference voltage setup time ^{Note 2}	t _{WAIT1}		5			ms	
Voltage boost wait time ^{Note 3}	t _{WAIT2}	C1 to C5 ^{Note 1} = 0.47 μF	500			ms	

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L3} and GND

C5: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = C5 = 0.47 $\mu\text{F} \pm 30\%$

- This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).
- This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.7.3 Capacitor split method

(1) 1/3 bias method

($T_A = -40$ to $+85^\circ\text{C}$, $2.2\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	$C1$ to $C4 = 0.47\ \mu\text{F}$ ^{Note 2}		V_{DD}		V
V_{L2} voltage	V_{L2}	$C1$ to $C4 = 0.47\ \mu\text{F}$ ^{Note 2}	$2/3 V_{L4} - 0.1$	$2/3 V_{L4}$	$2/3 V_{L4} + 0.1$	V
V_{L1} voltage	V_{L1}	$C1$ to $C4 = 0.47\ \mu\text{F}$ ^{Note 2}	$1/3 V_{L4} - 0.1$	$1/3 V_{L4}$	$1/3 V_{L4} + 0.1$	V
Capacitor split wait time ^{Note 1}	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started ($V_{LCON} = 1$) until display is enabled ($LCDON = 1$).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

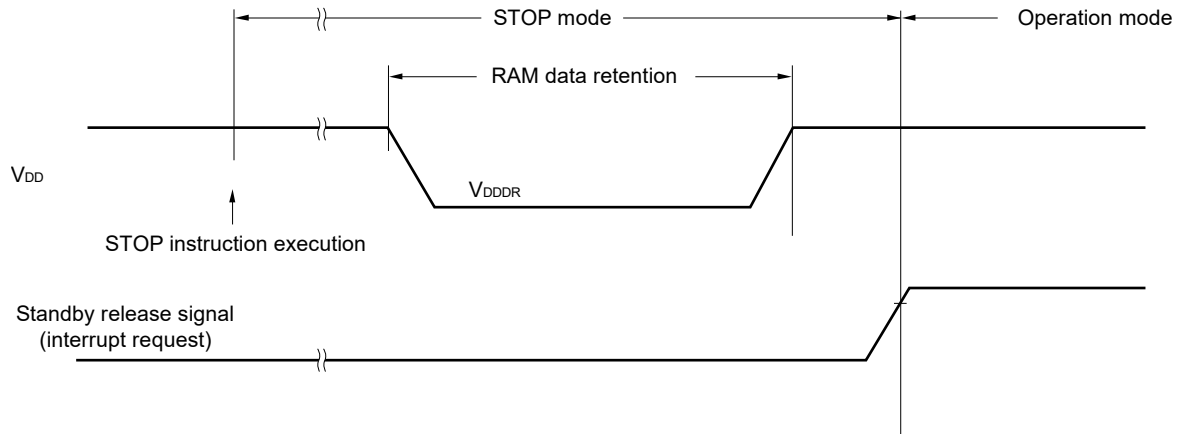
$C1 = C2 = C3 = C4 = 0.47\ \mu\text{F} \pm 30\%$

2.8 RAM Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.9 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$ ^{Note 4}, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ^{Note 4}	1		32	MHz
Number of code flash rewrites ^{Notes 1, 2, 3}	C_{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites ^{Notes 1, 2, 3}		Retained for 1 year $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library
 3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.
 4. Execute bank programming while the following conditions are satisfied.
 - (1) $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$
 - (2) Operation is in HS (high-speed main) mode or LS (low-speed main) mode.
 Bank programming is prohibited in LP (low-power main) mode and LV (low-voltage main) mode.
 Self-programming is possible when $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$.

2.10 Dedicated Flash Memory Programmer Communication (UART)

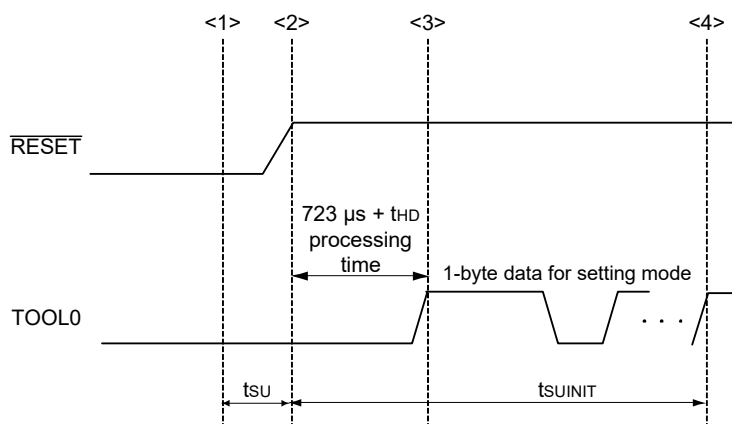
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.11 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq AV_{DD} = V_{DD} = EV_{DD} \leq 5.5\text{ V}$, $AV_{SS} = V_{SS} = EV_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{SUIINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark $t_{SUIINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level.

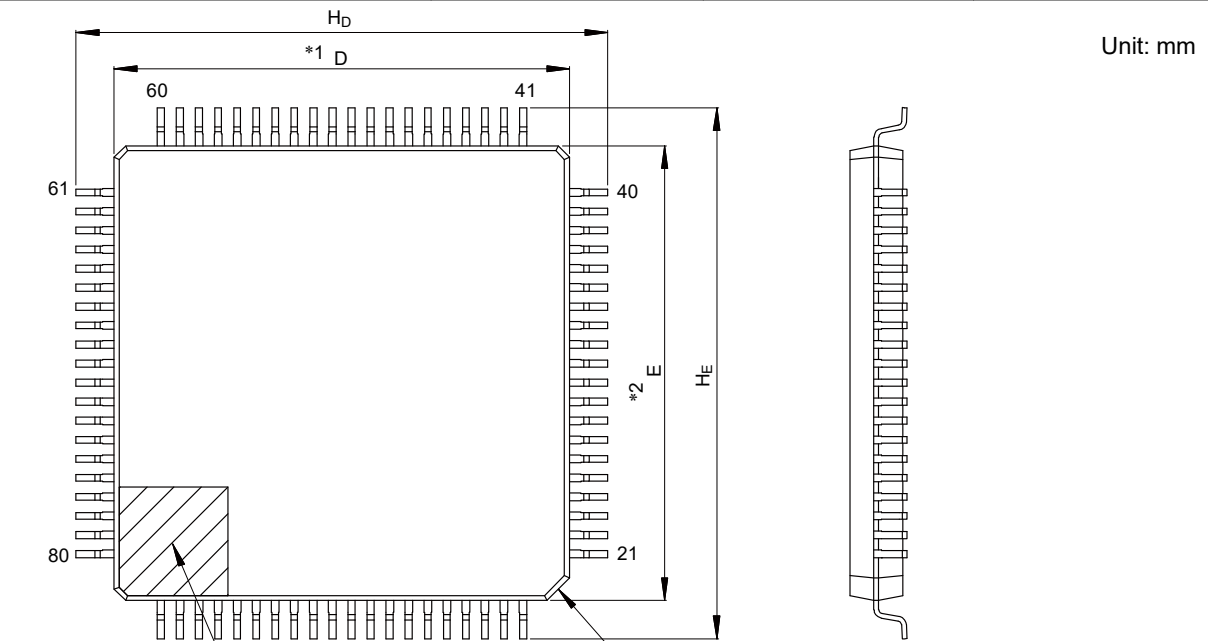
t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3. PACKAGE DRAWINGS

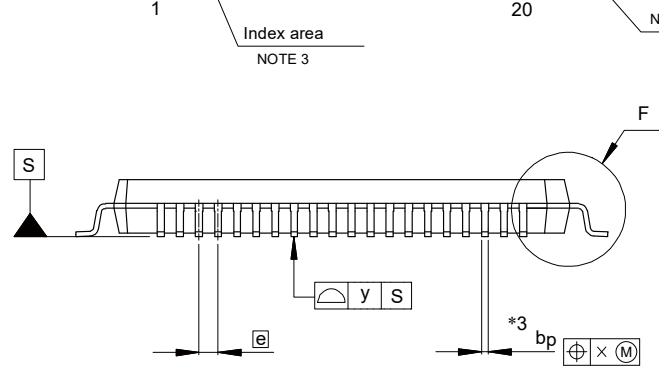
3.1 80-pin Product

R5F10NMLDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

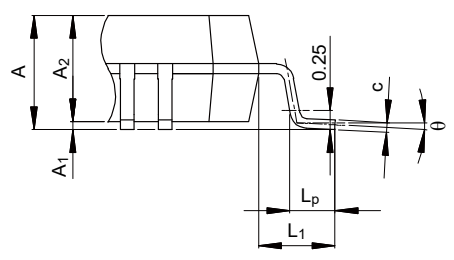


Unit: mm



- NOTE)
1. DIMENSIONS "**1" AND "**2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION "**3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

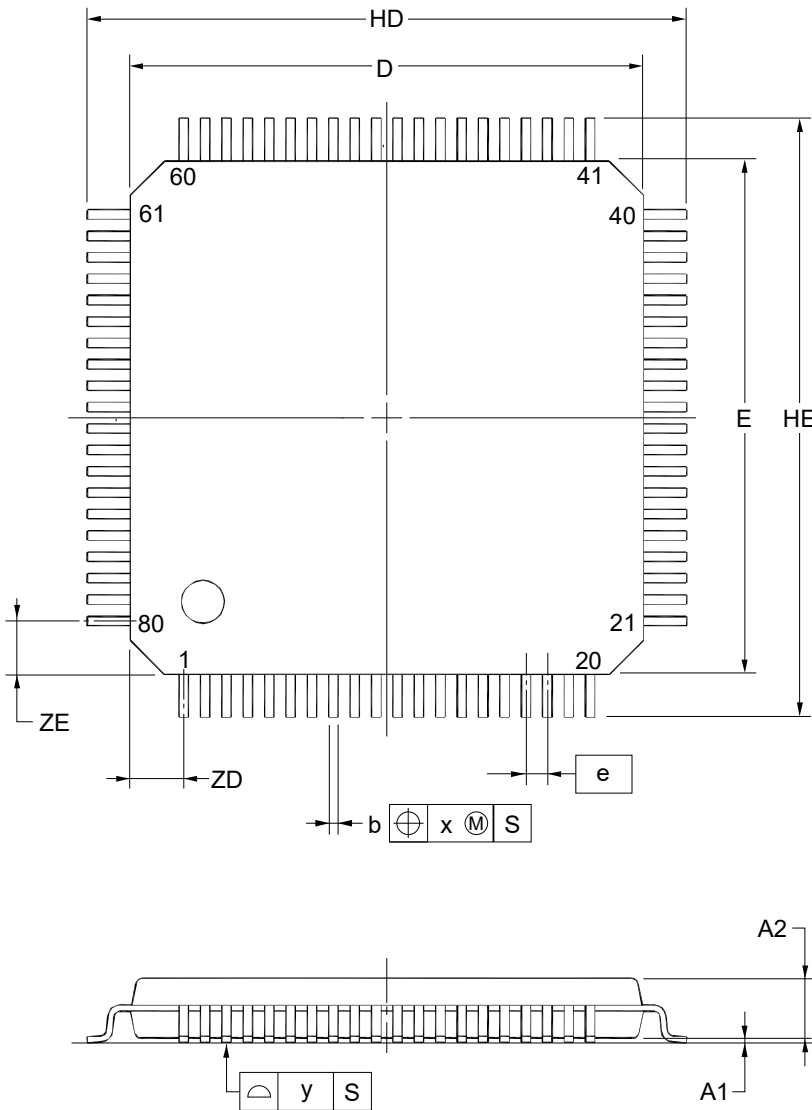
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A ₂	—	1.4	—
H _D	13.8	14.0	14.2
H _E	13.8	14.0	14.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
[e]	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—



Detail F

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU	0.53



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	0.145 ^{+0.055} _{-0.045}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

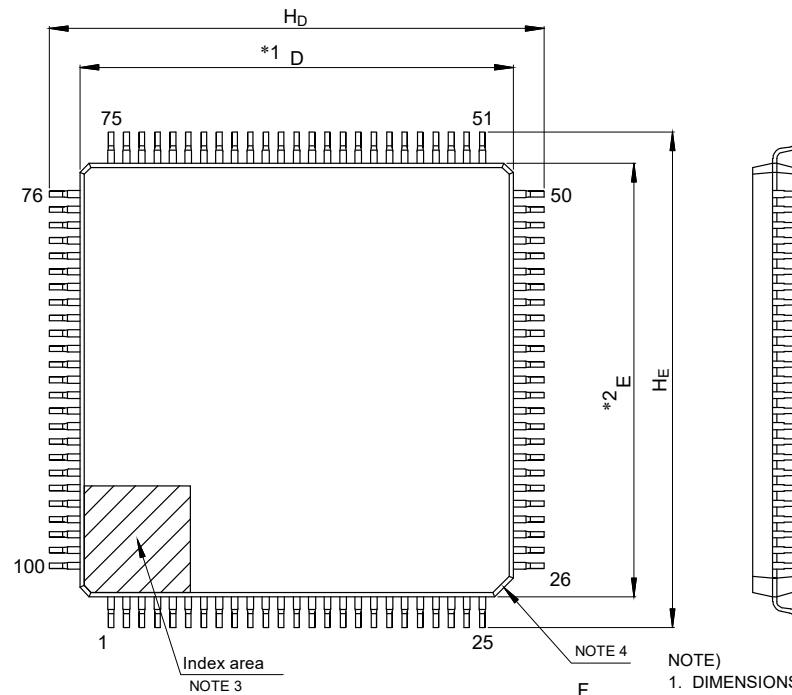
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

3.2 100-pin Product

R5F10NPLDFB

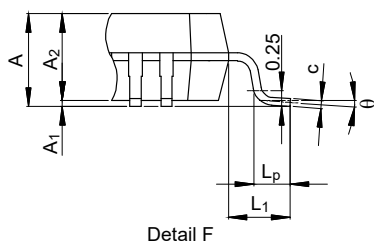
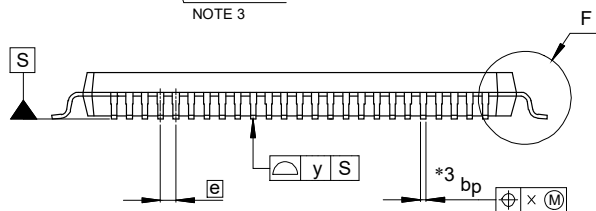
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)

1. DIMENSIONS "**1" AND "**2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "**3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

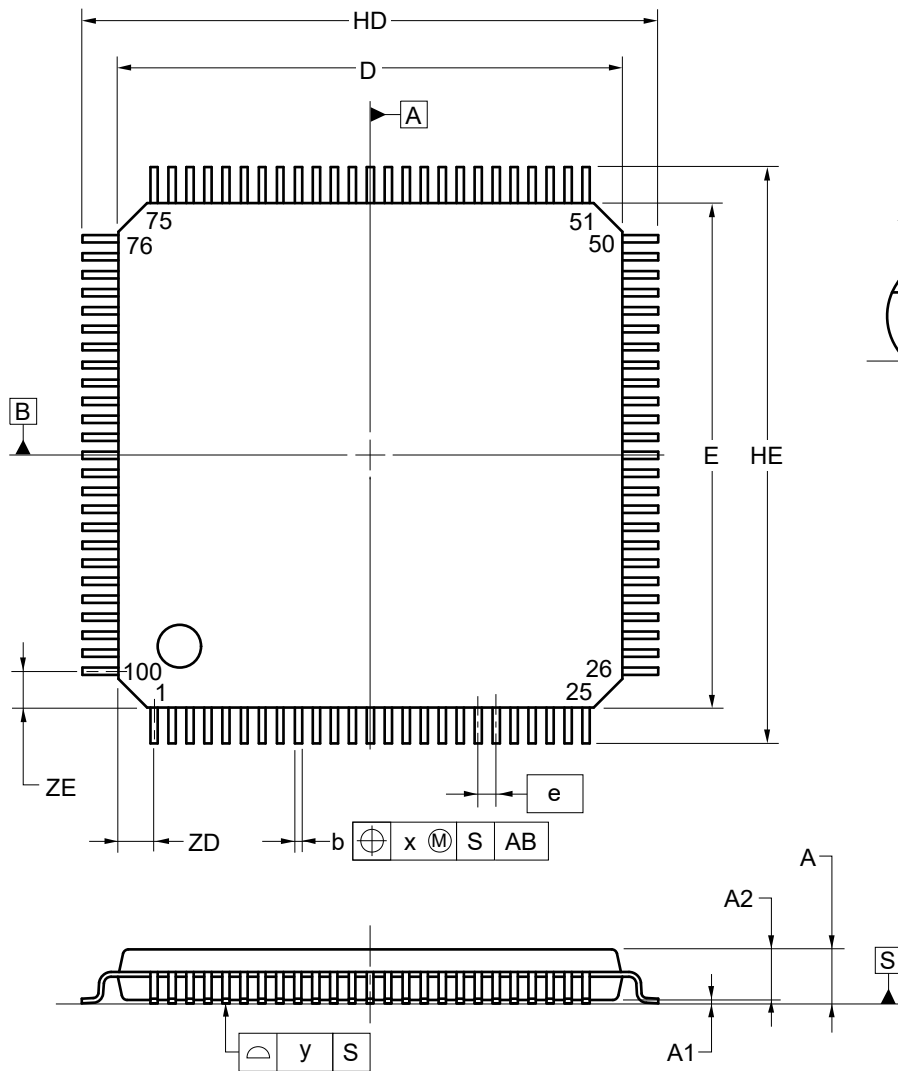


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
[e]	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

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<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14X14-0.50	PLQP0100KE-A	P100GC-50-GBR	0.69



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	0.145 ^{+0.055} _{-0.045}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

Revision History	RL78/I1C (512 KB) Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 25, 2020	-	First edition issued
1.01	Nov 30, 2022	Throughout	The module name for CSI was changed to simplified SPI.
			“Wait” was modified to “clock stretch”
1.10	Jul 20, 2023	P28	Modification of Note 1 and 4 in 2.3.2 Supply current characteristics
		P29	Modification of Note 9 to Note 5 in 2.3.2 Supply current characteristics
		P30	Modification of Note 5 to Note 6 in 2.3.2 Supply current characteristics
			Deletion of Note 6 in 2.3.2 Supply current characteristics
P31	Modification of Note 1, 5 and 6 in 2.3.2 Supply current characteristics		
1.11	Mar 22, 2024	p.4	Modification of Figure 1-1. Part Number, Memory Size, and Package of RL78/I1C (512 KB)
		p.4	Modification of Table 1-1. List of Ordering Part Numbers
		p.5	Addition of Caution 3 in 1.3.1 80-pin product
		p.6	Addition of Caution 5 in 1.3.2 100-pin product
		p.22	Addition of description and note in the table of 2.3.1 Pin characteristics
1.12	May 29, 2026	p.90	Addition of package drawing in 3.1 80-pin Product (PLQP0080KE-A)
		p.92	Addition of package drawing in 3.2 100-pin Product (PLQP0100KE-A)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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