

RMLV1616A-U Series

16Mbit LPSRAM (1M word × 16bit / 2M word × 8bit)

R10DS0314EJ0100

Rev.1.00

2022.12.05

Description

The RMLV1616A-U Series is a family of 16-Mbit asynchronous SRAMs organized 1,048,576-word × 16-bit. The RMLV1616A-U Series has realized higher soft error immunity compared to typical SRAMs with on-chip ECC, archived by Renesas's unique Advanced LPSRAM technologies. Therefore, it is suitable for battery backup systems. It is offered in 48pin TSOP (I) or 48-ball fine pitch ball grid array.

Features

- Ultra-low standby current consumption:
 - ~ 25°C: 0.4μA (typ.) / 3μA (max.)
 - ~ 85°C: 4.4μA (typ.) / 8μA (max.)
- High speed access time: 45ns / 55ns (max.)
- Higher soft error immunity (< 0.04 FIT/Mb)^{*1} compared to typical SRAMs with on-chip ECC
- Single 3V supply: 2.7V to 3.6V
- Organized 1,048,576-word × 16-bit
(48pin TSOP (I) also configurable as 2,097,152-word × 8bit)
- Easy memory expansion by CS1# and CS2
- No clocks, No refresh
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation
- Available in Pb-free and RoHS applicable package

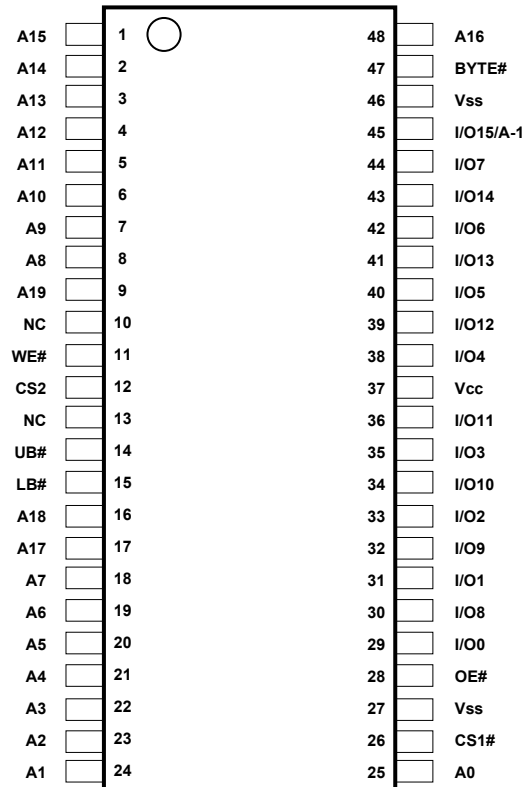
Part Name Information

Part Name	Access time	Temperature Range	Package
RMLV1616AGSA-4U2	45 ns	-40 ~ +85°C	12mm x 20mm 48pin plastic TSOP (I) (JEITA Package Code: P-TSOP(1)48-12×18.4-0.50)
RMLV1616AGSA-5U2	55 ns		
RMLV1616AGBG-4U2	45 ns		48-ball FBGA with 0.75mm ball pitch (JEITA Package Code: P-TFBGA48-7.5x8.5-0.75)
RMLV1616AGBG-5U2	55 ns		

Note 1. Based on an accelerated test that complies with JEDEC standard JESD89A. Contact us for details.

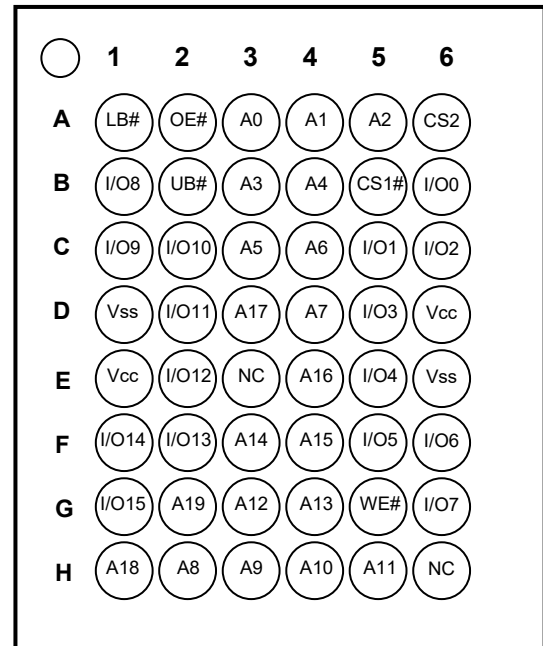
Pin Arrangement

48pin TSOP (I)



(Top view)

48-ball FBGA



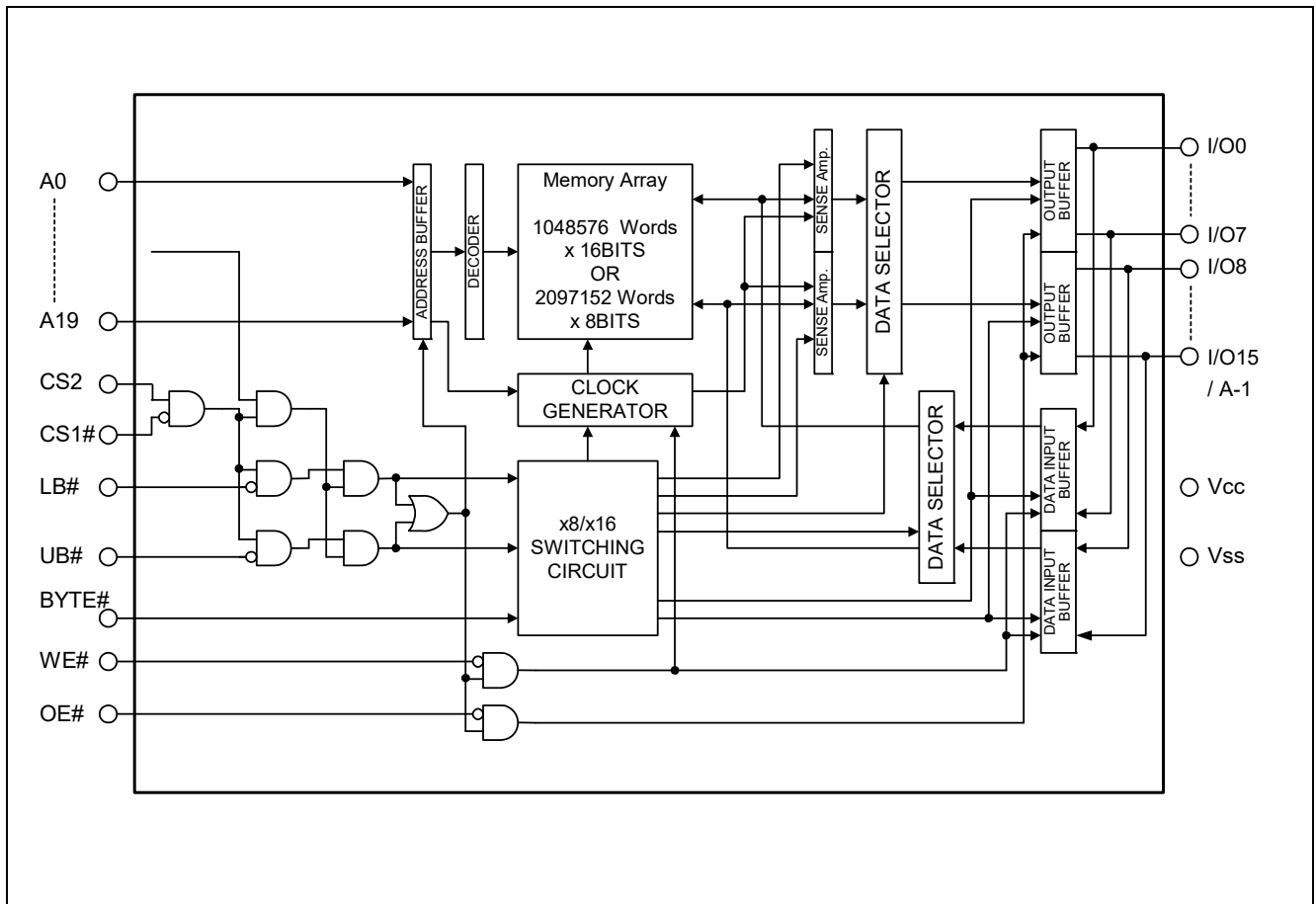
(Top view)

Pin Description

Pin name	Function
A0 to A19	Address input (word mode)
A-1 to A19	Address input (byte mode)
I/O0 to I/O15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte enable
V _{CC}	Power supply
V _{SS}	Ground
NC ²	No connection

Note 2. NC pins are not connected internally to the silicon die.

Block Diagram



Note 3. BYTE# pin applies only to 48pin TSOP (I).

Operation Table

Byte mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0~7	I/O8~14	I/O15	Operation
H	X	X	X	X	X	L	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	L	High-Z	High-Z	High-Z	Stand-by
L	H	H	L	X	X	L	Dout	High-Z	A-1	Read
L	H	L	X	X	X	L	Din	High-Z	A-1	Write
L	H	H	H	X	X	L	High-Z	High-Z	A-1	Output disable

Note 4. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

5. BYTE# pin applies only to 48pin TSOP (I).
48-ball FBGA type equals BYTE#=H mode (Word mode).

Word mode

CS1#	CS2	WE#	OE#	UB#	LB#	BYTE#	I/O0~7	I/O8~14	I/O15	Operation
H	X	X	X	X	X	H	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	H	High-Z	High-Z	High-Z	Stand-by
X	X	X	X	H	H	H	High-Z	High-Z	High-Z	Stand-by
L	H	H	L	L	L	H	Dout	Dout	Dout	Read
L	H	H	L	H	L	H	Dout	High-Z	High-Z	Lower byte read
L	H	H	L	L	H	H	High-Z	Dout	Dout	Upper byte read
L	H	L	X	L	L	H	Din	Din	Din	Write
L	H	L	X	H	L	H	Din	High-Z	High-Z	Lower byte write
L	H	L	X	L	H	H	High-Z	Din	Din	Upper byte write
L	H	H	H	L	L	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	H	L	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable

Note 6. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

7. BYTE# pin applies only to 48pin TSOP (I).
48-ball FBGA type equals BYTE#=H mode (Word mode).

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5 ⁸ to $V_{CC}+0.3$ ⁹	V
Power dissipation	P_T	0.7	W
Operation temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Note 8. -2.0V for pulse ≤ 30 ns (full width at half maximum)

9. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	$V_{CC}+0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	10
Ambient temperature range	T_a	-40	—	+85	°C	

Note 10. -2.0V for pulse ≤ 30 ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions*11	
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}	
Output leakage current	I _{LO}	—	—	1	μA	CS1# = V _{IH} or CS2 = V _{IL} or OE# = V _{IH} or WE# = V _{IL} or LB# = UB# = V _{IH} , V _{I/O} = V _{SS} to V _{CC}	
Average operating current	I _{CC1}	—	27*12	35	mA	Cycle = 45ns, duty =100%, I _{I/O} = 0mA, CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL}	
		—	23*12	30	mA	Cycle = 55ns, duty =100%, I _{I/O} = 0mA, CS1# = V _{IL} , CS2 = V _{IH} , Others = V _{IH} /V _{IL}	
	I _{CC2}	—	1.6*12	4	mA	Cycle = 1μs, duty =100%, I _{I/O} = 0mA, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V, V _{IH} ≥ V _{CC} -0.2V, V _{IL} ≤ 0.2V	
Standby current	I _{SB}	—	0.1*12	0.3	mA	CS2 = V _{IL} , Others = V _{SS} to V _{CC}	
Standby current	I _{SB1}	—	0.4*12	3	μA	~+25°C	V _{in} = V _{SS} to V _{CC} , (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V
		—	0.6*13	5	μA	~+40°C	
		—	2.2*14	6	μA	~+70°C	
		—	4.4*15	8	μA	~+85°C	
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1mA	
	V _{OH2}	V _{CC} - 0.2	—	—	V	I _{OH} = -0.1mA	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2mA	
	V _{OL2}	—	—	0.2	V	I _{OL} = 0.1mA	

Note 11. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ or BYTE# $\leq 0.2V$

12. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=25^\circ C$), and not 100% tested.

13. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=40^\circ C$), and not 100% tested.

14. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=70^\circ C$), and not 100% tested.

15. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=85^\circ C$), and not 100% tested.

Capacitance

($T_a = 25^\circ C$, $f = 1MHz$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	—	—	8	pF	$V_{in} = 0V$	16
Input / output capacitance	C I/O	—	—	10	pF	$V_{I/O} = 0V$	16

Note 16. This parameter is sampled and not 100% tested.

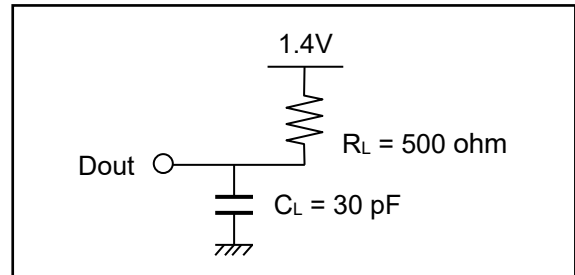
Thermal Resistance and Thermal Characterization Parameter

Parameter	Symbol	48pin TSOP (I)	48-ball FBGA	Unit	Note
Thermal resistance, junction to ambient	Θ_{ja}	70.3	37.6	$^\circ C/W$	Reference value Air flow = 0 m/s (still air)
Thermal resistance, junction to case	Θ_{jc}	8.6	10.4	$^\circ C/W$	
Thermal characterization parameter, package top surface to junction	Ψ_{jt}	0.20	0.30	$^\circ C/W$	

AC Characteristics

Test Conditions ($V_{CC} = 2.7V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels: $V_{IL} = 0.4V$, $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	-4U2		-5U2		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	45	—	55	—	ns	
Address access time	t_{AA}	—	45	—	55	ns	
Chip select access time	t_{ACS1}	—	45	—	45	ns	
	t_{ACS2}	—	45	—	45	ns	
Output enable to output valid	t_{OE}	—	22	—	22	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	—	45	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	18,19
	t_{CLZ2}	10	—	10	—	ns	18,19
LB#, UB# enable to low-Z	t_{BLZ}	5	—	5	—	ns	18,19
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	18,19
Chip deselect to output in high-Z	t_{CHZ1}	0	18	0	18	ns	17,18,19
	t_{CHZ2}	0	18	0	18	ns	17,18,19
LB#, UB# disable to high-Z	t_{BHZ}	0	15	0	18	ns	17,18,19
Output disable to output in high-Z	t_{OHZ}	0	15	0	18	ns	17,18,19

Write Cycle

Parameter	Symbol	-4U2		-5U2		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	45	—	55	—	ns	
Address valid to end of write	t_{AW}	35	—	35	—	ns	
Chip selection to end of write	t_{CW}	35	—	35	—	ns	21
Write pulse width	t_{WP}	35	—	35	—	ns	20
LB#,UB# valid to end of write	t_{BW}	35	—	35	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	22
Write recovery time	t_{WR}	0	—	0	—	ns	23
Data to write time overlap	t_{DW}	25	—	25	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	18
Output disable to output in high-Z	t_{OHZ}	0	15	0	18	ns	17,18
Write to output in high-Z	t_{WHZ}	0	15	0	18	ns	17,18

Note 17. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

18. This parameter is sampled and not 100% tested.

19. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

20. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.

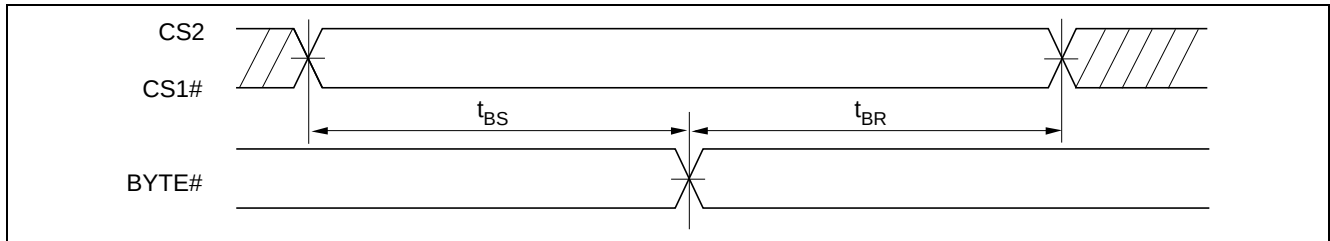
21. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.

22. t_{AS} is measured from the address valid to the beginning of write.

23. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

BYTE# Timing Conditions (BYTE# pin supported by only 48pin TSOP (I) type)

Parameter	Symbol	Min.	Max.	Unit	Note
BYTE# setup time	t_{BS}	5	-	ms	
BYTE# recovery time	t_{BR}	5	-	ms	

BYTE# Timing Waveforms

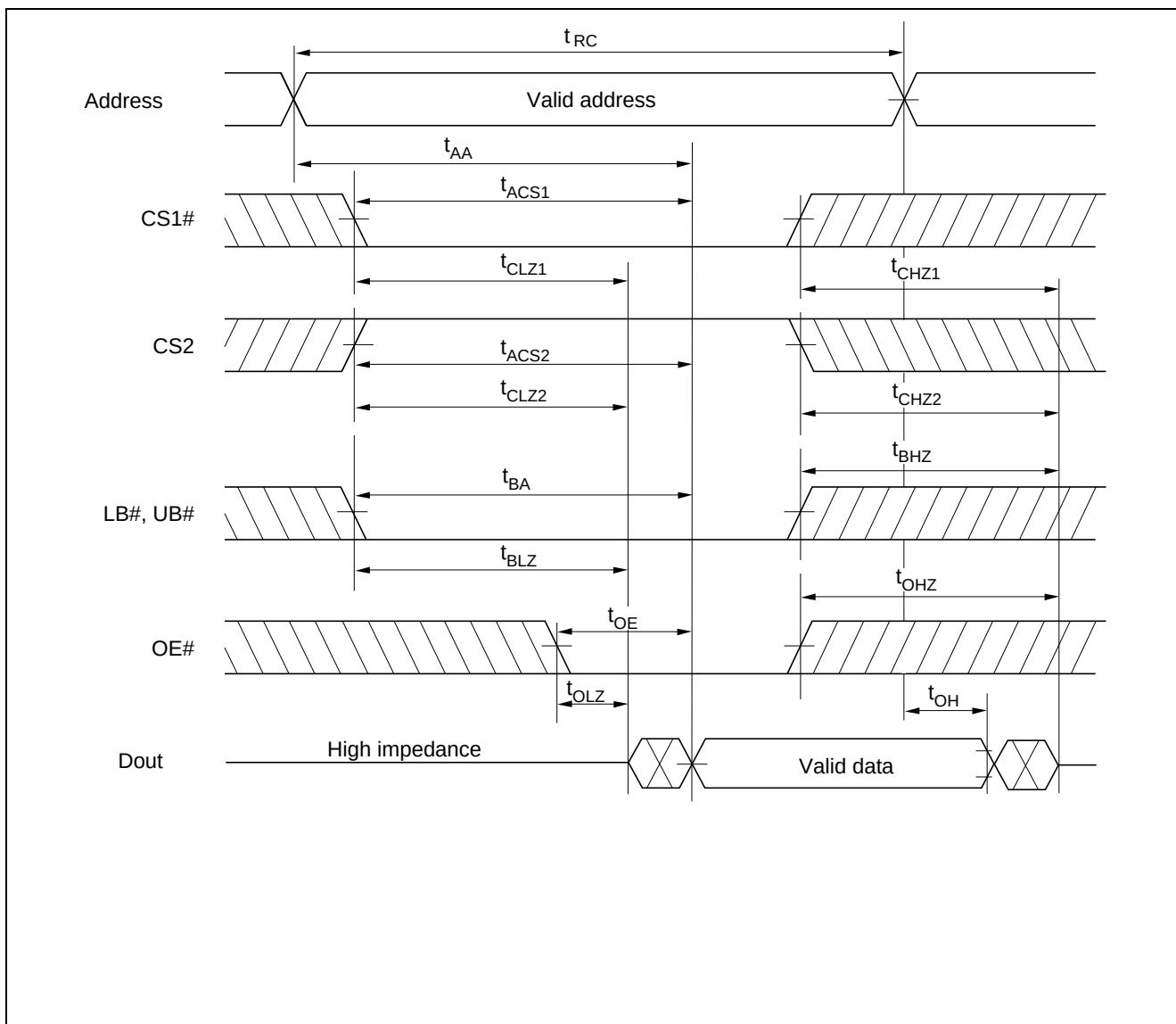
Note 24. Timing specs for switching between word-mode (1M x16) and byte-mode (2M x8) on the fly (when dynamically switch while Vcc supply).

Tie the BYTE# pin to SRAM's Vcc to use it fixedly as word-mode (1M x16).

Tie the BYTE# pin to Vss (GND) to use the SRAM fixedly as byte-mode (2M x8).

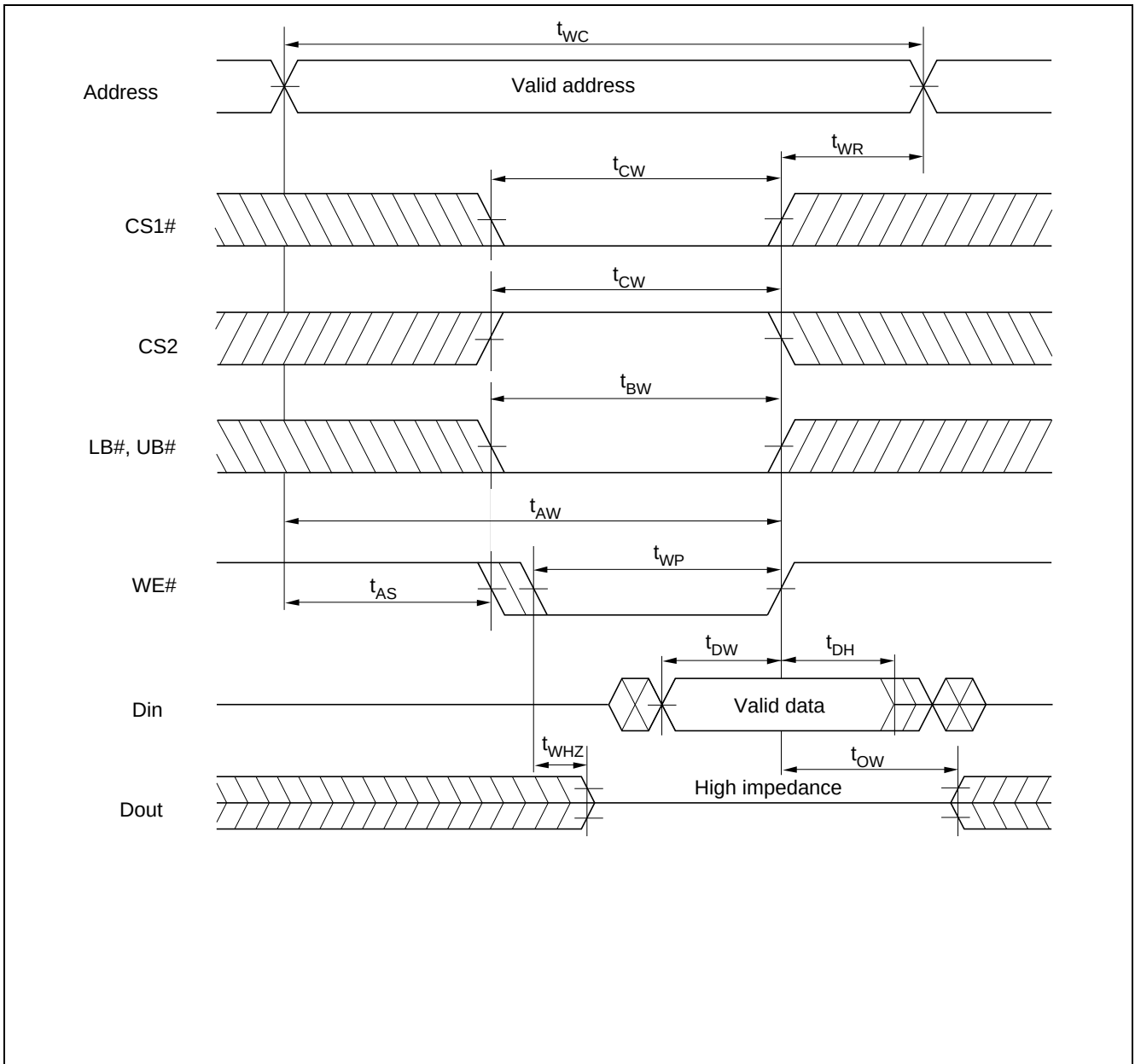
25. When used as word-mode together with a battery backup, tie the BYTE# pin to backup Vcc supply (SRAM's Vcc). Do not tie the BYTE# pin to the regular Vcc that is to be discharged to Vss level when power shutdown.

Timing Waveforms

Read Cycle^{*26}

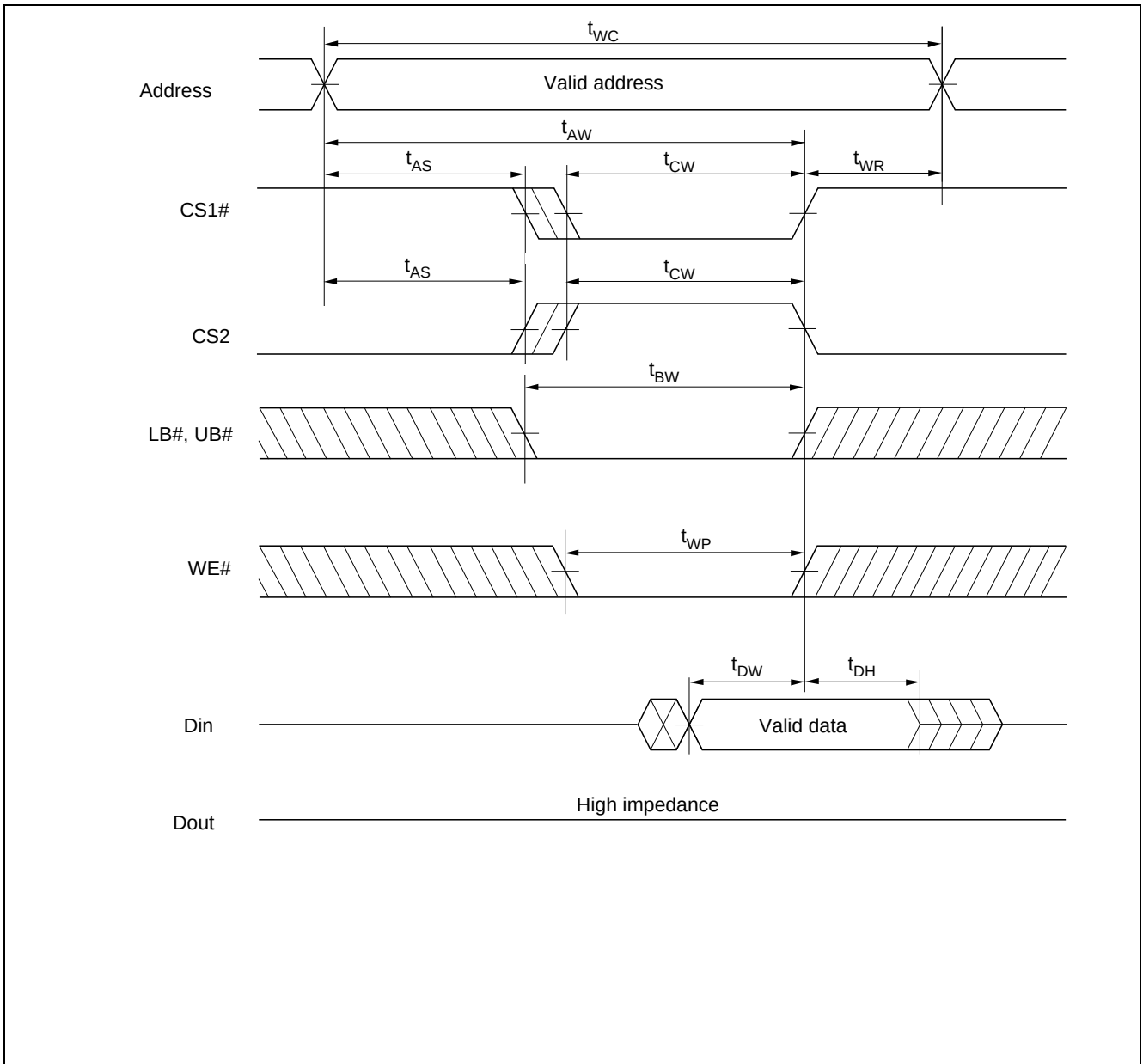
Note 26. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

Write Cycle (1)^{*27} (WE# Clock)

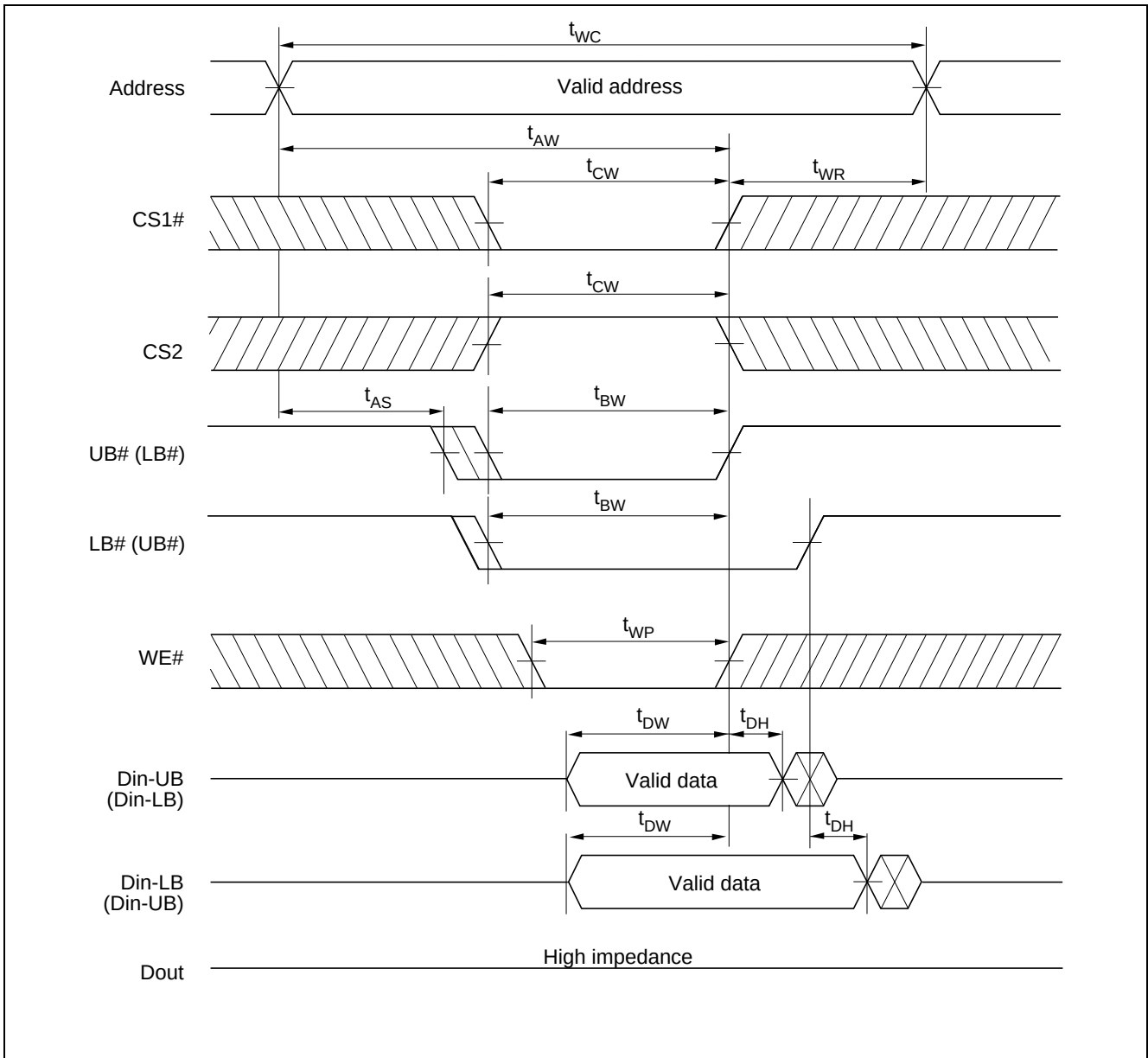
Note 27. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

Write Cycle (2)^{*28} (CS1#, CS2 Clock, OE# = V_{IH})


Note 28. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

Write Cycle (3)^{*29} (LB#, UB# Clock, OE# = V_{IH}, Word Mode)

Note 29. BYTE# pin applies only to 48pin TSOP (I).
 BYTE# $\geq V_{CC} - 0.2V$ (Word mode)

Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions*30,31	
V _{CC} for data retention	V _{DR}	1.5	—	3.6	V	Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V	
Data retention current	I _{CCDR}	—	0.4*32	3	μA	~+25°C	V _{CC} = 3.0V, Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V
		—	0.6*33	5	μA	~+40°C	
		—	2.2*34	6	μA	~+70°C	
		—	4.4*35	8	μA	~+85°C	
Chip deselect time to data retention	t _{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t _R	5	—	—	ms		

Note 30. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ or BYTE# $\leq 0.2V$

31. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and Din buffer.

If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2V$ or $0 \leq CS2 \leq 0.2V$.

The other inputs levels (address, WE#, OE#, LB#, UB#, I/O) can be in the high impedance state.

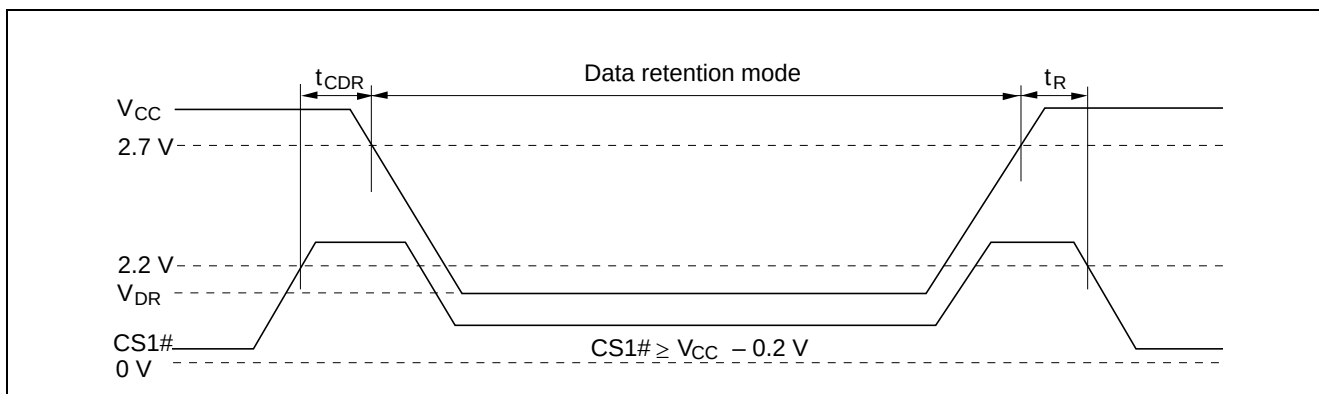
32. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=25^{\circ}C$), and not 100% tested.

33. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=40^{\circ}C$), and not 100% tested.

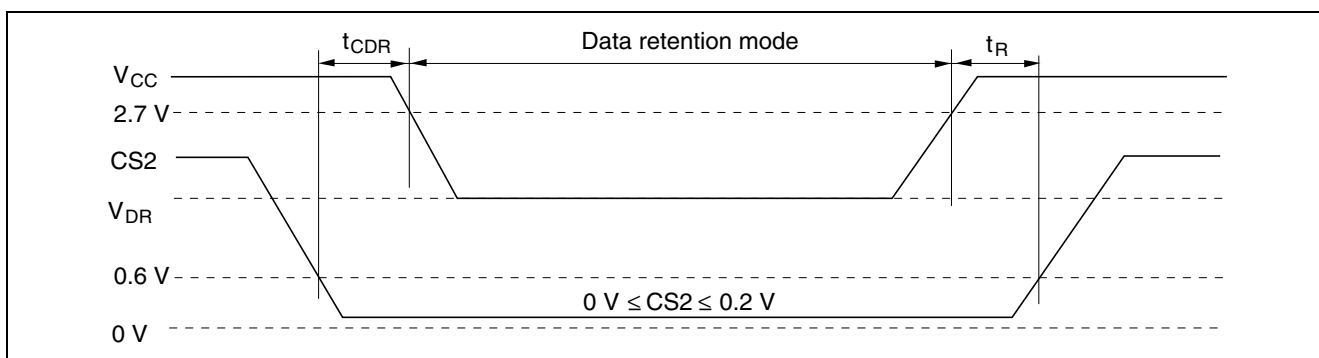
34. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=70^{\circ}C$), and not 100% tested.

35. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=85^{\circ}C$), and not 100% tested.

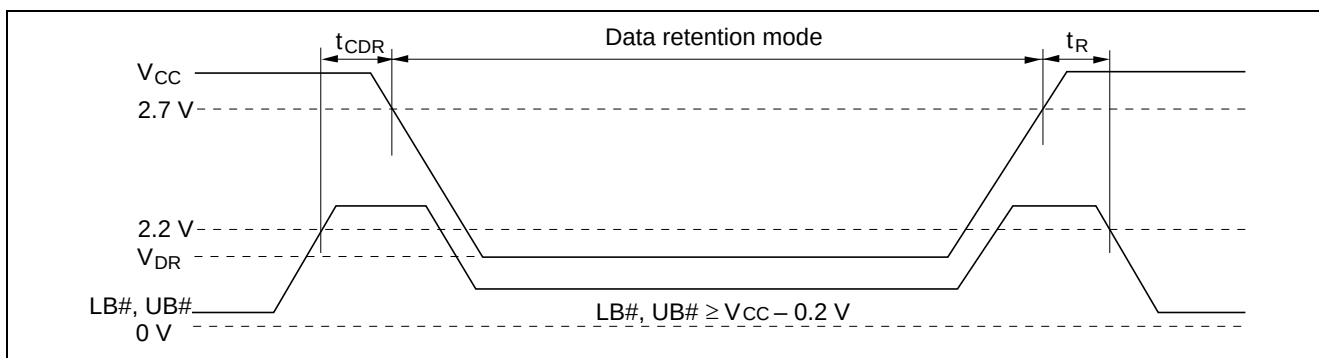
Low Vcc Data Retention Timing Waveforms (1) (CS1# Controlled)*36



Low Vcc Data Retention Timing Waveforms (2) (CS2 Controlled)*36



Low Vcc Data Retention Timing Waveforms (3) (LB#, UB# Controlled, Word Mode)*37



Note 36. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ or BYTE# $\leq 0.2V$

37. BYTE# pin applies only to 48pin TSOP (I).

BYTE# $\geq V_{CC} - 0.2V$ (Word mode)

Revision History	RMLV1616A-U Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2022.12.05	—	First Edition issued

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