RRA483xx

±15kV ESD Protected, 3.3V to 5V RS-485/422 Transceivers

Description

The Renesas RRA483xx (RRA48315, RRA48316, RRA48325, RRA48326, RRA48355, and RRA48356) are ±15kV IEC 61000-4-2 ESD protected, 3.3V to 5V powered single transceivers that meet both the RS-485/422 standards for balanced communication. These devices have very low bus currents (+125µA/-100µA), so they present a true 1/8 unit load to the RS-485 bus. This allows up to 256 transceivers on the network without violating the RS-485 specification's 32 unit load maximum, and without using repeaters. For example, in a remote utility meter reading system, individual meter readings are routed to a concentrator using an RS-485 network, so the high allowed node count minimizes the number of repeaters required.

Hot plug circuitry ensures that the Transmitter (Tx) and Receiver (Rx) outputs remain in a high impedance state while the power supply stabilizes.

Rx inputs feature a full fail-safe design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

The RRA48315, RRA48316, RRA48325, and RRA48326 use slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications. Slew rate limited versions also include receiver input filtering to enhance noise immunity in the presence of slow input signals.

The RRA48316, RRA48326, and RRA48356 are configured for full duplex (separate Rx input and Tx output pins) applications. The half duplex version multiplexes the Rx inputs and Tx outputs to allow transceivers with output disable functions in 8 Ld packages.

Features

- IEC 61000-4-2 ESD protection on RS-485 I/O pins
  - Air-gap discharge: ±15kV
  - Contact discharge: ±8kV
  - HBM Class 3B ESD level on all other pins: ±9kV
- IEC 61000-4-4 Electrical Fast Transient (EFT) protection on RS-485 I/O pins: ±5kV
- Full fail-safe (open, short, terminated/floating) receivers
- Hot plug - Tx and Rx outputs remain three-state during power-up
- True 1/8 unit load allows up to 256 devices on the bus
- Single 3.3V or 5V supply
- High data rates: up to 20Mbps
- Low quiescent supply current: 400µA (Typ)
  - Low shutdown (SHDN) current <0.6µA (Typ)
- -7V to +12V common-mode input/output voltage range
- Half and full duplex pinouts
- Three-state Rx and Tx outputs available
- Current limiting and thermal shutdown for driver overload protection
- Pb-free (RoHS compliant)

Applications

- Automated utility meter reading systems
- High node count systems
- Field bus networks
- Security camera networks
- Building environmental control/lighting systems
- Industrial/process control networks

Table 1. Summary of Features

Part Number	Half/Full Duplex	Data Rate (bps)	Slew-rate Limited?	Hot Plug?	# Devices On Bus	Rx/Tx Enable?	Quiescent I_{CC} (µA)	Low Power Shutdown?	Pin Count
RRA48315	Half	250k	Yes	Yes	256	Yes	400	Yes	8
RRA48316	Full	250k	Yes	Yes	256	Yes	400	Yes	10, 14
RRA48325	Half	1M	Yes	Yes	256	Yes	400	Yes	8
RRA48326	Full	1M	Yes	Yes	256	Yes	400	Yes	10, 14
RRA48355	Half	20M	No	Yes	256	Yes	400	Yes	8
RRA48356	Full	20M	No	Yes	256	Yes	400	Yes	10, 14

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1. Overview

1.1 Typical Operating Circuits

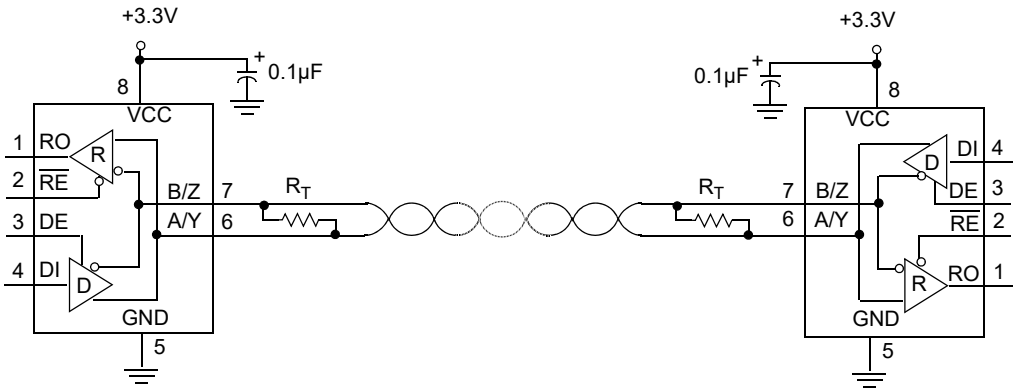


Figure 1. RRA48315, RRA48325, and RRA48355 Circuits

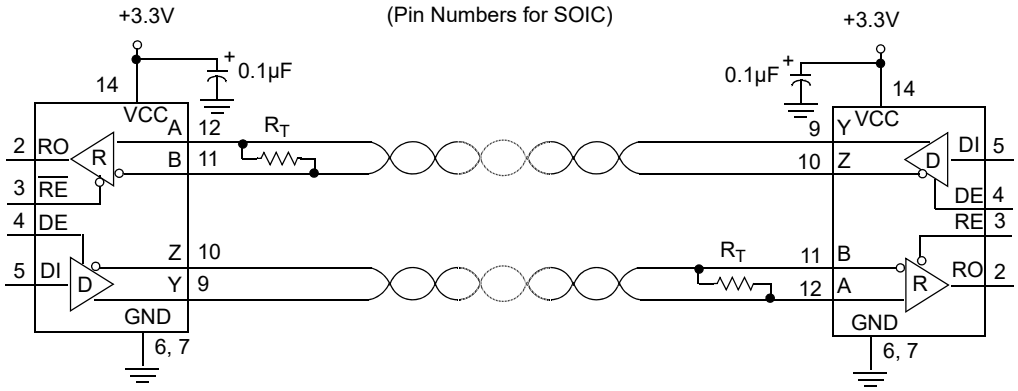


Figure 2. RRA48316, RRA48326, and RRA48356 Circuits

2. Pin Information

2.1 Pin Assignments - 8 Ld MSOP/SOIC

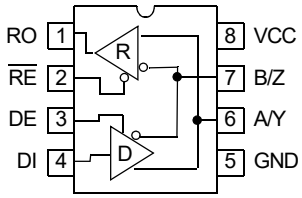


Figure 3. Pin Assignments (8 Ld MSOP/SOIC) - Top View

2.2 Pin Descriptions - 8 Ld MSOP/SOIC

Table 2. 8 Ld MSOP/SOIC Pin Descriptions

Pin Number	Pin Name	Function
1	RO	Receiver output: If A-B ≥ -50mV, RO is high; If A-B ≤ -200mV, RO is low; if A and B are unconnected (floating) or shorted, RO = High.
2	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND or through a 1kΩ to 3kΩ resistor to GND.
3	DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the Tx enable function is not required, connect DE to V_{CC} through a 1kΩ to 3kΩ resistor.
4	DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	GND	Ground connection.
6	A/Y	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, non-inverting receiver input and non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
7	B/Z	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
8	VCC	System power supply input (3.0V to 5.5V).

2.3 Pin Assignments - 10 Ld MSOP

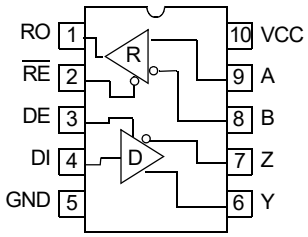


Figure 4. Pin Assignments (10 Ld MSOP) - Top View

2.4 Pin Descriptions - 10Ld MSOP

Table 3. 10 Ld MSOP Pin Descriptions

Pin #	Pin Name	Function
1	RO	Receiver output: If A-B ≥ -50mV, RO is high; If A-B ≤ -200mV, RO is low; if A and B are unconnected (floating) or shorted, RO = High.
2	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND or through a 1kΩ to 3kΩ resistor to GND.
3	DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the Tx enable function is not required, connect DE to V_{CC} through a 1kΩ to 3kΩ resistor.
4	DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	GND	Ground connection.
9	A	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, non-inverting receiver input.
8	B	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, inverting receiver input.
6	Y	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, non-inverting driver output.
7	Z	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, inverting driver output.
10	VCC	System power supply input (3.0V to 5.5V).

2.5 Pin Assignments - 14 Ld SOIC

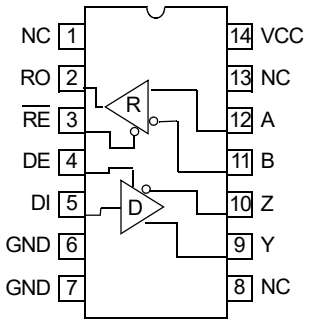


Figure 5. Pin Assignments (14 Ld SOIC) - Top View

2.6 Pin Descriptions - 14 Ld SOIC

Table 4. 14 Ld SOIC Pin Descriptions

Pin #	Pin Name	Function
2	RO	Receiver output: If A-B ≥ -50mV, RO is high; If A-B ≤ -200mV, RO is low; if A and B are unconnected (floating) or shorted, RO = High.
3	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function is not required, connect $\overline{RE}$ directly to GND or through a 1kΩ to 3kΩ resistor to GND.
4	DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the Tx enable function is not required, connect DE to V_{CC} through a 1kΩ to 3kΩ resistor.
5	DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
6, 7	GND	Ground connection.
12	A	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, non-inverting receiver input.
11	B	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, inverting receiver input.
9	Y	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, non-inverting driver output.

Table 4. 14 Ld SOIC Pin Descriptions (Cont.)

Pin #	Pin Name	Function
10	Z	±15kV IEC 61000-4-2 ESD Protected RS-485/422 level, inverting driver output.
14	VCC	System power supply input (3.0V to 5.5V).
1, 8, 13	NC	No Connection.

2.7 Truth Tables

Table 5. Transmitting Truth Table

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z[1]	High-Z[1]

1. Devices are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts do not enter shutdown. If the inputs are in this state for at least 600ns, the parts enter shutdown. Low Power Shutdown Mode.

Table 6. Receiving Truth Table

Receiving				
Inputs				Output
$\overline{RE}$	DE Half Duplex[1]	DE Full Duplex	A-B	RO
0	0	X	$V_{A-B} \geq -0.05V$	1
0	0	X	$-0.05V > V_{A-B} > -0.2V$	Undetermined
0	0	X	$V_{A-B} \leq -0.2V$	0
0	0	X	Inputs Open/Shorted	1
1	0	0	X	High-Z[2]
1	1	1	X	High-Z

1. In the half-duplex versions, under normal operation, the RO output follows the DI input with a time delay (sum of the driver differential output delay and receiver input to output delay) when $\overline{RE}$ = 0 and DE = 1.
2. Devices are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts do not enter shutdown. If the inputs are in this state for at least 600ns, the parts enter shutdown. Low Power Shutdown Mode.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC to GND	-	7	V
Input Voltages			
DI	-0.3	V_{CC} +0.3	V
DE, $\overline{RE}$	-0.3	V_{CC} +0.3	V
Input/Output Voltages			
A, B, Y, Z	-17	17	V
RO	-0.3	V_{CC} +0.3	V
Short-Circuit Duration			
Y, Z	Continuous		
Storage Temperature Range	-65	150	°C
Junction Temperature (Plastic Package)	-	150	°C

3.2 ESD Ratings

Parameter	Test Conditions	Rating	Unit
RS-485 Bus Pins (A, Y, B, Z, A/Y, B/Z)	IEC 61000-4-2, air-gap discharge method	±15	kV
	IEC 61000-4-2, contact discharge method	±8	kV
	Human Body Model, from bus pins to GND	±20	kV
	IEC 61000-4-4 EFT	±5	kV
All Pins	Human Body Model to JEDEC JS-001	±9	kV
	Charged Device Model to JEDEC JS-002	±1.5	kV

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	118	°C/W
		θ_{JC}	Junction to case	65	°C/W
Thermal Resistance	8 Ld MSOP Package	θ_{JA}[1]	Junction to ambient	156	°C/W
		θ_{JC}	Junction to case	75	°C/W
Thermal Resistance	10 Ld MSOP Package	θ_{JA}[1]	Junction to ambient	152	°C/W
		θ_{JC}	Junction to case	75	°C/W
Thermal Resistance	14 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	88	°C/W
		θ_{JC}	Junction to case	55	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-40	+105	°C
Supply Voltage	3.0	5.5	V

3.5 Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 5.5V; unless otherwise specified. Typicals are at V_{CC} = 5.0V, T_A = +25°C[1]

Parameter	Symbol	Test Conditions		Temp (°C)	Min[2]	Typ	Max[2]	Unit
DC Characteristics								
Driver Differential V_{OUT}	V_{OD}	R_L = 100Ω (RS-422) (Figure 6)		Full	2	3.6	-	V
		R_L = 100Ω (RS-422), V_{CC} ≥ 4.5V (Figure 6)		Full	3	3.6	-	V
		R_L = 54Ω (RS-485) (Figure 6)		Full	1.5	3.1	-	V
		R_L = 54Ω (RS-485), V_{CC} ≥ 4.5V (Figure 6)		Full	2.5	3.1	-	V
		No Load		Full	2.1	-	V_{CC}	
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 7)		Full	1.5	3	-	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V, V_{CC} ≥ 4.5V (Figure 7)		Full	2.4	3	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 6)		Full	-	-	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 6)		Full	-	V_{CC}/2	3.3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 6)		Full	-	-	0.2	V
Driver Short-Circuit Current	I_{OSD}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V		Full	-	±150	±200	mA
Input Current (A, B)	I_{IN2}	DE = 0V, VCC = 0V to 5.5V	V_{IN} = 12V	Full	-	-	125	µA
			V_{IN} = -7V	Full	-100	-	-	µA
Receiver Differential Threshold Voltage, Rising	V_{TH+}	-7V ≤ V_{CM} ≤ 12V		Full	-	-90	-50	mV
Receiver Differential Threshold Voltage, Falling	V_{TH-}	-7V ≤ V_{CM} ≤ 12V		Full	-200	-140	-	mV
Receiver Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-	50	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = -50mV		Full	V_{CC} - 0.6	V_{CC} - 0.2	-	V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV		Full	-	0.2	0.4	V
Three-State (high impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-1	-	1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V		Full	96	170	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}		Full	±15	-	±85	mA
Logic Input High Voltage	V_{IH}	DI, DE, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DI, DE, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Hysteresis[3]	V_{HYS}	DE, $\overline{RE}$		25	-	70	-	mV
Logic Input Current	I_{IN1}	DI, DE, $\overline{RE}$		Full	-1	-	1	µA
Thermal Shutdown Threshold	T_{SD}	-		Full	-	160	-	°C

Test Conditions: V_{CC} = 3.0V to 5.5V; unless otherwise specified. Typicals are at V_{CC} = 5.0V, T_A = +25°C[1] (Cont.)

Parameter	Symbol	Test Conditions		Temp (°C)	Min[2]	Typ	Max[2]	Unit
Supply Current								
No-Load Supply Current	I_{CC}	DI = 0V or V_{CC}	DE = V_{CC}, $\overline{RE}$ = 0V or V_{CC}	Full	-	400	600	µA
			DE = 0V, $\overline{RE}$ = 0V	Full	-	350	550	µA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}		Full	-	0.6	3	µA
Driver Switching Characteristics (RRA48315, RRA48316, 250kbps)								
Maximum Data Rate[4]	f_{MAX}	V_{OD} = ±1.5V, C_D = 820pF (Figure 10)		Full	250	-	-	kbps
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	-	780	1300	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	-	40	100	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	550	1000	1300	ns
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)		Full	-	275	600	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)		Full	-	200	600	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)		Full	-	30	60	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)		Full	-	30	60	ns
Time to Shutdown[5]	t_{SHDN}	-		Full	60	120	600	ns
Driver Enable from Shutdown to Output High[5]	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)		Full	-	2000	3000	ns
Driver Enable from Shutdown to Output Low[5]	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)		Full	-	2000	3000	ns
Driver Switching Characteristics (RRA48325, RRA48326, 1Mbps)								
Maximum Data Rate[4]	f_{MAX}	V_{OD} = ±1.5V, C_D = 820pF (Figure 10)		Full	1000	-	-	kbps
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	-	280	400	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	-	4	10	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	100	200	300	ns
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)		Full	-	100	300	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)		Full	-	100	300	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)		Full	-	30	60	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)		Full	-	30	60	ns
Time to Shutdown[5]	t_{SHDN}	-		Full	60	120	600	ns
Driver Enable from Shutdown to Output High[5]	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)		Full	-	2000	3000	ns
Driver Enable from Shutdown to Output Low[5]	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)		Full	-	2000	3000	ns
Driver Switching Characteristics (RRA48355, RRA48356, 20Mbps)								
Maximum Data Rate[4]	f_{MAX}	V_{OD} = ±1.5V, C_D = 350pF (Figure 10)		Full	20	-	-	Mbps
Driver Differential Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	-	20	30	ns
Driver Differential Output Skew	t_{SKEW}	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)		Full	-	1	4	ns

Test Conditions: V_{CC} = 3.0V to 5.5V; unless otherwise specified. Typicals are at V_{CC} = 5.0V, T_A = +25°C[1] (Cont.)

Parameter	Symbol	Test Conditions	Temp (°C)	Min[2]	Typ	Max[2]	Unit
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 54Ω, C_D = 50pF (Figure 8)	Full	-	10	15	ns
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)	Full	-	25	50	ns
Driver Enable to Output Low	t_{ZL}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)	Full	-	25	50	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)	Full	-	30	60	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)	Full	-	30	60	ns
Time to Shutdown[5]	t_{SHDN}	-	Full	60	120	600	ns
Driver Enable from Shutdown to Output High[5]	$t_{ZH(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = GND (Figure 9)	Full	-	2000	3000	ns
Driver Enable from Shutdown to Output Low[5]	$t_{ZL(SHDN)}$	R_L = 500Ω, C_L = 50pF, SW = V_{CC} (Figure 9)	Full	-	2000	3000	ns
Receiver Switching Characteristics (RRA48315, RRA48316, 250kbps)							
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V, -7V ≤ V_{CM} ≤ 12V	Full	1	10	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	V_{ID} = ±1.5V, -7V ≤ V_{CM} ≤ 12V (Figure 11)	Full	-	100	130	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 11)	Full	-	6	12	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	10	40	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12	Full	-	10	40	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	10	40	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12)	Full	-	10	40	ns
Time to Shutdown[5]	t_{SHDN}	-	Full	60	120	600	ns
Receiver Enable from Shutdown to Output High[5]	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	2000	2500	ns
Receiver Enable from Shutdown to Output Low[5]	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12)	Full	-	2000	2500	ns
Receiver Switching Characteristics (RRA48325, RRA48326, 1Mbps)							
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V, -7V ≤ V_{CM} ≤ 12V	Full	1	10	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	V_{ID} = ±1.5V, -7V ≤ V_{CM} ≤ 12V (Figure 11)	Full	-	100	130	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 11)	Full	-	6	12	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	10	40	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12	Full	-	10	40	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	10	40	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12)	Full	-	10	40	ns
Time to Shutdown[5]	t_{SHDN}	-	Full	60	120	600	ns
Receiver Enable from Shutdown to Output High[5]	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	2000	2500	ns
Receiver Enable from Shutdown to Output Low[5]	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12)	Full	-	2000	2500	ns

Test Conditions: V_{CC} = 3.0V to 5.5V; unless otherwise specified. Typicals are at V_{CC} = 5.0V, T_A = +25°C[1] (Cont.)

Parameter	Symbol	Test Conditions	Temp (°C)	Min[2]	Typ	Max[2]	Unit
Receiver Switching Characteristics (RRA48355, RRA48356, 20Mbps)							
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V, -7V ≤ V_{CM} ≤ 12V	Full	20	25	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	V_{ID} = ±1.5V, -7V ≤ V_{CM} ≤ 12V (Figure 11)	Full	-	30	50	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 11)	Full	-	2	5	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	8	20	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12	Full	-	8	20	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	8	20	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12)	Full	-	8	20	ns
Time to Shutdown[5]	t_{SHDN}	-	Full	60	120	600	ns
Receiver Enable from Shutdown to Output High[5]	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 12)	Full	-	2000	2500	ns
Receiver Enable from Shutdown to Output Low[5]	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 12)	Full	-	2000	2500	ns

1. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
3. Only applies to RRA48315, RRA48316, RRA48325 and RRA48326. For RRA48355 and RRA48356, there is no logic input hysteresis.
4. Limits established by characterization and are not production tested.
5. Devices are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts do not enter shutdown. If the inputs are in this state for at least 600ns, the parts enter shutdown. Low Power Shutdown Mode.

3.6 Test Circuits and Waveforms

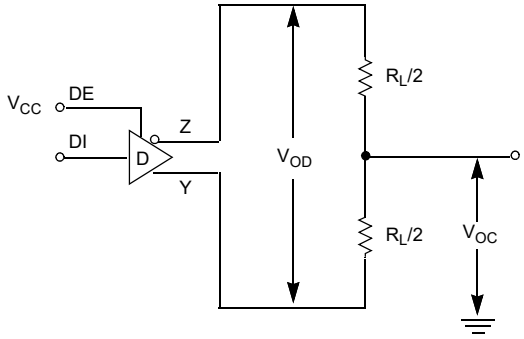


Figure 6. DC Driver Test Circuit V_{OD} and V_{OC}

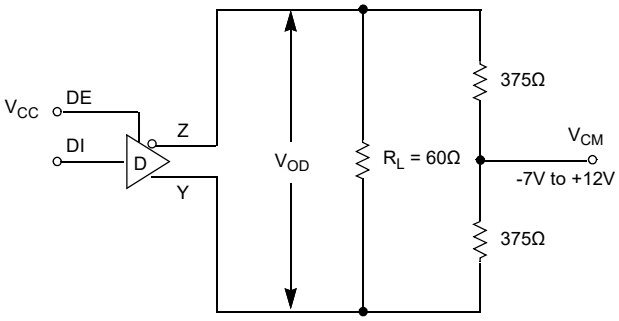
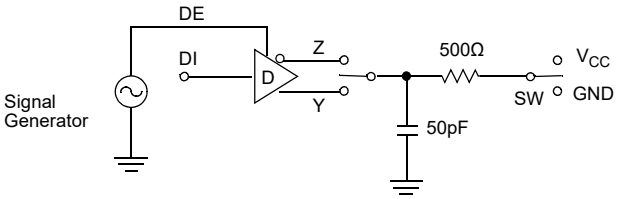


Figure 7. DC Driver Test Circuit V_{OD} with Common-Mode Load

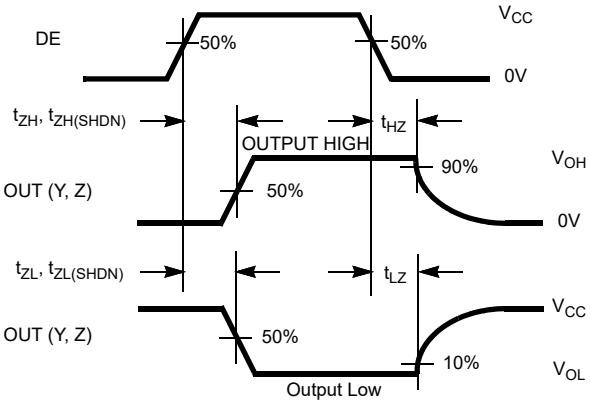


Figure 8. Driver Propagation Delay and Differential Transition Times



Parameter	Output	$\overline{RE}$	DI	SW
t_{HZ}	Y/Z	X	1/0	GND
t_{LZ}	Y/Z	X	0/1	V_{CC}
t_{ZH}	Y/Z	0[1]	1/0	GND
t_{ZL}	Y/Z	0[1]	0/1	V_{CC}
$t_{ZH(SHDN)}$	Y/Z	1[2]	1/0	GND
$t_{ZL(SHDN)}$	Y/Z	1[2]	0/1	V_{CC}

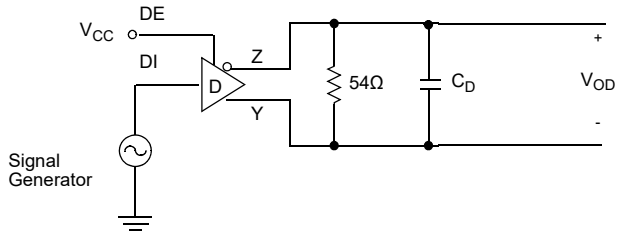
1. When testing devices with the shutdown feature, keep $\overline{RE}$ = 0 to prevent the device from entering shutdown.
2. Set the $\overline{RE}$ signal high time >600ns to ensure that the device enters shutdown.



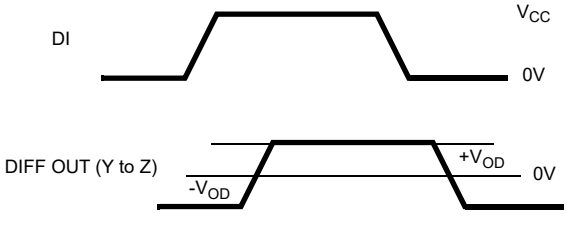
Test Circuit

Measurement Points

Figure 9. Driver Enable and Disable Times

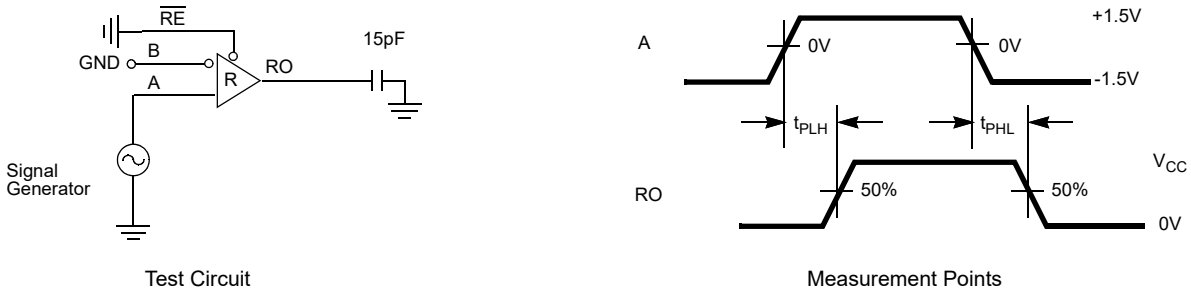


Test Circuit



Measurement Points

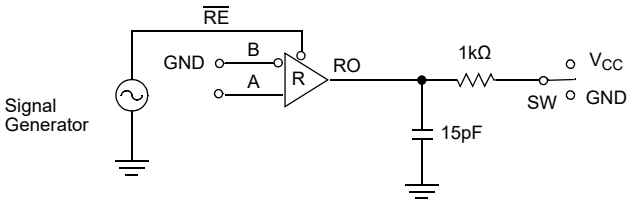
Figure 10. Driver Data Rate



Test Circuit

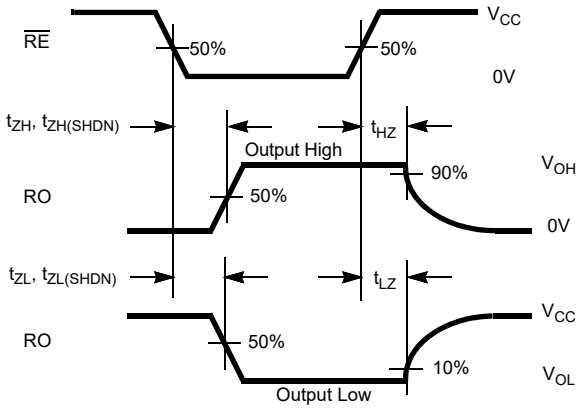
Measurement Points

Figure 11. Receiver Propagation Delay



Parameter	DE	A	SW
t_{HZ}	X	+1.5V	GND
t_{LZ}	X	-1.5V	V_{CC}
t_{ZH}[1]	0	+1.5V	GND
t_{ZL}[1]	0	-1.5V	V_{CC}
$t_{ZH(SHDN)}$[2]	0	+1.5V	GND
$t_{ZL(SHDN)}$[2]	0	-1.5V	V_{CC}

1. When testing devices with the shutdown feature, the $\overline{RE}$ signal high time must be short enough (<60ns) to prevent the device from entering shutdown.
2. Set the $\overline{RE}$ signal high time > 600ns to ensure the device enters shutdown.



Test Circuit

Measurement Points

Figure 12. Receiver Enable and Disable Times

4. Typical Performance Curves

V_{CC} = 5.0V, T_A = +25°C, unless otherwise specified

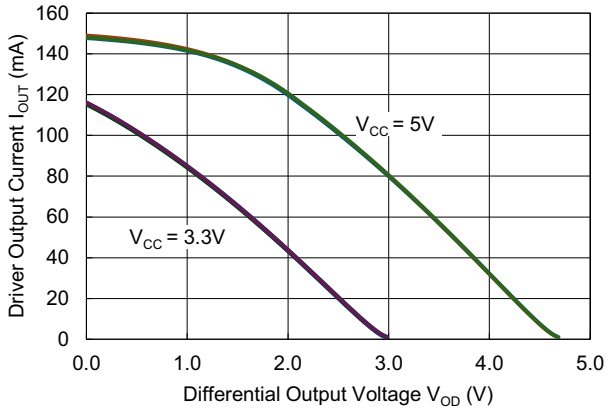


Figure 13. Driver Output Current vs Differential Output Voltage

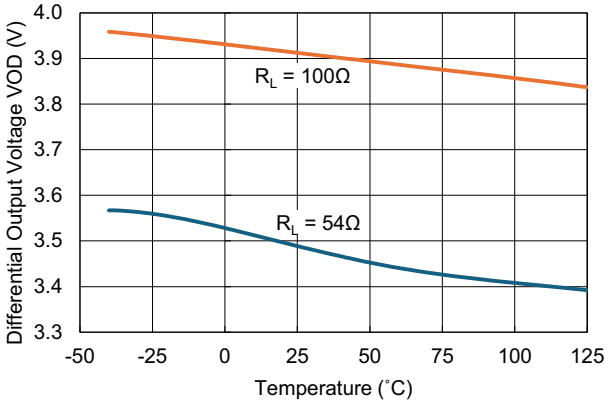


Figure 14. Driver Differential Output Voltage vs Temperature (V_{CC} = 5V)

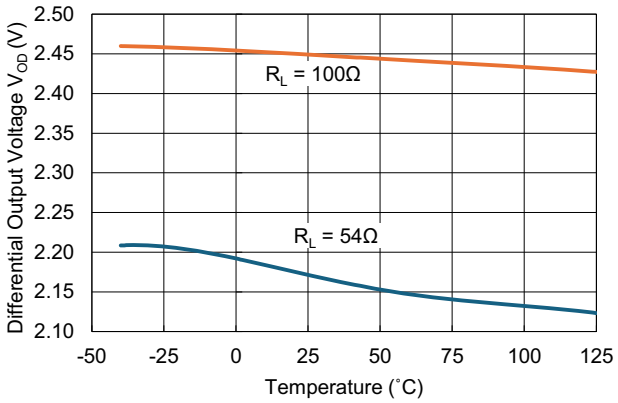


Figure 15. Driver Differential Output Voltage vs Temperature (V_{CC} = 3.3V)

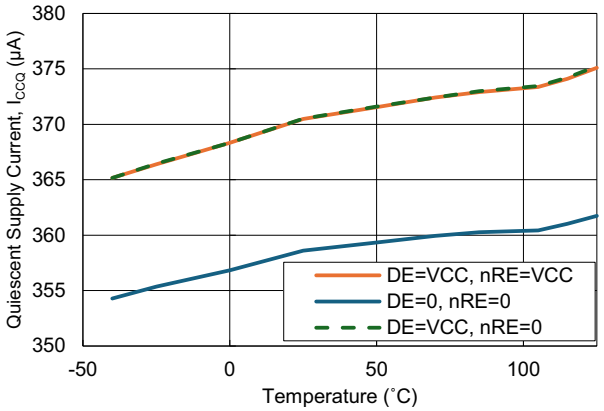


Figure 16. No-Load Quiescent Current vs Temperature (V_{CC} = 5V)

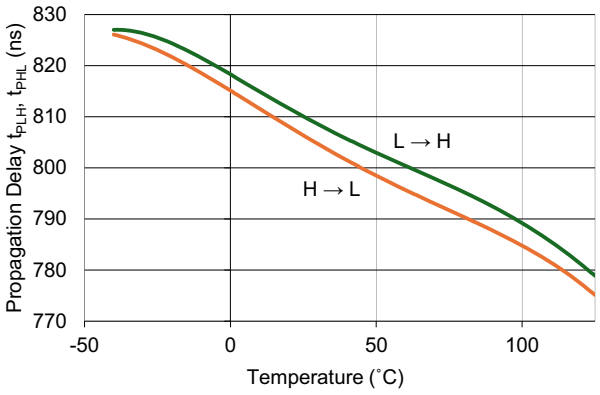


Figure 17. Driver Differential Propagation Delay vs Temperature (V_{CC} = 5V, 250kbps versions)

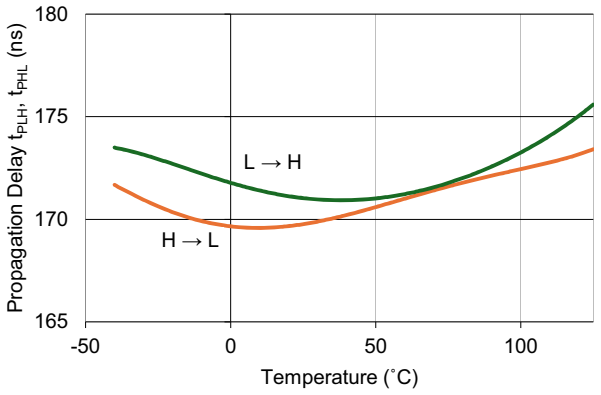


Figure 18. Driver Differential Propagation Delay vs Temperature (V_{CC} = 5V, 1Mbps versions)

V_{CC} = 5.0V, T_A = +25°C, unless otherwise specified (Cont.)

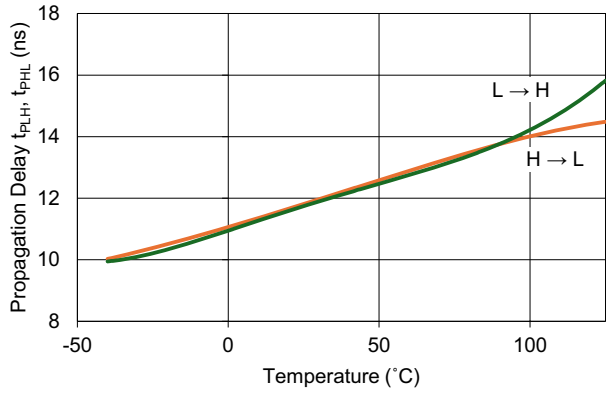


Figure 19. Driver Differential Propagation Delay vs Temperature (V_{CC} = 5V, 20Mbps versions)

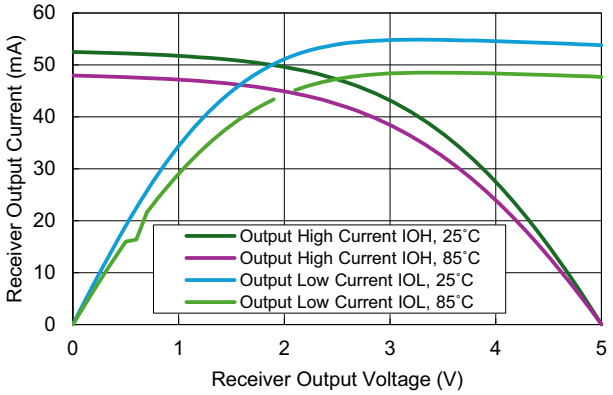


Figure 20. Receiver Output Current vs Receiver Output Voltage (V_{CC} = 5V)

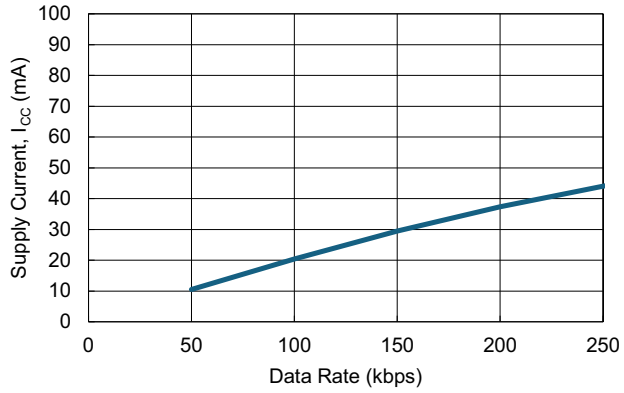


Figure 21. Supply Current vs Data Rate (V_{CC} = 5V, 25°C, R_{Diff} = 54Ω, C_{Diff} = 50pF, 250kbps versions)

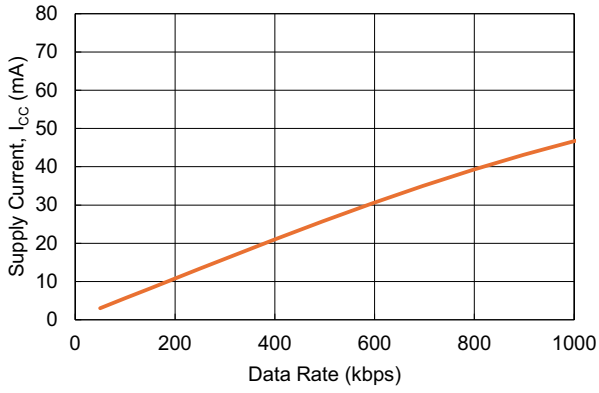


Figure 22. Supply Current vs Data Rate (V_{CC} = 5V, 25°C, R_{Diff} = 54Ω, C_{Diff} = 50pF, 1Mbps versions)

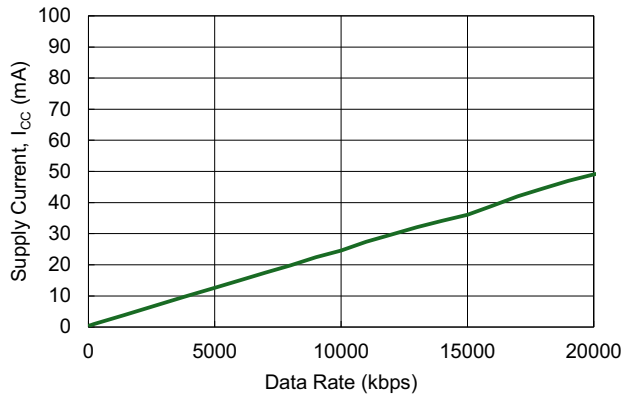


Figure 23. Supply Current vs Data Rate (V_{CC} = 5V, 25°C, R_{Diff} = 54Ω, C_{Diff} = 50pF, 20Mbps versions)

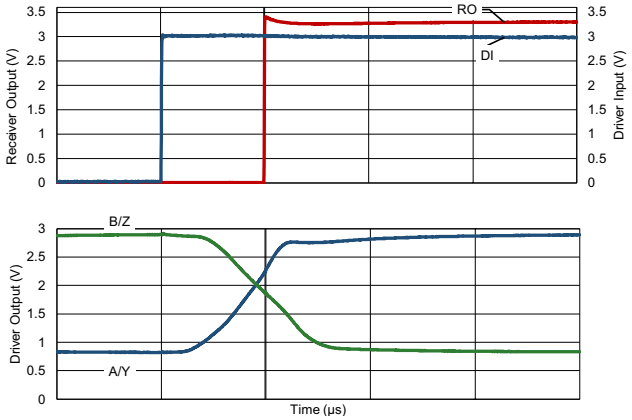


Figure 24. Driver and Receiver Waveforms, Low-to-High (V_{CC} = 3.3V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 250kbps versions)

V_{CC} = 5.0V, T_A = +25°C, unless otherwise specified (Cont.)

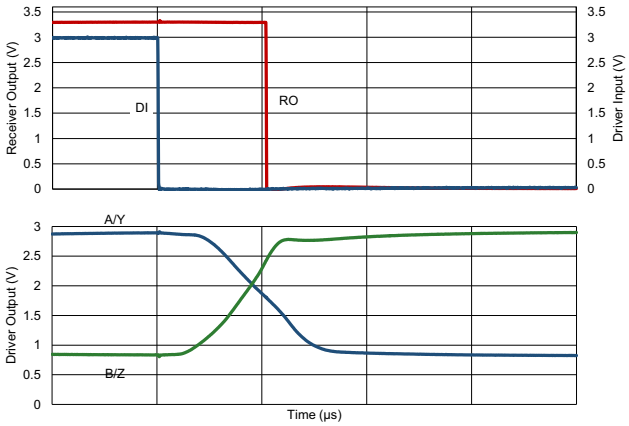


Figure 25. Driver and Receiver Waveforms, High-to-Low (V_{CC} = 3.3V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 250kbps versions)

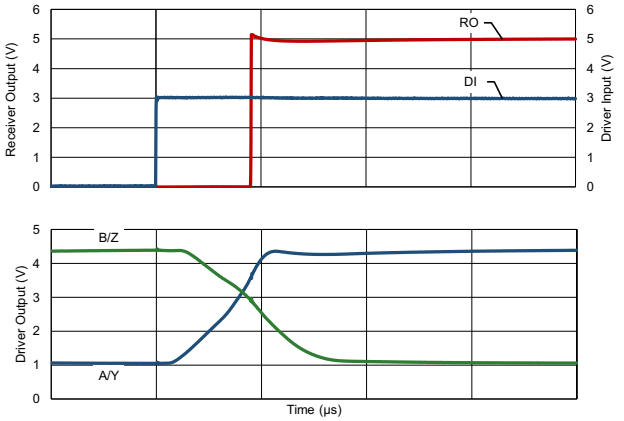


Figure 26. Driver and Receiver Waveforms, Low-to-High (V_{CC} = 5V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 250kbps versions)

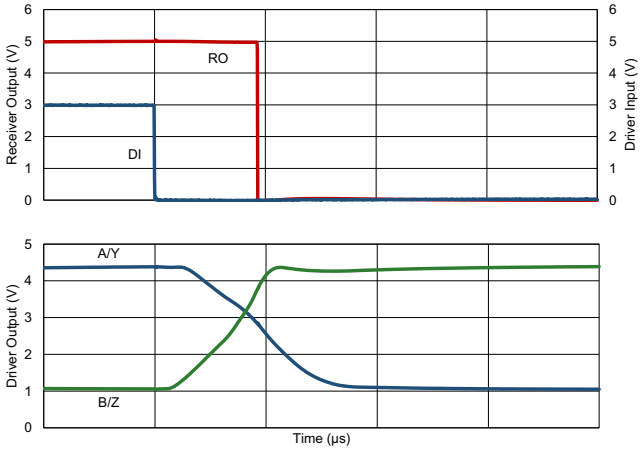


Figure 27. Driver and Receiver Waveforms, High-to-Low (V_{CC} = 5V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 250kbps versions)

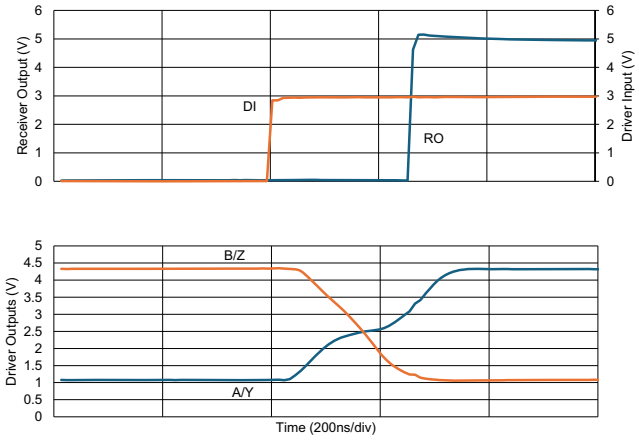


Figure 28. Driver and Receiver Waveforms, Low-to-High (V_{CC} = 5V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 1Mbps versions)

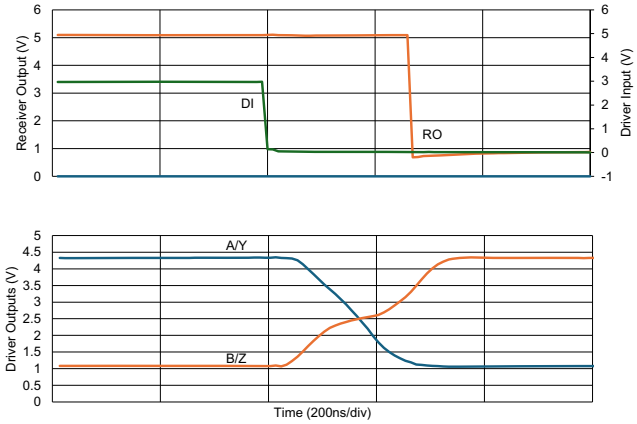


Figure 29. Driver and Receiver Waveforms, High-to-Low (V_{CC} = 5V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 1Mbps versions)

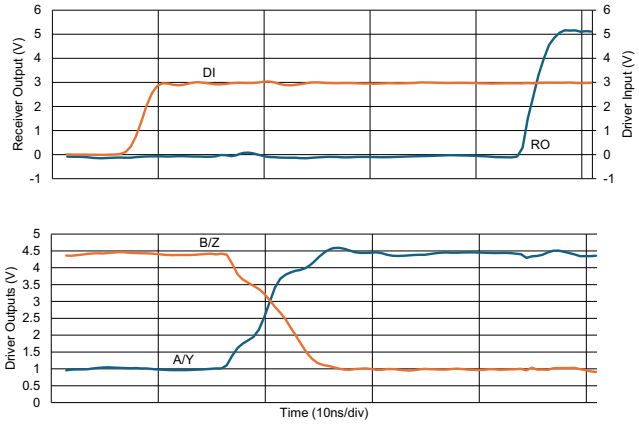


Figure 30. Driver and Receiver Waveforms, Low-to-High (V_{CC} = 5V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 20Mbps versions)

V_{CC} = 5.0V, T_A = +25°C, unless otherwise specified (Cont.)

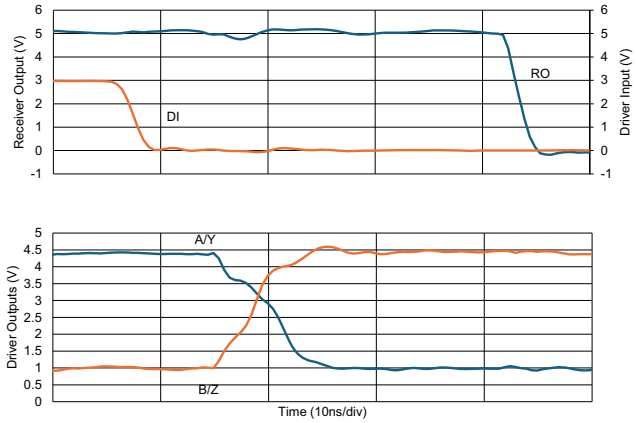


Figure 31. Driver and Receiver Waveforms, High-to-Low (V_{CC} = 5V, R_{Diff} = 54Ω, C_{Diff} = 50pF, 20Mbps versions)

5. Application Information

RS-485/422 are differential (balanced) data transmission standards for use in long-haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one-unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common-mode range (CMR), which specifies that the driver outputs and receiver inputs withstand common-mode voltages ranging from -7V to +12V. RS-422 and RS-485 are intended for runs as long as 4000ft, so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

5.1 Receiver Features

These devices use a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is better than ±200mV, as required by the RS-485/422 specifications.

The receiver input resistance of 96kΩ exceeds the RS-422 specification of 4kΩ and is eight times higher than the RS-485 Unit Load (UL) requirement of 12kΩ minimum. Therefore, these products are known as one-eighth UL transceivers and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs support a common-mode range of -7V to +12V, making them ideal for long networks where induced voltages and ground potential differences are realistic concerns.

All the receivers include a full fail-safe function that guarantees a high-level receiver output if the receiver inputs are unconnected (floating) or shorted. Fail-safe with shorted inputs is achieved by setting the Rx upper switching point to -50mV, thereby ensuring that a 0V differential input is interpreted as a logic-high input.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs are three-state using the active-low $\overline{RE}$ input.

5.2 Driver Features

The RS-485/422 driver is a differential output device that delivers at least 1.5V across a 54Ω load (RS-485) and at least 2V across a 100Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width and to minimize EMI.

All drivers are three-state through the active-high DE input.

The 250kbps and 1Mbps driver outputs are slew rate limited to minimize EMI and to reduce reflections in unterminated or improperly terminated networks.

5.3 Hot Plug Function

When a piece of equipment powers up, a period of time occurs in which the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power up may crash the bus. To avoid this scenario, the RRA483xx devices incorporate a hot plug function. During power up, circuitry monitoring V_{CC} ensures that the Tx and Rx outputs remain disabled for a period of time, regardless of the state of DE and $\overline{RE}$. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

5.4 ESD Protection

All pins on these devices include Class 3B (±9kV) Human Body Model (HBM) ESD protection structures. However, the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events up to ±20kV HBM and ±15kV IEC 61000-4-2 air-gap discharge and 8kV IEC 61000-4-2 contact discharge. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common-mode range of -7V to +12V. This built-in ESD protection eliminates the need for board-level protection structures (for example, transient suppression diodes), and the associated, undesirable capacitive load they present.

5.5 IEC 61000-4-2 Testing

The IEC 61000-4-2 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting Level 4 criteria without the need for additional board-level ESD protection on the RS-485 port.

5.5.1 Air-Gap Discharge Test Method

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on factors such as approach speed, humidity, and temperature. Therefore, it is difficult to obtain repeatable results. The RRA483xx RS-485 pins withstand ±15kV air-gap discharges.

5.5.2 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. The RRA483xx survive ±8kV contact discharges on the RS-485 pins.

5.6 Data Rates, Cables, and Terminations

RS-485/422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. The 250kbps versions can operate at full data rates with lengths of several thousand feet.

Twisted pair is the cable of choice for RS-485/422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative when using the 20Mbps devices to minimize reflections because the 20Mbps devices are not slew-limited. Short networks using the 250kbps and 1Mbps versions do not need to be terminated, but terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multi-receiver applications, keep stubs connecting receivers to the main cable as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Keep stubs connecting a transceiver to the main cable as short as possible.

5.7 Built-In Driver Overload Protection

As stated previously, the RS-485 spec requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement via driver output short-circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short-circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 spec, even at the common-mode voltage range extremes. Additionally, these devices use a foldback circuit which reduces the short-circuit current, and therefore the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short-circuit condition, devices use a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops by approximately 15°C. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

5.8 Low Power Shutdown Mode

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts and include a shutdown feature that reduces the already low quiescent I_{CC} to a less than 0.6uA (Typ), 3uA (Max) current. These devices enter shutdown whenever the receiver and driver are simultaneously disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver does not enter shutdown.

Note: The receiver and driver enable times increase when the transceiver enables from shutdown. For more information, refer to the notes at the end of the Electrical Specifications table.

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
RRA48315-IST	48315 IST	8 Ld SOIC	M8.15	Reel, 2.5k	-40°C to +105°C
RRA48315-IMT	48315	8 Ld MSOP	M8.118D	Reel, 2.5k	-40°C to +105°C
RRA48316-IPT	48316	10 Ld MSOP	M10.118	Reel, 2.5k	-40°C to +105°C
RRA48316-IRT	48316 IRT	14 Ld SOIC	M14.15	Reel, 2.5k	-40°C to +105°C
RRA48325-IST	48325 IST	8 Ld SOIC	M8.15	Reel, 2.5k	-40°C to +105°C
RRA48325-IMT	48325	8 Ld MSOP	M8.118D	Reel, 2.5k	-40°C to +105°C
RRA48326-IPT	48326	10 Ld MSOP	M10.118	Reel, 2.5k	-40°C to +105°C
RRA48326-IRT	48326 IRT	14 Ld SOIC	M14.15	Reel, 2.5k	-40°C to +105°C
RRA48355-IST	48355 IST	8 Ld SOIC	M8.15	Reel, 2.5k	-40°C to +105°C
RRA48355-IMT	48355	8 Ld MSOP	M8.118D	Reel, 2.5k	-40°C to +105°C
RRA48356-IPT	48356	10 Ld MSOP	M10.118	Reel, 2.5k	-40°C to +105°C
RRA48356-IRT	48356 IRT	14 Ld SOIC	M14.15	Reel, 2.5k	-40°C to +105°C

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the product information page for the RRA48315, RRA48316, RRA48325, RRA48326, RRA48355, and RRA48356. For more information about MSL, refer to TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

8. Revision History

Revision	Date	Description
1.01	Oct 13, 2026	▪ Updated Features section. ▪ Added Notes 3 and 4 and their corresponding references to the Electrical Specifications table. ▪ Updated the Driver Enable to Output High and Driver Disable from Output High typical specifications for the RRA48315, RRA48316 (250kbps) devices. ▪ Added RRA48325, RRA48326, RRA48355, and RRA48356 information throughout document. ▪ Updated Typical Performance Curves.
1.00	Sep 17, 2026	Initial release.

A. ECAD Design Information

This information supports the development of the PCB ECAD model for these devices. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
RRA48315-IST	8	SOIC	M8.15/GS0008AC
RRA48315-IMT	8	MSOP	M8.118D/HV0008AC
RRA48316-IPT	10	MSOP	M10.118/HM0010AA
RRA48316-IRT	14	SOIC	M14.15/GS0014AB
RRA48325-IST	8	SOIC	M8.15/GS0008AC
RRA48325-IMT	8	MSOP	M8.118D/HV0008AC
RRA48326-IPT	10	MSOP	M10.118/HM0010AA
RRA48326-IRT	14	SOIC	M14.15/GS0014AB
RRA48355-IST	8	SOIC	M8.15/GS0008AC
RRA48355-IMT	8	MSOP	M8.118D/HV0008AC
RRA48356-IPT	10	MSOP	M10.118/HM0010AA
RRA48356-IRT	14	SOIC	M14.15/GS0014AB

A.2 Symbol Pin Information

A.2.1 8-SOIC/MSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	RO	Output	-
2	$\overline{RE}$	Input	-
3	DE	Input	-
4	DI	Input	-
5	GND	Power	-
6	A/Y	Input/Output	-
7	B/Z	Input/Output	-
8	VCC	Power	-

A.2.2 10-MSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	RO	Output	-
2	$\overline{RE}$	Input	-
3	DE	Input	-
4	DI	Input	-
5	GND	Power	-
6	Y	Output	-
7	Z	Output	-
8	B	Input	-
9	A	Input	-
10	VCC	Power	-

A.2.3 14-SOIC

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	NC	Passive	-
2	RO	Output	-
3	$\overline{RE}$	Input	-
4	DE	Input	-
5	DI	Input	-
6	GND	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
7	GND	Power	-
8	NC	Passive	-
9	Y	Output	-
10	Z	Output	-
11	B	Input	-
12	A	Input	-
13	NC	Passive	-
14	VCC	Power	-

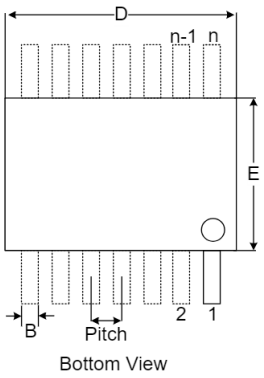
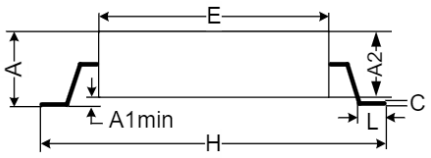
A.3 Symbol Parameters

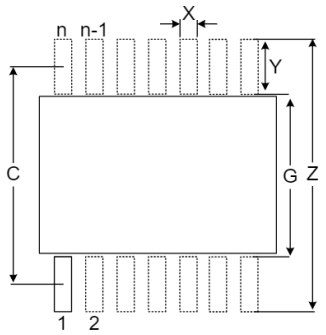
Orderable Part Number	Qualification	Mounting Type	RoHS	Min Operating Temperature	Max Operating Temperature	Min Supply Voltage	Max Supply Voltage	Data Rate	Duplex	Quiescent Current	ESD Protection	Interface
RRA48315-IST	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	250 kbps	Half	400 µA	Yes	RS-422,RS-485
RRA48315-IMT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	250 kbps	Half	400 µA	Yes	RS-422,RS-485
RRA48316-IPT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	250 kbps	Full	400 µA	Yes	RS-422,RS-485
RRA48316-IRT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	250 kbps	Full	400 µA	Yes	RS-422,RS-485
RRA48325-IST	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	1 M	Half	400 µA	Yes	RS-422,RS-485
RRA48325-IMT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	1 M	Half	400 µA	Yes	RS-422,RS-485
RRA48326-IPT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	1 M	Full	400 µA	Yes	RS-422,RS-485
RRA48326-IRT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	1 M	Full	400 µA	Yes	RS-422,RS-485
RRA48355-IST	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	20 M	Half	400 µA	Yes	RS-422,RS-485
RRA48355-IMT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	20 M	Half	400 µA	Yes	RS-422,RS-485
RRA48356-IPT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	20 M	Full	400 µA	Yes	RS-422,RS-485
RRA48356-IRT	Extended Industrial	SMD	Compliant	-40 °C	+105 °C	3.0 V	5.5 V	20 M	Full	400 µA	Yes	RS-422,RS-485

A.4 Footprint Design Information

A.4.1 8-SOIC

IPC Footprint Type	Package Code/POD Number	Number of Pins
SOIC	M8.15/GS0008AC	8

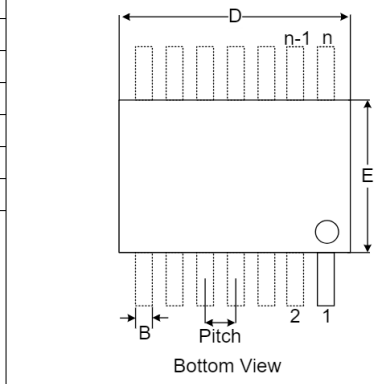
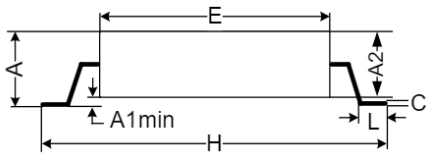
Description	Dimension	Value (mm)	Diagram[1]
Minimum lead span (horizontal side)	Hmin	5.80	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.20	
Minimum body span (pin1 side)	Dmin	4.80	
Maximum body span (pin1 side)	Dmax	5.00	
Minimum body span (vertical side)	Emin	3.80	
Maximum body span (vertical side)	Emax	4.00	
Minimum Lead Width	Bmin	0.33	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	1.27	

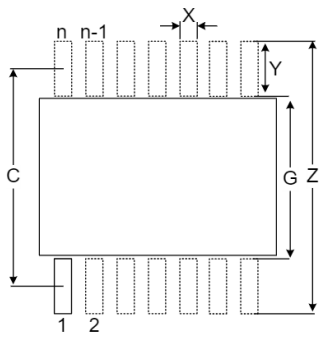
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram[1]**
Distance between left pad toe to right pad toe.	Z	7.40	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.00	
Row spacing. Distance between pad centers	C	5.20	
Pad Width	X	0.60	
Pad Length	Y	2.20	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.2 8-MSOP

IPC Footprint Type	Package Code/POD Number	Number of Pins
SOP	M8.118D/HV0008AC	8

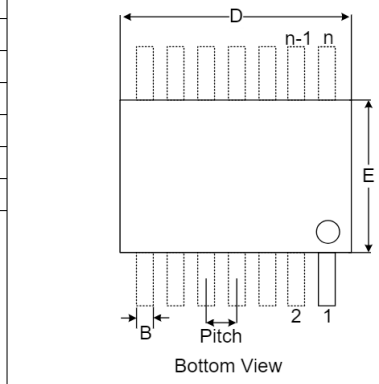
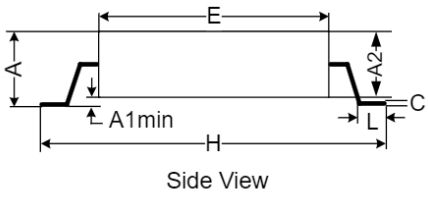
Description	Dimension	Value (mm)	Diagram[1]
Minimum lead span (horizontal side)	Hmin	4.70	 Bottom View
Maximum lead span (horizontal side)	Hmax	5.10	
Minimum body span (pin1 side)	Dmin	2.90	
Maximum body span (pin1 side)	Dmax	3.10	
Minimum body span (vertical side)	Emin	2.90	
Maximum body span (vertical side)	Emax	3.10	
Minimum Lead Width	Bmin	0.22	
Maximum Lead Width	Bmax	0.40	
Minimum Lead Length	Lmin	0.40	 Side View
Maximum Lead Length	Lmax	0.80	
Maximum Height	Amax	1.10	
Minimum Standoff Height	A1min	0.00	
Minimum Lead Thickness	cmin	0.08	
Maximum Lead Thickness	cmax	0.23	
Total number of pin positions (including absent pins)	PinCount	8	
Distance between the center of any two adjacent pins	Pitch	0.65	

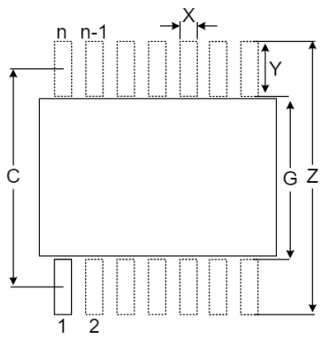
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram[1]**
Distance between left pad toe to right pad toe.	Z	5.50	 PCB Top View
Distance between left pad heel to right pad heel.	G	3.10	
Row spacing. Distance between pad centers	C	4.30	
Pad Width	X	0.32	
Pad Length	Y	1.20	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.3 10-MSOP

IPC Footprint Type	Package Code/ POD number	Number of Pins
SOP	M10.118/HM0010AA	10

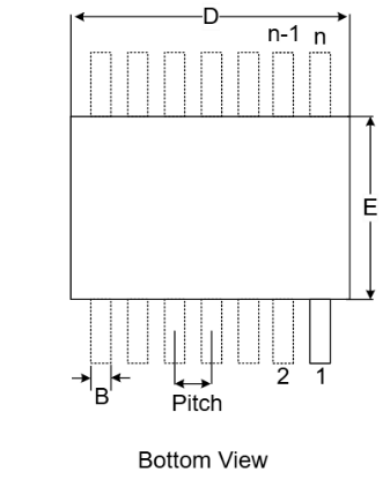
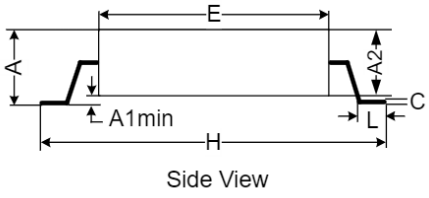
Description	Dimension	Value (mm)	Diagram[1]
Minimum lead span (horizontal side)	Hmin	4.75	
Maximum lead span (horizontal side)	Hmax	5.05	
Minimum body span (pin1 side)	Dmin	2.95	
Maximum body span (pin1 side)	Dmax	3.05	
Minimum body span (vertical side)	Emin	2.95	
Maximum body span (vertical side)	Emax	3.05	
Minimum Lead Width	Bmin	0.18	
Maximum Lead Width	Bmax	0.27	
Minimum Lead Length	Lmin	0.40	
Maximum Lead Length	Lmax	0.70	
Maximum Height	Amax	1.10	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	10	
Distance between the center of any two adjacent pins	Pitch	0.50	

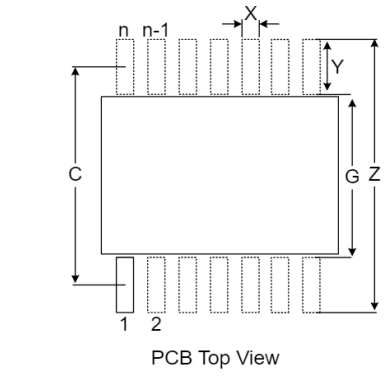
Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram[1]**
Distance between left pad toe to right pad toe.	Z	5.80	
Distance between left pad heel to right pad heel.	G	3.00	
Row spacing. Distance between pad centers	C	4.40	
Pad Width	X	0.29	
Pad Length	Y	1.40	

1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

A.4.4 14-SOIC

IPC Footprint Type	Package Code/POD Number	Number of Pins
SOIC	M14.15/GS0014AB	14

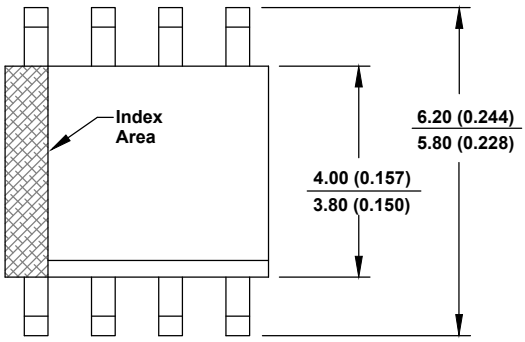
Description	Dimension	Value (mm)	Diagram[1]
Minimum lead span (horizontal side)	Hmin	5.95	
Maximum lead span (horizontal side)	Hmax	6.05	
Minimum body span (pin1 side)	Dmin	8.55	
Maximum body span (pin1 side)	Dmax	8.75	
Minimum body span (vertical side)	Emin	3.80	
Maximum body span (vertical side)	Emax	4.00	
Minimum Lead Width	Bmin	0.31	
Maximum Lead Width	Bmax	0.51	
Minimum Lead Length	Lmin	0.40	
Maximum Lead Length	Lmax	1.27	
Maximum Height	Amax	1.75	
Minimum Standoff Height	A1min	0.10	
Minimum Lead Thickness	cmin	0.19	
Maximum Lead Thickness	cmax	0.25	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	1.27	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram[1]**
Distance between left pad toe to right pad toe.	Z	6.60	
Distance between left pad heel to right pad heel.	G	4.20	
Row spacing. Distance between pad centers	C	5.40	
Pad Width	X	0.41	
Pad Length	Y	1.20	

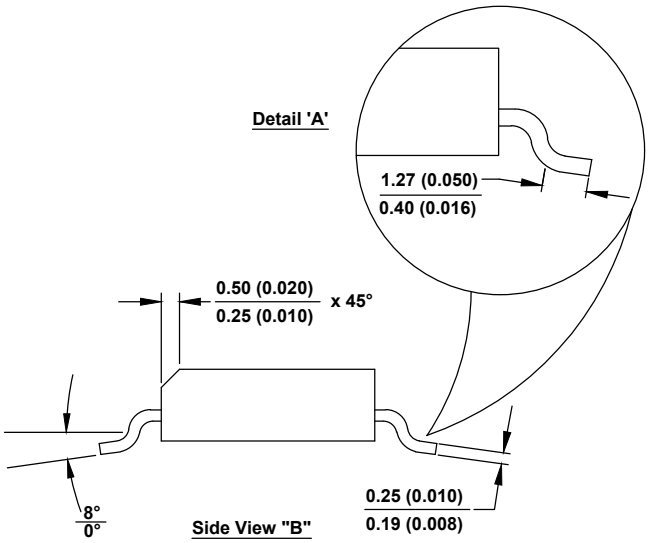
1. The diagrams show table attribute referencing. For the exact diagrams, see the package outline drawing.

Package Outline Drawing

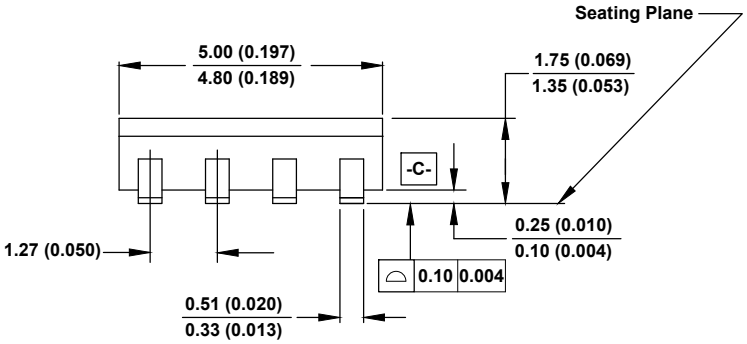
M8.15
GS0008AC
8-Lead Narrow Body Small Outline Plastic Package 4.90 x 3.90 x 1.43 mm Body, 1.27 mm Pitch
Rev08, Jul 7, 2025



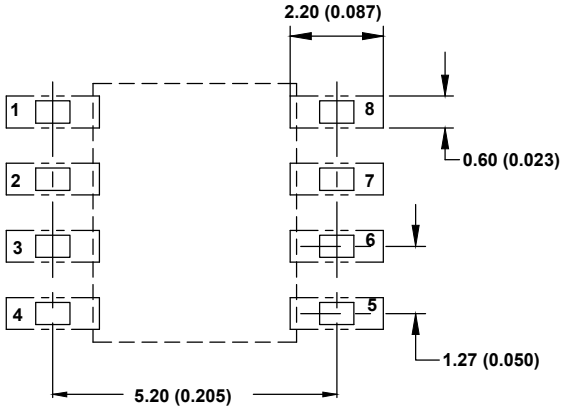
Top View



Side View "B"



Side View "A"



Typical Recommended Land Pattern

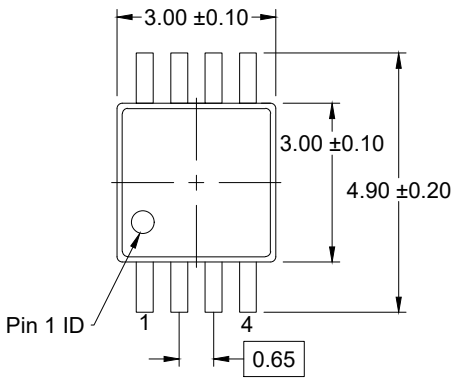
Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

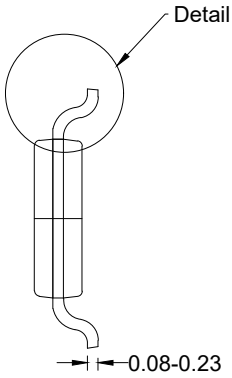
© Renesas Electronics Corporation

Package Outline Drawing

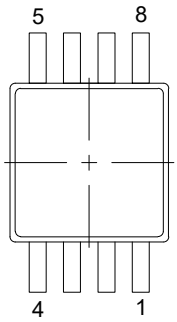
M8.118D
HV0008AC
8-MSOP 3.00 x4.90 x 1.10 mm Body, 0.65 mm Pitch
Rev03, Jul 11, 2025



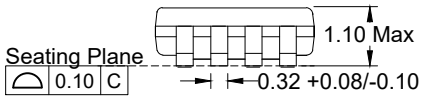
Top View



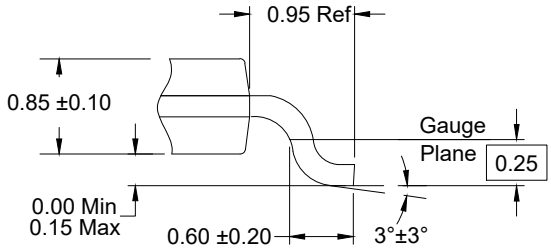
Side View



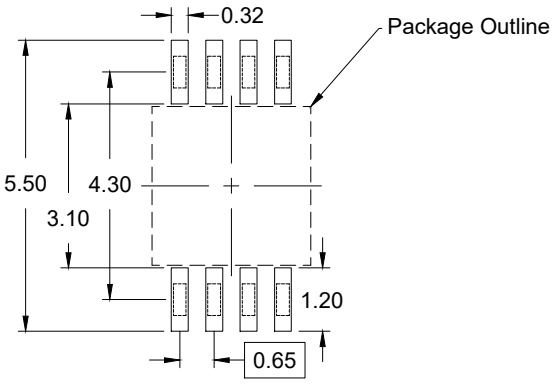
Bottom View



Side View



Detail "X"



Typical Recommended Land Pattern

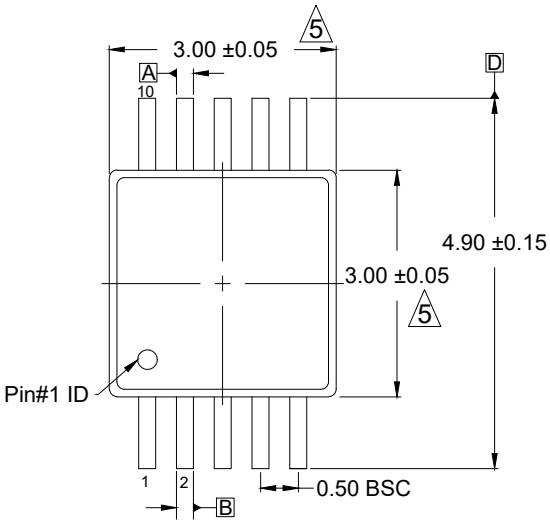
Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

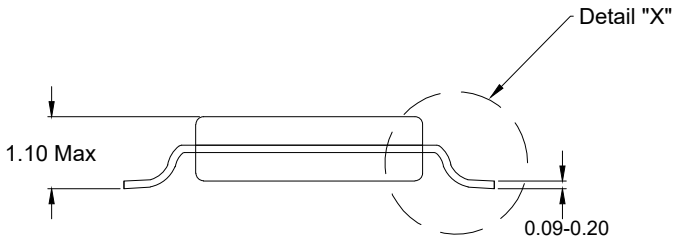
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Package Outline Drawing

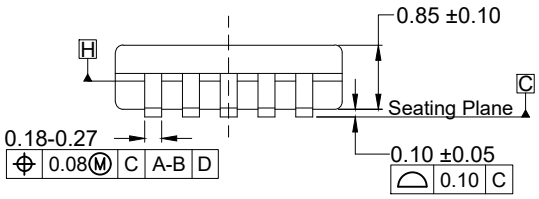
M10.118
HM0010AA
10-Lead Mini Small Outline Plastic Package 3.0 x 3.0 x 1.10 mm Body, 0.50 mm Pitch
Rev03, Aug 21, 2026



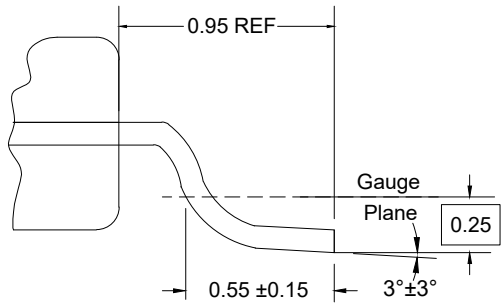
Top View



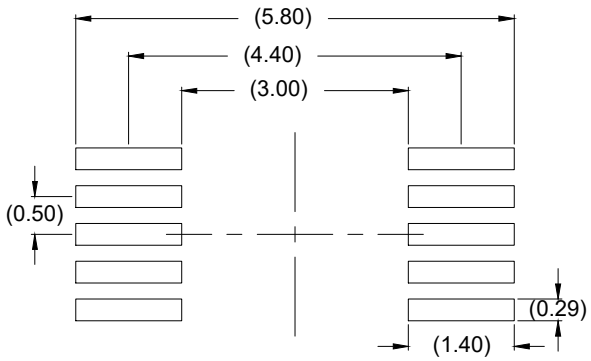
Side View 2



Side View 1



Detail"X"



Typical Recommended Land Pattern

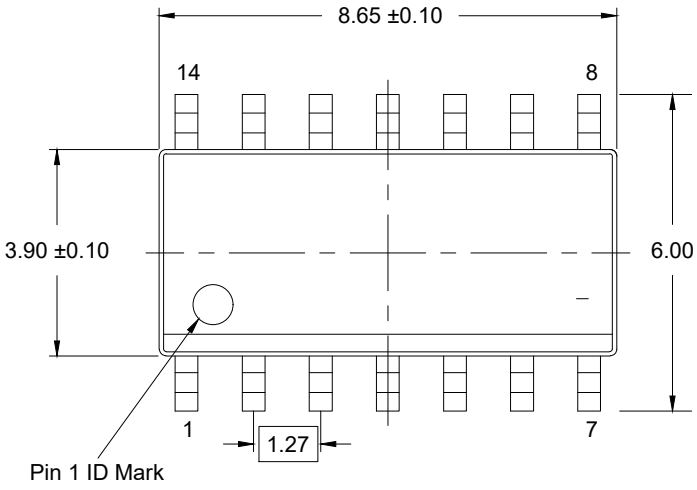
Notes:

1. All Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and ASME Y14.5M-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

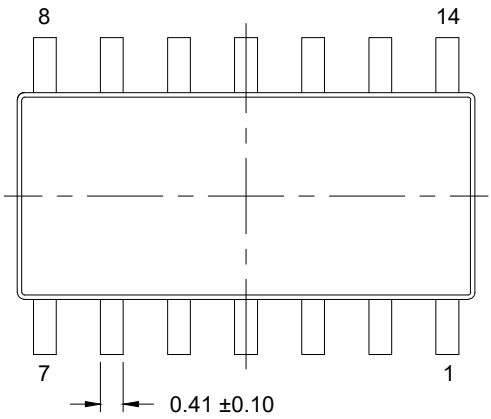
© Renesas Electronics Corporation

Package Outline Drawing

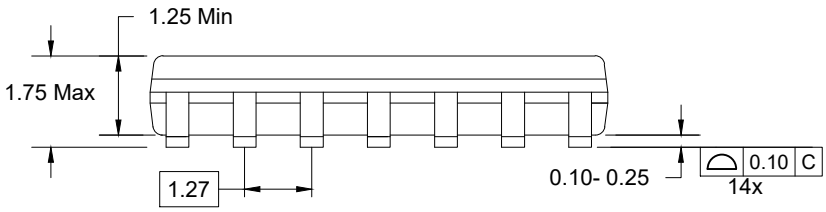
M14.15
GS0014AB
14-SOICN 8.65 x 3.90 x 1.75 mm Body, 1.27 mm Pitch
Rev03, Jun 26, 2025



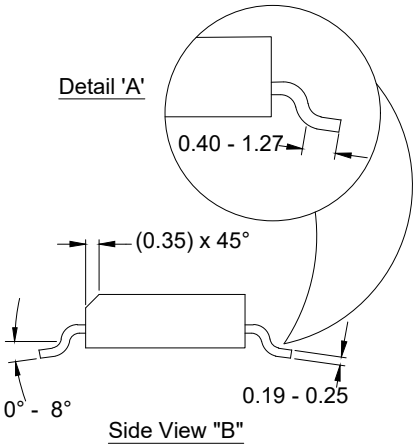
Top View



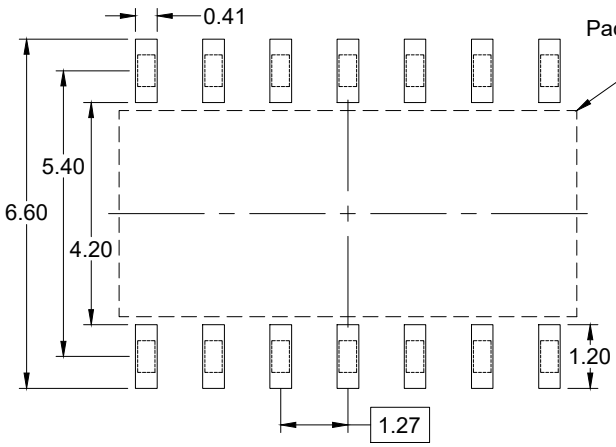
Bottom View



Side View



Side View "B"



Typical Recommended Land Pattern

Notes:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

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